WAFER BONDING OF GaAs, InP, AND Si ANNEALED WITHOUT HYDROGEN FOR ADVANCED DEVICE TECHNOLOGIES

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In this paper we report on the direct bonding of compound semiconductors and silicon annealed at low temperatures (400°C) using hydrogen and nitrogen. Pressure and temperature relationships on interface characteristics were investigated with high resolution transmission electron microscopy and energy dispersive x-ray spectroscopy. It was found that no morphology differences existed between hydrogen and nitrogen annealed samples. Applying our N_2 bonding process, 850nm bottom emitting vertical cavity surface emitting lasers (VCSELs), were bonded to a transparent AlGaAs substrate. Finally, high anneal temperatures (up to 450°C) and shear stress values (>1.6MPa) were obtained for GaAs bonded to Si using a dry (plasma) activation technique.

INTRODUCTION

In many applications the driving force for a suitable direct bonding method between non lattice matched systems is because low dislocation density compound semiconductors are not readily grown on silicon. In addition, the thermal budget required for fabrication of devices on silicon is often much higher than most compound semiconductor process temperatures. Therefore, it is also desirable to have partially or fully completed devices which can be bonded to obtain heterogeneous integration. To date, lasers on silicon (1), doubly stacked GaAs-InP based lasers (2), and other heterogeneous devices have been fabricated using wet chemical activation pretreatment and hydrogen annealing. Research and development efforts continue for applications involving heterogeneous materials for advanced devices and integration of technologies. The current investigators in this field use a hydrogen ambient during annealing, purportedly for the elimination of oxides at the interface and we felt that this deserved further study. The first goal of this work was to investigate the necessity of hydrogen annealing and temperature-pressure conditions for compound semiconductor wafer bonding. An issue is the lowering of temperatures needed for strong bonding and/or

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increasing the initial bond strength such that higher anneal temperatures can be tolerated for heterogeneous bonds in advanced device technologies. The second goal was to demonstrate a novel device employing bonding which can not be fabricated on one substrate. Finally, we examined bonding compound semiconductors to silicon. This paper discusses our current research on GaAs, InP, AlGaAs, and Si heterogeneous wafer bonding with the emphasis on realizing true optoelectronic integration without the use of hydrogen annealing.

EXPERIMENT

InP and GaAs were bonded under ambient conditions using a 20 second pre-clean with $NH_4OH:H_2O$ (1:20). Both plasma activation (3) and sulfur surface passivation were used. After drying, the pieces were placed face to face where they were contact bonded and put into a graphite screw clamping fixture. These samples were annealed in a purged horizontal furnace at various temperatures for 2 hours. Hydrogen annealing was implemented in a vertical MOCVD chamber. The effects of the ambient atmosphere on the interfacial properties have been examined using hydrogen, nitrogen, and wet nitrogen during annealing. The temperature and pressure of the anneal was optimized to minimize the interfacial defect density. Interface inspection was carried out by cross-sectional HRTEM and EDX spectroscopy.

Using the N_2 bonding process described above, top emitting GaAs based VCSELs (850nm) wafers were bonded to transparent, $Al_{0.08}Ga_{0.92}As$ substrates to form bottom emitting VCSEL arrays. Device characteristics were measured on VCSELs from the same wafer for bonded (bottom emitting) and non-bonded (top emitting) devices..

GaAs and InP was bonded to Si using both wet ($NH_4OH:H_2O$) and dry (plasma) activation techniques. For this study die sized pieces as well as whole wafers were used. GaAs bonded to Si wafers were annealed to 450°C for 65 hours and cut into 3x4mm die. The die were subsequently subjected to shear testing and backside thinning.

RESULTS AND DISCUSSION

For bonding of InP/GaAs, no interfacial oxide has been detected for any of the gases used in the anneal, and no oxygen signals above the minimum detection limits of EDX were found, even using wet N_2. The GaAs-InP interfaces examined after annealing at 400°C, N_2 (as in figure.1) and H_2 annealed structures were identical. Intimate atomic contact was observed with a 3-5 monolayer thick disordered interface region. Under higher bonding pressure and temperatures (600°C), voids appeared in samples annealed

in dry N_2 and phase segregation occurred when wet N_2 anneals were used see figures 2 and 3, respectively. EDX measurements of the large (>50nm) triangular inclusions in figure 3 give a composition of $In_{0.56}P_{0.03}Ga_{0.07}As_{0.34}$. Anneal temperatures below 400°C did not provide sufficient strength to survive the sawing procedures used in the TEM preparation. This was true even when using alternative surface activation techniques such as dry plasmas and sulfur passivation.

With our low temperature (400°C) inert gas bonding process just described for the InP/GaAs system, it was possible to bond VCSEL's to AlGaAs substrates resulting in the first wafer bonded 850nm transparent substrate bottom emitting lasers (figure 4). The many grown layers needed to fabricate the distributed Bragg reflection mirrors and active layers leave a rough surface incapable of contact bonding but intimate atomic bonding was achieved after anneal. Again, we were not able to bond below 400°C and this set our lower temperature limit for bonding GaAs based materials. A comparison of device characteristics are given in figure 5, where top emitting (non-bonded) lasers are compared to the bottom emitting (bonded) lasers, both devices are from the same prefabricated VCSEL wafer. The threshold current is lower for the top emitting VCSEL, due to lower mirror loss from the higher reflectivity of the semiconductor/air interface. Although the threshold voltage of the bonded VCSEL is lower, its differential resistance is higher (85 compared to 53 ohms). This is most likely due to the disordered bonded interface and/or substrate resistance. Finally, the output power is reduced for the bottom emitting VCSEL because of absorption in the AlGaAs substrate.

The bond strength of GaAs bonded to Si using a wet pre-treatment was insufficient for annealing above ~180°C due to differential thermal expansion, with or without applied pressure. From the previous discussion, this temperature is not high enough to realize GaAs based wafer bonding. However, with an insitu plasma treatment(3), whole wafers of GaAs bonded to Si can be annealed up to 450°C for as long as 65 hours without the addition of pressure due to the increased bond strength of plasma activation. This temperature falls inside the minimum annealing temperature required for GaAs/InP bonding, as mentioned. Figure 6 shows an IR photograph of a 2" GaAs wafer bonded onto a 4" Silicon wafer after a 300°C, 4 hour anneal. After subsequent annealing to 450°C, shear tests on the isolated die produced a failure stress in excess of 1.6 MPa with a three-dimensional mode of failure. This is nearly four times that reported for a similar study of InP bonded to Si (4). These same die withstood backside lapping of either the Si or the GaAs to approximately 50μm, at which point the thinned material would break up into small fragments. We attribute this failure to the large residual interface stress resulting from differential thermal expansion between the two materials. TEM preparation encountered similar difficulties. We propose that the sharp edges and corners act as crack intensifiers and lead to premature crack-propagation failure in this highly strained system. Further work on bonding GaAs to Si is currently in progress.

CONCLUSION

In summary, we report a low temperature, inert gas, N_2 anneal, bonding process suitable for bonding various compound semiconductors. The first wafer bonded 850nm bottom emitting VCSELs fabricated using our inert bonding process and device characteristics were presented. Finally, preliminary work on bonding compound semiconductors to Si was described. The results of this work shows promise for future heterogeneous material advanced device technologies.

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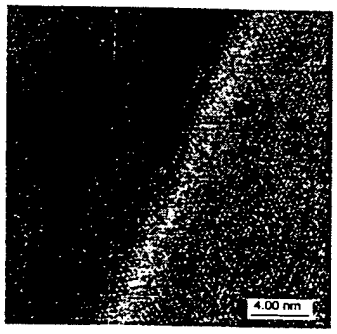

Figure 1. Cross-sectional TEM of GaAs/InP interface for 400°C, N2 annealed sample. Identical results were obtained for H2 annealed specimens.

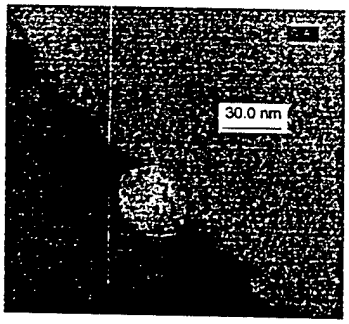

Figure 2. Cross-sectional TEM of GaAs/InP interface for 600°C, dry N2 annealed sample, showing voids in the interface.

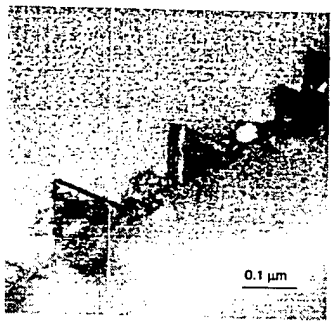

Figure 3. Cross-sectional TEM of GaAs/InP interface for 600°C, wet N2 annealed sample, showing triangular inclusions of InAs ($In_{0.56}P_{0.03}Ga_{0.07}As_{0.34}$.).

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