New Trends in the Commercial IC Industry and The Impact on Defense Electronics

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ABSTRACT

The unprecedented rate and scope of change in the commercial microelectronics industry presents a significant challenge to, and a significant opportunity for, achieving affordable superiority in defense electronics. A proactive approach to making the industry inherently more leveragable is discussed.

INTRODUCTION

Defense microelectronics is inexorably linked to the commercial semiconductor industry. This is obvious in the case of COTS (Commercial Off the Shelf parts) and MOTS (Modified - e.g., upscreened - Off the Shelf parts) as these parts are produced by the commercial industry. However, even captive defense integrated circuit (IC) lines building specialized parts are being forced by their dependence on a commercial-industry-driven supplier base to follow commercial product/process/design trends.

The just released 1997 version of the Semiconductor Industry Association (SIA) National Technology Roadmap for Semiconductors (NTRS) describes the unprecedented changes occurring in the commercial industry. As shown in Figure 1 (and discussed in more detail below) the industry is evolving from a more stable pre-1994 technology evolution to a discontinuous post-1997 technology evolution.

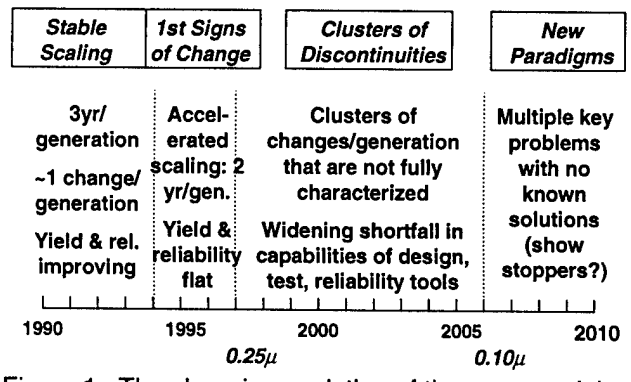

Figure 1. The changing evolution of the commercial industry

The purpose of this paper is to discuss how these changes present both major challenges and major opportunities, for defense microelectronics, especially for applications involving long lifetimes, harsh environments and/or high consequences of failures.

TRENDS IN THE COMMERCIAL INDUSTRY

The commercial industry is driven by desire to continue its 15% per year growth that results from staying on Moore's Law (28% per year reduction in cost per transistor). As shown in Figure 2, Moore's law is enabled by the superposition of a number of areas of improvement including feature size shrinking, increasing wafer size, higher yields, and "other" (including improved equipment productivity). However, since 1994 the mix has changed. The rate of feature size shrinkage has increased over historic levels to compensate for reductions in yield and "other" improvements. The historic three years between technology changes (e.g., 0.35 to 0.25 μm feature sizes) has been reduced to two years or less.

Moore's *second* law is that the cost of a new mainstream commercial fabrication plant doubles with each new generation of technology. By the

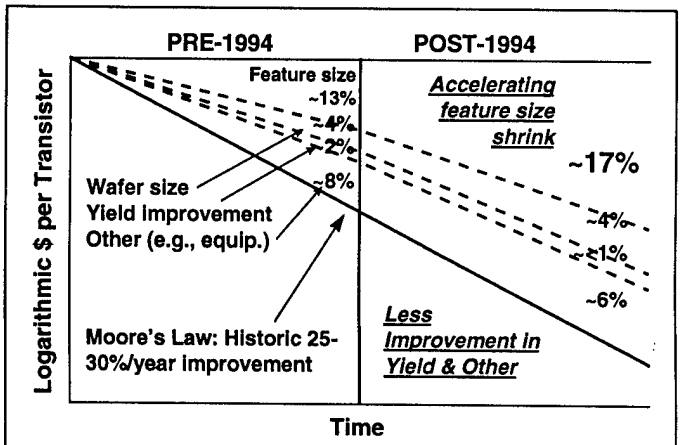

Figure 2. Change in contributors to Moore's Law (After Jim Owens, Sematech)

DISCLAIMER

year 2005, a plant designed for a 0.10 μm technology is projected to cost ten billion dollars. Furthermore, the minimum economically viable number of wafer starts per month goes up with each new technology node. These economics drive the commercial industry to focus on even larger volume customers.

Scaling of dimensions and voltages continues relentlessly as shown in Table I. One consequence of scaling is that parts will become less robust.

TABLE I
Scaling of Key Attributes in '97 NTRS
(Leading-edge Logic Products)

ATTRIBUTE	1997	2006
Feature Size (μm)	0.25	0.10
# Transistors/cm2 (M)	3.7	839
# Wiring Levels	6	7-8
Supply Voltage (V)	1.8-2.5	0.9-1.2
Gate Ox. Thick. (nm)	4-5	1.5-2
1st. Year Yield (%)	90	75

Two of the major approaches to screening out defective parts will be seriously impacted by scaling. Scaled parts will have a reduced ability to operate at higher temperatures (and at higher gate oxide electric fields) limiting the ability to perform dynamic burn-in. The fact that subthreshold leakage does not scale will lead to an increase in off-state leakage currents which will reduce the effectiveness of Iddq testing.

One of the major discontinuities and risks facing the industry is illustrated in Figure 3. Historically, the industry has recognized that "no change is a small change" and has been very conservative in the adoption of new materials which occurred at the rate of one per generation. However, as the evolution of the technology runs up against material limits, future generations of technologies will introduce not one, but clusters of new materials per generation. Furthermore, past experience has suggested that it can take up to a decade to fully characterize the impact of a new material. These clusters of new materials are significantly less well characterized than previously introduced new materials.

Among the most significant of the material changes are the introduction of Cu interconnect (starting in 1999), lower dielectric constant interlevel dielectrics (shortly thereafter) and new gate dielectrics (~2006). While these new materials look promising, they present the risk on new failure modes that may not be uncovered until they are in volume production or until they are in the field for several years.

Mainstream commercial parts are typically characterized for 10-year life and warranted for 1 year. There is pressure to trade off "excessive" end-of-life reliability safety margins for increased performance.

The impact of all these changes has been that failure rates, which had been decreasing prior to 1994, have leveled off since then as indicated in Figure 4. There is a concern that with all the changes coming up, especially the adoption of new materials, the failure rate may increase during future technology changes. Furthermore, as seen in Table I new technologies will be introduced with lower initial yields. These higher

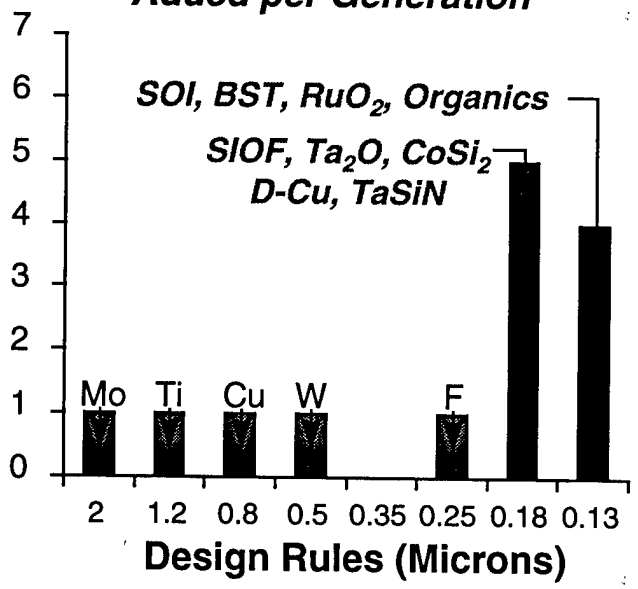

Figure 3. Future generations of technology will introduce an unprecedented number of new materials (after Jim Owens, Sematech)

defect levels will result in more early life failures (a rule of thumb is that 1/100 to 1/500 of all yield failures will be early field failures.)

There are similar challenges in scaling and new materials introductions in advanced packaging. There will be a stronger interaction between the package and the die. Thermal management, stresses, and handling high frequency signals will be major packaging challenges. The move to flip chip will present major failure analysis challenges requiring the development of backside analysis techniques.

IMPACT ON DEFENSE MICROELECTRONICS

The evolution of the commercial industry is targeted at a mainstream high volume marketplace. To first order, this marketplace requires very large volumes of a relatively smaller number of standard parts to be used in systems in an office-like environment in products that will become obsolete in 5 years. The emphasis is on initial quality and early (1-year) failure rates.

For defense applications that mimic this benign application (perhaps through mitigation at the system level), and which can live with 1-year part warranties, the evolution of the commercial industry is very good news. These applications will have access to devices with increasing performance, expanded functionality and a decreasing cost per function.

However, there are critical defense applications that are different from the mainstream commercial applications due to:

⇒ longer lifetimes

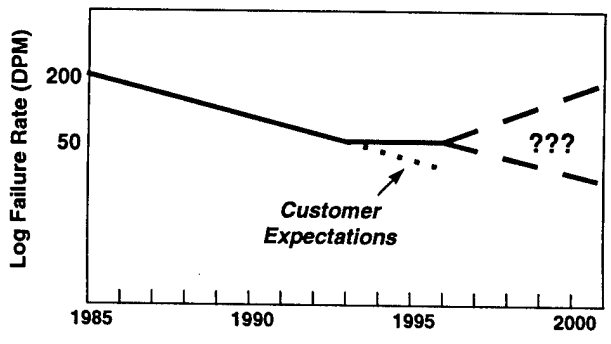

Figure 4. Average 1st year reliability vs. Time (Source: Sematech Reliability Roadmap)

⇒ harsher environments

⇒ higher consequences of failure

For these applications the evolution of the commercial semiconductor technology presents considerable challenges.

Scaling and reduced reliability margins will make commercial parts less usable outside of commercial specifications. For example, commercial parts will have reduced margins for junction leakage currents and threshold voltage variations, which will reduce their ability to operate at higher temperatures.

In general, the radiation hardness of COTS integrated circuits (ICs) will decrease when technology scales into the deep sub-micron regime. Smaller feature sizes and higher integration densities will require new design and process techniques to mitigate the degrading effects of ionizing radiation in both terrestrial and space applications. In addition, reduced operating voltages and low-power requirements will introduce new physics and complex failure modes for ICs operating in these radiation environments. The primary radiation threats of concern are: (1) total-ionizing dose leading to increases in leakage currents and timing delays, and eventually to device failure; (2) transient (or high-dose-rate) radiation that results in large photocurrents on the surface of the chip causing logic upset, latchup, burnout, and/or catastrophic failure; and (3) single-event phenomena leading to "soft," temporary upsets and/or "hard," permanent failures. Perhaps the most serious threat as defined in the National Technology Roadmap For Semiconductors is the single-event or "soft error" problem in which an energetic neutron or proton (found in abundance in space or on the surface of the Earth) can cause a temporary upset of an IC. With scaling comes reduced charge per logic state and thus increasing susceptibility to SEU.

Screening devices to improve reliability or to use ICs in environments beyond the commercial specs will also become more difficult. The fact that the subthreshold leakage does not scale will mean that Iddq testing will be less effective in finding latent or hard defects. Furthermore, scaled devices may not be able to operate

through the high temperatures of burn-in or the high voltages of wafer level screens.

Decreasing robustness and the focus of the commercial industry on large volumes of standardized parts will lead to a continued, and perhaps growing, need for custom fabs for high value specialty parts. Increasing process complexity and cost are challenges that need to be faced in order for custom fabs to pace the more rapid evolution of commercial technologies.

The new materials present special risks for defense applications. Cu is a highly diffusive species, which, if not contained, can degrade products, such as increasing junction leakage. Defense applications that involve longer lifetimes and/or higher temperatures will be most at risk. Similarly, longer lifetimes, higher temperatures and/or radiation environments have the potential to degrade the mechanical or electrical stability of lower dielectric constant interlevel dielectrics. The switch away form SiO_2 to a high dielectric constant material could impact a number of critical properties, including radiation hardness. These new materials are not fully characterized for the more benign mainstream environments and present an even greater risk of new failure modes in special defense applications.

The move to systems-on-a-chip and integrated microelectronic/micromechanical products will present an even greater level of challenges due to interactions between technologies (see www.mdl.sanida.gov/Micromachine).

Finally, the mismatch between long defense systems development cycle and commercial cycle times will widen as the industry moves from 3 to 2 years between technology nodes. Future commercial products will be more complex, aggravating the sunset technology problem.

A STRATEGIC APPROACH

Defense microelectronics has moved from a proscriptive Mil Specs approach to a more passive, reactive approach to leveraging. This places increased reliance on system developers. This approach will probably not lead to superiority in light of the changes described in this paper and due to the easy worldwide access to advanced semiconductor products.

We are more likely to succeed with a more proactive, strategic program to be the first and best at leveraging advances in the commercial industry for defense applications. The goal should be to a differentiated ability to make the industry inherently more leveragable for COTS, MOTS and custom products/captive fabs.

Inherent leveraging can be achieved by focusing government R&D on those dual-benefit areas that improve leveraging. For example, development of reliability and failure analysis technologies help meet critical mainstream commercial needs while at the same time providing the knowledge of failure modes required for defense applications.

The government microelectronics community needs to stay closely coupled with the commercial industry through participation in national committees, roadmapping, etc. A more detailed study of the implications of commercial trends on defense applications should be conducted for the '97 and all future NTRS. The synergism between defense and other critical electronics applications needs to be exploited (see www.sandia.gov/eqrc/cichome.html).

Now is the time to lay the foundation for defense insertion of emerging commercial microsystems-on- a- chip that integrate electronics, sensors and micromachines.

Finally, a commercial leveraging enabling center should be established as a bridge between the commercial and defense communities. The escalating change, complexity and costs of the infrastructure required to support successful insertion of commercial technologies will outstrip the capabilities of most government programs and contractors. The center should be a nexus for R&D programs aimed at leveraging and should provide the defense community with access to the detailed information and advanced engineering capabilities required for successful, affordable insertion of advanced technologies.

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