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Thermal Tests of MC3811 Rigid/Flex Printed Wiring Boards

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Abstract

Rigid/flex multilayer printed wiring boards are more sensitive to thermal environmental changes than conventional printed wiring boards. This is manifested because of a composition of dissimilar materials used within the construction of this type of product. During fabrication and assembly, stresses can develop within the plated-through holes from differences in thermal properties of the rigid and flexible materials, primarily thermal coefficient of expansion. Thermal shock and thermal stress tests and rework simulation as defined in MIL-P-50884 have been performed in this study as indicators of processing quality to detect faults and to verify improvements in board reliability.

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Acknowledgment

The work reported in this document was conducted by C. W. Jennings, who has since retired from Sandia National Laboratories. This report is a summation of his unpublished results from testing early MC3811 rigid/flex product before production.

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Summary

Thermal shock testing, which has been devised to evaluate resistance to aging, consists of cycling a printed wiring board between temperature limits for designated intervals until a given number of cycles is reached or failure occurs. Failure is indicated when the electrical resistance of a monitored circuit rises above some designated level, frequently 10%. Thermal stress testing, which is used to measure resistance to degradation in a soldering environment, consists of floating a test coupon or section of a board on a molten solder surface at 288°C (550°F) for 10 s. The specimens are cross sectioned and examined microscopically for defects generated by this treatment. Rework simulation, which is also related to soldering, consists of soldering and unsoldering a wire in a plated-through hole (PTH) five times and then examining the hole visually and in cross section for any damage.

Cross sections of board specimens taken after thermal shock and thermal stress were examined at 100 to 500X magnification for barrel cracks and for inner-layer conductor separation. The most important variable affecting cycle life for any of the boards was found to be the high- and low-temperature limits or temperature span to which the board is exposed. Higher failure rates are observed when cycled from −65°C to +125°C than when cycled from −55°C to +105°C. The worst-case temperature span expected for the MC3811 is only −20°C to +80°C. With this span, >1000 cycles were run, with <10% change in resistance.

Weight-percent moisture absorption in MC3811 boards was obtained from measurements before and after they were subjected to different humidity environments. The release of absorbed moisture as steam during soldering or other high-temperature excursions can be very damaging to the physical state of a board or laminate. Steam pressure can be generated rapidly in the material surrounding the PTH and can lead to barrel cracking or inner-layer conductor separation.

The thermal stress and the thermal shock were proven to be discriminating tests to judge the reliability of a plated-through hole. The thermal stress simulates the soldering operation, while the thermal shock can be used to qualitatively estimate the lifetime of a board in its end-use environment. Both tests can be used to indicate quality for the materials and fabrication operations and to assess the effect of any changes on board reliability. The pass or failure criterion for thermal stress is the presence or absence of barrel cracks or a separation gap between the inner-layer copper conductors and the wall of the PTH. For thermal shock, there is an additional requirement that one or more test circuits do not change in electrical resistance by some specified value after 100 cycles between upper and lower temperature limits. This value is usually 10%.

Thermal Tests of MC3811 Rigid/Flex Printed Wiring Boards

Introduction

Printed wiring boards (PWBs) made with combinations of rigid and flexible materials offer possibilities for lighter and smaller electronic assemblies that can cost less and have fewer wiring errors than conventional PWB assemblies. Problems can, however, arise when a rigid/flex (RF) PWB is subjected to a change in thermal environment that could occur in processing, testing, or field use. The problems are related to stresses that can develop from the differences in thermal properties of the rigid and flexible materials, primarily thermal coefficient of expansion (TCE).

This report is concerned with the effect of thermal stresses on the electrical functionality of the rigid/flex board in the MC3811 programmer. This board is shown in Figure 1. A breakdown of the material composition is seen in Figure 2. The details of board fabrication have been reported by F. L. Gentry, Printed Circuit Division 7413.[1] It should be noted, however, that all this work was done before 1988. Much additional work has since been done and will be reported in a separate document.

The RF/PWBs were exposed to three different thermal environments: (1) thermal shock, (2) thermal stress, and (3) rework simulation. The details of these tests are given in MIL-P-55110D, MIL-P-50884, and SS379453. *Thermal shock*, which has been devised to evaluate resistance to aging, consists of cycling a board between temperature limits for designated intervals until a given number of cycles is reached or failure occurs. Failure is indicated when the electrical resistance of a monitored circuit rises above some designated level, frequently 10%. *Thermal stress*, which is used to measure resistance to a soldering environment, consists of floating a coupon or section of a board on a molten solder surface at 288°C (550°F) for 10 s. The specimens are cross sectioned and examined microscopically for defects generated from this treatment. *Rework simulation*, which is also related to soldering, consists of soldering and unsoldering a wire in a plated-through hole (PTH) five times and then examining the hole visually and in cross section for any damage.

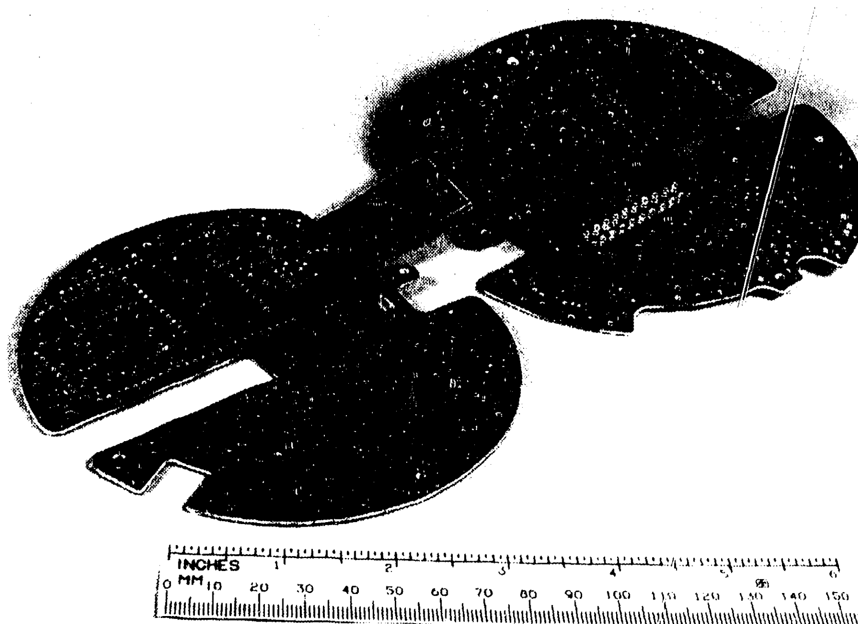


Figure 1. MC3811 Rigid/Flex Printed Wiring Board

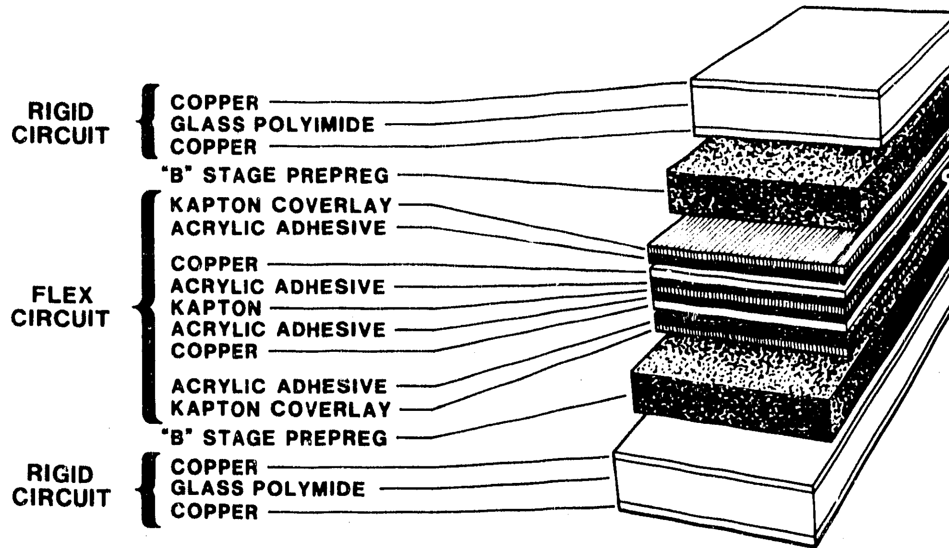


Figure 2. Rigid/Flex Material Stackup

Most of the testing was carried out with thermal shock, and to a lesser extent, thermal stress. Little rework simulation testing was carried out because it is a destructive test, and it is difficult to maintain the desired degree of reproducibility. Thermal shock, which is thought to be the most discriminating of the tests, has been adopted as a general test to predict potential fatigue and other problems on products that are expected to have a long reliable life even in adverse thermal environments. It is also being used as an indicator of processing quality and as such has been valuable in detecting faults and showing areas for improvement in board reliability, especially with respect to PTHs. Barrel cracks (BC) and inner-layer conductor separation (CS) in PTHs (Figures 3 and 4) have been observed in development boards that failed after only a few thermal cycles. No direct correlation between thermal shock and thermal stress has been reported.

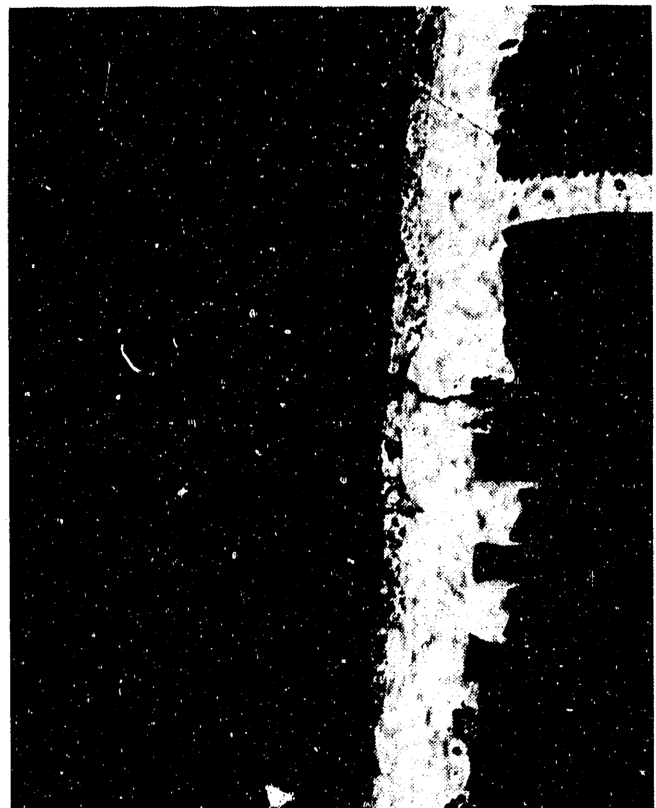


Figure 3. Example of a Barrel Crack

Figure 4. Example of Conductor Separation

The RF/PWB specification, SS379453, specifies thermal shock testing in accordance with MIL-P-202, Method 107, to the test conditions (thermal limits) specified on the product drawing. The boards or test specimens are subjected to a high- and low-temperature extreme for a minimum dwell time of 15 min (maximum of 17 min). Normally this is done in a two-chamber test system. Transfer time between temperature chambers is to be such that the specified temperature is reached within 2 min after the specimen has been transferred from one chamber to another. After completion of a designated number of cycles, a test for electrical resistance change is performed by comparing the initial and final measurements at the same temperature. Electrical resistance change of 10% or more was considered a failure for this investigation. Visual and cross-section examinations are made of the cycled specimens.

Three circuits of the MC3811 board that contained 7, 12, and 19 holes in series were monitored in thermal shock testing. A circuit with an open or a high-resistance change was probed electrically to determine the source of the change, usually in a PTH. Most of the boards tested came from an Allied-Signal, Kansas City Division (KCD), lot that had some holes drilled in incorrect locations not associated with the circuits being monitored. The remainder came from developmental orders from Litronics and SNL as identified in Table 1.

Results

Table 1 shows the largest percentage resistance change of the three circuits after 100 cycles and the cycles to failure for boards with different materials and processing. A breakdown by circuits is shown in Table 2. Cross sections of board specimens taken after thermal shock and after thermal stress were examined at 100 to 500X magnification for barrel cracks and for inner-layer conductor separation. The presence of faults such as shown in Figures 3 and 4 is noted in Table 3. Boards from the misdrilled lot, A through K, show qualitative board-to-board comparisons and the effect of changes in testing variables.

Table 1. Percentage Resistance Change and Number of Cycles to Failure

Board Source	Board Designation	Temp (°C)	Wt Change After Cycling (%)	100 Cycles Max Δ R (%)	Min No. Cycles to Failure	Avg Hole Cu Thickness as Rec'd (mil)	Thickness Tolerance (Sigma) (mil)	Notes
KCD	A	a	−0.60	5.1	146	2.58	0.29	
(Misdrilled	B	a	−0.50	4.2	146	2.25	0.17	
Lot)	C	a	−0.56B	4.0	146	2.37	0.14	
	D	a	−0.55B	3.2	146	2.63	0.29	
	E	c	−0.02	<1	1011	2.42	0.29	
		c+d	−0.77B	<1	1011			
	F	c	+0.01	<1	1011	2.56	0.21	
		c+d	−0.04	<1	1011			
	G	a	−0.55	5.3	150	2.47	0.24	(Leads in holes)
	H	a	−0.56	8.5	150	2.42	0.27	(Leads in holes)
	J	b	+1.24H	<1	187	2.33	0.29	(H at start)
			to −0.48					
	K	b	+1.23H	<1	450	2.51	0.14	(H at start)
			to −0.48					
Litronics	L1	a		414	24			
	L2	d	−0.16	1.3	>100	1.67	0.08	
		d+a		1730	50			
	L3	d	−0.67B	>1	>100	1.82	0.10	
		d+a	−0.08	3.1	<154			
SNL	G4	b	−0.22	<1	>1008	2.50	1.34*	
	G5	b	−0.19	<1	>1008	2.50	0.91*	
	G6	b	−0.37	Open	47	2.50	1.31	
SNL	E1	b′	−0.21	<1	>500	1.99	0.41	Barrel cracks†
(Epoxy		b′+a	−0.28	1.2	>500			
Flex)	E2	b′	−0.18	<1	>500	2.39	0.29	
		b′+a	−0.26	<1	>500			
	E3	b′	−0.16	<1	>500	2.38	0.33	Barrel cracks†
	E4	b′	−0.16	<1	>500	0.83	0.22	Barrel cracks†
KCD	N1	b	−0.63	<1	654	3.49	0.26	
	M12	b	−0.42	1.6	>497	3.60	0.31	
	M14	b	−0.42	1.5	>497	4.03	0.38	
SNL	G10	b	−0.32	1.5	>140	3.08	0.19	(Epoxy Flex)
(Epoxy		b+a	−0.23	2.4	>40			
Flex)	G11	b	−0.47	322	50	3.06	0.18	Lamination problems
		b+a	−0.1	Open				
	G12	b	−0.35	<1.	>140	2.81	0.16	
		b+a	−0.26	<1.9	>40			
	G13	b	−0.38	5.9	>140	3.45	0.20	Lamination problems
		b+a	−0.31	37.	<40			

a −65 to +125°C
b −55 to +105°C
b′ −65 to +105°C
c −65 to +25°C
d −20 to +80°C

B = Baked out (125°C for minimum of 16 hr)
H = 100% RH
*No solder or solder mask
†Solder float after cycling

Table 2. Resistance Changes for Individual Circuits

Temperature Cycle (°C)	Board	Percent Resistance Change at 100 Cycles			Cycles at Failure			Notes
		Circuit			Circuit			
		1	2	3	1	2	3	
−65 to +125	A	0.4	5.1	2.6	>292	146	196	
	B	0.8	4.2	1.9	>292	196	146	
	C	0.2	4.0	1.2	>292	196	146	
	D	1.6	3.2	1.1	146	196	146	Baked
	G	1.1	5.3	0.9	>320	150	150	Lead in holes; baked
	H	1.4	8.5	3.5	>320	150	150	Lead in holes
−55 to +105	J	0.3	0.1	0.4	187	450	187	100% RH
	K	0.7	0.9	0.0	450	>544	544	100% RH; then baked at 100°C for 16 hr before testing
−20 to +80	E	0.3	0.3	0.1	>1011	>1011	>1011	
	F	0.2	0.1	0.5	>1011	>1011	>1011	Baked at 120°C 24 hr before testing

Table 3. Thermal Stress Cross Sections

Board	As Received	Solder Float	Solder Float After Cycling
A			*
B			*
C			*
D			*
E			CS
F			CS
G			*
H			*
J			*
K			*
L1		BC	
L2	BC	BC	
G4	*	*	BC
G5	*	CS	*
G6	*	CS	*
E1			BC
E2			BC
E3			
E4			BC
M12			
M14			
G10			
G11			
G12			CS
G13			

BC = Barrel Crack
CS = Conductor Separation
*No BC or CS

The most important variable affecting cycle life for any of the boards is the high- and low-temperature limit or temperature span to which a board is exposed. Compare for example the cycle life of boards A, B, C, D, G, and H with that of J and K. The former were cycled from −65 to +125°C and the latter, from −55 to +105°C. The worst-case temperature span expected for the MC3811 is −20 to +80°C. With this span, >1000 cycles were run, with <10% change in resistance (Boards E and F). Because of the long cycle life with the smaller temperature spans, the temperature limits were frequently increased after 500 or 1000 cycles to induce failure within some reasonable interval of time.

Soldering leads into the circuit holes did not appear to affect cycling life, nor did subjecting the boards to 100% relative humidity before the start of cycling. Substituting Rogers Flexible epoxy (R/Flex 8970) for Pyralux in the flex section had a positive effect in that it lowered resistance changes and increased cycle life. The four boards, E1, E2, E3, and E4, had resistance changes of <1% for 500 cycles between −65 and +105°C (Figure 5) and <3% for E1 and E2 after an additional 500 cycles of −65 to +125°C (Figure 6). However, barrel cracking was observed in cross sections of some of the circuit holes of these boards.

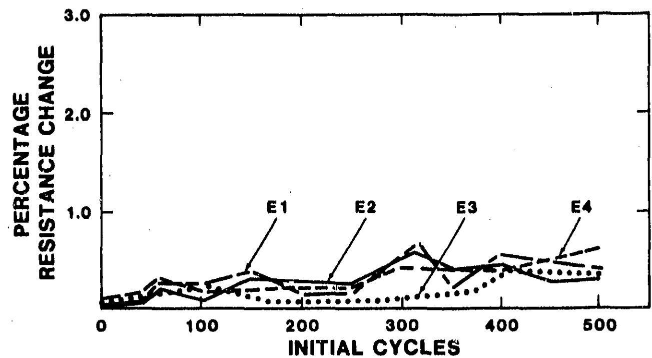


Figure 5. Average Resistance Change for Three Circuits From Boards E1 Through E4 (−65°C to +105°C)

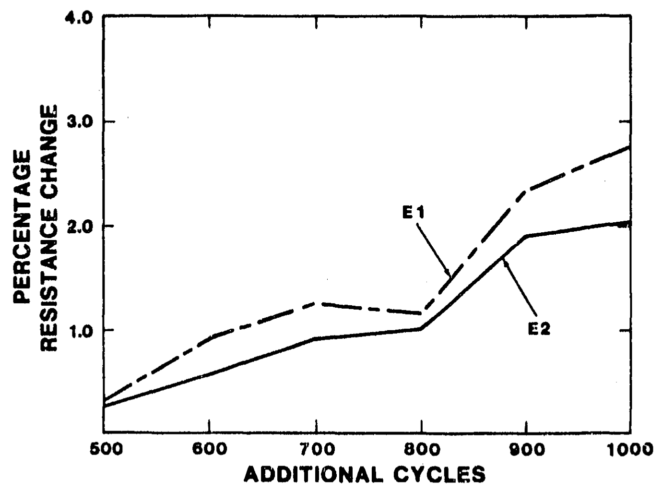


Figure 6. Additional Average Resistance Change for Boards E1 and E2 (−65°C to +125°C)

Weight-percent moisture absorption in MC3811 boards was obtained from measurements before and after they were subjected to different humidity environments. The changes from cycling are given in Table 1. Typical board weights ranged from 50 to 60 g with solder mask coating. Based upon thermal gravimetric analysis (TGA) measurements (Figure 7), it is estimated that the laminate weight is ~60% of the board weight.

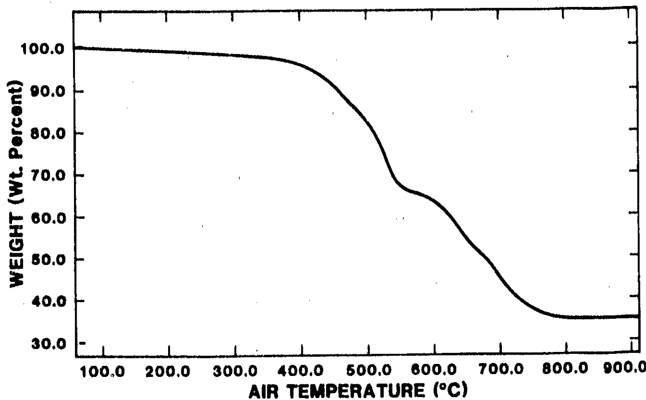


Figure 7. Perkin-Elmer TGA 7 Series Thermal Analysis System

In addition to the weight changes listed in Table 1 for boards that were thermal cycled, weight changes were also obtained in specimens of materials making up the boards following their insertion into wet and dry environments. These changes expressed in weight percent are: epoxy glass, 0.8 to 1.0; polyimide glass, 1.6 to 1.8; Pyralux, 5 to 6; and flexible epoxy, 2.0 to 2.4. The moisture capacity of a material is determined from the weight change at room temperature between a specimen equilibrated at 100% RH and then equilibrated to <1% RH (Drierite desiccant) or from bakeout. J. W. Lula of KCD is studying the time-temperature relationship for moisture removal for rigid/flex materials.[2] Typical equilibration curves are shown in Figures 8 and 9. Weight gains of Pyralux and epoxy adhesive in 100% RH are shown in Figure 10.

The release of absorbed moisture as steam during soldering or other high-temperature excursions can be very damaging to the physical state of a board or laminate. Steam pressure can be generated rapidly in the material surrounding the PTH with a soldering heat pulse. If there are voids in the hole wall, the steam could escape through the void, causing bubbles to form in the solder. If the dwell is short and the cooling rate sufficiently rapid, bubbles could be frozen in the solder. J. Balde and G. Messner have reported that absorbed moisture in a laminate can also affect its dielectric constant.[3]

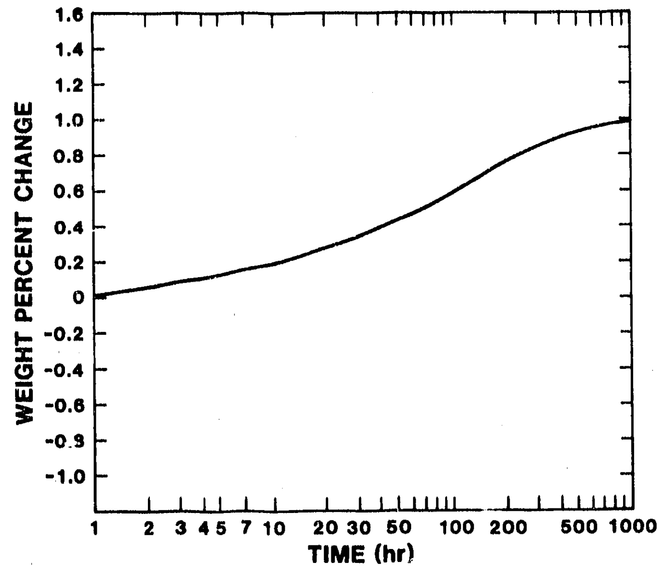


Figure 8. Equilibration of Polyimide-Glass to 100% RH and 100°C

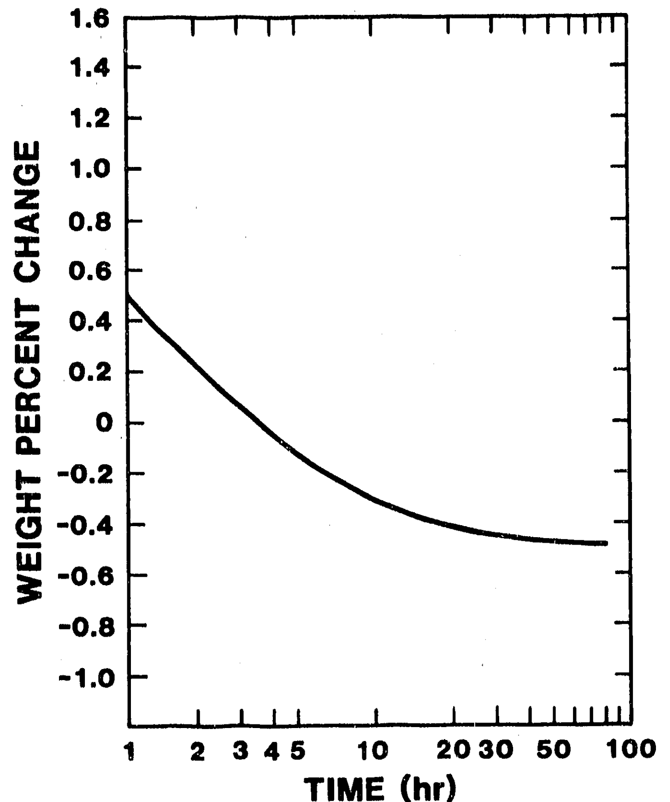


Figure 9. Equilibration of Polyimide-Glass With 100°C Bakeout

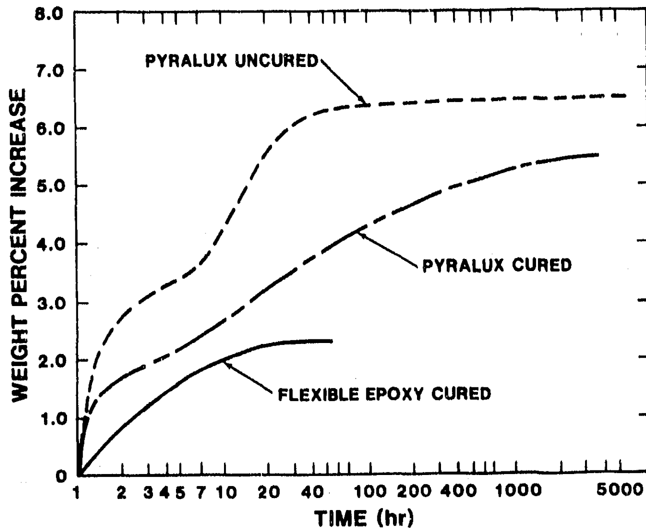


Figure 10. Water Absorption of Pyralux Film and Flexible Epoxy at 25°C and 100% RH

In early testing, boards having PTH walls with >1.5-mil-thick copper had longer cycle lives in thermal shock than those with thinner copper. In subsequent board fabrication, copper plating thickness was adjusted to produce hole walls with 2 or more mils of copper. Average hole wall thicknesses were measured at specified hole locations with a Caviderm CD8. Figure 11 shows variations in thickness with different hole location for KCD- and SNL-fabricated boards. Table 1 lists the average of nine thickness measurements taken at specified locations on each board.

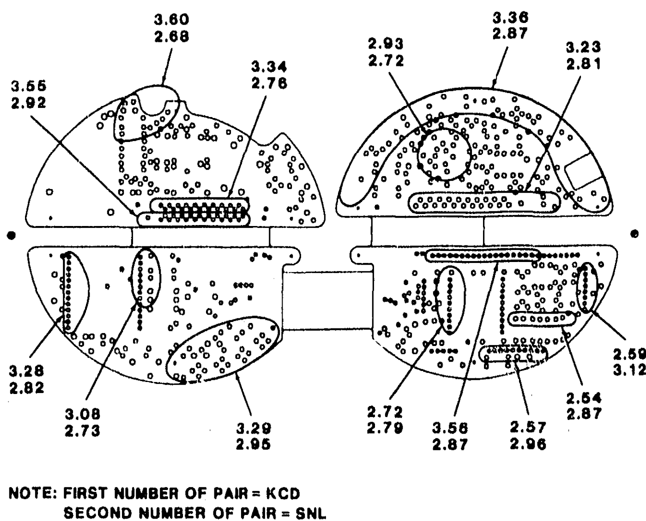


Figure 11. Copper PTH Thickness Distribution Over Board Surface (in mils)

Caviderm measurements made on the same holes before and after thermal shock showed some boards to have an increase in hole resistance corresponding to thinner wall thickness, e.g., <1 mil. These changes were related to barrel cracking seen at higher magnification in hole cross sections. This suggests that a thickness scan to inspect for barrel cracks could be made for a set of PTHs in much less time than is required for microsection examinations.

A barrel crack or inner-layer conductor separation can extend over part or all of a hole wall. For a 360° crack, as intimated in Figure 12, an open circuit or high resistance is expected. A partial crack or incipient crack, as suggested in Figures 13 and 14, may not always be detected by cross section because one sees only a limited fraction of the hole wall. There is probably a threshold circuit resistance change corresponding to crack formation, but this has not as yet been obtained. It is not the 10% change given in the MIL-P-55110.

A crack at a wall to inner-layer conductor interface does not always show up in a continuity test, and sometimes there is intermittent continuity that probably corresponds to the faces of the crack making touching contact. When the current is increased on the board circuits, at some value hot spots begin to appear at high-resistance connections such as a cracked PTH connection. These can be detected with liquid crystal papers or by finger touch. An infra-red camera or other heat-sensing equipment would be needed to better locate the hot spots.

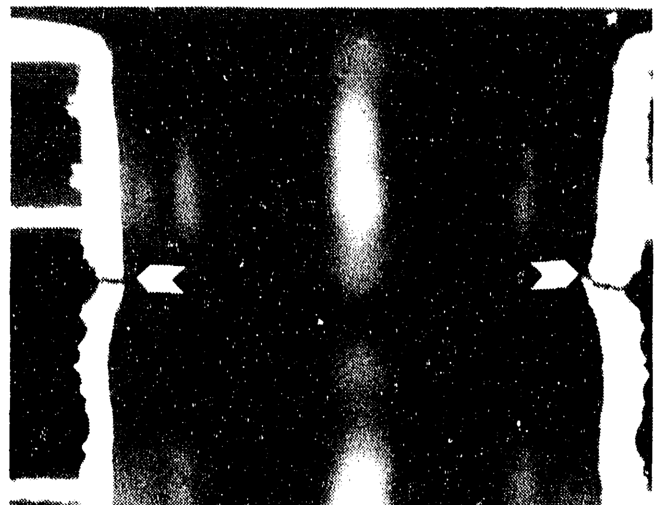


Figure 12. Indication of Possible 360° Cracks

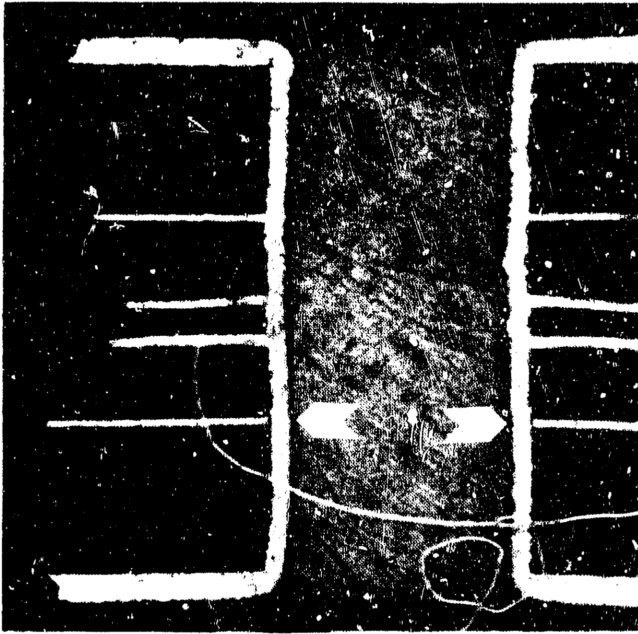


Figure 13. Indication of Inner-Layer Separation

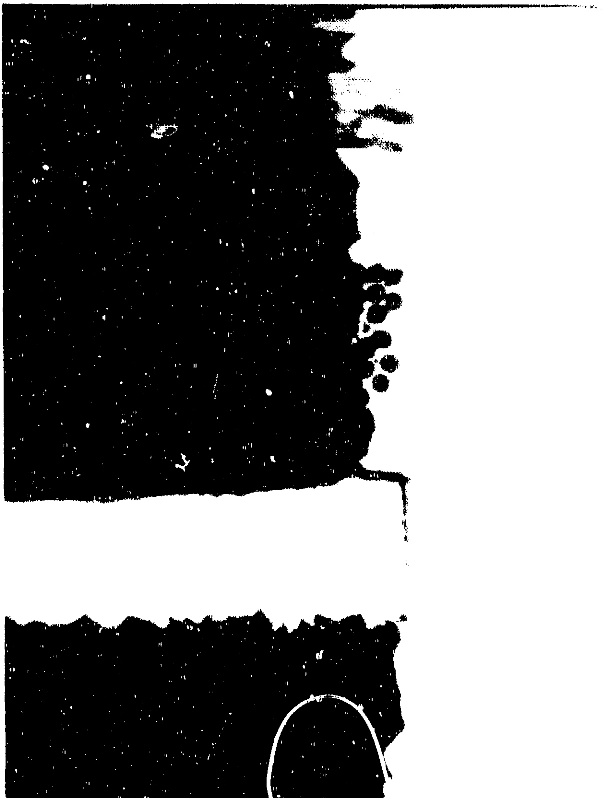


Figure 14. Crack Initiation at Hole Wall/Inner-Layer Conductor Interface

Thermal Stress

Because this test is destructive, most of the testing was done with specimens from boards after thermal cycling. Cross sections of specimens taken from the same location on each board were examined for barrel cracks and conductor separation. The results are given in Table 3. A direct correlation between thermal stress and thermal shock was not obtained and should not be expected, with the possible exception of boards with poorly made PTHs.

In the thermal stress test, the board receives a sudden heat pulse as the specimen is placed on the molten solder. The PTH heats up rapidly to the solder temperature and transfers heat at a lower rate to the surrounding laminate, creating temperature gradients in the laminate surrounding the hole. When the specimen is removed from the solder surface, the PTH is cooled in air at a rate corresponding to the release of heat from the solder in the PTH and from the lateral conduction of heat to the body of the laminate. Thermal shock involves slower temperature changes and includes a low-temperature interval and multiple heating and cooling. The temperature gradients are not as severe as in the thermal stress, but with a longer time at the high-temperature limit, fatigue stresses can be present.

The thermal stress test is an overtest with respect to the soldering time and temperature it is to simulate; i.e., the solder temperature for thermal stress is 288°C, while that for the drag soldering temperature is ~215°C. Exposure time is slightly higher, 10 versus 8 s for thermal stress.

The degree of overtest is being investigated by using a test set of the temperature and time. This work will be reported in a follow-up document. Similarly, an investigation is being planned to determine the extent that the present thermal shock test limits are an overtest for product acceptance. In this investigation, the −65 to +125°C span was used primarily to learn more of the effect of material and process changes on the PTHs.

Conductor separation at the interface of the PTH wall and an inner-layer conductor is usually determined by microscopic examination of cross sections. The inspector must decide in viewing the cross section whether there is a dark line or dark region at this interface and whether it is greater than the normal etch line caused by the difference in etch rate of the two plated copper microstructures (Figures 15 and 16). The decision is often a gray, rather than black or white, situation and can be influenced by magnification used in the examination, degree of etching, and mount preparation. Inasmuch as lot acceptance may

depend on the inspector's decision, we need to learn more about the dark region at this interface, its composition, and how it could be formed. Is it caused by the copper inner layer pulling away from a well-bonded interface as a result of excessive radial stress, or is it the result of lower radial stress at a poorly bonded interface?

Excessive radial stress could be generated from the difference in thermal coefficients of expansion of the materials or from escaping steam in the region near the hole wall. A poorly bonded interface could be the result of smear from drilling or other non-conducting contaminant on the face of the inner-layer conductor so that it is not completely removed, preventing the formation of a metal bonded to metal interface. If there is a crack or incipient crack at this interface, such as shown in Figure 16, we do not know whether the crack would propagate in its end-use environment or during the assembly and testing operations (the Appendix shows the temperatures the MC3811 RF/PWB is expected to experience). An indication of a crack or incipient crack, even with accelerated testing, gives little comfort to a reliability engineer.

Because of the difficulties in assuring that all the interconnections to PTHs are crack free, another approach to achieve higher interconnection reliability is being pursued. This is to reduce the radial and other stresses on the PTH-inner-layer conductor interface. It involves knowing what, if anything, is in this interface, what the role of moisture is in this region, what type of material substitutions would be most beneficial, and how the copper strength affects crack formation and propagation. Since only a fraction of the holes show BCs or CSs, there must be lower stresses or stronger copper in the noncracked holes. It would also be helpful to know why barrel cracks form in some boards and conductor separation in others. With proper control of processing parameters and more realistic overtest requirements for acceptance, WR-quality RF/PWBs should be achievable.

Cross sections of PTHs showing a dark region at the wall-conductor interface were submitted to SNL Organization 1822 for analysis. From scanning electron microscopy (SEM), back-scattered electrons (BSE), elementary distribution photomicrography (EDP), and energy-dispersion spectrum analyses, we concluded that the black material did not contain calcium, aluminum, carbon, tin, or lead but that it did contain silicon and oxygen. Microlaser Raman spectroscopy identified the silicon and oxygen as alpha quartz. We thought a colloidal suspension that is used for final polishing of cross sections explained the silicon and oxygen; however, Raman spectroscopy identified this material as amorphous silica, which leaves unresolved the source of material or lack of it in the dark interface region.

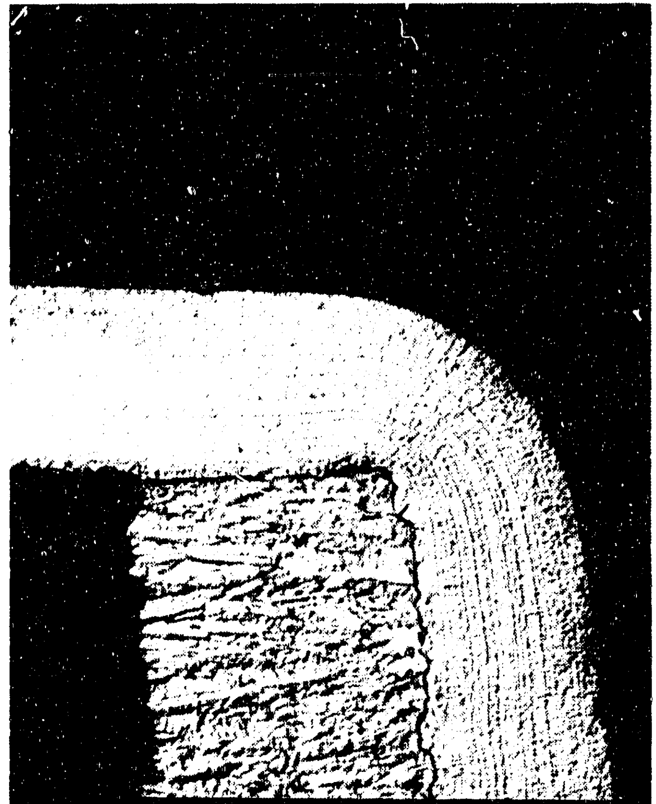
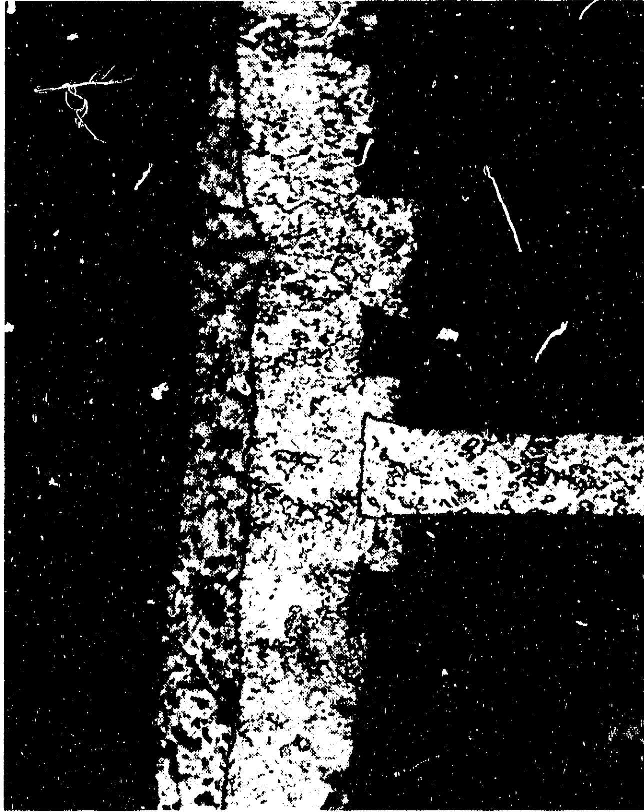


Figure 15. Etch Line Between Two Plated Copper Microstructures



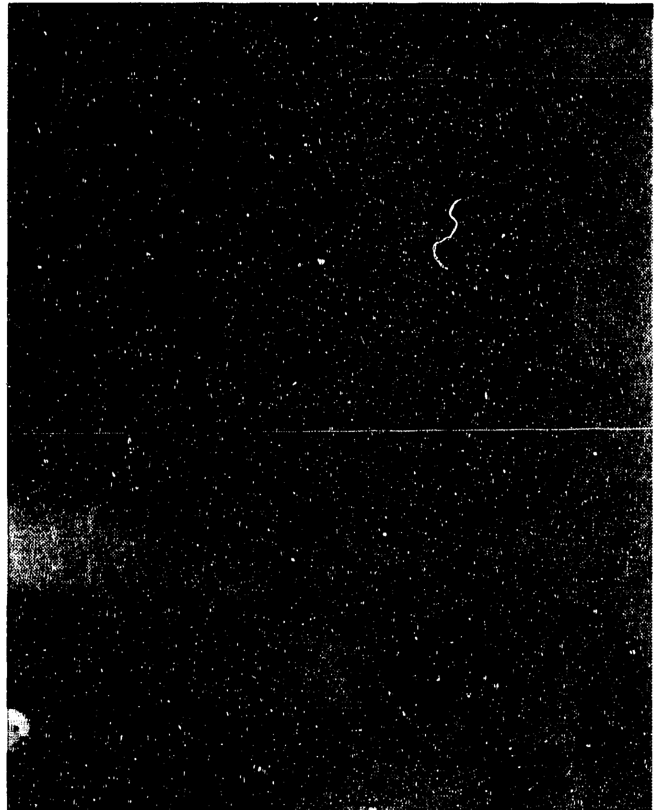


Figure 16. Degrees of Conductor Separation

Conclusions and Recommendations

In this investigation, two thermal tests were run—thermal stress to simulate the soldering operation and thermal shock to qualitatively estimate the lifetime of a board in its end-use environment. Both tests are used as quality indicators for the materials and fabrication operations and to assess the effect of any changes on board reliability. Pass or failure criteria are the presence or absence of barrel cracks (BC) or a separation gap between the inner-layer copper conductor and the wall of a PTH (CS), as seen in microscopic examination of a cross section of a PTH. For thermal shock, there is an additional requirement that one or more test circuits do not change in electrical resistance by some specified value after 100 cycles between upper and lower temperature limits. For MIL-P-55110 this value is 10%.

Rigid/flex multilayer printed wiring boards are more sensitive to thermal environmental changes than conventional rigid printed wiring products made from common material compositions. This is manifested because of dissimilar materials used within the construction of this type of product. Because of that, they must be treated with more care; however, this is not to imply that they are less reliable. It has been proven that properly prepared RF boards can exceed 1000 thermal cycles without any appreciable resistance change.

During fabrication and assembly, stresses can develop within the plated-through holes from differences in thermal properties of the rigid and flexible materials, primarily thermal coefficient of expansion. The temperature of the solder in the thermal stress and the temperature cycling limits in the thermal shock test were found to be the most important variable affecting defect occurrence or circuit resistance change.

The most important variable affecting cycle life for any of the boards tested was found to be the high- and low-temperature limits or temperature span to which the board is exposed. Higher failure rates are observed when cycled from −65°C to +125°C than when cycled from −55°C to +105°C. The worst-case temperature span expected for the MC3811 is only −20°C to +80°C. With this span >1000 cycles were run, with <10% change in resistance.

It can also be concluded that the thermal stress test is an overtest with respect to the soldering time and temperature it is to simulate; i.e., the solder temperature for thermal stress is 288°C, whereas that for machine soldering temperature is ~215°C. There seems to be a general consensus within the rigid/flex industry that the military requirements imposed by MIL-P-50884 may have been arbitrarily chosen and may not actually represent true product requirements.

The adequacy of the acceptance requirements is also questionable in that a minimum gap separation or sufficient differentiation between gap and an etch line is not always clearly defined. The acceptance of a board or lot of boards may depend on the judgment of an inspector. The resistance requirement also needs investigation in that barrel cracks were found in cross sections of board circuits having a resistance change of ≪10%. Ascertaining the absence of cracks at the inner-layer conductor/hole wall interface for a lot of RF/PWBs is not a simple matter; it involves a degree of sampling used in testing, process control checks, and test circuits that can be monitored.

The test pattern shown in Figure 17 was not available in the first part of this study but will be used for all future thermal tests for product evaluations. It provides five holes for cross-section examination and has a known number of interconnecting inner layers. Additional testing is planned to correlate tests made with this pattern to those made on board specimens. Use of a common test pattern will also facilitate data comparisons among RF/PWB users.

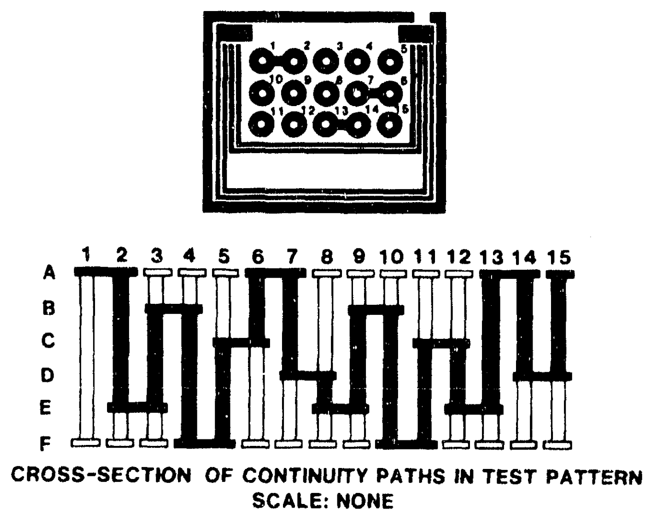


Figure 17. Serpentine Test Pattern (six layers)

Rigid/flex multilayers offer many advantages over conventional printed wiring assemblies. This includes error-free assembly because of the elimination of interconnecting wiring between boards, reduced number of solder joints, ease of assembly testing, smaller packaging, and lighter weight. It is our conclusion that for the thermal requirements of the MC3811,

rigid/flex boards are very reliable. However, for applications involving higher temperature requirements, a designer should be aware of some of the RF limitations. In that case, higher temperature materials and alternate constructions should be considered. Ongoing work is presently being conducted to address these anticipated additional requirements for future applications.

References

[1]F. L. Gentry, *Development and Process Control for Rigid/Flex, Multilayer Printed Wiring Boards*, SAND86-1555 (Albuquerque, NM: Sandir National Laboratories, August 1987).

[2]J. W. Lula, *Moisture Absorption and Bakeout Characteristics of Rigid/Flexible Multilayer Printed Wiring Boards*, BDX-613-3730 (Kansas City, MO: Allied-Signal Aerospace, April 1987).

[3]J. Balde and G. Messner, "Local Dielectric Constant—The Substitute of the Future," *Current World*, Vol. 14, No. 1 (1957), pp 11-14.

APPENDIX

MC3811 Programmer Processing Temperatures

Level	Operation	Temperature (°C)	Time
PWB	Before Soldermask	120	0.5 hr
(After	Soldermask Curing	148	1.0 hr
Plating)	Before Soldering	135	8.0 hr
	Soldering Dipping/Leveling	232	(4.0 s)
	Final Drying	112	2.0 hr
PWA	Before Soldering	93	12.0 hr
	Drag Soldering	246	(5.0 s)
	Component Burn-In	100	168.0 hr
	Acceptance Testing	5	1.5 hr
	Acceptance Testing	80	1.5 hr
	Stabilization	100	24.0 hr
Polystyrene Bead	Encapsulation	96	1.5 hr
Encapsulation	Acceptance Testing	5	1.5 hr
	Acceptance Testing	80	1.5 hr
Stress	Temperature Cycling	25 to 80	25 min (2.25°C/min)
Screening	(4 cycles)	80	1.0 hr
		80 to −55	1.0 hr (2.25°C/min)
		−55	1.0 hr
		−55 to 25	35 min (2.25°C/min)
	Acceptance Testing	5	1.5 hr
	Acceptance Testing	80	1.5 hr
E-Test	Temperature Cycling	25 to 80	25 min (2.25°C/min)
(Sampling Plan)	(10 cycles)	80	1.0 hr
		80 to 95	1.0 hr (2.25°C/min)
		−55	1.0 hr
		−55 to 25	35 min (2.25°C/min)
	Encapsulation (Cerrolow-117)	71	2.0 hr
	Decapsulation	71	2.0 hr
	Acceptance Testing	5	1.5 hr
	Acceptance Testing	80	1.5 hr

END

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