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CEDAR PROJECT — ORIGINAL GOALS AND PROGRESS TO DATE

Progress Report

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This work encompasses a broad attack on high speed parallel processing. Hardware, software, applications development, and performance evaluation and visualization as well as research topics are proposed. Our goal is to develop practical parallel processing for the 1990's.

Cedar Project — Original Goals and Progress to Date

The Center for Supercomputing Research and Development was founded in late 1984 with major funding beginning in January of 1985. The principal project at that time was the Cedar Project, which was designed to be the focal point for bringing to fruition our work on high performance computation. The goal of this project, as stated in a 1984 report [CSRD464*], was to demonstrate that supercomputers of the future can exhibit general–purpose behavior and be easy to use. The Cedar Project was based on five key developments which taken together offered a comprehensive solution to achieving high performance computation:

1. The development of VLSI components made large memories and small, fast processors available at low cost.
2. Based on many years of work at Illinois and elsewhere, we had designed a shared memory and switch which provide high bandwidth over a wide range of computations and applications areas.
3. The Parafrase project at Illinois had for more than 10 years been aimed at developing software for restructuring ordinary programs to effectively exploit supercomputer architectures. This technology was ripe for a real test.
4. By using a hierarchy of control, we believed that dataflow principles could be used at a high level (macro–dataflow), thus avoiding some of the problems with traditional dataflow methods.
5. Work in numerical algorithms indicated great promise in exploiting multiprocessors without the penalty of high synchronization overhead, which had proved fatal in some earlier studies.

We believe that with the developments over the past six years we have made substantial progress toward our goal. In this section we will outline our progress since the beginning of the Cedar Project and briefly describe specific Cedar work that remains to be done.

CSRD Developed Boards and Physical Equipment

The Cedar hardware (see Figure 1) has been operative for the past two years, and 16 processors have been installed and are functional. The debugging and integration of Cedar has continued until Q4 1990, and we are currently installing all 32 of the intended processors. Continued maintenance will be required for as long as the Cedar system is useful.

We have developed prototype performance evaluation boards, and we are planning to manufacture and integrate a comprehensive set of these boards.

A limited amount of new development will be done on Cedar. For example, the memory system is being improved by building a compatible global memory board using 4 MBit parts. These projects are described in more detail elsewhere in this report.

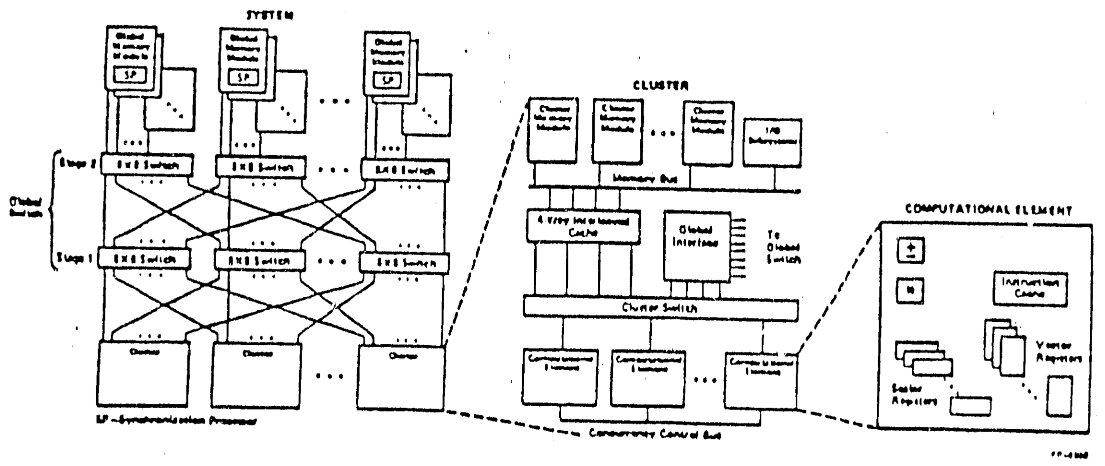


Figure 1. Architectures of the Cedar I

Boards and equipment developed at CSRD for Cedar can be classified into five categories: global hardware boards, support boards, performance boards, diagnostic hardware, and physical equipment.

Global Hardware Boards

The global hardware boards are the main boards for Cedar operation. The Global Interface Board (GIB) provides the interface from the Alliant FX/8 to the Global Network (GN). This board is 20 by 24 inches and has approximately 1,000 equivalent integrated circuits with 11 layers. The GIB is fabricated mainly in TTL technology to gain the most in functionality; however, its Global Network interface is designed in ECL. The Alliant backplane and computational elements (CEs) were modified for CSRD by Alliant to accept this board. Since the Alliant backplane was modified for four additional slots, four GIBs can be loaded into each Alliant (cluster), giving four CEs access to GN.

In addition to providing the interface to the global memory, the GIB provides Cedar-specific functions. The GIB implements the special Cedar synchronization primitives. This board also performs prefetching of vectors from Global Memory at an issue rate of one request every other clock. Cross Processor Interrupt (CPI) between clusters is also designed into the GIB.

An enhanced GIB, the GIB1A, was also designed for Cedar 1A, and its functionality is much like that of the GIB. This board has enhancements that allow for eight GIB1As to exist in each cluster, providing a global hardware interface for each CE in the cluster. Since early 1989, Cedar 1A has been operating using GIB1As.

On the GN interface side of the board, the GIB can issue requests into the network at the rate of one every two clocks. This matches the bandwidth of the Alliant issue rate. On the receiving side, the GIB has a four-deep FIFO for receiving return requests from GN. These requests can be routed by the GIB to the Alliant, the prefetch data buffer, the synchronization processing unit, or the CPI logic, whichever is appropriate.

The next set of board types constitute the GN. This expandable shuffle network is composed of two board types GNBI and GNBK. Both boards are on 20 by 24-inch form factors, and GNBI has approximately 1,150 ICs and 17 layers, while GNBK has 600 ICs and 8 layers.

GNBI is the main board of the set. This board is essentially an 8 x 8 crossbar packet switch, and each port is 80 bits wide. GNBI is designed using ECL technology to provide high bandwidth. In each clock cycle, GNBI can accept a word on all input ports, resolve conflicts, route them, and present the results to the output ports.

GNBI is made possible with a CSRD-designed ECL gate array that does most of the switch function and data queuing. The gate array is a four-bit 8 x 8 crossbar connection matrix with input and output queuing on each port. Nineteen of these gate arrays exist on each GNBI. The control for this switch uses MSI circuitry and handles contention resolution as well as providing queuing control of incoming data. Each port has a two-deep input queue and an output latch. The board has 1280 differential ECL signals presented to it via cable and provides 640 single-ended ECL signals for backplane driving to the next board, GNBK.

GNBK receives the switched data from GNBI via backplane connections. This board provides one level of queuing (latch) and converts the single-ended signals from the backplane to differential signals for cable driving to the next GN pair, GM, or GIB.

The GMB contains main memory and implements Cedar synchronization. The board is identical in size to the GIB and network boards and has approximately 1200 ICs with 15 layers. All paths on the board are 64-bits wide. It is designed with a mixture of ECL and TTL technology to provide the best compromise between speed and functionality. GMB has 2 Mbytes of RAM, and ECC protection with a 64-bit word size. This board also contains the synchronization processor that completes (together with the GIB) the implementation of the special Cedar synchronization primitives. GMB has three levels of input buffering and three levels of output buffering. It can sustain a 64-bit data streaming rate of one datum in four clocks. The latency is six clocks, a read-modify-write cycle takes eight clocks, and the synchronization processor adds three clocks for performing 32-bit operations. Normally, there is one GMB for every GIB. By reconfiguring the network, this ratio can be modified.

The memory system of Cedar is being improved by a compatible global memory board that uses 4 MBit DRAM chips instead of the 256 KBit chip which will permit the expansion of a single global memory board from 2 MBytes to up to 32 MBytes. The global memory board has significant control- and data-path board-space overhead, so that it makes economic sense to use 4 MBit DRAMS instead of 1 MBit, even if the cost ratio (of 4MBit devices) is as much as two to four times higher. This will extend the lifetime of the system for interesting applications work by allowing larger problems to be run. In addition, if board space permits we would like to restore synchronization functionality that had to be deleted in the first generation global memory board for space reasons, which will allow experimentation with a richer set of synchronization techniques than is now possible. We feel that this is a significant research area for the future in which experimental work could be quite important.

In order to bring these boards together, CSRD-designed backplanes have been produced. There is a backplane for GN that allows GNBI and GNBK to communicate with each other, and which supplies the 600+ amps of power required. Similarly, there is a backplane for GMB that provides the power as well as diagnostic interfaces and cable attachments.

Another Cedar system board is the global clock board, which provides clocks to all global hardware boards as well as to each cluster. The clock board also provides clock synchronization to each cluster to keep all clusters in lock-step.

To allow for eight GIB1A boards to exist in the cluster, CSRD has redesigned the Alliant backplane. This "stretched" backplane was designed by using the Alliant backplane database, adding connectors, and lengthening the backplane using the Calay CAD system.

Support Boards

There have been myriad support boards developed at CSRD. To test hardware, there is a GIB emulator board that emulates the memory and network for GIB debugging and diagnostics. The network board pairs required two special boards that, along with an IBM PC/AT, form a network testbed that allows testing of the network boards under very controlled conditions to debug and test conflict resolution and data path integrity.

CSRD has also designed diagnostic and maintenance boards for the Cedar system. Diagnostic "hooks" are provided on both the GIBs and GMBs. A number of 8751 attached processors monitor the status of GIBs and GMBs and report any errors, via RS232, to a Sun IV workstation. GN has internal diagnostics that provide a simple go/no-go LED indication on each board.

For maintenance, a global reset board and an environmental monitor system have been designed at CSRD. The global reset board provides a precise reset capability for Cedar. The environmental monitor system, which is composed of four small boards, monitors Cedar environmental aspects such as air temperature, cooling fluid temperature, and power supply load and status.

Performance Monitoring Hardware

Throughout the design of the Cedar-specific boards, performance monitoring has been a critical objective. The level of design complexity required for the basic functionality of the interface, interconnection network, and shared memory prevented the incorporation of integral performance monitoring counters and timers on the boards themselves. Consequently, to supplement the large number of performance signals available on the cluster (Alliant) backplane, a significant number of representative signals were identified on each board as observation points, and these signals were buffered and brought out to the edge of each board. The interface board contains 49 signals (e.g., start and stop triggers, access to the data path, prefetch unit state data, synchronization operation data, processor side and network side interface data), the network switch has 128, and the shared global memory has 55 per board.

To collect and process these data, the industry standard VME bus has been adopted by CSRD for the development of all moderate-to-very-sophisticated performance monitoring hardware tools. Prototype board quantities have been constructed for two fundamental hardware performance tools: a hardware Histogrammer and a hardware Tracer. The Histogrammer is capable of histogramming 64K different events at a 170-nanosecond rate. The Tracer is capable of tracing 20 bits of data with a depth of 1 million samples at a 170-nanosecond rate. Both of these boards support interleaving to increase acquisition speed and depth. This allows the Tracers and Histogrammers to be used on a one-per-CE basis for software event rates, and on a two-per-CE basis for hardware event rates. A Sun processor board resides in the VME chassis with the performance analysis hardware to extract data from these boards and to provide analysis capabilities and an ethernet connection to the other computers at CSRD.

For smaller problems and individual signal measuring, a substantially smaller "black box" card is used, and thus small, specific, limited function cards can be developed quickly and inexpensively. Three such modules have been developed to date: two types of data acquisition boards (with associated data probes) for collecting TTL and ECL signals from Cedar, and a dual-channel 16-bit counter-timer with storage capable of storing 32K counts. An interface between the black box and a Multibus chassis (the principal I/O bus of Cedar) has been built, and the necessary software support for black box control has been written.

Diagnostic Hardware

The ability to detect and identify hardware problems in a working system was established as a very important design aspect in the early phase of Cedar development. The large number of boards in this system, coupled with the problems of online diagnostic and isolation techniques, makes the process of board-swapping for fault isolation wholly unacceptable. We chose the approach of attached diagnostic processors for groups of boards and designed error status and handling circuitry into each board type to report errors (via the diagnostic processors) to a host work station.

We chose to keep the diagnostic processor design as simple as possible to increase reliability and ease the design requirements for both the diagnostic itself as well as the error reporting circuitry on each of the board types. To this end, we chose to use a single chip microcontroller that provides a bit-serial interface to the outside world, and surrounded it with the "glue" logic necessary for interface to each board type. In addition, the ROM-resident code for the diagnostic processors is contained in the microcontroller as well as the static RAM for the storage of error status.

At present, we have all required diagnostic processor boards for both the GIB and GMB boards (the diagnostics processors are embedded in the global network boards). The diagnostic is fully operational in the Cedar 1A system. All the application-specific code has been generated and debugged for the diagnostic processors. The serial interface mentioned above is currently being used to dump diagnostic information to a Sun IV workstation.

We have chosen to use a Sun as the workstation to tie all the diagnostic processors together. Additionally, Alliant-based code has been developed to exercise the Cedar system, and work continues on the development of system code to perform on-line checks and fault isolation.

Physical Equipment

Physical equipment designed at CSRD includes three different extender board types as well as the powering, cooling, and housing of Cedar. Four cabinets have been designed at CSRD. Two of these hold the four Alliant clusters (Cedar 1A), one holds the network, and the fourth, smaller cabinet, contains the memory system. Powering is provided by large switching supplies with a total output current capability in excess of 2000 amps. Cooling is provided for by chilled water heat exchangers, of which there are three in each cabinet. The capacity of each exchanger is 7.5 Kwatts.

Operating System

Xylem (Cedar)

We have taken a very conservative approach to implementing an operating system for Cedar. Instead of starting from scratch, we chose to adopt Unix and to start with Alliant Concentrix (which is based on Berkeley 4.2). Our system is called Xylem[1]. The main areas where Concentrix needed to be modified were to provide: (1) support for the utilization of multiple clusters by a single program, (2) management of the physical main memory hierarchy (global vs. cluster), (3) support for shared virtual memory between

[1] "A complex tissue in the vascular system of higher plants...functioning chiefly in conduction but also in support and storage..."

clusters, and (4) inter-cluster synchronization and communication mechanisms. Xylem has evolved in such a way that each Alliant cluster still appears to execute an independent Concentrix OS while also managing Xylem-specific programs that utilize the features of the Cedar system. This year has seen progress in a number of areas, described in the following paragraphs.

User-level inter-cluster and inter-processor synchronization mechanisms have been further developed. We have run-time library routines for doing mutual exclusion and post-wait event style synchronization. Internal interfaces within these routines have been simplified and overall they have been made more robust, including fixing a bug that could lead to deadlock during interrupt routines.

The saving and restoring of Cedar-specific hardware registers during interrupts and context switching has been fixed. This was done incorrectly in the first implementation and so the use of Cedar synchronization hardware was unreliable. There were small timing windows during which the contents of these registers could be corrupted by the OS, resulting in the execution of operations that were not intended. This problem has been cured, and a number of diagnostic tests are now available to verify correct operation of the hardware while under control of the OS.

The hardware group has corrected the problems we had with the high-resolution (10-microsecond) clocks on each cluster. Previously these would appear to drift, as if running at slightly different rates. As a result, it was difficult to tell the same time in tasks on different clusters. Elaborate software mechanisms were in the kernel to detect this drift and then resynchronize the software. This resynchronization process would necessarily tie up clusters for long periods of time, and it happened often enough during normal scheduling activities to impact user program performance. A new algorithm has been designed to sync the clocks only once during system initialization. At the same time, rather than computing pairwise time deltas between clusters, we will use the notion of synchronizing against a global time base. As a result, it will be much easier for programs to measure time and coordinate events across clusters, with no system interference. For example, a periodic system utility can run once a day to verify that the clocks have indeed maintained synchronization.

Another problem that required a considerable amount of attention was the diagnosis of bugs in the physical memory allocators and process swapping algorithms in the kernel. Some of the indicators of these bugs are that processes might get swapped out and then never get swapped back in, or processes might get stuck in memory (i.e., not swapped out) such that other processes could not be swapped even though they we ready and had sufficient priority. These problems were caused by a combination of incorrectly accounting for how physical memory was being used, and incorrect computation of working set sizes by the system swapper. We are confident of our diagnosis, and most of these problems have been corrected, but there are still accounting errors to be isolated. Algorithms in the swapper have been made more fault tolerant of such inconsistencies.

Instrumentation of Xylem

The current implementation of Xylem is partially instrumented. For example, facilities exist to account for every page fault in terms of what kind of memory was faulted (e.g., cluster vs. global, shared vs. private), and how it was resolved (image from memory or disk,) [CSRD857** & CSRD858*]. Accounting for system-wide paging activities has recently been installed, and we are looking forward to observing the paging behavior and tuning this aspect of system performance.

We have designed a comprehensive instrumentation approach using the hardware facilities available on the Cedar GIB board. This hardware will let us collect trace events and send them to a dedicated processor. Without adding much overhead in the kernel, we intend to collect timestamps on all kinds of system wide activities, such as interrupts, context switches, and page faults. Some low level subroutines are already in place to make trace events and write them to the hardware buffer. With these capabilities fully functional, we will be able to determine what is really happening inside the OS.

Single User Batch

Recently, a single user batch facility has been implemented and installed on Cedar to make it possible to submit a job to be run in single user mode automatically. At predetermined or regularly scheduled times, the normal time-sharing system will shut itself down and initiate single user batch processing. If there are any jobs in the single user batch queue, they will be run one at a time, and when finished, normal time-sharing will resume. This will remove a large burden on our user community. Many of these people need the machine in a single user mode, but still operate under Xylem, primarily to do benchmarking runs. Previously, they had to sign up in advance for time slots in the evening or early morning, and then come to the machine room and work at the console during their assigned time.

Debugging Support in Parallel Programming Environments

This study involves some of the problems of debugging parallel programs, particularly those at a low level (i.e., machine code level). Problems unique to parallel programming environments include identifying and probing execution threads and synchronization of the debugger within itself and with the user's program. This work also intends to identify a small set of specific facilities that the operating system kernel can provide to support parallel debugging tools. An initial implementation of interactive parallel debugging facilities has been done in the Xylem environment. Different approaches are being tried, and deficiencies in kernel support have been identified. Ideally, this work will build a base upon which high-level debuggers can be built.

Research

Recently, we have been discussing new ideas for the design of a multi-processor operating system. We observe that Unix-based operating systems have gotten larger and more complex over the past decade, as much as one to two orders of magnitude compared to the early Bell Labs versions. Yet with this tremendous increase in size and complexity, there is very little improvement in functionality or performance. As a result, our thinking leans toward a very simple design, which is portable to a number of shared and hierarchical memory machines.

For example, unlike most research efforts, we are considering a kernel that does not require or utilize virtual memory management hardware. This is prompted by two considerations: (1) users continually request that we eliminate virtual memory because it always interferes with performance, and (2) we are targeting Cray machines, which do not have virtual memory hardware.

Currently, we envision the multiprocessor kernel as only providing processor and physical memory management, scheduling, swapping, and trap handling. I/O and network activity may be passed off (via messages) to attached host processors.

Languages and Compilers

Our work on languages and compilers has been guided by three main objectives: (1) to provide the programmers of the Cedar System with high quality compilers and restructurers; (2) to conduct research on compilers and restructurers leading to the development of algorithms that are useful for our work on Cedar, but will also be applicable on a wide spectrum of machines; and (3) to study compilation and restructuring techniques for languages other than Fortran.

Fortran Translation

Fortran, the most frequently used language in supercomputing today, is the most natural language on which to base a major portion of our effort mainly because most supercomputer applications are dominated by numerical computations, including most of the algorithm research work at CSRD. In addition, Fortran will most likely be used on supercomputers for a long time to come.

Cedar Fortran

Our work on Fortran began with the design of extensions to Alliant Fortran for parallel processing on Cedar. Alliant Fortran includes extensions for vector operations. These are essentially those in the current Fortran 8X proposal. We decided to adopt the extensions and concentrate our efforts on extensions for concurrency. To this end, we developed constructs for task parallelism and loop parallelism. For task parallelism we designed constructs similar to those of Cray Fortran. These constructs are adequate, and the applications group at CSRD felt comfortable with them. One major difference between Cray Fortran and our (**ctskstart**) task spawning routine is that the latter allocates not one processor, but several to the newly created task, in order to allow the cluster tasks to use the Alliant hardware in the execution of concurrent loops. We have also developed a micro-task spawning mechanism centered around the **mtskstart** routine. This routine creates a microtask and queues it according to a priority specified in one of its parameters. Helping (or implicit) tasks remove microtasks from the queue and execute them to completion before going back to the queue for more work. Microtasking has a lower spawning overhead than regular tasking. However, microtasking is in some cases harder to use since it does not allow synchronization operations other than those used to wait for the completion of a microtask (**mtskwait** and **mtskwaitall** in Cedar Fortran).

Extensions for loop parallelism included **doall** and **doacross** loops. These resemble the regular Fortran **do** loop, but their iterations may proceed in parallel. Concurrent loops may be confined inside a cluster or execute across clusters. In the first case they make use of the Alliant hardware for the scheduling of iterations on processors. When concurrent loops are executed across clusters, there are two alternatives. In the first, whole (virtual) clusters are used to execute the loop in a self-scheduled manner. In the second alternative, several individual processors from two or more clusters are used to execute the loop, also in a self-scheduled manner. The scheduling in these two last cases is handled by software under the microtasking scheme. Concurrent loops executed by whole clusters are supposed to enclose concurrent loops of the cluster-confined type to allow the use of all the processors in a cluster.

Cedar Fortran includes extensions to specify at which memory hierarchy level individual variables and common blocks are to reside, and includes extensions to handle the Cedar memory synchronization hardware primitives. A detailed description of Cedar Fortran can be found in [PaLa86], [Guzz87], and [GPLH90].

From the point of view of implementation, the Cedar Fortran compiler comprises a source-to-source preprocessor, a slightly modified version of the Alliant Fortran compiler, and an object-to-object postprocessor. The preprocessor executes before the Alliant Fortran Compiler and translates Cedar Fortran constructs to Alliant Fortran constructs or to subroutine calls. The postprocessor executes after the Alliant Fortran compiler and translates Unix object files into Xylem object files. The only modifications to the Alliant Fortran compiler were those needed to generate the machine code for vector prefetching from global memory via the Global Interface Board. A major portion of the compiler work was the development of new run-time library routines needed for the Cedar Fortran constructs, and the modification of the Alliant run-time routines to allow them to run under Xylem. The Cedar Fortran compiler with its run-time library is now operational and has been extensively tested. Much effort has been invested lately in decreasing the overhead associated with the run-time library and providing efficient mechanisms for data communication and synchronization. To this end, we are experimenting with strategies for dispatching and scheduling DOALL loops across the four Cedar clusters. For example, we have found that static dispatching brings the overhead down to 40 uses. Self-scheduling using the Cedar synchronization hardware is also being tested.

Fortran Restructurer

A second component of the Fortran translation system is a restructurer that translates from Fortran 77 to Cedar Fortran. The present version of the restructurer is KAP, a commercial product developed by KAI. We have modified this source-to-source restructurer to generate Cedar Fortran as its output. In its current state, the implementation automatically identifies concurrent loops and vector operations. The system performs strip-mining as necessary to permit the exploitation of the three levels of parallelism available in Cedar. It also allocates variables in one of the memory hierarchy levels either automatically or by using user-supplied statements.

So far we have demonstrated good performance on Cedar for program kernels and some algorithms. Additional work is needed to exploit efficiently the architectural features of Cedar. To make the restructurer a powerful tool for the Cedar system we need to accomplish the following:

1. Make it possible for the restructurer to accept Cedar Fortran as input. There are several reasons why this is desirable. One is the obvious appeal of not having to think in terms of two dialects of Fortran. The second, and probably the most important, is that programmers may want to indicate parallelism explicitly before restructuring takes place, and Cedar Fortran is the most natural way to do this. Accepting Cedar Fortran implies that the input to the parallelizer might be a parallel program. The transformation of parallel programs presents some difficulties that are under study [MiPa90].

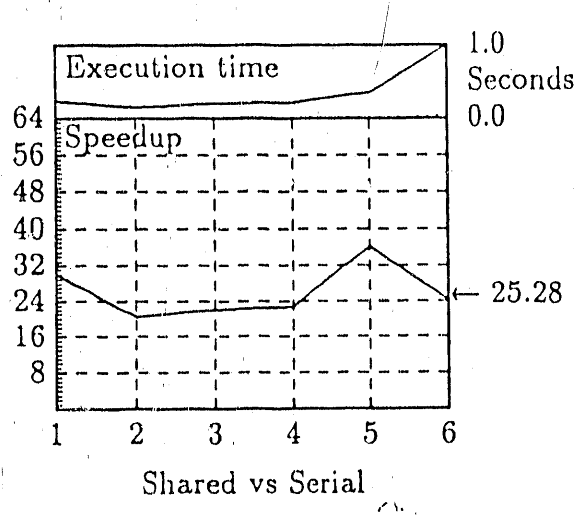
2. Spreading (the transformation that generates task parallelism) has not yet been implemented. An effective implementation of spreading requires a good interprocedural analysis subsystem, which has not yet been implemented either. Interprocedural analysis has been discussed in [LiYe88a,b&c]. Spreading was studied in detail in [Veid85].

3. Finally, we have to apply the restructurer to a broad range of algorithms and application programs. This enables us to study and refine its operation in practice. In a series of experiments we have identified a number of improvements to compilation techniques and strategies that cause significant performance gains in large codes. The following section illustrates some experiments. Incorporating these experimental results into the restructurer's capabilities is an ongoing effort.

Experiments with the Restructurer

We have timed various applications from the Perfect Benchmarks ™ on Cedar and measured the performance of individual loop nests (by summing the wall-clock time of all the activations of each lexically outermost loop). The measurements of OCEAN and FLO52 are summarized by the graphs in Figure 2, where each tic on the x-axis represents a different loop nest within the program. Of course, each loop nest has a different impact on the overall performance of a program, so we present them sorted in increasing order by their serial execution time. Loop nests plotted at the far right cover more of the application's execution time than those to the left.

The y-axis contains two regions: at the bottom we report a speedup ratio for each nest, and on top we accumulate the execution time of all nests from left to right. On the top region, we represent the maximum time accumulated by any of the nests in any version of the program. The solid curve in this region represents accumulated serial execution time. The dotted curve in this region is the execution time of the parallelized version. To the right of each speedup plot an arrow reports the overall speed-up of the whole program.



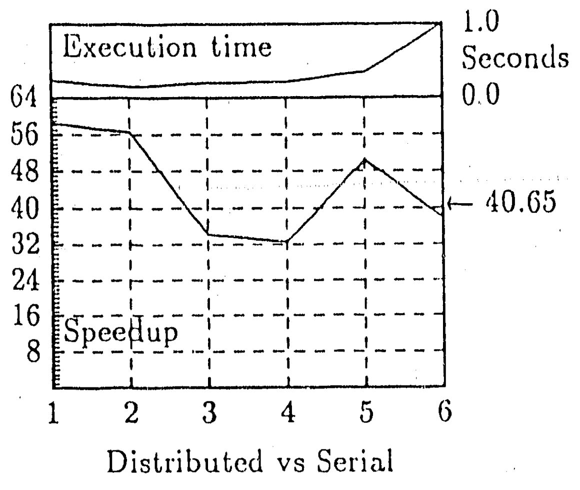


Figure 2: Speedup of Perfect Benchmarks ™ OCEAN and FLO52

The serial version in Figure 2 uses the traditional serial optimizations (like common subexpression elimination) applied by the Alliant code generator. The (SDOALL) version of the program is the result of applying the Cedar Restructurer to the serial version, commanding it to place all interface variables in GLOBAL memory, thus enabling a maximum number of SDOALLs.

The obvious conclusion to be reached from the graphs of Figure 2 is that the overall performance of an application nearly equals the performance of its most important loop(s). We will refer to the loops which accumulated the top 90% of execution time as the *significant* loops of the program. In OCEAN, the Cedar Restructurer's SDOALL version did well on many of the low-run-time loops, but not as well with the significant ones. Consequently, overall speedup was poor (0.74). In FLO 52, the SDOALL version performed well on the most significant fifth, and the mixed performance elsewhere did not detract from a respectable speedup of 6.7 for the whole program.

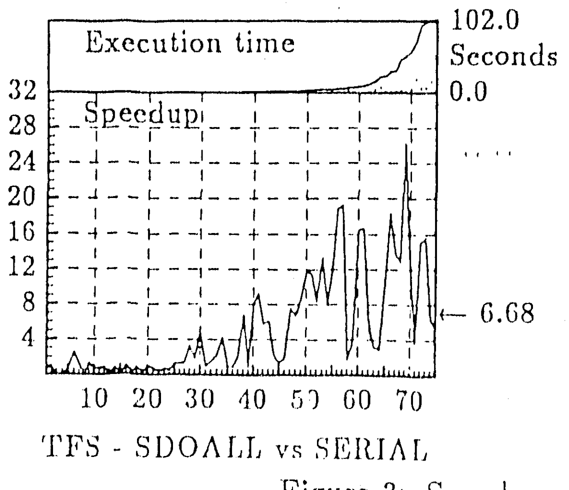
The OCEAN program makes complex use of induction variables in many of its significant loops, the Cedar Restructurer had trouble following some of this. It also calls a handful of low-level subroutines in many loops, forcing the loops serial. Occasionally, inner loops of a loop nest contained calculations with no subroutine calls and these were successfully stripmined and run as SDOALLSs, while the outer loop remained serial because of subroutine. Interprocedural analysis was not applied in this experiment because of the problems with our version of KAP in its in-line expansion pass. We have recently fixed some of these problems, and are planning to use in-line expansion in the next experiment. We also plan to study the development of a more sophisticated induction variable analysis.

The significant loops of the FLO52 program contain many easily vectorizable calculations. All of the significant loop nests had at least an inner loop which was parallelizable, and some nests could be totally parallelized. In the FLO52 program, three significant loop nests had an outer loop that was forced to remain serial because there were too many inner loops. Increasing the data structure sizes allowed two of these to be parallelized. Presumably the other could be parallelized with even larger data structures. The recurrence solvers that we use have not been optimized for Cedar, which was the source of poor performance on two significant loops.

In the FLO52 code, the Cedar Restructurer produced parallel versions of many of the significant loops, but their speedup is less than optimal. Why is that? The most important reason may be that the average running time for most of the loops, even in the serial version, is very short and barely overcomes the SDOALL loop overhead costs. Multi-version loops might cut our losses here.

In one benchmark exercise we solved a banded linear system of 255 equations using the Conjugate Gradient algorithm. Our test data required approximately 65,000 iterations in the key loops, enough to exploit all the parallelism in Cedar. The kernels were transformed into SDOALL/CDOALL/vector loop nests. Figure 3 shows the speedups for the main kernels of this code. The basic statistic is the *minimum* execution time over several hundred repetitions. This statistic eliminates a few executions inadvertently delayed by other system software.

These runs were made on a half-sized Cedar with 16 CEs, each having 4 stages in its vector pipeline, so 64 calculations can occur in parallel. But the effective parallelism in the shared memory network never exactly matches the processor parallelism. Speedup ratios vary from kernel to kernel because each has a different ratio between the



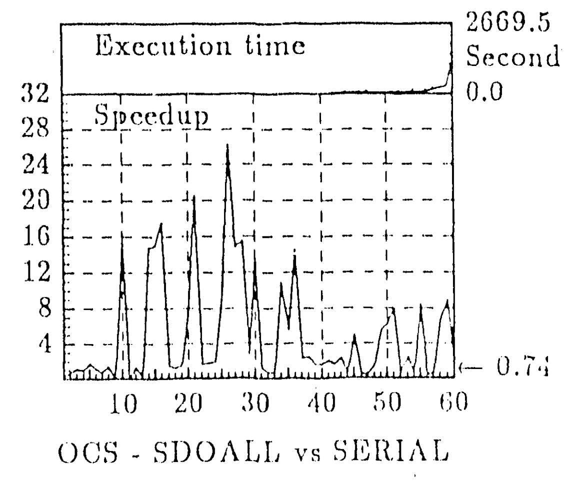


Figure 3: Speedup of Conjugate Gradient Algorithm

number of memory references and the number of arithmetic operations. The beneficial effects of cache and prefetching, and the detrimental effects of network contention affect each loop differently.

The second diagram in Figure 3 reports the speedup (parallel times vector) due to manual application of the data distribution techniques. The bandwidth of the global network and memory, which limits the shared methods, does not restrict this scheme. The overall speedup is now 40, and individual kernels are becoming processor-bound.

Other Translators

Two other projects have been undertaken in the compiler area. We plan to continue both of them. However, in this section we only describe them briefly. Later in the proposal, some specific parts of these projects will be discussed in detail.

The first project is Parafrase 2. The main objective of this project is to develop a successor to the Parafrase Fortran restructurer. The Parafrase-2 project involves the construction of a multilingual parallelizing compiler for C and Fortran, which will incorporate the latest technology on parallelization, as well as recent research results of our group. Parafrase-2 is being developed not only as a source-to-source parallelizer but also as a fully develo[illegible] a compiler which generates code for an abstract parallel architecture.

Although this is an ongoing project involving a faculty member and four graduate students, the compiler has passed its first phase of development and is currently in use at CSRD as well as several other universities and research centers in the U.S. At present, Parafrase-2 is capable of performing loop parallelization inter- and intra-procedurally. Powerful data dependence analysis with new techniques for symbolic dependence analysis have been implemented along with inter-procedural analysis. Several transformations and optimizations have also been completed, including loop parallelization, scalar expansion, loop blocking, induction variable recognition, loop interchange, loop distribution and vectorization.

In addition, an interactive graphics interface has been added to Parafrase-2, which provides a convenient means for visualizing and manipulating internal program representations such as the control flow graph, the procedure call graph, and the data dependence graph. Parafrase-2's graphics interface, which runs under X windows, has provided a powerful tool in interacting with the compiler and guiding parallelization wherever needed. Parafrase-2, which has been developed in C and runs under Unix, comprises at present 80K lines of C code. The use of data abstraction in the development of the system has proven instrumental in its use as the basis for building simulators or other compilers on top of it, at several centers where it is being used.

The second project, MIPRAC, is an attempt to fuse the techniques of automatic parallelization of numerical codes (as employed in Parafrase and its descendants) with those of symbolic codes (as employed in PARCEL, a LISP parallelizer [HaPa88]). The goal is to use intersections and unions of these techniques to arrive at a compiler that can parallelize, for example, a C program that manipulates pointer variables, dynamically allocated objects, as well as arrays of numerical data. The compiler itself will operate upon an intermediate form into which programs in a variety of languages may be rewritten. We have implemented translators from Scheme and Fortran 77 into MIPRAC's intermediate form and are implementing one for Pascal. We intend that programs that are written in several source languages may be sensibly analyzed, compiled, and linked using this multilingual translator.

To ensure that MIPRAC's intermediate form is as compact as possible, several phases of syntactic and control-flow normalization are used to coerce input programs into a highly normalized form. Following this normalization, an interprocedural analysis is performed which extends the side effect and lifetime analysis used in PARCEL to vector and array data. MIPRAC's parallelizing transformations will include array- and DO-loop-oriented transformations (loop distribution, loop interchange, scalar expansion) as well as recursion- and WHILE-loop-oriented transformations (recursion splitting, exit-loop parallelization).

To date, the phases of syntactic and control-flow normalization and the first phase of interprocedural analysis have been implemented.

MIPRAC will produce a machine-independent, parallel intermediate code that can be executed using PARCEL's run-time system, which is being extended to accommodate the requirements of MIPRAC's intermediate form.

The Ansi C, Scheme, and Common LISP front ends for MIPRAC are implemented, and we have begun debugging them. The front ends rewrite C and Common LISP programs into the intermediate language used by MIPRAC (called MIL). The control structures in these languages (tail recursion in Scheme, `foreach` and `mapcar` in Common LISP, `for`, `do / while`, `break` in C) are too many and too diverse to be represented directly in the intermediate form. Our solution is to give all of these structures a simple translation in terms of `gotos` and labels, in MIL. Afterward, a phase of control flow normalization eliminates all `gotos` and labels, leaving only properly nested `begins`, `ifs`, `whiles`, and procedure calls. A final phase of normalization rewrites the `while` loops as tail-recursive procedures, so that in the end we have only `begin`, `if` and procedure call as control structures in a MIL program. The normalization phases are complete and have been debugged.

The interprocedural analysis of MIPRAC has been implemented and is being tested and debugged. The analysis is in C; its interface to MIPRAC is a simple, ASCII one: an encoding of the program arrives on standard input as an ascii text, and the output is returned in ascii format. The analysis is therefore available to others, as a module separable from MIPRAC. Three kinds of information are gathered by the analysis: the interprocedurally visible side effects of procedures; the lifetimes of dynamically allocated objects; and structure sharing within the data structures created by the program. The analysis uses a new algorithm for finding the fixpoints of functionals efficiently. This algorithm employs techniques from data flow analysis to direct the solution of fixpoint equations. We intend to parallelize the analysis and to run it remotely on the Alliants or Cedar, to speed the analysis of large programs.

We are also developing a new theory of automatic parallelization based entirely upon recurrence relations. The idea is that in every iterative or recursive structure there are simple recurrence relations (e.g., induction variables) from which more complex recurrence relations are computed, and finally from which the sequence of memory addresses that are accessed are computed. Automatic parallelization requires two things: a view of the relationship between objects in memory, and a view of the recurrence relations computed by iterative and recursive structures. These two components allow us to reason about whether the addresses issued in one iteration overlap with those issued in another iteration. In general, we find that if the recurrences that carry us from locations to new locations are "linear" in that they do not return to previously accessed locations, then the iterations of a recursive or iterative structure are independent. These observations may be made the basis of an algorithm for automatic parallelization that treats both subscripted and pointer accesses in a single framework. We are trying to do exactly this in MIPRAC. The two components of the framework are the above-mentioned interprocedural analysis (which gives us a view of the objects in memory and their interrelationship) and an interprocedural recurrence recognizer, which gives us a view of the recurrences described by iterative and recursive structures. (In fact, by the time these analyses occur in MIPRAC, all iterative structures from Fortran, C, and Common LISP are rewritten as recursive or tail-recursive procedures in the intermediate language of MIPRAC.)

Finally, we are designing a code generator and run-time support for MIL (the intermediate language of MIPRAC) for the Cedar machine. The intermediate language has been designed to make this particularly simple: there are only a handful of control forms, and low-level operations that correspond mostly to sequences of a few instructions. Input/output operations are equally simple: block reads and writes, creation and deletion of files, and positioning of the cursor (point of reading/writing) within a file. The run-time support for a source language like Common LISP, which has many built-in procedures, is written entirely in MIL itself, and compiled using MIPRAC, so that this portion of the run-time system will not require porting. We are concentrating upon the efficient translation of the intermediate form into the Alliant/Cedar instruction set. One especially interesting aspect of the run-time system and code generator is its automatic storage reclamation. The run-time system will not use a conventional garbage collector, but rather will automatically deallocate objects according to their lifetimes, as determined by the interprocedural analysis. This means, for one thing, that we will support automatic storage reclamation for C programs. For another, it means that the system will have the desirable aspects of concurrent garbage collection (no lengthy pauses in processing to reclaim storage). The reclamation algorithm is particularly simple to implement, but its success will ultimately depend entirely upon the accuracy of the interprocedural analysis.

Multiprocessor Performance on Algorithms and Applications

In the past year, the Applications Group in the Center has been involved in two main activities:

1. The design and implementation of various hierarchical numerical algorithms that take advantage of the three levels of parallelism of the four-cluster Cedar in which each cluster contains four vector processors (e.g., the 4x4 Cedar).
2. The parallelization of several large-scale application codes in ocean modeling, crash worthiness, and thermal hydraulics, and their implementation on Cedar.

Algorithm development on Cedar

Several parallel algorithms have been developed for implementation on the 4x4 Cedar in which each cluster memory consists of 2MW and a global memory of 2MW with a modified intermediate global network. These algorithms deal with crucial parts in important applications:

SPIKE: A Hierarchical Parallel Block-Tridiagonal System Solver

The solution of large banded diagonally dominant or symmetric positive definite linear systems constitutes one of the most common computational tasks associated with implementations of the finite element method in applications such as fluid dynamics and structural analysis. The design of multiprocessor algorithms for solving large block-tridiagonal systems becomes of paramount importance for efficient implementation of these applications on vector and parallel machines. In [Berr90], we discuss the design and implementation of a hierarchical-based method, SPIKE, for solving these systems on the 4-cluster (16-processor) Cedar machine. We compare the performance of SPIKE with that of an efficient block Gaussian elimination scheme, BGE, on an 8-processor Alliant FX/80. Results for the SPIKE algorithm on CEDAR block-tridiagonal system of order 16384 with block size 16 indicate speedups of greater than 6.5 vs. the best segmental scheme and a speed improvement of 11.5 vs. SPIKE on one processor.

A Symmetric and Antisymmetric Domain Decomposition in Structural Mechanics

Domain decomposition has recently become a topic under intensive research (see [GGMP88] and [CGPW89] for references). The symmetric and antisymmetric domain decomposition introduced in [Chen88] and [ChSa89a&b] is ideally suited for problems in structural mechanics. It is ideally suited for multiprocessors such as Cray Y-MP, Cray-2, Alliant FX/80, and Cedar. Unlike other methods that decompose the symmetric and antisymmetric response of a structure (e.g., see [NoPe87a&b], [BrDM88], [DoSm88]), our scheme exploits special properties of reflexive matrices to decompose stiffness matrices into several independent subproblems. Speedups realized for 2-D and 3-D elasticity problems on an Alliant FX/80 vs. the best sequential solvers range from 5.5 to 7.0 (out of a maximum of 8) depending on the problem. For the three levels of parallelism of Cedar, speedup of 9 (out of a maximum of 16) is realizable (see [Chen90]), even on unsymmetric structures that can be preconditioned using the symmetric and antisymmetric domain decomposition on the symmetric structure which is considered as a small perturbation of the original problem.

The Block Cimmino Method

The block Cimmino algorithm is a row projection scheme for nonsymmetric indefinite linear systems with arbitrary spectral distributions [Bram89], [BrSa90a]. The method can be more robust than other commonly used iterative solvers such as conjugate gradients (CG) on the normal equations or Krylov subspace based methods such as GMRES*(k)*. The most time-consuming part of the algorithm involves forming matrix-vector products, with a matrix that is the sum of orthogonal projectors. For structured problems such as those arising from discretizations of partial differential equations, each projection can be computed as a set of parallel tasks, each such task having some vectorization possible. Block Cimmino is thus especially suitable for the Cedar architecture, because the algorithm allows the necessary three levels of parallelism. A particular implementation is described and tested on Cedar [Bram90], showing speedups of 11 (out of a maximum of 16) that are realizable even on modest size problems.

Parallel Elliptic and Parabolic Problem Solvers

A rapid elliptic solver based on a parallel block cyclic reduction scheme [GaSa89] has been implemented on 2x4 Cedar with favorable results [Fran90]. Further, algorithms based on the conjugate gradient schemes, with and without preconditioning, have been implemented on Cedar [MeEi90] for self-adjoint elliptic problems on regular domains, and on T-shaped domains with the Schwarz alternating procedure [GaFM90].

Parallel algorithms for solving linear parabolic problems via implicit methods, based on Pade and Chebyshev rational approximation to matrix exponential, are implemented on the 4x4 Cedar. The algorithms are ideally suited for the hierarchical memory organization of Cedar and realize high speedup vs. the classical sequential Crank-Nicolson scheme. Moreover, these algorithms are those of choice if the goal is to compute the solution at a given time point as quickly as possible.

Direct Sparse System Solvers

In this activity we have developed two solvers:

1. McSparse [GaMW90] - This algorithm is ideally suited for large grain parallelism that takes advantage of the multicluster organization of Cedar. This algorithm consists of two stages. The first uses a hybrid ordering [Wijs89b] which produces (on most general sparse matrices) a block sparse upper triangular matrix. A sparse block Gaussian elimination procedure (with pivoting) produces an LU-factorization using the four clusters of Cedar with reasonable load balancing.
2. DSPACK [Yang90] - This algorithm was designed to test Cedar as a "flat" multiprocessor which utilizes mainly the global memory and capitalizes on the fine-grain parallelism of the 16-CE Cedar. In spite of lack of explicit utilization of the individual cluster memories, speedups of around 6 (out of a maximum of 16) vs. the best sequential scheme are realizable.

Multiprocessing of Large Scale Codes

The purpose of this project is to apply techniques of paral'el computing to mature computational fluid dynamics (CFD) and structural dynamics (SD) computer codes. Specifically, although the power and utility of parallel computers and the corresponding software development techniques have been demonstrated on small scale prototype problems, full-scale production use has lagged behind because parallelizing large engineering codes requires coordination and interaction among engineers (who understand the physical problem being modeled), numerical algorithm designers (who specialize in designing efficient algorithms to solve basic computational problems), and performance evaluation experts (who build software tools and machine models that enable the design of efficient programs for a specific computer). For this effort, we are collaborating with another DOE site, Argonne National Laboratory, combining our expertise to bear on industrially important problems. We are also continuing our work on a problem of concern to environmental activities, namely the multiprocessing of a state-of-the-art ocean circulation model (OCM).

Upon completion, we expect two major results. First, the very process described above will expose the strengths and weaknesses of existing techniques for parallelizing programs and will identify those problems that need to be solved in order to enable widespread production use of parallel computers. Second, the increased efficiency of the CFD and SD codes will allow the simulation of larger, more accurate engineering models. In particular, we hope that the work could serve as an exemplary model for similar future activities.

Our main parallel machines are the 4 CPU Cray X-MP and Y-MP, Alliant FX/80 and FX/2800 and Cedar.

Parallel Ocean Circulation

Global ocean circulation modeling is an important component of climate prediction studies. In an effort to conduct faithful simulations, one needs considerable computational power and storage capabilities. Interest in such efforts is evidenced in DOE's recent CHAMMP initiative. Much pioneering work in the parallelization of ocean global circulation modeling has been conducted by Semtner and Chervin for the Cray. Our interest is to build models that profit from computational and memory hierarchies for good performance. We hope that such models will maintain good performance as machine and problem size scale.

In cooperation with A. Navarra from IMGA-CNR, Modena, Italy we are developing a parallel version of a state-of-the-art model of circulation in the Mediterranean basin. The model is based on the ocean circulation codes from GFDL, Princeton University, and simulates the basic aspects of large-scale baroclinic ocean circulation. A preliminary multicluster Cedar implementation of the code has been completed. In this phase of the work we have concentrated on the aspects of the code not dealing with the two-dimensional relaxation procedure, used to compute transport streamfunction The two models of interest consist of 167 x 57 x 8 and 334 x 118 x 16 gridpoints respectively. The smaller model is used primarily to allow some performance evaluation of a single cluster code, since the large model is slowed down considerably on one cluster due to paging. For example, Figure 4 shows the effect of using four clusters of Cedar relative to the performance of the eight advanced computational elements of the Alliant FX/80. The times for one and two Cedar clusters are very large due to the small memory available compared to that of the FX/80 and the paging behavior. Figure 5 corresponds to the smaller model. It shows that the two clusters of Cedar (8 CEs) perform almost as well as the eight faster Advanced CEs of the FX/80.

Tables 1 and 2 show the times, speedups, and efficiencies for each of the phases of the calculation. The three-dimensional computations have been distributed across the clusters. The relaxation was left on one cluster as we are currently implementing a multicluster version.

All the multicluster Cedar speedups we have shown are constrained by our not parallelizing the two-dimensional relaxation. This, together with the evaluation of different data-partitioning techniques constitutes our next task in the project.

COMMIX and WHAMS

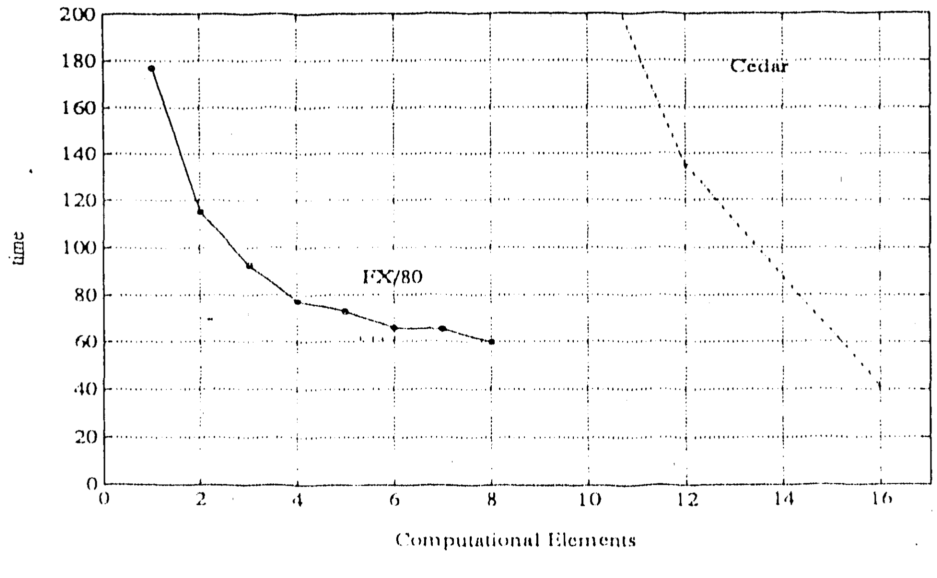


Figure 4. Preliminary performance of OCM on Alliant FX/80 and Cedar for 3 time steps of 334 x 118 x 16 grid.

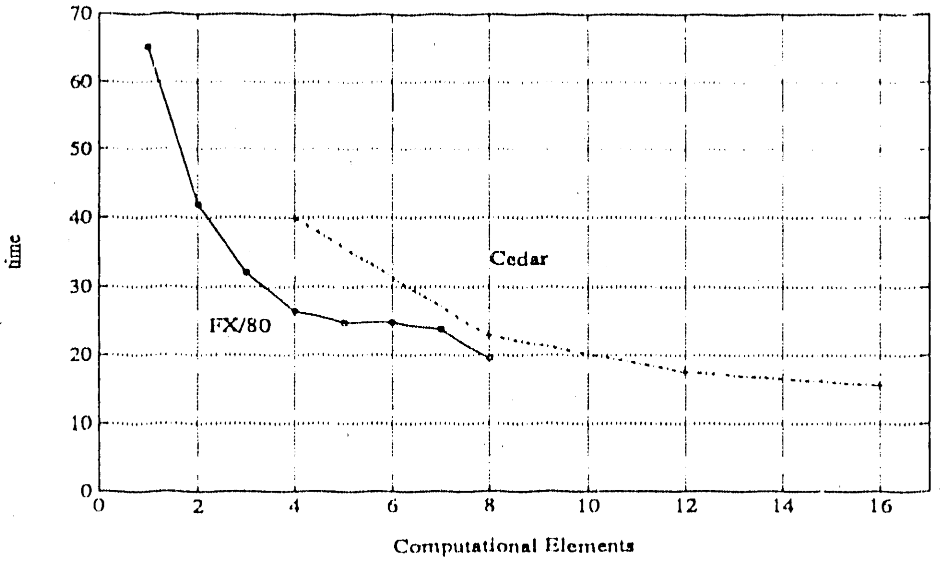


Figure 5. Preliminary performance of OCM on Alliant FX/80 and Cedar for 10 time steps of 167 x 57 x 8 grid.

proc.	number of clusters			
	1	2	3	4
startup	0.03	0.03	0.03	0.03
3D phase	36.62	18.88	13.26	10.98
relaxation	3.55	3.79	3.58	3.62
total	40.20	22.70	16.87	15.03

Table 1. Small ocean model running 10 time steps (preliminary).

Clusters (CE)	Speedup	Efficiency	Speedup for 3D ph.	Eff. 3D ph.
1 (4)	1.00	1.00	1.00	1.00
2 (8)	1.77	0.89	1.94	0.97
3 (12)	2.38	0.79	2.76	0.92
4 (16)	2.67	0.67	3.33	0.83

Table 2. Small ocean model running 10 time steps (preliminary).

COMMIX and WHAMS-3D are two production codes that have been developed at ANL and are widely used by industry and government laboratories. The first is a computational fluid dynamics code that is used for both nuclear reactor design and safety and as a design tool for the casting industry. COMMIX 1-ARP consists of approximately 30,000 lines of code across 150 subroutines [BIGG89]. WHAMS-3D is a three-dimensional structural dynamics code used in nuclear reactor safety as well as crashworthiness studies [BeTs82]. Both codes are available for both sequential and vector computers only. Our main goal is to optimize these two codes on shared memory multiprocessors. The first phase of this project has been completed and fully documented in [ABCG90]. It consisted of an intense profile study of both codes using data sets typically used by ANL for testing the validity of the codes.

Argonne's development and refinement of COMMIX, which has continued for more than ten years, was originally supported by the U.S. Nuclear Regulatory Commission for application to a wide variety of reactor safety problems. COMMIX has been developed using a unique porous media approach to the solution of the Navier-Stokes equations in an arbitrary three-dimensional region. In its various versions, COMMIX can model separate single-phase fluids, multiphase flows, and free surface flows. The code uses differenced momentum/mass conservation equations which are combined to form a pressure equation. Once the pressures are known, the fluid velocities are updated to provide input to the energy simulation and the next iteration or time step. The hydraulic driving force may be flow or pressure boundary conditions at inlets and outlets, one of several pump models, or a fluid temperature/density distribution. The energy equations are differenced using the updated velocities, and the source terms are accumulated from the treatments of convection boundaries, conduction boundaries, thermal structures, or heat generation in the fluid itself. One-dimensional shell structures superimposed on the fluid geometry model various fluid system thermal components such as vessels, pipes, baffles, tube-shell heat exchangers, and reactor fuel. Once the fluid temperature distribution is updated, the submerged thermal structures' internal temperature distributions are recomputed, assuming one-dimensional conduction through each thermal structure segment.

The momentum and fluid energy equation time differencing is implicit, which requires that the difference equation coefficients be constructed from end-of-timestep temperatures and velocities. The pressure equations of the mass-momentum loop are solved using conjugate gradient (CG) with incomplete Cholesky factorization preconditioning.

A large amount of the computing time is spent constructing matrix equations, a process that would require massive recoding to vectorize because of its large, logic-loaded loops. Such loops, however, are expected to lend themselves very well to the parallelization efforts which we plan to pursue in the context of this work.

We next list the function of the most important routines in the set:

energi	Construct coefficients in the energy equation.
lowfcv	Solve the upper and lower triangular system as part of the conjugate gradient solution of the pressure equation.
peqn	Construct the coefficients in the pressure equation.
qstrds	Calculates finite differences of solid/fluid heat transfer rate over the thermal structures.
qstruc	Set solid-to-fluid source term for the fluid energy equation.
solvev	Solver of linear system for the energy equation using Gauss-Seidel relaxation on red-black ordering.
xmomi, ymomi, zmomi	Sweep over all fluid cells to set-up the x, y, and z direction momentum equations.

Table 3 summarizes the runtimes for each of the machines and compilation options for two typical data sets, P1r0 (steady-state calculation) and P1r2 (transient calculation). The compilation options S,V,C stand for scalar, vector, and concurrent optimization. The notation SV(Zv) stands for enhanced vectorization.

Routine	P1r0	P1r2
Cray SV	93.96	920.94
Cray SV(Zv)	81.48	872.90
Cray SVC	225.25	2025.48
1 CPU	22.35	297.28
2 CPU	31.76	405.18
3 CPU	47.19	461.88
4 CPU	123.95	861.20
Alliant FX/80		
SV (1 CE)	1,322.4	12,331.2
SC (8 CE)	1,128.7	10,015.0
SVC (8 CE)	1,136.7	10,048.6

Table 3. Execution times for SV, SV(Zv) and SVC COMMIX-1AR/P on the Cray X-MP/48 and Alliant FX/80.

Data set	P1r0		P1r2	
Routine	SV	SV(Zv)	SV	SV(Zv)
QSTRDS	6.20	6.68	6.19	6.69
ZMOMI	6.42	7.19	6.42	7.15
ENERGI	6.06	6.61	6.06	6.64
SOLVEV	10.29	36.28	10.37	33.51
YMOMI	6.97	7.78	6.97	7.81
QSTRUC	6.67	7.28	6.66	7.29
PEQN	3.05	3.49	3.06	3.50
XMOMI	6.93	7.82	6.93	7.84
LOWFCV	30.98	34.12	30.99	34.57
Overall	9.12	11.76	7.68	8.76

Table 4. MFLOPS profile of the most time consuming subroutines in baseline scalar-vector, and enhanced vectorization -Zv compilation modes for the COMMIX-1AR/P code running on Cray X-MP using data decks P1r0 and P1r2 (from PERFTRACE).

Table 4 shows that the best MFLOPS rate is achieved for the **solvev** and **lowfcv** subroutines, for a performance far superior to all other listed subroutines. These have been written to take advantage of vectorization and thus perform at more than 30 MFLOPS on one CPU of the Cray X-MP. This is in contrast to a meager average of 6.5 MFLOPS for those sections of the code working on the task of matrix construction. This of course causes the overall performance to drop to almost 11 MFLOPS, even for the full vector optimization. It is thus clear that a first step in improving the performance of the code is going to be the restructuring of the matrix construction phase.

Table 4 indicates a great deal about the nature of the work to be done during the next phase of this project:

1. The difference in performance for **solvev** under the different compilation options tells one about the ability of restructuring compilers to take advantage of the machine capabilities, if the code is written properly. It also shows that the use of more sophisticated restructurers can be very beneficial. We should keep in mind however that **solvev** was coded for vector processing.
2. The high performance of **lowfcv** for both SV and SV(Zv) shows that even a less sophisticated restructurer can do well if it has some help from the user (in the form of inline directives).
3. The low performance for both SV and SV(Zv) options for all other routines shows that there is work to be done until these commercial compilers can handle satisfactorily dusty-decks. ("Dusty-decks" as the matrix assembly routines were not coded to take advantage of the architecture.) We will thus investigate the use of novel restructurers as part of Phase 2 of our work.
4. The overall low performance for both compilation options, and the small difference among the two, shows that it is dangerous to concentrate only on those stages of the code that are related to well-defined algebraic computations in need of new algorithms (e.g., linear system solvers), at least until the automatic transformation tools become more powerful.

An important goal of this work is to demonstrate the effectiveness of multiprocessing for these codes applied to industrial-strength data sets. We have secured such sets from the Thermal Hydraulics Section of Commonwealth Edison, including a 12-hour simulation when performed on one vector processor of an IBM 3090.

The WHAMS-3D computer program employs explicit time integration to do nonlinear, transient analysis of frames, shells, plates, and continua in three dimensions. Both material nonlinearities due to elasto-plastic behavior and geometric nonlinearities due to large displacements can be treated. This program has been developed jointly at Northwestern University and Argonne National Laboratory and is internationally recognized as a state-of-the-art program for performing nonlinear transient analysis. The program employs a finite element format, so that it possesses considerable versatility in modeling complex shapes and boundary conditions. The element library consists of the following: quadrilateral and triangular plate-shell elements, a beam element, a spring element, and a hexahedral continuum element. In addition, a rigid linkage is included which permits the efficient modeling of very stiff portions of a structure, such as the bottom ring of a core barrel. In a rigid linkage, the motion of a master node defines the motion of all slave nodes linked to the master node. This option is also useful for eccentrically connected elements where the midlines of the connected elements do not coincide, as, for example, in stiffeners. All of the elements in the program are three dimensional. Table time steps can be automatically computed or input by the user or a driving program. Mixed time integration, a procedure that allows for different time steps in different parts of the mesh, may be employed.

The performance results of the original code WHAMS3D on the Cray X–MP/48 for several input data decks are presented in Tables 5 to 7. Table 5 shows the execution

Version	Execution Time			
	buckle	cylpanel	frame	spcap
S	59.19	391.19	4048.66	88.02
SV	9.73	64.11	650.07	14.72
SVC	9.66	61.53	633.92	15.30

Table 5. Execution times for WHAMS–3D on the Cray X–MP/48 (from HPM).

No. of Concurrent CPUs (i)	Connect time (T_i) in each CPU			
	buckle	cylpanel	frame	spcap
1	3.15	19.66	162.35	5.99
2	0.59	9.92	131.54	1.88
3	2.45	12.30	147.89	4.34
4	3.47	19.74	211.34	3.08
Total exec. time	9.66	61.63	653.12	15.30
Total CPU time	25.54	155.37	1714.46	35.10

Table 6. Execution times for SVC version of WHAMS–3D on the Cray X–MP/48 (from HPM).

Version	MFLOPS			
	buckle	cylpanel	frame	spcap
S	11.36	11.50	11.37	11.25
SV	71.00	71.65	72.65	69.05
SVC	71.38	74.49	76.97	66.56

Table 7. MFLOPS for WHAMS–3D on the Cray X–MP/48 (from HPM).

time for all four data sets. As can be seen from this table, the vector speedup of the SV version over the S version ranges from 5.98 for the data set *spcap* to 6.23 for *frame*. It is also observed that the SVC version does not yield good performance although four CPUs are available.

We have started using tools developed at CSRD to capture the detailed histories of routine invocation together with machine performance statistics. The goal is to study performance behavior at a more refined level using trace data of routine entry and exit actions. We used tracing tools developed for the Cray X–MP and Cray 2 which are described in [MaLR90]. In summary, these tools can capture detailed histories of routine invocation together with machine performance statistics. The produced trace graphs visually depict where time is being spent in routines during the execution and the routine calling dynamics as the application proceeds.

Part of our work has concentrated on the effectiveness of using software tools to detect opportunities for parallelism. It is clear that the greatest potential for improvements, and consequently the biggest challenge, lies in the substitution of the key algorithms in the application code with redesigned algorithms which exploit the new architectures and use better numerical techniques. This will constitute a major activity of this project. We have already started work in evaluating the effect of numerical algorithms more amenable to parallelization and their effect on the codes. For example, we are studying the behavior of and alternatives to the use of CG with incomplete Cholesky preconditioner in COMMIX.

Overall the first phase has shown that significant improvements in the codes' performance result from vectorization. This is partly because of the effectiveness of vectorizing compilers, and partly because the principles of vectorization have been available to programmers for more than 15 years. The results of the first phase also show that applying existing automatic restructurers for multiprocessing gives little improvement or even degradation in performance, but provides clues on how to achieve better results.

Perfect Benchmarks™

Success in the field of parallel computing must be calibrated by measuring the performance gains made on real applications programs. A number of examples in this progress report use applications codes drawn from the Perfect Benchmarks ™, which are a collection of 13 applications level Fortran programs totaling over 60,000 lines of code. The effort has been collective with early participation from academia (University of Illinois, Princeton, Caltech, Florida State), industry (Cray, IBM) and various research centers (Houston Area Research Consortium, Institute for Supercomputer Research - Tokyo, NASA-Ames).

The programs were chosen to satisfy various constraints, including portability, breadth of application areas, reasonable running times and perhaps most importantly maturity and popularity of the codes themselves (see [Berr89, CKPK90] for more discussions about the effort and references on each of the codes). It is important to note that each Perfect code represents more than a Fortran program in that it solves a well defined scientific or engineering problem. Initially, the codes were ported to and timed on 8 machines [Berr89] and subsequently the process has been repeated on more than 20 additional machines. Insight into system software and architecture is sought, not just benchmarking numbers. The Perfect Benchmark ™ program is a collaborative effort, and contributions such as new codes or new analysis techniques are welcome and encouraged at all times.

The Perfect benchmarking effort strives to collect baseline and optimized execution statistics. A baseline measurement involves running the code as is, with only those program changes necessary for porting allowed. Note that all the Perfect codes were originally written for and used on some high-performance system; thus certain performance biases were built-in to the data, as would be the case with any such real-world collection of codes. After a baseline measurement is made, the user is encouraged to undertake any kind of program rewriting to improve performance. Diaries describing program transformations, which include loop reordering, subroutine in-lining, library routine substitutions or algorithm replacement for example, are to be kept. Loosely speaking, in a baseline measurement the original Fortran program is an invariant while in an optimized execution the scientific problem is invariant.

Table 8 contains some basic information about the Perfect codes.

Perfect Performance Data

Each of the 13 Perfect Benchmark™ codes is a stand alone program that uses no external library calls and upon successful execution creates an output file containing execution times, a MFLOPS rate and the results of a validation check. Both wall clock and CPU time are recorded. The derived MFLOPS rate on all machines is based on a reference floating point operation count obtained by the Cray XMP hpm. The validation check is performed by comparing known correct output values against the values computed by the current execution. The comparison is not always exact but uses a meaningful threshold that was determined by the code's author or maintainer at the time the code was included in the benchmark suite. The validation check has turned out to be quite useful since there are numerous reported incidents involving precision problems and incorrect code generation by buggy compilers, even though a code may compile, execute and terminate.

The Center for Supercomputing Research and Development at the University of Illinois publishes periodic reports containing tabulations of results. The last report contained over 40 tables of raw data on about 30 machines' performance [Poin90]. Efforts have been made to port codes to massively parallel machines but such endeavors are labor intensive and only two codes have been run successfully on hypercube-type machines at Caltech. The Perfect Benchmark™ database contains no results on SIMD machines for the same reason.

Observations

The Perfect Benchmark™ data demonstrates the complexity of computer systems performance. Put another way, no single number captures performance in any meaningful way and, conversely, efforts to quantify performance by a single number are intrinsically oversimplified. However, some general observations based on the totality of data are possible.

1. *Delivered performance is significantly lower than peak performance and is growing at a slower rate.* Figure 6 is a scatterplot of Perfect code performances on various supercomputers of the 1980's. It clearly illustrates that the correlation between peak performance and delivered performance is weak. It should be noted that the Perfect Benchmarks™ are by and large complete applications, in some cases with scaled down problem sizes that may lead to poorer performance. Machine performance on more homogeneous, simpler algorithms could be significantly higher. This gap between peak and delivered performance reaches two orders of magnitude in Figure 6 and will become even more dramatic as machines with more processors and/or functional units become available.

2. *Increased performance leads to increased performance variations.* Variations in performance, quantified as the ratio between maximum and minimum delivered megaflops, are correlated with peak performance as can be seen from Figure 6. Calling this ratio *instability*, higher performance machines appear to be more unstable because of advanced hardware features that are difficult to take advantage of uniformly. Note that instabilities also approach two orders of magnitude in Figure 6. Further development of the notion of instability is currently underway at CSRD.

3. *Porting applications level codes to hypercubes and SIMD machines is difficult so that comprehensive applications-based benchmarking of these classes has not been possible to date.* After three years, only two Perfect codes have been successfully ported to hypercube machines and none to SIMD machines. This is a particularly troubling fact since much of the current enthusiasm over existing massively parallel machines is based on the performance of simple algorithms.

Conclusion

As stated throughout this report, much progress has been made not only on the Cedar hardware, operating system, applications and algorithms, but also in advancing the state of the art. Further emphasis must be placed on much that is left to do. We are on the verge of more breakthroughs in parallel processing which has been acknowledged to be the means to achieving truly high performance computing.

Code Name	Lines of Code	Application	Contributor	Algorithms Used 1	2	3	4	5	6	7	8	9
ADM	6105	Air pollution, Fluid dynamics	IBM	.	.	x	.	.	.	.	.	.
ARC2D	3964	Supersonic reentry, 2-D fluid dynamics	NASA Ames	x	.	.	x	.	.	[illegible]	.	.
BDNA	3977	Nucleic acid simulation, Molecular dynamics	IBM	.	.	.	.	.	x	.	.	.
DYFESM	7608	Structural dynamics, Engineering design	CSRD	x	x	.	.	.	x	.	.	.
FLO52	1986	Transonic flow, 2-D Fluid dynamics	Princeton	.	.	.	.	x	x	.	.	.
MDG	1238	Liquid water simulation, Molecular dynamics	IBM	.	.	.	.	.	x	.	.	.
MG3D	2812	Seismic migration, Signal processing	Cray	.	.	x	.	.	x	.	.	.
OCEAN	4343	Ocean simulation, 2-D fluid dynamics	Princeton	.	.	x	.	.	.	.	.	.
QCD	2327	Lattice gauge, Quantum chromodynamics	Caltech	.	.	.	.	.	.	x	.	.
SPEC77	3885	Weather simulation, Fluid dynamics	CSRD	.	.	x	x	.	.	.	.	.
SPICE	18521	Circuit simulation, Engineering design	CSRD	x	.	.	.	.	x	.	.	.
TRACK	3784	Missile tracking, Signal Processing	Caltech	.	.	.	.	.	.	.	.	x
TRFD	485	2-electron transform integrals, Molecular dynamics	IBM	.	.	.	.	.	.	.	x	.

Algorithms:

1. Sparse Linear Systems Solvers
2. Nonlinear Algebraic System Solvers
3. Fast Fourier Transforms
4. Rapid Elliptic Problem Solvers
5. Multigrid Schemes
6. Ordinary Differential Equation Solvers
7. Monte Carlo Schemes
8. *Integral Transforms*
9. Convolution

Table 8. The Perfect Benchmarks ™.

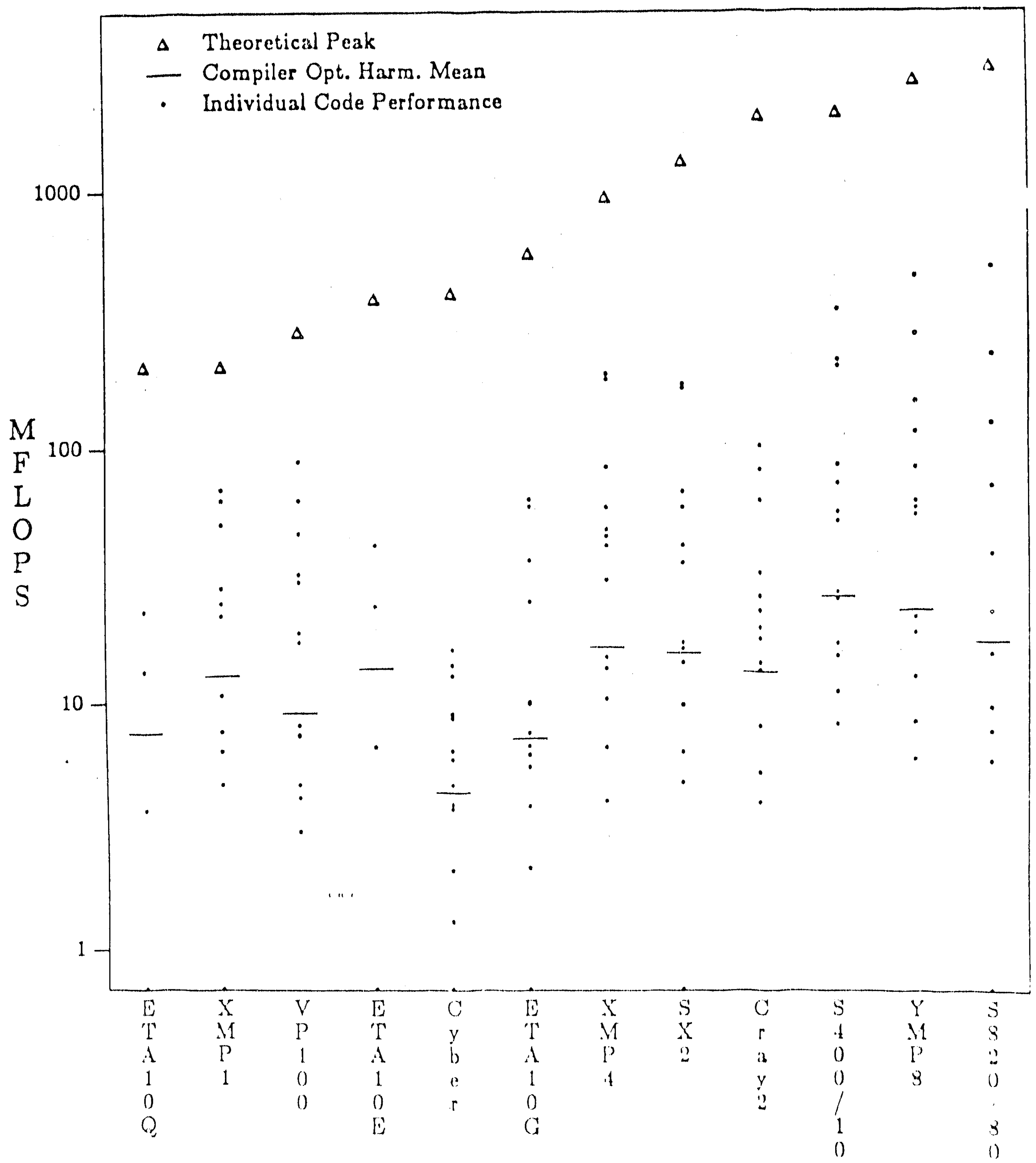


Figure 6. Instability Scatter Plot.

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