

SAND 97-2997C
SAND--97-2997C

IMPROVED DESIGN OF OPTICAL MEMS USING THE SUMMIT FABRICATION PROCESS

CONF-980514--

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ABSTRACT

This paper describes the design and fabrication of optical microelectromechanical systems (MEMS) devices using the Sandia Ultra-planar Multi-level MEMS Technology (SUMMIT) fabrication process. This state-of-the-art process, offered by Sandia National Laboratories, provides unique and very advantageous features which make it ideal for optical devices. This enabling process permits the development of micromirror devices with near-ideal characteristics which have previously been unrealizable in standard polysilicon processes. This paper describes such characteristics as elevated address electrodes, individual address wiring beneath the device, planarized mirror surfaces, unique post-process metallization, and the best active surface area to date.

KEYWORDS: Optical MEMS, MOEMS, SUMMIT, Micromirrors

INTRODUCTION:

Micromirror devices have become some of the most recognized and useful spatial light modulators (SLM) and have been successfully implemented in recent years in a variety of military and commercial systems. The designers of these devices, however, are faced with a number of engineering compromises which prevent near-ideal operation. For instance, many forms of micromirrors fabricated in the standard three-layer polysilicon process known as Multi-User MEMS Process (MUMPS) have been designed with reduced reflective surface area in order to make room for the flexures which support the mirror or were scarred with serious topographical effects in the reflective surface due to features fabricated beneath it [1]. Both drawbacks were previously unavoidable in most, if not all, commercially available surface-micromachining fabrication services.

Ideally, an advanced fabrication process would remove these and other drawbacks so that a more functional micromirror device can be realized. The devices studied in this paper were fabricated in such a process. Ultimately, the designer is able to develop micromirrors and other optical micromechanical structures with dense wiring beneath the device for large arrays, raised address electrodes, thin flexures for reduced address potentials, planarized mirror surfaces, and only 1 μm design rules which make possible an active surface area of 98% or better. Added to this, several design techniques such as metallization shielding, shorting, and trapped oxide wiring can be employed to further enable the designer to optimize micromirror devices.

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MICROFABRICATION:

As in most surface-micromachining polysilicon processes, micromechanical devices are formed by the alternate deposition of structural polysilicon layers and sacrificial oxide layers. The polysilicon layers are patterned (using the same advanced photolithography technology employed by the microelectronics industry) to form intricate structures such as motors, gears, mirrors, and various sensors. Cuts made through the oxide layers are used to anchor the upper structural levels to the silicon substrate or underlying structures. At the end of the process the sacrificial layers, as the name suggests, are removed using a variety of methods, such as a hydrofluoric acid release etch, which frees the device to move relative to the substrate.

The complexity of the micromachines which can be manufactured in a given process is a function of the number of independent layers of structural material the technology provides. A single independent level of structural material limits designers to simple sensors whereas geared mechanisms require two independent levels (one to form the hubs and the other the moving gears) and motorized geared mechanisms require a minimum of three independent levels. Far more complex mechanisms and systems require even more layers. Figure 1 illustrates this concept with micrographs and cross-section drawings of these devices of varying complexities:

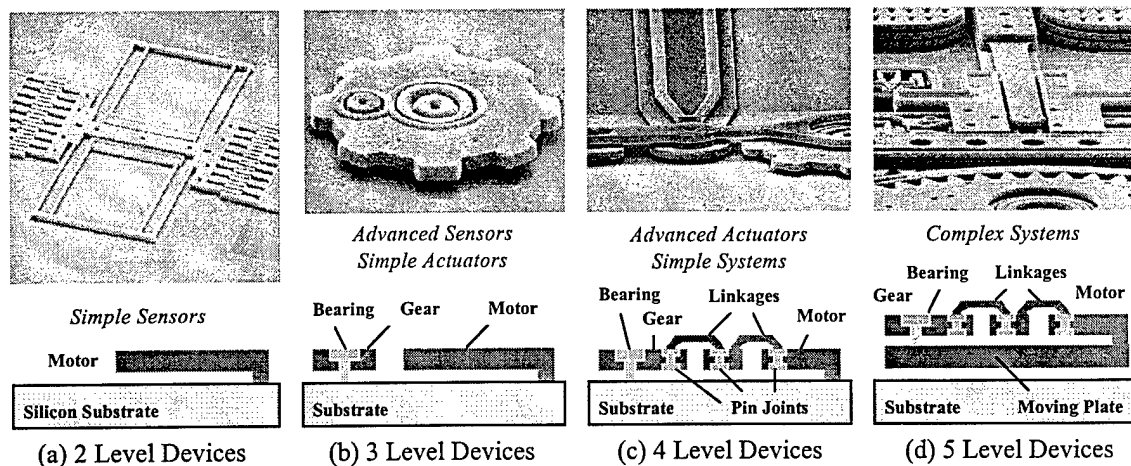


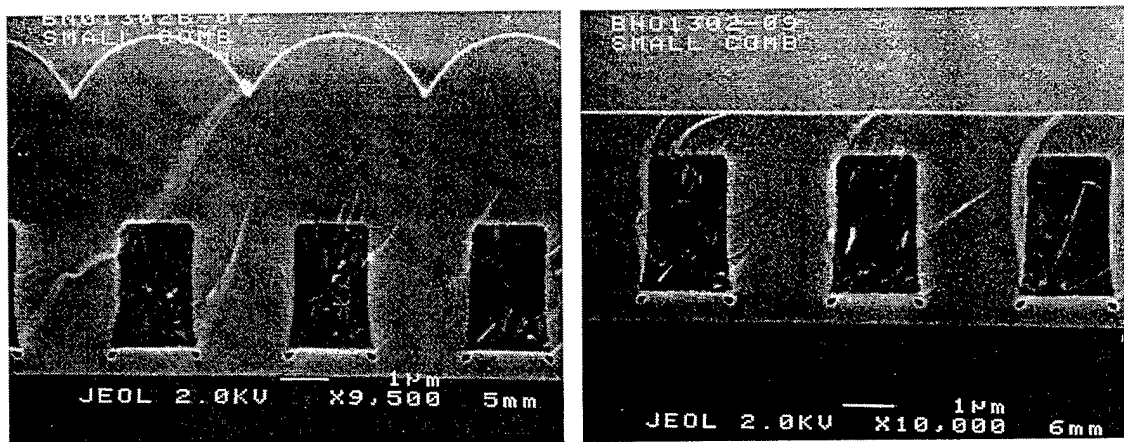
Figure 1. Device complexity relative to the number of available structural layers.

Using some of the more common fabrication services, designers have typically been faced with a variety of problems and limitations which prevent the ideal optimization of devices. For instance, most processes have conservative design rules and minimum feature sizes which reduce the area of active surfaces or stretch the mechanical tolerances of joints and linkages. The conformal deposition of upper polysilicon layers over features patterned in underlying layers can create very adverse topographical effects which can either hinder or even prevent the operation of the device. Furthermore, these layers are typically plagued with high internal stresses which cause deformations or other undesirable mechanical behavior. Finally, and probably most significantly, even the most advanced of commercial services offer a maximum of only two releasable layers of structural material. If highly complex micromechanical systems are to be realized, far more advanced fabrication services must address these limitations.

ADVANCED PROCESS TECHNOLOGY:

The micromirror devices presented in this paper were fabricated in the Sandia Ultra-planar Multi-level MEMS Technology (SUMMiT) process commercially available through the Sandia Agile MEMS Prototyping, Layout tools, and Education (SAMPLE) service [2]. The SUMMiT process is the only commercial MEMS process in the world to offer three releasable structural layers (Poly-1 through Poly-3) above the ground layer (Poly-0). It also offers a planarized upper layer and a unique "pin joint" cut, shown in Figure 1(c), for making rotating joints. Additionally, as shown in Figure 1(d), recent improvements to this process include a fourth releasable layer (Poly-4) which is also planarized [3]. This process is not yet commercially available, but will soon make highly complex and intricate micromechanical systems easily realizable.

The current SUMMiT process offers state-of-the-art advantages over standard processes which include planarization of the upper polysilicon layer, ultra-low-stress structural material, design rules and feature sizes of only $1\text{ }\mu\text{m}$ with $0.1\text{ }\mu\text{m}$ mask resolution, and the ability to make flanged gear hubs. The planarization eliminates any unwanted mirror surface topography which is normally induced by the conformal deposition of one layer over the mechanical features of the underlying layers. As shown in Figure 2, the uppermost sacrificial oxide is planarized using a technique of Chemical Mechanical Polishing (CMP) so that the following structural layer is flat [4].



(a) Normal oxide deposition profile

(b) Planarized oxide surface

Figure 2. Micrographs of uppermost oxide layer before and after CMP planarization.

The entire wafer is placed face down in a chemical slurry and slowly polished so that the normal oxide deposition profile, shown in Figure 2(a), is ground into a planarized surface, shown in Figure 2(b). Without this process step, as can be seen in Figure 2(a), the succeeding layer of polysilicon would conform to the oxide and result in a deformed surface which is not suited well to optical applications or complex mechanical motion. Furthermore, the deposition of ultra-low-stress polysilicon developed by Sandia enables SUMMiT designers to use larger expanses of structural material without concern that the device will curl due to internal stress. As a result of these advanced process technologies, first-generation test micromirror devices demonstrated less than 17 nm of total curvature across several $100\text{ }\mu\text{m}$ surfaces. Recent enhancements to the process have included increasing the thickness of the uppermost polysilicon layer which further improves its stiffness for even flatter reflective surfaces.

MICROMIRROR DEVICE DESIGN:

Given the capabilities of the SUMMiT process, the design goal for this research was simply to create a variety of highly optimized devices which demonstrate improved performance over current micromirrors. The first and most valuable design characteristic of these optimized devices is the upper layer of planarized polysilicon which is used as the mirror surface. As illustrated in Figure 3, since it is the third releasable layer, the flexures and address electrodes can easily be placed under the surface of the device. The planarization of the mirror surface eliminates the standard design trade-off between mirror flatness and active surface area [1]. Using the SUMMiT fabrication process, the support features of micromirror devices can be hidden in order to maximize reflective area while completely eliminating adverse topographical effects in the mirror surface which would typically be observed as upper layers conform to underlying structures.

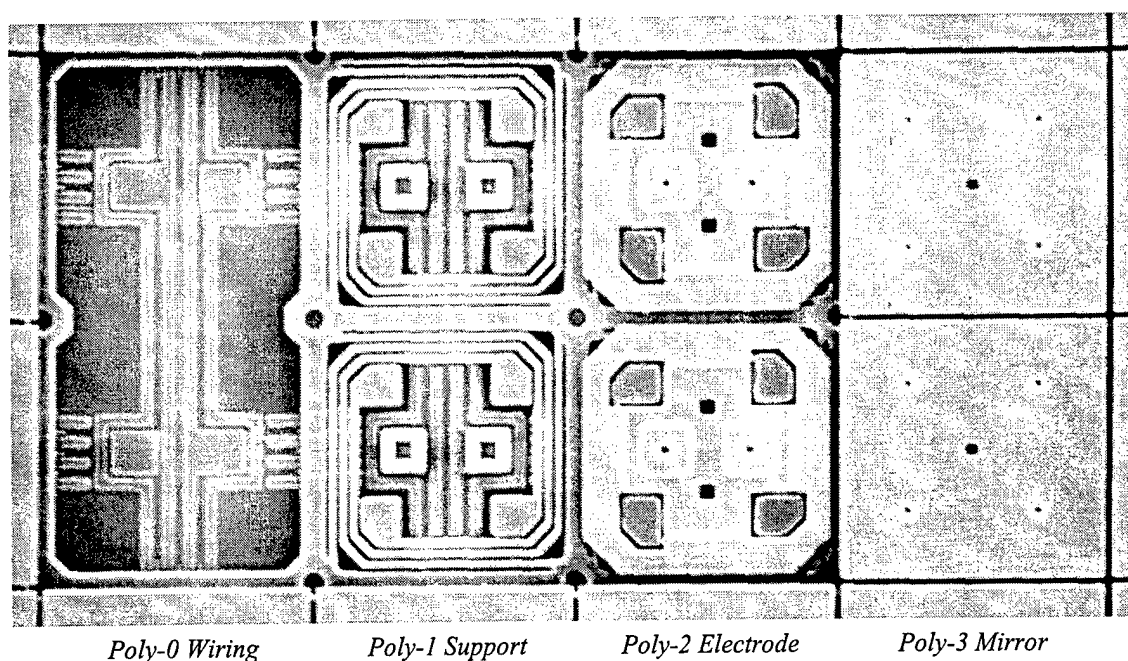


Figure 3. Micrograph of a hidden-assembly micromirror with planarized mirror surface.

Another design characteristic is the use of the additional layer of polysilicon provided in the fabrication process. With three releasable layers of varying thickness available to the engineer, micromirror devices can become more complex and be easily designed to behave as desired. For instance, the device shown in Figure 3 illustrates the use of these layers in order of fabrication. First, the Poly-0 wiring, which runs beneath the device, allows for large arrays of individually addressable devices. The Poly-0 landing pads shown between the wires are connected to the address electrode via support posts and are simply shorted to the address wire of choice. The compliant flexures are made in Poly-1 which is the thinnest (only 1 μm thick) of the structural layers in order to reduce the spring constant and therefore the address potential [5]. To further reduce the potential, the address electrode is elevated using the Poly-2 layer so that a resting separation of only 2 μm between the address plates is realized. The planarized mirror surface is formed in Poly-3 and is anchored to the flexures through holes cut in the address electrode. As a result of exploiting each layer in this design process, this device can be actuated at an address potential directly compatible with CMOS electronics.

POST PROCESS METALLIZATION:

A novel post-process metallization procedure was developed to create a reflective surface on micromirror devices. This technique can be used to deposit a desired material and thickness on micromirror arrays since the material does not have to survive the harsh release etch. The metallization shield is built into the design layout so that no post-process masking is needed. This shield isolates each bond pad and allows no address wiring to be exposed anywhere on the chip. It is beneficial to use this shield as the ground plane, so a significant margin around the bond pads must be maintained to prevent shorting during bonding and packaging of the chips.

This shield is also included in the micromirror design. Figure 4 shows a side view of the same micromirror device shown in Figure 3 in which a Poly-1 metallization gutter surrounds the device and runs beneath any gaps in the mirror surface. This gutter catches any material deposited by this post-process metallization so that the Poly-0 wiring is not shorted and the mechanical workings of the device are not hindered.

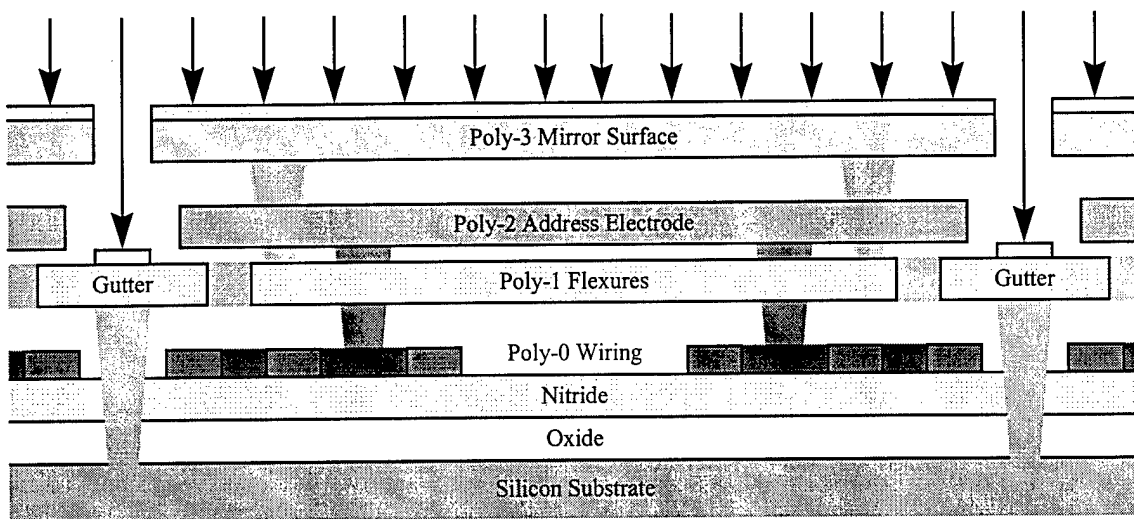


Figure 4. Use of metallization gutters to protect address wiring during metallization.

Post-process metallization can also be used to extend the functionality of test chips containing several large arrays of individually addressable micromirrors where the number of devices drastically outnumbers the bond pads that can be placed around the edge of the test chip. The micromirror arrays must be spaced approximately 250 μm apart so that a metallization mask can be roughly positioned to isolate an array of choice. A small window in the shield is fabricated directly over a small gap in the address wiring which connects the arrays of test devices to the primary address lines. These address lines are wired directly to the bond pads which creates an active network of address lines leading to each of the micromirror arrays. When a desired test array is masked and metallized, the wiring gaps are shorted, thereby connecting its devices to the bond pads. In order to strengthen the metallization shield during mask placement, the oxide and wiring beneath the shield was trapped so that the shield becomes a rigid surface firmly attached to the substrate. This metallization technique was successfully demonstrated by depositing 150 nm of gold using masking materials such as small strips cut from electrostatic discharge protection pouches, glass slides supported just above the test chip, and sheets of aluminum foil with pin-hole cuts placed above the arrays [6].

CONCLUSION:

This research has clearly shown the advantages of the SUMMiT process for the fabrication of highly-advanced micromirror devices demonstrating unprecedented active surface area of 98% or better. The advanced features of this fabrication process allow for the design of more complex micromirrors and significantly larger arrays of individually addressable devices. The near-ideal optical flatness and mechanical uniformity of these devices across the array make possible ultra-high optical efficiencies which are necessary for most adaptive optics, scanning, and projection applications. The number of structural layers permits the designer to create highly functional optical devices such as a variety of micromirrors, optical gratings, and complex three-dimensional systems which are erected above the surface of the substrate. Furthermore, the varying thickness of the structural layers allows the designer a wide range of mechanical properties from which to form devices. As a result, the address potentials of these micromirror devices can be easily tailored to suit the needs of the application. Finally, the post-process metallization and shielding technique developed specifically for these micromirrors can be used to deposit a material of choice onto reflective surfaces without concern for unwanted effects such as shorting address wires or hindering mechanical motion of underlying structures.

ACKNOWLEDGMENTS:

The portion of this work done at Sandia National Labs was supported by the U.S. Dept. of Energy contract DE-AC04-94AL85000. Sandia is a multiprogram laboratory operated by Sandia Corporation, a Lockheed Martin Company, for the U.S. Dept. of Energy.

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M98001369



Report Number (14) SAND--97-2997C
CONF-980514--

Publ. Date (11) 199712
Sponsor Code (18) DOE/CR, XF
UC Category (19) UC-900, DOE/ER

DOE