SERI/STR-211-3188
UC Category: 63
DE87012260

SERI/STR--211-3188

DE87 012260

Gallium Arsenide and Multibandgap Solar Cell Research

Final Subcontract Report
April 1984 - April 1986

S.M. Vernon
S.P. Tobin
R.G. Wolfson
Spire Corporation
Bedford, MA

July 1987

SERI Technical Monitor: C. Leboeuf

Prepared under Subcontract No. XL-4-04024-1

Solar Energy Research Institute
A Division of Midwest Research Institute

1617 Cole Boulevard
Golden, Colorado 80401-3393

Prepared for the
U.S. Department of Energy
Contract No. DE-AC02-83CH10093

Printed in the United States of America
Available from:
National Technical Information Service
U.S. Department of Commerce
5285 Port Royal Road
Springfield, VA 22161

Price: Microfiche A01
Printed Copy A04

Codes are used for pricing all publications. The code is determined by the number of pages in the publication. Information pertaining to the pricing codes can be found in the current issue of the following publications, which are generally available in most libraries: *Energy Research Abstracts, (ERA); Government Reports Announcements* and Index (*GRA* and I); *Scientific and Technical Abstract Reports (STAR);* and publication, NTIS-PR-360 available from NTIS at the above address.

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SECTION 1
INTRODUCTION

1.1 PROGRAM GOAL

The aim of this contract is the achievement of a high efficiency, low-cost solar cell. The basic approach to the problem is centered upon the hetero-epitaxial growth of a III-V compound material onto a single-crystal silicon wafer. The growth technique employed throughout this work is metalorganic chemical vapor deposition (MO-CVD) in an atmospheric pressure reactor which has been described previously.[1] The silicon wafer may serve as a mechanical substrate and ohmic contact for a single-junction device, or may contain a p-n junction of its own and form the bottom cell of a two-junction tandem solar cell structure. The III-V material for the single-junction case is a GaAs and for the two-junction case is either GaAlAs or GaAsP, either material having the proper composition to yield a bandgap of approximately 1.7 eV. The use of a single-crystal film of Ge, deposited onto the silicon wafer by CVD, is also being studied as part of this program. This thin Ge interlayer helps the GaAs film to nucleate and also serves as a region in which to accomplish the transition from the lattice parameter of Si to that of GaAs.

This work is a direct continuation of a previous SERI-funded effort which began in 1980. Under the previous contracts, the following achievements were made:

- Growth of smooth, single-crystal Ge on Si
- Growth of smooth, single-crystal GaAs on Ge on Si
- Fabrication of high-efficiency GaAs cells on GaAs
- Fabrication of preliminary GaAs cells on Ge on Si
- Fabrication of GaAs cells on bulk Ge wafers
- Fabrication of preliminary GaAlAs cells on GaAs
- Demonstration of the growth of single-crystal GaAs and GaAlAs films directly on Si with no Ge interlayer.

The basic tasks in the present two-year program may be outlined as follows:

- Optimization of a GaAs cell technology on Ge-coated Si
- Establishment of a GaAs cell technology directly on Si
- Comparison of the above two approaches and eventual selection of one of them
- Establishment of a GaAlAs baseline cell technology
- Construction of MO-CVD reactor for GaAsP growth
- Development of a GaAsP growth process
- Establishment of a preliminary GaAsP baseline cell technology
- Improvement of growth of GaAlAs on Si
- Establishment of GaAlAs on Si cell technology

In the period covered by this report, the first seven items above have been pursued and some successes will be reported for each of these areas. The last two items have been delayed and will be pursued in the future.

1.2 SCOPE OF THIS REPORT

This final report discusses the accomplishments of a two-year program. The results generated during the first 18 months of this period have been previously reported in detail[1-3] and will be only summarized here. The majority of this document will cover results from the last 6 months of the contract; this period was devoted to optimizing the baseline processing (on GaAs substrates) of GaAs, GaAlAs, and GaAsP cells and to defining the fabrication yields of these three structures. These are necessary steps before attempting the more difficult problem of processing III-V cells on Si substrates. The fabrication of GaAs, GaAlAs, and GaAsP cells on Si will be the subject of future studies.

1.3 SUMMARY OF RESULTS FROM THE FIRST 18 MONTHS OF THIS CONTRACT

The tasks addressed in this time period are:

- Startup of new MOCVD reactor
- Growth of Ge films on Si substrates
- GaAs cells on Ge-coated Si substrates
- GaAs cells on bare Si substrates

- GaAsP cells on GaAs substrates
- Improvement of cell fabrication techniques
- Improvement of GaAlAs solar cells

Each of these areas are summarized below.

1.3.1 Start-Up of New MO-CVD System

During the early part of this two-year contract, a new MO-CVD system was constructed and put on-line in our laboratory. This new system was needed to be able to deposit GaAsP, as the previous reactor had no provision for the use of PH_3. In addition, construction of this new reactor allowed us to incorporate the latest design principles developed after the first system had been completed. These latest improvements included the use of an IBM-PC-based control system, improved leak integrity of all system plumbing, provisions for pumpout of the metalorganic source lines, and an expanded number of dopant lines for greater system flexibility.

This new system was started up and debugged at the end of 1984. The system performance was characterized by uniformity measurements and by Hall-effect measurements on undoped GaAs films. The Hall data is summarized here:

Layer	=	6 microns thick undoped GaAs
n	=	2×10^{14} cm^{-3}
μ_{77}	=	80,000 cm^2/V-sec
μ_{300}	=	7,200 cm^2/V-sec

Uniformity of thickness and doping were also measured over a run of five 2-inch diameter wafers with the following results:

- Thickness uniformity of the entire 5-wafer batch (71 points) = $\pm$ 3.7%.
- Thickness uniformity over each of the five individual wafers = $\pm$ 1.2%, 1.6%, 2.1%, 3.5%, and 5.4%.
- Doping uniformity over one 2 inch wafer (9 points) = $\pm$ 11%.
- Doping uniformity of this wafer together with two points from each of the other four wafers in the run (17 points) = $\pm$ 12%.

The thickness measurements were done by cleave-and-stain techniques and the doping measurements were done on a Polaron Profile Plotter. All layers were approximately 10 microns thick and were doped with SiH_4 to approximately $1x10^{18}$ cm^{-3}.

The chemical-utilization efficiency of our SPI-MO CVD™ 450 reactor operating at atmospheric pressure was calculated from experimental data (growth rate vs. flow of trimethylgallium). The results were a utilization efficiency of 32% for Ga and 3% for As. These values are quite high for an MOCVD process and lead to a source chemical cost (excluding substrate) of \$0.11 per cm^2 of epitaxial GaAs solar cell material.

1.3.2 Growth of Ge on Si

During this contract the quality of the Ge-on-Si films was improved over that of previous experiments. A number of variables in the deposition process were studied and optimized. These include:

Si substrate preparation	Post-etch H_2 bakeout
In-situ HCl etching procedure	AsH_3 doping

After much experimentation a procedure has been defined that reproducibly gives high quality layers of n^+ Ge on Si that are specular, single crystal, and have a defect level of $10^9/cm^2$. Table 1-1 is a summary of this optimized deposition procedure.

TABLE 1-1. GROWTH CONDITIONS FOR AS-DOPED GE FILMS

Substrate -Specs	:	2", 0.01 ohm-cm, 2° off (100), As-doped
Prep	:	NH_4OH - H_2O_2 - H_2O clean, HF dip, DI rinse, N_2 dry
Growth Conditions	:	
HCl etch	-	1200°C, 1 min.
H_2 bake	-	1200°C, 20 min.
Deposition	-	480°C to 520°C for 10 min.
GeH_4 Flow	-	152 Sccm of 10% GeH_4 in H_2
AsH_3 cylinder concentration	-	250 ppm in H_2
AsH_3/GeH_4	=	$7x10^{-5}$ to $7x10^{-4}$

1.3.3 GaAs on Ge-Coated Si

GaAs deposition on Ge/Si wafers is accomplished at fairly standard GaAs growth conditions. These parameters are 630°C, V-III ratio = 10, growth rate = 4 μm/hour. A number of GaAs cell runs were made to compare different growth conditions of the Ge layer; the GaAs cell growth conditions were held constant. Three variables were examined: the growth temperature, Ge layer thickness, and whether or not the layer was doped n^+ during growth. Table 1-2 lists the Ge growth conditions and the cell results.

TABLE 1-2. Ge GROWTH CONDITIONS AND CELL RESULTS FOR GaAs CELLS GROWN ON Ge-COATED Si SUBSTRATES IN LOT 4709.

Ge Growth Temp. (°C)	Ge thick. (μm)	Doped in-situ?	MOCVD Run	Cell ID	Eff. (%)	V_{OC} (V)	J_{SC} (mA/cm^2)	FF (%)
480	.42	Y	2-233	A-D	3.0	.717	10.8	39.4
500	.18	Y	2-233	B-E	2.9	.690	10.1	42.0
520	.26	Y	2-233	C-D	3.3	.641	13.5	38.4
520	.26	Y	2-234	1-A	1.7	.739	9.1	25.7
500	.47	N	2-234	2-C	2.2	.717	8.4	36.4
480	.52	N	2-234	3-E	3.0	.752	11.6	34.1
480	.86	Y	2-235	1-D	5.3	.656	15.1	53.2
520	.75	Y	2-235	2-E	6.9	.743	15.9	58.3
500	.72	Y	2-235	3-E	7.4	.751	16.2	60.5
500	.51	N	2-237	1-H	6.7	.730	15.3	60.2
520	.83	N	2-237	2-G	8.8	.762	17.3	67.1
480	.82	N	2-237	3-A	7.7	.778	16.5	59.9
520	.40	N	2-248	1-A	4.0	.759	12.5	42.2

Of the three Ge growth variables, only the layer thickness appears to have a strong effect on cell efficiency. Figure 1-1 shows this relationship. It is apparent that a thicker layer improves the cell efficiency, presumably by providing a less defective seed for the growth of GaAs active cell layers. The results suggest that even thicker Ge

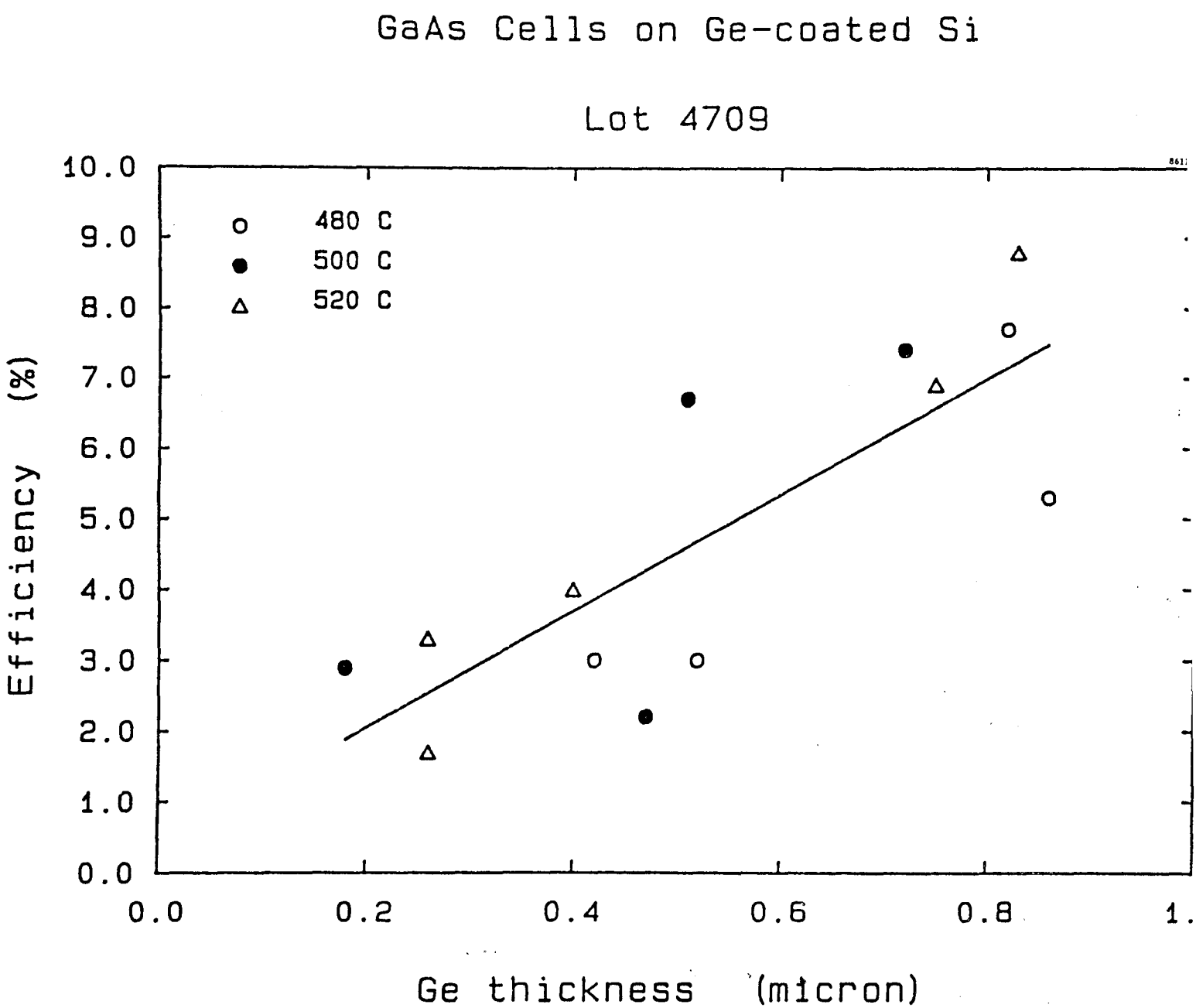

FIGURE 1-1. EFFICIENCY VERSUS Ge THICKNESS FOR GaAs CELLS ON Ge-COATED Si FROM LOT 4709.

layers be explored. The growth temperature, which had a strong effect on the morphology of the Ge layers, had a much smaller effect on the cell results. There is a trend toward lower efficiency for growth at 480°C, but 500 and 520°C are comparable. One can speculate that the reduction of defect density with distance from the Ge-Si interface must be more or less temperature-independent. Whether or not the Ge layer was doped during growth had no apparent effect on the cells. This is explained by diffusion of As from the GaAs overlayers into the Ge, making it n^+ regardless of the initial doping.

Two caveats should be added to the interpretation of Table 1-2 and Figure 1-1. The first is that all of the higher efficiency cells (>5%) came from MOCVD runs 2-235 and 2-237, while all of the lower efficiency cells were from the other three runs. The growth conditions were nominally identical for all runs, but there is some possibility that run-to-run variations and not Ge layer thickness are responsible for the efficiency variation. A second oddity is very low fill factors for the low efficiency cells. The fill factors are limited by a very high series resistance of undetermined origin. In several cases the resistance is high enough to also limit the short circuit current. One possibility is high contact resistance, but this does not explain why only certain MOCVD runs were affected. Another is a high density of thermal expansion cracks, but the problem was also observed for some of the control cells on GaAs substrates. Until these questions are resolved, the exact role of Ge thickness is uncertain.

1.3.4 GaAs Directly on Si

Much progress was made in this time period regarding improvement of the quality of GaAs on Si films and the reproducibility of this technology. Preliminary studies were also performed in which the growth of single-crystal $Ga_{.76}Al_{.24}As$ (1.7 eV bandgap) was demonstrated.

The optimized growth conditions as determined during this contract phase are shown in Table 1-3.

Work was conducted on improving GaAs/Si cell efficiency. As part of this, a laser spot scanner was developed to measure short-circuit current versus localized laser illumination (spot size - 13 micron x 33 micron ellipse) in order to detect the presence of "dead" regions of the cell that were isolated from the grid by microcracks. These

TABLE 1-3. GROWTH CONDITIONS FOR GaAs ON Si.

Substrate:	Si, 2° off (100) → (110)
Substrate prep:	HF dip, DI rinse, N_2 dry
Bakeout:	950°C, 30 minutes, in H_2 only
Nucleation Step:	425°C, V-III = 5, 60 sec
Layer Growth:	650°C, V-III = 10, 4 micron/hour

experiments led to improvement of our grid design and cell fabrication procedure. The best GaAs/Si cell of the previous contract phase was only 2.7% efficient; in this phase that value was raised to 7.0% efficiency (AM1.5, 100mW/cm^2, 28°C). The performance parameters for the best cell are V_{oc}=0.698 V, J_{sc}=14.8 mA/cm^2, and FF=0.67. This cell had poor blue response due to a problem that had caused the entire GaAlAs window layer to become oxidized.

1.3.5 GaAsP on GaAs

Development of techniques for the deposition of high-quality $GaAs_{1-y}P_y$ films (y, ~.25, E_g ~1.7 eV) on GaAs substrates was initiated during this time period. Some of the basic findings concerning the MOCVD growth of GaAsP on GaAs are:

- Thick, graded-composition buffer regions improve surface morphology
- Low growth temperature (~725°) is needed for good surfaces
- Graded buffer regions containing from 6 to 15 steps yield similar surfaces

It was also found that the PH_3 cracking efficiency at temperatures greater than or equal to 700°C in our reactors are quite high, and thus the P/As ratio in the epilayers is the PH_3/AsH_3 ratio in the gas stream.

$GaAs_{.8}P_{.2}$ solar cell structures having lattice matched $Ga_{.1}Al_{.9}As_{.8}P_{.2}$ window layers were characterized by TEM to have dislocation densities of ~$5x10^7$ cm^{-2}. Cells made from such material had "first try" efficiencies as high as 14.7% at a bandgap of 1.64 eV.

1.3.6 Improvement of Cell Fabrication Techniques

A number of efficiency improvements in our baseline solar cell process have been pursued in the past 18 months. These include a redesign of the grid pattern and development of double-layer antireflection (DLAR) coatings. Areas of the process needing better control have also been addressed, including contact resistance of the metallizations and the oxidation resistance of the thin AlGaAs window layer. The following list summarizes the items studied:

- Grid pattern
  - adopted double-busbar design for use on cracked materials
  - improved lithography to get narrower fingers
  - reduced contact pad area

- Antireflection coating
  - improved optical model of the AR coating and window layer
  - refined optical model by ellipsometry studies
  - improved deposition of Ta_2O_5 coatings
  - investigated DLAR coatings of MgF_2 on Ta_2O_5

- Metallization
  - investigated cleaning of GaAs surfaces prior to metal depositions
  - optimized ohmic-contact annealing procedure

- Window Processing
  - studied oxidation of window layers on GaAs/Si cells
  - determined problem to be in cap-etch step
  - improved cap-etch techniques to minimize loss of window layer thickness

At the beginning of this reporting period, GaAs cell fabrication was performed in very small batches by a highly skilled engineer. During this research phase, the fabrication process was transferred to our general device-processing laboratory where large cell batches are handled by technicians. This process transfer went quite smoothly and the capacity to produce 20% efficient GaAs cells with good reproducibility was established. The best GaAs cell of this period was 20.2% efficient (AM1.5, 100mW/cm^2,

28°C) with V_{oc}=1.004 V, J_{sc}=24.5 mA/cm^2, and FF=0.82. This cell was fabricated using the procedures discussed in the previous section.

1.3.7 Improvement of GaAlAs Cells

The previous contract phase had produced a GaAlAs (~1.7 eV) solar cell of only 7.3% efficiency. In addition, there were obvious problems in terms of material quality and reproducibility. During the present phase, a program to improve GaAlAs material quality was initiated; two of the major variables in the MOCVD growth of GaAlAs that were studied are the growth temperature and the use of in-situ methods of purifying the AsH_3 gas. The AsH_3 purifier used was a Ga-In-Al getterer as described previously.[2] It was found that the strongest influence on material quality is from the growth temperature, with the AsH_3 drier having a smaller effect. A typical set of data is shown in Figure 1-2. The best GaAlAs cell fabricated had a bandgap of 1.70 eV and an efficiency of 17.0% (AM1.5, 100mW/cm^2, 28°C).

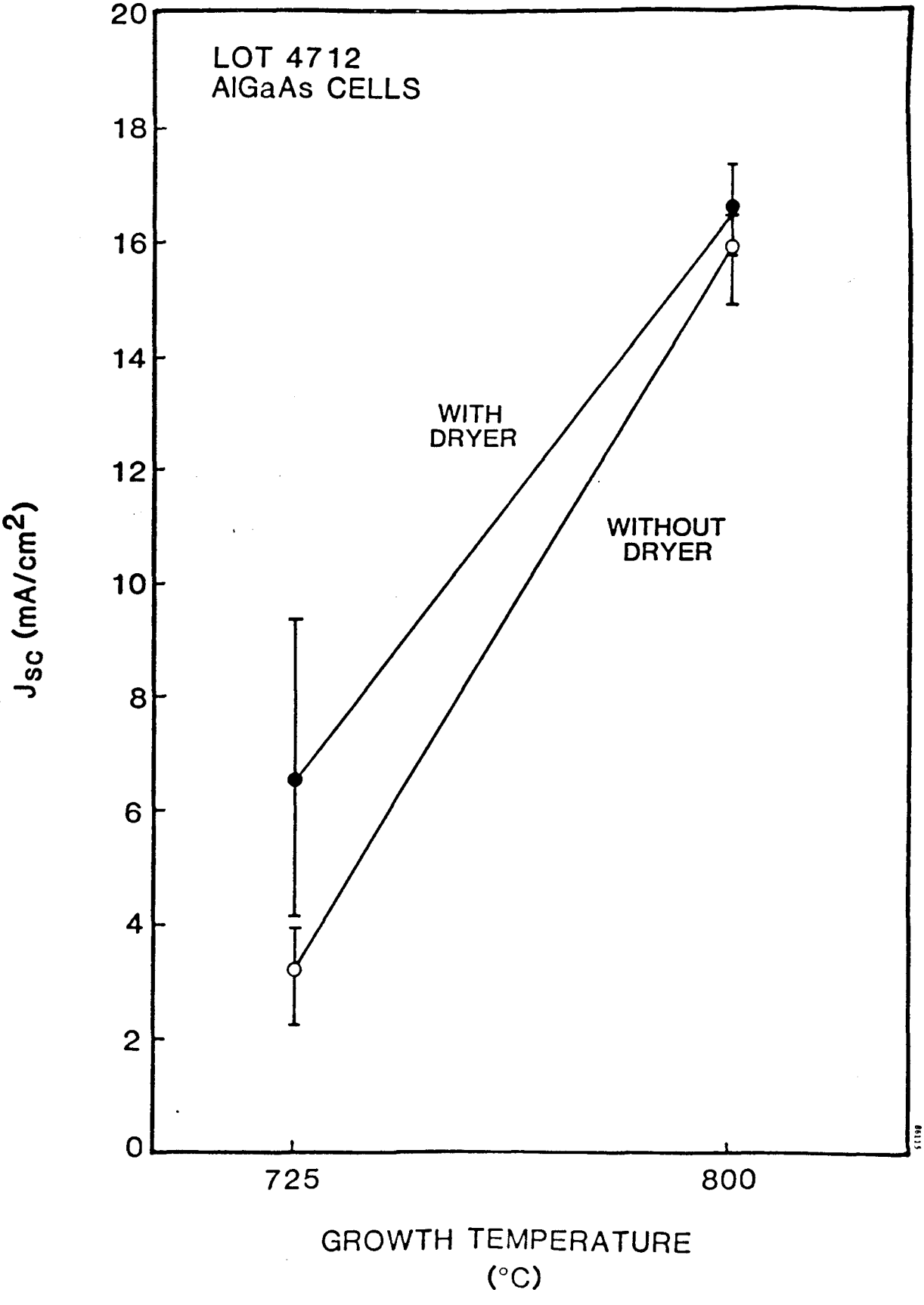

FIGURE 1-2. EFFECT OF GROWTH TEMPERATURE AND ARSINE PURIFIER ON AlGaAs CELL EFFICIENCY.

SECTION 2
CELL DEVELOPMENT AND RESULTS

2.1 GaAsP CELLS

2.1.1 Process

A solar cell fabrication process has been developed for GaAsP p/n heteroface cells grown on GaAs substrates. It is very similar to the process for GaAs and AlGaAs cells, with adjustments made for the different chemistry of GaAsP cap layers and AlGaAsP window layers.

Figure 2-1 shows the cell structure. The active solar cell layers, including the window and cap layer, are all lattice matched. A number of different lattice grading schemes were investigated for the buffer layers; the one shown gave the highest efficiency cells. Processing consisted of the following steps:

1. Evaporate back contact (AuGe)
2. Alloy back contact
3. Photolithography for front grid
4. Evaporate front contact (CrAu)
5. Liftoff
6. Sinter front contact
7. Photolithography for mesa etch
8. Mesa etch
9. Selective etch to remove GaAsP cap layer
10. Evaporate antireflection coating

The I-V curve of the best cell fabricated during our initial batch is shown in Figure 2-2.* The efficiency of 14.7% is felt to be quite good at this stage of development. The efficiency is limited by a low fill factor, which results from high series resistance. This in turn can be traced to a high contact resistance; some contacts were even non-ohmic. We speculate that more work is needed on achieving very high doping levels in the GaAsP cap, so that our standard non-alloyed contacts can be used.

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* For this measurement, the solar simulator was calibrated with a silicon reference cell calibrated by JPL. Subsequent measurements have shown that, due to spectral mismatch, the short circuit current of GaAsP cells is overestimated by about 9% using a silicon reference cell.

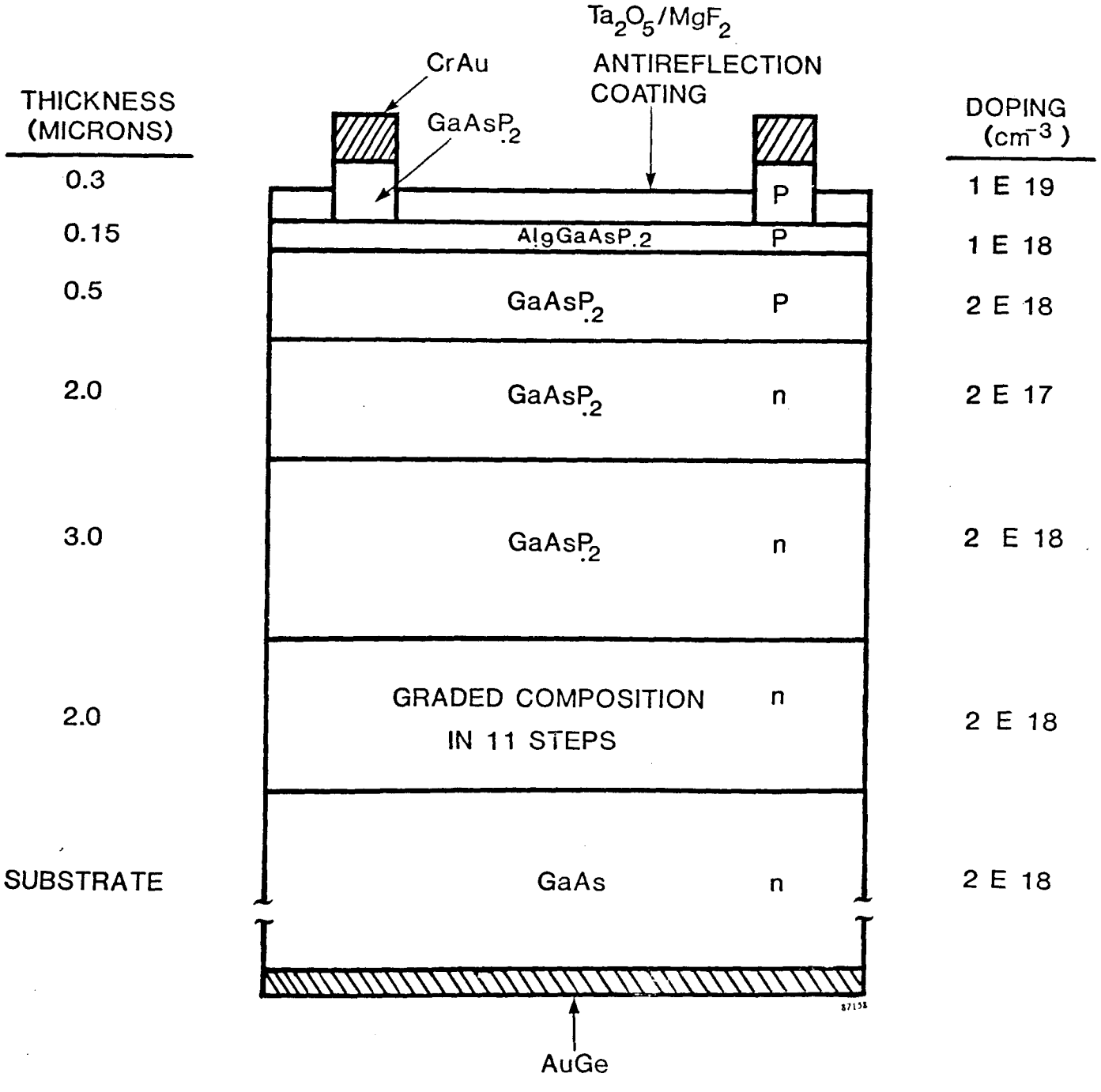

FIGURE 2-1. SOLAR CELL STRUCTURE FOR INITIAL GaAsP DEVELOPMENT.

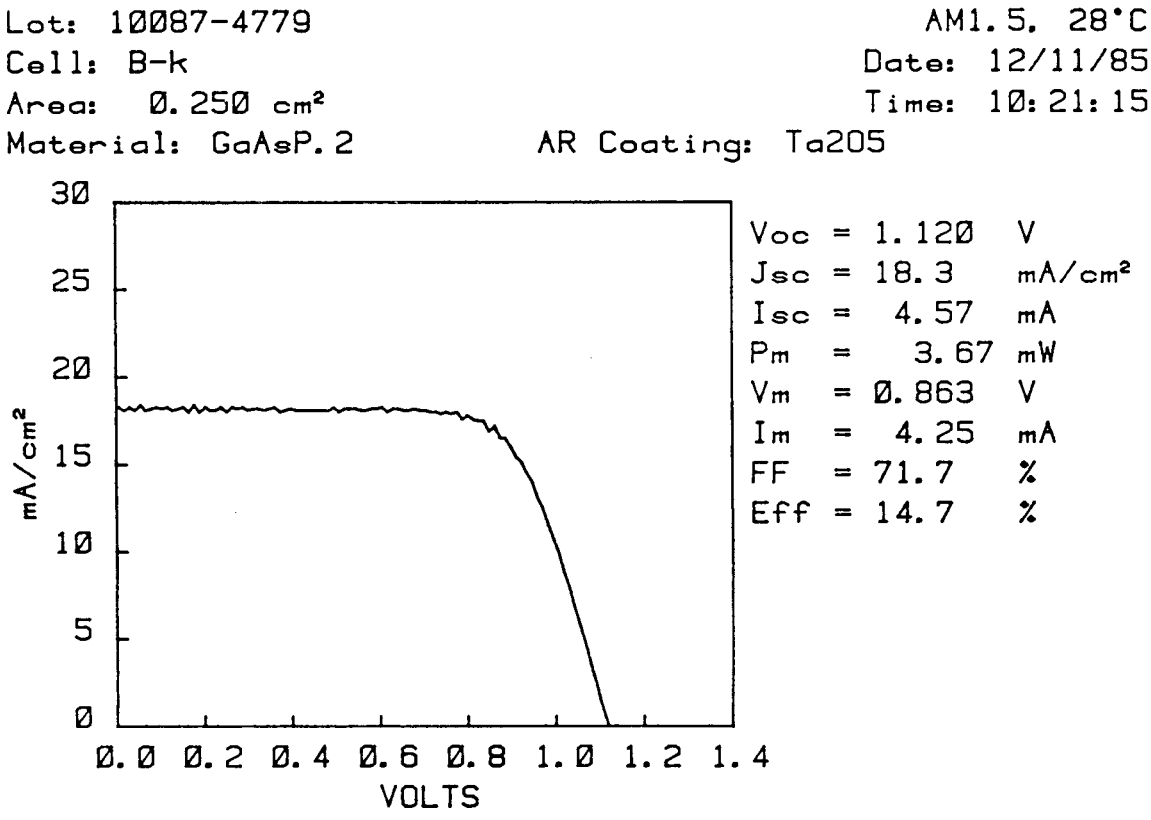

FIGURE 2-2. EFFICIENCY CURVE OF THE BEST GaAsP CELL FROM THE FIRST BATCH.

From the cutoff in the quantum efficiency curve of this cell (Figure 2-3) the energy gap is about 1.64 eV. The peak external quantum efficiency of 75% is indicative of relatively long diffusion lengths in this material, despite the lattice mismatch to the substrate. Log I-V characteristics showed that the cell was limited by space-charge-layer generation-recombination dark current up to several suns. This probably results from the high density of threading dislocations.

2.2 GaAs SUBSTRATE COMPARISON STUDY

2.2.1 Experiment

The object of this experiment was to compare GaAs substrate wafers from several different vendors. Three suppliers (denoted C, M, and S) of wafers grown by the horizontal Bridgman technique and one source (denoted L) of Liquid-Encapsulated Czochralski (LEC) wafers were evaluated. Five GaAs cell growth runs were made, with five substrates in each run. Eight wafers, chosen from three different runs, were then processed as one batch with our standard solar cell process. A total of 238 cells were processed.

2.2.2 Results

Figure 2-4 summarizes the efficiency distributions for each wafer in the experiment. Cells with obvious defects (anomalously low fill factors and/or open circuit voltages) are not included in the figure. These defective cells almost invariably occur close to the wafer edge and are attributed to handling damage. The electrical yield (defined as the percentage of cells which are not defective) can be found in Table 2-3. The error bars in Figure 2-4 denote the total spread in efficiency across each wafer.

2.2.3 Analysis

It can be seen that the spread in efficiency across a wafer is quite small, usually in the range of 1 to 2 percentage points. The larger spread in efficiency from wafer to wafer has two main sources. First is the type of substrate. It was found that all three LEC wafers gave low efficiency cells. These cells suffered from low open-circuit voltages and either low fill factors or short-circuit currents. Subsequent doping profile analysis showed that the substrate doping in the LEC wafers was low and extremely variable; wafer 502-5 had less than 1E16 cm^{-3} carriers. Cells from this wafer had very odd log I-V characteristics, with high series resistance and negative diode ideality factors

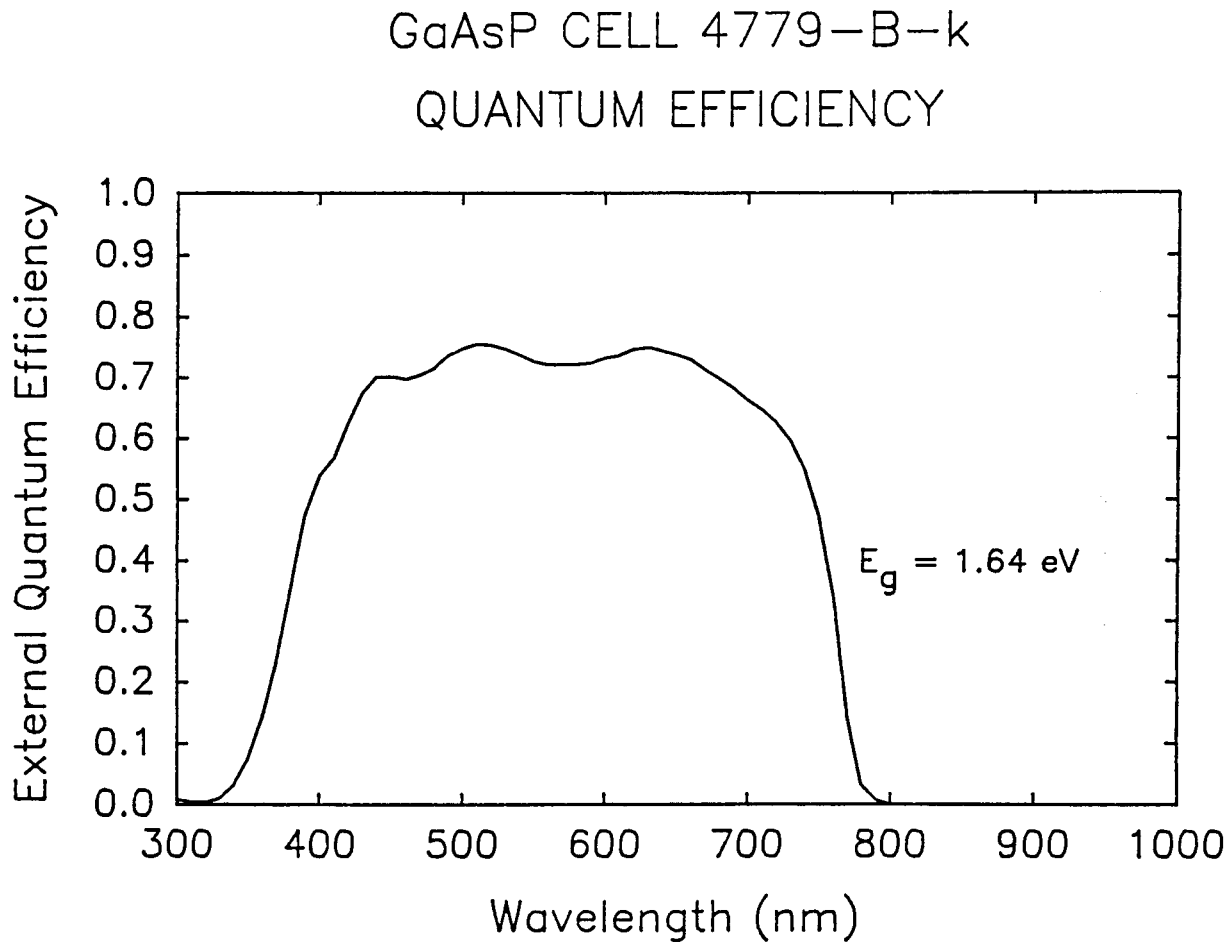

FIGURE 2-3. EXTERNAL QUANTUM EFFICIENCY OF THE BEST GaAsP CELL FROM THE FIRST BATCH.

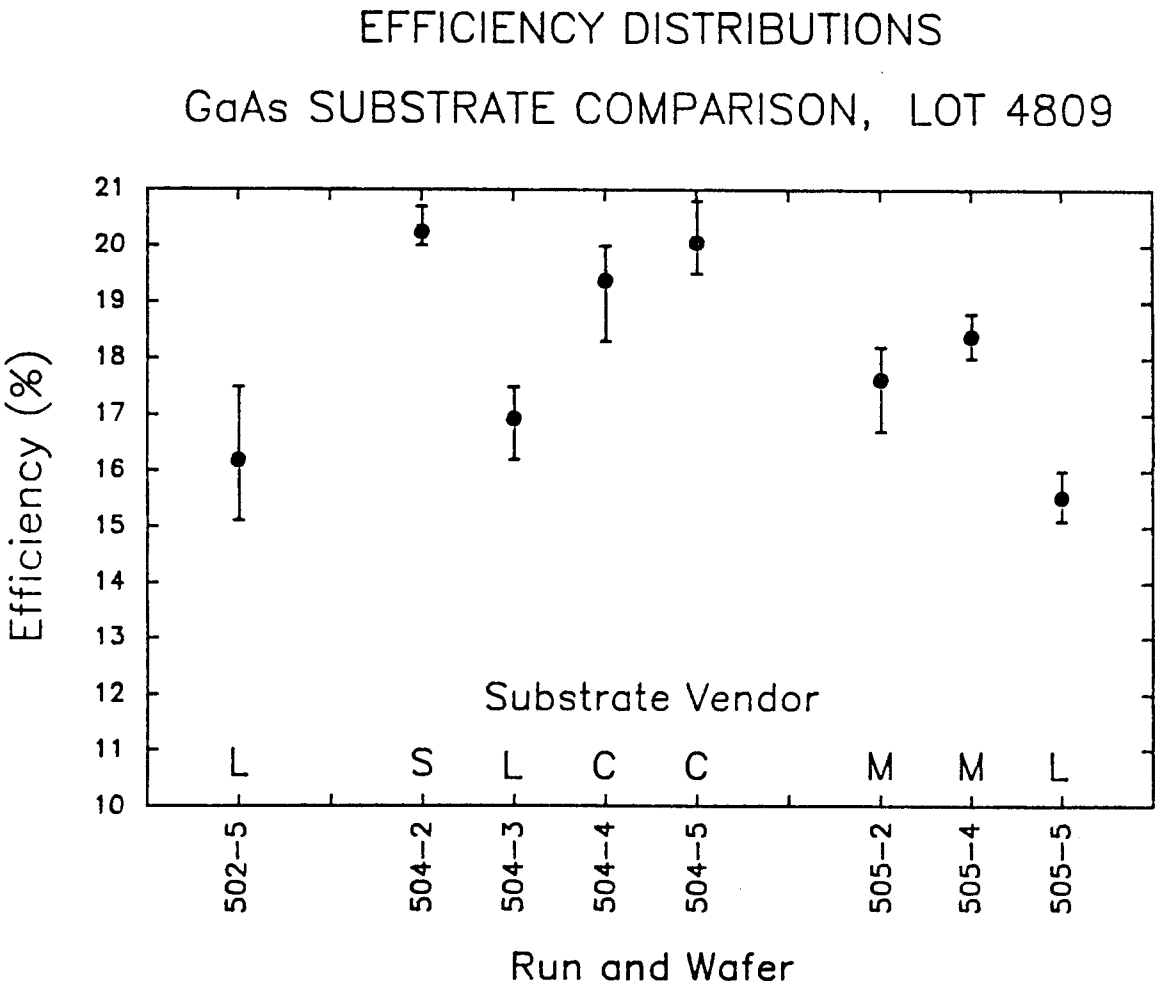

FIGURE 2-4. COMPARISON OF GaAs CELL EFFICIENCY DISTRIBUTIONS FOR EIGHT WAFERS IN THE GaAs SUBSTRATE COMPARISON EXPERIMENT.

for the V_{oc} - J_{sc} curve. Based on these results, LEC wafers (from this batch at least) do not appear to be compatible with high efficiency GaAs solar cells (however, conflicting data was later obtained; see Section 2.3.1 of this report).

The second source of low efficiencies was apparently a bad MOCVD run (Run 505). This run appeared to have no AlGaAs window layer, or at best, a very thin one. After the GaAs cap layer was etched off, no transparent window was visible on the wafer. The blue response of these cells was very low, as expected for an unpassivated front surface. Low J_{sc} was primarily responsible for the lower efficiencies of cells from this growth run.

Ignoring wafers with LEC substrates or from Run 505, we can compare substrates from manufacturers C and S. Wafers 504-2 and 504-5 were quite comparable in efficiency, both in terms of averages and best cells (see Tables 2-1 and 2-2). Results from the next section showed that substrates from manufacturer M also gave comparable efficiencies. We conclude that Bridgman substrates from any of several manufacturers are capable of giving high efficiency cells. Our experience to date with LEC substrates has not been good, but this is just one batch of substrates from one supplier. And, as mentioned earlier, we later obtained good cells on an LEC substrate.

TABLE 2-1. COMPARISON OF THE BEST CELL RESULTS FROM EACH WAFER OF THE GaAs SUBSTRATE COMPARISON EXPERIMENT.

Run	Wafer	Supplier	V_{oc} (V)	J_{sc} (mA/cm^2)	FF (%)	Efficiency (%)
502	5	L	0.886	24.92	79.2	17.5
504	2	S	0.994	24.98	83.5	20.7
504	3	L	0.925	22.68	83.3	17.5
504	4	C	0.991	23.85	84.4	20.0
504	5	C	0.991	25.05	83.9	20.8
505	2	M	0.976	22.35	83.3	18.2
505	4	M	0.987	22.75	83.5	18.8
505	5	L	0.941	20.71	82.0	16.0
Lot Averages:			0.961	23.41	82.9	18.7

TABLE 2-2. COMPARISON OF THE AVERAGE CELL RESULTS FROM EACH WAFER OF THE GaAs SUBSTRATE COMPARISON EXPERIMENT.

Run	Wafer	Supplier	V_{OC} (V)	J_{SC} (mA/cm^2)	FF (%)	Efficiency (%)
502	5	L	0.843	24.90	77.2	16.19
504	2	S	0.994	24.77	82.3	20.25
504	3	L	0.918	22.44	82.2	16.93
504	4	C	0.984	23.66	83.3	19.38
504	5	C	0.984	24.53	83.1	20.06
505	2	M	0.971	21.90	82.9	17.63
505	4	M	0.986	22.40	83.2	18.39
505	5	L	0.932	20.19	82.5	15.53
Lot Averages			0.951	23.10	82.1	18.05

TABLE 2-3. COMPARISON OF YIELD AND STANDARD DEVIATIONS FOR EACH WAFER OF THE GaAs SUBSTRATE COMPARISON EXPERIMENT.

Wafer	Total # of Cells	Electrical Yield	Min. Eff (%)	V_{OC} (% SD)	J_{SC} (% SD)	FF (% SD)	Efficiency (% SD)
502-5	41	0.829	15.1	2.34	0.51	1.55	3.67
504-2	19	1.000	20.0	0.15	1.03	0.90	0.91
504-3	41	0.854	16.2	0.50	0.97	1.25	1.83
504-4	30	0.867	18.3	0.36	0.83	1.39	2.16
504-5	20	0.800	19.5	0.46	1.27	0.78	1.84
505-2	23	0.696	16.7	0.36	1.35	1.24	2.65
505-4	23	0.652	18.0	0.13	1.00	1.06	1.36
505-5	41	0.780	15.1	3.65	1.24	0.93	1.64
Lot Avgs:	30	0.810	17.4	0.99	1.03	1.14	2.01

One comment is in order on the difference in efficiencies between wafers 504-4 and 504-5. These were wafers from the same manufacturer, and from the same MOCVD growth run. Wafer 504-4 was lower in efficiency almost entirely because of lower short-circuit current. Its quantum efficiency was lower across all wavelengths equally, suggesting that some extrinsic mechanism, such as grid shadow, was responsible, and not intrinsic material quality. The difference is thus one of processing.

2.3 REPRODUCIBILITY STUDY

The purpose of this series of experiments was to evaluate the yield and reproducibility of our solar cell growth and processing in a research laboratory environment. Three solar cell materials were evaluated: GaAs, AlGaAs, and GaAsP. The latter two had compositions of about 1.7 eV, suitable as the top cell in a tandem structure. For each material, five solar cell growth runs were made, usually with five wafers in each run. Thus, nominally 25 wafers were grown for each material. Of these wafers, at least one from each run was processed together as a batch. The GaAs and AlGaAs cells were processed together, while a separate process lot was run for the GaAsP cells. Approximately 150 solar cells were processed for each material. The solar cell fabrication process was as described in Section 2.1. Minor variations are noted in the following sections.

2.3.1 GaAs Cells

2.3.1.1 Experiment

In this experiment, not all of the growth runs were identical. We varied the thickness of the AlGaAs window layer to evaluate its influence on efficiency. The first two runs, 502 and 503, had windows of 150 nm thickness, while the rest had 50 nm windows. There was also a problem with one of the growth runs, number 505, as noted in the previous section. This run apparently had no window layer. A sixth growth run, number 523, was therefore undertaken to replace it. We processed a total of eight wafers from the six growth runs; one from each run, plus duplicates to check reproducibility and the effect of different substrates within a run.

2.3.1.2 Results

The cell efficiency distributions are shown in Figure 2-5. Tables 2-4, 2-5, and 2-6 summarize the results in terms of the best cells, averages, and yield and uniformity data.

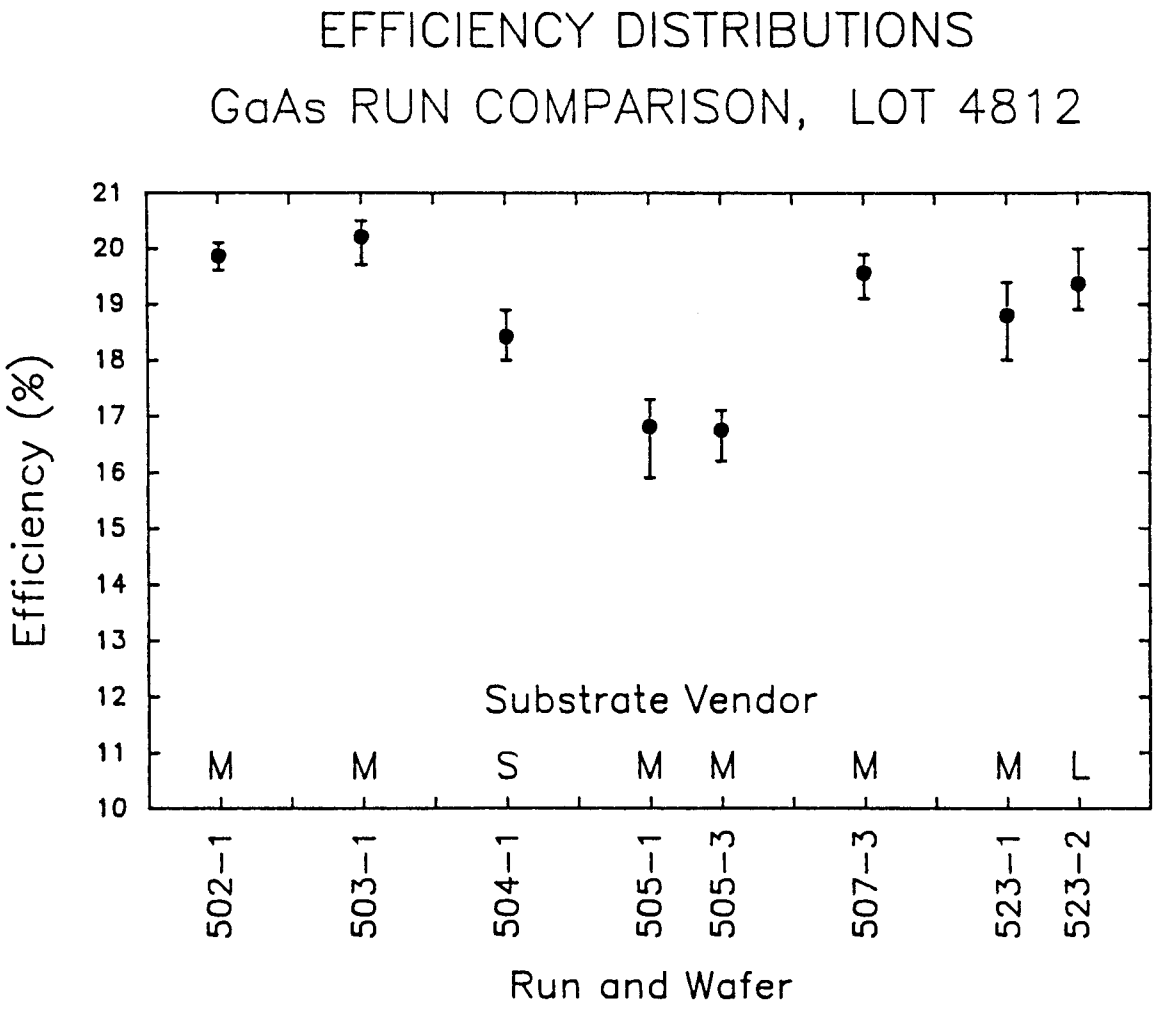

FIGURE 2-5. COMPARISON OF GaAS CELL EFFICIENCY DISTRIBUTIONS FOR EIGHT WAFERS IN THE GaAS REPRODUCIBILITY EXPERIMENT.

TABLE 2-4. COMPARISON OF THE BEST CELL RESULTS FROM EACH WAFER OF THE GaAs REPRODUCIBILITY EXPERIMENT.

Run	Wafer	Cell	V_{OC} (V)	J_{SC} (mA/cm^2)	FF (%)	Efficiency (%)
502	1	1	1.004	25.04	79.8	20.1
503	1	1	1.009	24.86	81.5	20.5
504	1	15	0.979	23.15	83.2	18.9
505	1	8	0.980	21.17	83.3	17.3
505	3	6	0.979	21.05	82.8	17.1
507	3	A	1.001	24.64	80.6	19.9
523	1	1	0.990	23.43	83.5	19.4
523	2	28	0.997	23.74	84.4	20.0
Lot Averages:			0.992	25.39	82.4	19.2

TABLE 2-5. COMPARISON OF THE AVERAGE CELL RESULTS FROM EACH WAFER OF THE GaAs REPRODUCIBILITY EXPERIMENT.

Run	Wafer	V_{OC} (V)	J_{SC} (mA/cm^2)	FF (%)	Efficiency (%)
502	1	1.004	24.90	79.4	19.86
503	1	1.006	24.55	81.9	20.21
504	1	0.979	22.71	82.8	18.42
505	1	0.975	20.81	82.9	16.81
505	3	0.978	20.82	82.2	16.75
507	3	0.996	24.29	80.9	19.57
523	1	0.983	22.99	83.2	18.80
523	2	0.988	22.51	83.4	19.37
Lot Averages:		0.989	22.95	82.1	18.72

TABLE 2-6. COMPARISON OF YIELD AND STANDARD DEVIATIONS FOR EACH WAFER OF THE GaAs REPRODUCIBILITY EXPERIMENT.

Wafer	Total # of Cells	Electrical Yield	Min. Eff (%)	V_{OC} (% SD)	J_{SC} (% SD)	FF (% SD)	Efficiency (% SD)
502-1	7	0.714	19.6	0.26	0.57	1.16	0.82
503-1	30	0.933	19.7	0.18	0.54	0.89	0.98
504-1	28	0.893	18.0	0.20	0.89	0.80	1.26
505-1	34	0.882	15.9	0.41	1.35	0.78	1.98
505-3	13	0.923	16.2	0.27	1.23	1.12	1.49
507-3	20	0.750	19.1	0.28	0.96	0.62	1.36
523-1	30	0.933	18.0	0.37	1.24	1.03	1.62
523-2	30	0.767	18.9	0.46	1.22	0.92	1.68
Lot Averages:		0.849	18.2	0.30	1.00	0.92	1.40

With the exception of run 505, almost all the cells have efficiencies between 18 and 21 percent. Ranges of efficiency within a given wafer are tighter, usually one percentage point or less. This indicates good uniformity of the growth and processing. The two wafers from run 505 had nearly identical efficiency, suggesting that the growth and processing are uniform from wafer to wafer.

One interesting result is that the LEC wafer from run 523 did not suffer from the problems found earlier for other LEC substrates, although it was from the same batch of wafers. The carrier concentrations were found to vary greatly between wafers, and this may explain some of the efficiency variations.

2.3.1.3 Analysis

It appears from Figure 2-5 that the runs with thicker AlGaAs windows (502 and 503) had slightly higher efficiencies on average than those with 50 nm windows. This is the opposite of theoretical predictions, because thinner windows should give higher J_{SC} due to reduced absorption losses. Tables 2-4 and 2-5 show that the efficiency difference is caused by both V_{OC} and J_{SC} differences. More detailed V_{OC} analysis in Table 2-7 shows that higher diffusion saturation currents (Jo1) in the cells with thinner windows were responsible for the lower V_{OC}. In this table, we show the results of deconvolving the log J-V curve into n=1 (diffusion) and n=2 (space charge layer generation-recombination)

currents. Also shown is the relative contribution of each current mechanism at open-circuit conditions. One notable exception to the trend was run 507, which had both a 50 nm window and low Jo1. Also note that for most cells V_{oc} does not correlate well with the generation-recombination saturation current, Jo2. Except for runs 502 and 507, the cells are mostly diffusion-current-limited at open circuit.

Turning now to J_{sc}, external quantum efficiency curves are compared in Figure 2-6 for the best cells of each window thickness. The cells with thin windows had better blue response (as expected), but lower peak QE. The reason for different quantum efficiency shapes is optical interference between the window and Ta_2O_5 AR coating layers. Optical modeling of the reflectance of these structures nicely reproduced the features of the measured curves above 450 nm, where window absorption is not important. Below 450 nm, more light is lost to AlGaAs absorption in the thicker window cell.

One explanation for the V_{oc} and J_{sc} difference in average cells is higher heteroface recombination velocities in the thin window cells. We suspect that this may reflect process-induced damage, either during the cap etching or antireflection coating steps. The high V_{oc} and J_{sc} for run 507 argue against any inherent material problem with thin AlGaAs windows.

TABLE 2-7. ANALYSIS OF V_{oc}-LIMITING MECHANISMS IN GaAs CELLS FROM LOT 4812. Temperature = 25°C.

Wafer No.	Nominal AlGaAs Thickness (nm)	V_{oc} (V)	Diffusion Current Jo1 (A/cm^2)	% at V_{oc}	g-r Current Jo2 (A/cm^2)	% at V_{oc}
502-1	150	1.004	1.08E-19	39	5.16E-11	61
503-1	150	1.006	1.60E-19	63	2.98E-11	37
504-1	50	0.978	5.70E-19	78	2.99E-11	22
505-1	50	0.980	4.73E-19	75	2.97E-11	25
505-3	50	0.979	4.16E-19	38	3.91E-11	62
507-3	50	1.001	1.18E-19	67	5.48E-11	33
523-1	50	0.990	3.44E-19	78	2.26E-11	22
523-2	50	0.997	2.78E-19	78	2.15E-11	22

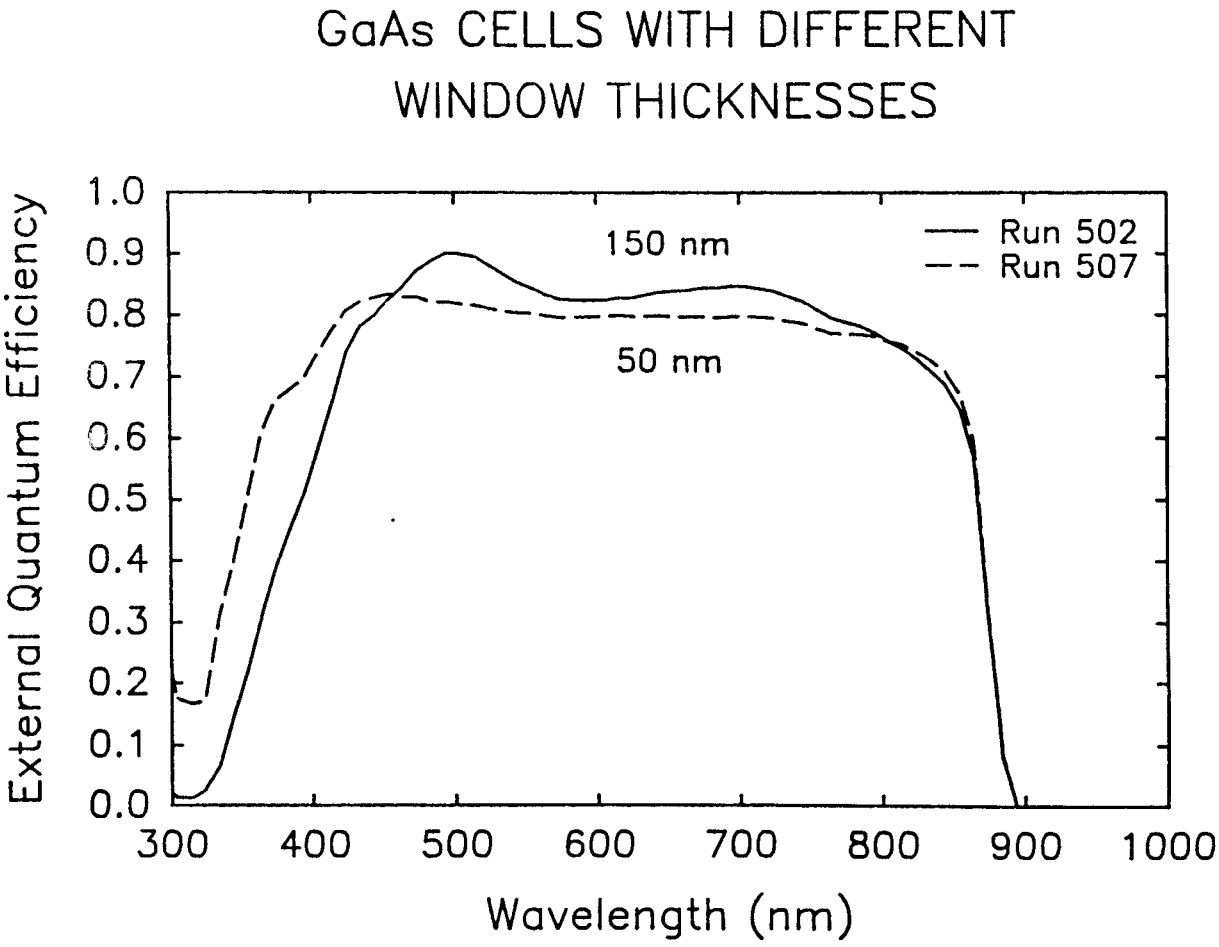

FIGURE 2-6. COMPARISON OF EXTERNAL QUANTUM EFFICIENCY CURVES FOR GaAs CELLS WITH 50 NM AND 150 NM AlGaAs WINDOWS.

2.3.2 AlGaAs Cells

2.3.2.1 Experiment

In this experiment, five consecutive AlGaAs cell growth runs were made with nominally identical conditions. The $Al_xGa_{1-x}As$ composition was x=0.20, for a bandgap of 1.65 eV. The cell structure, shown in Figure 2-7, is very similar to GaAs cells. The major difference is a thinner emitter to compensate for lower diffusion lengths in AlGaAs. One wafer from each run was processed together as a lot, with the GaAs cells already described. All GaAs substrates were Bridgman wafers from the same supplier. A total of 146 AlGaAs cells were processed from the five wafers.

2.3.2.2 Results

Figure 2-8 shows the efficiency distribution of the five runs. It should be noted at the outset that these efficiencies are inflated by about 10%. We used a silicon reference cell to set the intensity of the solar simulator; spectral mismatch causes an error in J_{sc} and efficiency. The maximum efficiencies were thus in the 17 to 18 percent range.

Table 2-8 lists the results for the best cell from each wafer, and Table 2-9 lists wafer averages. These numbers have not been corrected for spectral mismatch. Table 2-10 compares the yield and standard deviations for each wafer.

2.3.2.3 Analysis

Taking the process lot as a whole, the uncorrected efficiencies range from 15 to 20%. Even after spectral mismatch correction, these efficiencies are good for AlGaAs, and indicate high-quality material. However, the range is larger than for GaAs cells. The spread in efficiency across a given wafer is in the two to three percentage point range, also higher than for GaAs. An analysis of the standard deviations of cell performance parameters in Table 2-10 shows that J_{sc} and fill factor are responsible for most of the variation. (Comparable numbers for GaAs, from Table 2-6, are noticeably lower.) Reasons for these variations are discussed later.

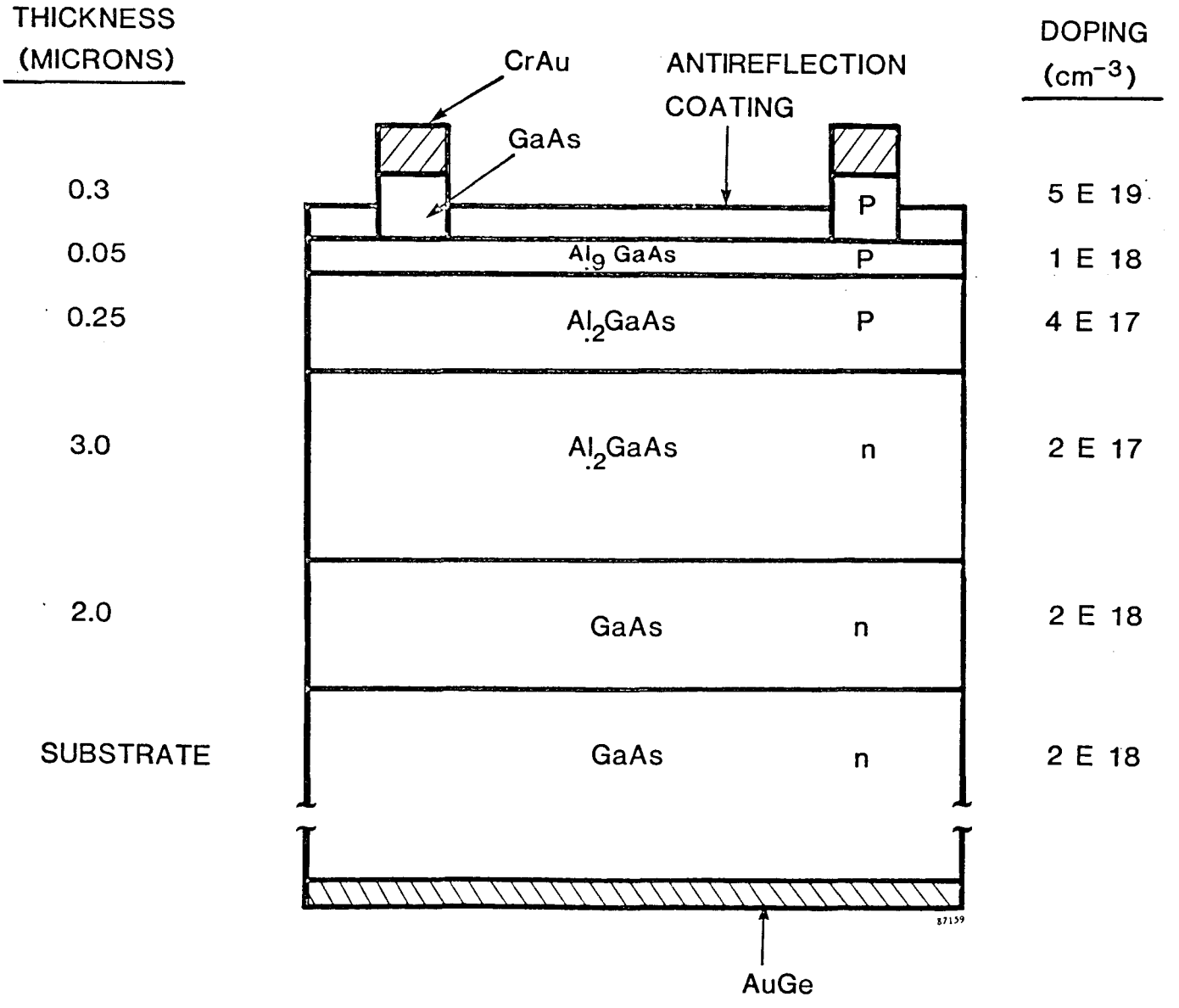

FIGURE 2-7. LAYER STRUCTURE OF AlGaAs SOLAR CELLS GROWN BY MOCVD.

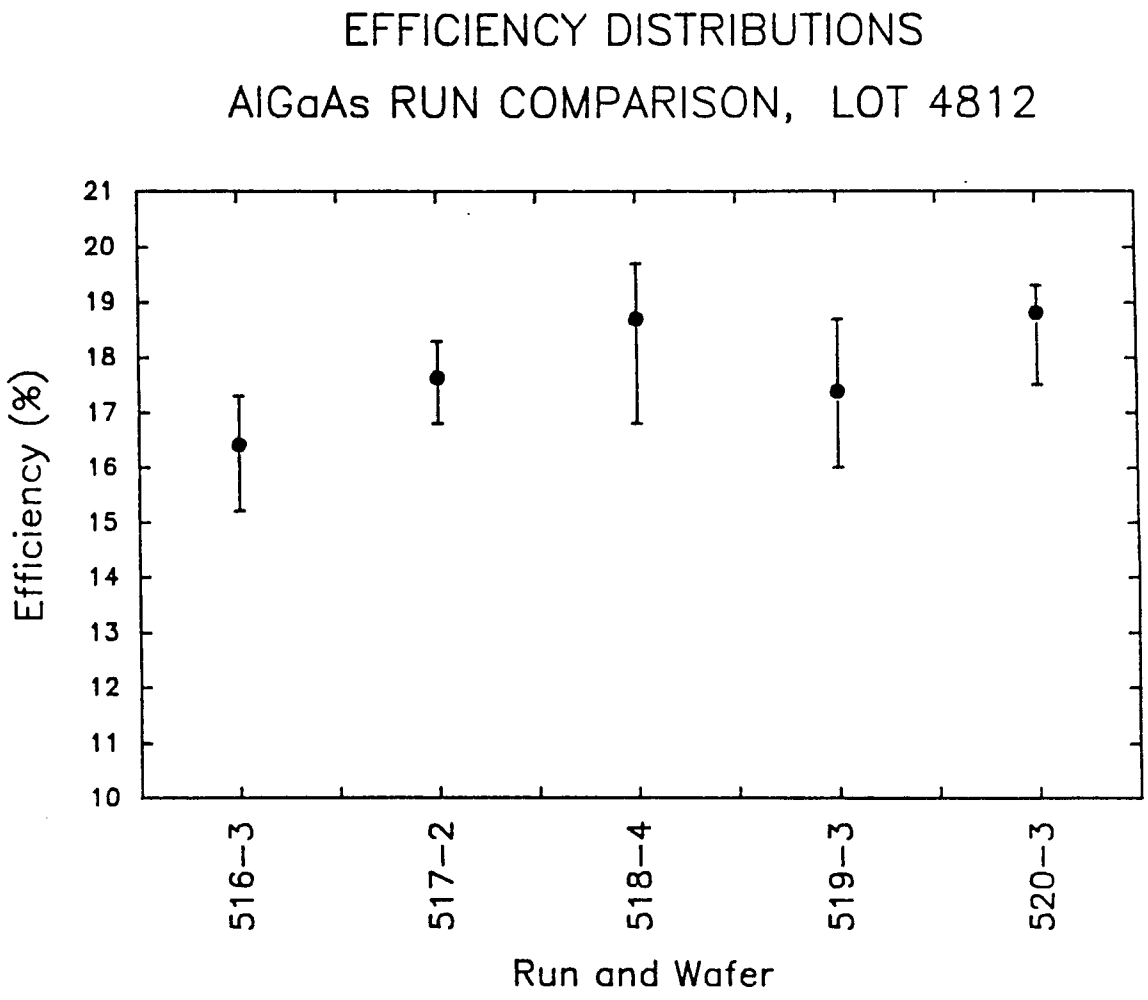

FIGURE 2-8. COMPARISON OF AlGaAs CELL EFFICIENCY DISTRIBUTION FOR FIVE MOCVD RUNS IN THE AlGaAs REPRODUCIBILITY EXPERIMENT.

TABLE 2-8. COMPARISON OF THE BEST CELL RESULTS FROM EACH WAFER OF THE AlGaAs REPRODUCIBILITY EXPERIMENT.

Run	Wafer	Cell	Eg (eV)	V_{OC} (V)	J_{SC} (mA/cm^2)	FF (%)	Efficiency (%)
516	3	K	1.645	1.185	19.10	76.2	17.3
517	2	3	1.666	1.221	18.80	79.8	18.3
518	4	16	1.652	1.211	20.05	81.2	19.7
519	3	32	1.649	1.186	19.14	82.3	18.7
520	3	40	1.652	1.187	19.90	81.6	19.3
Lot Averages:			1.653	1.198	19.40	80.2	18.7

TABLE 2-9. COMPARISON OF THE AVERAGE CELL RESULTS FROM EACH WAFER OF THE AlGaAs REPRODUCIBILITY EXPERIMENT.

Run	Wafer	V_{OC} (V)	J_{SC} (mA/cm^2)	FF (%)	Efficiency (%)
516	3	1.180	18.18	76.5	16.41
517	2	1.215	18.87	76.9	17.63
518	4	1.208	19.37	79.9	18.70
519	3	1.177	18.91	78.1	17.38
520	3	1.192	19.46	81.1	18.81
Lot Averages:		1.194	18.96	78.5	17.79

TABLE 2-10. COMPARISON OF YIELD AND STANDARD DEVIATIONS FOR EACH WAFER OF THE AlGaAs REPRODUCIBILITY EXPERIMENT.

Wafer	Total # of Cells	Electrical Yield	Min. Eff (%)	V_{OC} (% SD)	J_{SC} (% SD)	FF (% SD)	Efficiency (% SD)
516-3	24	0.833	15.2	1.10	3.10	1.02	3.74
517-2	16	0.875	16.8	0.49	0.95	2.54	2.79
518-4	30	0.767	16.8	0.90	2.43	3.05	4.49
519-3	32	0.719	16.0	1.01	1.80	3.64	3.76
520-3	44	0.886	17.5	0.63	2.76	1.72	2.29
Lot Averages:		0.816	16.5	0.83	2.21	2.40	3.41

The electrical yield of good cells was about 82%, comparable to GaAs. Again, the majority of bad cells were located around the periphery of the wafers, and were characterized by anomalously low V_{OC} and/or fill factor. We attribute these bad cells to handling damage, probably from tweezers. In a production environment, this loss could probably be avoided.

From Table 2-8, the AlGaAs bandgap was quite reproducible from run to run. It was somewhat higher for run 517, where a problem was noted with the aluminum flow controller. Figure 2-9 shows the energy bandgap measured at 30 points across a wafer by photoluminescence. The uniformity is good, with an average of 1.661 eV and a standard deviation of 0.006 eV.

The reason for variations in efficiency from run to run was investigated. We found a good correlation between efficiency and cleaning of the reactor and wafers, as seen in Table 2-11. When the glass bell jar and susceptor were etched before the run, the efficiencies were somewhat higher. There may also be an effect from etching the wafers prior to growth, although this seems less likely. No similar correlation could be found for the GaAs cells. More work will be necessary to verify this effect, but it seems plausible, based on the sensitivity of AlGaAs quality to impurities. Another possible trend is the steady increase in efficiency for the first three runs. It is well known that making several growth runs is a good way to clean out the system.

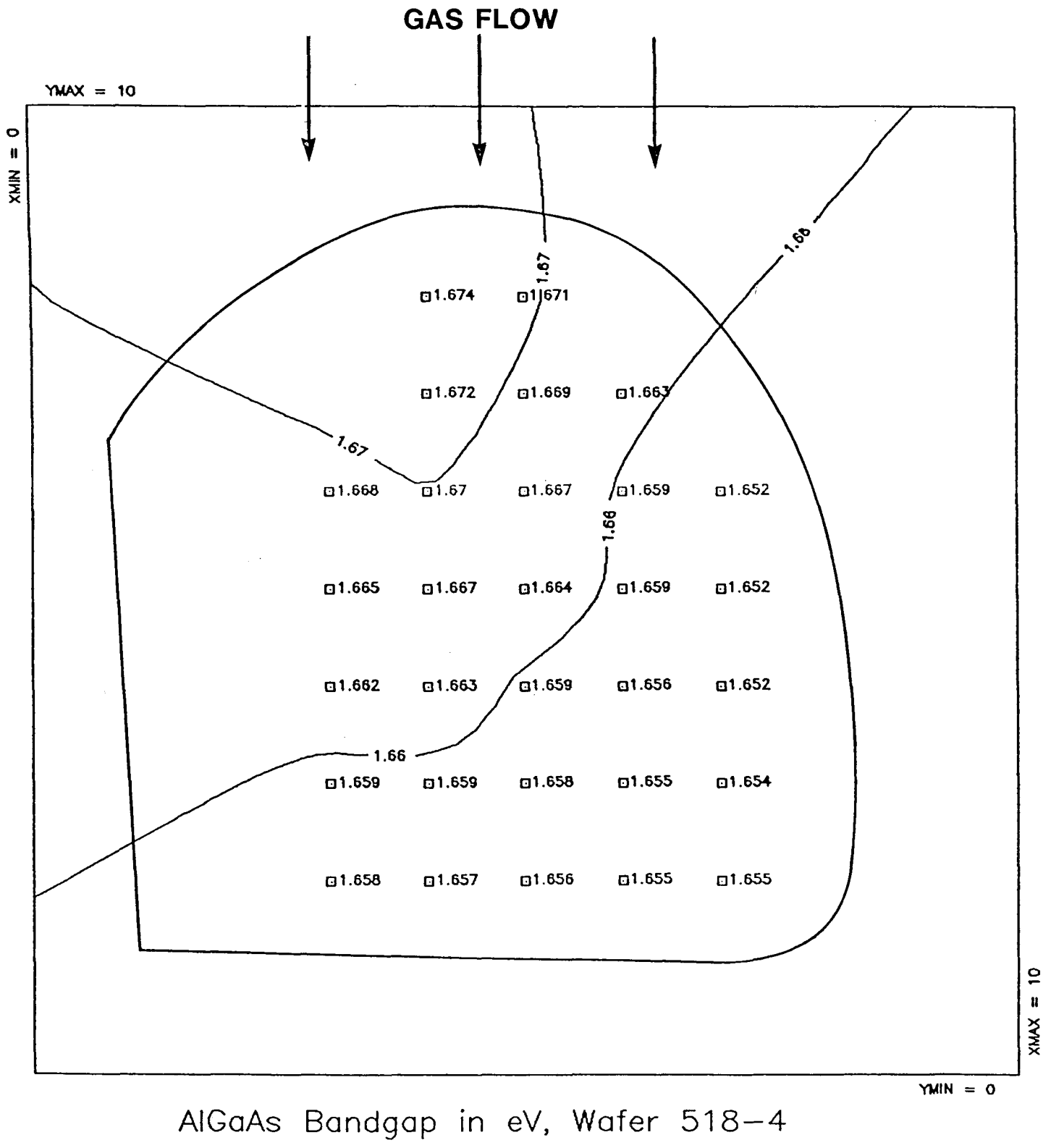

FIGURE 2-9. UNIFORMITY MAP OF AlGaAs BANDGAP ACROSS A SOLAR CELL WAFER.

TABLE 2-11. AlGaAs CELL EFFICIENCY VS. REACTOR AND WAFER CLEANING HISTORY.

Run No.	Best Eff.	Ave. Eff.	Clean Glassware	Etched Susceptor	Wafer Etched
518	19.7	18.7	Yes	Yes	No
520	19.5	18.8	Yes	Yes	No
517	18.3	17.6	No	No	Yes
519	18.7	17.4	No	No	Yes
516	17.3	16.4	No	No	Yes

An analysis of dark current mechanisms was made, with results in Table 2-12. As in GaAs cells, both diffusion and space-charge recombination currents limit V_{oc}. For the best AlGaAs cells, diffusion currents are reduced and space-charge recombination is more important.

TABLE 2-12. ANALYSIS OF V_{oc}-LIMITING MECHANISMS IN AlGaAs CELLS FROM LOT 4812. Temperature = 25°C.

			Diffusion Current		g-r Current	
Wafer No.	AlGaAs Bandgap (eV)	V_{oc} (V)	Jo1 (A/cm^2)	% at V_{oc}	Jo2 (A/cm^2)	% at V_{oc}
516-3	1.645	1.185	1.17E-22	59	8.26E-13	41
517-2	1.666	1.221	2.38E-23	47	5.51E-13	53
518-4	1.652	1.211	3.02E-23	42	7.26E-13	58
519-3	1.649	1.186	1.35E-22	73	5.37E-13	27
520-3	1.652	1.187	1.38E-22	72	5.85E-13	28

In Figure 2-10, we compare the external quantum efficiencies for the five wafers. Overall, the uniformity is good. The blue responses are very similar, with most differences occurring in the red. The higher bandgap of run 517 is noticeable, but otherwise the reproducibility of the AlGaAs composition is excellent. The downward slope of the curves above 500 nm indicates that the base diffusion length is less than the absorption length for red photons. The shallow junction is also partly responsible, although our experience indicates that the lost red response is compensated by increased blue response.

The fill factors of AlGaAs cells are generally lower than GaAs, despite the higher V_{oc}. Increased series resistance is the major reason, from higher emitter sheet resistance (about 5000 ohms per square for AlGaAs, vs. 500 for GaAs). The emitter thickness, mobility, and doping are all lower than for GaAs.

2.3.3 GaAsP Cells

2.3.3.1 Experiment

In this experiment, cells were compared from five consecutive GaAsP solar cell growth runs. All runs were nominally the same, with a GaAsP composition of x=.23, corresponding to a 1.7 eV bandgap. A batch of cells, consisting of one wafer from each run, was processed together. A total of 159 cells were produced from the five wafers. The cell structure is shown in Figure 2-11. Because the cells were grown on a lattice-mismatched substrate (GaAs) with about 1% mismatch, it was necessary to grade the lattice constant from that of GaAs to that of GaAsP. Another difference from the previous cells is that a quaternary window layer (AlGaAsP) was required to provide a high-bandgap, lattice-matched heteroface at the front of the cell. Solar cell processing was similar to that of GaAs and AlGaAs cells.

2.3.3.2 Results

Figure 2-12 shows the efficiency distributions. For these efficiency measurements we used a silicon reference cell with a KG-5 filter to simulate the cutoff of a 1.7 eV cell. The filtered reference cell was calibrated by SERI, and it is felt that no corrections to the measured data are needed. The complete data are summarized in Tables 2-13, 2-14, and 2-15.

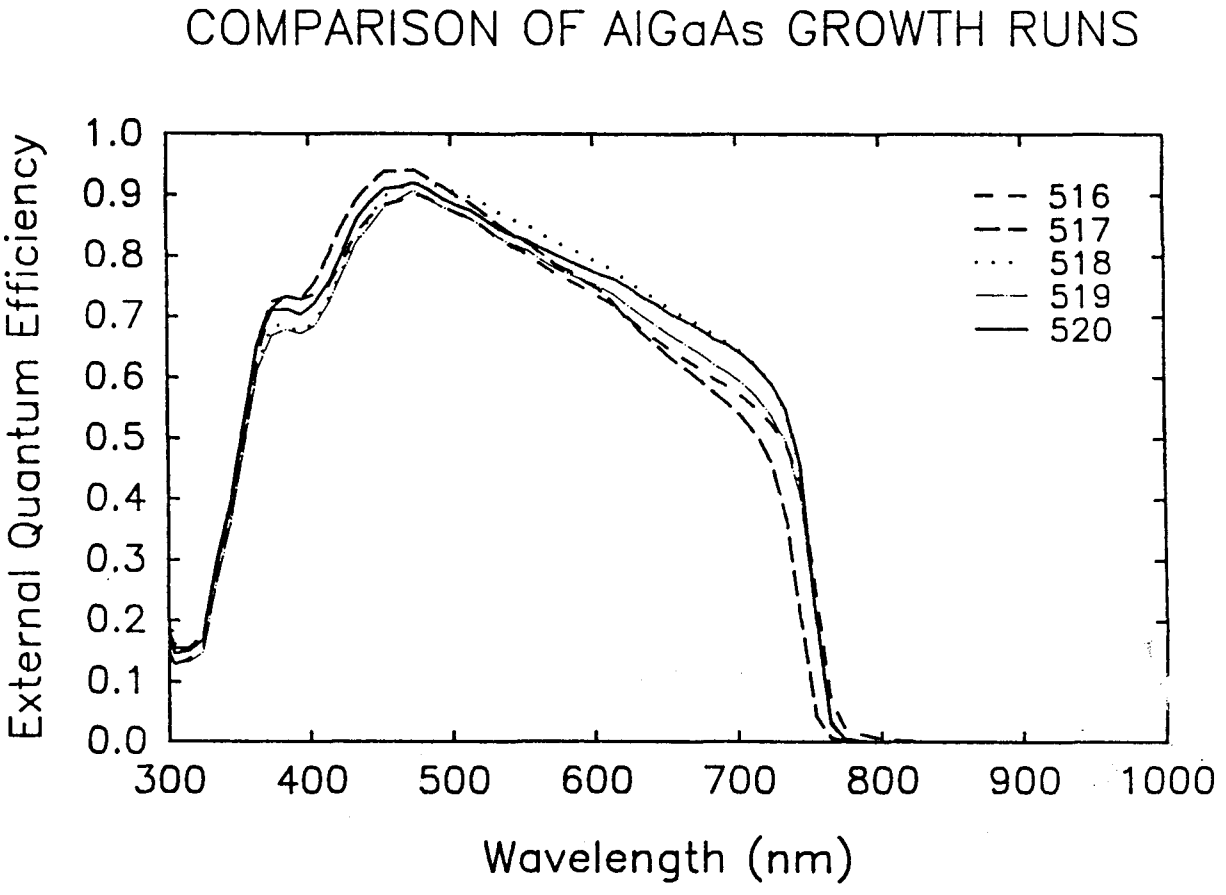

FIGURE 2-10. COMPARISON OF EXTERNAL QUANTUM EFFICIENCY CURVES FOR AlGaAs CELLS FROM DIFFERENT GROWTH RUNS.

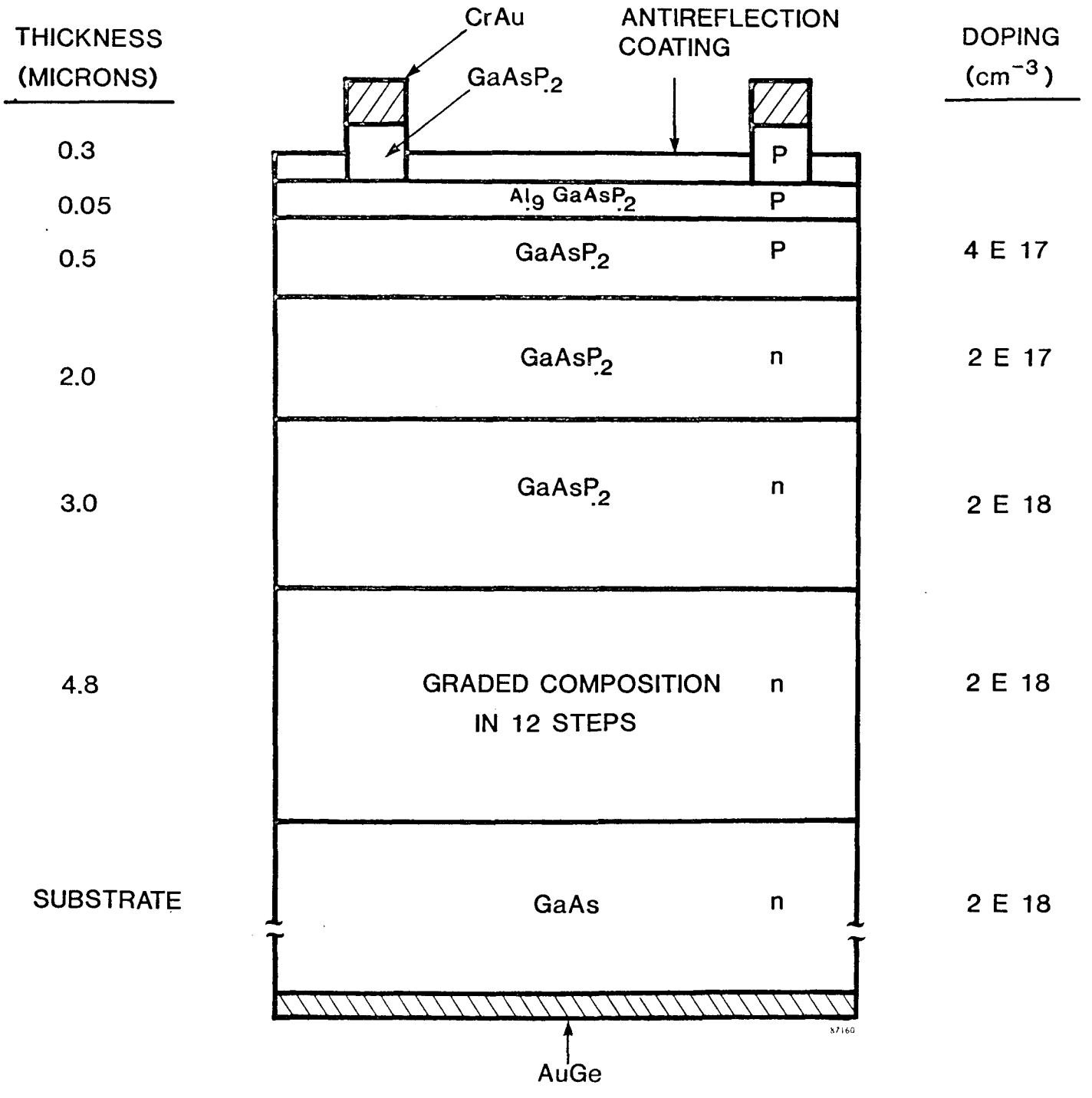

FIGURE 2-11. LAYER STRUCTURE OF GaAsP SOLAR CELLS GROWN BY MOCVD.

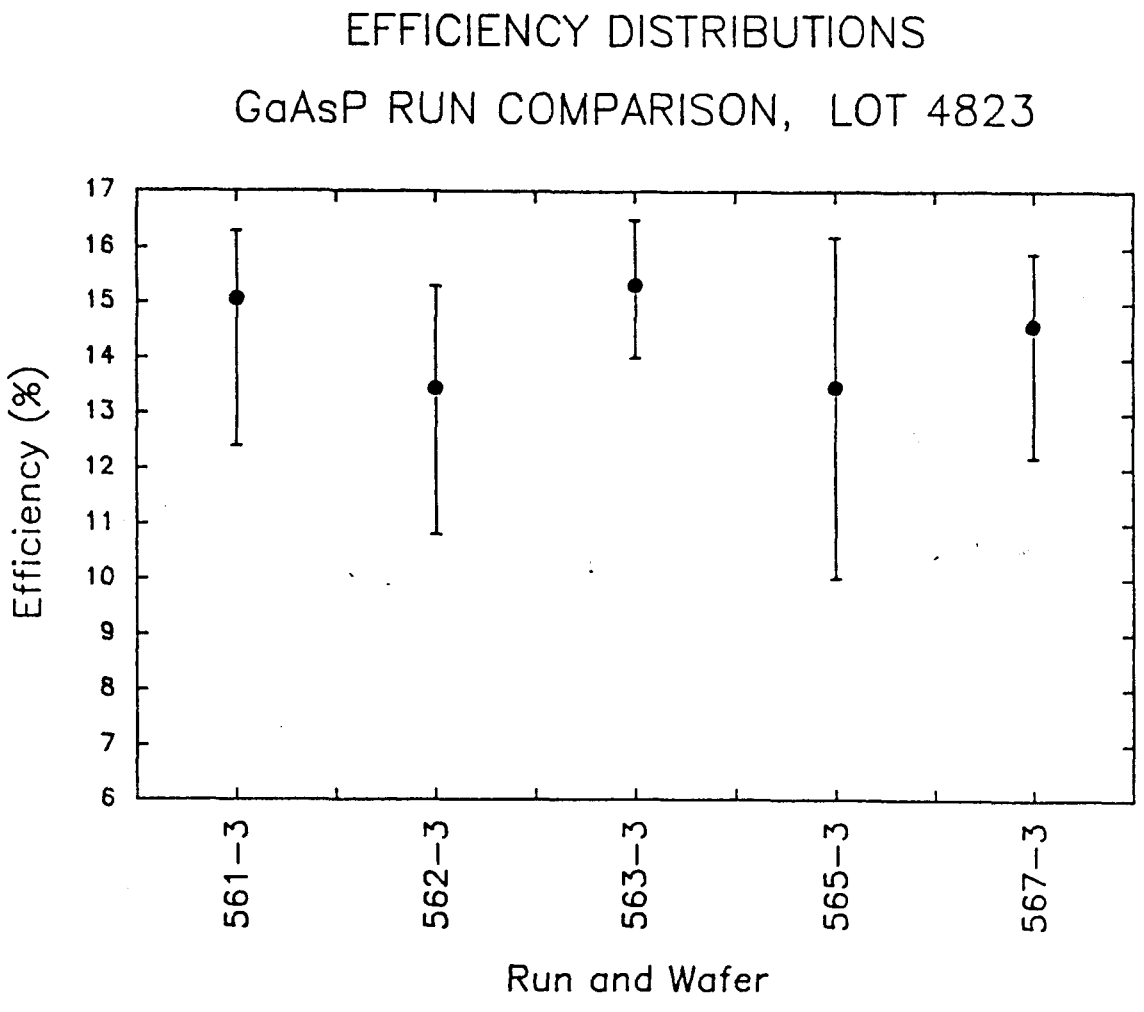

FIGURE 2-12. COMPARISON OF GaAsP CELL EFFICIENCY DISTRIBUTIONS FOR FIVE MOCVD RUNS IN THE GaAsP REPRODUCIBILITY EXPERIMENT.

TABLE 2-13. COMPARISON OF THE BEST CELL RESULTS FROM EACH WAFER OF THE GaAsP REPRODUCIBILITY EXPERIMENT.

Run	Wafer	Cell	Eg (eV)	V_{OC} (V)	J_{SC} (mA/cm^2)	FF (%)	Efficiency (%)
561	3	16	1.720	1.259	15.79	82.0	16.3
562	3	34	1.692	1.209	15.38	82.0	15.3
563	3	11	1.702	1.212	16.77	81.0	16.5
565	3	24	1.688	1.214	16.51	80.4	16.2
567	3	17	1.712	1.157	16.54	82.8	15.9
Lot Averages:				1.210	16.20	81.7	16.0

TABLE 2-14. COMPARISON OF THE AVERAGE CELL RESULTS FROM EACH WAFER OF THE GaAsP REPRODUCIBILITY EXPERIMENT.

Run	Wafer	V_{OC} (V)	J_{SC} (mA/cm^2)	FF (%)	Efficiency (%)
561	3	1.218	15.15	81.6	15.06
562	3	1.188	13.95	81.0	13.45
563	3	1.215	15.79	79.9	15.32
565	3	1.172	14.18	80.8	13.47
567	3	1.148	15.59	81.5	14.59
Lot Averages:		1.188	14.93	80.9	14.38

TABLE 2-15. COMPARISON OF YIELD AND STANDARD DEVIATIONS FOR EACH WAFER OF THE GaAsP REPRODUCIBILITY EXPERIMENT.

Wafer	Total # of Cells	Electrical Yield	Min. Eff (%)	V_{OC} (% SD)	J_{SC} (% SD)	FF (% SD)	Efficiency (% SD)
561-3	34	0.882	12.4	2.30	5.14	0.76	7.42
562-3	38	0.763	10.8	2.09	6.94	1.31	8.99
563-3	15	0.867	14.0	1.20	3.94	1.35	5.07
565-3	30	0.633	10.0	1.79	12.17	1.66	14.06
567-3	42	0.881	12.2	1.83	5.20	0.91	6.11
Lot Averages:		0.805	11.9	1.84	6.68	1.20	8.33

The best cells for each wafer are around 16% efficient, with good reproducibility from run to run. However, the spread of efficiency within a wafer is larger than for either GaAs or AlGaAs, and varies from wafer to wafer. Consequently, the average efficiencies are variable. The overall efficiencies for the lot vary from 10 to 16.5%.

The yield of good cells again averaged about 80%, similar to GaAs and AlGaAs. However, the definition of "good" is stretched over a wider efficiency range.

2.3.3.3 Analysis

The spread in efficiency results mostly from nonuniformity in J_{SC} (see Table 2-15). We found systematic gradients in J_{SC} across the wafers, unlike GaAs and AlGaAs. These gradients were related to systematic bandgap gradients. Figure 2-13 shows a contour map of bandgap for wafer 567-3. The bandgap was generally higher at the bottom of the barrel-shaped susceptor, farther from the input gas stream, indicating a higher concentration of phosphorus. Probably we are seeing effects of more complete phosphine cracking at the bottom of the susceptor. With changes in the geometry and gas flows, it should be possible to improve the uniformity significantly. It should be kept in mind that GaAsP is a new material for us, and still needs more development than GaAs or AlGaAs.

We found no apparent correlation of efficiency with either substrate vendor or reactor cleaning history. If present, these effects are second order and masked by growth nonuniformities.

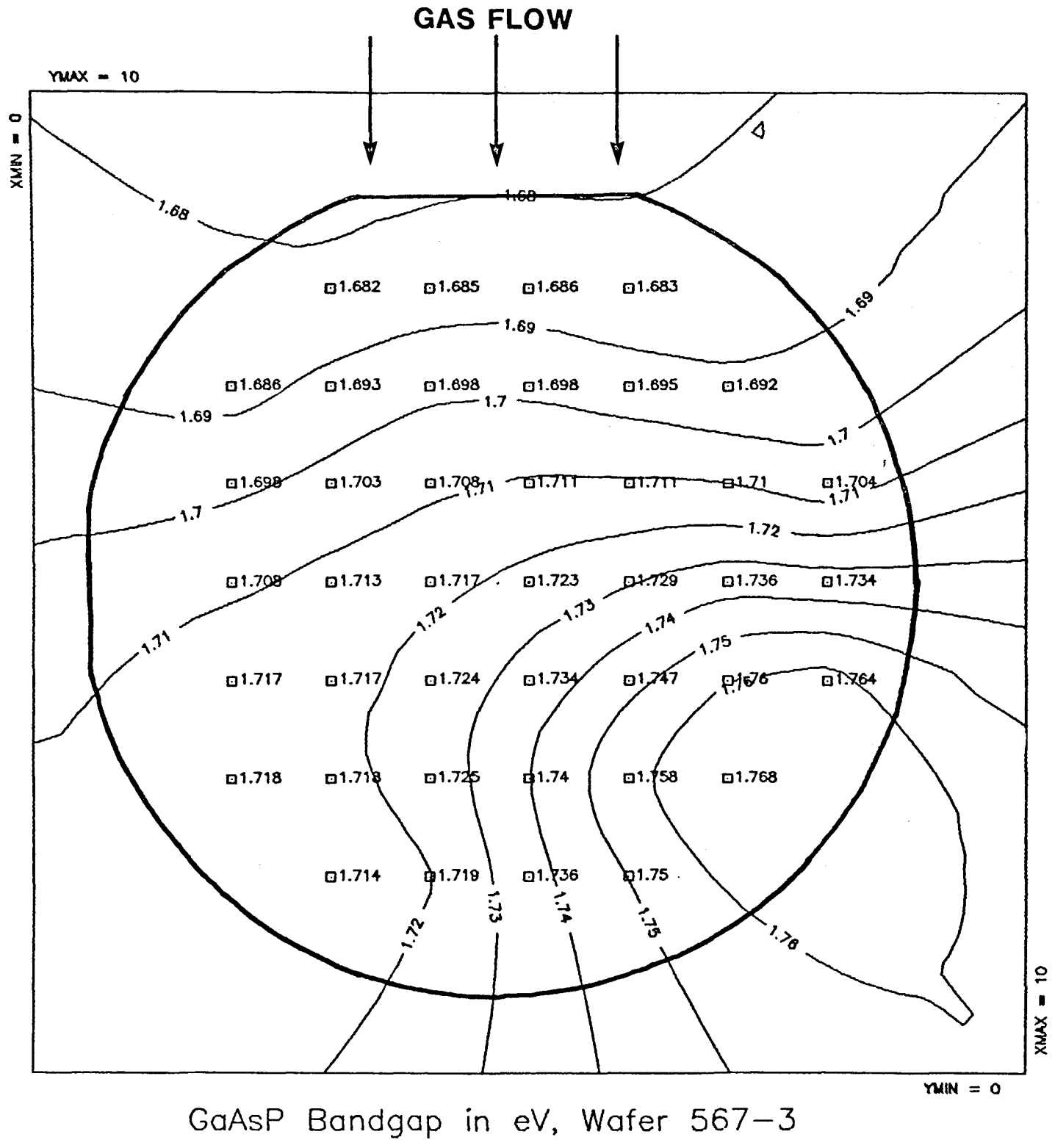

FIGURE 2-13 UNIFORMITY MAP OF GaAsP BANDGAP ACROSS A SOLAR CELL WAFER.

2.4 COMPARISONS OF DIFFERENT CELL MATERIALS

The efficiency distributions are summarized and compared for the three cell materials in Figure 2-14. Each curve shows the fraction of the total number of cells that meet or exceed a given efficiency. For example, 62% of the GaAs cells had efficiencies of 19% or greater. Each curve includes all cells that were processed from five different growth runs, roughly 150 for each material. The GaAs curve does not include cells from run 505. The efficiency of AlGaAs cells has been corrected for spectral mismatch to allow a valid comparison with GaAs and GaAsP cells.

The most obvious features of the figure are the higher efficiencies and tighter distributions in the descending order of GaAs, AlGaAs, GaAsP. Maximum efficiencies of the three materials were 20.5, 17.7, and 16.5 percent, respectively. Some of this difference is expected because of the energy bandgap differences; the higher bandgap cells have lower efficiencies. To see how much of the efficiency difference is due solely to bandgap, we have plotted the experimental V_{oc} and J_{sc} vs. bandgap in Figures 2-15 and 2-16. Also plotted in the figures are the theoretical limits. The limit for J_{sc} was calculated by integrating all available power in the AM1.5 Global spectrum up to a given energy gap. This assumes 100% external quantum efficiency. The curve has some structure corresponding to structure in the terrestrial spectrum. The theoretical limit for V_{oc} was calculated after Henry[4], assuming radiative recombination to limit V_{oc}, and using the theoretical limit J_{sc} values.

From Figure 2-15, the AlGaAs V_{oc} values are closer to the theoretical limit than is GaAsP. In fact, the difference between theory and measured values is almost the same for GaAs and AlGaAs. This points to the high quality of our AlGaAs material. The GaAsP cells, on the other hand, were limited by high space-charge-layer generation-recombination dark currents, and so had lower V_{oc}. It should be possible to reduce the dark current by improving the lattice grading between the substrate and GaAsP active layers, and so reduce the number of recombination sites at crystal defects.

From Figure 2-16, all three materials had J_{sc} values somewhat less than 80% of the theoretical maximum. This could be improved in all cases by reducing extrinsic losses (shadow and reflection) with more sophisticated processing. (In these experiments, the process was deliberately kept simple to minimize the effects of process variations.) It is encouraging that AlGaAs and GaAsP cells are similar to GaAs in relation to the

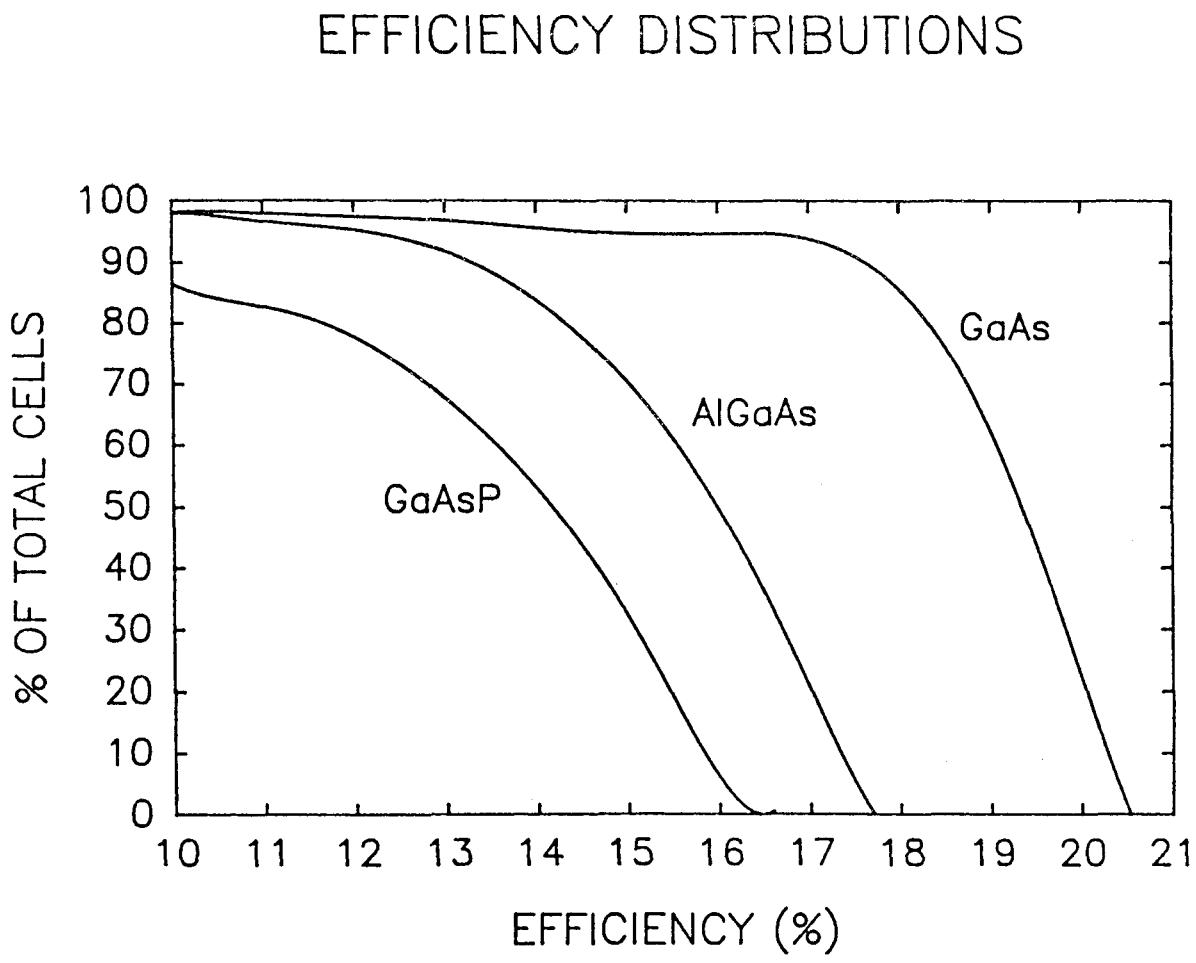

FIGURE 2-14. OVERALL SUMMARY OF THE SOLAR CELL REPRODUCIBILITY EXPERIMENT, COMPARING THE EFFICIENCY DISTRIBUTION OF GaAs, AlGaAs, and GaAsP CELLS.

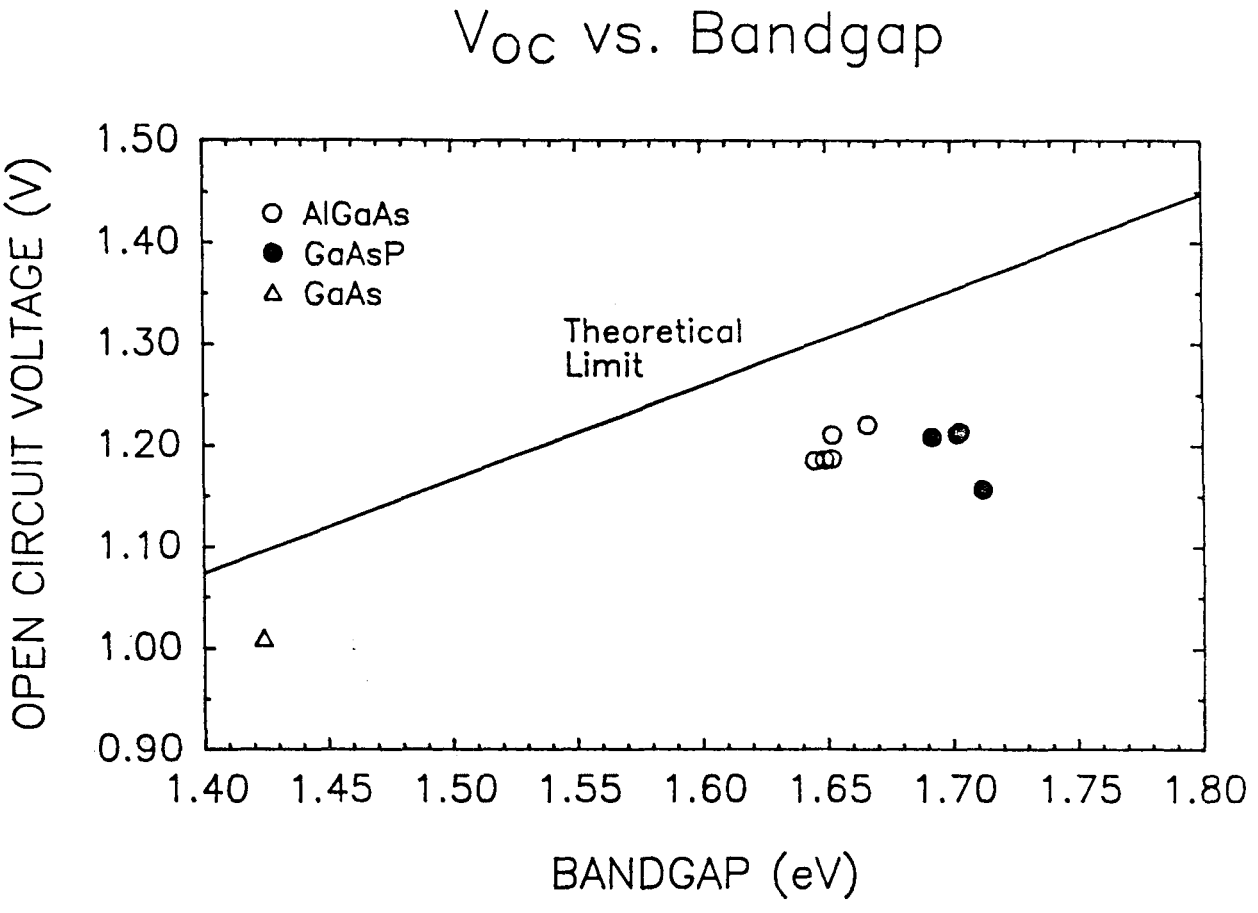

FIGURE 2-15. COMPARISON OF THEORETICAL AND EXPERIMENTAL OPEN CIRCUIT VOLTAGES AS FUNCTION OF BAND GAP.

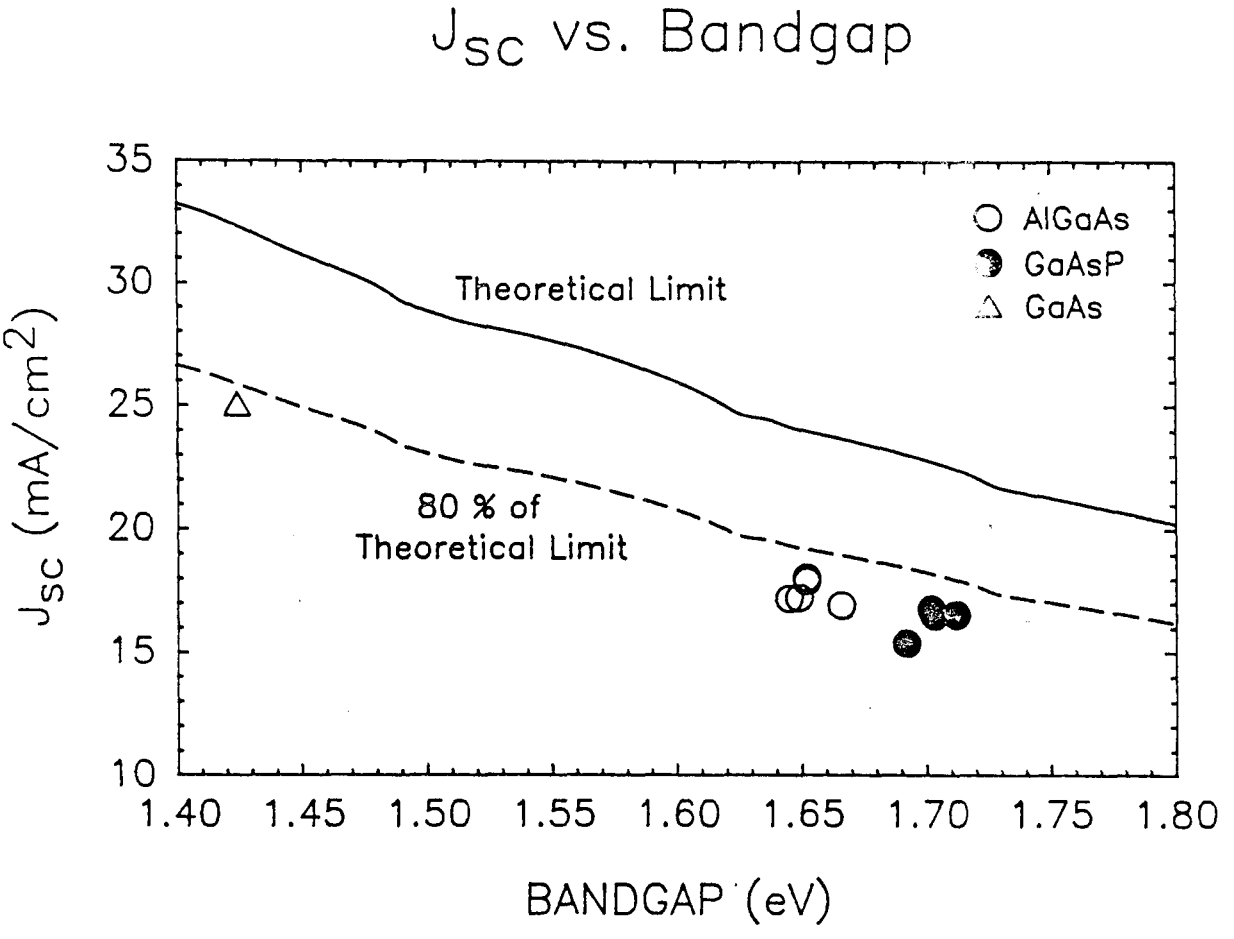

FIGURE 2-16 COMPARISON OF THEORETICAL AND EXPERIMENTAL SHORT CIRCUIT CURRENT DENSITIES AS FUNCTIONS OF BAND GAP.

theoretical J_{sc} limit. Despite the high dislocation densities in GaAsP, and the lower diffusion lengths in AlGaAs, we are able to obtain high collection efficiencies in these materials, similar to GaAs.

We conclude that, at the present state of development, AlGaAs is superior to GaAsP for the 1.7 eV high-bandgap cell in a tandem structure. It has demonstrated higher efficiencies than GaAsP, even when the bandgap differences are taken into account, and better uniformity. At least part of its advantage lies in more extensive development of material growth and device processing technologies. GaAsP, on the other hand, is intriguing because it has produced high efficiency cells even with very limited development. This material seems to be relatively insensitive to high densities of crystal defects. For applications as the top cell in a lattice-mismatched monolithic tandem, GaAsP may prove to be the better material in the long run.

2.5 CONCLUDING REMARKS

The overall results of this study have been quite encouraging. The yield of high-efficiency cells was very good, especially for GaAs. We have seen excellent uniformity within a wafer and very good reproducibility from run to run. The major problem with reproducibility in this type of experiment is probably the overwhelming urge to vary parameters in a research environment. In a production environment, we would expect to see further improvement of the yields as processes are standardized. The yield-related problems that we did identify can be summarized as follows:

1. Leaky cells near the periphery of wafers, probably resulting from handling or substrate wafer preparation. Obvious solutions are to keep cells away from the edges, or develop better handling methods.

2. Nonuniformity in the phosphorus content of GaAsP layers. More development of the material growth process is needed.

3. Breakage of GaAsP cell wafers, caused by stress and warpage presumably related to lattice mismatch with the substrate.

SECTION 3
SUMMARY

The following areas of research have been addressed under this contract phase with results as noted:

- Start-up and characterization of a new MOCVD reactor for the growth of GaAs, GaAlAs, and GaAsP on five two-inch diameter substrates with excellent uniformity.
- Optimization of the growth of Ge films on Si by a simple CVD technique.
- Production of a 9% efficient GaAs-on-Ge-on-Si solar cell.
- Much advancement in the understanding of the GaAs-on-Si growth process and in the quality of grown films.
- Production of a 7% efficient GaAs-on-Si solar cell.
- Development of a GaAsP-on-GaAs growth technology.
- Production of a 16.5% efficient GaAsP (1.7 eV) solar cell on GaAs.
- Production of a 17.7% efficient GaAlAs (1.7 eV) solar cell on GaAs.
- Production of a 20.8% efficient GaAs-on-GaAs solar cell.
- Improvements in cell processing technology, including the use of a double-layer AR coating.
- Study of the reproducibility of solar cell production (GaAs, GaAlAs, and GaAsP cells) in a research laboratory environment.

SECTION 4
ACKNOWLEDGEMENTS

The authors would like to gratefully acknowledge the contributions of Messrs. Victor Haven and John Enterkin for the MOCVD growths; Ms. Clara Bajgar, Mr. Chris Keavney, and the personnel of Spire's Process Laboratory for solar cell fabrication; Mr. Michael Sanfacon for device characterization; and Ms. Judy Breen for manuscript preparation.

SECTION 5
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Document Control Page	1. SERI Report No. SERI/STR-211-3188	2. NTIS Accession No.	3. Recipient's Accession No.

4. Title and Subtitle
Gallium Arsenide and Multibandgap Solar Cell Research, Final Subcontract Report, April 1984 - April 1986

5. Publication Date
July 1987

6.

7. Author(s)
S. M. Vernon, S. P. Tobin, and R. G. Wolfson

8. Performing Organization Rept. No.

9. Performing Organization Name and Address
Spire Corporation
Bedford, MA 01730

10. Project/Task/Work Unit No.
3496.20

11. Contract (C) or Grant (G) No.
(C) XL-4-04024-1
(G)

12. Sponsoring Organization Name and Address
Solar Energy Research Institute
A Division of Midwest Research Institute
1617 Cole Boulevard
Golden, Colorado 80401-3393

13. Type of Report & Period Covered
Technical Report

14.

15. Supplementary Notes
Technical Monitor: Cécile Leboeuf

16. Abstract (Limit: 200 words)

This report presents results of research in high-efficiency, low-cost solar cells, emphasizing heteroepitaxial growth of a III-V compound material onto a single-crystal silicon wafer. The report describes the start-up and characterization of a new metal-organic vapor deposition (MOCVD) reactor for the growth of GaAs, GaAlAs, and GaAsP on 2-in.-diameter substrates with excellent uniformity; optimization of the growth of Ge films on Si by a simple CVD technique; and production of a 9% efficient GaAs-on-Ge-on-Si solar cell. The advancements in the understanding of the GaAs-on-Si growth process and in the quality of the films are described. The work also included production of a 7% efficient GaAs-on-Si cell; development of a GaAsP-on-GaAs growth technology; production of a 16.5% efficient GaAsP cell and a 17.7% efficient GaAlAs cell on GaAs; and production of a 20.8% efficient GaAs-on-GaAs cell. Also described are improvements in cell processing technologies, including the use of a double-layer antireflection coating.

17. Document Analysis

a. Descriptors
Photovoltaic cells ; silicon solar cells ; gallium arsenide solar cells ; chemical vapor deposition ; efficiency

b. Identifiers/Open-Ended Terms

c. UC Categories
63

18. Availability Statement
National Technical Information Service
Department of Commerce
5285 Port Royal Road
Springfield, Virginia 22161

19. No. of Pages
57

20. Price
A04