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RADIATION-TOLERANT HIGH-VOLTAGE CMOS/MNOS TECHNOLOGY*

~~FOR MNOS PERIPHERALS*~~

G. F. Derbenwick and W. C. Black, Jr.+
X3274
sec x5426
Sandia Laboratories
Albuquerque, NM 87185

ABSTRACT

A radiation-tolerant metal-gate CMOS technology has been developed for use on non-volatile MNOS integrated circuit chips. These CMOS peripherals are capable of the high voltage operation (> 25 V) required to drive the memory array and require only the standard seven mask levels, including passivation. One additional mask is required to define the MNOS memory array. Fabrication and characterization of these circuits is described. Processing sequences compatible with known radiation-hardening procedures have been defined.

INTRODUCTION

A common problem in the fabrication of metal-nitride-oxide-silicon (MNOS) nonvolatile memories is the design of peripheral circuitry which can handle the high voltages (> 25 V) required to drive the memory array for high performance. Usually epitaxial silicon substrates are used where deep diffusions are performed to isolate regions of the epi layer. In this manner the potentials of the isolated epi regions can be controlled permitting high voltage write-erase pulses to be applied between a memory gate and epi substrate. Because of the high voltages, usually p-channel devices with depletion-mode loads are used. In general, these circuits suffer from slow speed, high standby power dissipation, and low radiation tolerance due to the depletion load devices used. An attractive alternative would be to use CMOS peripherals, but it has been difficult to obtain enhancement mode n-channel devices with drain breakdown voltages greater than 25 or 30 volts without resorting to extra diffusion and masking steps (1,2). The recently developed inverted CMOS process (3) is particularly attractive for MNOS peripherals since it is capable of high-performance, high voltage operation, and the p-channel memory array is automatically isolated in a separate n-well. This avoids the necessity of using epitaxial silicon wafers to provide the isolation for write and erase operations. The process presented here is a modification of the basic inverted CMOS process which permits fabrication of MNOS transistors on the same chip and provides for radiation-tolerant operation. Because of the inherent speed of the high voltage CMOS, the technology is particularly suitable for RAM applications.

FABRICATION

A cross section of the inverted CMOS-MNOS structure is shown in Figure 1. Two possible mask sequences for fabrication of radiation hardened circuits are shown in Table I. The circuit is fabricated on <100> 8-16 ohm-cm p-type silicon and phosphorus n-wells are implanted at 170 k eV with a fluence of 1×10^{13} cm^{-2}. These receive a 24-hour drive at 1200°C. Diffused p and n sources and drains are defined and driven-in. After field oxide deposition the gate windows are cut and a pregate boron threshold adjust is performed. For process labelled A, steam gate oxides are grown at 850°C, and memory gates and contact windows are then opened. After Si_3N_4 deposition the nitride is stripped from the peripheral gates and a nonselective clean-etch is used to guarantee that all contact windows are open. Metal deposition and definition and p-glass passivation complete the process.

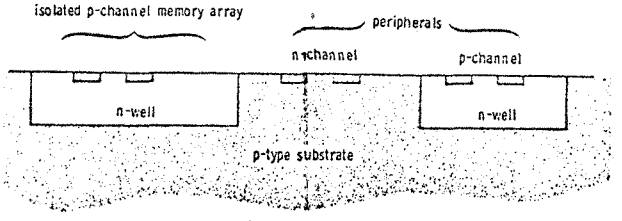

Figure 1. Cross section of the inverted CMOS structure. For simplicity, the oxide and metallization are not shown.

Although stripping the nitride in process A improves the radiation hardness of the gate oxides as compared to that of an unstripped

*This work supported by the U. S. Department of Energy (DOE) and Air Force Weapons Lab, Kirtland AFB, NM.
+Present Address: Dept. of Elect. Engr. and Comp. Sci., Univ. of Calif., Berkeley, CA 94720.

SiO_2-Si_3N_4 sandwich (4), the hardness is inferior to that of an 850°C wet oxide immediately after growth. It is believed that the ammonia anneal received by the gate oxide during nitride depositon may be responsi- ble for the degraded hardness. The radiation hardness can be enhanced if the peripheral gate oxide is grown last as indicated by process B in Table I. This involves a tradeoff since the memory transistor characteristics are affected by the "wet oxide anneal" of the nitride (5). After the pregate boron threshold adjust the nitride is deposited directly. The nitride is defined and etched so that it remains only in the memory channels. The 850°C wet oxidation follows with the nitride preventing oxidation in the memory transistor channel. Contact windows are cut and metallization and passivation follow. Both process sequences A and B require eight mask levels and the choice of which process to use involves a trade-off between memory transistor characteristics and circuit radiation hardness.

CHARACTERIZATION

The processes described above have been characterized and typical parameters obtained are lsted in Table II. The n-well must be driven in at least 5 or 6 μm to avoid p+ to substrate punch-through. The final choice of oxide thickness is flexible and depends upon the operating voltage and radiation hardness desired. Radiation tolerance is enhanced by using thinner gate oxides but the oxide electrical breakdown and stability under high fields place a lower limit on the oxide thickness. The p-channel K-factor, μC_{po}, can be increased by driving in the p+ sources and drains as much as 3 μm. This shortens the channel length for given mask dimensions yet punch-through is not encountered due to the heavier phosphorus concentration at the n-well surface. However, the n+ sources and drains cannot be driven in more than about 2.5 μm due to the onset of punch-through. The high parasitic vertical pnp bipolar gain indicates that either gold doping (6) or neutron irradiation (7) will be required to eliminate radiation-induced parasitic SCR latch-up.

The n- and p-channel threshold voltages can be selected by varying the pregate boron threshold adjust. This is shown in Figure 2 for the n-channel transistor for both wet and dry oxidations. The threshold adjust is more effective for the wet oxide presumably because the 850°C wet oxidation does not drive the boron in as far as the 1000°C dry oxidation. Degradation of the n+ drain breakdown voltage due to the threshold adjust implant is barely observed for V_{Tn} = 3 V for the wet oxide, but is degraded to about 30 V for V_{Tn} = 1 V for the dry oxide. This dictates the use of a hardened 850°C wet oxide for the processing rather than a hardened 1000°C dry oxide.

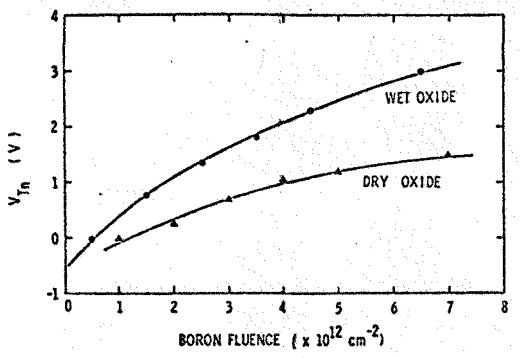

Figure 2. N-channel threshold voltage vs. 25 keV pre-gate boron threshold adjust fluence. Curves for 850°C wet and 1000°C dry oxides are shown. P-channel voltage shifts are about 80 percent of the n-channel shifts for the same fluence.

The degradation of the n-channel K-factor, $\mu_n C_o$, due to the threshold adjust implant is shown in Figure 3. This is caused by increased impurity scattering for carriers in the inversion layer. The p-channel transconductance actually increases slightly with increasing threshold adjust. The boron implant at the surface probably causes the actual inversion layer to be centered somewhat below the Si-SiO_2 interface, reducing the surface scattering.

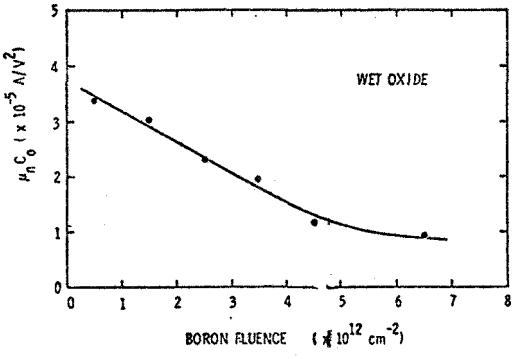

Figure 3. N-channel K-factor, $\mu_n C_o$, versus threshold adjust fluence.

The field threshold over the n-well is sufficiently high initially and becomes higher after irradiation such that guardbands are not required in the n-well. Guardbands are required in the p-substrate.

DISCUSSION

The major problem in developing a simple high voltage CMOS process is obtaining enhancement mode n-channel transistors with large

drain breakdown voltages. With careful adjustment of the p-well implant, drive-in and boron threshold adjust, we have tailored the doping profile such that n-channel threshold voltages of +2 V and drain breakdown voltages of about 26 V are obtained, but it is difficult.

Inverted CMOS offers some big advantages over conventional CMOS. First, drain breakdown voltages are easier to control. The metal semiconductor workfunction differences ($\phi_{MS} \approx$ -1V for n-channel, $\approx$ -0.2 V for p-channel) are such that much lower n-well surface concentrations are required to get acceptable p-channel threshold voltages. Since phosphorus piles up at the surface, the dopant concentration deeper in the n-well is still lower. Hence, much higher and controllable breakdown voltages are observed in n-wells than in p-wells. Likewise, the lightly doped p-type substrate prevents the n^+ breakdown voltage from occurring at the sharp radius of the junction--it is usually limited by the shallow boron threshold adjust implant.

Another major gain results since most Si_3N_4 memory transistors perform best as p-channel devices (the two memory threshold voltage states occur at negative gate voltages). Isolation of the memory array would require epitaxial silicon for conventional CMOS, but p-channel memory arrays are automatically isolated in n-wells for inverted CMOS.

The third big advantage is that guardbands are required only over the substrate for inverted CMOS. After irradiation field thresholds become higher over n-type silicon and lower over p-type silicon so guardbands would be required for both n- and p-channel transistors for conventional CMOS.

Tunnels in inverted CMOS are n+ diffusions. Since these have lower sheet resistances than p+ tunnels, drive capabilities are enhanced for inverted CMOS.

Finally, the effectivenss of the threshold adjust implant is about equal for both n- and p-channel transistors in inverted CMOS and a nonselective pregate threshold adjust can be used. In conventional CMOS the p-channel transistors must be masked when the n-channel threshold adjust is performed since the p-channel voltage shift is about three times greater than the n-channel threshold shift for the same threshold adjust implant.

The major disadvantage of inverted CMOS is a lower transconductance for the p-channel device since it is in a heavier-doped region. This can be greatly offset, however, by driving the p+ sources and drains in deeper giving shorter actual channel lengths and lower p+ sheet resistances.

RADIATION HARDENING

Radiation tolerance of this technology is enhanced by using gate oxides less than 100 nm thick, eliminating the Si_3N_4 from the peripheral transistors, avoiding threshold adjust implants through gate oxides, and fabricating on <100> substrates. Metal-gate technology has been chosen since silicon gate radiation-hardened technologies tend to require shallow junctions with inherently low breakdown voltages.

Hardening considerations also dictate the allowable memory transistor structures. Usually MNOS transistors have so-called step gate or gate-protected structures as shown in Figure 4(a). The two peripheral thick SiO_2 transistors in series with the thin SiO_2 memory gate

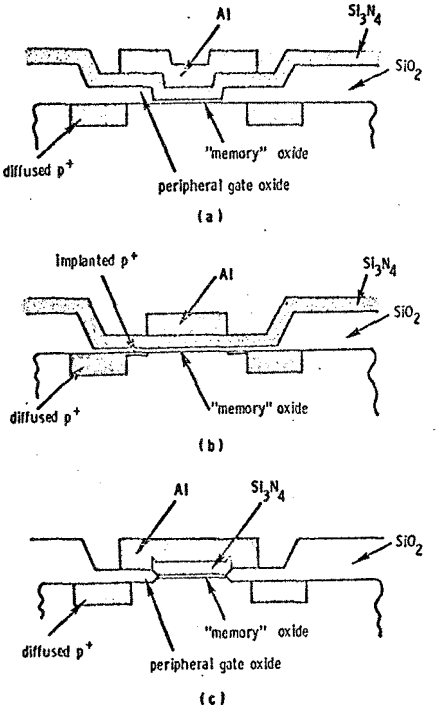

Figure 4. Memory Transistor Structures.
(a) Conventional stepped-gate,
(b) stripped-nitride self-aligned,
(c) locally oxidized stepped-gate.

perform two functions. They prevent depletion mode operation by always cutting the channel off at the peripheral transistor enhancement mode threshold, and they prevent tunneling due to high fields at the drain when the drain is biased a write voltage away from the gate. However, the structure shown in Figure 4(a) is radiation intolerant due to large negative threshold voltage shifts (positive charge trapping) in the composite thick SiO_2-Si_3N_4 gate structure. Thinning the peripheral gate SiO_2 layer increases the radiation tolerance (1) but is suspected of giving rise to gate instabilities due to the large number of traps in the gate insulator.

Since the Si_3N_4 cannot be stripped in a pattern self aligned with the step in the gate, the stripped-nitride process (A, Table I) requires a monogate structure. To minimize the large gate to drain overlap capacitance, the structure shown in Figure 4(b) can be fabricated. The nitride is stripped so that it only remains in the center of the channel and a non-selective boron implant after metallization definition connects the source and drain up to the channel. The subsequent 450°C sinter provides sufficient activation for this implant. This structure suffers from parasitic sidewall subthreshold leakage current (8) since the channel width cannot be defined by the metal pattern. Whether one choses to accept subthreshold leakage or high gate-to-drain capacitance when the stripped nitride process is used depends upon circuit design considerations.

A stepped gate structure for the memory-gate-first process (B, Table I) is shown in Figure 4(c). The peripheral stepped gates are automatically self-aligned with the nitride cut. Since the peripheral gate oxide is grown last, this technology has the greatest radiation hardness. However, the effect on radiation hardness of the "bird's beak" which forms at the edges of the nitride has not been assessed yet.

TABLE I

Mask Level	Process A	Process B
1	n-Well	n-Well
2	p^+ Source & Drain	p^+ Source & Drain
3	n^+ Source & Drain	n^+ Source & Drain
4	Gate & Contact Window	Gate & Contact Window
5	Memory Gate & Contact Window	Nitride Definition
6	Nitride Strip	Contact Window
7	Metallization Pattern	Metallization Pattern
8	Passivation Windows	Passivation Windows

CONCLUSIONS

High voltage inverted CMOS-MNOS processes have been defined and characterized. Radiation tolerance has been enhanced by avoiding dele- terious processing steps. Radiation tolerant memory cell structures have been designed.

TABLE II

	R_S(Ω/□)	X_J(μm)	V_{BD}(V)
N-well	1000	7	
p^+	15	2.4	36
n^+	7	2.4	35

oxide thickness	70 nm
nitride thickness	50 ± 5 nm
$\mu_p C_o$	5.4×10^{-6} A/V^2
n-well field threshold	-36 V
p-substrate field threshold	-6 V
parasitic pnp gain	120

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