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A FOUR-CHANNEL BIPOLAR MONOLITHIC PREAMPLIFIER FOR RHIC DIMUON PAD READOUT*

C. L. Britton, Jr., E. J. Kennedy†, R. A. Todd, A. L. Wintenberg, G. R. Young

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Abstract

This paper presents a four-channel, low power-consumption bipolar monolithic preamplifier designed to amplify signals from pads with detector capacitance values from 10 pF to 50 pF used in a RHIC (Relativistic Heavy Ion Collider) dimuon experiment. The circuit utilizes a folded-cascode topology with a novel feedforward compensation that improves the low-capacitance transient response and provides self-biasing without resorting to bandgap or current references. The circuit was fabricated by Harris Semiconductor in the VHF dielectrically isolated complementary bipolar process. Measured data for gamma irradiation to 1.25 MRad are presented.

*Research sponsored by the U. S. Department of Energy. The Oak Ridge National Laboratory is operated by Martin Marietta Energy Systems, Inc. for the U. S. Department of Energy under Contract No. DE-AC05-84OR21400

(manager (C. Britton will correct)

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I. INTRODUCTION

The proposed pad readout chip architecture for RHIC experiments shown in Fig. 1 includes preamplifiers, analog memory, A/D converter circuitry, and appropriate tagging and crossing-select circuitry. Two approaches were considered for implementation: a consolidated readout with the preamp through the ADC on one chip, and a distributed readout where memory through the ADC was separate from the preamp chip.

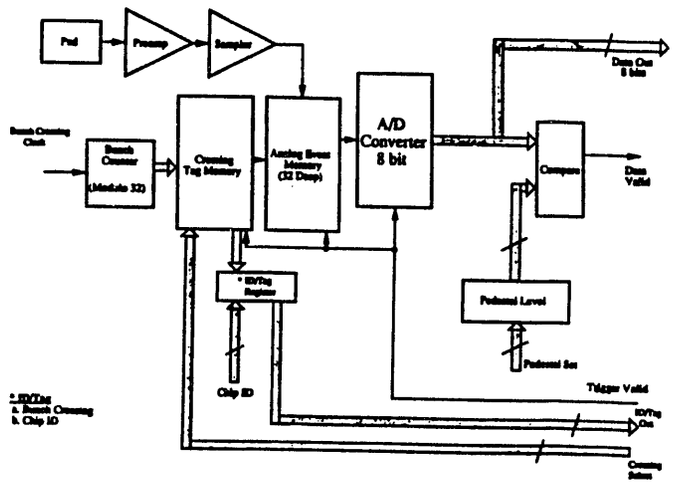

Fig. 1 Proposed Pad Readout Chip Architecture

A consolidated solution was considered advantageous because there were few off-chip analog signals and the system cost might be reduced, but possibly it was not the best partitioning of technologies with respect to speed and noise, because the preamplifier could be implemented in bipolar with lower noise and higher speed. The distributed readout approach would likely optimize each portion of the system at the cost of a larger wiring plant and higher expense.

To implement the preamplifier for the distributed readout, a design was submitted as part of the Oak Ridge National Laboratory (ORNL) beta site test of the Harris FASTRACK software. This test resulted in a multiproject 10-wafer run with Harris as well as review of the software operation. The Harris system process was considered to be a candidate for the high-energy and heavy-ion physics environment because of its high bandwidth, low noise, and radiation tolerance characteristics[1], which are required of preamplifiers in high-radiation environments such as electromagnetic or hadron calorimeters. Besides the pad readout preamplifier for RHIC, eight other circuits were implemented. Seven of these were preamplifiers for SSC-related work[2], and one was for a non-DOE project.

II. HARRIS FASTRACK SOFTWARE AND VHF PROCESS

FASTRACK, a complete ASIC development system on a single industry-standard workstation, is configured around the Cadence Analog Artist tools and includes schematic capture, Harris' SLICE circuit simulator, Cadence waveform display, and layout tools with design rule checker as well as Cadence PD compare, which checks layout vs. schematic, and Cadence PD extract, which performs a layout component extraction. Extraction is helpful when simulating behavior of the layout with the parasitic wire capacitances included. Because of some problems with the AC analysis of an early Beta version of the SLICE circuit simulator, the simulated noise numbers quoted in this paper were obtained by using HSPICE. The statistical performance analysis capability available with FASTRACK allowed the designer to predict the performance spectrum and to estimate yield to any given specification such as noise, bandwidth, or power dissipation. The analysis uses correlated random number techniques in setting device parameter variations based on the manufacturing process statistics.

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The Harris VHF process is a dielectrically isolated 20-V bipolar process with transition frequency (f_T) values of 1.2 GHz (npn) and 1.0 GHz (pnp). Early voltages (V_A) were nominally 90 V (npn) and 18 V (pnp), with nominal current gains of 150 (npn) and 125 (pnp). A p-channel JFET device, diffused and thin-film resistors, MOS capacitors, a zener diode, and manufacturing structures were also provided.

III. Preamplifier Circuit Topology

The circuit, shown in Fig. 2, is essentially a folded-cascode amplifier with a diamond driver output stage. The primary amplification path is the cascode QIN1-Q1 and the output driver stage comprised of Q3, Q4, Q7, and Q8. DC Bias is provided by Q2, Q5, and Q6, which are current sources, and Q9-Q10, which, in addition to their associated resistor and capacitor strings, provide both DC voltage bias and feedforward compensation. The gain of the Q9-Q10 paths at frequencies below 10 KHz is approximately 5% of the main cascode path. The chip layout for a quad configuration (i.e., 4 preamps) is shown in Fig. 3. The feedback resistor and feedback capacitor are externally connected between the INPUT and OUTPUT terminals.

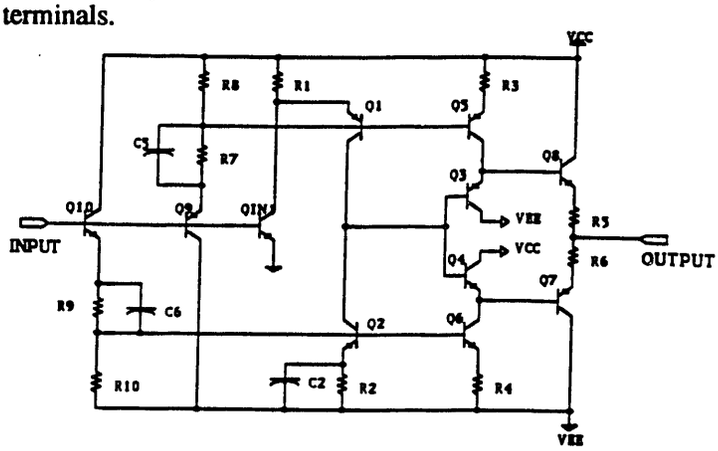

Fig. 2 Circuit schematic

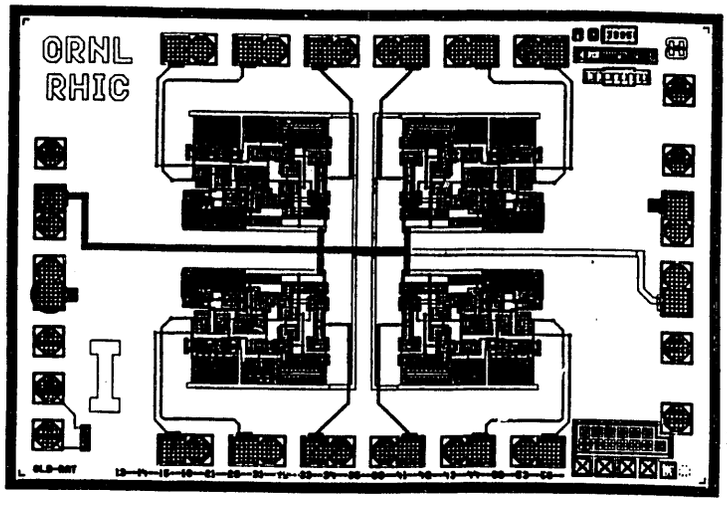

Fig. 3 Circuit layout

The large output charge of the pad system (~5 M electrons/minimum ionizing particle) required a preamplifier conversion gain of approximately 0.5-1 V/pC. This corresponded to a feedback capacitor of 1-2 pF. The input signal was to be similar to one already reported[3] with a peaking time of 20 ns or less resulting in a slew-rate requirement, for 2 V output, of ~100 V/μs. It should be noted that, for comparative purposes, the noise and risetime data reported in this paper are for input pulses of ~1 ns risetime. Because of the large feedback capacitor (when compared to 0.1-0.3 pF used in silicon strip and straw-tube front-ends), the resultant loop transmission can become high for small detector capacitances. The high loop transmission results in a fast rise time (assuming an appropriately fast transistor process has been employed) and a small phase margin. One constraint for this preamplifier was the required stability over a range of 10 to 50 pF detector capacitance (CD). When designing with processes whose f_T is on the order of 1-4 GHz, the designer must keep in mind that these high transition frequencies occur not at 50-100 μA, but closer to 0.5-1 mA. If any need for low power consumption exists, transistors will probably be operating with f_T closer to 300-500 MHz. In the case of this preamplifier, poles due to the transistor f_T began to be important at 300-500 MHz. Phase effects become apparent at frequencies lower than amplitude effects for most systems, so that even at 50 MHz the f_T affects the overall phase margin. Typically, the overshoot of preamplifiers causes little problem with the resultant pulse response of the time-invariant, semi-gaussian filters that were planned for this system because the filter peaking time was 50 ns. The concern is therefore one of yield; with process variations that are inherent in any semiconductor process, how many preamplifiers will be made that are of adequate stability for all detector capacitances? We found that the resultant topology of Fig. 2 with feedforward via Q9 and Q10 increased the phase margin by ~10° with respect to a simple bias string for Q1. Simulations, shown in Fig. 4, reveal that this compensation has little effect below 10 MHz and begins to improve open-loop phase shift at around 50 MHz.

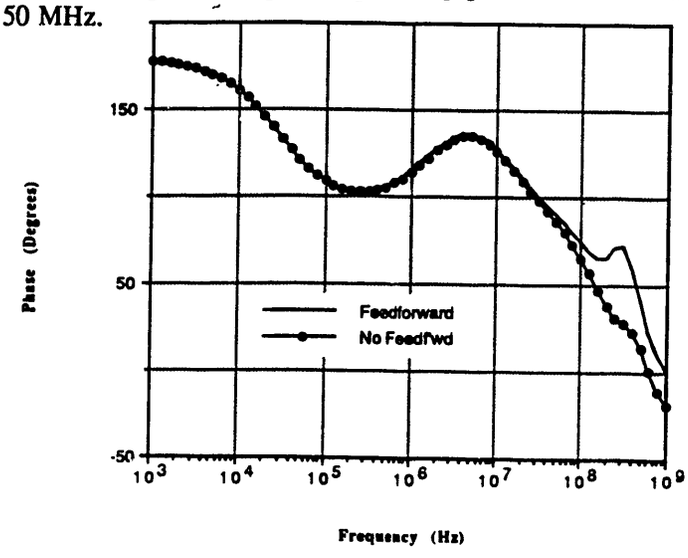

Fig. 4 Phase response simulations

The midband phase response is dominated by an effect seen when using transistors having a low Early voltage in a cascode arrangement[4]. The input impedance at the emitter of Q1 is larger than simply $1/g_m$ because of the collector-emitter resistance of Q1 (r_{o1}). This impedance is further increased by the fact that the resistance in the base of Q1 is unbypassed at midband frequencies. The "phase dip" apparent at ~ 200 KHz in Fig. 4 is due to the interaction of the changing impedance at the collector of Q1 above the dominant pole and its effect, due to feedback of r_{o1}, on the impedance at the emitter of Q1. The pole-zero pair due to c_{o1}-r_{b1}[5] of Q1 are almost coincident and thus have little effect on the overall phase. The experimentally observed transient response for the preamp is shown in Fig. 5.

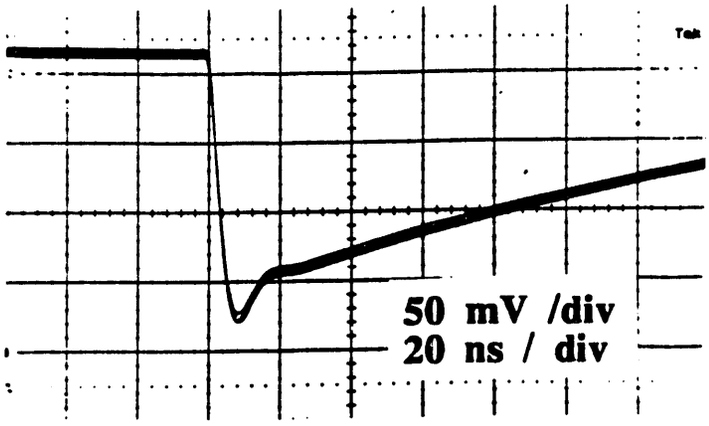

Fig. 5 Output for CD = 10 pF

IV. Manufacturing Yield

The yield of this chip during development was calculated by FASTRACK using the previously mentioned Monte Carlo techniques. Because Harris was asked to perform only DC tests on the wafer probe, the yield was based on DC parameters including power supply currents and offset voltages. The parametric yield, assuming a single circuit per chip, was 78%. The wafer run on which this circuit was included consisted of 10 wafers with 23 of the RHIC die per wafer (a single wafer consisted of ~ 800 die total of all the projects). The actual yield for this die was 61% given that two of the ten wafers were rejected. If these two wafers are not included, the RHIC die yield for the remaining eight wafers was 77%.

V. Noise Performance

The noise analysis of the traditional grounded-emitter topology has been well documented previously[6] and will not be repeated here because many noise sources are common to both topologies. Of interest, however, are the contributions of the additional noise sources unique to this topology. Figure 6 is a simulation plot of preamplifier output spot noise versus frequency for the dominant noise generators. The obvious contributors to preamplifier-generated parallel noise are normally the feedback resistor and the base (or gate) current generated by the input transistor. At low frequencies, the feedback resistor RF and the input base current of QIN1 are dominant sources predicted in the classical cascode analysis. In addition, this topology adds two other sources, the base currents of Q9 and Q10. These sources appear predictably as part of the low-frequency parallel noise. At frequencies above 4 MHz, the series noise sources of QIN1 (collector shot noise and base spreading resistance) dominate as expected. The HSPICE overall predicted noise agrees very well with the measured noise, as shown in Table I.

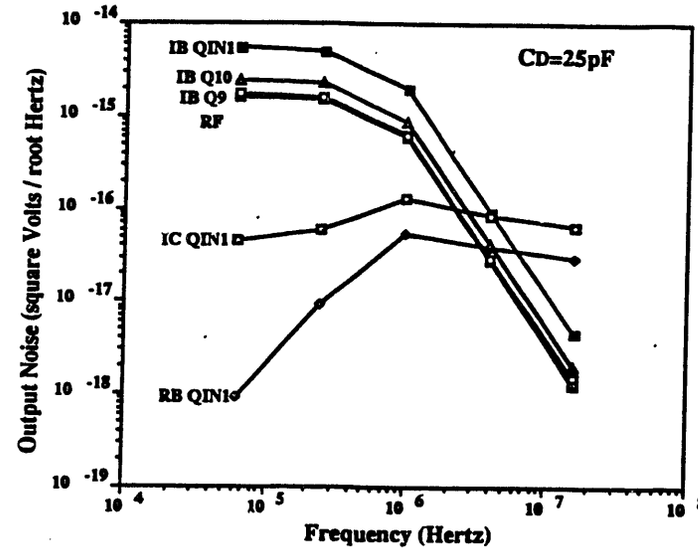

Fig. 6 Plot of simulation of output noise vs. frequency for dominant noise generators

Table I
Simulated vs. Measured Noise

CD	Simulated	Measured
10 pF	1700 e⁻	1500 e⁻
25 pF	———	2200 e⁻
50 pF	3100 e⁻	3500 e⁻

VI. Power Supply Rejection

In a large detector system, an almost certainty is that noise and voltage fluctuations will occur on the power lines going to electronics. Truly differential, high-gain amplifiers can typically be made to exhibit greater than 50-60 dB of power supply rejection at moderate frequencies. The fast, low DC gain (typically 2000 to 5000) amplifiers typically used for charge-sensitive preamplifiers at shaping time < 100 ns are more difficult to make with low power supply sensitivity. Part of the problem occurs because the input is a single-ended device and there is, therefore, little, if any, of the common-mode cancellation possible with a differential pair. Also, the input collector biasing was done using a resistor for purposes of low noise instead of using a current source which would improve the rejection somewhat. This preamplifier has a measured voltage gain from the power supply rails to the output of less than -17 dB at frequencies < 100 KHz for the

positive supply and -24 dB at frequencies < 100 KHz for the negative supply. This result compares favorably with the simulated values of -14 dB and -21 dB for positive and negative respectively. The preamplifier tests (other than power supply rejection) were performed with 29 Ω resistor in series and a 0.1 μF capacitor in parallel with each supply pin. This combination gave filtering above approximately 50 KHz. Because the center frequency of a 50 ns peaking filter lies near 3 MHz, this filtering was found to be quite adequate.

VII. Channel-To-Channel Coupling

The measured channel-channel coupling was approximately -30 dB. The reason for this value is that in the ceramic dip package version of this chip, the substrate was not tied to any reference and was left floating. In the final packaging, the substrate would be tied to ground and we would expect to see much better isolation.

VIII. Short-Circuit Protection

During assembly and testing, one problem that can occur is shorts on printed circuit boards due to solder splashes, failed components, etc. One would desire that the integrated circuits be protected and not self-destruct under fault conditions. Short circuit output protection occurs in this preamplifier because the output devices were sized such that the desired current would be supplied to the subsequent shaping amplifier, but the current gain h_{FE} would be drastically reduced for a short to ground or to a power supply, thus effectively tying the output to the fault through a silicon resistor. Upon removal of the fault, the preamplifier will return quickly to normal operation. The h_{FE} vs. I_C curve of a typical LN3 device (1 emitter stripe, 2 base stripes, ring collector) is shown in Fig. 7. IKF, the current marking the onset of high-level injection,is typically 10-20 mA. The associated PNP device has a similar IKF.

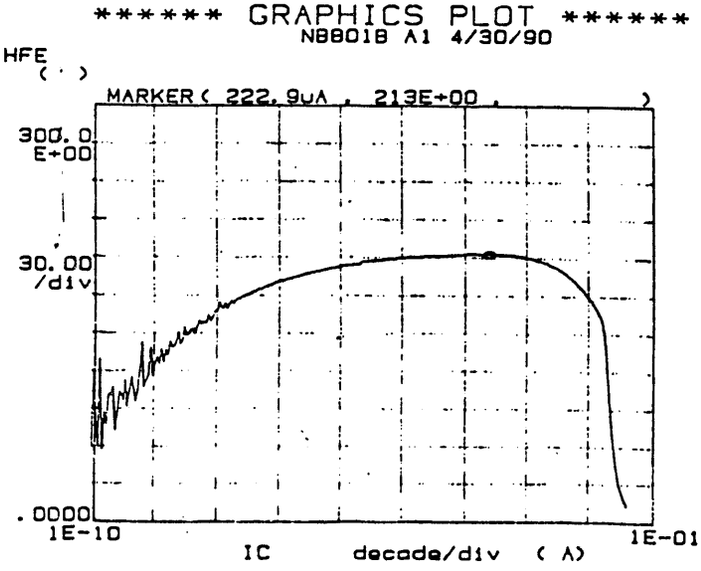

Fig. 7 h_{FE} vs. I_C for LN3 device

Another factor that contributes significantly to short circuit protection is the relatively large collector ohmic resistance for each transistor. For the LN3-size device, the collector ohmic resistance is typically 600 Ω. It is thus impossible to obtain very large output currents because of this series-limiting resistance.

IX. Radiation Effects

A summary of the Harris device measurements both before and after gamma radiation has been published[1]. The quad preamplifier was irradiated with ^{60}Co to 1.25 MRad with a dose rate of 33 KRad/hr and then tested. Pre- and post-radiation performance is summarized in Table II. As can be seen, no change occurred in risetime or slew-rate, and only a small change occurred in the noise and power dissipation. Heavy ion and neutron irradiations were not performed because of the lack of a suitable source at the time of testing.

Table II
Radiation Performance Summary

Dose (MRad)	Power mW/ch	Detector Cap (pF)	Risetime (ns) / Noise (e^-)	Slew Rate (V/μs)
0	10	9.7	4 / 1497	150
		25.7	5.8 / 2212	
		52.7	9 / 3485	
1.25	9.25	9.7	4 / 1574	150
		25.7	5.8 / -------	
		52.7	9 / 3539	

X. Discussion

The decision to pursue the consolidated readout approach ended our development of the bipolar version of this preamplifier. An all-CMOS integrated circuit designed at ORNL that includes preamplifiers, correlated samplers, analog memory pipelines, and ADC has been fabricated and is awaiting tests. If the CMOS front-end becomes unsuitable as development progresses, the bipolar approach will be resumed. The bipolar preamplifier will be used for some planned bench tests of the streamer tube-pad detector.

XI. Conclusions

A full custom bipolar preamplifier fabricated in Harris Semiconductor VHF Process was described. Data for gamma pre- and post-irradiation to 1.25 MRad indicated that the dynamic characteristics of the circuit were unchanged and that the biasing and noise showed only a few percent change after exposure to radiation.

XII. Acknowledgements

We would like to thank Harris Semiconductor for the opportunity to be involved with the beta test of FASTRACK

and the help they extended during the test. We would also like to thank Norma Hensley for her seemingly infinite patience during the preparation of this paper.

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2. C. L. Britton, Jr., et. al., *Bipolar Monolithic Preamplifiers for SSC Silicon Calorimetry*, Proc. Symp. On Detector Research and Development for the Superconducting Super Collider, Oct. 1990, pp. 523-525.

3. R. Albrecht, et. al., *Self-Quenching Streamer-Tube Detectors In the WA80 Experiment*, Nucl. Inst. Meth. A276 (1989) 131-139.

4. A. Abidi, *On the Operation of Cascode Gain Stages*, IEEE Jour. Solid State Ckts., Vol. 23, No.6, Dec. 1988, pp. 1434-1437.

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6. Veljko Radeka, *Low-Noise Techniques In Detectors*, Ann. Rev. Nucl. Part. Sci. 1988. 38: 217-277.

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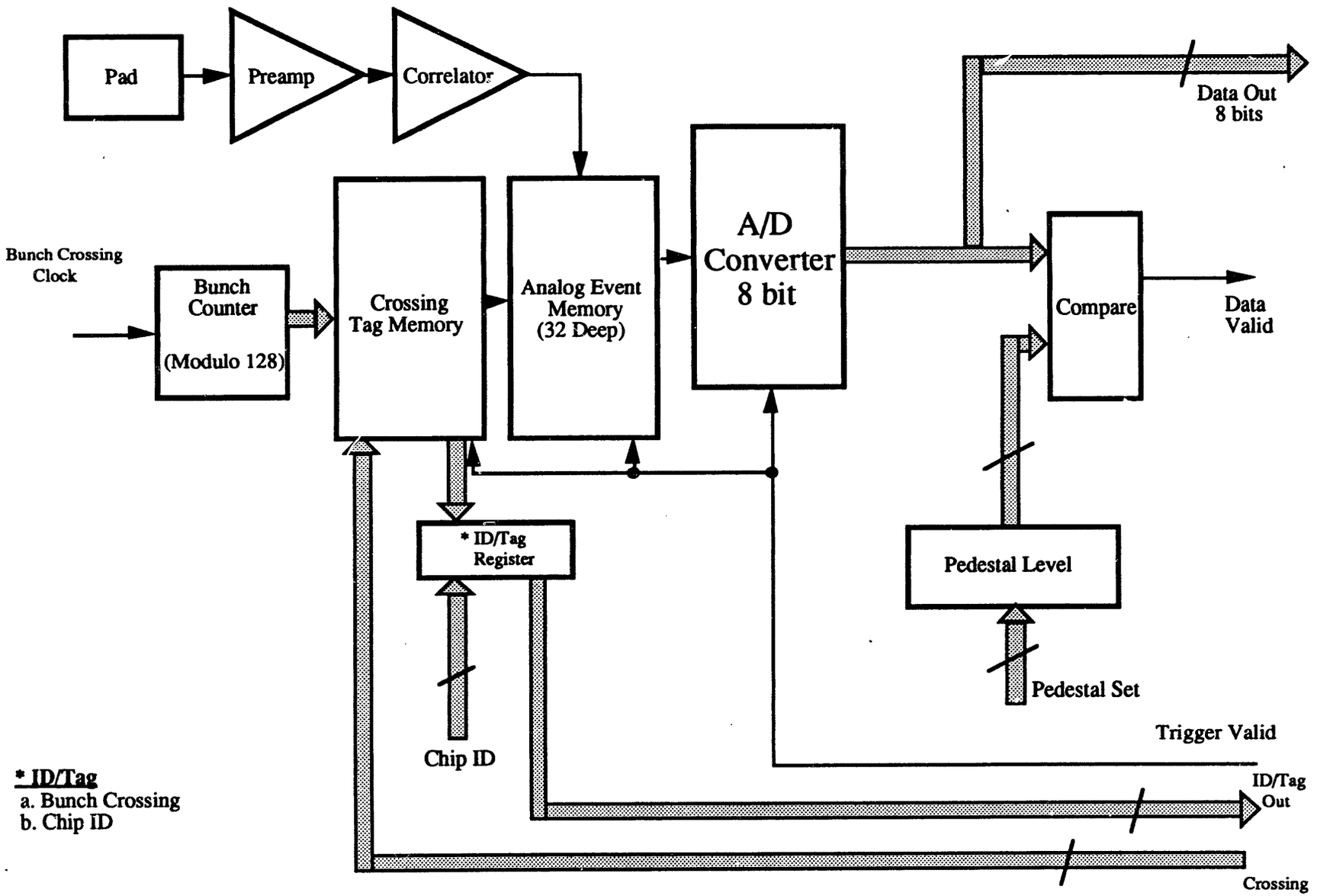
Oak Ridge National Laboratory
The University of Tennessee, Knoxville

Presented at the 1991 Nuclear Science Symposium
Santa Fe, NM
November 1991

(C. Britton will add credits/disclaimer)

This Is What We'll Cover.....

* Introduction to preamp needs
* Software beta test and VHF process
* Topology
* Yield, noise performance, supply rejection, short-circuit protection
* Measured radiation effects
* Conclusions



Proposed Pad Readout Chip Architecture

SELF-QUENCHING STREAMER-TUBE DETECTORS IN THE WA80 EXPERIMENT

R. ALBRECHT, R. BOCK, G. CLAESSON *, H.H. GUTBROD, J. HOFFMANN, B.W. KOLB, U. KOPF, A. LOOS, I. LUND **, M. MARQUARDT, A. PRZYBYLA, R. SCHULZE and T. SIEMIARCZUK +

GSI Darmstadt, FRG

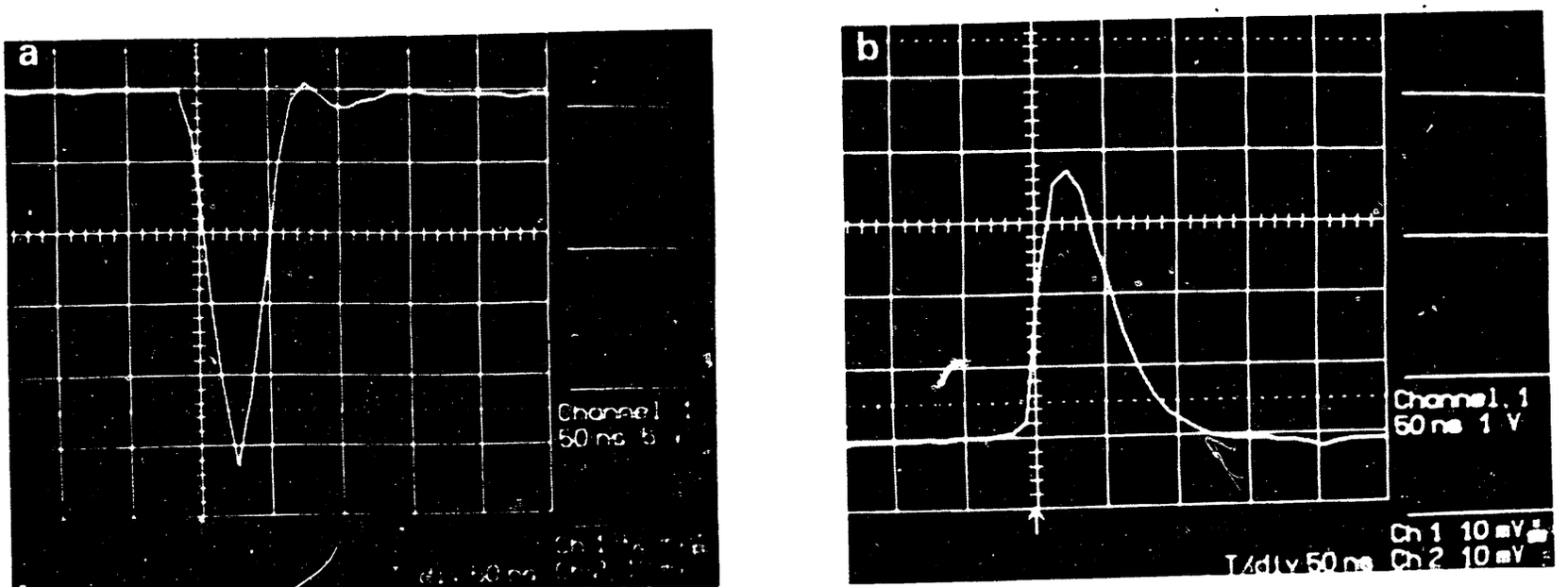


Fig. 4. (a) A negative wire signal from the streamer tubes; (b) a positive pad signal. The units on the ordinates are 10 mV per division and the units on the abscissae are 50 ns per division.

Nuclear Instruments and Methods in Physics Research A276 (1989) 131–139
North-Holland, Amsterdam

We Have Considered Two Approaches for Implementation

* **Consolidated readout**
  (preamp through ADC on one chip)
  - ***All-in-one solution (few off-chip analog signals)***
  - ***Probably cheapest***
  - ***Possibly not optimum use of technologies***

* **Distributed readout**
  (preamp chip, memory through ADC elsewhere)
  - ***Better partitioning of technologies***
  - ***Probably more expensive***
  - ***Larger wiring plant***
  - ***Reliability?***

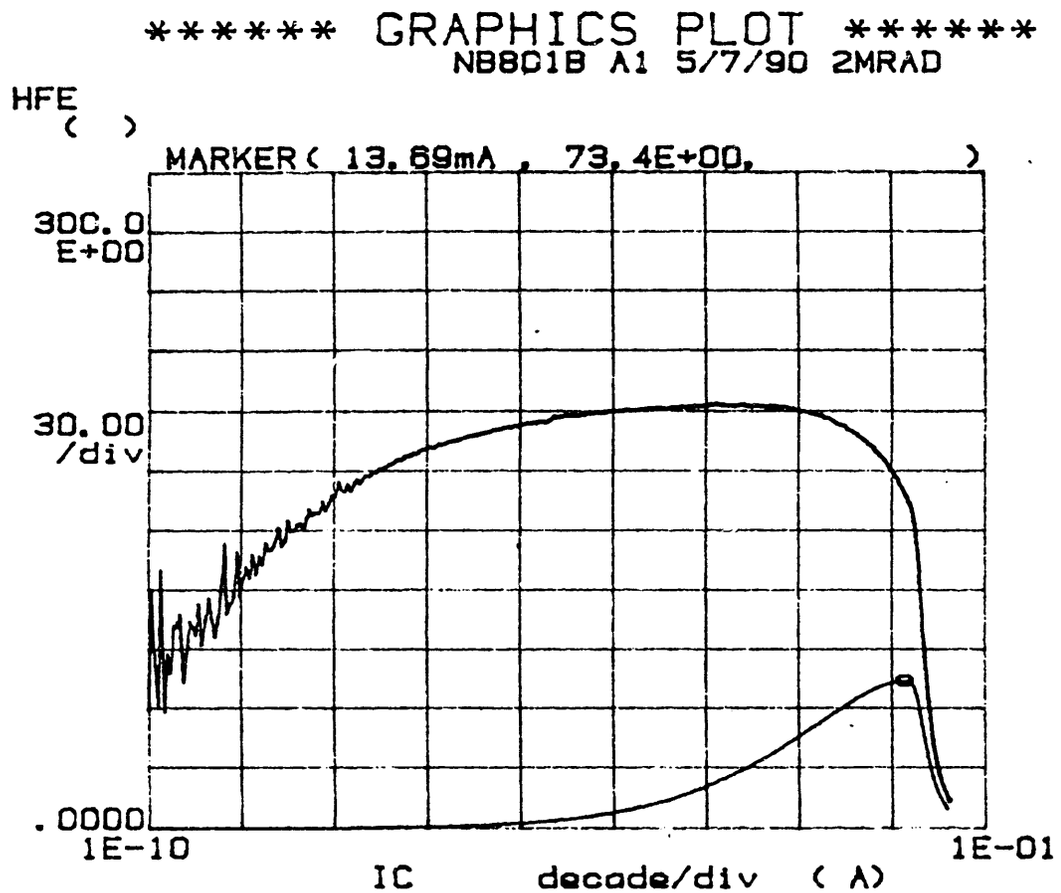
The Design Was Done At ORNL While Beta Testing Harris FASTRACK®

* Built around Cadence Analog Artist
* Includes
  - Schematic capture
  - SLICE simulator
  - Waveform display
  - Polygon pushing
  - Design rule checking
  - Extract and compare

The VHF Process
(*Dielectrically Isolated*)

* **Transistors** **1.2GHz npn** **hfe = 150** **V_A = 90V**
  1.0GHz pnp **hfe = 125** **V_A = 18V**
  P-channel JFET

* **Zener diode**
* **Diffused and thin-film resistors**
* **MOS capacitors**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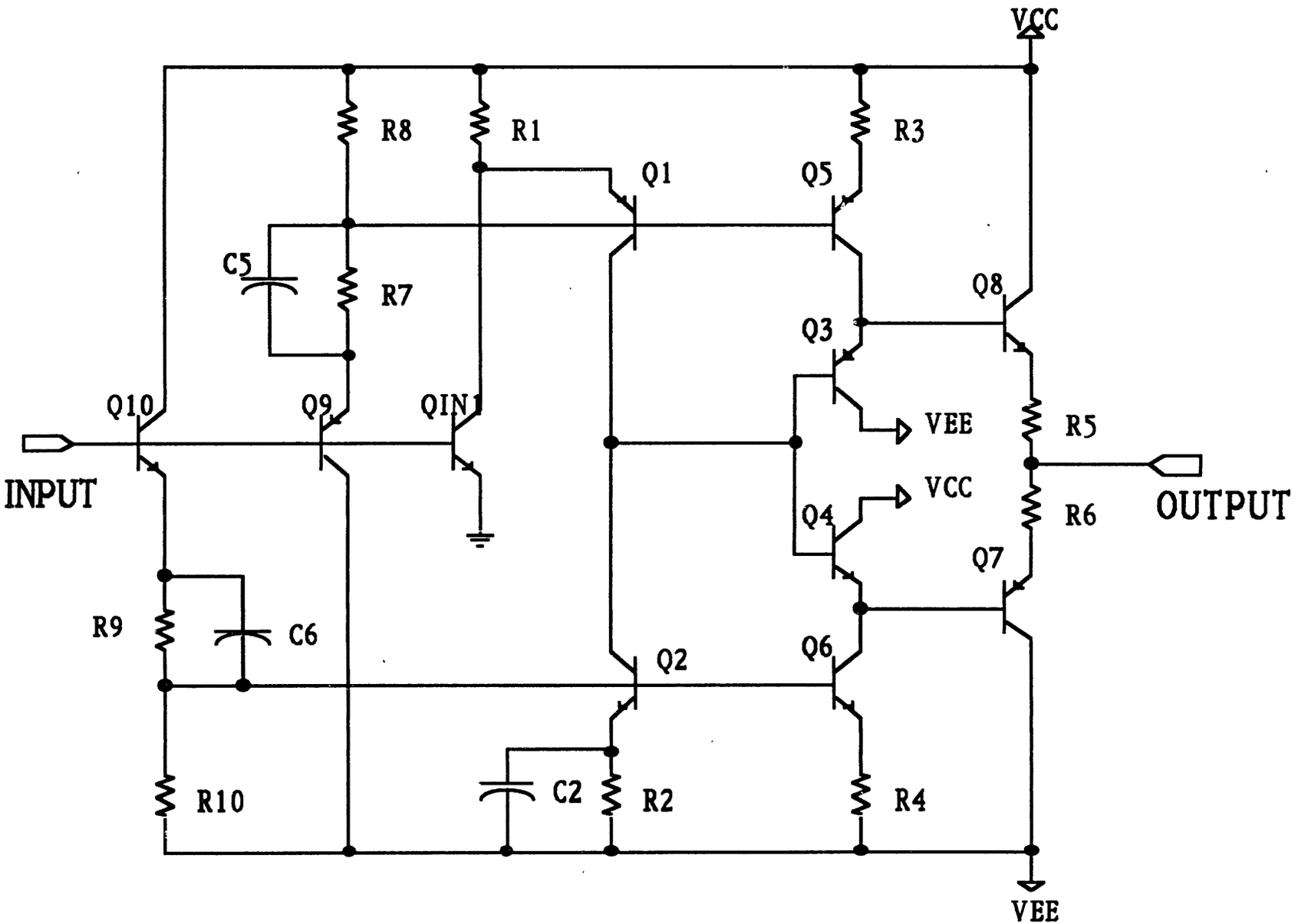
HFE ( ) = IC/IB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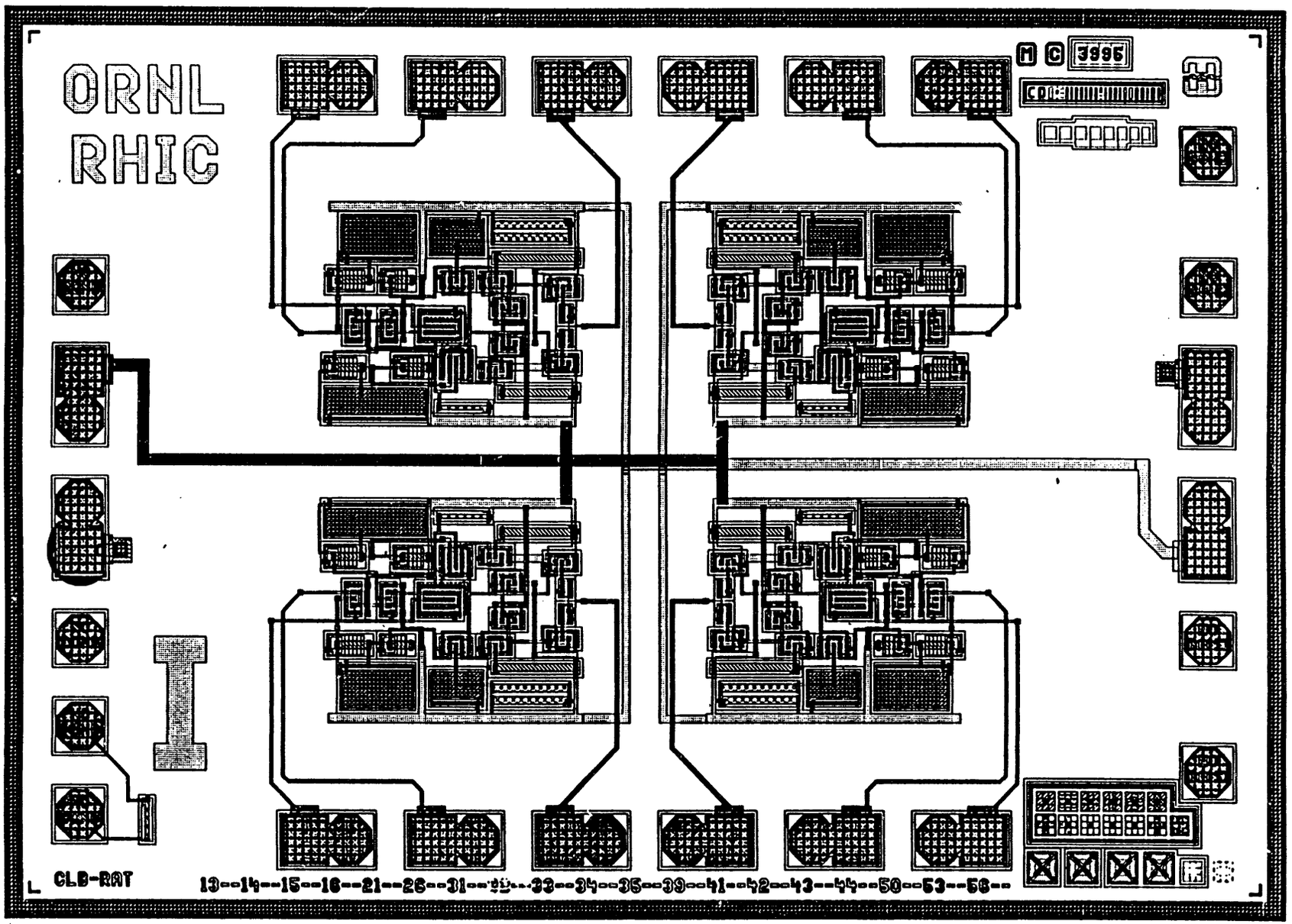
R2
R4
VEE


ORNL
RHIC
M C 3995
CLB-RAT

RHIC Bipolar Pad Quad Preamplifier Preradiation Measurements

* Noise

(50ns CR-RC)

Cd	Noise
10pF	1600e
26pF	2200e
53pF	3400e

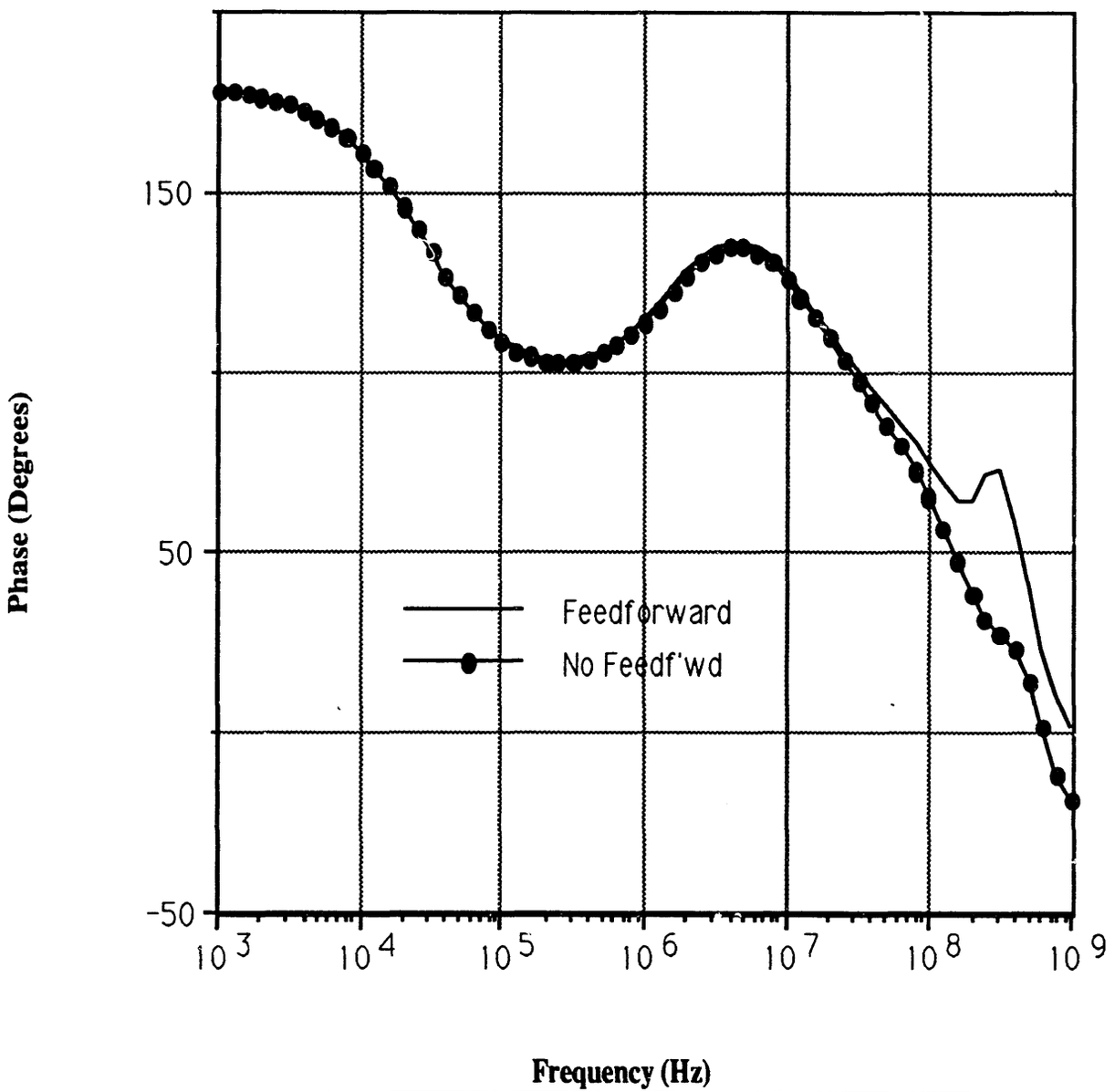
* Power Dissipation

10mW/channel

* Risetime

Cd	Tr
10pF	4.0ns
26pF	5.5ns
53pf	8.5ns

(This gives S/N=1450/1 @ 1MIP=5M electrons for 50pF pad dynamic range = 11,000:1 for 26pF pad --2V out.)


Phase (Degrees)
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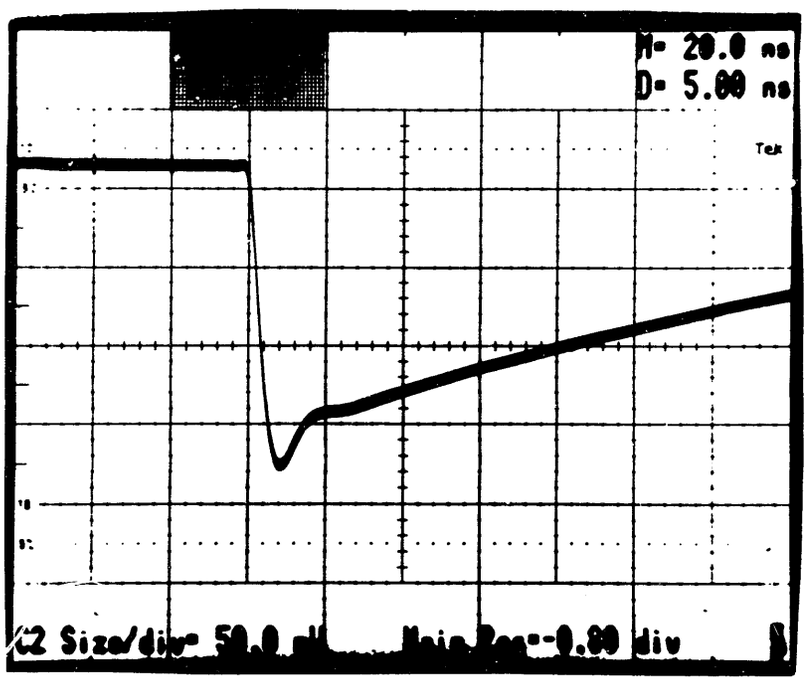
50
-50
Feedforward
No Feedf'wd
10 3
10 4
10 5
10 6
10 7
10 8
10 9
Frequency (Hz)


M= 20.0 ns
D= 5.00 ns
Tek

Predicted vs. Actual Yield

* **Quad die yield based on DC parameters for 10 wafers -**

  61%

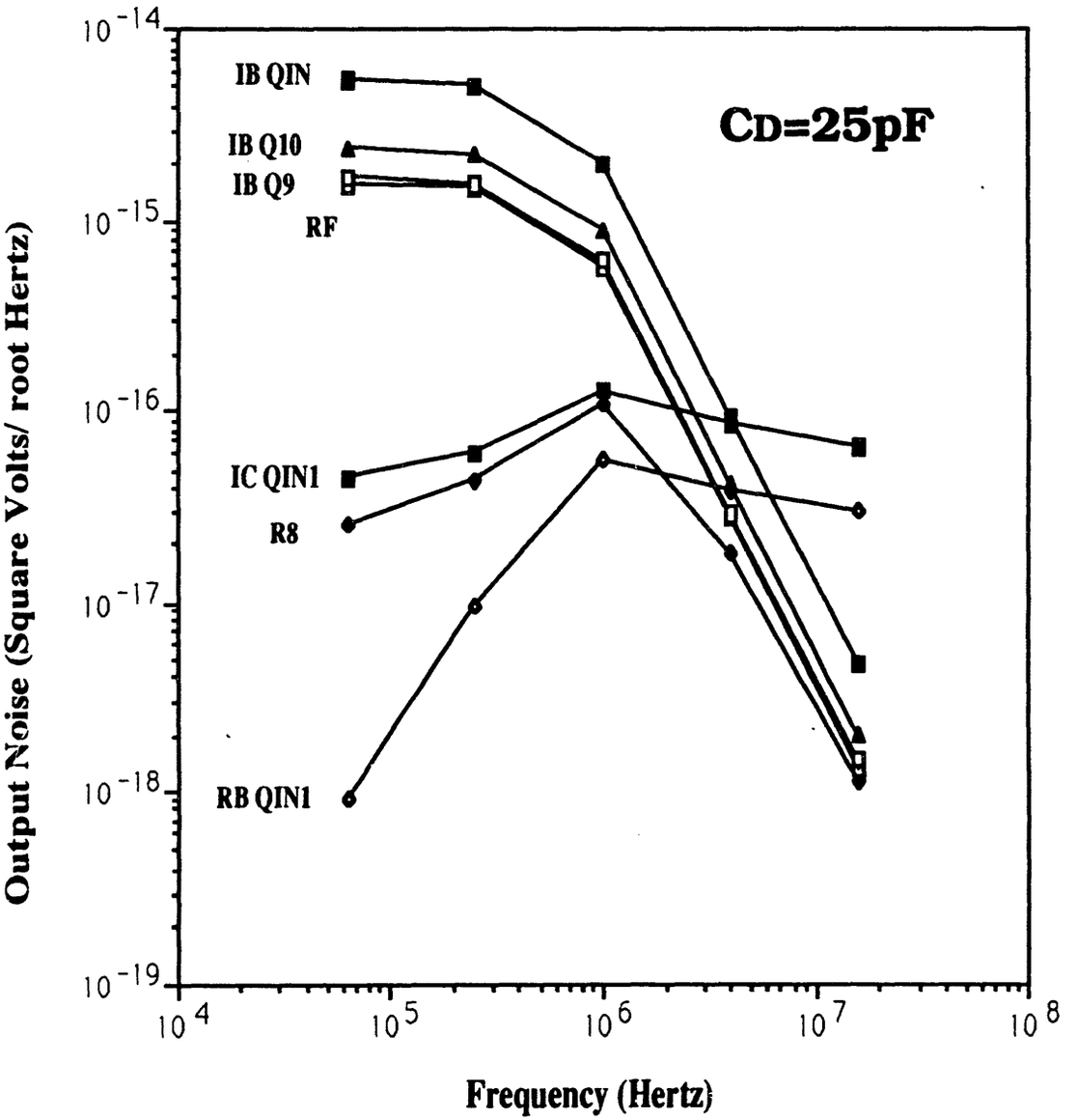
* **Quad die yield on 8 good wafers -**

  77%

* **Predicted by FASTRACK for single die-**

  78%

Noise of Various Sources vs. Frequency



We Attempted To Address Real System Issues

* **Power supply rejection *(<100KHz)***

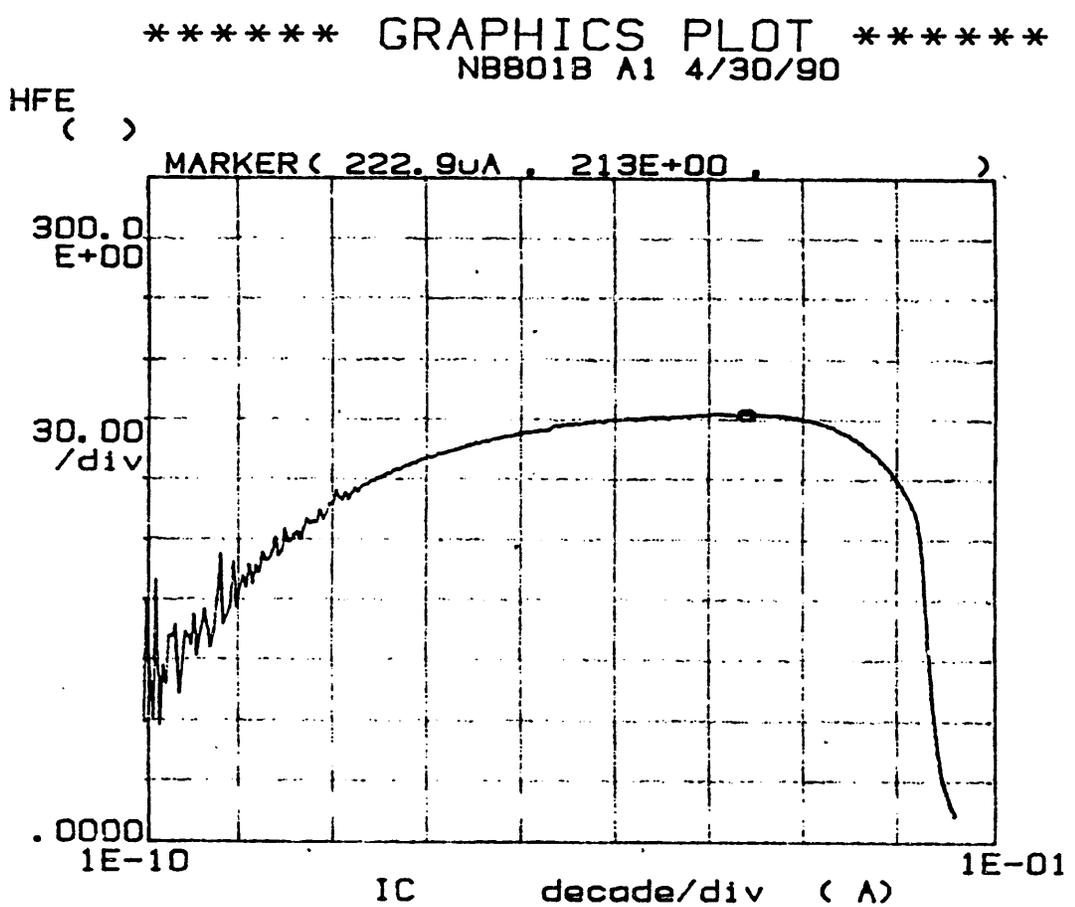
  Measured **+ *supply* - 17dB**

  - *supply* - 24dB

* **Channel-channel coupling *(Pulse measurement)***

  Measured **-30dB**

* **Short-circuit protection**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NB8018 A1 4/30/90
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.0000
1E-10
1E-01
IC decade/div (A)

HFE ( ) = IC/IB

RHIC Bipolar Pad Quad Preamplifier

Radiation Measurements Comparison

(1.25MRad)

*** Noise**

(50ns CR-RC)

Cd	Pre	Post
10pF	1500e	1570e
26pF	2200e	------
53pF	3500e	3550e

***Slew-Rate**

Pre	Post
150V/μs	150V/μs

*** Power Dissipation**

Pre	Post
10mW/ch.	9.25mW/ch.

*** Risetime**

Cd	Pre	Post
10pF	4ns	4ns
26pF	6ns	6ns
53pf	9ns	9ns

In Summary.....

* The beta test was successful
* The process appears to be useful to some level of radiation exposure
* The topology chosen worked as expected
* Some real issues were addressed

DATE
FILMED
12/19/91