CONF-890518--2

UCRL--100692

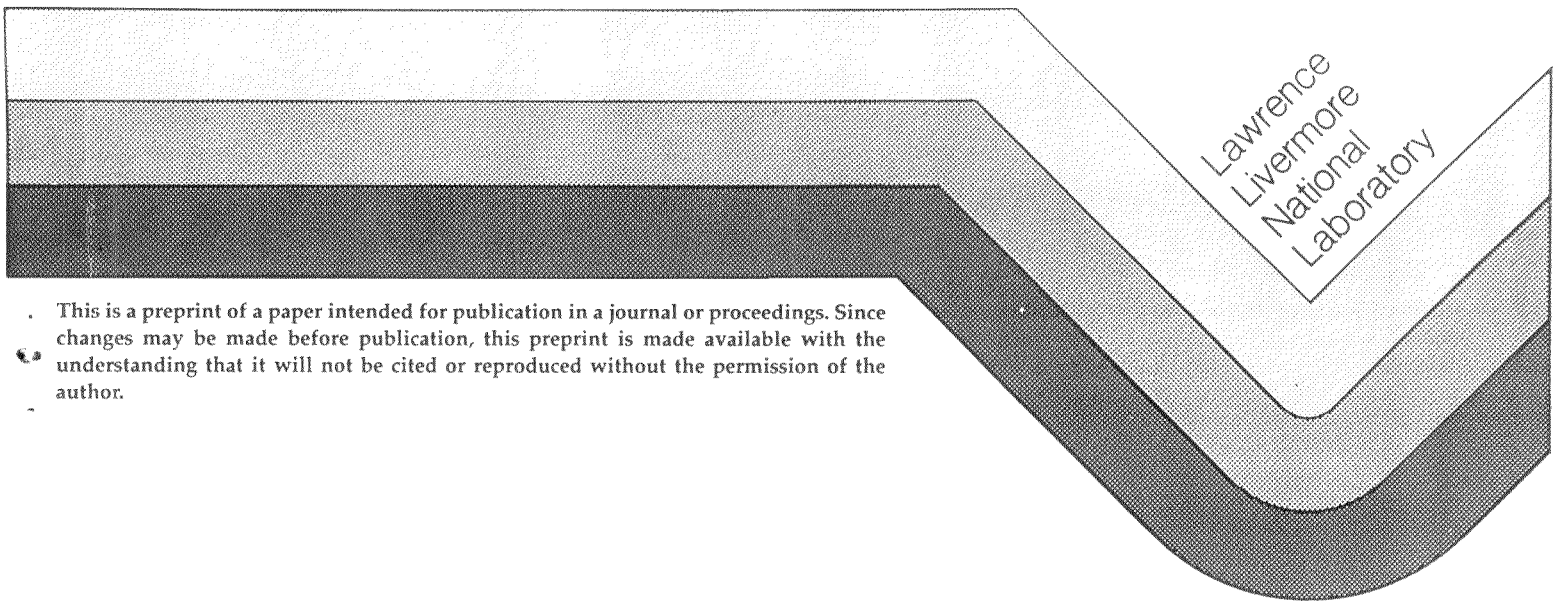
DE89 011632

EMBEDDED CONDUCTORS BY ELECTROCHEMICAL PLANARIZATION

Robert J. Contolini
Anthony F. Bernhardt
David B. Tuckerman

This paper was prepared for submittal to
Electrochemical Society
Los Angeles, CA
May 7, 1989

April 1989



EMBEDDED CONDUCTORS BY ELECTROCHEMICAL PLANARIZATION

Robert J. Contolini, Anthony F. Bernhardt,
and David B. Tuckerman

Lawrence Livermore National Laboratory
P.O. Box 808, Livermore, CA 94550

Abstract

An electrochemical process is described for planarization of metal interconnect layers on integrated circuits and multichip modules. Electroplating is used to deposit metal over a patterned SiO_2 dielectric, followed by electropolishing to remove excess metal. Electropolishing simultaneously smooths and further flattens the surface. The process yields a planar surface with conductors embedded in the etched regions of the dielectric. It is shown that pulsed plating is superior to galvanostatic plating in this application.

Introduction

Planarization processes are becoming necessary components of modern multilevel interconnection schemes. Examples of planarization techniques intended for integrated circuits (IC's) include: oxide reflow (1), spin-on dielectrics (2,3), plasma etchback (4), and metal reflow techniques (5). Modern multichip modules and wafer-scale circuits also require planarization for multilevel interconnection of high speed VLSI/ULSI computer chips. Here the conductors must have greater cross sections (e.g., 5 μm thick by 10 μm wide) than in IC technology, in order to propagate signals long distances (≈10 cm) between chips. Some multichip module technologies achieve sufficient planarization by using a spin-on polyimide dielectric, but polyimide requires high temperature processing (≈400°C) and has high moisture retention and low thermal conductivity compared with SiO_2.

We present here a metal planarization process which uses electroplating to deposit metal over a patterned (plasma-etched) SiO_2 dielectric, followed by electropolishing to remove excess metal. This yields a planarized surface which contains conductors embedded in the etched regions of the dielectric and flush with its surface. Since the electroplating process is isotropic, the width of a trench etched into the SiO_2 will decrease at twice the plating rate. The trench closes when approximately half of the initial width of the trench has been deposited. The electropolishing process thus starts with a substantially planar, though rough, surface and removes most of the excess material, smoothing and planarizing the surface in the process.

Our process can produce planarized multilayer interconnects incorporating vertical-walled conductors, without the need for an anisotropic metal etching process or a dielectric planarization process, both of which can be complex and lengthy procedures. Although only copper is reported here, we have obtained similar results with gold, and the method should be applicable to any metal which can be electroplated and electropolished, such as silver, nickel, zinc, chromium, and others.

Experimental Techniques

75-mm and 100-mm thermally-oxidized silicon wafers were coated with 10 μm of SiO_2 deposited by low-temperature plasma-enhanced chemical vapor deposition (PECVD). The wafers were then patterned with conventional lithographic and plasma etching techniques to form 5 μm deep vertical-walled trenches having varying widths of 6 to 20 microns. A 400 Å-thick adhesion layer of Ti or Cr was sputter-deposited on the oxide followed by a 2000 Å-thick copper "seed" layer.

Copper was electroplated from a copper sulphate - sulfuric acid solution using both galvanostatic and pulsed voltage techniques. Average current densities of from 10 to 50 mA/cm^2 gave rates from 0.1 to 1 μm/min in a single-wafer high-speed "flow" plating system (6) shown in figure 1. The top of the inner tube was capped with a metal anode screen approximately 0.5 cm from the front surface of the plating wafer. The solution had a flow rate of between 40 to 80 liters/min through a 3.5" diameter orifice and overflowed into the larger containment cylinder. For both the galvanostatic and pulsed plating the deposition uniformity was ± 3% across a 100 mm wafer.

The electroplated copper had a resistivity of 1.8 μΩ-cm, as measured with a 4-point probe. (Copper bulk resistivity at room temperature is 1.7 μΩ-cm).

The excess metal was then removed at rates from 0.25 to 1.0 μm/min by constant-potential electropolishing in a phosphoric acid solution. Several variations on the design of the electropolishing cell were tried, including designs similar to those of Peck and Nakahara (7) and Sedahmed *et al* (8). Best results were achieved when the copper anode plate and cathode (sample) were vertical and facing each other with very little solution movement. A calomel reference electrode was suspended between a copper cathode plate and the wafer anode.

Figure 2 shows the current-voltage curve during a voltage scan from 0 to 4 volts (vs. calomel electrode) of a copper electropolishing cell. Although polishing occurs between 1.2 volts and 4 volts, excessive oxygen bubbling from the anode sample above 2 volts precludes higher voltage electropolishing. Approximately 1.5 volts was chosen as optimum for copper electropolishing.

Electropolishing was terminated when the copper first began to clear to prevent rapid overetching of the embedded conductors. The maximum copper thickness remaining on most samples was 0.25 μm. We normally removed this residual metal by ion milling or sputter etching.

Results and Discussion

At rates of copper deposition from 0.25 to 1.0 μm/min, both galvanostatic and pulsed plating conditions resulted in embedded lines having a 2 - 3 μm deep cleft in the top surface. However, subsequent electropolishing reduces this depression to less than 0.5 μm, which is sufficient flatness for building up additional circuit layers on top of these buried conductors.

Galvanostatic plating causes voids to be trapped in the center of the plated trench. In figure 3a, 6 μm wide trenches have been plated at 0.55 μm/min to a depth of 5.5 μm. 2 - 3 μm voids are observed near the center of the line and the cleft is also apparent. The void creation process is shown in figure 3b, where a void larger than 3 μm is forming in 10 μm wide trenches.

To understand the void formation process, note that metal is deposited faster at the top edges of the trench than at the bottom of the trench due to the higher (primary) current density expected at sharp edges. Also, since the thickness of the diffusion layer is larger than the pattern dimensions, the copper ion density is depleted in the trench bottom and sides compared to the edges and top surface. At lower plating rates and hence lower current densities the latter effect is not as pronounced. For example, 5 μm trenches plated at 0.3 μm/min have voids less than 0.5 μm in diameter, as shown in figure 3c. Similarly, figure 3d shows a 10 μm wide trench almost completely filled without incipient voids after a 6 μm deposit of copper.

One well-known means of reducing the thickness of the diffusion layer is by use of pulsed plating techniques (9,10,11). In particular, pulsed voltage plating techniques have been shown to provide increased "throwing power" (the ability to plate at the same rate in protrusions as in crevices) (12). Figure 4 is the pulsed voltage plating analog of figures 3a and c: the same 6 μm trench has been pulsed voltage plated (1 ms on/ 1 ms off) at 0.67 μm/min. The void is now absent, even though the deposition rate is significantly higher than it was in the dc case.

Electropolishing the plated metal layer resulted in a mirror-like finish even if large metal crystals covered the surface. The copper was electropolished at 0.25 μm/min at 1.5 volts (vs. calomel electrode). Figures 5a and b show the results of electropolishing 8.5 μm thick copper down to less than 0.25 μm thick in the field. The resulting embedded conductors of 6 μm and 10 μm widths (5 μm deep) are flat and their top surfaces are even with the top surface of the dielectric.

Figure 6a shows a copper transmission line embedded in oxide after completion of electroplating and electropolishing. Figure 6b is a schematic of a cross section through the same structure. The copper conductor is level with the SiO_2 along its length. Note that the via at the end of the line has also been filled.

Conclusion

We have demonstrated a new electrochemical planarization process for multilevel interconnection using electroplating and electropolishing of the metal level. Fully planar multilevel structures can be fabricated using this process; no dielectric planarization or anisotropic metal etch is required. 5 μm thick, 6 and 10 μm wide metal transmission lines embedded in SiO_2 were produced with good dimensional uniformity over a 100-mm wafer. We have also shown that pulsed voltage copper plating offers advantages over galvanostatic plating by preventing formation of voids in the conductors.

Acknowledgements

This work was performed under the auspices of the U. S. Department of Energy by Lawrence Livermore National Laboratory under Contract No. W-7405-Eng-48. This work was supported in part by the VHSIC Program of the Department of Defense.

References

1. P. B. Johnson and P. Sethna, Semiconductor International, Oct. 1987, p.80

2. A. Endo and T. Yada, J. Electrochem. Soc., 132, p. 155, (1985)

3. J. K. Chu, J. S. Multani, S. K. Mittal, J. T. Orton, and R. Jecmen, 1986 V-MIC Conf., 1986

4. Paul E. Riley and Egil D. Castel, Proc. Electrochem. Soc. 1987, 87-4, p. 194, (Proc. Symp. Multilevel Met., Interconnect., Contact Technol.,1986)

5. D. B. Tuckerman and A. H. Weisberg, IEEE Elec. Dev. Lett., EDL-7, p. 1, (1986)

6. Edward S. Figuli, Western Electric Engineer, 18, p. 18, (1974)

7. W. F. Peck, Jr., and S. Nakahara, Metallography, 11, p. 347, (1978)

8. G. H. Sedahmed, S. S. Iskander, I. A. S., Masnour, and M. A. Fawzy, Surface Technology, 11, p. 67, (1980)

9. Jean-Claude Puippe and Frank Leaman, eds., Theory and Practice of Pulse Plating, American Electroplaters and Surface Finishers Society, 1986

10. D. T. Chin, J. Electrochem. Soc., 130, p. 1657, (1983)

11. D. L. Rehrig, H. Leidheiser, and M. R. Notis, Plat. Surf. Finish., Dec., 1977, p. 40

12. U. Landau, Seventh Workshop on Electrochemical Engineering, Case Western Reserve University, 1988

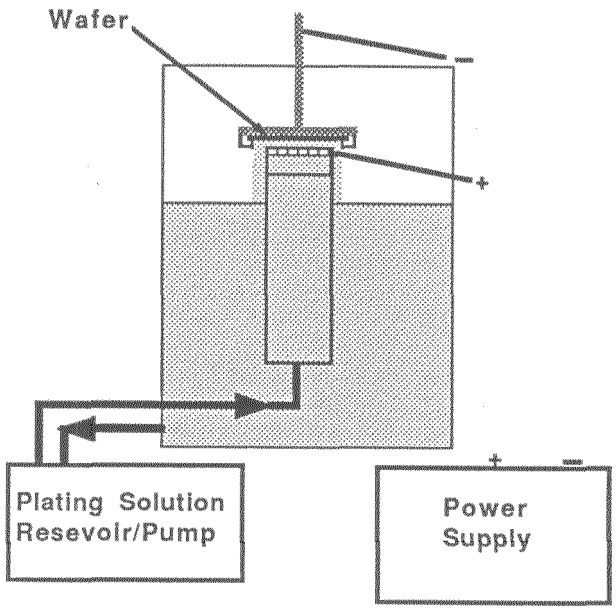


Figure 1: Schematic diagram of the flow plating apparatus. The plating solution is forced up through a 3.5" diameter glass tube, flows radially across the wafer and spills into a larger vessel which returns the electrolyte to the pump. A copper screen stretched across the top of the tube forms the anode while the wafer forms the cathode.

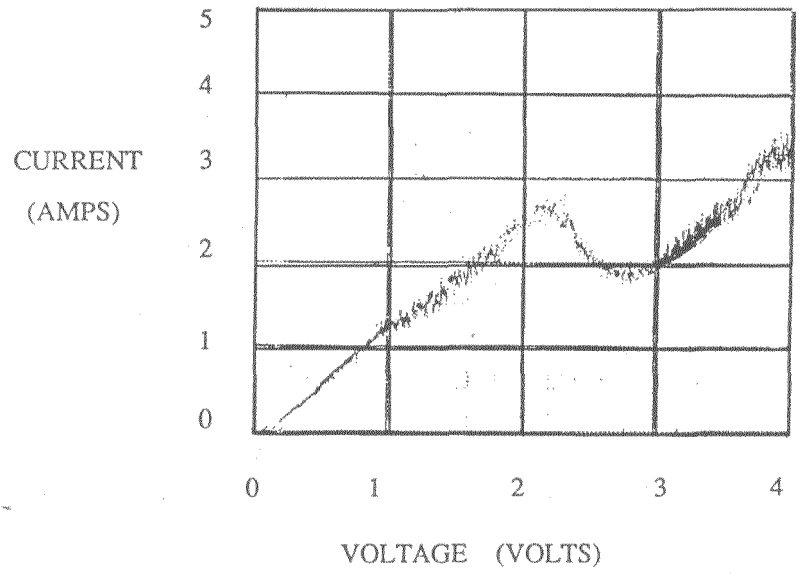
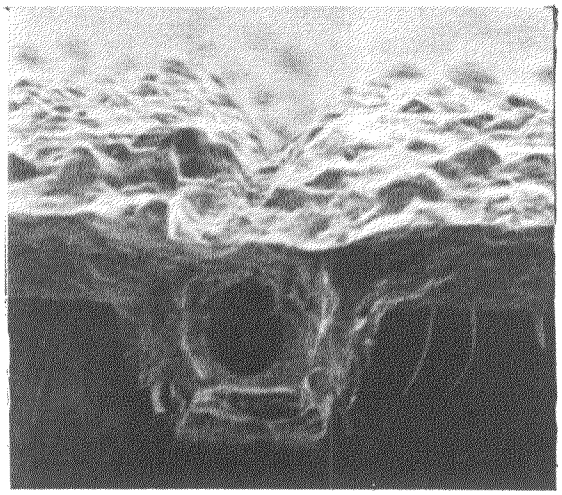
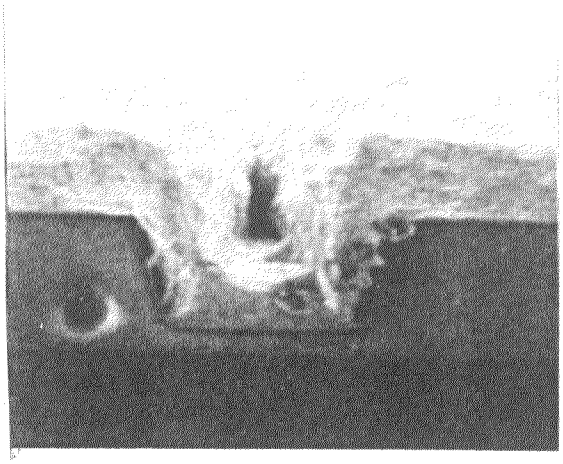


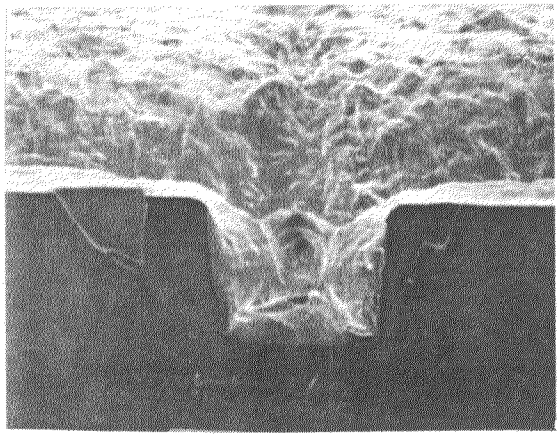
Figure 2: Current plotted against voltage for copper polishing in phosphoric acid. Above 2 volts oxygen is evolved at the anode.



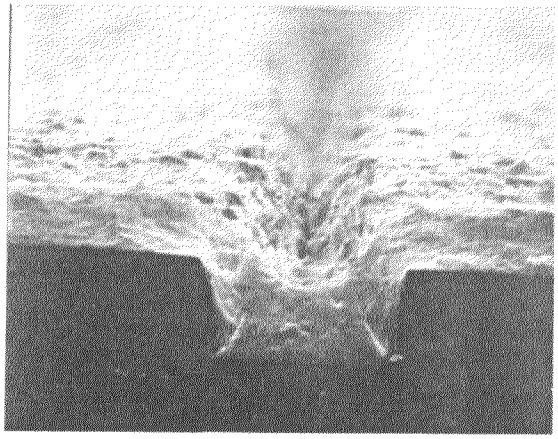
(a)



(b)



(c)



(d)

Figure 3: SEM's of cross-sectioned wafers after galvanostatic plating showing void and cleft formation. a) plating rate of 0.55 μm/min on a 6 μm wide trench. b) plating rate of 0.55 μm/min on a 10 μm wide trench. c) plating rate of 0.3 μm/min on a 5 μm wide trench. d) plating rate of 0.55 μm/min on a 10 μm wide trench.

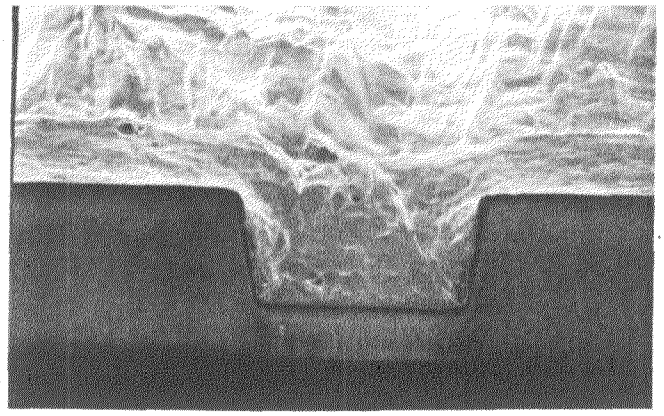
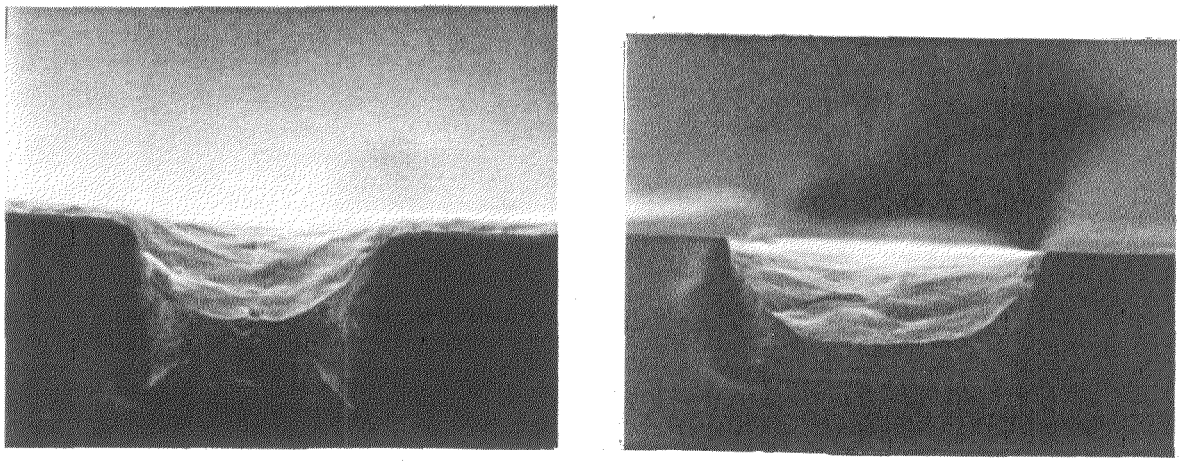


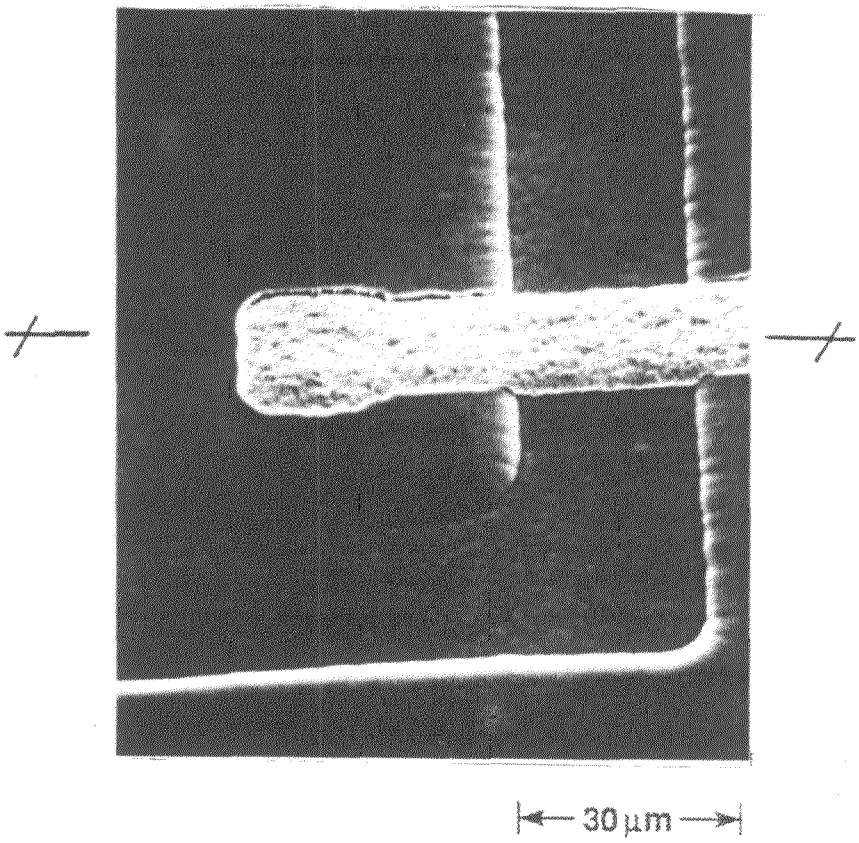
Figure 4: SEM of a cross-sectioned wafer after pulsed voltage plating over a 6 μm wide trench at 0.67 μm/min. No voids are formed in this process.



(a) (b)

Figure 5: SEM's of cross-sectioned wafers after plating and electropolishing. An initial copper depth of 8.5 microns was polished at 0.25 micron/min and 1.5 volt. Residual copper depth across the wafer was less than 0.25 micron. a) 6 micron wide embedded conductor. b) 10 micron wide embedded conductor.

(a)



(b)

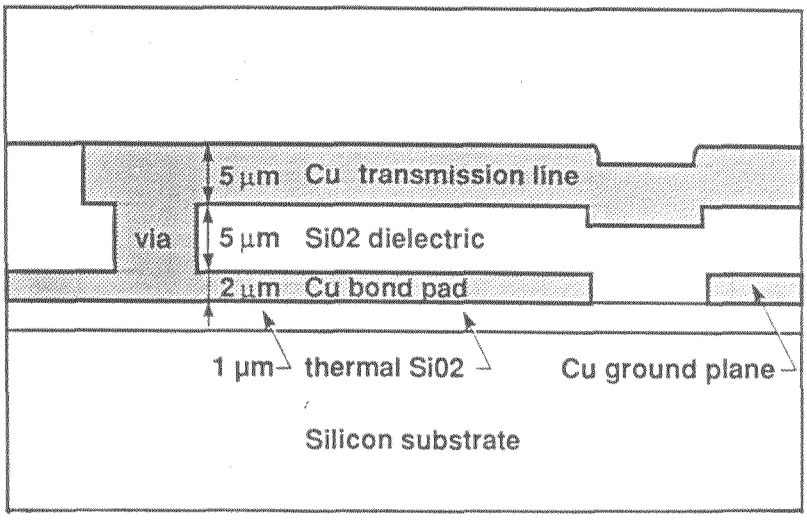


Figure 6: a) Top view SEM of a planarized conductor. b) Schematic cross-section of the structure shown in a). Both the trench and the via below its termination are filled with copper in the process.