GaN DEVICE PROCESSING

S.J. Pearton [1], F. Ren[2], J.C. Zolper[3] and R.J. Shul[4]
[1]Department of Materials Science and Engineering, University of Florida, Gainesville, FL
[2]Bell Laboratories, Lucent Technologies, Murray Hill, NJ
[3]Office of Naval Research, Arlington, VA
[4]Sandia National Laboratories, Albuquerque, NM

ABSTRACT

Recent progress in the development of dry and wet etching techniques, implant doping and isolation, thermal processing, gate insulator technology and high reliability contacts is reviewed. Etch selectivities up to 10 for InN over AlN are possible in Inductively Coupled Plasmas using a Cl_2/Ar chemistry, but in general selectivities for each binary nitride relative to each other are low (≤2) because of the high ion energies needed to initiate etching. Improved n-type ohmic contact resistances are obtained by selective area Si^+ implantation followed by very high temperature (>1300°C) anneals in which the thermal budget is minimized and AlN encapsulation prevents GaN surface decomposition. Implant isolation is effective in GaN, AlGaN and AlInN, but marginal in InGaN. Candidate gate insulators for GaN include AlN, AlON and Ga(Gd)O_X, but interface state densities are still to high to realize state-of-the-art MIS devices.

INTRODUCTION

Current GaN-based device technologies include light-emitting diodes (LEDs), laser diodes and UV detectors on the photonic side and microwave power and ultra-high power switches on the electronics side.[1] The LED technology is by now relatively mature, with lifetimes of blue and green emitters apparently determined mostly by light-induced degradation of the polymer package that encapsulates the devices.[2] The main trends in this technology appear to be optimization of optical output efficiency and solving the polymer package degradation issue. For the laser diodes one of the main lifetime limiters was p-ohmic metal migration along dislocations to short out the GaN p-contact layer by spiking all the way to the n-side of the junction.[3,4] This is exacerbated by the generally high specific contact resistance (R_C) of the p-ohmic contact and the associated heating of this area during device operation. The advent of lower threshold devices and the dislocation-free GaN overgrowth of SiO_2 masked regions has allowed achievement of laser lifetimes over 10,000 hours.[5] Facet formation on the laser has been achieved by dry etching, cleaving, polishing and selective/crystallographic growth. In structures grown on Al_2O_3 both contacts must be made on the top of the device and hence dry etching is necessary to expose the n-side of the junction. Fabrication of UV detectors is relatively straightforward and the main issue seems to be one of improving material purity and quality.

For electronic devices for microwave power applications, the main process improvements are needed in the areas of low R_C n-ohmic contacts (the requirements are more stringent than for photonic devices, with $R_C \leq 10^{-7}\Omega cm^{-2}$ being desirable), stable and reproducible Schottky contacts, and low damage dry etching that maintains surface stoichiometry. For the proposed high power switches (capable of 25 kA with 3kV voltage stand-off) there are a number of possible device structures, including thyristors and several types of power MOSFET. A schematic of the latter is shown in Figure 1. In this case, critical technologies include high

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implant activation efficiency, gate insulator, trench etching for capacitor formation and high temperature/high current stable ohmic contacts.

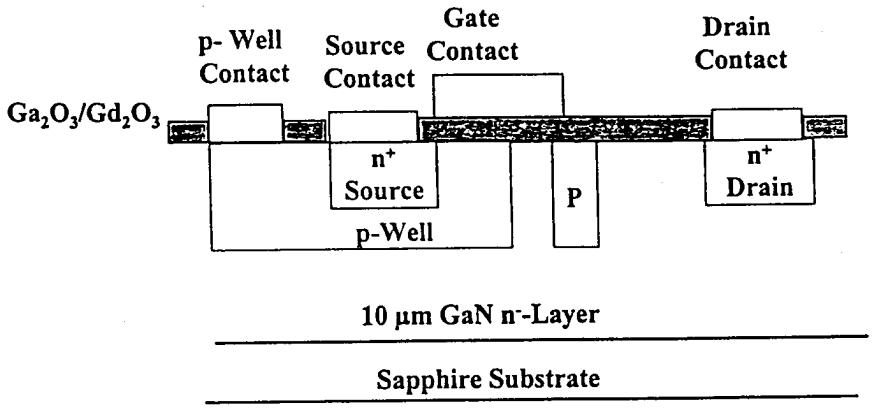

Figure 1. Schematic of an ultra high breakdown voltage GaN power MOSFET.

DRY ETCHING

It is now well-established that high density plasma techniques such as Electron Cyclotron Resonance (ECR) and Inductively Coupled Plasma (ICP) produce much higher etch rates than conventional Reactive Ion Etching (RIE) or low pressure (0.3 mTorr) Reactive Beam Etching (RIBE).[6-8] Figure 2 shows GaN etch rates in Cl_2/Ar-based chemistries as a function of dc chuck bias (or grid acceleration voltage in the case of RIBE) for these four techniques. ECR and ICP produce faster rates at equivalent ion energies because of their higher ion flux and degree of dissociation. Figure 3 shows etch yields calculated from this data - the higher values for the ECR and ICP reactors indicates there is also an enhanced chemical component in these systems, in addition to the higher ion flux. This originates from the enhanced reaction $Cl_2 + e \rightarrow 2\ Cl$, leading to higher efficiency of atomic neutral creation.

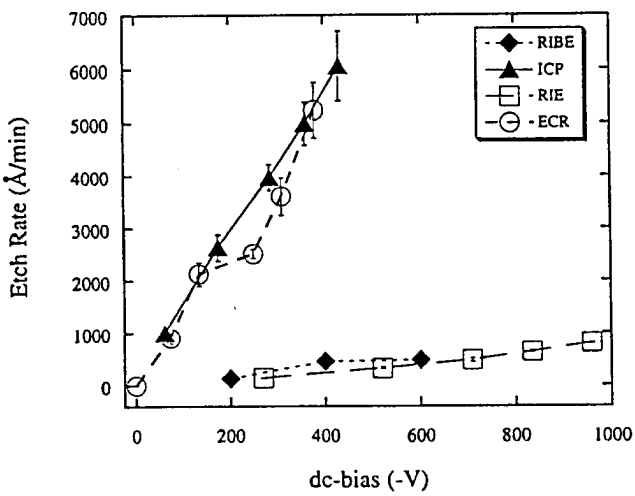

Figure 2. Dry etch rate of GaN in Cl_2/Ar-based plasmas created in four different types of reactor, as a function of dc chuck bias.

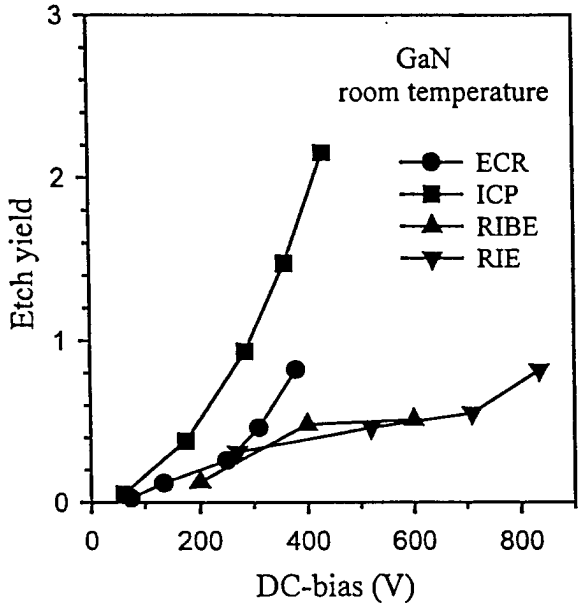

Figure 3. Etch yield of GaN in Cl_2/Ar-based plasma created in four different types of reactor, as a function of dc chuck bias.

Etching selectivity for one material over another occurs most often when there is formation of an involatile etch product upon exposure of one of the material to the plasma, i.e. presence of a strong chemical reaction. Due to the requirement for a substantial physical component in III-nitride etching due to the strong bonds in these materials, selectivities are generally not that high. In electronic device structures there will be a need to selectively etch InN-based ohmic contact layers from underlying binary or ternary nitride active channel layers. Figure 4 shows that maximum selectivities of 3-10 for InN over the nitrides can be achieved in ICP Cl_2/Ar plasmas as source power is increased. Shul et al.[9] performed a detailed study of etch selectivity of GaN with respect to AlN and InN in Cl_2 and BCl_3 plasmas with addition of Ar or SF_6 and found maximum values typically of 2-4.

Since the nitride etching is generally ion-driven, sidewall anisotropy is generally excellent as long as mask erosion is avoided. As an example, Figure 5 shows a feature etched into InN in an ICP 25Cl_2/Ar, 2 mTorr 500W source power, 250W rf chuck power discharge. The SiN_X mask is still in place. Note the excellent verticality of the sidewalls, although striations are present and these will lead to scattering losses if present on a laser facet.[11]

To this point there has been no definitive identification of the etch products of any of the nitrides. Figure 6 shows a mass spectrum of an ICP Cl_2/Ar plasma during etching of a GaN wafer. There are peaks due to H_2O, N_2 (from residual atmosphere in the gas lines and chamber), plasma lines from Cl, Cl_2 and Ar, and an identifiable etch product peak due to $GaCl_2$. This is the primary fragment of $GaCl_3$ and is known to dominate the cracking pattern of the latter.[12] We cannot definitively identify N_2 as the etch product because of its presence in the spectrum even when no wafer is loaded in the chamber. Lee et al.[13] have recently reported detection of N_2 emission lines in optical emission spectra obtained during GaN etching in a Cl_2 plasma. Therefore the plasma etch reaction contains at least the following component:

$$2GaN + 3Cl_2 \rightarrow 2GaCl_3 + N_2$$

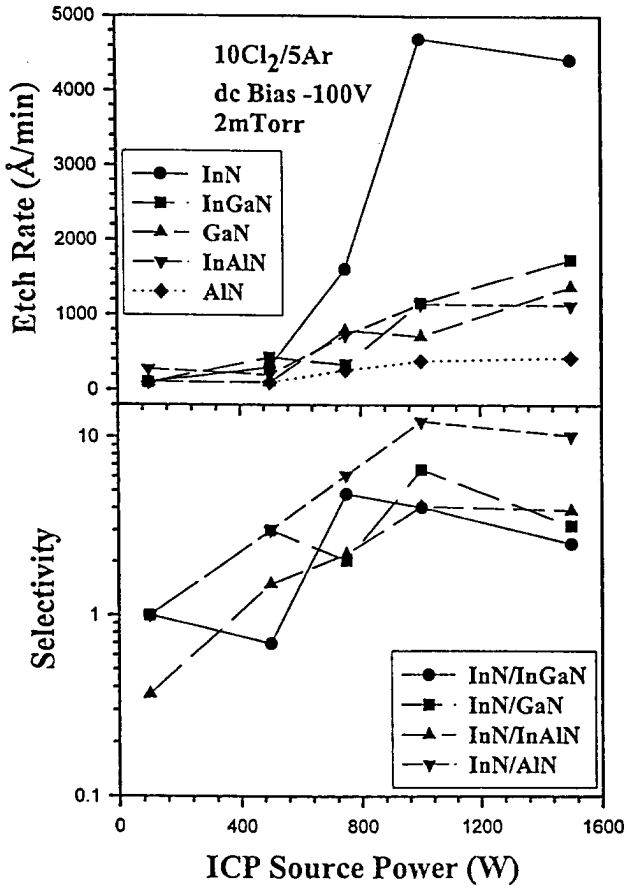

Figure 4. Etch rates (top) and etch selectivities (bottom) for nitrides in Cl_2/Ar, -100V dc, 2 mTorr plasmas, as a function of ICP source power.

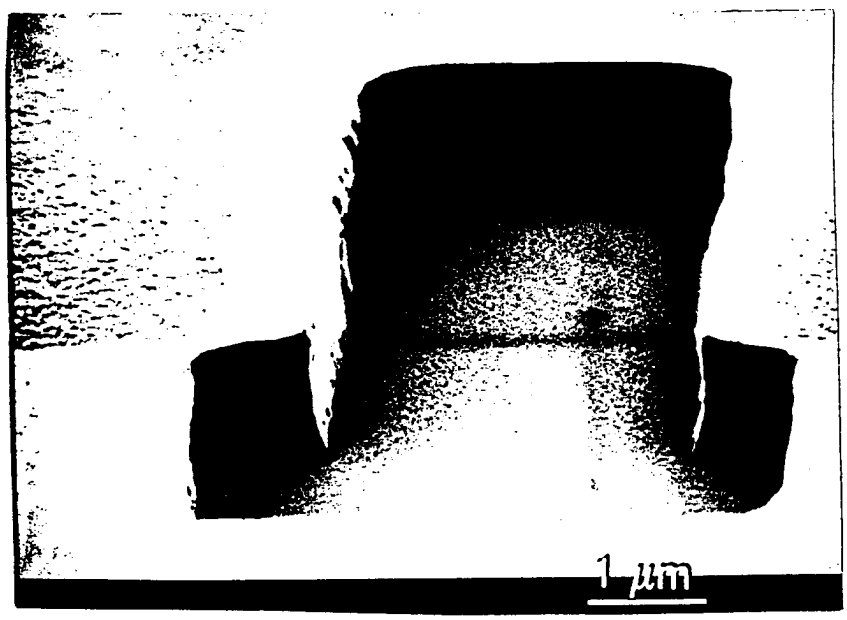

Figure 5. SEM micrograph of a feature etched into InN using an ICP Cl_2/Ar plasma. The SiN_x mask is still in place.

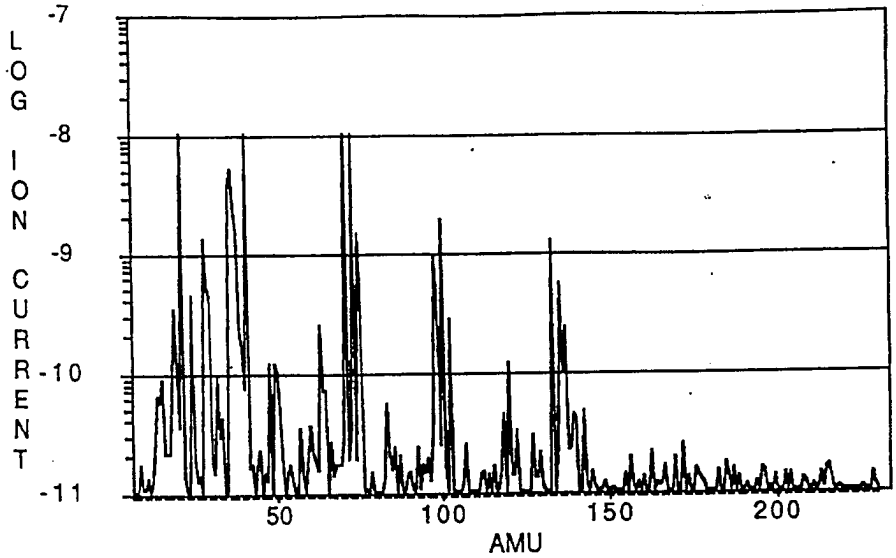

Figure 6. Mass spectrum obtained during ICP Cl_2/Ar etching of GaN.

The issue of sidewall smoothness on laser facets has also received attention recently. Ren et al.[14] reported a number of different methods for minimizing sidewall roughness on dry etched GaN features formed using high density plasmas. In many instances striations on dry etched mesas is a result of roughness in the initial photoresist mask employed, and this roughness is transferred sequentially to the dielectric mask and then to the GaN. Combined with mask erosion during etching, this can produce sidewalls of the type shown in Figure 7. Ren et al. reported that flood exposure of the resists, optimization of the bake temperature, choice of plasma chemistry and ion flux/energy for patterning the dielectric mask all influence the final GaN sidewall morphology. An optimized process leads to the much smoother sidewalls of Figure 8.

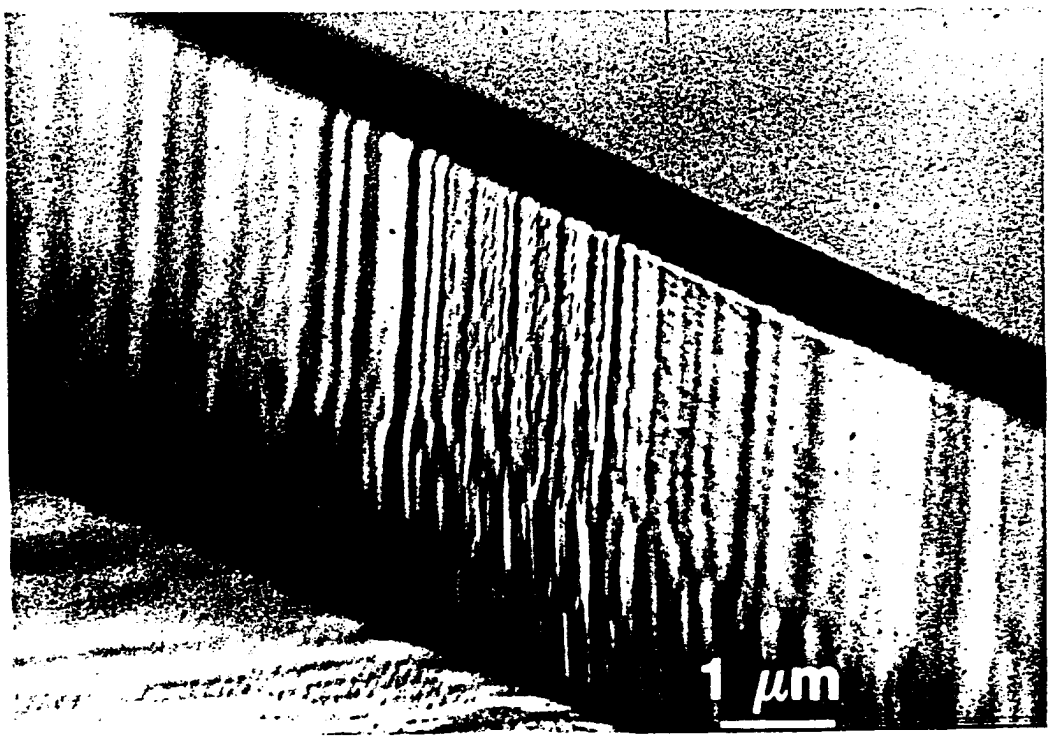

Figure 7. SEM micrograph of GaN feature sidewall when mask erosion occurs during dry etching and critical photoresist sidewall smoothness is not optimized.

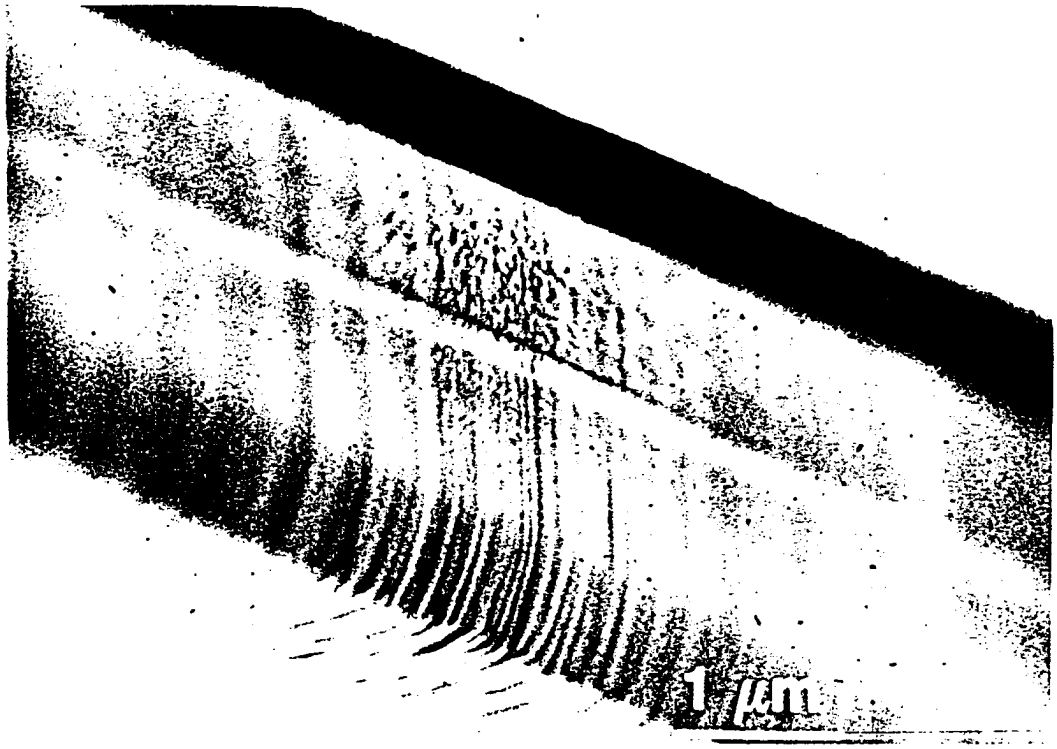

Figure 8. SEM micrograph of GaN feature sidewall when mask erosion is minimized and initial photoresist sidewall smoothness is optimized.

WET ETCHING

Only molten salts such as KOH or NaOH at temperatures above ~250°C have been found to etch GaN at practical rates, and the difficulty of handling these mixtures and the inability to find masks that will hold up to them has limited the application of wet etching in GaN device technology. We have found that AlN and Al-rich alloys can be wet etched in KOH at temperatures of 50-100°C.[15] The Adesida group has recently published several reports on photochemical etching of n-GaN using 365 nm illumination of KOH solutions near room temperature.[16] Rates of 3,000Å·min^{-1} were obtained for light intensities of 50mW/cm^2, and the etch reaction was assumed to be:

$$2GaN + 6h^+ \rightarrow 2Ga^{3+} + N_2 \uparrow$$

The etching was generally diffusion-limited, with somewhat rough surfaces. Intrinsic and p-GaN do not etch under these conditions, and undercut encroachment occurred in some small-scale features due to light scattering and hole diffusion in the GaN itself. This process looks very promising and may be useful for several different fabrication steps in both electronic and photonic devices.

IMPLANT ACTIVATION

Pioneering work by Zolper[17] and Williams et al.[18] has shown that for high implant doses (~5x10^{15}cm^{-2}) amorphous layers will form in GaN at 25°C, and these revert to polycrystalline after annealing up to 800°C, but they do not recover their original crystalline quality even for 1100°C anneals. For lower doses (<10^{14}cm^{-2}), residual damage is detectable by

channeling even after 1100°C annealing and this may account for the generally low carrier mobilities observed in implanted material. The use of elevated temperature (200°C) implants did little to reduce accumulated damage. The basic message of this work was that higher annealing temperatures were desirable both the remove the lattice damage and improve the electrical characteristics of the implanted region.

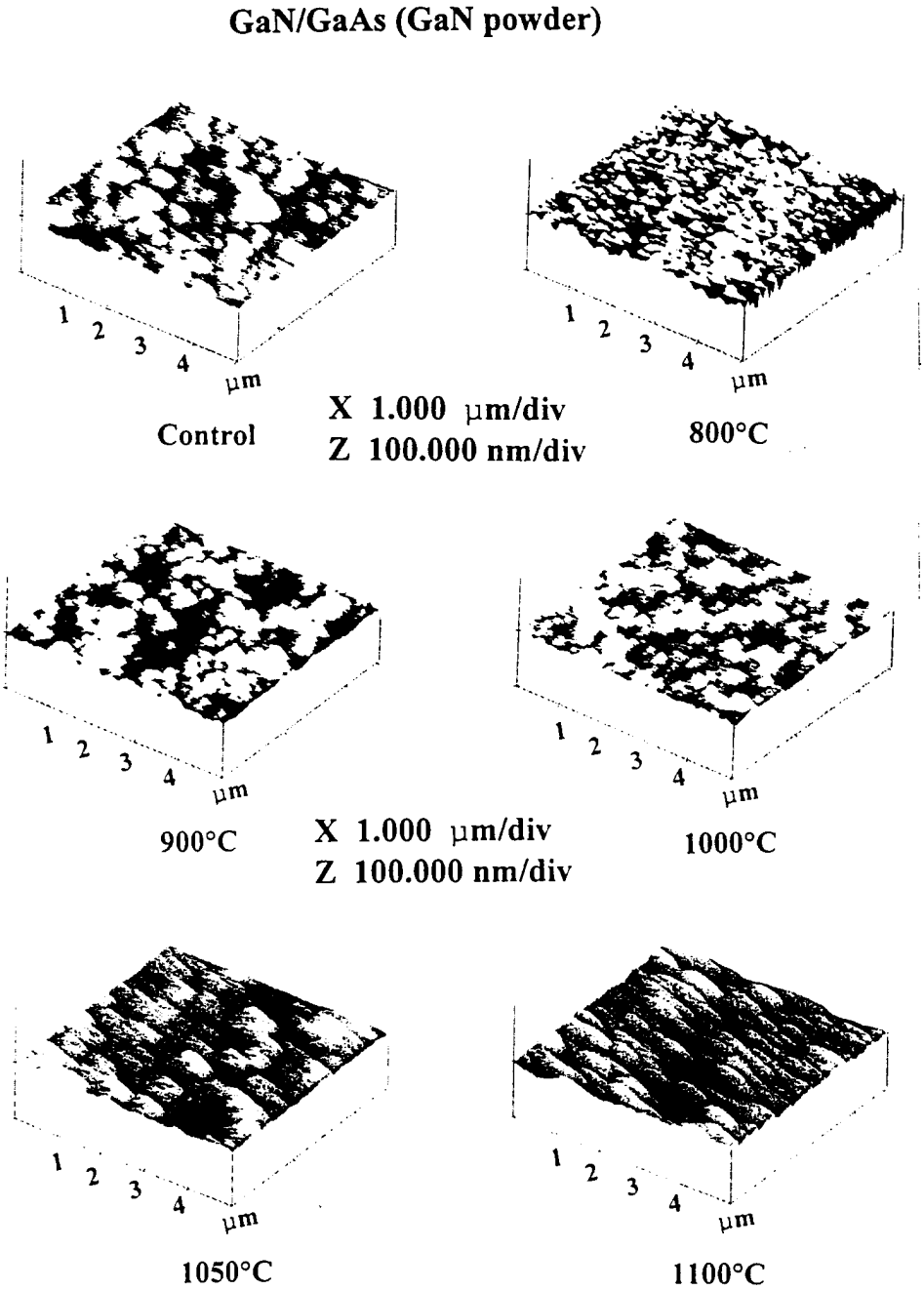

Figure 9. AFM images as a function of anneal temperature for GaN annealed with GaN powder in the susceptor reservoir.

The main problem with use of higher temperature anneals is preservation of the nitride surface. Hong et al.[19] compared use of GaN, InN and AlN powders for providing a nitrogen partial pressure within a graphite susceptor during high temperature rapid thermal annealing. Some typical atomic force microscope images of GaN after RTA at different temperatures using

GaN powder in the reservoirs are shown in Figure 9. At temperatures above ~750°C, vapor transport of In from InN powder produced In droplet formation on the surface of all nitride samples being annealed. GaN powder was shown to provide better surface protection than AlN powders for temperatures up to ~1050°C when annealing GaN and AlN samples, as shown in the surface root-mean-square (RMS) roughness data for GaN in figure 10.

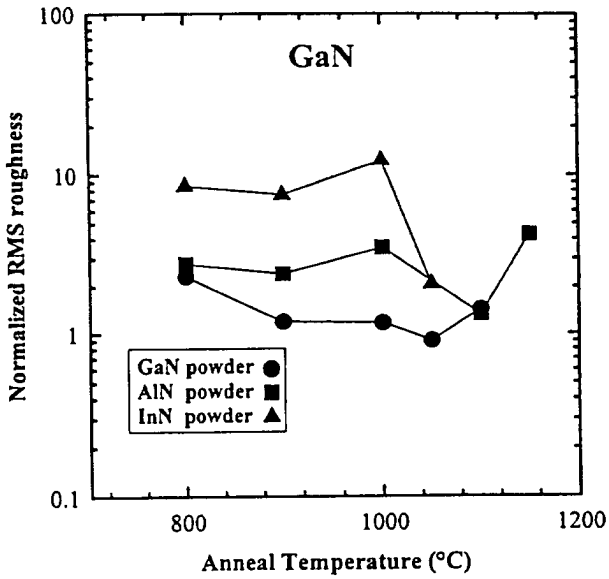

Figure 10. Normalized RMS surface roughness as a function of annealing temperature for GaN annealed with different powders in the susceptor reservoirs.

Figure 11 shows the rapid annealing times at various temperatures using GaN powder for which surface degradation is first visible by SEM. The areas above each line represent conditions under which there will be clear surface dissociation, whereas the areas below each line represent annealing conditions that will not lead to visible surface degradation. For example, for 10 s anneals under our conditions, any temperature ≥1050°C will lead to pitted GaN surfaces. Changes to the near-surface stoichiometry that affect electrical properties will occur at somewhat lower temperatures than those at which visible surface degradation is obvious (generally by 50-100°C is the rule of thumb for other III-V materials).[20] Therefore the approach of providing surface protection during annealing by placing powdered nitrides in the reservoir susceptor is not sufficient to prevent some dissociation during implant activation processes in GaN, where temperatures of 1050-1100°C are required.[21,22] A superior technique is the one reported by Zolper et al.[23] who used sputtered AlN films as encapsulants for annealing implanted GaN at ≥1100°C – the AlN can be selectively removed in KOH solutions after the annealing process. If the data in Figure 12 are replotted in Arrhenius fashion, the slopes (from admittedly a small number of points) yield approximate activation energies of 3.8 eV, 4.4 eV and 3.4 eV, respectively, for GaN, AlN and InN. These are fairly close to the values reported in ref. 24 for dissociation of nitrogen from vacuum-annealed nitrides, i.e. 3.93 eV for GaN, 4.29 eV for AlN and 3.43 eV for InN. Therefore we are confident that the changes in the surface quality for GaN and InN at least are predominantly a result of preferential dissociation of nitrogen during the RTA treatment. For AlN the equilibrium decomposition pressure is much lower than the ambient N_2 pressure in the furnace and at least some of the surface changes in morphology may be due to annealing of crystalline defects.

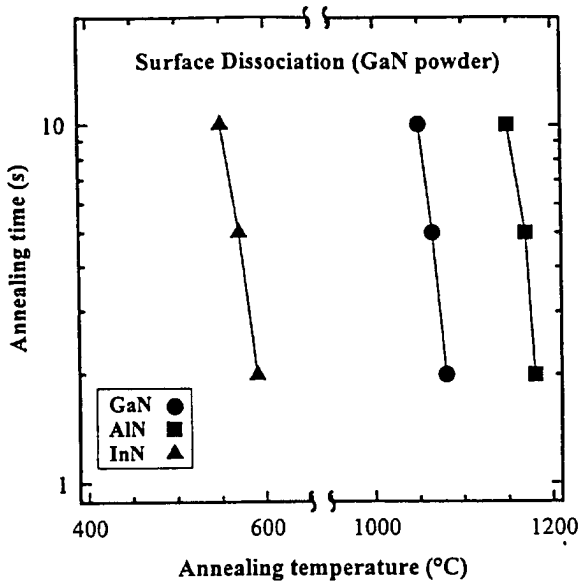

Figure 11. Time-temperature plots for the thermal stability of GaN, AlN and InN surfaces annealed with GaN powder in the susceptor reservoirs. Surface dissociation is visible for annealing conditions to the right of each plot; to the left of each line there is no surface pitting visible by SEM.

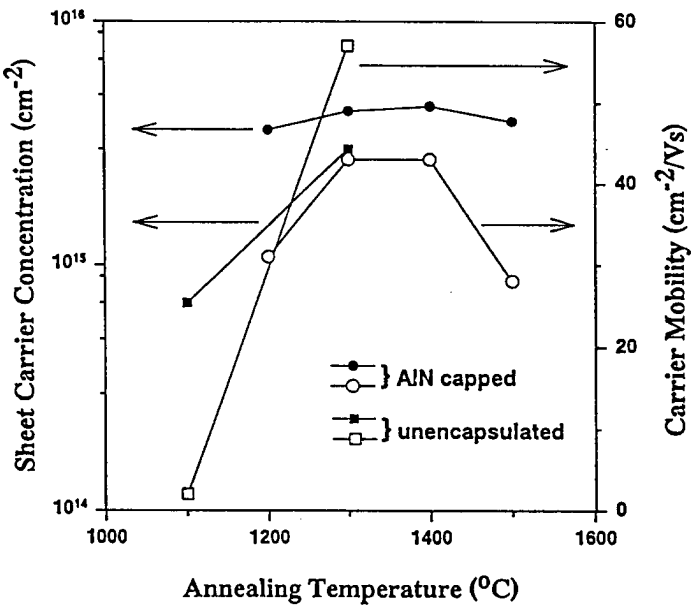

Figure 12. Sheet carrier density and electron mobility in Si^+ implanted (100keV, $5x10^{15}cm^{-2}$) GaN as a function of annealing temperature, either with or without AlN encapsulation. For unencapsulated samples, the GaN is lost by evaporation at ≥1300°C.

While the GaN powder approach works well up to ~1050°C, it clearly does not provide acceptable surface protection for higher temperatures. AlN encapsulant layers can hold up to temperatures of 1400-1500°C, and can be selectively removed by KOH etching at ~80°C after the annealing. Using this approach we have achieved activation efficiencies of ~90% for Si^+ implants (100 keV, $5x10^{15}cm^{-2}$) onto GaN, as shown in Figure 12. Note all that the mobilities

are above 40 cm^2/Vs for the anneal temperatures of ≥1300°C. The reduction in carrier density at 1500°C may be due to several factors, including Si site-switching and loss of some of the near-surface region through cap failure.

IMPLANT ISOLATION

Very effective isolation of AlGaN/GaN heterostructure field effect transistor (HFET) structures has been achieved using a combined P^+/He^+ implant process.[25] The groups of Asbeck and Lau at UCSD demonstrated that a dual energy (75/180 keV) P^+ implant (doses of $5x10^{11}$ and $2x10^{12}cm^{-2}$, respectively), followed by a 75 keV He^+ implant ($6x10^{13}cm^{-2}$) was able to produce sheet resistance of $\sim10^{12}\Omega/\square$ in AlGaN/GaN structures with 1μm thick undoped GaN buffers. The temperature dependence of the resistivity showed an activation energy of 0-71eV, consistent with past measurements of deep states induced in GaN by implant damage.[22]

OHMIC AND SCHOTTKY CONTACTS

There are still large variations in barrier heights reported by different workers for standard metals on GaN. Pt appears to produce the highest consistent values (~1.0-1.1eV) with Ti producing the lowest (0.1-0.6eV). The variability appears to result from the presence of several transport mechanisms, and to materials and process factors such as defects present in these films, the effectiveness of surface cleans prior to metal deposition, local stoichiometry variations, and variations in surface roughness which could affect uniformity of the results. For Schottky contacts P^t appeared to be stable to approximately 400°C for 1h, while PtSi was somewhat more stable (500°C 1h), and also had barrier heights of ~0.8eV.[26]

The commonly accepted ohmic contact to n-GaN is Ti/Al, which is generally annealed to produce oxide reduction on the GaN surface. Multi-level Au/Ni/Al/Ti structures appear to give wider process windows, by reducing oxidation of the Ti layer.[27] R_C values of $\leq10^{-5}\Omega cm^2$ have been produced on HFET devices using Ti/Al annealed at 900°C for 20 secs.

WSi_X contacts on n^+GaN produce R_C values $\leq 10^{-5}\Omega cm^2$ stable to annealing temperatures of ~1050°C. Reaction with the GaN is relatively limited, although β-W_2N interfacial phases are found after 800°C anneals, and this appears to be a barrier to Ga outdiffusion.[28]

The standard p-ohmic contact to GaN is NiAu, with R_C values $\geq10^{-2}\Omega cm^2$. Efforts to find a superior alternative has proved fruitless to date[29], even though strong efforts have been made on multi-component alloyed contacts where one attempts to extract one of the lattice elements, replace it with an acceptor dopant, and simultaneously reduce the "balling-up" of the metallization during this reaction. The model system for this type of contact is AuGeNi/n-GaAs. A promising approach is to reduce the bandgap through use of p-type InGaN on the top of the GaN. To date there have been reports of achieving p-doping ($\sim10^{17}cm^{-3}$) in compositions up to ~15% In.

GATE DIELECTRICS

Work in this area for power MOSFETs and gate turn-off thyristors is just commencing and some preliminary results are becoming available for AlN, AlON and $Ga(Gd)O_X$, the latter producing excellent characteristics on GaAs and InGaAs and now being applied to GaN.[30] Channel modulation has been demonstrated for AlN and $Ga(Gd)O_X$, but interface, state densities appear well above $10^{11}cm^{-2}$ at this point and much future effort is required to reduce this.

SUMMARY AND CONCLUSIONS

Rapid progress is being made on most of the process modules needed for GaN devices. Apart from the p-ohmic contact on laser diodes and gate dielectrics on emerging power MOSFET and thyristor devices, the processing does not appear to limit the device performance.

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