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TITLE: A HIGH SPEED CAMAC DIFFERENTIAL BRANCH HIGHWAY DRIVER

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A HIGH SPEED CAMAC DIFFERENTIAL BRANCH HIGHWAY DRIVER

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ABSTRACT

A new CAMAC branch driver is described that incorporates several unusual features which combine to give reliable, high speed performance. These include balanced line driver/receivers, stored CAMAC command lists, 8 DMA channels, pseudo LAMS, hardware priority encoding of LAMS and hardware implemented Q controlled block transfers.

INTRODUCTION

When the original SDS 930 Data Acquisition Computer System at the Los Alamos Scientific Laboratory (LASL) Van de Graaff facility became obsolete, a new triple MODCOMP IV/25 shared memory multiprocessor system was obtained to replace it.[1] At first it was planned to build high speed, special purpose, digital interfaces for the anticipated data devices such as Tennelec PACE ADCs, EG&G time of flight clocks, etc. in a manner similar to what existed on the SDS 930. However, it soon became evident that high performance CAMAC interfaces were feasible so the development of such a device was undertaken in order to gain the advantages of an international, modular standard.

The first MODCOMP/CAMAC interface built at LASL was done for the dual MODCOMP IV/25 system at the Weapons Neutron Research Facility at the Los Alamos Meson Physics Facility.[2] This was a dedicated CAMAC crate controller driven directly by a MODCOMP I/O bus. This system has a very fast response time to CAMAC LAMs, but must operate within the 25 to 100 foot limit of the MODCOMP I/O bus, operates only one crate and uses only one DMA channel. These characteristics were not appropriate for the Van de Graaff facility because of the distances between the experimenter's work area and the computer room, the very wide range of experiments performed which indicated the need for more than one CAMAC crate and multiple DMA operations. Thus a second interface was developed called a Differential Branch Driver (DBD) and i s associated Differential Branch Transciever (DBT).

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Design Considerations

MODCOMP IV/25 computers offer several features which are very advantageous for high speed, real time applications. The design of the DBD attempted to exploit these as fully as possible. Some of these features in regard to I/O operations and their significance in this application are as follows.

(1) Independent I/O Processor Data Path to main memory. This is important because high speed direct memory transfers can be supported without significantly impacting CPU or even other I/O memory operations. some computer architectures with a single memory bus, the bus can become a bottle neck, either locking out all other users while high speed I/O occurs or the I/O must be slowed down in order to allow other users to get to the main memory.

(2) High speed secondary I/O processor (SIOP) available. This is significant because it allows the CAMAC DBD to be run on the SIOP while all normal peripherals are supported by the standard primary I/O processor (PIOP). Since the SIOP has higher priority than the PIOP, the data acquisition I/O can occur at the maximum possible rate.

(3) Multiple DMA channels with:

(a) Internal word transfer counter.

(b) Internal transfer address control.

(c) Internal error sensing (e.g. memory parity error, acces

rights violation, and length error sensing).

Since these essential features for any DMA system are provided in the MODCOMP I/O processors it simplifies the design of the DBD.

(4) Single word (16 bit) or double word (32 bit) transfer per DMP request. This capability allows the most efficient use of the I/O bandwidth because even though CAMAC has a 24 bit data word, many devices such as ADCs only generate 10 to 13 bits of precision which can be easily handled by a 16 bit word transfer. In other cases the full 24 bits can easily be handled by a double word transfer. (By being able to do a double word with one DMP request, overhead in accessing the IOP is halved.)

(5) "Endless" or "broken" chain block transfers. This allows a controller such as the DBD to continusously fill a series of data buffers in a "round robbin" fashion with no action required by the software except when the data is coming so fast that an empty buffer is not currently available to be filled. Data Interrupts (DIs) and Service Interrupts (SIs) are provided by the IOPs and compatible controllers to allow the software to manage this situation.

The DBD Design

Figure 1 is a functional block diagram of the Differential Branch Driver with the MODCOMP I/O bus portion on the left designed like the "front end" logic of a typical MODCOMP DMA controller. The differential CAMAC branch highway signals are shown entering and leaving the DBD on the right. Some of the salient features of the system are as follows:

(1) Integrated circuit SN75110AN differential line drivers and SN75107AN receivers are used to implement the differential branch highway in the DBD and also in the Differential Branch Transceiver (DBT) located at the other end of the differential branch near the CAMAC crates. These current sensitive devices provide long branch highway capabilities of up to 3.0 kilometers compared to the normal branch length of 25 meters or less. They also provide ground isolation and common mode noise rejection between the CAMAC and computer systems which contributes to a more reliable and a lower noise system.

(2) The 7 unassigned pairs of wires of a branch highway designated BV(1-7) are used as dedicated lines for selected LAMS, called "Pseudo" LAMS. These signals are carried completely through to the branch driver which has special logic to recognize and priority encode them without having to go through the normal graded LAM cycle. This significantly increases the speed of response to these LAMS. Seventeen additional LAMS are serviced by the standard graded LAM cycle procedure and are also priority encoded by hardware in the DBD.

(3) A high speed random access memory (RAM) that is 256 words long by 28 bits wide is used to store 8 lists of CAMAC commands and up to 128 words of data if desired. In addition to the normal CNAF, the command contains bits to determine which of four modes of operation are to be used. The four possible modes are "single cycle", "address scan", Q repeat, and "Q stop". Other bits control whether the input/output from the computer will be single word (16 bit) or double word (32 bit), end of stack, and there are seven multipurpose bits. These seven bits control the maximum number of cycles allowed in the "Q Stop" and "Scan Address" modes or control interrupt generation, etc. in the Single CAMAC Cycle and "Q Repeat" modes of operation. The CNAF is also internally decoded to determine whether an input or output request is to be made to the computer which allows intermixed read and write commands to be implemented.

(4) Each of the 8 lists of commands stored in the RAM (called "STACKS") may be connected to any of the Pseudo or Normal LAMS by DIP switches or they may be executed by a computer command to the DBD. Each STACK may drive a separate direct memory access channel with independent transfer address, transfer count, and end of block interrupt. Automatic block chaining is also supported with the appropriate DI and SI interrupts generated at the end of block and end of chain.

Construction

Construction of the DBD and DBT was implemented using a computer aided wire wrap system called CASH by its vendor Standard Logic, Inc. Figures 2 and 3 show the actual hardware which has remained essentially the same throughout the development and production models. There are a total of about 400 integrated circuits in the system. Eight systems have been built for use at LASL and two have been supplied for use on the MODCOMP systems at the Lawrence Berkeley Laboratory. Two more are under construction for use with a MODCOMP CLASSIC 7860 to be mounted in trailer and moved to various accelerators away from Los Alamos. The long branch highway capability was essential in this application.

Results

Data rate tests have been performed to verify the high performance capability of this system. For example when the system was reading in an ADC at a 50 KHz sample rate, the addition of a 100 KHz word transfer to refresh a graphic display increased the dead time of the ADC by only 0.7% a negligible effect.

In another test when the MODCOMP was made to run a CPU bound program, the addition of 50 KHz input from an ADC slowed the program execution by only 10% which is perfectly acceptable for a system whose main task is to acquire data.

The system can support single parameter histogramming data rates between 90 KHz and 115KHz depending on the ADC type.

Since the standard CAMAC branch cycle involves a transit time handshake, the raw speed of the system depends on the highway cable length, transfer mode, and block lengths. Nominal figures for this system are ≈ 3 μsec/16 bit word with ≈ 150 feet (≈45.7 meters) of cable and ≈ 2μsec/16 bit word with ≈ 60 feet (≈ 18.3 meters) of branch highway cabl

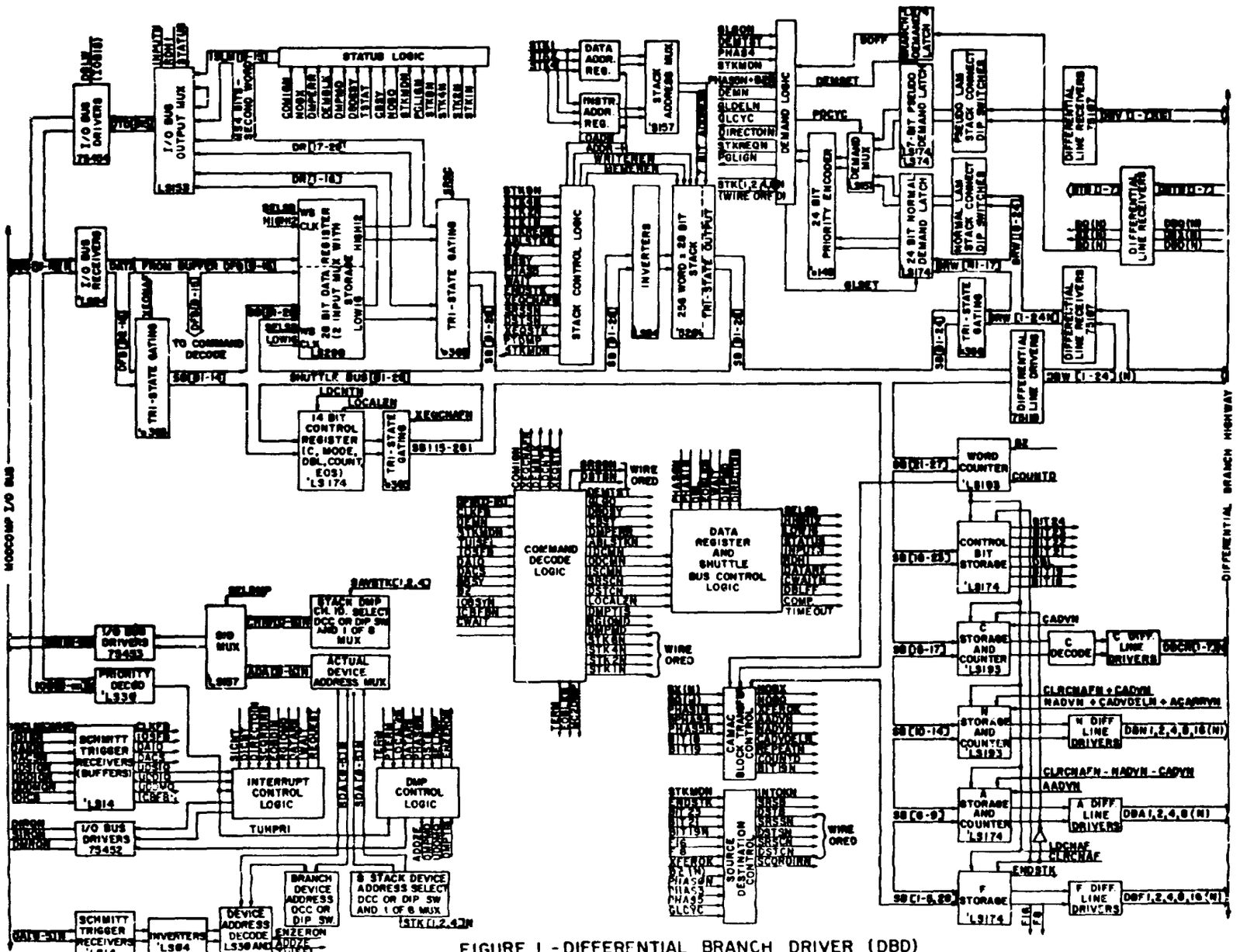

FIGURE 1 - DIFFERENTIAL BRANCH DRIVER (DBD)

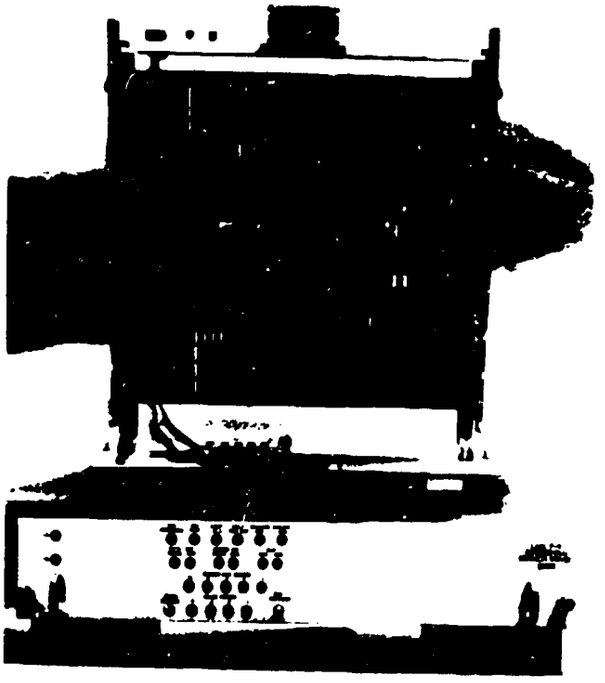

FIGURE 2. Front and top views of the Differential Branch Driver (DBD)

Reliability of the units have been excellent with essentially no maintenance required on the units installed at the Van de Graaff over the 2 to 3 years they have been in continuous use.

References

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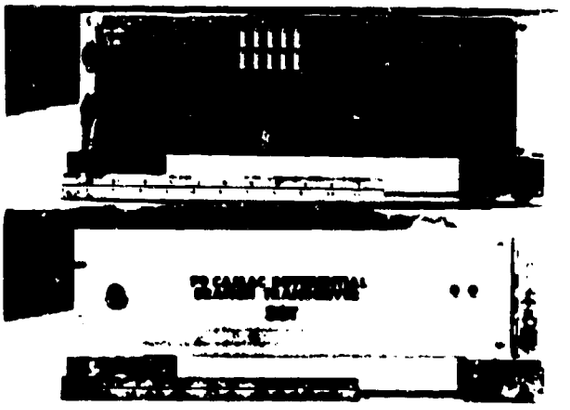

FIGURE 3. Front and back views of the Differential Branch Transciever (DBT)