Light-Triggered Thyristors for Electric Power Systems

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ABSTRACT

A program to develop a method of triggering a 53mm, 2600-volt, 1,000-amp thyristor with a light source is described. Normally, these devices are electrically triggered, but the need for placing a large number of these units in series for high-voltage applications made electrical triggering, with its associated insulation problems, expensive and complex. In this program, a light-sensitive gating method was developed, with associated amplifying layers built integrally into the power thyristor. LEDs and LDs were used as the light source. Fiber optics provided the electrical isolation and transmitted the light directly into the thyristor package.

Results were a turn-on capability to handle a voltage rate-of-change of 2000 volts per microsecond, with a light input to the thyristor gate of 30 nanojoules. A problem was encountered and investigated in high rates of current flow at the instant of light trigger. This resulted in excess temperature levels in localized spots where the current flow was initiated. Packaging and light source options are discussed.

EPRI PERSPECTIVE

PROJECT DESCRIPTION

It is well known that thyristors have revolutionized dc converter technology, replacing mercury-arc valves, vacuum tubes, and gas tubes in practically all applications, including HVDC converters. The specification of thyristors in HVDC converter terminals is unique; a large number of thyristors are connected in series (say 100-200 for a 200-kV valve), and they all have to be fired simultaneously with mutual electrical isolation. At present, electrically fired thyristors are used in HVDC converters. The technique used to fire these thyristors is based on an optical scheme that involves sending a light pulse to the thyristor module, converting the light pulse to an electrical pulse, and firing the thyristor through a pulse transformer. The power for the electronics is derived from snubber circuits. However, such a scheme involves many electronic components, and the development of direct light-fired thyristors, along with a satisfactory optical firing system, became the goal of this project. This is the final report of this development work by the General Electric Co.

PROJECT OBJECTIVES

The goal of the project was to establish the feasibility of the light-fired thyristor for electric power systems and more specifically for HVDC converters. The specifications were written with application to HVDC converter terminals in mind; this called for very stringent gain, dV/dt, and di/dt requirements, along with a limited tolerance in turn-on and turn-off voltage characteristics. The cell size chosen was 53 mms since for this size the electrically fired thyristors are well established at a rating of 2600 V and 1000 A. A high performance goal was set so that the laboratory-engineered light-fired thyristor prototype, combined with commerically available optical fibers and light sources, would have a good chance of replacing electrically fired thyristors.

CONCLUSIONS AND RECOMMENDATIONS

Owing to the expertise and diligence of the project investigators, the goal has been achieved. This successful project is a pioneering step and clearly points to the potential of light-fired thyristors, not only in HVDC converter valves, but also in controlled VAR generators, in high-voltage switching devices where series thyristors are not needed. This wide range of applications is expected because of the simplicity, freedom from electromagnetic interference in triggering circuits, and anticipated lower cost of a system using light-fired thyristors. Further advances are, of course, needed to establish commericially acceptable devices with high production yields; advances are also expected in optical sources and fiber optic systems. Data for this project have assured us that such advances are within reach.

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Section 1

SUMMARY

PROGRAM OBJECTIVES

The main objective of this program was to develop a light triggered high power thyristor of the type useful in electric utility applications. One example of an intended use is in solid state High Voltage Direct Current (HVDC) conversion stations. These stations convert large blocks of power from 60Hz to DC and then back to 60Hz for long distance transmission or asynchronous ties between utility systems. In such applications, direct light fired gating promises a number of improvements at the systems level. First, virtually infinite gate isolation is achieved. Second, the control circuitry is assured of almost total noise immunity. Third, the gate photo-current risetime can be an order of magnitude smaller than the electrical gate current risetime in the electrically gated HVDC module. In addition to these benefits, there is the possibility of a simple system with cost and reliability benefits achieved from the elimination of the high voltage pulse transformers and the auxiliary power supplies now required to generate gating pulses for electrically gated thyristors.

This work centers on the modification of an existing high power thyristor characterized by the diameter of the silicon wafer which is 53mm (∿2 inches). The thyristor rating is presently at 2600 volts and 1000 amperes, and it is used in HVDC stations currently under construction. This thyristor was so redesigned such that it could be triggered into conduction by a beam of light instead of the conventional conducted gate current. In addition, it was also intended to apply new thyristor gate designs to obtain a measure of internal cell protection against specific system transients. Such internal self-protection could conceivably reduce the probability of device failures when triggered into conduction either by excess anode voltage or by excess rate of rise of anode voltage (dV/dt). The new light sensitive thyristor was to be housed in a modified Press Pak production package, suitable modifications to the package being made to permit entry

and registration of the trigger beam of light with the package installed in a typical HVDC module.

One fundamental constraint conditions the entire approach to light fired thyristor design. This constraint is the small and limited quantity of photo-energy available for triggering the thyristor when practical light sources and light pipes are used to generate and convey the photon flux to the light active area of the thyristor. Translated into thyristor terms, this requires thyristors with very high gate sensitivities, of the order of 100 times that of the electrically fired device. However, high gate sensitivity always leads to high sensitivity to noise which, stated in another way, means low dV/dt capability. This leads to a trade-off which we (1) and others (2-5) have solved by going to small light active regions and physically small initial turn-on regions. Responding to the dV/dt gate sensitivity trade-off in this manner automatically reduces the ability of the thyristor to handle large rates of rise in anode current. The answer to this problem is not yet clear but there appears to be potential solutions which merit attention.

The highly interdependent nature of the thyristor characteristics the final HVDC system architecture requires a thorough knowledge of potential light sources and the fiber optics used to channel and control the light beams. As a result, work was also to be done to review the present state-of-the-art in applicable light sources and fiber optics or coupling media. Final device tests were to be run to characterize operational parameters important to HVDC system operation with particular emphasis being placed on testing those cell parameters currently specified for HVDC module operation.

Practical problems involving light source and light pipe coupling and the important problem of device packaging were also considered and will be discussed in this report.

CHRONOLOGICAL SYNOPSIS

While activities were reported on a regular basis, a number of accomplishments particularly stand out over the entire contract period. In the design phase, two computer programs were developed, one to predict photo-current in the thyristor for any light source and for any thyristor forward blocking voltage and one to shape the turn-on line periphery for optimum di/dt. In addition, a number of dV/dt correction factors were identified to increase our ability to predict and design to a specific dV/dt capability. In fabrication, three runs of light fired devices were made with several sub-variations in design, all with a relatively high yield of testable devices. In device testing, xenon flash lamps, cw YAG lasers, solid state lasers and LED's were all used to turn on the thyristor. Turn-on threshold incident photo-energies at blocking voltages of 100 volts ranged from 10 to 30 nanojoules with threshold d.c. gate power levels from 5 to 10 milliwatts. Measurements proved dV/dt capability to be within 10% of the design point of 2000 V/μsecond at 105°C. Forward drop, leakage current and blocking voltage were comparable to the original electrically fired device while delay time and turn-on time were somewhat improved and reduced. Di/dt capability varied widely as a function of snubber design and operating temperature. Turn-on tests show di/dt's of from a low value of tens of amperes per microsecond to thousands of amperes per microsecond.

For turn-on analysis, a model was derived which could be used for understanding turn-on as affected by snubber design, ambient and transient temperature and details of the external circuit. While this model and the associated computer program are in the development stage, some results are used in this report to identify improved designs for high di/dt capability and more reliable turn-on.

DETAILED REVIEW

In the first stage of this work, device design computer programs were developed to simulate an improved two dimensional model which more accurately determines threshold levels for dV/dt turn-on as well as for gated turn-on. In addition, considerable vendor queries were made for the selection of suitable light sources and light pipes. Work was also done on light pipe insertion into hermetic packages.

In the next stage, the major effort was expended in considering and selecting a design for the first light fired device mask set. This design aimed at a <5ma gate current turn-on threshold level along with a dV/dt capability of 2000 V/μsecond. This performance was to be achieved by a double amplifying gate design. The first or gate stage was to be the most sensitive to dV/dt turn-on as well as to gated turn-on so that a measure of cell self-protection against dV/dt turn-on failure was anticipated. A number of significant accomplishments were also made in the area of light sources and transmission media. A survey of optical sources allowed the selection of the 9000Å GaAs laser. However, GaAs LED's remained a second candidate owing to the desire for a long pulse length and their lower cost. Likewise the initial survey of transmission media led to the selection of Galite 3000 tefzel jacketed 19 fiber bundle manufactured by Galileo Optics as the prime transmission media compatible with solid state laser type optical sources. Package modifications to the standard 53mm Press Pak and heat sink design were made which allowed demonstration of light pipe insertion into the cell with the cell in the completed cell assembly.

Next a major effort was made to completely understand the photo-rectification properties of the proposed light fired thyristor device, the proposed device being referred to as the EPRI-GE1. This was done by varying wavelength, voltage and etch depth and measuring the photo-current on a similarly diffused wafer. With this complete knowledge of the spectral response, it became possible to predict photo-gate current for any light source and any anode voltage. A computer program was initiated to help in this analysis.

The completed masks for the EPRI-GE1 were finally delivered late in the third quarter. While awaiting mask fabrication for the EPRI-GE1, a set of test light fired thyristors were fabricated based on GE's L1 thyristor (1). These were termed the L1A and L1B devices and were partially optimized L1 devices in that the gate (L1A) or gate and pilot (L1B) amplifying stages were made more sensitive in just the same way that is planned for the EPRI-GE1 device. These devices were partly tested and were found to have turn-on thresholds betwen 2 and 5ma. They were also successfully tested for blocking voltage, dV/dt capability and turn-on speed (initial di/dt capability) at room temperature. These tests, although incomplete, indicated the gate thyristor amplifying stage to be as sensitive as 1-3ma. These tests also indicated what kind of light pulse overdrive factor might be suitable using junction laser sources operating at room temperature. However, from those results, both at 25°C and 125°C, and at voltages from 5V to 2500V, it appeard that, with a 100nsec photo-pulse length, an overdrive factor of ~50 was needed for fast and reliable turn-on. LED tests were completed which relate to the possible use of LED's for the light source. In addition, light source-light pipe coupling tests were continued with two main areas of attack. In the first area, considerable effort was expended in accurate, lens assisted coupling from an LD68* laser into different light pipes to get an upper bound on the amount of photo-power available at the output end. In the second area, cheap, simple and reliable coupling was attemped through mechanical alignment procedures without use of lenses.

In the fourth quarter, major efforts were expended in three areas, the most important being the joint fabrication of the EPRI-GE1 light fired thyristor by SPCO, Collingdale, PA and by CRD in Schenectady, NY. This effort resulted in a first run of approximately 40 devices with two groups based on light sensitive area and two subgroups based on light sensitivity. The second major effort in this quarter was the collection and unification of our work on light sources and light coupling arrangements. In this area, we concentrated on laser sources.

* Laser Diode Laboratories, New Jersey.

The third major work of the fourth quarter involved further tests of the L1A and L1B devices fabricated and partly tested in the third quarter. In this quarter, the first low temperature (77°K) light sources were used to fire the L1A and L1B devices with interesting results. Tests were also made with a longer wavelength laser (1.06μ) and with longer laser pulses (up to 20μseconds). Tests were also initiated to determine how light pulses applied under reverse bias conditions might affect thyristor performance and reliability. Finally, to complete the photo-response study begun in the third quarter, we presented some results of the computer program initiated in the third quarter which allows the level of photo-gate current to be predicted under various conditions of voltage for virtually any light source or thyristor junction design.

During the fifth quarter, the major effort was expended in measuring characteristics of the EPRI-GE1 thyristors fabricated during the fourth quarter. These devices were thoroughly tested for breakdown voltage, leakage current, forward voltage drop, and dV/dt capability before light fired turn-on testing. In all these areas, the devices met the criteria of being as good as, or better than the original electrically fired devices. Turn-on tests were then performed with different light sources. These tests established that device sensitivity ranged from 2.5 to 6ma in threshold gate current. A threshold criterion expressed in energy of 10 to 20 n joules is more realistic considering the shortness of the laser pulse. Delay times were suitably short for gate pulse energies several times larger than the threshold energy value.

The problem of excessive snubber circuit di/dt was investigated in a number of the devices. Tests consisted of increasing stored snubber energy and peak snubber discharge current as well as ambient temperature until the device failed or measurably degraded in blocking voltage. All devices but two were able to withstand 25°C turn-on from 2000 Volts with di/dt's of close to 1000 A/μsecond from a 1μfd, 10Ω snubber discharge as well as turn-on from 1800 volts at a 100 °C ambient temperature with a di/dt of 350 A/μsec. Going to large capacitor values and small snubber resistance enchanced the probability of failure which then occurred in some cases along the turn-on line of the main thyristor. With the limited data now in hand, it would appear

that the present design has an enhanced main emitter di/dt capability but may now require some restriction on snubber design to protect the gate stage from excessive temperature excursions.

During the final quarter, 35 additional devices were made for testing and have been identified as run #2. These devices were more sensitive than the run #1 devices and consequently, had a lower dV/dt rating of about 1800V/μsecond. Breakdown voltages were several hundred volts lower* but most devices could be rated at 2600 volts. Tests of turn-on capability were continued on both the run #1 and run #2 devices. Nine were packaged and tested in regular HVDC test equipment with several problems showing up. Only one device in three passed the leakage test. Only one of the devices passed the regular HVDC one minute di/dt test. These results pinpoint the problems of the light fired thyristor as they presently exist. A later part of this report will deal with the amplifying gate vs. the non-amplifying gate alternative because of its importance with respect to the ultimate di/dt capability of thyristors with small turn-on line lengths. In the same section, we will deal with the possible advantages and disadvantages of the hybrid light fired thyristor being pursued by Brown, Boveri and Company in Europe. Some preliminary tests will be described pertaining to the hybrid approach.

Much of our understanding of the turn-on amplifying gate thyristors is contained in a model described in this report and which is presently being further developed. Computer calculations show how di/dt capability may be enchanced both in integrated and in hybrid structures.

Experiments involving voltage breakdown self-protection were begun during the final quarter but as yet no devices have been obtained. Light pipes for a practical panel firing system were also obtained but have not yet been tested.

* The starting material came from a wafer lot with slightly lower resistivity.

Section 2

THE LIGHT FIRED THYRISTOR IN AN HVDC APPLICATION

SYSTEM IMPOSED CONSTRAINTS

Consider replacing the combined optical-magnetic system now used, as shown schematically in Figure 2-1A, with the direct light fired system which is shown schematically in Figures 2-2 and 2-3. The control signal to trigger the value is produced in the control circuitry some distance from the valve hall. This causes lasers in Modules A and B at ground potential in the valve hall to be pulsed and emit light. For each panel in the valve, light from four separate lasers is combined into two light pipes which plug into a connector module in the panel. A separate light pipe, bifurcated at one end and separating into separate light pipes conducts the light from the panel light pipe connector into each light fired thyristor. It is desirable that the panel switch effectively under the following modes of failure:

(i) random failure of a laser.

(ii) failure of a laser pulser module.

(iii) breakage of one of the laser-to-panel light pipes.

Spare light pipes are included in the panel for easy repair of broken light pipes in the panel.

It is also mandatory that the light pipes and the connectors be rugged, simple to install and to replace. These conditions can be easily met in the present GE HVDC panel except at the plug-in point of the light pipe into the thyristor package. Since the light pipe cannot be bent beyond a maximum curvature, it may be necessary to rearrange the way the thyristor modules are placed inside a panel for easier access.

Redundancy and ease of installation and repair are not the only conditions that must be considered in the delivery of photo-gate pulses to the thyristor. Light source reliability, light source

compatibility to the thyristor, and light source - light pipe coupling must be considered. Solid state laser light sources operated at room temperature are attractive on all of the above counts. Such sources are particularly reliable when run at less than maximum current and reduced duty cycle as could be the case in an HVDC system.

With the dual laser pulser modules and with the proper lasers, the gate photo-pulses need not occur either in coincidence or at a one per cycle rate. Instead, pulser module B might be delayed 20-50 μsec. in order to retrigger devices which may not have turned on or which may have turned on and rung off. Repeating pulses A and B in this manner for 120^{o} at .5 to 1 millisecond intervals would also be possible and could result in improving overall system behavior with respect to major line disturbances.

The above discussed features are tabulated in Table 2-1 which also gives an idea of the size of photo-signal losses between the source and the thyristor. Note that the energy available for firing (watts times pulse length) is very small. When you also consider that it is desirable that this energy be 10 to 20 times the threshold firing energy of the thyristor, it is clear that the thyristor must be made very sensitive. This, in fact, is the one overriding technical consideration or constraint in development of an HVDC directly light fired thyristor. High thyristor sensitivity has another benefit in terms of cost reduction. More sensitive thyristors require fewer, less expensive laser sources, less powerful laser pulses and fewer optical fibers.

THE THYRISTOR ENVIRONMENT

Assuming 4 LD168 lasers to 12 thyristors (with 3 spare light pipes) in each panel, a pulse amplitude of approximately 2.67 watts is available for each thyristor. With a 100 n second pulse length, this is approximately 267 n joules. If a laser pulser module or a laser-to-panel light pipe fails, this becomes a 133 n joule pulse which implies that a thyristor with a gate threshold energy of 10 to 20 n joules would still remain operating at 5 to ten times the threshold firing energy. Converted into a d.c. gate durrent for an electrically fired thyristor, this would mean a threshold gate current of 3-5ma,

50 times the sensitivity of the normal electrically fired thyristor. In practice, our light fired thyristors have had a threshold incident photo-energy of 10-30 n joules and it is these thyristors which are required to have the additional characteristics described below. Note that many HVDC cell characteristics are not included, these being unaffected by the conversion from the old electrical design to the optically fired version:

(i) dV/dt capability - 2000V/μsec

(ii) delay time - invariable to within .5 second over all the thyristors in the valve

(iii) di/dt capability - 50A/μsec at 1800V and 105°C

In addition to these characteristics, it is necessary that the light fired version be compatible with the protective circuity which is used in HVDC valves to protect the cell from destructing under various unwanted transient conditions.

The light-pipe package coupling is the last constraint. However, it is a severe one since the light fired device, as presently viewed, is hermetically sealed for long term stability of electrical characteristics. In addition the hostile environment in the immediate vicinity of the thyristor requires special light pipes which have to be operable at 125°C, must be impervious to moisture, and must be able to withstand all effects of the high local electric fields.

Table 2-1

NECESSARY AND DESIRABLE FEATURES OF AN HVDC PHOTO-GATE SUB-SYSTEM

	ADVANTAGE	DISADVANTAGE
1. Redundant pulses and source (desirable)	(i) reliability	(i) cost
2. Redundant source-to-panel light pipe (desirable)	(i) reliability	(i) cost of light pipe
3. Redundant panel-to-thyristor light pipe (desirable but not presently advisable)	(i) reliability	(i) cost of light pipe (ii) need thyristor with two gates (iii) more costly and complicated package
4. Solid State Laser Source (necessary with light pipes > 30 feet)	(i) reliability (ii) couples well into light pipes (iii) operable at room temperature	(i) more costly than LED (ii) may not be as reliable as LED and may have to be operated at reduced duty cycle.
5. Double and repeated pulsing (desirable)	(i) improved response to unnatural valve conditions	(i) places higher stress on light sources
6. Simple rugged connectors (necessary)	(i) reliability (ii) ease of maintenance and repair	(i) 2-3 db loss per connector step
7. High optical coupling efficiency (desirable)	(i) Laser-light pipe insertion loss, 3-5db (ii) Light pipe transmission loss, 1-3db (iii) Panel coupling loss, 2-4db	
8. High Laser Source Energy (necessary)	(i) Fewer sources, fewer optical fibers. An LD168 laser could gate several thyristors	(i) Only solid state lasers are believed sufficiently reliable. However, no absolutely dependable operating life data exists at present.

Notes: 1. Usually a practical net loss from source to thyristor is about 10db.
2. The LD168 emits over a 20 x 20 mil area. Its duty cycle is .01% or 1000Hz for a 100nsec pulse width. It rated light output power is 100 watts.

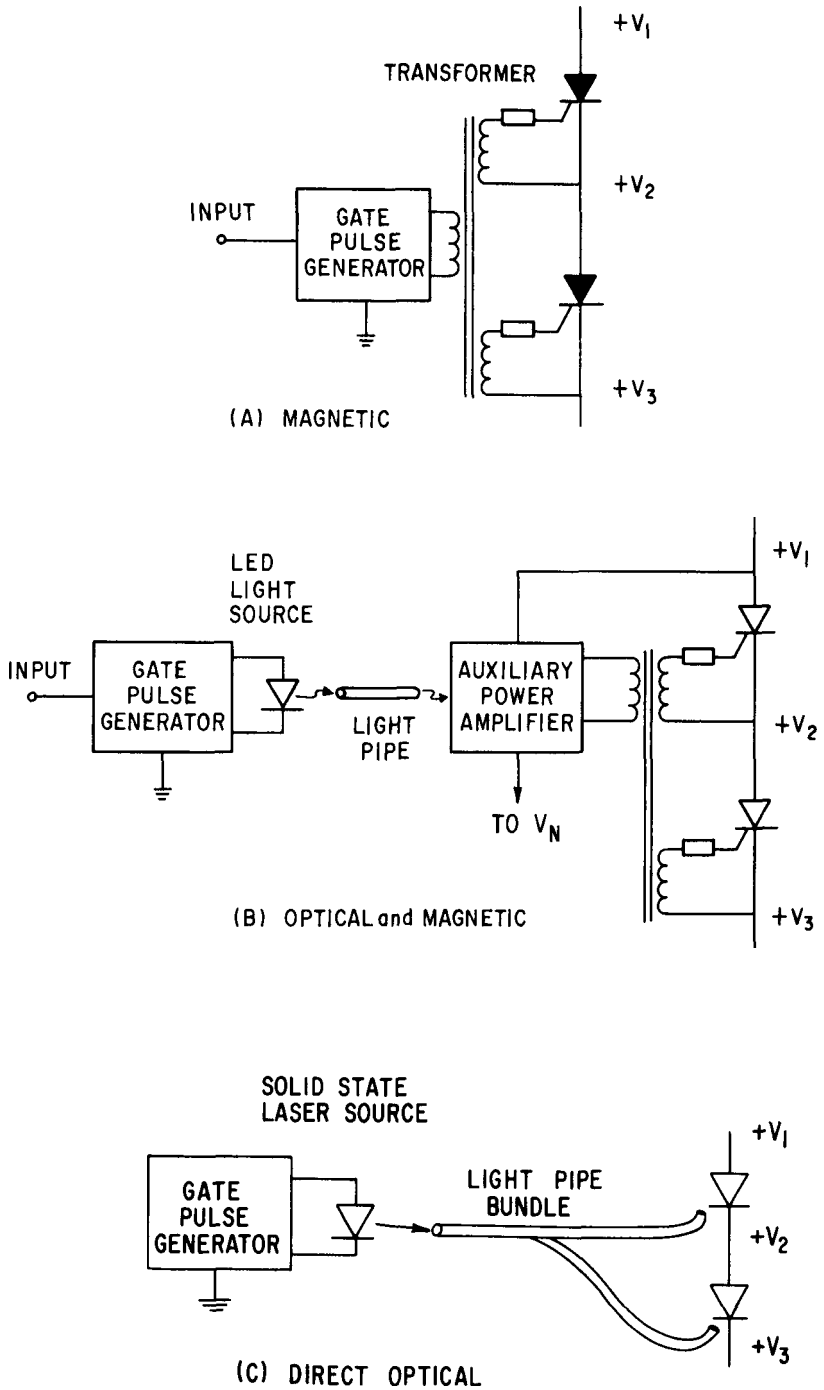


Figure 2-1. Simplified Schematic of Different Gating Systems for Thyristors in an HVDC Value.

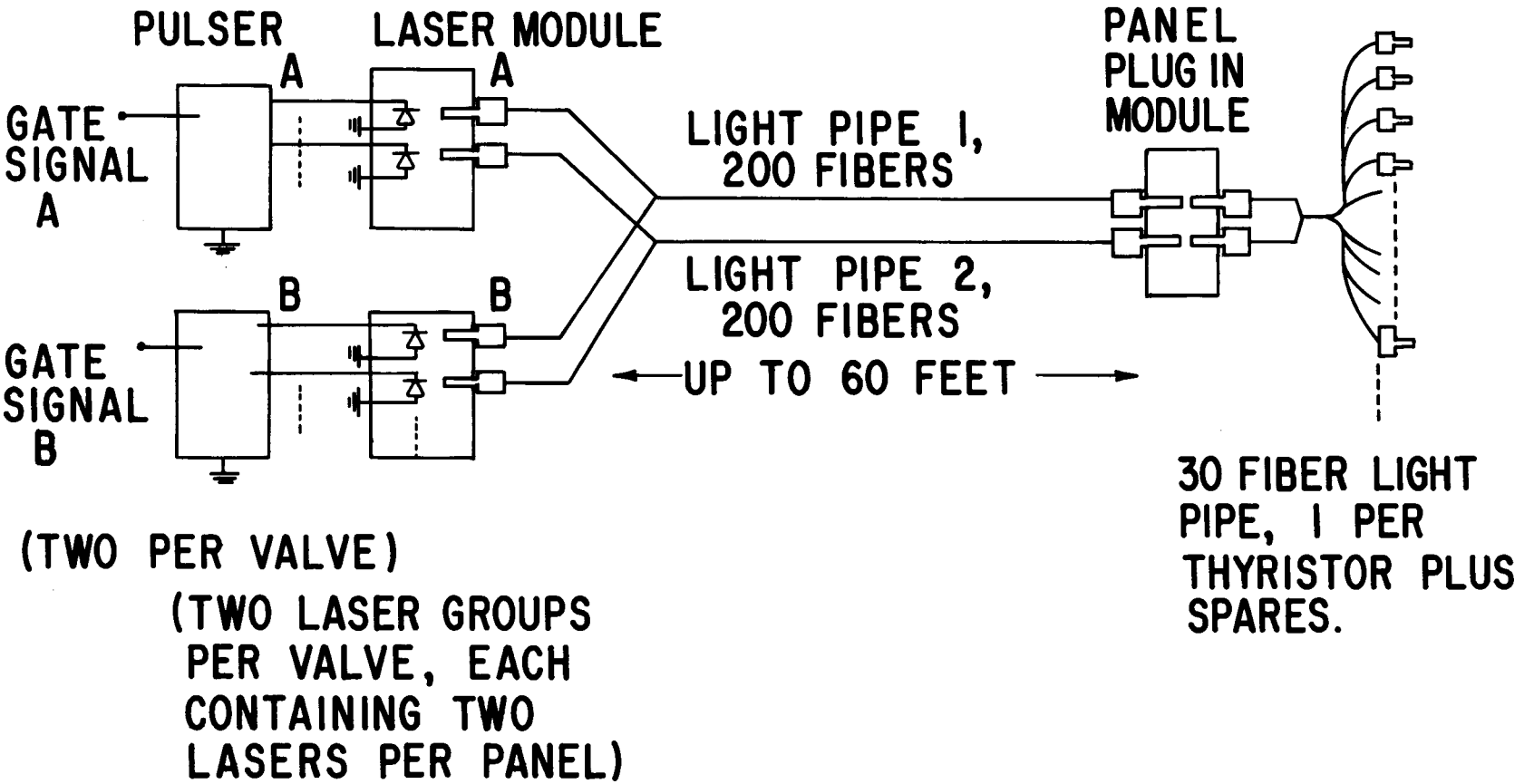


Figure 2-2. A Practical Gate Pulse System for Triggering Directly Light-Fired Thyristors with Source and Light-Pipe Redundancy

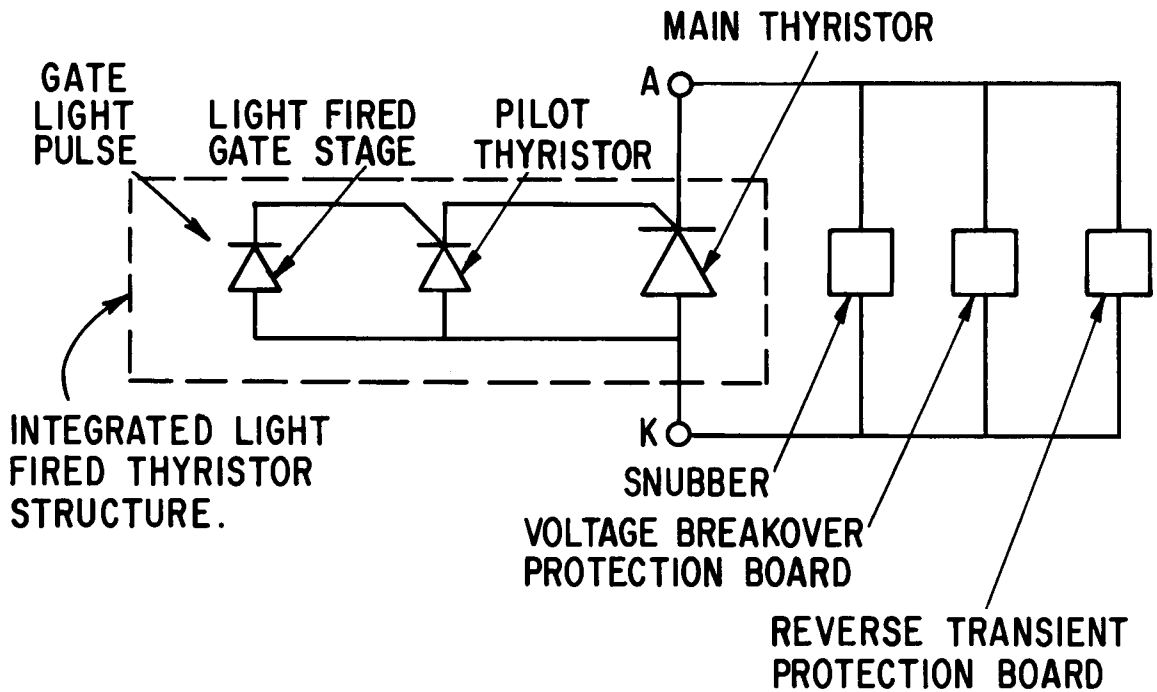


Figure 2-3. Simplified Schematic for a Single Level of an HVDC Thristor Stack

Section 3

LIGHT SOURCE SELECTION AND THYRISTOR PHOTO-RESPONSE CHARACTERIZATION

THE THYRISTOR TURN-ON PROCESS

In this section, the process of turn-on at low and high light intensity and the qualitative difference between electrical turn-on and photo-current turn-on of a thyristor will be described.

Figure 3-1 shows a radial cross-section of the center portion of a thyristor. In (A), the electrical turn-on case, the device is turned on by driving sufficient current between the gate "G" and cathode "K" to forward bias the n+ - p-base junction at the turn-on point (actually a line). This causes electron injection from the n+ cathode and these electrons, upon reaching the anode, call for hole injection from the anode. If the injection is sufficient to replace recombining carriers and carriers lost to the shorts, the electron and hole density rapidly builds up in the center n and p regions. Consequently, the conductivity, proportional to μ_n n plus μ_p p (μ, being mobility and n and p, being the electron and hole densities), increases. Current flows and the thyristor voltage falls rapidly. Since the gate current sees only the low gate voltage applied between the gate and cathode, the power dissipated by the gate signal is relatively low, perhaps 4 or 5 watts, over a period of perhaps 10 microseconds for a net energy of 50 μ joules even though the gate current might be several amperes.

In the light fired cases of 3-1 (B) and (C), hole-electron pairs, generated by absorbed photons, are separated at the forward blocking n_{base}-p_{base} junction. Holes flow to the cathode and electrons to the anode. Thus, the current flow path is different from the electrical case. The photo-gate current flows from anode-to-gate-to-cathode, with the electrons flowing to the anode being multiplied by the transistor gain of the lower p-n-p transistor. This has three important

consequences. First, the photo-gate current is larger than that of the original hole-electron pair generation by the factor $1/(1-\alpha_{PNP})$, the current gain of the lower "transistor". This gain factor is voltage and temperature dependent, increasing with increasing voltage and decreasing with increased temperature. The voltage dependence is not undesirable in the sense that it gives a higher gate overdrive factor where it is most needed. Second, hole injection from the anode begins sooner than with electrical triggering since electrons arrive at the anode without the upper n+ p-base junction having to be forward biased. As a result, overall delay time is somewhat reduced. Third, although the incident photo-gate signal may be low in energy, one or two hundred n joules for example, the carriers it creates see the full anode-cathode potential of up to 2000 volts. This leads to high power dissipation densitites in the photo-gate region whereby 20 - 40μ joules are dissipated in a small volume of semiconductor.

The difference between normal light firing and high level light firing is the level of light intensity. In Figure 3-1C, so many hole-electron pairs are created in the irradiated volume that a conducting or partially conducting filament is formed virtually instantaneously. Current flows as indicated by the large arrow to the cathode and turns on the remainder of the device. The light fired thyristors developed under this contract were to be turned on by normal or "regenerative" turn-on (1-5) and not by this high level or "direct modulated" turn-on as discussed in more detail elsewhere (1,6,7).

THYRISTOR LIGHT SENSITIVITY CHARACTERIZATION

The thyristor turn-on process has been briefly described in the previous section. However, the photo-rectification process itself needs to be briefly reviewed to better understand the problems involved in selecting a suitable light source.

To understand the rectification process, we first define what we term the "light active volume". The assumption is that only hole-electron pairs created in that volume are rectified and appear as photo-current. This volume has a surface area corresponding to the irradiated silicon area and an extent above and below the blocking junction as defined in Figure 3-2, this extent being composed of a somewhat temperature

dependent diffusion length and a voltage dependent depletion width. Light penetration into the silicon is characterized by a distance termed the absorption length. This absorption length is a function of the incident light wavelength. Low energy, long wavelength photons pass through the silicon without creating hole-electron pairs while short wavelength, energetic photons are absorbed before reaching the light active volume. This leads to an optimum wavelength for the incident light which is a function of the junction depth, the voltage and doping profile of the junction, and the carrier lifetimes. Over the wavelength range of greatest interest, the reflectivity of silicon is roughly constant at 32% but this reflectivity can be reduced with antireflective coatings.

Through absorption length, carrier diffusion lengths and depletion width are readily calculable, what is really required is a prediction of actual photocurrent which could be expected to flow. This, as pointed out in the previous section, is complicated by the voltage dependent photo-transistor action of the thyristor. Figure 3-3 shows a typical curve of photo-induced cathode current vs. time for a series of blocking voltages using a silicon doped GaAs LED (9400Å) light source. The bottom trace shows the LED current pulse. The top traces show the cathode current flowing as a result of the light pulse. This photograph has been included to illustrate the fact that the photo-induced cathode current pulse does <u>not</u> give the true value of the true diode photocurrent. In fact, the cathode current is given by diode photocurrent times a gain factor. As mentioned earlier, the thyristor detector is not a photo-diode but a combination between a photo-transistor and photo-thyristor. That part of the photocurrent which by-passes the n^+-p_{base} junction sees the transistor gain of the lower p-n-p layers while the n^+-p_{base} component is multiplied by the positive feedback gain of the thyristor. The first gain factor is usually between 1 and 5. The second gain factor is only present for amplitudes above threshold and, at such current levels, builds in time to infinity.

To understand the cathode photocurrent traces, it is necessary to realize that the diode photocurrent <u>does</u> increase as the voltage is increased. This effect, however, gradually saturates as the upper edge of the light active volume approaches the upper surface. An

example can be seen by looking at the current amplitudes at about 1μsec into the LED pulse in Fig. 3-3. The large current growth seen for later times is due to the variation of the photo-thyristor gain factor which is often considered a function of current density though, in fact, it is a function of local base region charge density. If the LED current pulse were several microseconds longer, the thyristor would turn on. Since, in this program, we were working to convert an existing electrically gated cell which would have basically the same n^+pnp^+ profile, process and lifetimes, it was decided to supplement our calculations by measuring photo-response directly as a function of (i) wavelength, (ii) blocking voltage, (iii) light region etch depth, and (iv) surface treatment. This immense catalog of data was stored in a computer program. Armed with this and given the spectrum of a particular light source, it is then possible to predict actual photo-gate current in the light fired thyristor under design.

Figure 3-4 is typical of the raw data taken and stored in the form of photo-response as a function of incident light wavelength with anode-cathode voltage the parameter. Similar sets of curves were taken with different etch down depths and with different surface treatments. Using light source spectra such as those of various Xenon flash lamps shown in Figures 3-5, 3-6, and 3-7 as input data, the computer calculates and plots the expected photo-currents. Examples are given in Figures 3-8 to 3-12. Note that the 9450Å LED source has the highest response at all voltages, just as one would expect looking at Figure 3-4. The Xenon sources have too much of their output at low wavelength and the 1.06μ YAG laser has too long an absorption length (too low an absorption coefficient). Qualitatively the curves are quite similar as a function of anode voltage. Over the initial 100 volts the response increases with the growth of the depletion region. With the exception of the highly penetrating radiation (e.g., 1.06μ wavelength in Figure 3-13), the remainder of the response variation is due to the increased transistor gain, $(1-\alpha)^{-1}$, which, at very high voltages is increased to $(1-\alpha M)^{-1}$ where M is the avalanche multiplication factor.

Figures 3-14A and B are shown as a sample of the types of surface conditons that were treated, the response in (A) being for a fixed anode voltage of 20 volts and the response in (B) being for a fixed anode voltage of 2000 volts.

LIGHT SOURCE-LIGHT PIPE SELECTION

A large number of variables need to be considered in the selection of a suitable light source and light pipe. Solid state lasers and LED's operating at room to 50°C or liquid nitrogen (77°K) temperature were considered the most likely choices. Flash lamps and the cw YAG laser were also used in our tests. Light pipe variables were fiber diameter and fiber type - low loss, low acceptance angle fibers vs. high loss, high acceptance angle fibers. Ultimately the solid state laser with its directed light output was selected to allow the use of low-loss light pipe whose acceptance angle, while low, was still large enough to admit most of the laser energy.

Light pipe selection work on the light source selection problem started early in this program since it was desirable to find an optimal source-light pipe match before selecting the initial thyristor design. To achieve this, a number of lasers and LED's were ordered and special test equipment was designed. A number of light pipe manufacturers were contacted including Dupont (Crofon light pipes), Corning Glass Works, Fiberoptic Cable Corporation, Galileo Optics, and Nippon Sheet Glass (maker of SELFOC light guides). The new 19 fiber Galite 3000 light pipe made by Galileo Optics is supplied with a carbon free "Tefzel" jacket which is impervious to moisture and should have excellent high field characteristics. This new product can be compared with Galite 2000 light pipe from the same manufacturer. The comparison is shown in Table 3-1. From this comparison it can be seen that, if numerical aperture (NA) losses are not included, the Galite 3000 should be approximately four times less lossy for a 60 foot light pipe although about equal for a 10 foot length. To a large degree, neglecting the NA losses is valid only for fairly well columnated laser sources. One or two preliminary tests were made with the Galite 2000 light pipe which show approximately 10db loss using a solid state laser diode (LD-66) junction laser coupling into a 25 foot light pipe.

Another feature of the Galite 3000 is that it has an unusually water free glass core. This improves the transmission at 9000Å (a common GaAs laser wavelength) by an order of magnitude over competing light pipes which, for the most part, were optimized for a 8200Å wavelength.

See, for example, the absorption losses for the various light pipes in Table 3-1 at 8200Å, 9000Å, and 9500Å.

LED Tests

Although LED's have a less columnated output than the junction laser, they have the advantage of a lower cost and a much larger pulse length and duty cycle at all temperatures. Hence, test apparatus was built and a number of LED's ordered for performance tests. The two questions to be answered by these tests were whether enough light can be generated to turn on the thyristor and whether LED operation at or close to the maximum pulse length, pulse amplitude, and duty cycle results in much decreased LED performance. Figure 3-15 shows the apparatus involved. Up to 24 diodes can be tested in parallel. They are mounted in a copper block which is shown sitting on a heating stage. A p-i-n light detector measures light output and a thermal probe measures temperature. Both are shown in the photograph. The experiment consisted of subjecting GaAs LED's (IRE 10's) obtained from Laser Diode Laboratories to 4A, 4μsec, 667 pps pulses and cycling the ambient temperature up to 150°C as shown in Table 3-2. Two devices failed after 150°C operation; otherwise, no destructive failures were observed. It appeared, even in these failures, that it was due to poor lead bonding rather than failure of the LED itself. Figures 3-16 and 3-17 show that a 150°C break-in period might be useful in eliminating failure prone devices. They also indicate that there is a little loss in light output after initial degradation. This is indicative of field (and temperature) assisted movement of a finite number of light absorbing centers into the light active region of the LED.

Laser Tests

Accelerated laser life tests were also performed on several solid state lasers. A Laser Diode Laboratories model LD66 single-junction laser was driven at 4 KHz repetition rate with 40 A peak-current pulses having a triangular form with a 220 n second half width. (These conditions are near the maximum as rated by the manufacturer.) The emission decreased about 10% in 73 days of operation, a time equivalent of 13 years at 60 Hz and about five times as long as the life test reported by the manufacturer. The same test was repeated for one-fifth the time with the laser at 70°C. No degradation was

detected. While far from conclusive, these results show that laser diodes can have adequate life for high-voltage switching-station use. In addition, none of the lasers regularly used in our normal turn-on testing, either at room temperature or at 77°K (liquid nitrogen), failed or degraded to any noticeable degree even though operated at peak current rating.

Possible Use of Different Light Sources

Having cataloged a complete series of curves as a function of thyristor voltage, junction depth and surface passivation material, it is possible to accurately predict the photo-induced gate current for a particular thyristor design, given the spectral output of the light source. Figures 3-8 to 3-13, already described, demonstrate this ability for a number of interesting cases in which the thyristor was assumed to be etched down 25 microns in the light sensitive region and the surface covered with an $\varepsilon = 4$, transparent, insultaing dielectric. This corresponds closely to the eventual condition of the packaged EPRI-GEl light fired thyristor. Six different sources were treated. To make a meaningful comparison, the total energy from each of the light sources between .5 and 1.2μ is the same, i.e.,

$$\int_{.5\mu}^{1.2} E(\lambda)\, d\lambda = 1$$

These figures showed the thyristor photocurrent as a function of forward blocking voltage. In Figure 3-11, the source is the 9000Å GaAs laser with all of the energy falling within ± 100Å. In Figure 3-12, the wavelength of 9450Å corresponds to an Si doped GaAs LED. Here again the line width is fairly narrow, being of the order of several hundred Å. Figure 3-13 corresponds to the 1.06μ YAG laser sometimes used in our tests. These sources have in common the fact they they are narrow bands and they they lie, in energy, close to the bandgap energy in Silicon, their penetration depths being 25μ, 50μ and more than 100μ, respectively.

The differences in the photocurrent vs. thyristor voltages in Figures 3-11 to 3-13 are based on the difference in penetration depth. Figures 3-11 and 3-12 are similar in that they do not penetrate to the

blocking junction whereby their effectiveness increases with voltage as the p-base layer depletion pushes up toward the upper surface where the light is impinging. As can be seen in the figures, this depletion layer growth is fairly rapid betwen 0 and 50 V but is slow thereafter due to the exponential form of the p-region doping profile. The rapid rise in response beginning at 1500 volts, which seems contradictory, is actually the result of increase photo-gain from the improving transistor action of the lower p-n-p layers of the thyristor due to the effective narrowing of the undepleted n-base.

In Figure 3-13, the photo-current increases much more rapidly. Here the light penetrates too far and the response grows, not as some function of the p-base depletion width but of the much faster growing n-base depletion width. As in Figure 3-11 and 3-12, the high voltage response is dominated by the voltage dependencies of the photo-transistor action of the thyristor. However, owing to the fact that most photons will pass completely through the depletion region, the net response in Figure 3-13 is about half that of Figures 3-11 and 3-12.

The light sources of Figures 3-5 to 3-7 are quite different. These spectra given in these figures represent Xenon flash tubes whose outputs cover a very wide range of wavelengths. Figures 3-5 and 3-6 represent the same flash tube operated at different voltage levels in order to stimulate a different ratio of infrared (IR) photons to visable band photons. The source in Figure 3-6, operating at half the voltage of that of Figure 3-5, has a higher photocurrent response as indicated by the comparison of Figure 3-9 to Figure 3-8. Figure 3-7 shows a different Xenon source with an even smaller IR energy and subsequently smaller photo-response as shown in Figure 3-10.

Although the best Xenon photo-response (Figure 3-9) is about half the 9000Å solid state laser (Figure 3-11), it would be a mistake to make a selection without considering the actual total power of these sources and the coupling problem in great deatil. The fact that the Xenon tube light output is isotropic makes it difficult to couple into low loss light pipe with its traditionally lower acceptance angles.

However, the high pulse energy available, namely joules per pulse, makes Xenon tube sources capable of driving hundreds of thyristors from a single source, providing the light intensity is sufficiently large. Reliability is not a serious problem if pulses are 5% of the explosion energy. For example, tube lifetimes of 10^7 pulses are might be expected. Moreover, the degradation is gradual and predictable. However, selection of one source or another requires too many system parameters to be stipulated to make a simple choice between the Xenon flash tube and the solid state laser. However, such sources have successfully been used to trigger our L1 thyristor (1) including firing with 10 feet of light pipe.

Light Pipe-Light Source Coupling Tests

Coupling experiments were carried out throughout the program. These were of two types. In one set of experiments, lenses and micropositioners were used to accurately and optimally (for the lens used) couple the light source to the light pipe. In the second set of experiments a simple, less sensitive and more rugged assembly was used with the aim being simplicity and low cost rather than high coupling efficiency.

In the first set of experiments, optical coupling using a lens or lenses between a solid-state laser and fiber-optic bundles was investigated in some simple systems. The experimental apparatus is shown in Figure 3-18. One source used was a Laser Diode Laboratories single-junction laser Model LD66. The emitting area of this unit is nominally 9 x 0.08 mils, (360 x 3.2 microns). The laser was focused on the optical fiber or fiber bundle either by a simple two-element condenser lens, (image or object distance approx. 33mm, f/1), or a more complex movie-projector lens system, (focal length approx. 55mm, f/1.6). The condenser lens system produced a relatively poor-quality unit-magnification image of the junction. The projection lens gave a much better image with resolution of the order of 2-line pairs-/mm for red light at the center of the field when used at 4-fold magnification or greater; however, the image quality deteriorated rapidly with lower magnification. Chromatic abberation was not a problem since the laser emits only a narrow wavelength band centered at 905mm.

All radiant power measurements were made with an EGG type SHS-100 Si diode operated in the biased mode in conjunction with a sampling oscilloscope that was also used to measure the laser drive current. The active diameter of the detector was 2.54mm, with sensitivity 0.6A/watt estimated for large angular-aperture conditions from the manufacturer's data. Filters were used as required to attenuate the incident power to ensure linearity of detector response.

With the laser operated at 40A peak current, the peak radiant power through the condenser lens system was 5.2 watts, and 5.4 watts for the projection lens system. Considering only the reflection losses at the four airglass interfaces, the transmission of the condenser lens system is estimated to be 0.7, implying 7.4 watts emission from the laser, in reasonable agreement with the manufacturer's claimed 8.0 watts minimum. The ratio of the detector responses for the two lens systems indicates 0.73 transmission for the projection lens system, a plausible value.

The focused laser emission just described was imaged on one end of a fiber bundle or on an individual fiber. Results for the emission emerging from the far end are summarized in Table 3-3. The Galite "1000" bundle was about twelve times the area of the "3000", and this in turn was about twelve times the area of the "Corguide" fiber. The "Corguide" fiber is about the same diameter as the individual fibers used in Galite "3000" bundles, and both have relatively small absorption losses compared to the "1000" fibers. The numerical aperture (NA) of both Galite bundles is large enough that all the laser emission could enter the fiber ends. (According to the manufacturer, 99% of the laser emission should enter a system with NA of 0.26 or larger.) Similarly, the image magnification used with the "Corguide" fiber reduced the angular spread so that all the incident energy could be accepted by the fiber. The tabulated power loss is in each case the ratio of the observed power emerging from a bundle to the estimated power from the beam incident within the circular area containing the fibers, (or the active area in the case of the single fiber).

In spite of its relatively large area, the Galite "1000" bundle has low output because of the high fiber attenuation in transmission through the 8 meter length, (about 7db). When used with the condenser lens system, the Galite "3000" bundle gave low output because the poor image quality caused much of the laser energy to miss the end of the bundle. The still-lower output from the single "Corguide" fiber results because only about 1/10 of the laser power falls on the 90 micron diameter active area even though the image quality is relatively good.

The second set of experiments involved the use of machined brass holders. Into one side is plugged the laser and into the other is plugged the light pipe termination. There is no attempt at focusing and no special modification of either the light pipe or the laser. Figure 3-19 shows one such brass block coupling arrangement capable of holding 14 lasers and 14 light pipes. The results, which show about .5 watts inserted into the light pipe, indicate that this arrangement may be a suitable one. A second test was performed with furcated cables consisting of a 10 branch light pipe bundle. The trunk end was plugged into the same laser. The output at the end of each of the 10 branches (each branch was a Galite 3000 T19 light pipe) was measured with a PIN detector and found to lie between 50 and 70ma.

Other experiments were performed to incorporate some degree of redundancy by using two sources, for example, to fire the thyristor. With the furcated 10 branch cable, it is possible to use 10 sources to fire a single thyristor provided the light active area of the thyristor is as large (40 mils) as the trunk end of the light pipe bundle.

All of the room temperature laser turn-on tests which follow in this report used the coupling apparatus shown in Figure 3-19. In most cases, if furcated light pipes were used, the trunk end was inserted into the brass coupler. This allowed one of the furcated ends to be used to monitor the photo-signal incident on the thyristor.

Table 3-1

LIGHT-PIPE COMPARISON LOSSES IN db

LIGHT PIPE	CORE/CLAD LOSS	PACKING FRACTION LOSS	NUMERICAL APERTURE LOSS	60' TRANSMISSION LOSSES AT 8200Å	9000Å	9500Å	END LOSSES
Galite 3000 *	1.94	1.2	6.4	1.8	1.8	2	~ 3
Galite 2000*	.82	.71	3.6	11	22	14	~ 3
Corning B-19**	1.11	1.2	10	.54	.70	1.8	~ 3
Dupont S10†	1.42	~ 1	5.3	.18	.15	.55	~ 3

* Available in water resistant, carbon free jacketing.

† Plastic fiber and cladding are rated only to 90°C. Also, high field qualities are unknown.

** PVC Jacket is not suitable for high field, high humidity environment.

Table 3-2

LED LIFE AND PERFORMANCE TEST

Test No.	Temp. (^{o}C)	Time (hrs.)	Total # of Failures	Relative Output
1	23	1	0	1
2	76	1.5	0	.63
3	108	2	0	.46
4	124	1	0	.36
5	153	1.5	0	.25
6	25	17	0	.87
7	75	.5	0	.53
8	106	.5	0	.38
9	122	12	0	.32
10	122	71	1	.31
11	148	7.5	1	.22
12	24	15	2	.84
13	75	2.5	2	.53
14	100	.5	2	.40
15	125	29	2	.30
16	125	39	2	.29
17	125	77.5	2	.30
18	125	19	2	.29
19	25	24	2	.79
20	72	24.5	2	.53
21	102	7.5	2	.39
22	122	120	2	.32
23	100	23	2	.40
24	75	.5	2	.54
25	25	1	2	.82
26	116	15	2	---
27	150	5.5	2	.22
28	26	26	2	.83
29	135	72	2	.26
30	25	16	2	.81

Total Hrs. - 633

I_F=4A, 5μS, 667pps

Table 3-3

LASER-LIGHT PIPE COUPLING TEST
(the experimental setup is shown in Figure 3-18)

Mfr. type	Number of fibers	N.A.	Overall bundle area (cm^2)	Estimated power loss (db)	Magnification/ optics	Measured power output (watts)
Galileo Type 1000 (3 meters long)	212	0.66	$\approx 1 \times 10^{-2}$	≈ 11	1:1 condensers	0.4
Galileo type 3000/7T (9 meters long)	7	0.48	$\approx .85 \times 10^{-3}$	≈ 5	1:1 condensers	0.3
				≈ 4	$\approx$1:3 proj. lens	1 1/4
Corning "Corguide" (1/3 meter long)	1	0.16	$\approx .6 \times 10^{-4}$	≈ 2	$\approx$1:4 1/2 Proj. lens	1/3

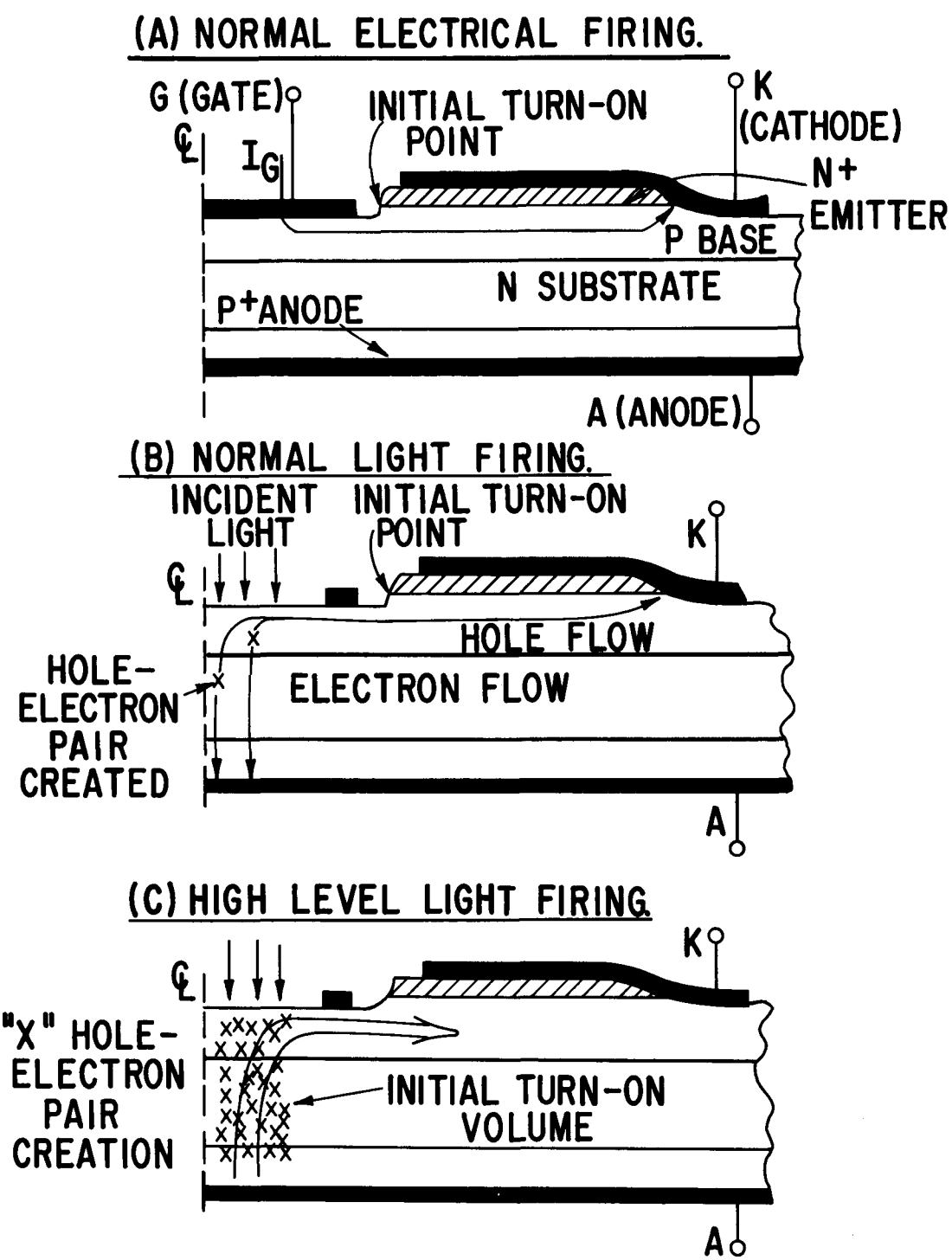


Figure 3-1. Illustration of thyristor turn-on process. (a) Normal electrical firing. Current flow from G. to K through the p-base resistance biases the initial turn-on line to cause electron injection. (b) Hole-electron pairs are separated by the junction field and flow as current from A to K as marked, also forward biasing the n+ emitter. (c) So many hole-electron pairs are created that the effective resistivity of the irradiated region is affected without the injection of electrons from the cathode or holes from the anode.

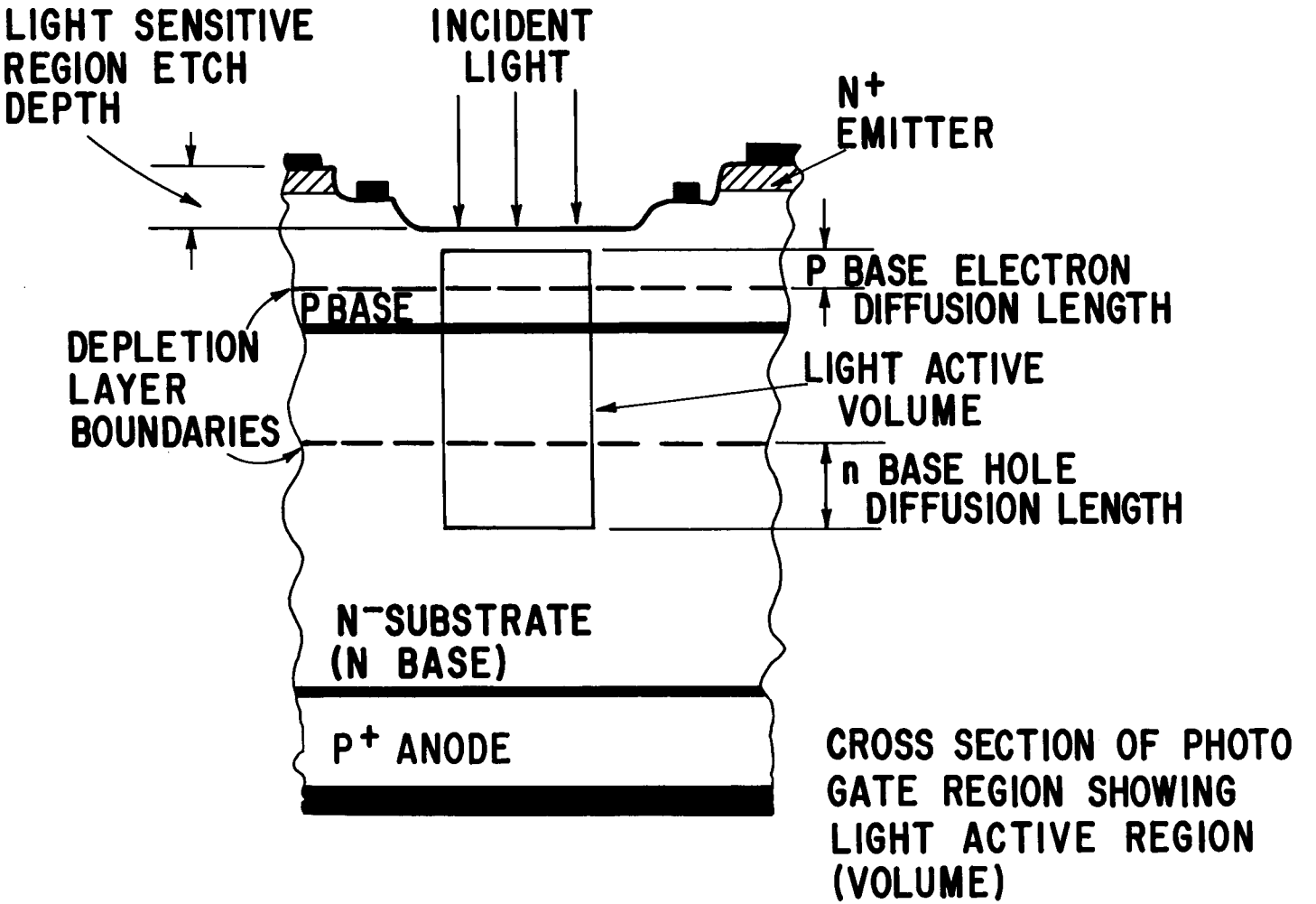


Figure 3-2. Enlarged cross-section view of a typical ight-fired thyristor showing the "light-active volume." Only hole-electron pairs created in that volume are effectively collected.

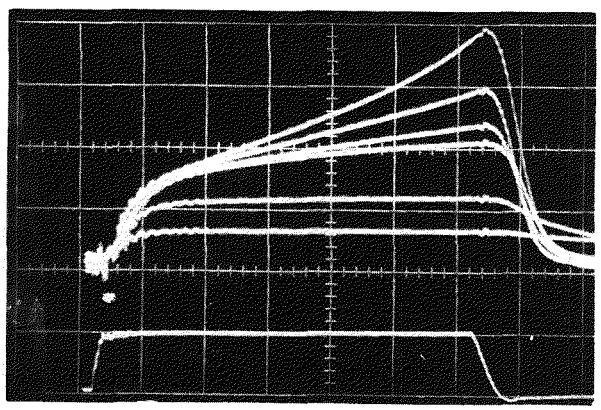


Figure 3-3. Photo-induced cathode current for different forward blocking voltages (V=5, 15, 30, 50, 200, and 400 volts).

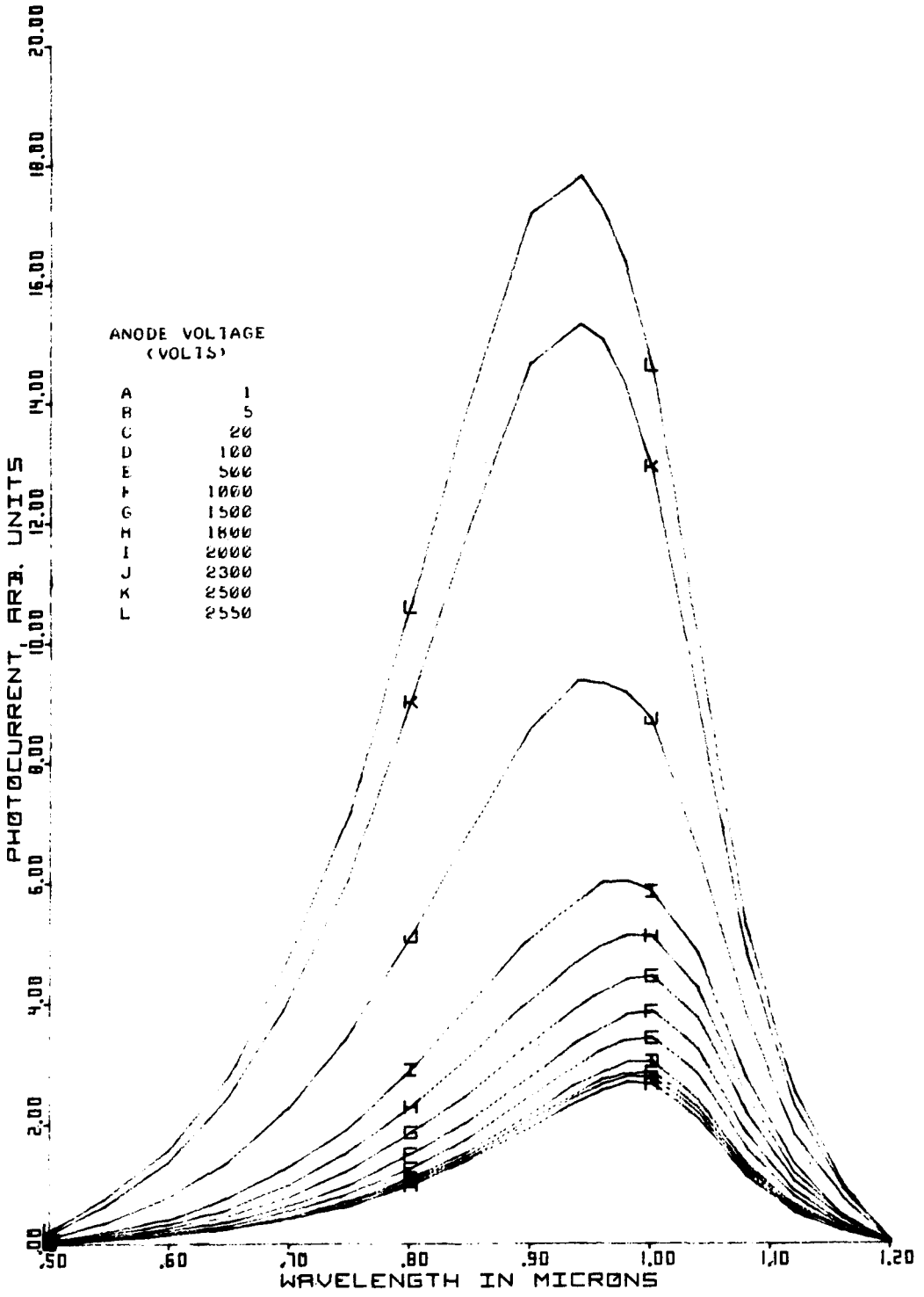


Figure 3-4. Photo-response of device 3. The photo-sensitive area was bare silicon, etched down 28 microns. (Original junction depth approximately 75 microns.)

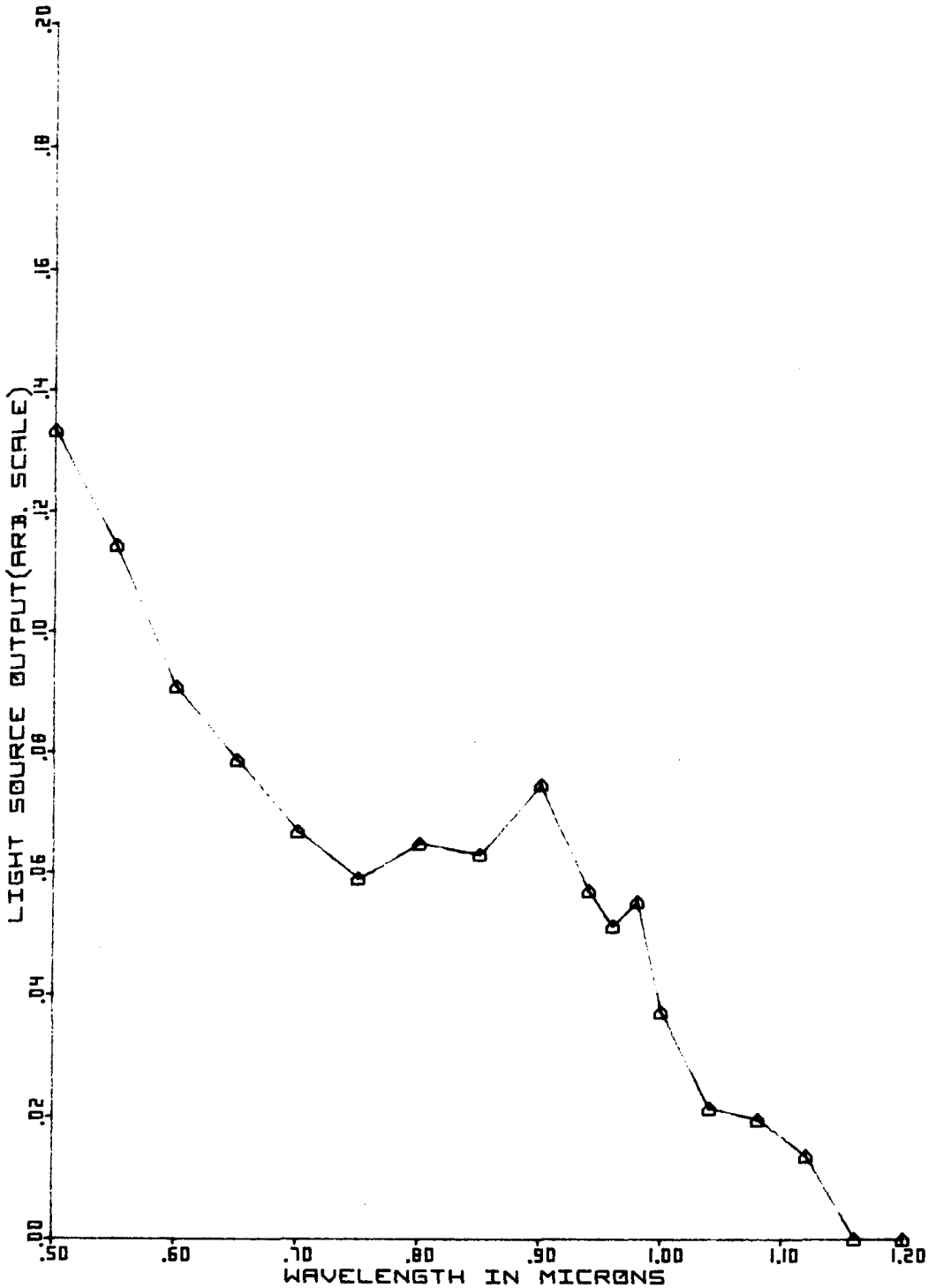


Figure 3-5. Output spectrum of an EGG Model FX-38 C-3 Xenon flash tube at 1400 V (51 μf).

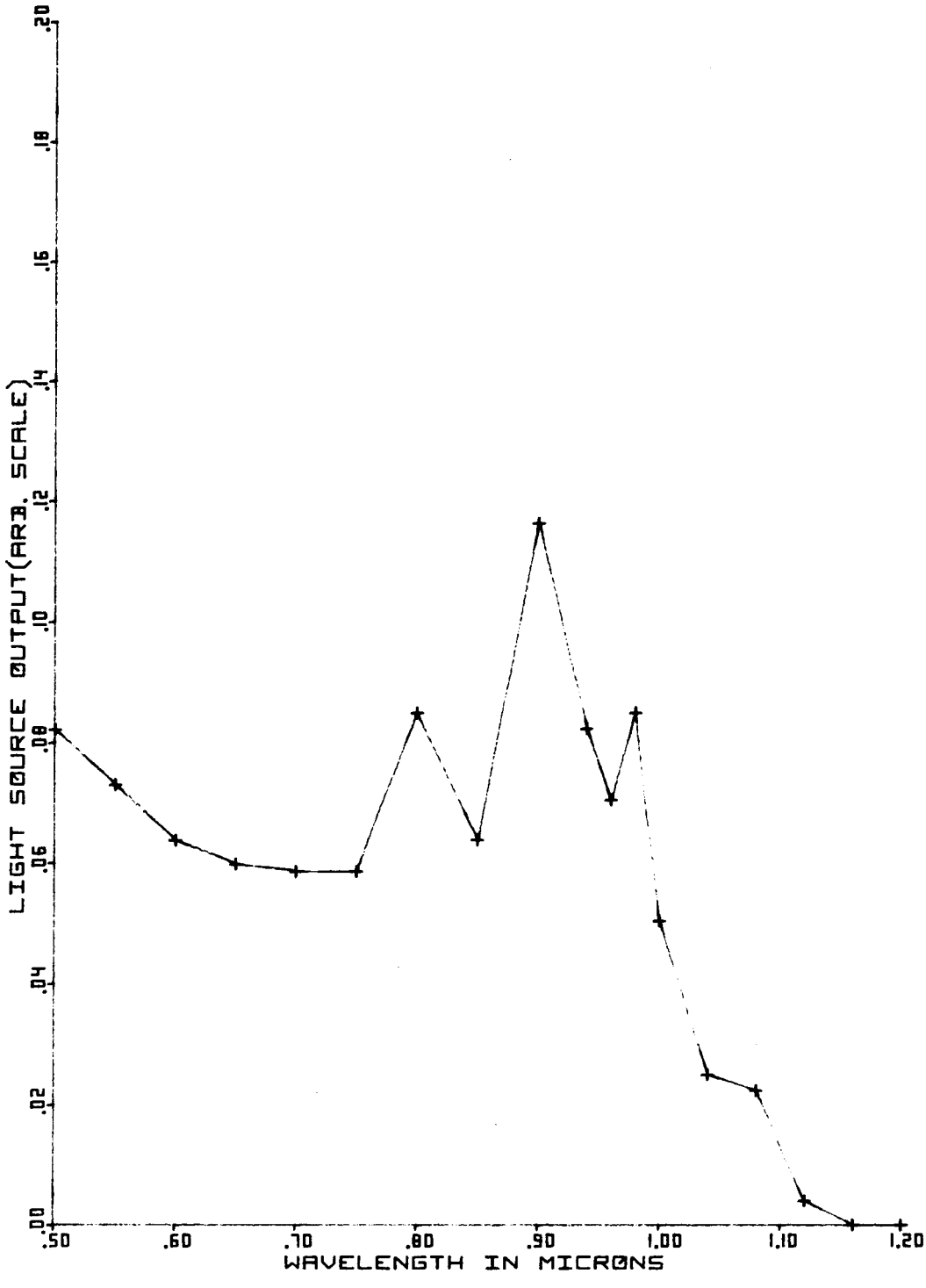


Figure 3-6. Output spectrum of an EGG Model FX-38 C-3 Xenon flash tube at 700 V (205 μf).

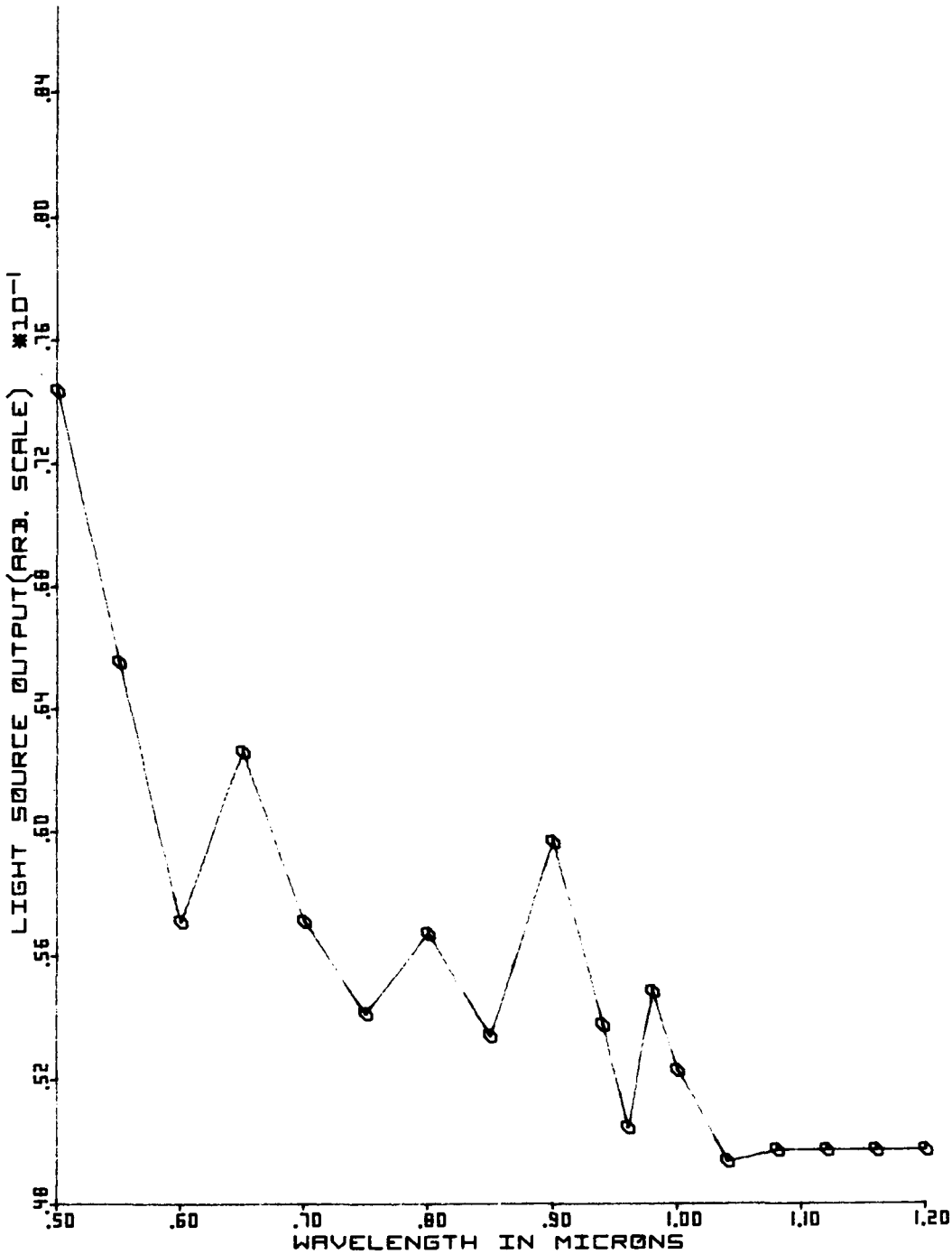


Figure 3-7. Output spectrum of an EGG Model FX-76 Xenon flash lamp.

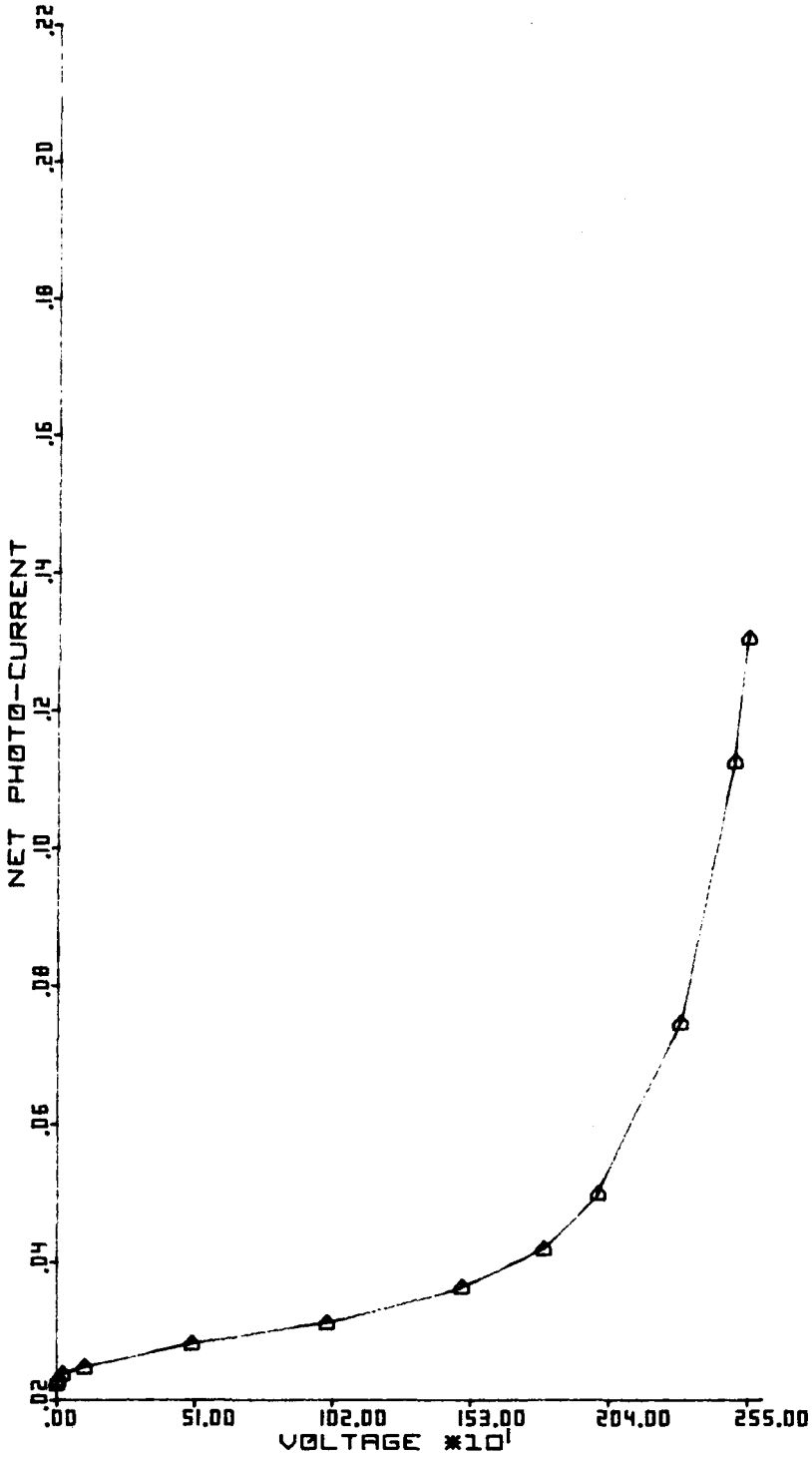


Figure 3-8. Photoresponse of a typical L1A, L1B, or EPRI-GE1 thyristor to unit of power from the light source shown in Figure 3-5.

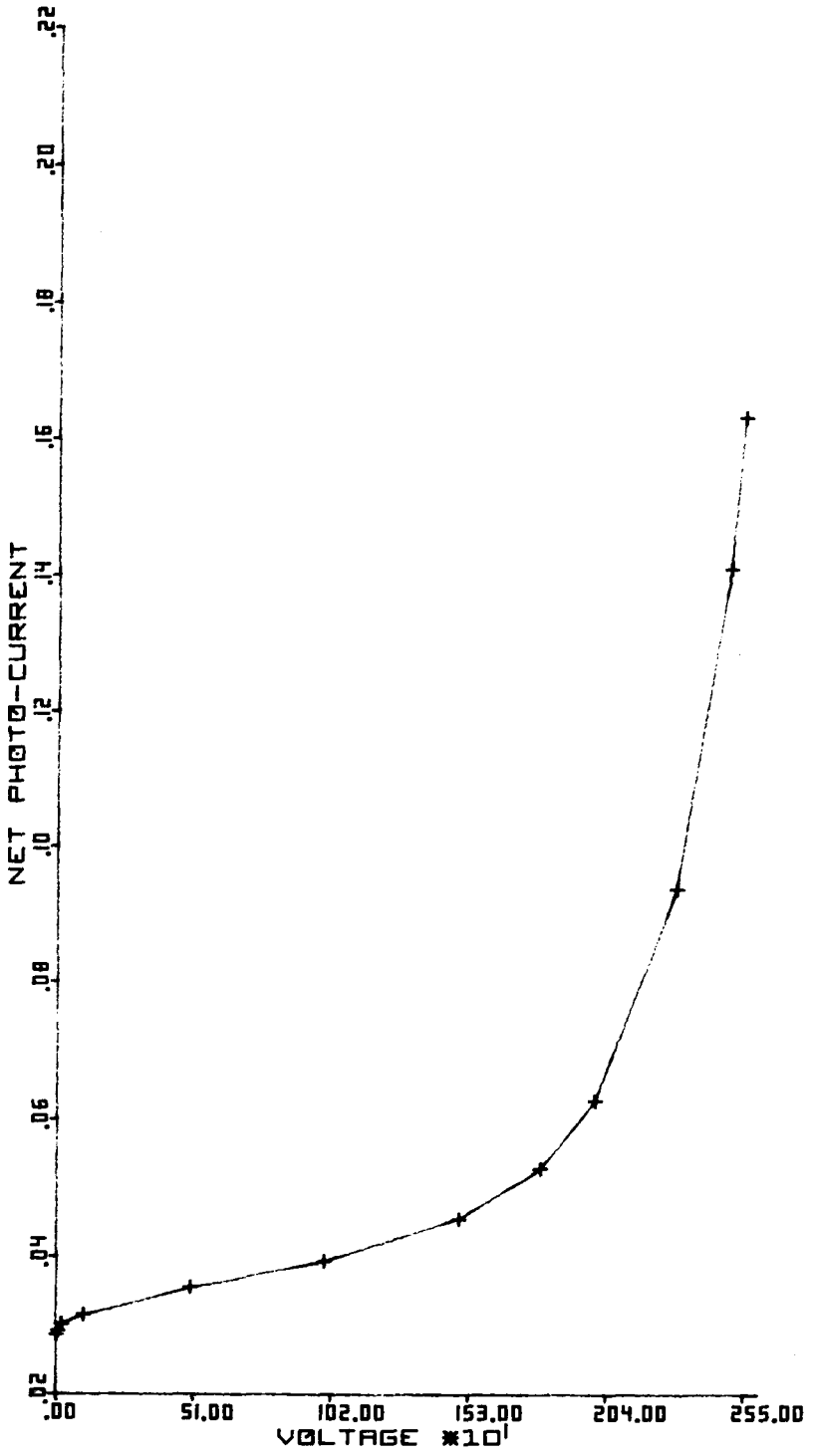


Figure 3-9. Photoresponse of a typical L1A, L1B, or EPRI-GE1 thyristor to unit of power from the light source shown in Figure 3-6.

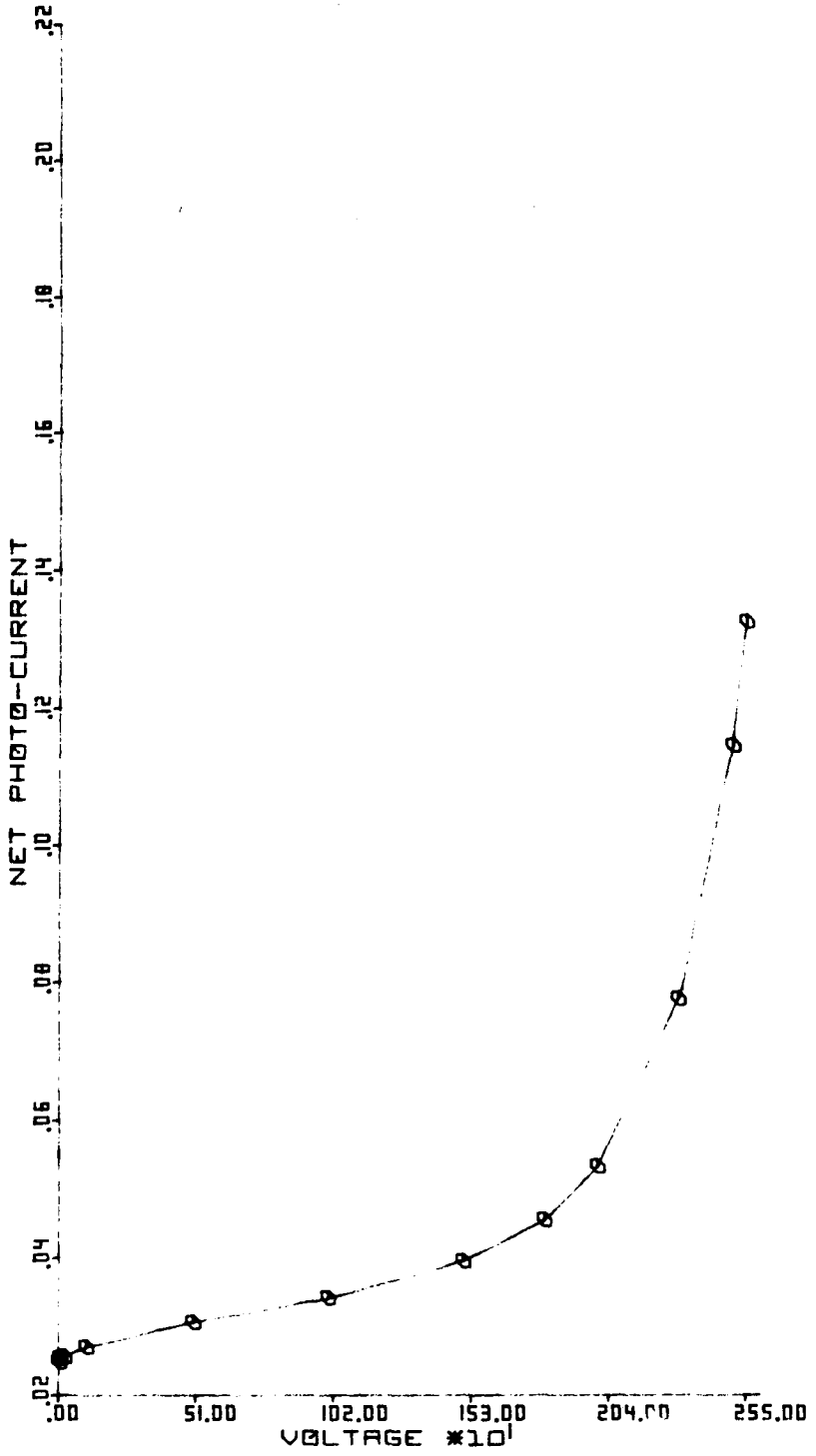


Figure 3-10. Photoresponse of a typical L1A, L1B, or EPRI-GE1 thyristor to unit of power from the light source shown in Figure 3-7.

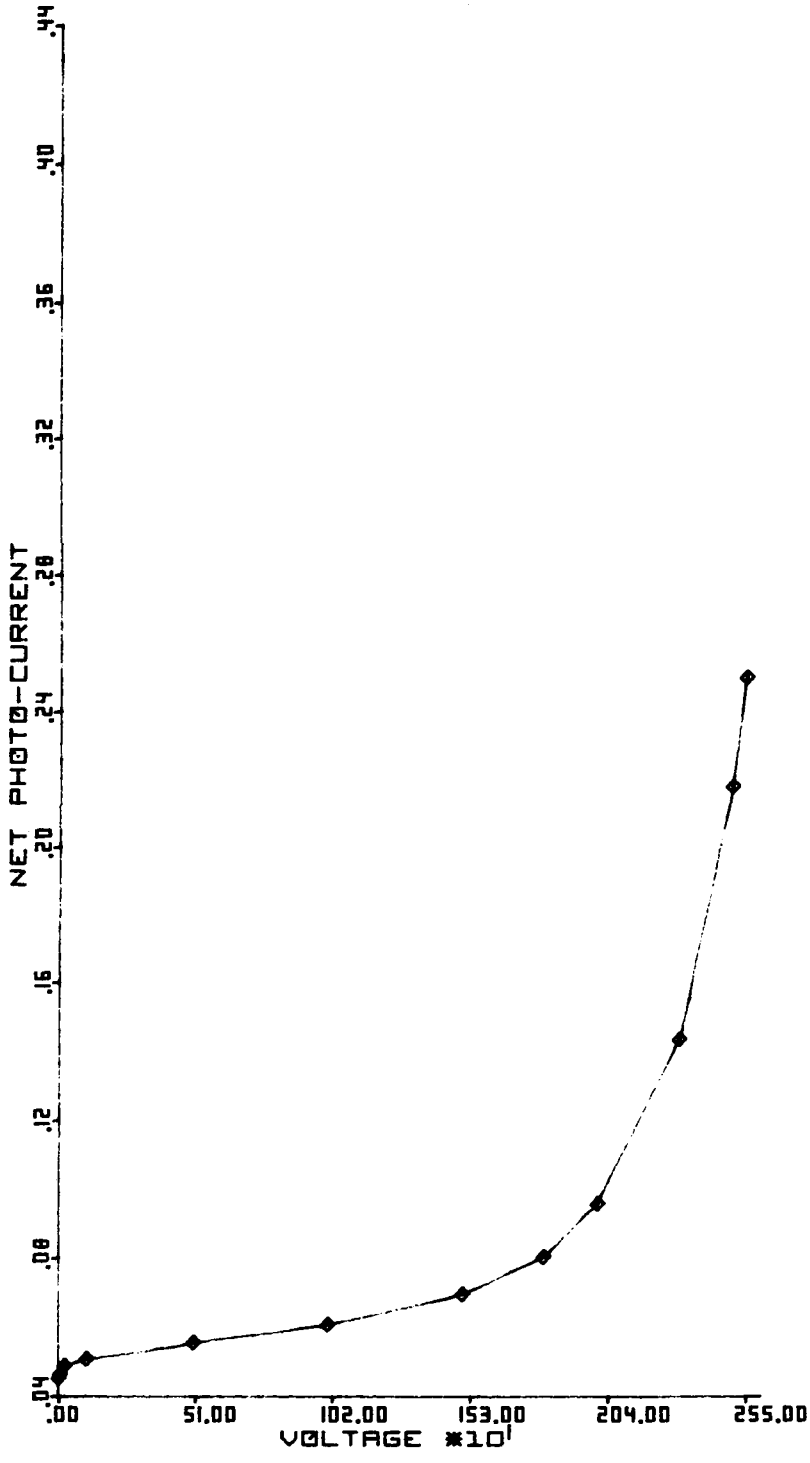


Figure 3-11. Photoresponse of a typical L1A, L1B, or EPRI-GE1 thyristor for a 9000Å laser source of unit power.

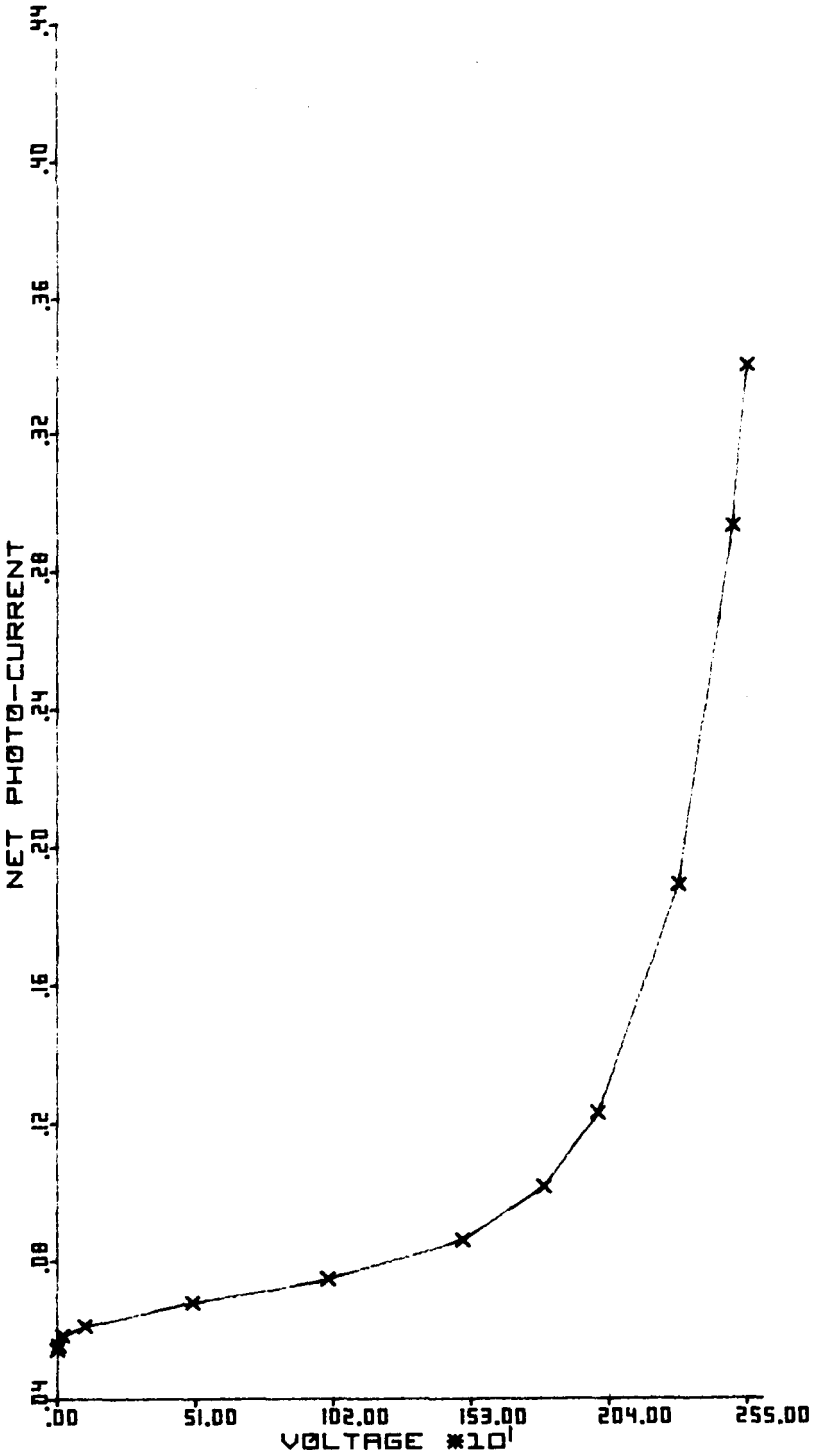


Figure 3-12. Photoresponse of a typical L1A, L1B, or EPRI-GE1 thristor for a 9450Å LED light source of unit power.

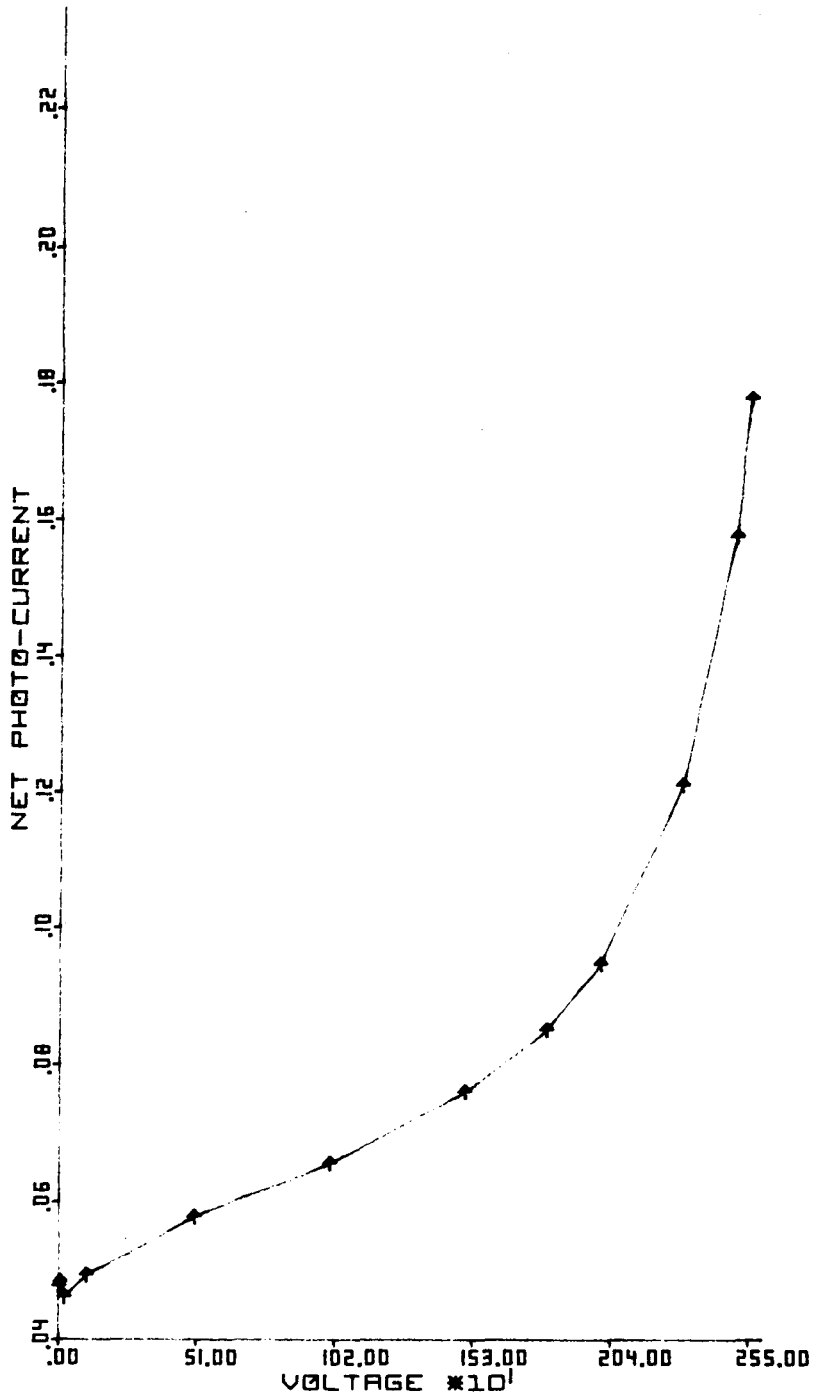


Figure 3-13. Photoresponse of a typical L1A, L1B, or EPRI-GE1 thristor for a 1.06μ YAG laser light source of unit power.

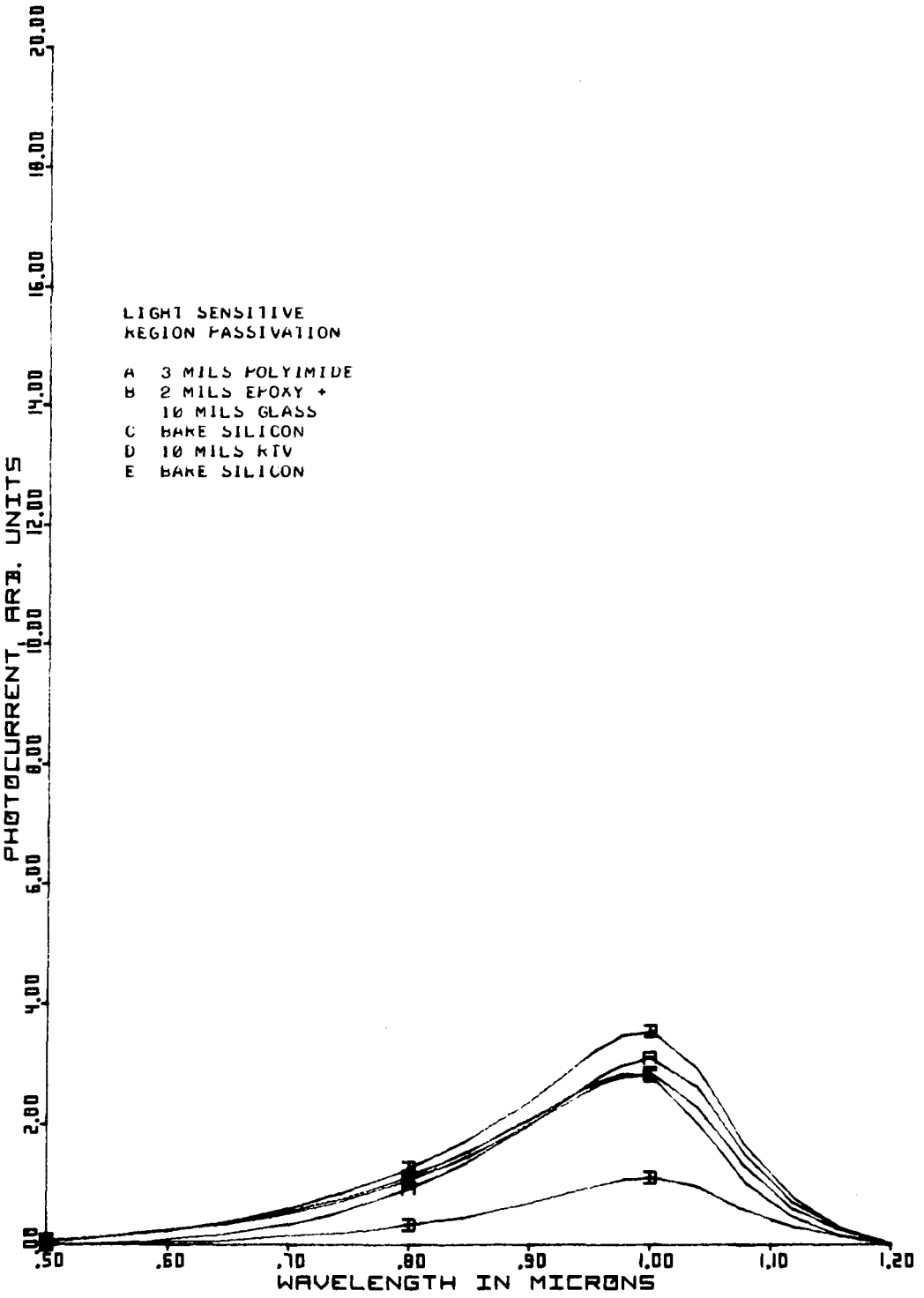


Figure 3-14A. Photoresponse for different surface passivations. Anode voltage = 20 volts.

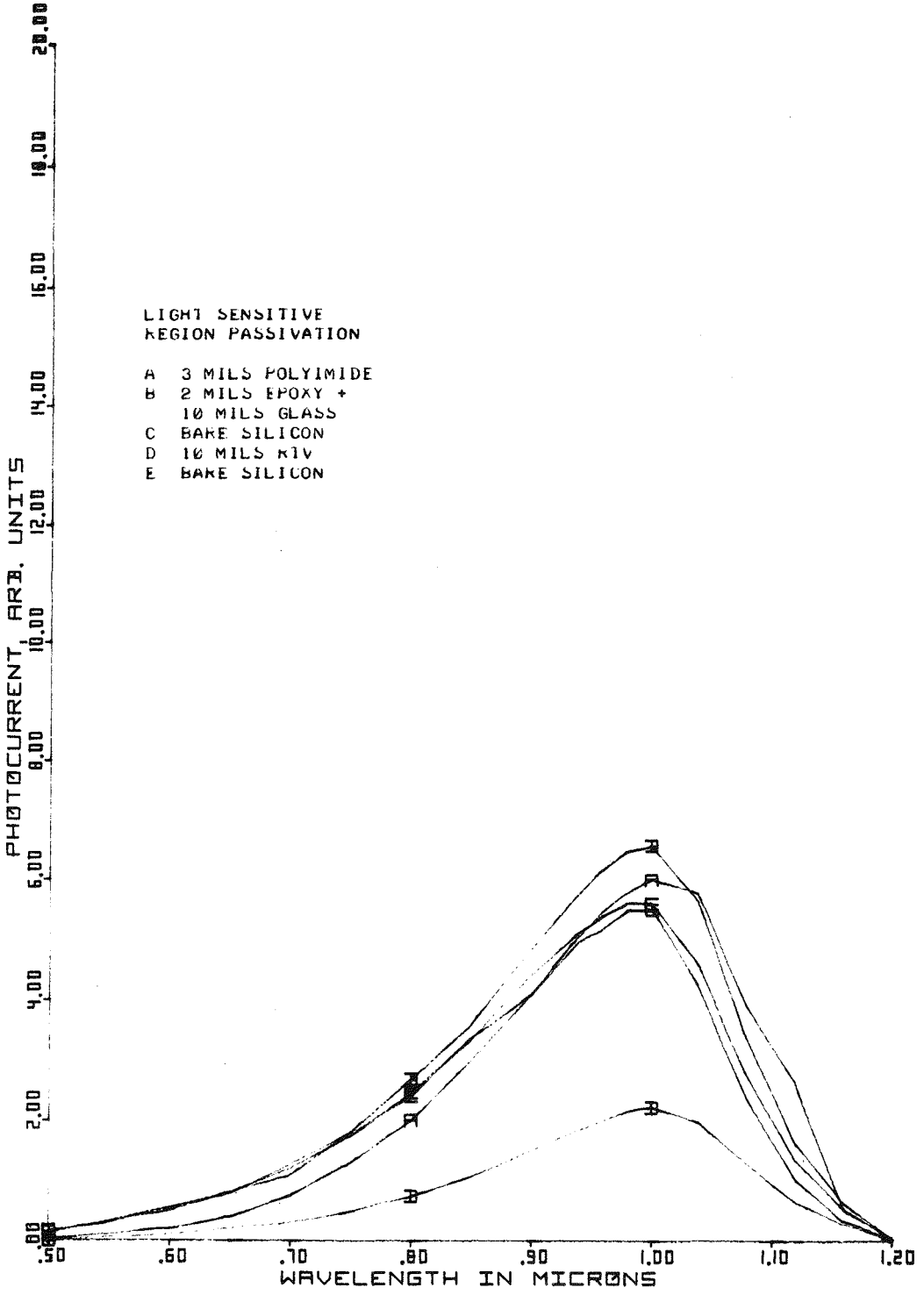


Figure 3-14B. Photoresponse for different surface passivations. Anode voltage = 2000 volts.

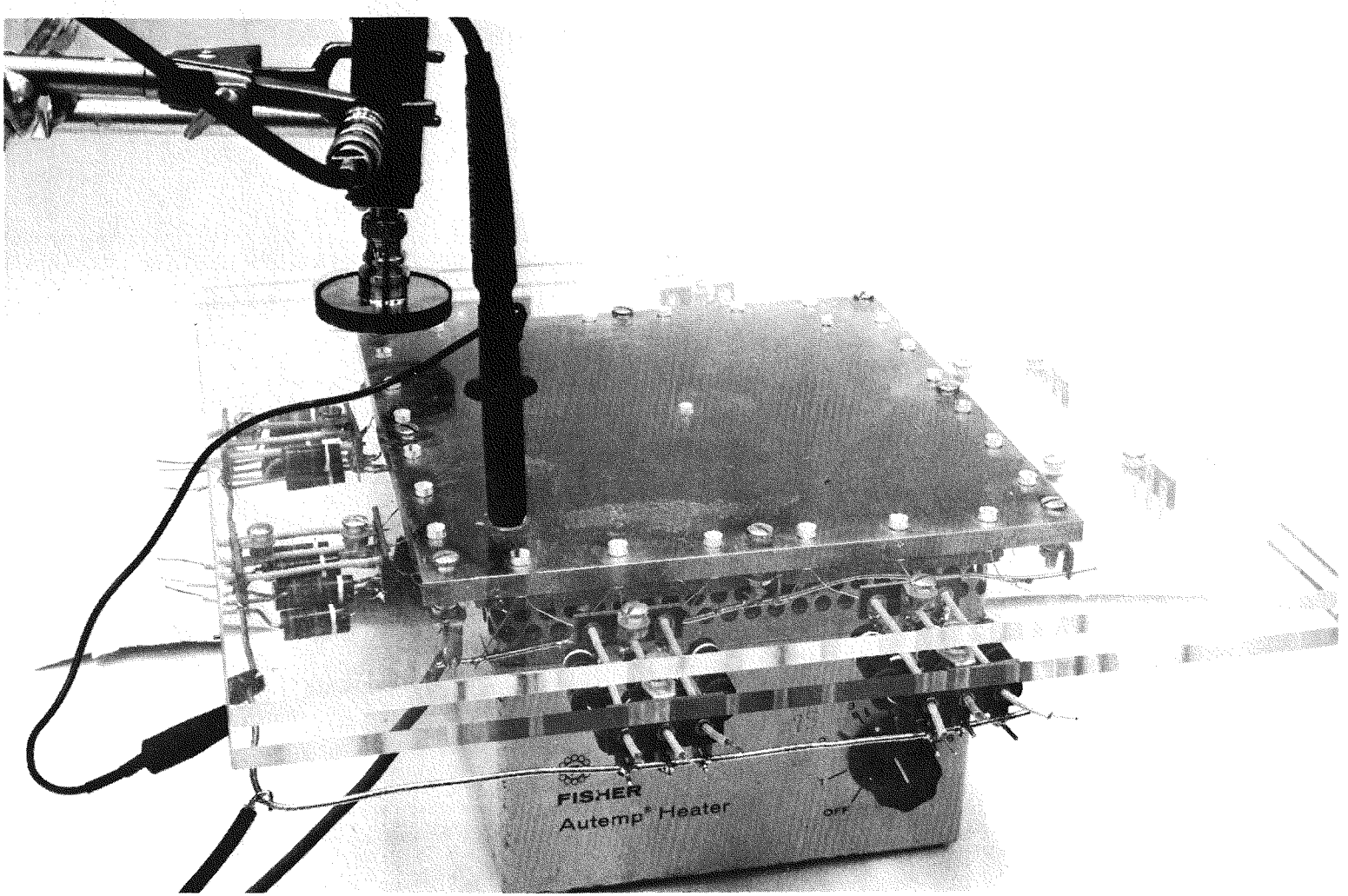


Figure 3-15. Photograph of apparatus for testing up to 24 solid-state light sources at elevated temperatures.

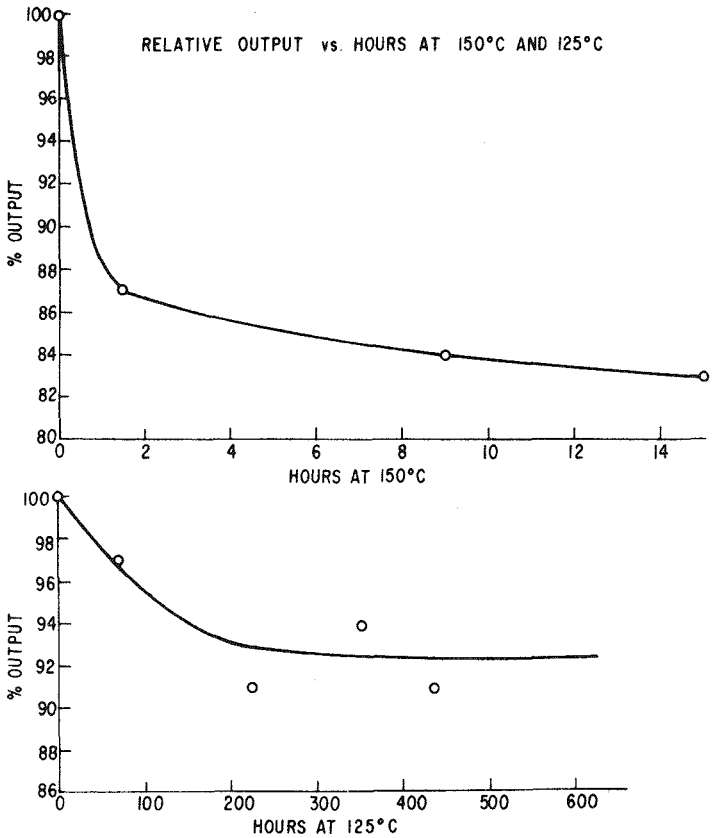


Figure 3-16. LED output after operation at 125°C and 150°C.

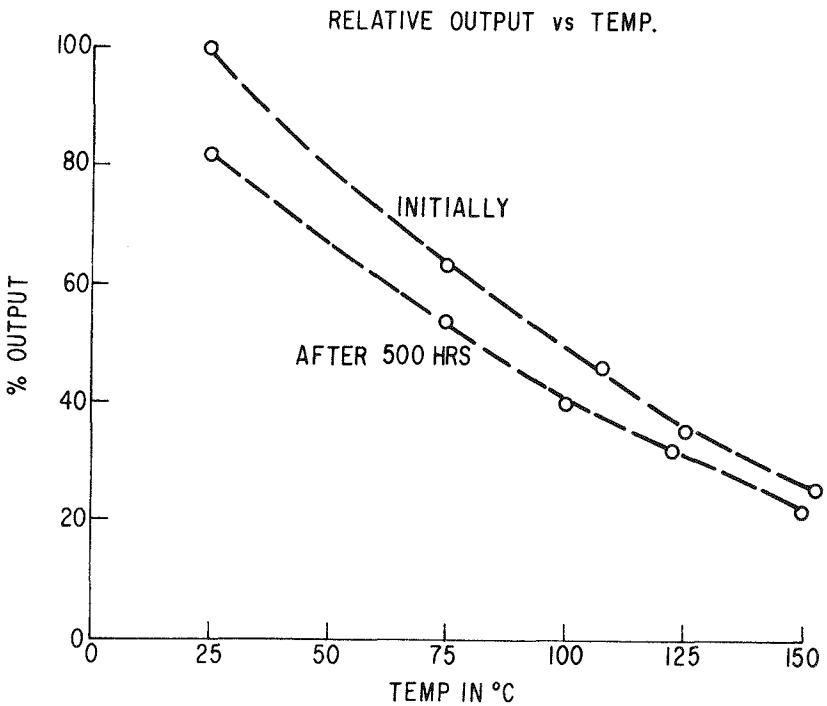


Figure 3-17. LED output as a function of temperature before and after accelerated life testing.

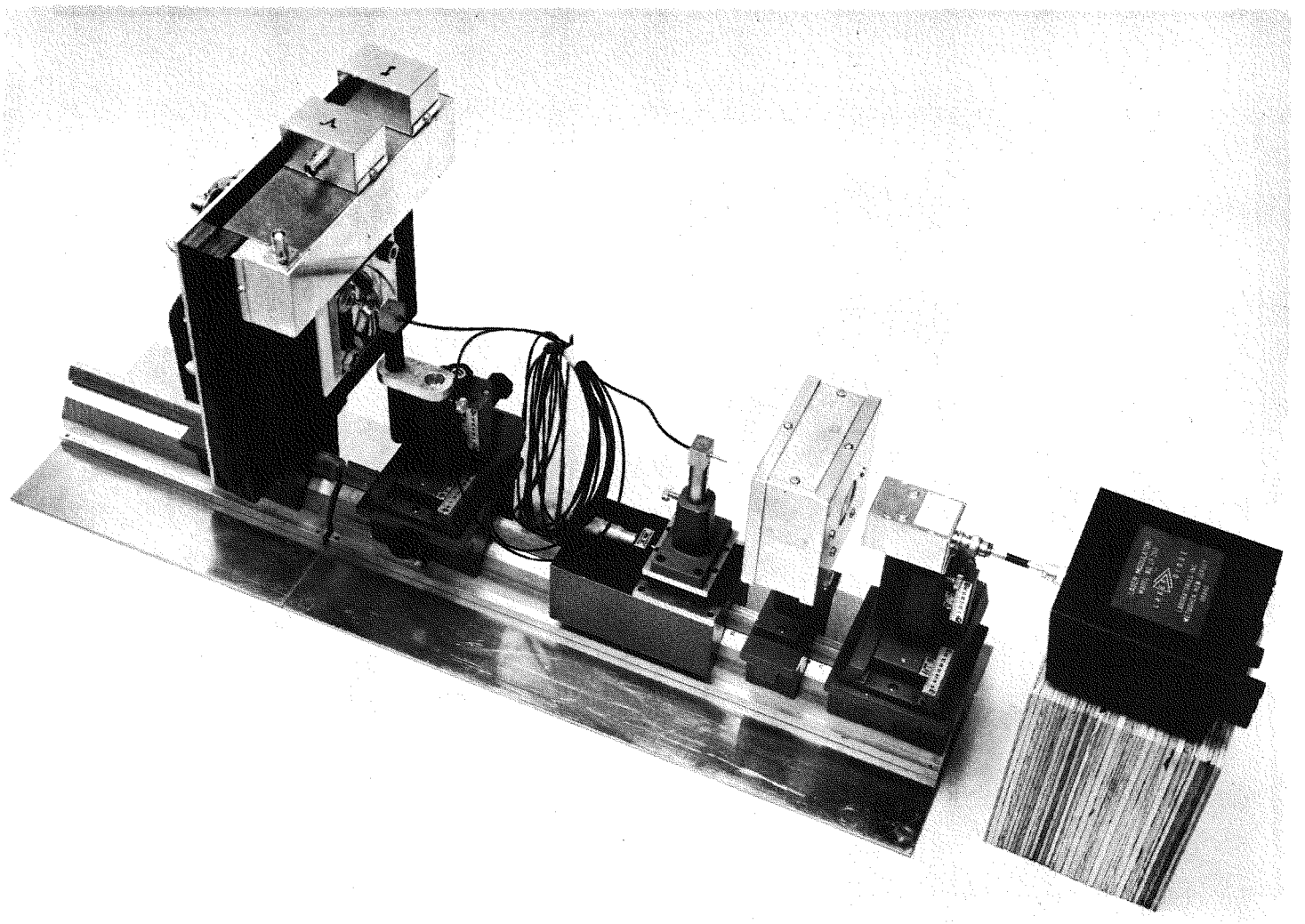


Figure 3-18. Photograph of light source-light pipe test system.

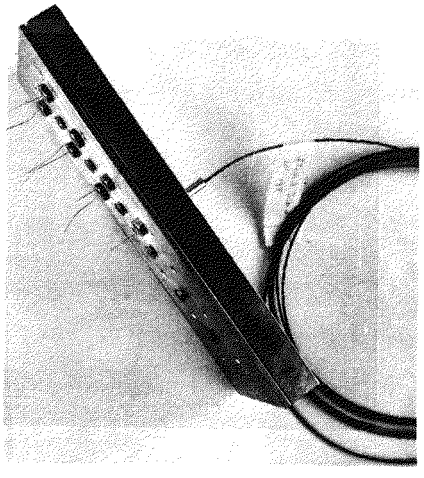


Figure 3-19. Plut-in laser-light pipe coupling arrangement. The block shown in capable of holding 14 laser-light pipe combinations.

Section 4

DESIGN OF THE EPRI-GE1 LIGHT FIRED THYRISTOR

BASIC DESIGN GOALS

The basic light triggered thyristor design is dictated by two circumstances; the first being the cost and difficulty in bringing an appropriate high intensity light signal to the packaged semiconductor device, and the second being the high dynamic performance level required by the HVDC thyristor. These circumstances have lead to the adoption of an amplifying gate type design in which two amplifying gates are used rather than one. These two amplifying gates are termed the gate thyristor or gate stage and the pilot thyristor or pilot stage. The device as a whole is referred to as the EPRI-GE1 device.

Because of the light intensity available from economical solid state light sources, it is desirable that the gate stage be designed with a gate threshold current level of less than 5ma. To lessen the delay time for subsequent turn-on of the pilot stage, it is also desirable that the pilot thyristor be less than a factor of 10 less sensitive with a gated threshold of about 20 to 40ma. The gated threshold level of the main emitter is not a critical design parameter. Hence, its design is dictated chiefly by dV/dt and di/dt considerations.

Considerations of the constraint imposed by device dV/dt capability and the need for dV/dt turn-on self-protection have pointed to dV/dt thresholds of approximately 2000, 3000, and 4000V/μsec for the gate, pilot, and main thyristor stages, respectively. This implies a device dV/dt capability of 2000V/μsec and a normal (gate-pilot-main) turn-on sequence should this quantity be exceeded.

The following sections outline the process by which this first design of the EPRI-GE1 device was reached. The process includes two setps; the first is an approximate design based on first order design equations, and the second is a more exact calcualtion using the computer

program to be described later in this report.

APPROXIMATE DESIGN EQUATIONS

As indicated above, the first step in the design process is the generation of an approximate design using closed form design equations (4-1) to (4-9). Equations (4-1) and (4-2) are the appropriate equations for calculating the photo generated current level necessary for threshold turn-on:

$$I_g = \frac{2\pi\sigma_E V_{th}}{\ln(r_o/r_{in})} \qquad (4\text{-}1)$$

or

$$I_g = \frac{L\sigma_E V_{th}}{r_2 - r_1} \qquad (4\text{-}2)$$

where σ_E is the net effective conductance of the p base and V_{th} (.7 volts) is the threshold voltage for turn-on. Equation (4-1) applies to the gate and pilot thyristor designs of Figure 4-1 where r_o and r_{in} refer to the outer and inner emitter dimensions. Equation (4-2) applies to the main thyristor design in Figure 4-2 where L is the length of the turn-on periphery and $r_2 - r_1$ is the distance from the turn-on periphery to the first row of emitter shorts.

The following equations apply to the dV/dt turn-on condition at the turn-on peripheries of the various thyristor stages:

$$dV/dt \approx \frac{4V_{th}\sigma_E}{C_o(r_o^2 - r_{in}^2)} \frac{F_2}{F_1F_3F_4} \qquad (4\text{-}3)$$

$$dV/dt \approx \frac{V_{th}\sigma_E L}{C_o A\ (r_2 - r_1)} \frac{F_2}{F_1F_3F_4} \qquad (4\text{-}4)$$

V_{th} and σ_E are the same as in equations (4-1) and (4-2) as are r_o, r_{in}, r_1, r_2, and L. A is the area enclosed by the main emitter turn-on periphery and C_o is the junction capacitance for a one cm^2 area at the breakdown voltage. F_1, F_2, F_3, and F_4 are correction factors which will be described shortly.

Equation (4-5) below applies to dV/dt turn-on in the shorted region of the emitters.

$$\frac{dV}{dt} \approx \frac{4V_{th}\sigma E}{C_O\left[2r_{12}^2 \ln \frac{r_{12}}{r_s} - r_{12}^2 + r_s^2\right]} \qquad (4\text{-}5)$$

Here r_{12} is one half the intershort spacing and r_s is the short radius.

In all of the equations applying to the dV/dt turn-on threshold, four important correction factors, F_1, F_2, F_3, and F_4, have been included. These correction factors are derived based on the assumption that, for a given dV/dt design target specification, a ramp voltage from zero volts to the breakdown voltage is applied (in this case $\geq$ 2600 (rated voltage is 2600 volts). The dV/dt current supplied by this signal lasts $V_{BR}/(dV/dt)$ seconds and is not constant since $C \propto 1/\sqrt{V}$ for V greater than a few volts. This results in a capacitance correction factor of F_1.

$$F_1 = C_{Av}/C(V_{BR}) \simeq 2 \qquad (4\text{-}6)$$

The second correction factor, F_2, applies to the size of gate current needed to trigger the device for a gate pulse proportional to C_{Av}/ dV/dt lasting only $V_{BR}/(dV/dt)$ seconds. The shorter this gate pulse, the more current it takes to fire the thyristor. Correction factor 2 is defined as follows:

$$F_2 = I_G \text{ (pulse length } = \infty)/I_G \text{ (pulse length } = V_{BR}/(dV/dt)) \qquad (4\text{-}7)$$

Where F_1 would tend to decrease the dV/dt rating, F_2 would tend to increase this rating. The amount above threshold needed for different pulse lengths to cause turn-on can be determined experimentally.

$$F_3 = \frac{I_{G1} \text{ (threshold at } 25^\circ C)}{I_{G2} \text{ (threshold at } T^\circ K)} \simeq \left(\frac{T}{298}\right)^{2.7} \qquad (4\text{-}8)$$

At 125°C the correction factor is 2.18.

Correction factor F_4 relates to the effect of the built-in transistor gain of the lower 3 junctions:

$$F_4 \approx \frac{1}{1 - \alpha_2 M} \qquad (4\text{-}9)$$

Note that α_2 is the current gain of the lower P^+N^-P transistor, and M is the avalanche multiplication factor. In these calculations, $M \cong 1$ except for voltages within 100 or 200 volts of the breakdown voltage. Generally, current gain, α_2, is about one half.

It will also be appreciated that factors F_2, F_3, and F_4 are also important when predicting the gating power level and pulse length required from the light source.

DESIGN COMPUTER PROGRAM

Figure 4-3 shows the central gate region of a single amplifying gate thyristor in radial cross section along with the usual simple electrical analog circuit for calculating turn-on potentials. Turn-on occurs when the current in D1 (or D2) reaches a critical value. Usually in simple models, instead of using this current criterion, a voltage criterion is used in which the voltage across R_p (or R_m) is treated as the critical value. Turn-on is assumed to occur when the voltage reaches about 0.7 volts. This is a convenient approach for computational purposes particularly if the diode is assumed to be ideal, i.e., open circuit up to the critical voltage and short circuit thereafter. However, the actual turn-on threshold is dependent on the injection properties of the upper n^+-p_{base} structure with turn-on occurring when the injected electron current is sufficiently large to maintain a build up of carriers in the depleted n_{base} region. Turn-on can also be at a particular point or over a whole area depending on the distribution of potentials and resultant injection currents generated by the gate signal. For this reason, calculations to determine a suitable gate structure for a high performance light triggered thyristor requires that geometrical effects be carefully considered.

To do this, a computer program, already in operation for calculating turn-on thresholds for simple one dimensional or radial geometries, which calculates n^+-p_{base} voltage drop as a function of gate current, photocurrent, dV/dt current, or leakage current has been modified to allow for some important two and three dimensional effects. Figure 4-4 shows an example of the improved electrical analog model which can be solved at this point. Note the ability to deviate from one dimensional geometries which, for example, will allow base voltage distribution due to the emitter-base short patterns to be taken into account. These shorts provide a path to ground for gate currents and locally distort the turn-on thresholds. Also included in this model is the n^+-p_{base} current. This current is most important from two points of view. First, this current is the one which initiates and maintains the turn-on. Secondly, this current reduces the n^+-p_{base} voltage across R_p (and R_m) as it begins to flow through the diode impedance paths D1 (and D2) to the cathode. Furthermore, the impedance of these diodes is highly dependent on the local p_{base} voltage, giving rise to a nonlinear problem impossible to solve exactly in closed form.

Figure 4-4 shows some of the topological complexity that this program can handle in turn-on situations. For example, Fig. 4-4(a) shows an n^+ emitter region, a bare p_{base} region, and two metallizations which are more or less of arbitrary shape. As shown in Fig. 4-4(b), the model is three dimensional in scope. The vertical current flow is approximately accounted for in the n^+-p_{base} junction by diodes and in the n_{base}-p_{base} junction by current sources. These latter are used to model leakage current, dV/dt current, and photocurrent that is rectified by the n_{base}-p_{base} junction.

Typical results of such a calculation are shown in Fig. 4-5. Note that both the n^+ emitter geometry and the base resistivity are two dimensional due to a patterned n^+ etch. The more important results of the calculation show, for example, what the distribution of voltage is for the n^+p_{base} junction for $V_G = 0.6$. It is also shown that for $V_G = 0.8$, part of the gate current is flowing to the cathode (1) via the base but not under the emitter, (2) via the base under the emitter, and (3) via the n^+-p_{base} junction. It is hoped that subsequent modifications will eventually allow for more than one emitter

area to be included and for a more generalized form of current injected through the n_{base}-p_{base} junction.

Figure 4-6 shows the electrical analog of an individual node of an improved model under consideration. There are three added factors to be considered. First is the inclusion of a current $G_4 * I_D$ where G_4 is the thyristor four layer current gain. Second is the inclusion of the transistor gain, G_3, of the lower p-n-p layers to be applied to leakage current, photocurrent, and dV/dt current. These gains would be current dependent functions. The third improvement is the inclusion of three separate emitter areas, corresponding to the main thyristor emitter region, the pilot thyristor region, and the gate thyristor region of a double amplifying gate thyristor. Simultaneous calculations encompassing these three critical areas would allow a proper design which ensures turn-on at the inner gate thyristor with adequate margin.

FINAL DESIGN OF THE EPRI-GE1 THYRISTOR

Using the previous design equations with $\alpha_2 = 0.5$ and F_2 as defined in Figure 4-7, photocurrent and dV/dt current threshold levels were calculated for the gate thyristor and the pilot thyristor designs shown in Figure 4-1. The numerical values are shown in Table 4-1 along with similar data for the main thyristor depicted in Fig. 4-2.

The next step in the design procedure required the application of the computer calculation just described to assess special design features. There were three main concerns all arising from the fact that equations (4-1) to (4-5) apply to simple unshorted radial geometries while, with the exception of the gate thyristor, all of the emitters are shorted. The first concern was, therefore, to establish the uniformity of the base voltage at the turn-on periphery for a given gate condition (or dV/dt) condition. Figure 4-8 shows the computed voltage distribution at a short on a typical section of the main emitter turn-on periphery.

The other two problem areas also lie on the turn-on periphery of the main emitter. These regions of concern are the inner and outer corners of the arm structure. Figures 4-9 and 4-10 show the potential distribution in these regions. It is desirable that the voltage of the turn-on periphery in these special regions should be either less than or equal to the voltage on the rest of the turn-on periphery. This, at least, ensures that the turn-on will not occur in these regions alone. The simplest way in which to ensure that this condition is met is to locate the n^+ emitter edge so that it approximately follows a particular equipotential line. In Fig. 4-9, the turn-on periphery is at ~.17 volts with the gate voltage equal to .4 volts. It then follows that the .17 volt equipotential is suitable from a design standpoint.

Figure 4-10 shows the voltage distribution around a short in the main emitter as calculated with the computer program for a current density of $1A/cm^2$. The maximum induced voltage is ~.4 volts implying a dV/dt (uncorrected for F factors) of 35,000 V/μsec value.

Individual masks entitled EPRI-GE1-1 (for the pre-etch step), EPRI-GE1-2 (for emitter definition), and EPRI-GE1-3 (for the contact definition) were then drawn using the APPLICON system at GE CRD, Schenectady. A fourth mask, EPRI-GE1-4 was fabricated to allow for an etch in the light sensitive region alone for increased junction photo-efficiency.

Table 4-1

CALCULATED TURN-ON THRESHOLD FOR THE DESIGNS OF FIGURES 4-1 and 4-2

	GATED TURN-ON THRESHOLD	dV/dt TURN-ON THRESHOLD*	F2/F1 F3 F4**
Gate Thyristor***	2.24 ma	1,890 V/μsec	2,600 V/μsec
Pilot Thyristor	26 ma	2,860 V/μsec	≧ 2,860 V/μsec
Main Thyristor	256 ma	4,800 V/μsec	≧ 4,800 V/μsec

* F1, F2, F3, and F4 not taken into account.

** F2 factor is an estimate only. F1, F3, and F4 are each taken to be 2. F2 for the gate thyristor is taken from the pilot and main thyristor as $\geq$ 8.

*** $\sigma_E \approx .000225$ for the gate thyristor and .001 for the pilot and main thyristors.

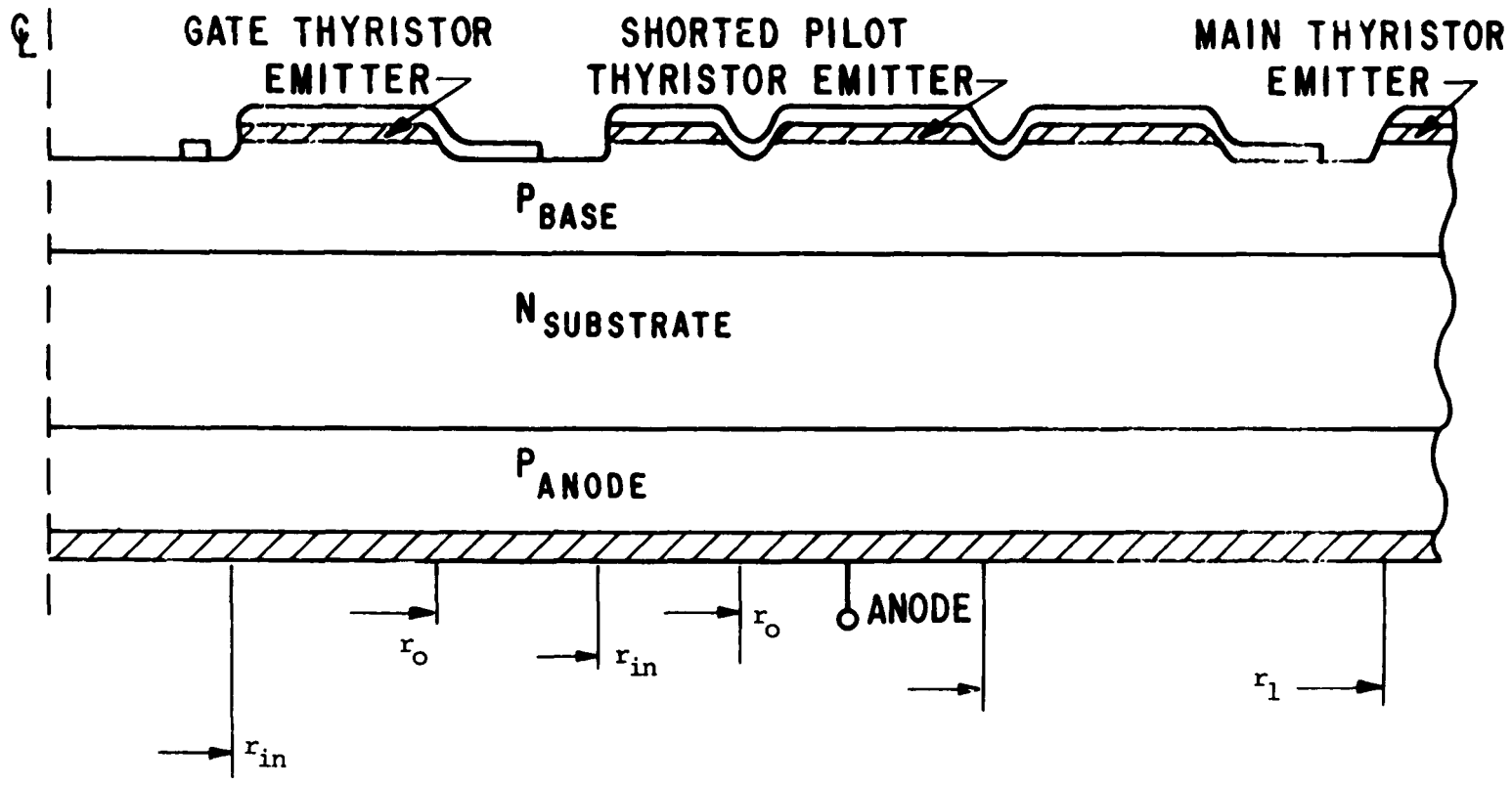


Figure 4-1. Gate and pilot thristor design.

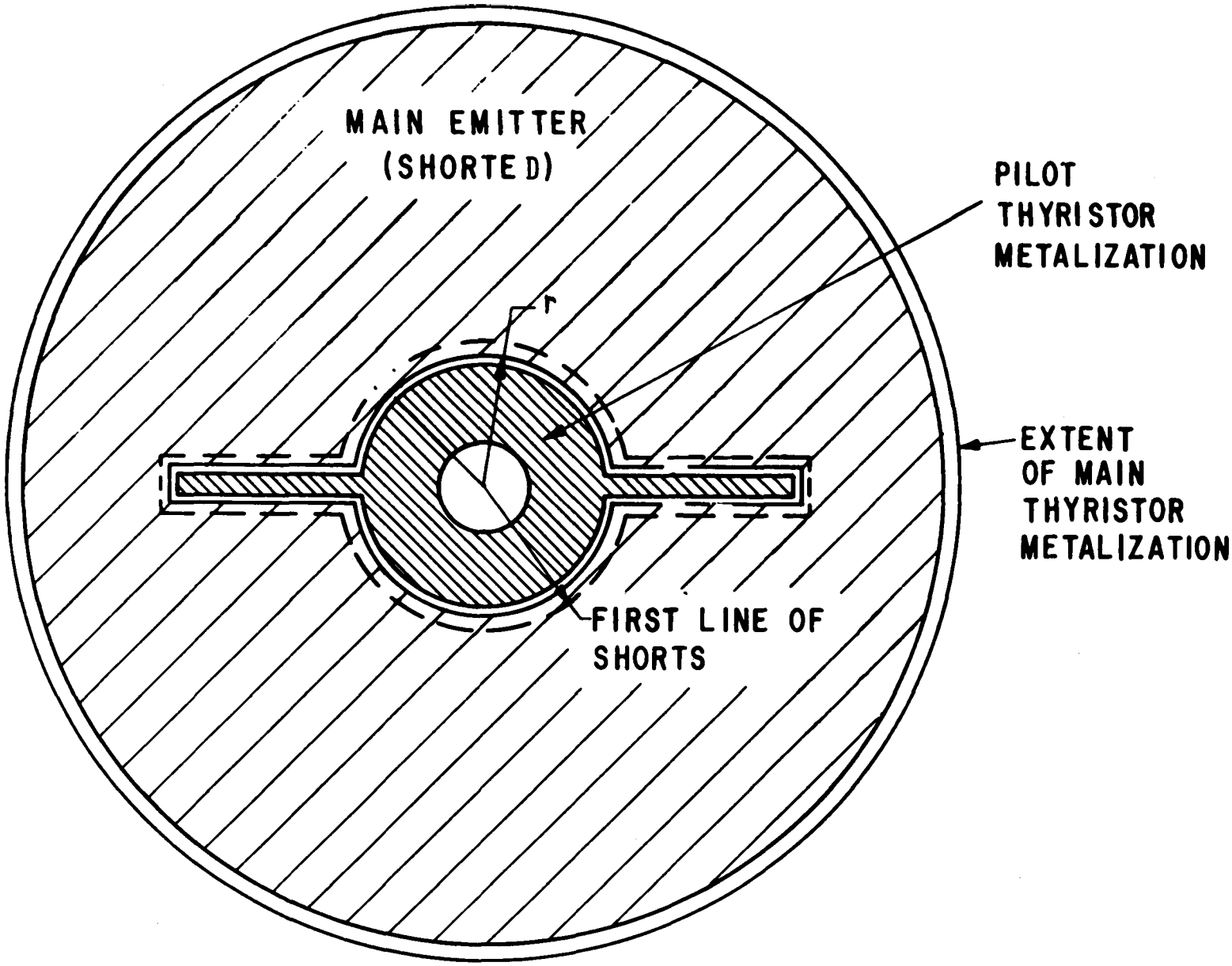


Figure 4-2. Main emitter design for longer turn-on periphery and improved dV/dt capability.

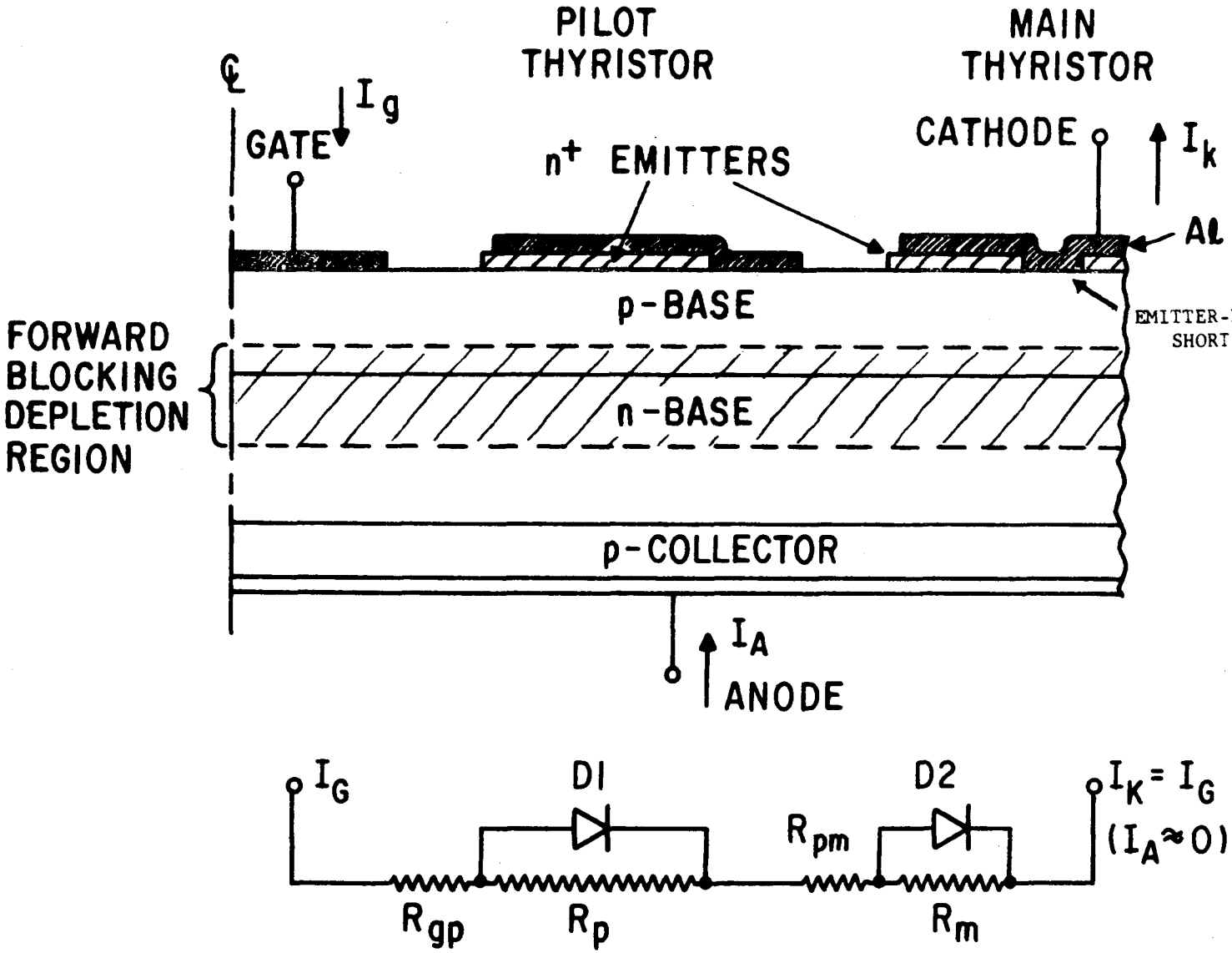
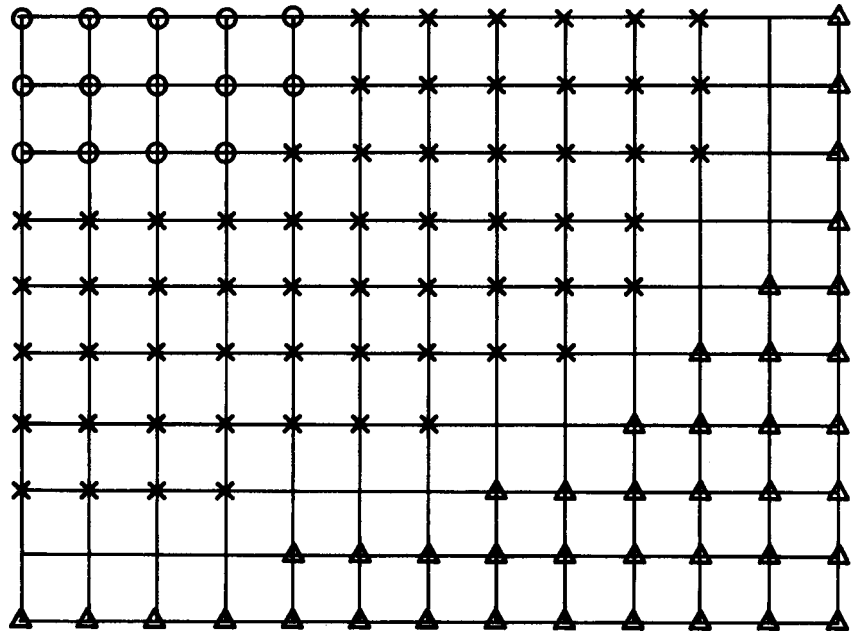
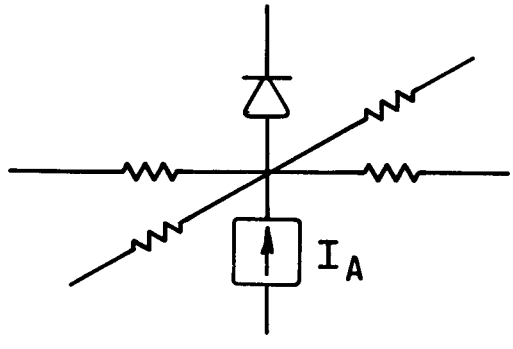


Figure 4-3. Simple thyristor turn-on model. (I_g can be photoelectrically induced. I_A is assumed to be evenly distributed.)



(a) Rectangular (or anular) two-dimensional mesh with (1) artibrary p_{base} conductivity at all points; (2) on arbitrary connected n+cathode area (denoted by *); (3) one arbitrary connected cathode metallization which must cover the n+cathode (there denoted by *) and one p_{base} short region (denoted by ⊕) of at least one point; (4) points "+" denote bare p_{base} material; and (5) points "Δ" denote gate contact metallization.



(b) Model of p_{base} nodes "*". Resistors model p_{base} resistance, diodes model the n+p_{base} junction, and current sources model the anode current.

Figure 4-4. Improved thyristor turn-on model used to check turn-on thresholds in final EPRI-GE1 design.

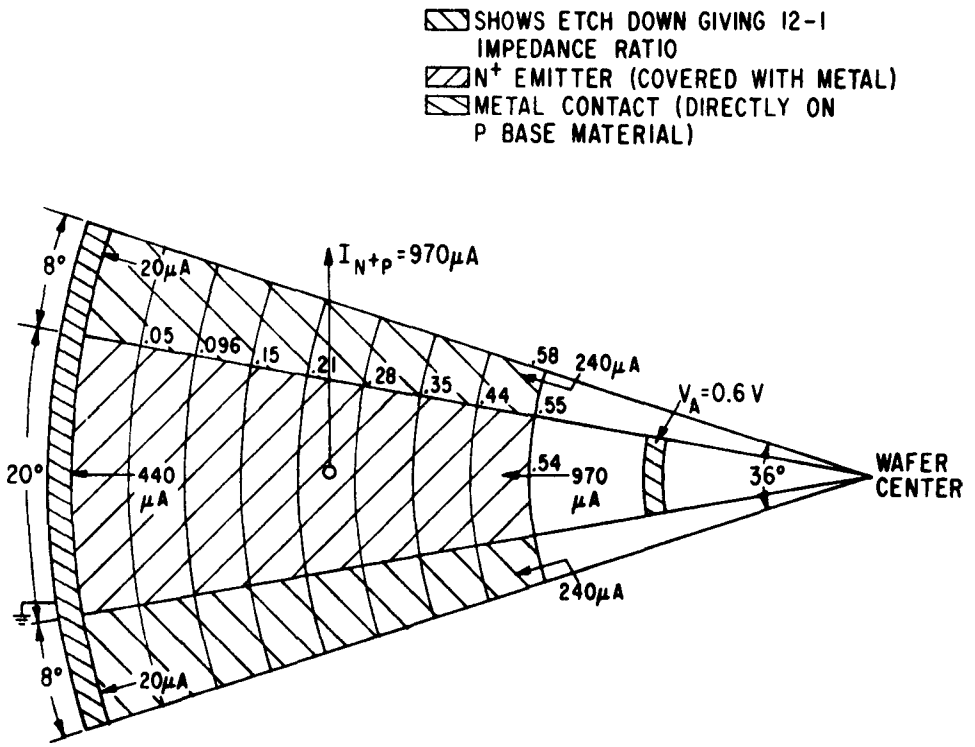


Figure 4-5. Some of the p_{base} voltages from a 1600 point mesh calculation for a gase voltage of 0.6 volts. The mesh covers 36° of an annular, fingered emitter containing 10 identical fingers in total. Note the etch down increases the base resistance in the outer 8°.

At 0.6 volts very little of the gate current flows up through the $n+p_{base}$ junction. However, at V_A = 0.8 volts, currents flow as marked in the figure. The etched down region forces 970 μa of a 1450 μa gate current to flow under the cathode finger. At the end of the finger 440 μa of 480 μa are flowing in the lower base resistivity area under the emitter finger. The rest of the 1450 μa gate current, 970 μa, flows to the cathode metallization through the $n+p_{base}$ junction.

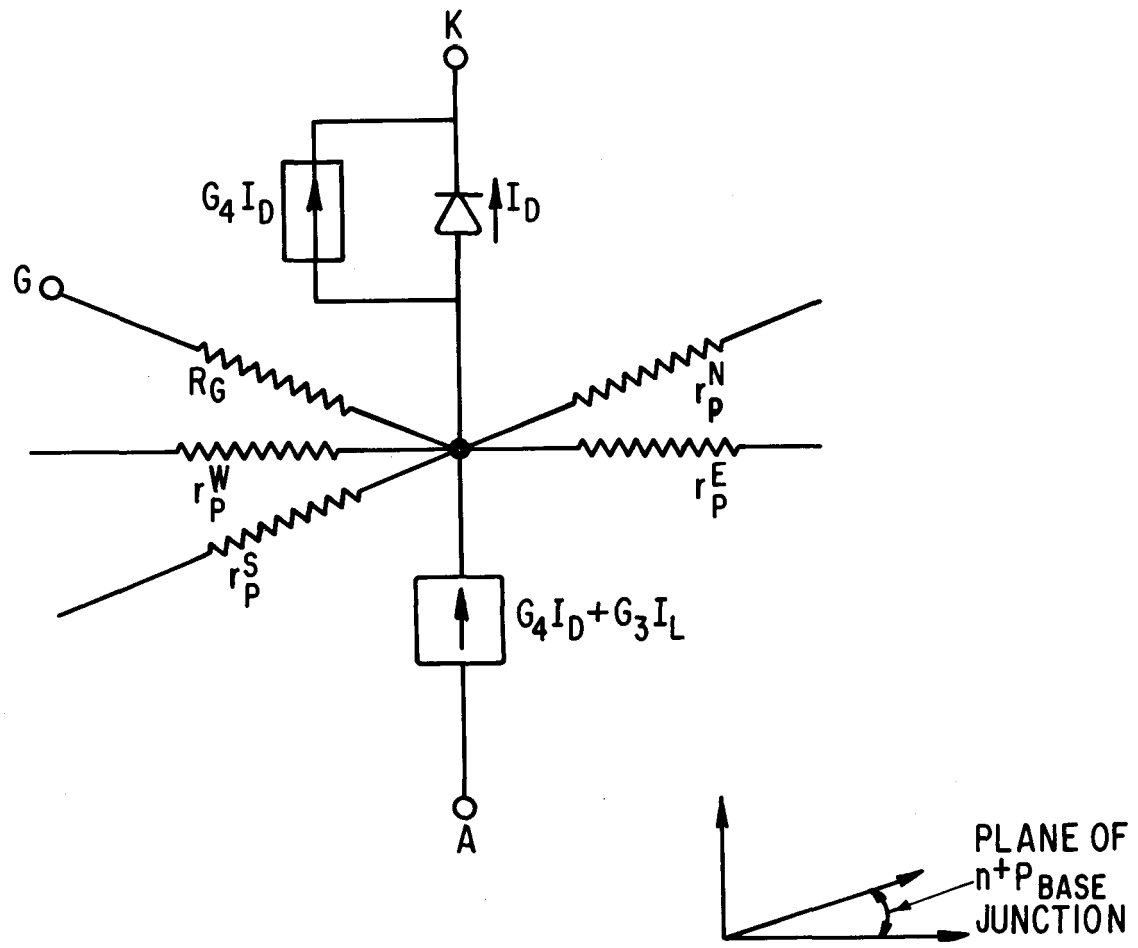


Figure 4-6. Possible future turn-on model analog electrical circuit (single node in a four-layer region of the device). G denotes the gate node and R_G is an arbitrary admittance which can be connected to any or all base nodes, P. I_L is the local sum of photocurrent, leakage current, and dV/dt current. I_D is the diode current controlled only by the voltage between K and P.

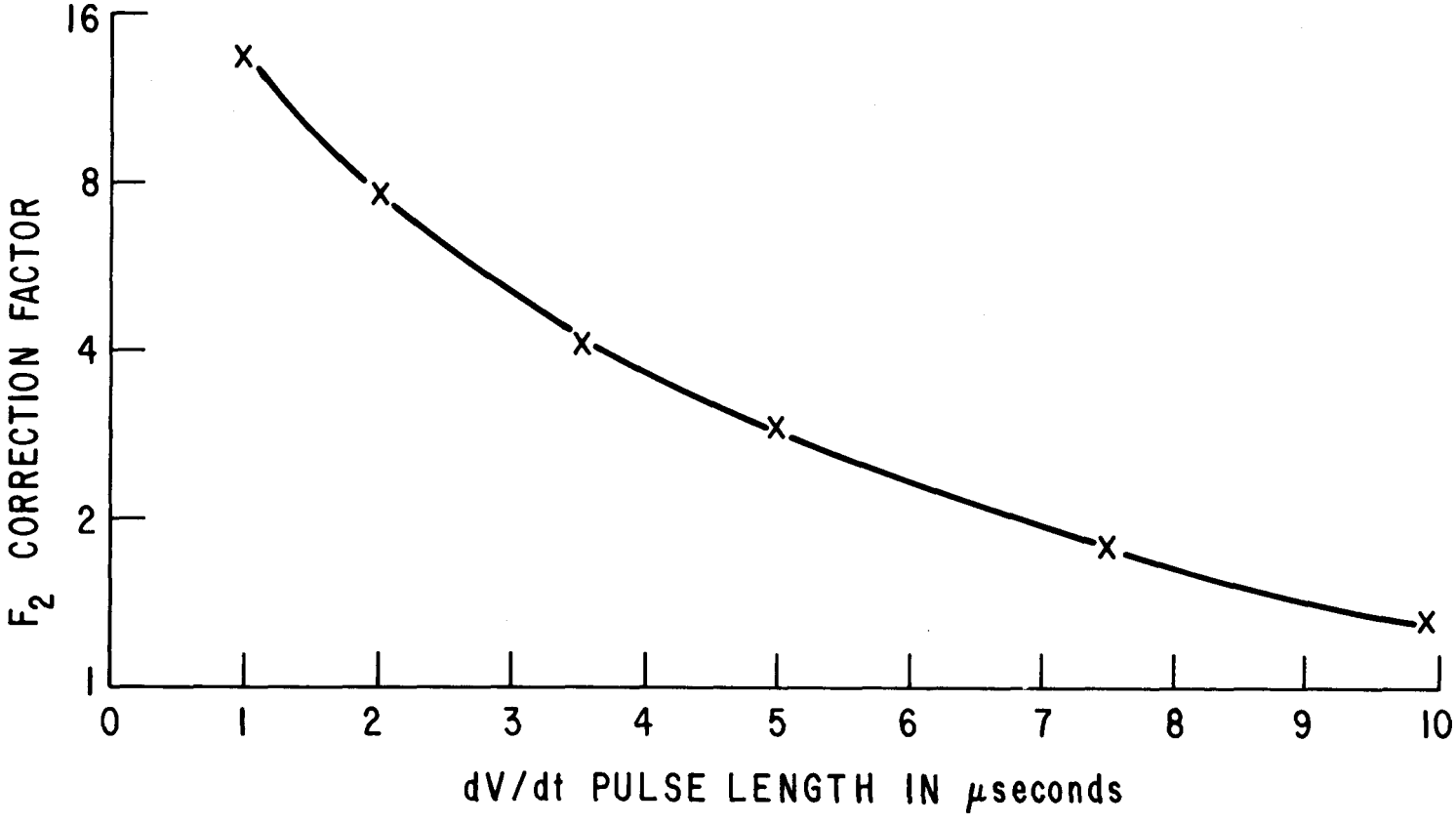


Figure 4-7. dV/dt correction factor for length of dV/dt pulse.

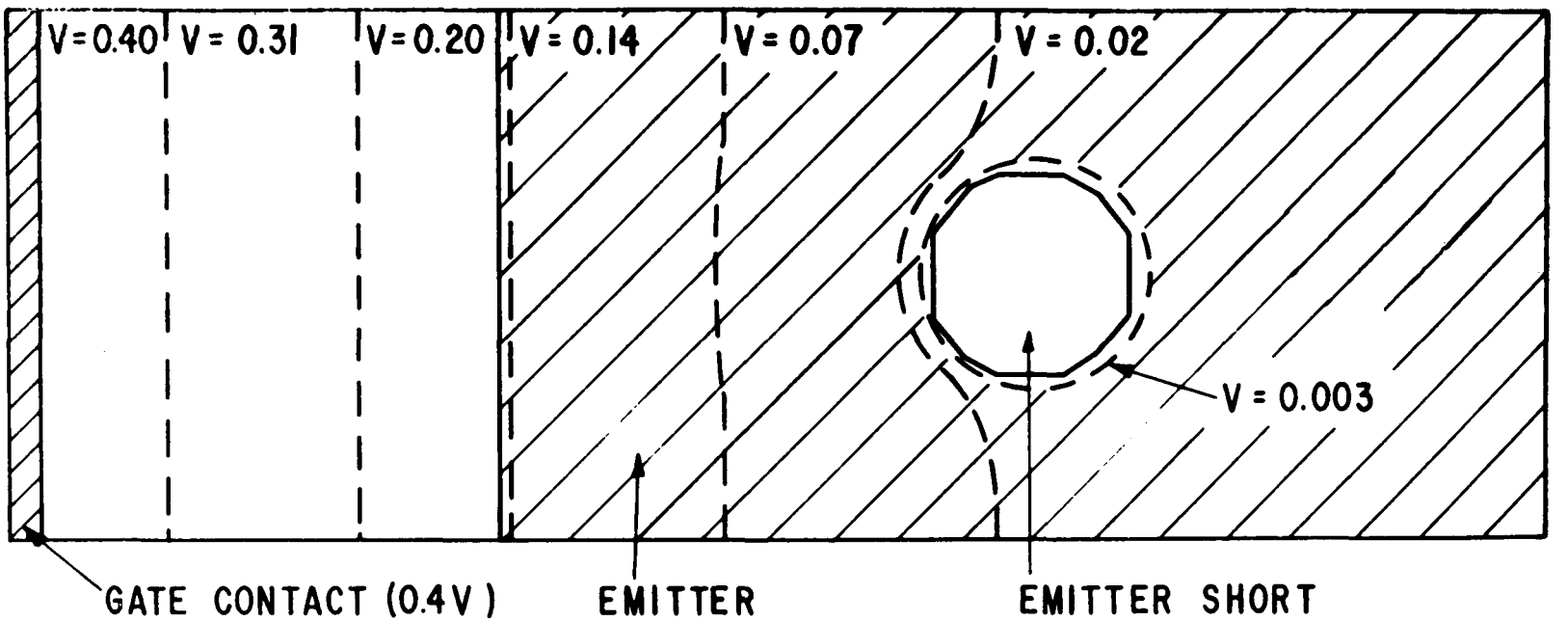


Figure 4-8. Pre-turn-on voltage distribution along main emitter turn-on line.

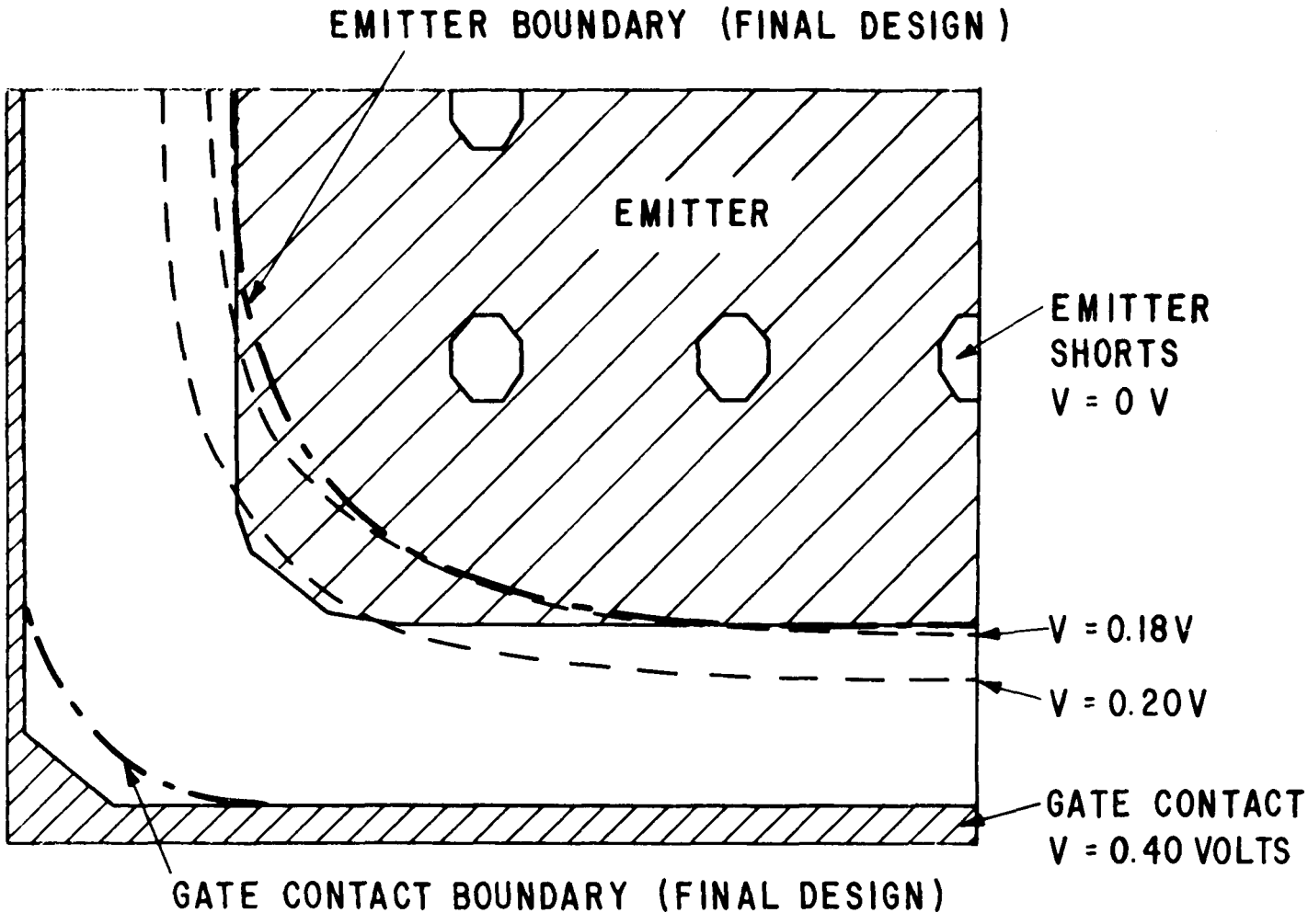


Figure 4-9. Pre-turn-on voltage distribution along main emitter turn-on line at the inside corners of the arm projections into the main emitter.

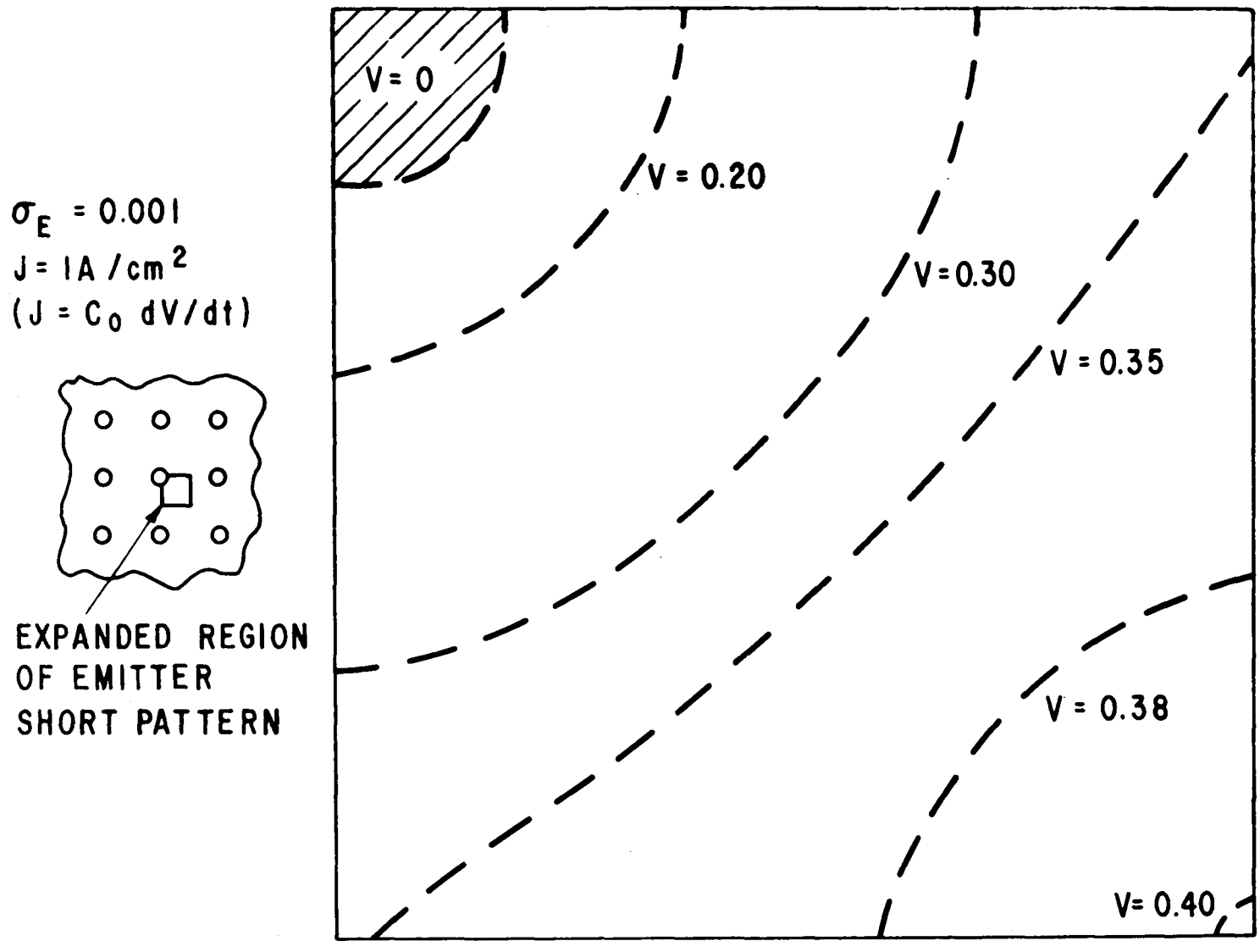


Figure 4-10. Voltage distribution around a typical emitter short in the main emitter for anode current density = 1A/cm^2.

Section 5

LIGHT FIRED THYRISTOR TEST DEVICES

INTRODUCTION

Because of the complexity of the EPRI-GE1 design described in the previous section, mask fabrication was more time consuming than anticipated, with the completed masks finally being delivered late in the third quarter. (This mask set is shown in Fig. 5-1 and described briefly in the caption.) To offset this loss in time, two sets of test light fired thyristors were fabricated based on GE's L1 thyristor.* These are termed the L1A and L1B devices and are partially optimized L1 devices in that the gate (L1A) or gate and pilot (L1B) amplifying stages have been made more sensitive in just the same way that is planned for the EPRI-GE1 device. These devices have been tested and found to have turn-on thresholds between 2 and 5ma. They have also been successfully tested for blocking voltage, dV/dt capability and room temperature turn-on speed (initial di/dt capability). These tests indicated that successful EPRI-GE1 devices would be possible with the gate thyristor amplifying stage as sensitive as 1-3ma. The tests also indicated what kind of light pulse overdrive factor would be needed for reliable thyristor turn-on using solid state junction laser sources operating at room temperature.** Tests with other light sources and with different light source conditions were also carried out. However, from the results, both at 25°C and 125°C, and at voltages from 5V to 2500V, it appears that, with 100nsec photo-pulse length, a large overdrive factor is needed for fast and reliable turn-on. This is described in more detail in the following.

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* The L1 tbyristor was a first attempt at an HVDC light fired thyristor (1).

** At room temperature the maximum laser pulse length is 200nseconds.

THE L1A AND L1B LIGHT FIRED THYRISTOR TEST DEVICES

Because of the conflicting requirements of high gate sensitivity, high dV/dt capability and high di/dt capability, and because of the necessity for a finite photo-sensitive area, it was decided to increase the number of mask steps in the fabrication of the EPRI thyristor from two, as was the case in the L1 device, to three. This extra step was utilized to increase the sensitivity of the first or gate amplifying stage over that found in the L1 device. It was also the aim of the EPRI design to have the amplifying stage (or stages) be the first to turn on when excess dV/dt was present. In order to test these concepts, as related to the etch down step, an experiment was performed using modified versions of the L1 device with the original L1 thyristor serving as a standard for comparison. Figure 5-2 shows the test structures. Device L1A shows the standard L1 structure, but with the gate amplifying stage sensitivity increased by an etch step. Approximately 30 devices were fabricated with etch depths from 12 to 20μ and an increased sensitivity of between 2 and 4 over the L1 device. Owing to the small area of the gate thyristor structure the dV/dt capability was still found to be in excess of 2000V/μsec at 125^{o}C.

Figure 5-2 also shows a modified version of the L1 device termed the L1B. In this device, the sensitivity of both the gate and pilot thyristor stages was increased by a pre-n^{+} emitter diffusion etch. Approximately 10 devices were fabricated with the same range of etch depths and increased sensitivities as the L1A devices.

Table 5-1 lists gate turn-on threshold measurements for the gate, pilot and main thyristor stages of each device. These threshold currents apply for a gate pulse of 10μsec duration with the device at room temperature. The measurements are made with a curve tracer with the thyristor anode open circuited. Thresholds at high voltages or high temperature would be somewhat lower. Figure 5-3 shows photographs of a typical series of sensitivity measurements. The current thresholds are taken as the break points on the I-V curves.

The devices were taken to a leakage current of 1μ ampere with the exception of a few devices which were taken to several milliamperes in order to measure breakdown voltage. Some of the devices were contoured for high voltage with a double positive bevel and are so indicated in Table 5-1.

The last column shows results of static dV/dt tests on all of the devices. These measurements were taken at 125°C except where indicated and, apart from some of the L1B devices, all showed excellent dV/dt capability as would be expected. However, some L1B devices showed room temperature dV/dt capability sufficiently small as to be within the measurement capability of the test apparatus. These dV/dt thresholds were due to turn-on at the pilot thyristor stage. None of the turn-ons were destructive which is an indication that we have a measure of dV/dt turn-on self-protection.

Figure 5-4 shows some photographs of 25°C, 100°C and 125°C dV/dt tests of device 2-6 which was an L1B type device. Turn-on is seen to occur more readily, and with shorter delay times at higher temperatures. Note that all devices were tested with a dV/dt ramp to 2200 volts.

Finally, Table 5-2 gives a list of both room and high temperature turn-on threshold values for both gate and dV/dt turn-on. Note the relatively good correlation between the observed and calculated dV/dt capability. The calculated dV/dt capability was based on turn-on at the pilot thyristor and used the correction factors described in the design section of this report. Initial di/dt capability, shown in the last column, and discussed in the next sub-section of this report, was somewhat variable, depending chiefly on temperature.

TURN-ON WITH A ROOM TEMPERATURE SOLID STATE LASER

Several L1A and L1B devices were partially tested for turn-on delay time and turn-on speed using a room temperature solid state GaAs laser. Device 2-6, which is representative of the L1B devices, was the device most thoroughly investigated. Its turn-on characteristics were measured as a function of temperature, anode voltage, light pulse amplitude and light pulse width. The light source that was used was an LD 168 laser which has a lasing threshold of about 30A at room temperature. Two different pulse widths were used as shown in Figures 5-5 and 5-6. These figures show the input current to the laser and the corresponding current caused by the light output at the end of a 10 foot Gallite 3000 light pipe incident on a PIN 25 detector rated at .33ma/mw. Hence, the peak photo-power in the incident beam ranges from zero to 420 mw for the narrow pulse in Fig. 5-5 and from zero

to 600 mw for the wide pulse in Figure 5-6. However, rather than specifying photo-power, succeeding tables and figures specify photo-current as taken from Figs. 5-5 and 5-6. This photo-current is considered to be a good estimate of the photo-gate current that would be caused to flow in the thyristor under test at low anode voltage at 25°C. However, with some difficulty, the actual photo-gate current caused by the pulse could be directly measured. Figure 5-7 shows the anode current on the scale of .1A/div over the first several microseconds with the scope triggered by the input current pulse driving the laser. The thyristor device type used for this test was the less sensitive L1 device described in reference 1. Note that the peak photo-current caused by the light pulse has an amplitude of about 300 ma. When measured on the PIN 25 detector, the photo-current was 140 ma, the maximum amplitude case in Fig. 5-5. Evidently this was sufficient to turn the device on with a delay time of 2.5μseconds. The regenerative processes initiated by the photo-pulse keep the current from falling to zero after the pulse and eventually lead to turn-on.

Figures 5-8 and 5-9 show turn-on delay time as measured from the onset of the current pulse into the laser (e.g., trace 1 in Figs. 5-5 or 5-6) to the 90% anode voltage point. In Fig. 5-8, with the 108 ma, 130 nsecond gate pulse, it is seen that the delay time is increased by going to 125°C despite the fact that the turn-on threshold is actually lower at that temperature. This is believed to be partly due to the temperature dependence of the base transport time. The dashed portion of the curve indicates a region in which the turn-on changes from one completely dependent on regenerative processes to one at least partly influenced by direct photo-carrier induced conductivity modulation.

To see whether turn-on was more reliable at lower, longer pulse lengths, the light pulse length was increased by a factor of 1.5. Turn-on delay time was measured at 25°C and at 125°C, for a 27 ma gate pulse amplitude. The results plotted in Fig. 5-9 show a large decrease in delay time as compared to those of Fig. 5-8 for approximately the same pulse amplitude. This is especially true for voltages below 500 volts. Note that even the 27 ma gate pulse amplitude, which is lower by a factor of 4 than that of Fig. 5-8 gives comparable delay times over the intermediate anode voltage range.

More complete data, including rise time (really voltage fall time between the 90% and 10% anode voltage points) and turn-on di/dt are given in Tables 5-3 to 5-6 which are typical of the data collected in turn-on tests of L1A and L1B devices. Note that the turn-on di/dt and the rise time-delay time sum both improve with the increase in pulse length and/or pulse amplitude and/or thyristor voltage as would be expected. And, except at pulse amplitudes near threshold, these quantities improve as the temperature is reduced.

Figure 5-10 shows delay time as a function of gate pulse amplitude for anode voltages of 50 and 2000 volts at 25°C. From these curves it can be seen that the 125°C, 27ma delay time is 9 μsec for V_A = 50 volts but at 25°C the device does not turn on at all. For larger gate pulse amplitudes, the turn-on delay time for V_A = 50 volts was the order of 1 μsec at 25°C and 2 μsec at 125°C. At V_A = 2000 volts, turn-on delay times for both the 125°C and 25°C cases were less than 1 μsec for all of the gate pulse amplitudes above 27ma.

Figure 5-11 shows some typical turn-on traces, the upper photograph showing anode voltage and current traces for turn-on from V_A = 50 volts and the lower photograph showing anode voltage and current traces for turn-on from V_A = 2000 volts. Although the peak current is not large (only 125A in the lower photograph), it is clear that the turn-on of the device with double amplifying gate structure can be very fast and that the 25°C device rating for initial di/dt is quite respectable. Note, however, that the di/dt values given in Tables 5-3 to 5-6 do not represent true ratings in that the device under test was not pushed to full rated current.

TURN-ON TESTS WITH A YAG LASER

In the last section, turn-on tests were described using the solid state GaAs laser, operated at room temperature, as the light source. Further turn-on tests were performed with the aim of cataloging turn-on behavior with longer pulse length light sources. The chief tool in this experiment was a CW YAG laser* operated in conjunction

* General Photonics YAG-TWO Laser.

with a modulator* to give pulse length variable between .1 and 20 μseconds. The experimental set-up is shown schematically in Fig. 5-12. A lens was used to focus the beam into a Galite 3000 10 foot light pipe containing 38 fibers which separated into two 19 fiber (T19) light pipes, one of which fed into the thyristor and one of which fed into a PIN-25 detector. For pulse lengths longer than 1 μsecond, the light pulse was approximately square with rise and fall times under 0.5 μseconds. Figure 5-13 shows the pulse shape.

With the experimental apparatus of Fig. 5-12, it was possible to determine what the threshold pulse length was for the thyristor at any given voltage. In the experiment from which the data in Figs. 5-14 and 5-15 are taken, the modulator pulse amplitude was set and, at each thyristor voltage, the pulse length carefully increased until the thyristor fired. This procedure was repeated for different light pulse energies and at several thyristor temperatures. The results indicate that if the EPRI-GE1 thyristor is to be capable of turn-on at 40 volts forward blocking then a minimum I_D value of 3.7ma is required, I_D being the photocurrent in the thyristor measured at 50 volts at T = 25°C.** Since the delay time of the turn-on is of the order or greater than the pulse length, Fig. 5-15 also indicates that the I_D = 3.7 case would lead to ~5 μsecond delay times at 50 volts. Therefore, only the I_D = 5.8 and I_D = 7ma cases are acceptable from the point of short turn-on delay time at low voltage. Figure 5-14 shows that increasing the temperature shortens the pulse length necessary to turn a device on.

Comparing results with those in the previous section which dealt with .1 to .2 μsecond pulse lengths, it can be seen that the pulse amplitude for acceptable turn-on is much lower. For light pulses less than 1 μsecond, the necessary pulse amplitude for turn-on has decreased approximately in proportion to the pulse length increase, much as expected. While YAG lasers and complex systems such as those used in this experiment are too costly and too unreliable, these results point to some advantages for light sources with a longer pulse duration. Such a source was investigated and results reported in the following section.

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* Lasermetrics KD*P Modulator.

** This use of the thyristor as the detector is necessary because of the very poor response of the PIN detector to 1.06 μlight.

TURN-ON TESTS WITH A LIQUID NITROGEN COOLED JUNCTION LASER

To test the feasibility of using a liquid nitrogen cooled GaAs junction laser as the light source in an HVDC system, a cryostat system was devised that was suitable for holding the laser and the light pipe. This system is shown in Fig. 5-16. The advantage of using the cooled laser is in the maximum rated pulse width increasing from .2 to 2 μseconds and a sevenfold increase in optical efficiency which much more than compensates for the threefold reduction in peak power. In fact, at $77^{o}K$, operating at full pulse power, the GaAs laser is capable of 3 times the energy in the output light pulse at less than one-half the input electrical energy. Furthermore, it is a much easier and cheaper task to design a laser pulser with a 1μsec. pulse with .25 μsecond rise and fall times than a 100 nsecond pulse with 25 nseconds rise and fall times. However, liquid nitrogen cooling, while inexpensive in itself, is, to say the least, inconvenient.

Figure 5-17 shows the photoresponse of a PIN diode to the light output of an LD168 junction laser* for the laser pulsed at 8 Amperes for pulse half-widths of .7 and 1.4 μseconds (approximately 25% and 50% of the rated maximum). Table 5-7 can be referred to for calibration from laser current, which is referred to in Figs. 5-18 to 5-20, to the PIN light detector diode current.**

Figure 5-18 shows, for device 2-6, the delay time as a function of thyristor voltage for a .5 μsecond, 8 A laser pulse. With the thyristor at 50 volts, the turn-on delay time is approximately 1.7 μsecs. Figure 5-19 shows delay time vs. thyristor voltage for device 2-1 at temperatures of $25^{o}C$, $75^{o}C$ and $125^{o}C$. Note that the amplitude of the light pulse is the same as that in Fig. 5-18 and again the 50 volt delay time (at $25^{o}C$) is about 1.7 μseconds. This delay time at 50 volts lengthens with increased temperature to approximately 2 μseconds at $75^{o}C$ to 2.5 μseconds at $125^{o}C$. This result was expected and is the result of shorter lifetimes and diffusion constants at higher temperature. The last curve in Fig. 5-19 is also at $125^{o}C$ but at approximately one-third the effective gate photocurrent amplitude.

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* Laser Diode Laboratories, NJ

** For the laser source, this current is approximately the same as that which would be produced in the thyristor at 50V room temperature.

As a result, the 50 V delay time is close to 5 μseconds. Figure 5-20 is included to show sample traces measured on the oscilloscope during the experiment. Turn-on is shown from 1500 volts with a 1.5 μsecond delay time. The lower trace shows the laser current to be 8 Amperes with a .5 μsecond half-width, and the upper trace shows approximately 80ma flowing in the PIN detector.

The last figure related to the $77^{o}K$ turn-on experiment is Fig. 5-21 in which, at each thyristor voltage from 50 to 1500 volts, the laser current was slowly increased until the device fired. That current is plotted as the ordinate, the thyristor voltage being the abscissa. The laser pulse width in all cases was kept at .5 μseconds.

EFFECT OF LIGHT PULSE ON BLOCKING CHARACTERISTICS

One of the possibilities that must be considered in a light triggered thyristor application is that of the light pulse occurring at a time when the thyristor is reverse blocking. At this point, any current rectified at the deep lying reverse junction acts like base current in a transistor and we will have the possibility of locally high current density equal to the rate of the photon generated carriers divided by $1-\alpha M$, α being the transistor current gain and M being the local avalanche multiplication factor. Figure 5-22 shows a calculation of the photon generated current as a function of voltage. To estimate actual current density, multiply by $1/(1-\alpha M)$ whose variation is well represented by the variation in net photocurrent in Figure 3-11 which would indicate a factor of 4 increase above the calculated value appearing in Fig. 5-22 at 2500 volts. Including this factor, it is seen that with the 9000Å light source the local reverse junction current density is still a fraction of an ampere/(cm^2) and of the order of milliamperes in total, these numbers being based on the actual geometry and properties of the EPRI-GE1 device. This current density should not cause any damage nor should a 1 μsecond, 1 or 2ma increase in leakage current cause any destructive action. This opinion was put to the test using the light pulse given in Fig. 5-23, which shows the laser pulse and related PIN detector current, and a number of typical L1A and L1B thyristors.

The experiment consisted of a pulse measurement of the room temperature thyristor forward and reverse blocking voltages before and after 5 minutes at 2500 volts reverse bias (dc) during which the light pulse was applied. Results are tabulated in Table 5-8. They show that there is no correlation between decreased reverse blocking voltage and increased leakage current and light pulses occurring at high reverse bias voltage. Careful inspection of Table 5-8 does show that devices originally leaky become worse after being held at 2500 volts whether or not the light source was turned on. While 5 minutes with 8 devices at room temperature is not a complete test, such results were not unexpected particularly considering the small penetration of 9000Å photons. With the 1.06 YAG laser, our results might have been quite different as the rectified photocurrent density would be orders of magnitude greater owing to the extremely deep light penetration.

TURN-ON TESTS AT REVERSE BIAS

A second special experiment was performed with the apparatus shown in Fig. 5-24. On the right-hand side of the figure is a test voltage waveform to be applied to the thyristor under test. Superimposed is the laser current pulse which is to be moved in time with respect to the start of the thyristor ramp voltage. The point of the experiment is to determine whether a light pulse applied some time before the thyristor is in its forward blocking mode may leave sufficient residual carriers to cause turn-on when the thyristor later becomes positive. Using a battery and the dV/dt tester along with a triggerable junction laser source, it is possible to create the voltage waveform. A double pulse source with variable delay between pulses is used to trigger the dV/dt ramp and the laser current pulse. No turn-on occurred in the experiments performed to date even with U_B being 50 volts and the zero crossing occurring as little as 2 μseconds after the laser pulse. However, it is important to point out that a higher amplitude, longer wavelength light source might give different results.

Table 5-1

THRESHOLD TURN-ON CURRENTS, LEAKAGE CURRENT AND dV/dt CAPABILITY

DEVICE	THRESHOLD CURRENT[1] GATE, PILOT, MAIN (ma)	25°C BLOCKING VOLTAGE[2] FORWARD, REVERSE (VOLTS)	dV/dt Capability[3] (VOLTS μsec)
1-1	--------	---------	>2500
1-2	4, 86, 150	>2200, >1300	>2500
1-3	1.5, 80, 150	>2500, >2350	>2500
1-4	2, 110, 170	>2350, >1900	>2500
1-5*	3, 100, 150	2670*, 2600*	>2500
1-6	3, 120, 180	>2450, >2500	>2500
1-7*	2, 80, 140	2900*, 2750*	>2500**
1-8	3, 120, 180	>1800, >1000	>2500
2-1	2, 20, 130	>2400, >2550	∿2000
2-2	4, 60, 130	>2400, >2000	>2500
2-3	2, 40, 110	>2400, >2000	∿2500
2-4	4, 44, 140	>2350, >1700	>2500
2-5	3, 40, 160	>2200, >2550	>2500
2-6	2, 28, 140	>2200, >2500	∿2500
2-7	3, 36, 150	>2400, >1800	∿3000
2-8	3, 35, 130	>2400, >2300	∿3000
3-1	3.5, 80, 130	>2500, >1700	
3-2	4, 80, 150	>2400, >2000	>2500
3-3	4, 120, 250	>2500, >2000	>2500
3-4*	4.5, 90, 150	2600*, 2600*	>2500
3-5	4.5, 90, 140	>2500, >1600	>2500
3-6	4, 90, 170	>2500, >2000	>2500
3-7*	4, 90, 140	2790*, 2600*	>2500
3-8*	5, 100, 160	2600*, 2600*	>2500
3-9*	5, 85, 170	2700*, 2600*	>2500
3-10*	5, 93, 150	2830*, 2600*	>2500
4-1	3, 100, 160	>2450, >2700	>2500
4-3	2.5, 100, 160	>2200, >2400	>2500
4-4	2.5, 90, 160	>2400, >2650	>2500
4-6	3, 180, 280	>300, >2500	>2500
4-7*	3, 65, 150	2880*, 2600*	>2500
4-10	3, 90, 180	>2500, >1600	>2500

* Indicate devices with a double positive bevel.
** 125°C value.

1. Threshold for d.c. gate current.
2. Values indicate voltage at which the current was 1 μampere. "*" indicates values where the current was in the 1-5 ma range. Note that only the latter values can be taken as breakdown voltage.
3. Measured at room temperature.

Table 5-2

TURN-ON MEASUREMENTS FOR DEVICE 2-6

TEMPERATURE	THRESHOLD TURN-ON CURRENTS [1] GATE,	PILOT,	MAIN	Dv/dt CAPABILITY [2] MEASURED/EXPECTED	INITIAL di/dt CAPABILITY [3]
25°C	2.2	28	140	3300/3000	a) 380 A/μsec b) 700 " "
125°C	1.2	15	75	2300/1800	a) 180 " " b) 400 " "

1) For a D.C. gate current. (Estimated from the gate characteristics, ie see figure 5-3.

2) See Table 5-1 and figure 5-4 for more detail.

3) Measured with a 136 ma .2μsec photogate pulse. "a" - turn-on from 1500 volts with a .1μf,10Ω snubber, "b" turn-on from 2000 volts.

Table 5-3

TURN-ON OF DEVICE #2-6, TEMP. = 25°C,
LASER PULSE WIDTH = 200 NSEC

LIGHT OUTPUT* (ma)	DEVICE VOLTAGE (VOLTS)	DELAY TIME (μsec)	Di/dt (A/μsec)	RISETIME (μsec)
27	50	5	0.6	3.1
92	50	0.9	0.5	3.9
136	50	0.85	0.5	3.1
208	50	0.8	0.55	2.6
27	2000	0.78	700	0.54
92	2000	0.26	710	0.53
136	2000	0.23	750	0.52
208	2000	0.21	780	0.51
136	5	6.5	0.005	40
136	20	1	0.06	10
136	50	0.8	0.45	3
136	100	0.9	1.6	2.6
136	200	0.8	26	1.9
136	500	0.4	37.5	0.78
136	1000	0.24	160	0.95
136	1500	0.24	380	0.78
136	1800	0.22	590	0.57
136	2000	0.22	700	0.48

* As measured in the PIN 25 detector.

Table 5-4

TURN-ON OF DEVICE #2-6, TEMP. = 125°C,
LASER PULSE WIDTH = 200 NSEC

LIGHT OUTPUT* (ma)	DEVICE VOLTAGE (VOLTS)	DELAY TIME (μsec)	Di/dt (A/μsec)	RISETIME (μsec)
27	50	9	0.37	4
92	50	2.3	0.36	4
136	50	1.9	0.30	4.4
200	50	1.7	0.40	3.6
92	1450	0.5	175	1.5
136	1450	0.42	165	1.38
208	1450	0.36	170	1.24
136	5	7.5	0.003	>50
136	20	2.4	0.06	> 8
136	107	1.5	1.25	3.25
136	215	1.5	3.3	2.55
27	300	1.8	15	2
27	500	1.2	48	1
27	1000	.9	300	.4
27	1500	.7	800	.3

* As measured in the PIN 25 detector.

Table 5-5

TURN-ON OF DEVICE #2-6, TEMP. = 75°C,
LASER PULSE WIDTH = 200 NSEC

LIGHT OUTPUT* (ma)	DEVICE VOLTAGE (VOLTS)	DELAY TIME (μsec)	Di/dt (A/μsec)	RISETIME (μsec)
92	50	1.7	.38	4.5
136	50	1.3	.34	4.1
208	50	1.3	.36	4.0
27	2000	1.08	500	0.52
92	2000	0.30	625	0.64
136	2000	0.26	600	0.68
208	2000	0.24	600	0.70

* As measured in the PIN 25 detector.

Table 5-6

TURN-ON DEVICE #2-6, TEMP. = 125°C,
LASER PULSE WIDTH = 130 NSEC

LIGHT* OUTPUT (ma)	DEVICE VOLTAGE (VOLTS)	DELAY TIME (μsec)	Di/dt (A/μsec)	RISETIME (μsec)
144	5	9	0.0016	>90
144	20	2.4	0.038	17.6
144	50	1.6	0.34	5.1
144	100	2.3	1.15	3.4
144	200	2.1	8.0	2.8
144	500	1.7	13.5	2.0
144	1000	1.3	74	1.6
144	1200	.7	115	1.2
144	1500	.55	164	1.2

* As measured in the PIN 25 detector.

Table 5-7

77^{o}K LASER CALIBRATION

Laser I, V	Laser pulse width (μ seconds)	PIN current (ma)
12 A	.5	400
10 A	.5	310
8 A, 24 V	.5	250*
8 A, 24 V	1.0	160*
6 A, 20 V	.5	165
4 A, 16 V	.5	80
3.2 A	.5	58
2.5 A	.5	38
2.1 A	.5	31
1.85 A	.5	23

* See Figure 5-13

Table 5-8

TEST OF LIGHT PULSE IN RESERVE BREAKDOWN VOLTAGE AND LEAKAGE CURRENT

Device	Initial Breakdown Voltage (Leakage Current)*		Final** Breakdown Voltage (Leakage Current)*	
	Forward	Reverse	Forward	Reverse
1-10	2750	2800	2750	> 2700(A)
2-5	> 2500	2800	2700 (2μa)	2800
3-10	2800	2800 (4 ma)	2800	2800 (4 ma)
2-3	2650	2750 (1 μa)	2650	2750 (1 μa)
4-2	2600	> 2700 (1 μa)	2600	> 2000 (2 μa) 2900 (1 ma)
1-1	2550	2600 (8 ma)	2550	2600 (20 ma)
4-4	2650	> 2800 (4 ma)	2650	> 2300 (25 ma)(B)
2-6	> 2400 (.5 ma)	> 2800 (4 ma)	> 2400 (.5 ma)	> 2200 (25 ma)

* Leakage currents are given in brackets

** The test consisted of 5 minutes of pulsing at 2500 volts reverse bias. The light pulse is shown in Figure 25.

(A) Leakage current increased slightly, the breakdown voltage is likely to be unchanged.

(B) Tested without light pulse.

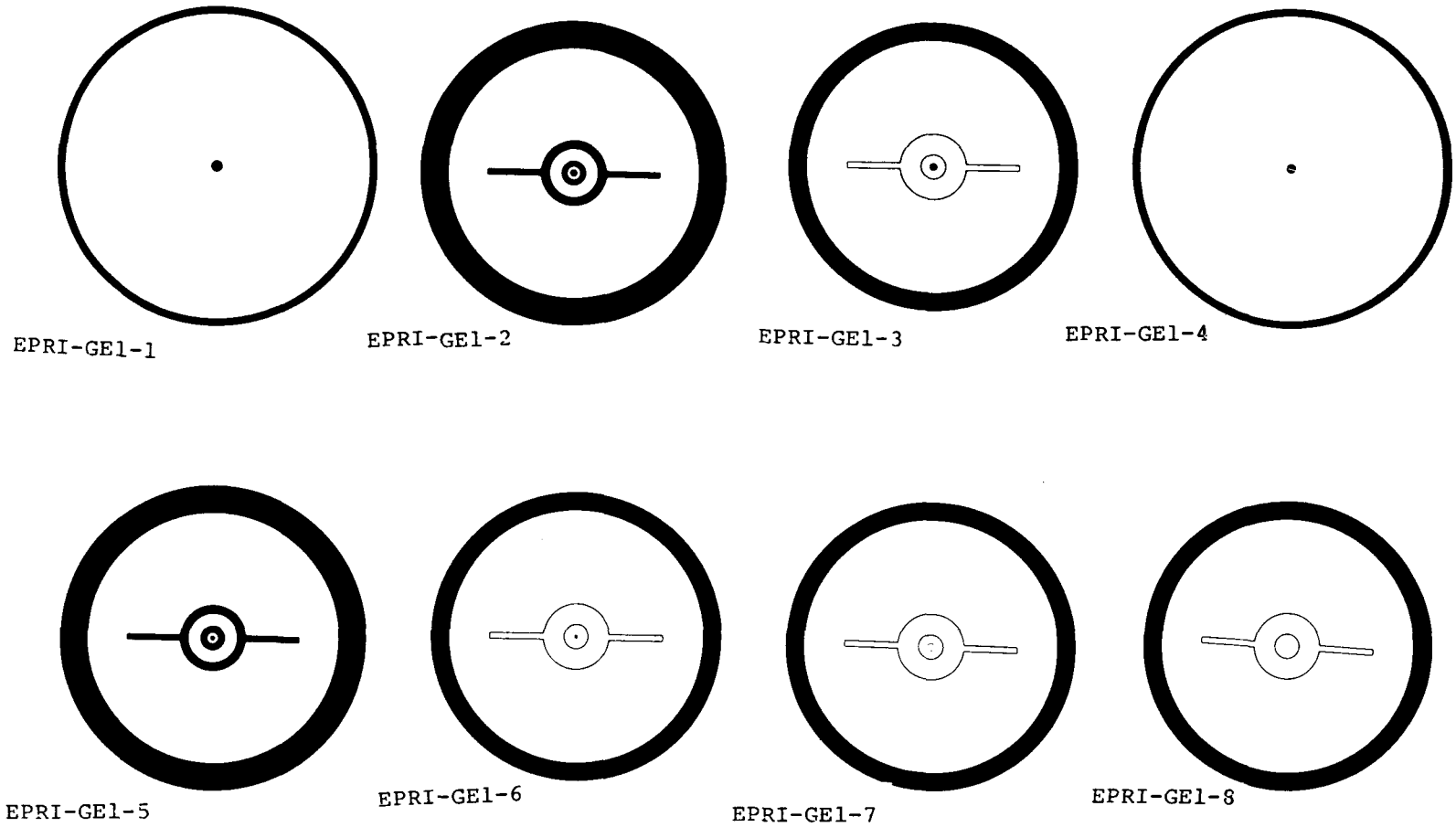


Figure 5-1. Photograph of a complete set of masks for the EPRI-GE1 light-fired thyristor. EPRI-GE1-1, EPRI-GE1-2, and EPRI-GE1-3 are in the pre-etch, the n+ definition, and the contact masks respectively for use with a 40 mil diameter light pipe. EPRI-GE1-4, EPRI-GE1-5, and EPRI-GE1-6 are the corresponding masks for use with a 20 mil diameter light pipe. Masks 7 and 8 are test masks.

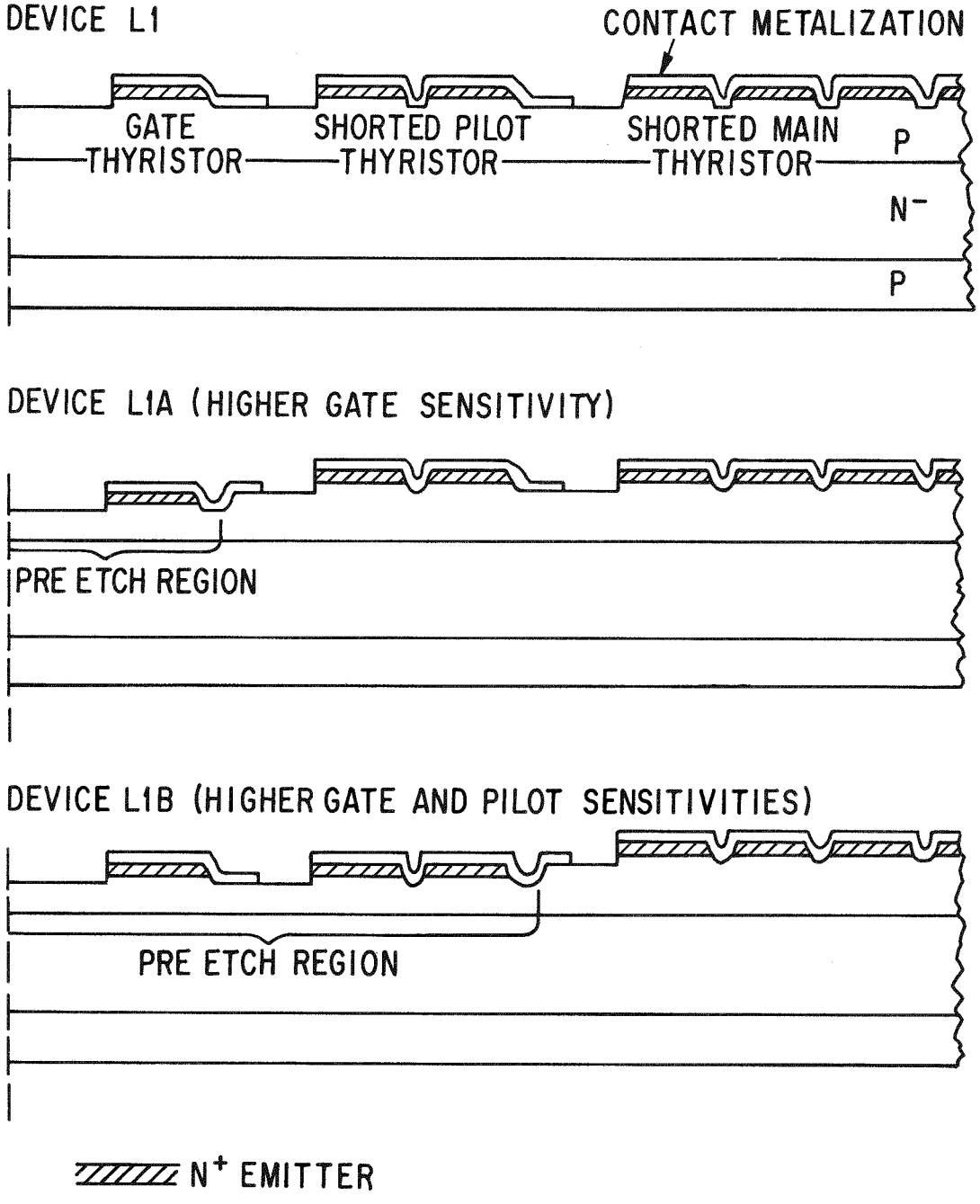
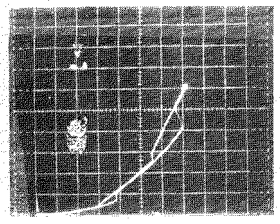


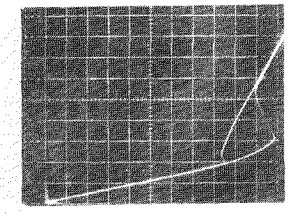
Figure 5-2. Schematic cross section of the L1 light-fired thyristor and two more sensitive test variations. Note that the sensitivity is increased by a center region etch prior to the n+ emitter diffusion.



50 ma/div

(a) Gate, Pilot and Main Thyristor

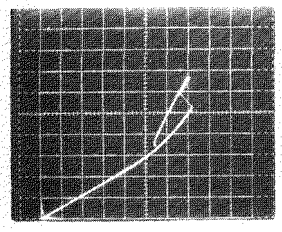
1.0 v/div



10 ma/div

(b) Pilot Thyristor Stage

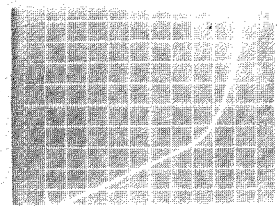
0.2 v/div



50 ma/div

(c) Main Thyristor

0.5 v/div

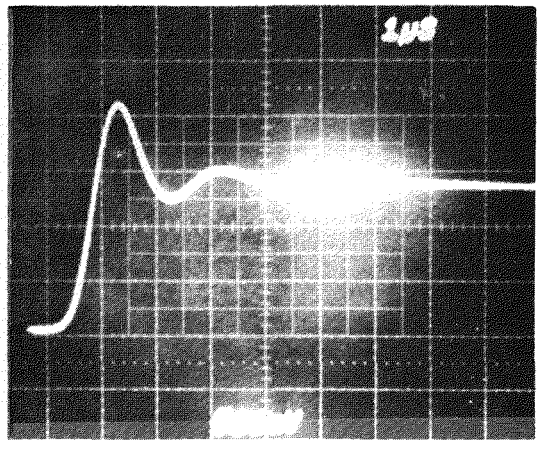


0.5 ma/div

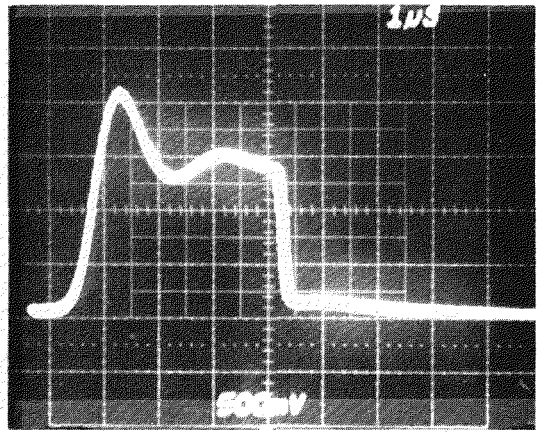
(d) Gate Thyristor

0.1 v/div

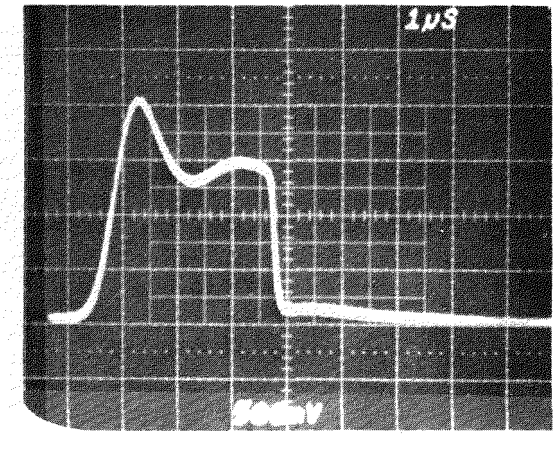
Figure 5-3. Typical threshold turn-on measurements. (The photographs show curvetracer gate-cathode IV's taken with the anode open circuited.)



25°C, no turn-on.

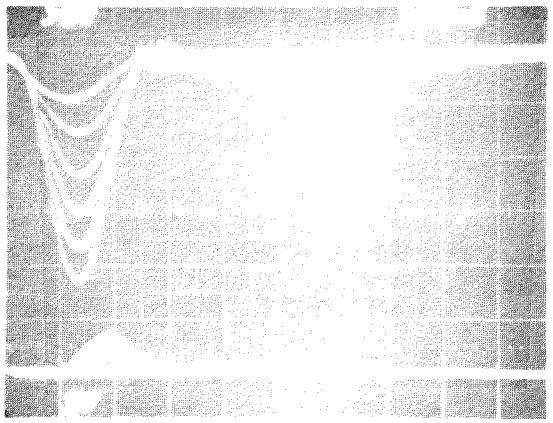


100°C, turn-on with a 3.5 μsec delay time.



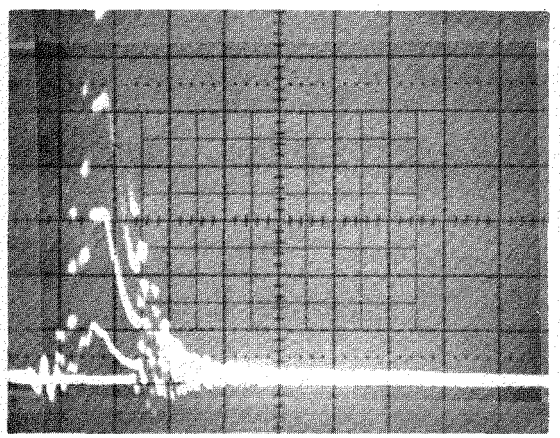
125°C, turn-on with a 3.0 μsec delay time.

Figure 5-4. dV/dt turn-on test of device 2-6 (L1B) at 25°C, 100°C, and 125°C.



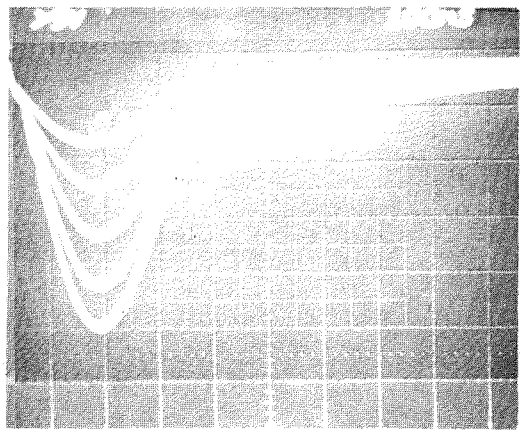
Laser current, 20A/div
(Multiple trace)

Detector current 200 ma/div
(Multiple trace)

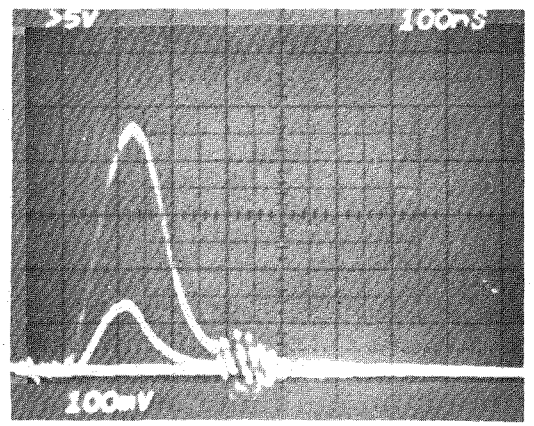


Detector current, 20 ma/div
(Multiple Trace)

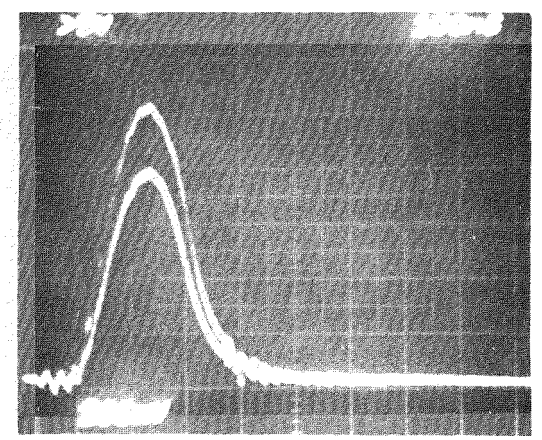
Figure 5-5. Light pulse calibration for the 130 nsec laser pulse width. Light output from the light pipe was measured at ∿0.3A/W by a PIN 25 detector.



LASER Current, 20A/div
(Multiple traces)

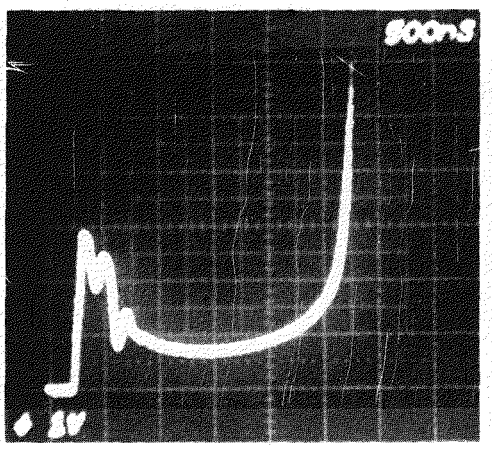


Detector output, 20 ma/div
(Multiple traces)



Detector output, 40 ma/div
(Multiple traces)

Figure 5-6. Light pulse calibration for the 200 nsec laser pulse width. Light output from the light pipe is measured at ∿0.33A/W on a PIN 25 detector.



Anode Current, .1A/div.

Figure 5-7. Anode current, prior to and at the onset of turn-on. Note the initial current caused by a 130 nsec LASER light pulse. Anode voltage = 450 volts.

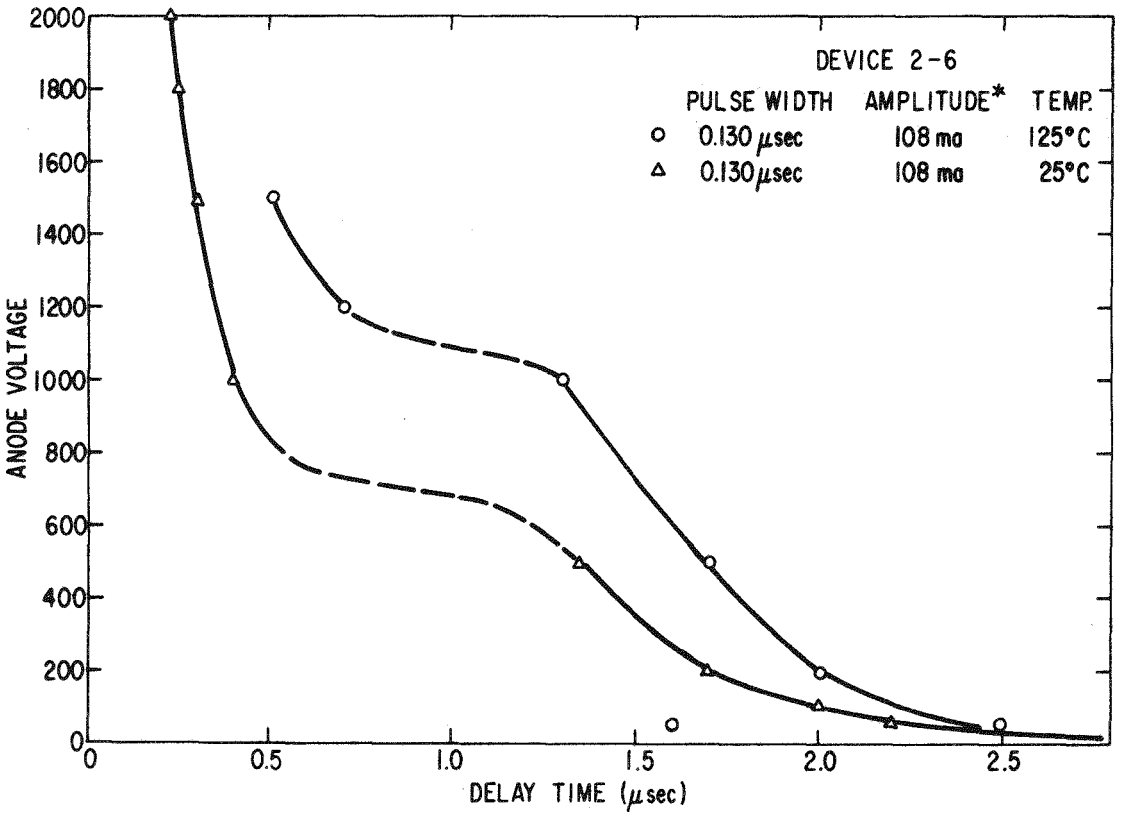


Figure 5-8. Turn-on delay time vs. blocking voltage for device 2-6 at 25°C and 125°C for the Narrow Pulse Width.

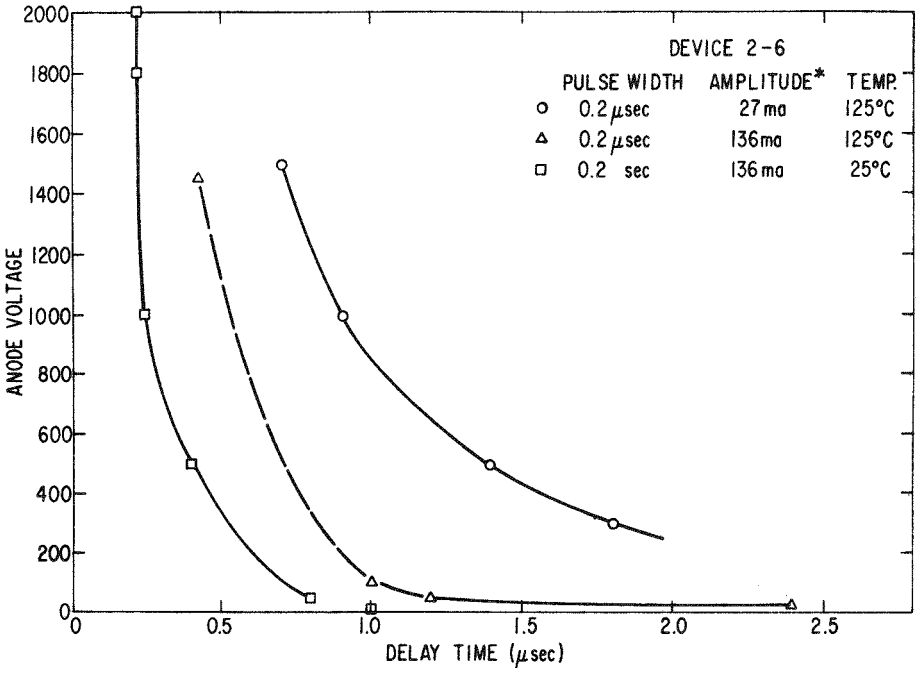


Figure 5-9. Turn-on delay time vs. anode voltage for device 2-6 at 25°C and at 125°C for the Wide Pulse Width.

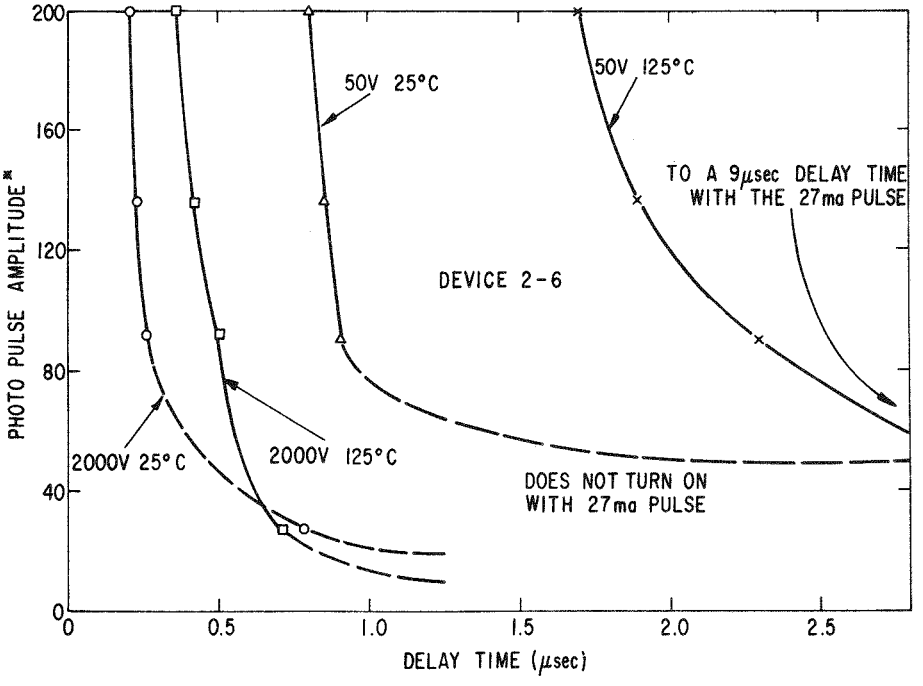
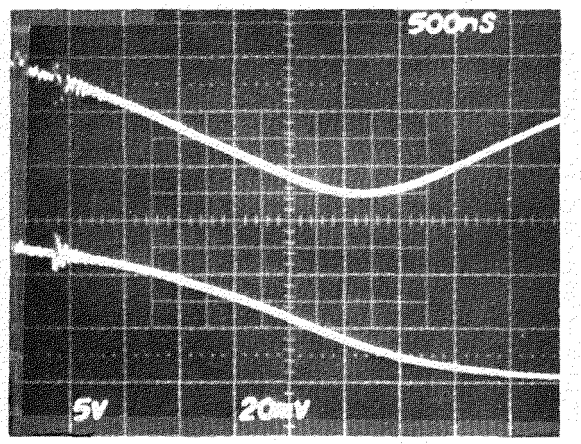
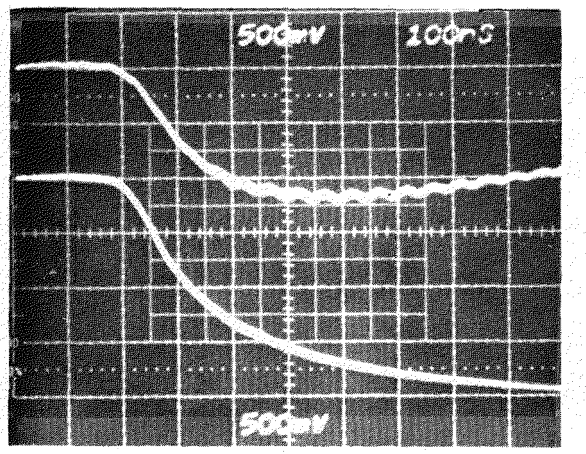


Figure 5-10. Turn-on delay time vs. gate pulse amplitude. Gate pulse width - 200 nsec.



I_A, 05A/div

V_A, 20V/div



I_A, 50A/div

V_A, 500V/div

Figure 5-11. 25°C turn-on of device 2-6 with a 200 nsec laser pulse.

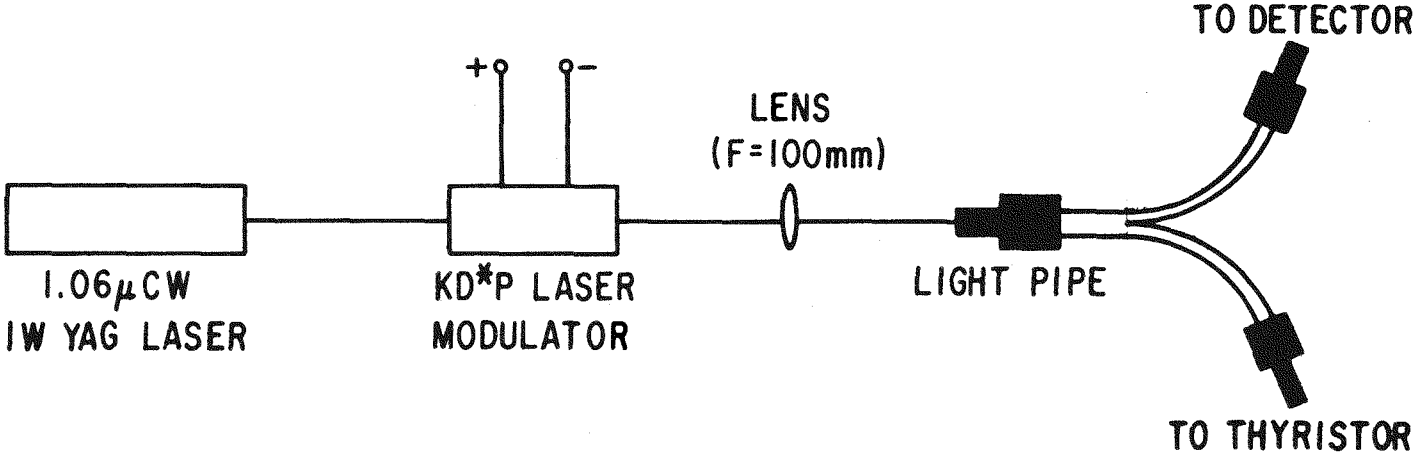
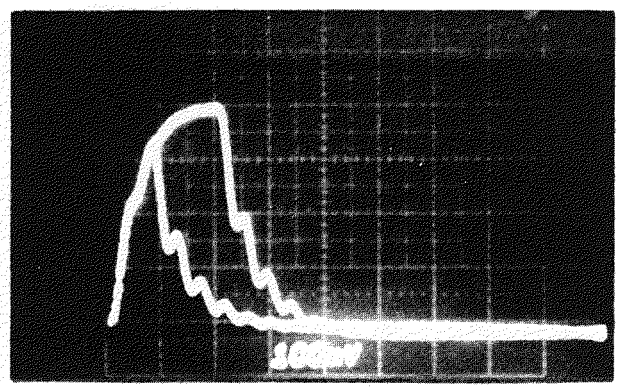


Figure 5-12. Experimental setup for YAG laser turn-on tests. The laser is a General Photonics YAG-TWO laser; the modulator is a Lasermetrics KD*P model 3078 FV.

.5μsec/div.



100 mv(2 ma)/div.

Figure 5-13. YAG laser light pulse shape for short pulses.

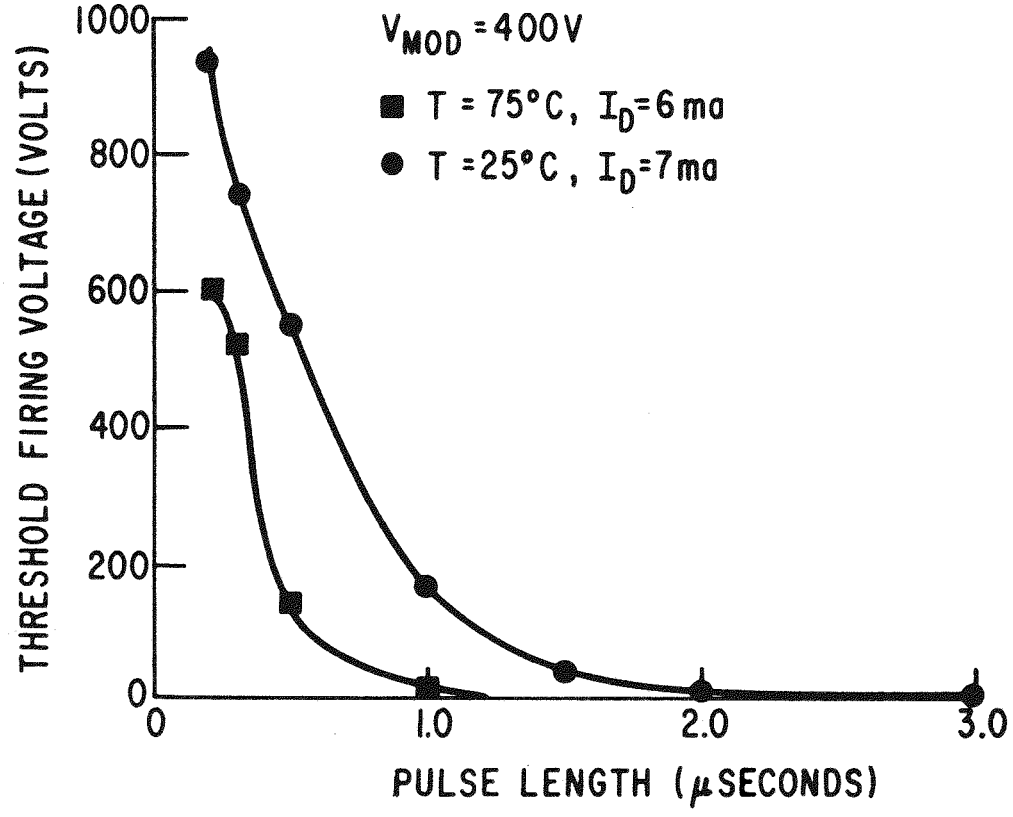


Figure 5-14. Threshold turn-on voltage of device 2-6 at 25°C and at 75°C.

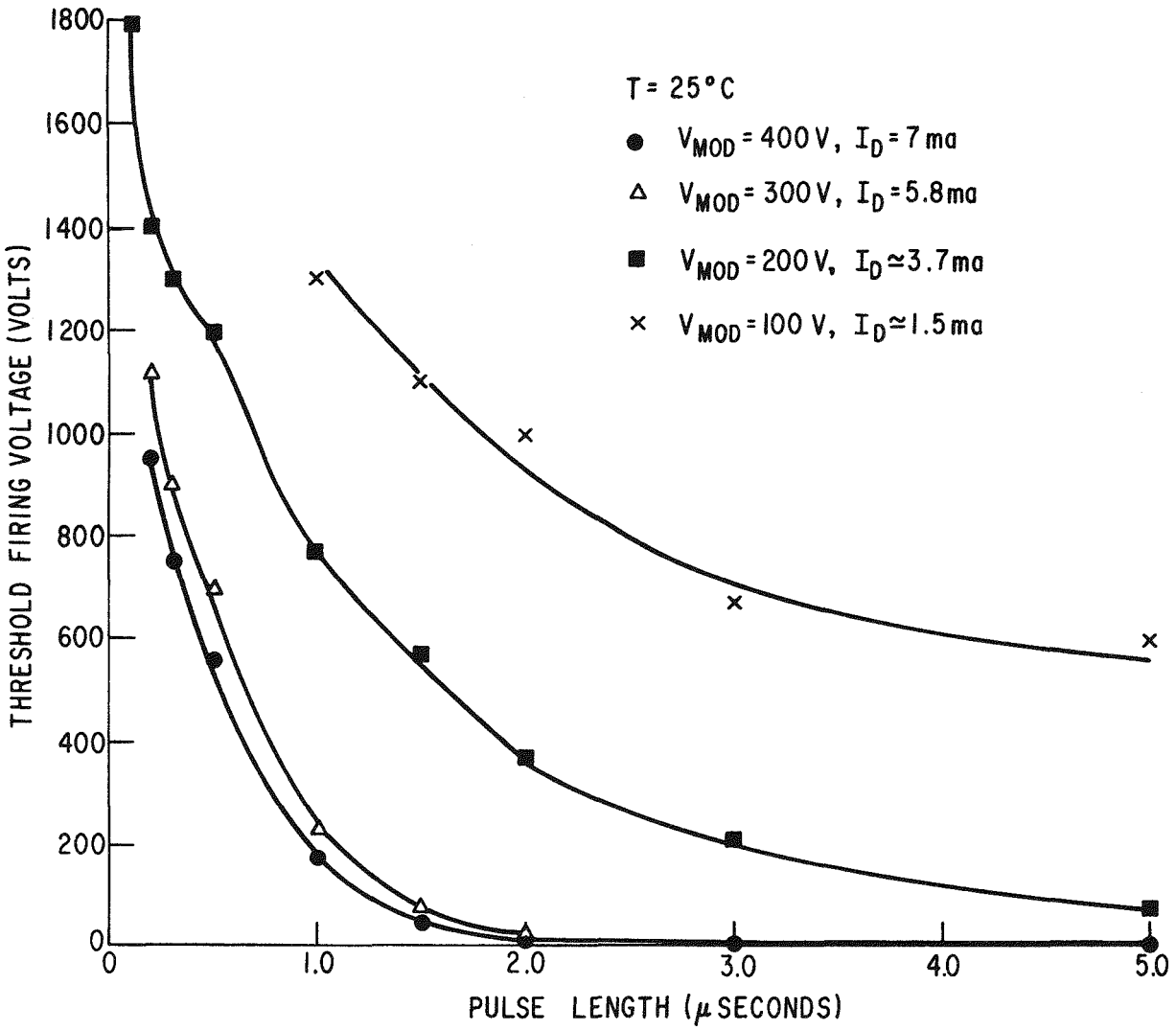


Figure 5-15. Threshold turn-on voltages of device 2-6 at 25°C for different light pulse amplitudes.

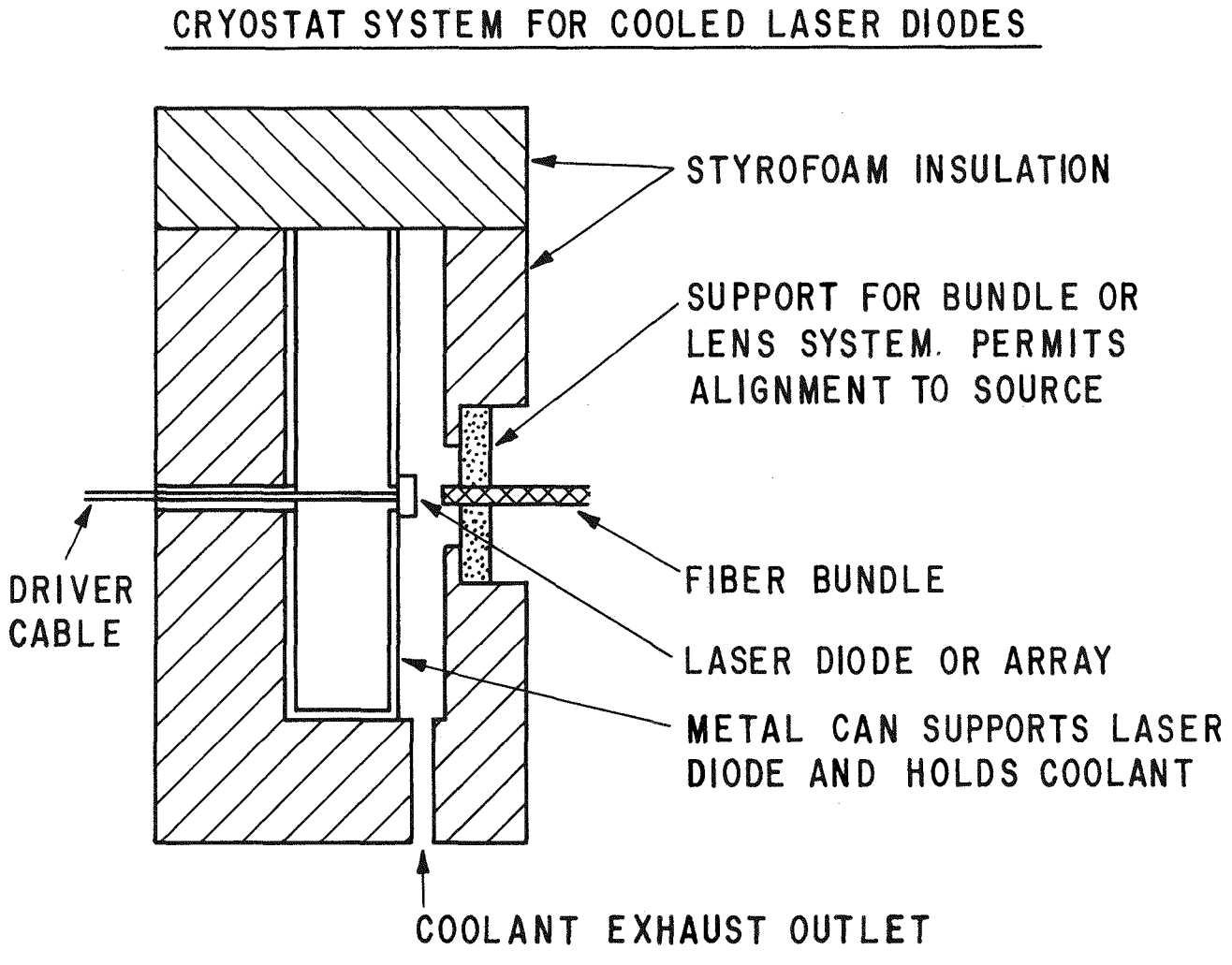
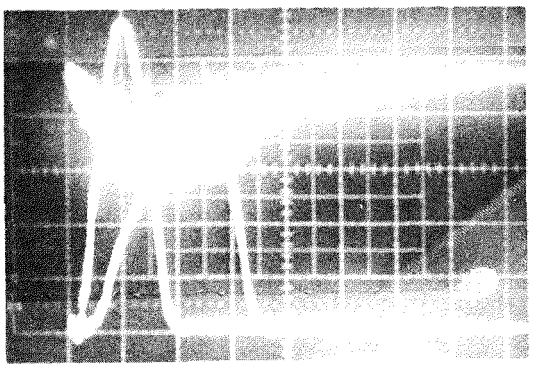


Figure 5-16. Schematic representation of apparatus for light source testing at low temperatures.

.5μsec/div.



Laser Current
4A/div.

PIN Detector
40 ma/div.

Figure 5-17. Light pulse shape of the LD168 laser at 77°K.

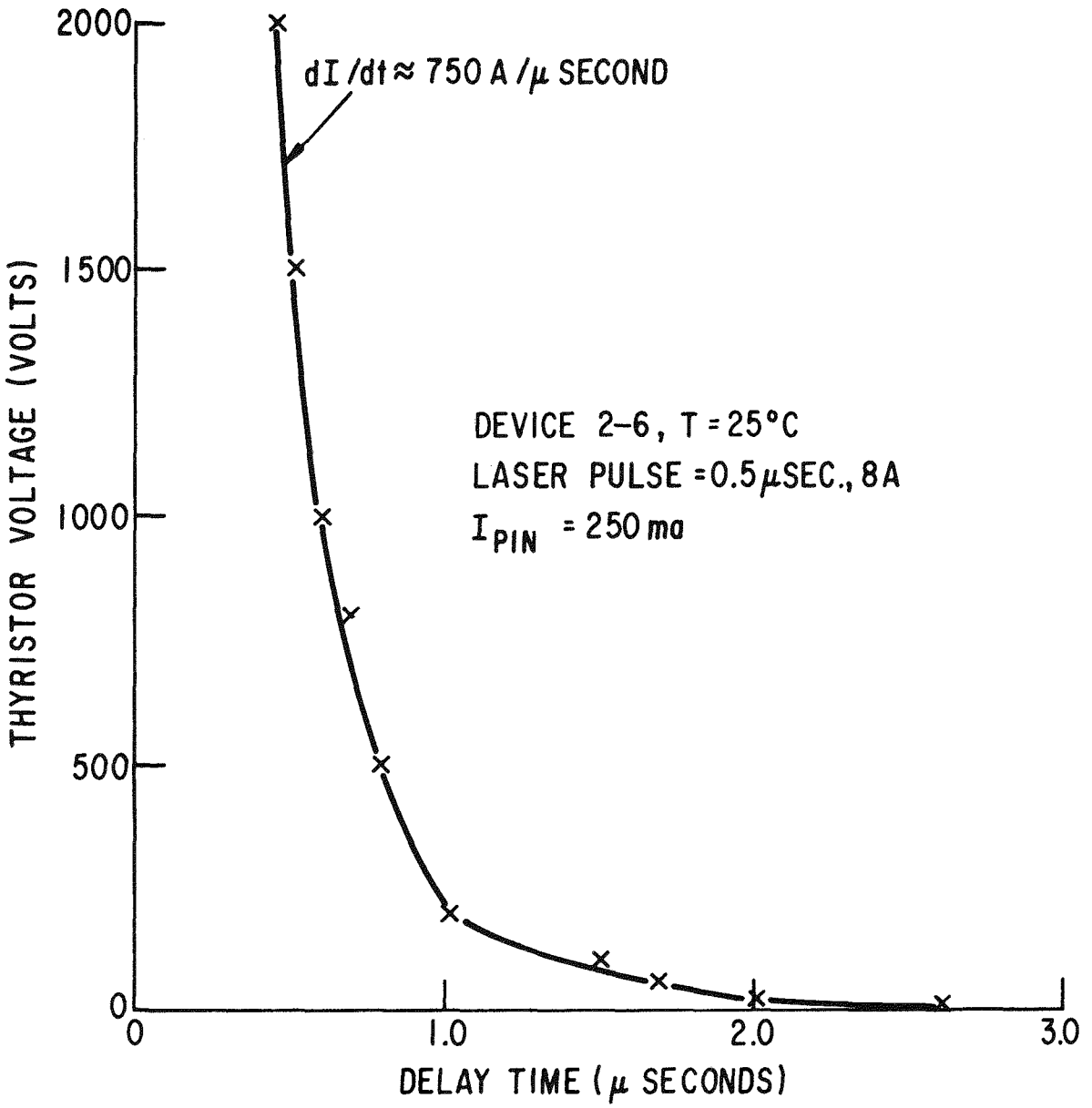


Figure 5-18. Delay time vs. thyristor voltage for the 77°K laser light source for device 2-6.

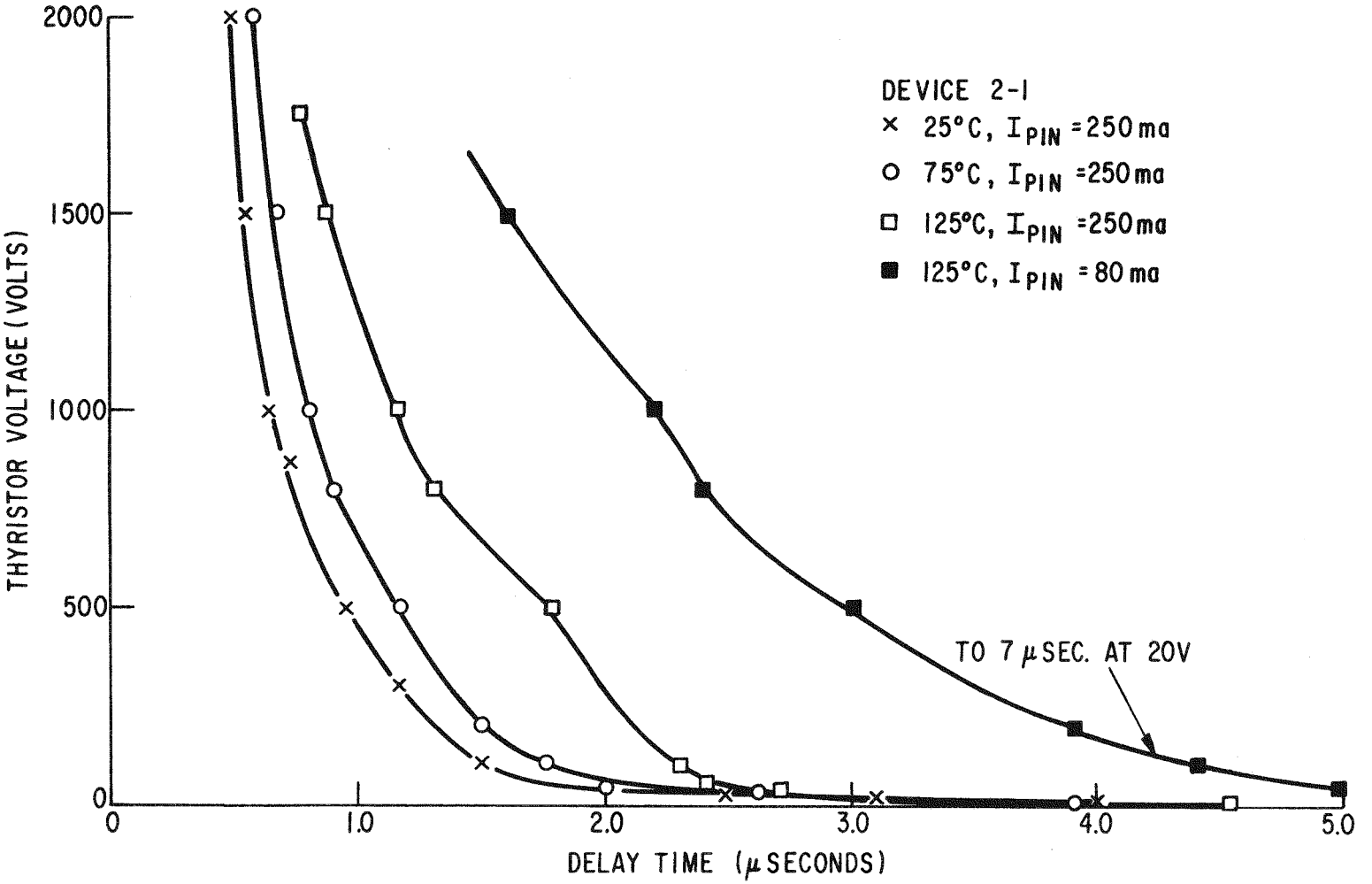
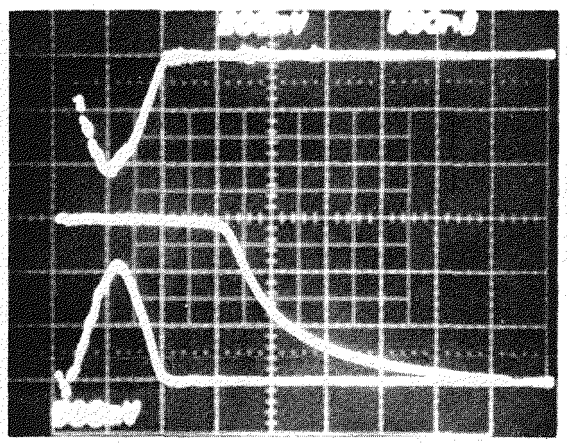


Figure 5-19. Delay time vs. thyristor voltage for device 2-1 at different temperatures for the 77°K laser light source (0.5 μ second pulse length).

.5μsec/div.



Laser Current
2A/div.

Thyristor Voltage
500V/div.

PIN Detector
40 ma/div

Figure 5-20. Typical thyristor turn-on (device 2-1) with the 77°K laser source. Device temperature is 125°C.

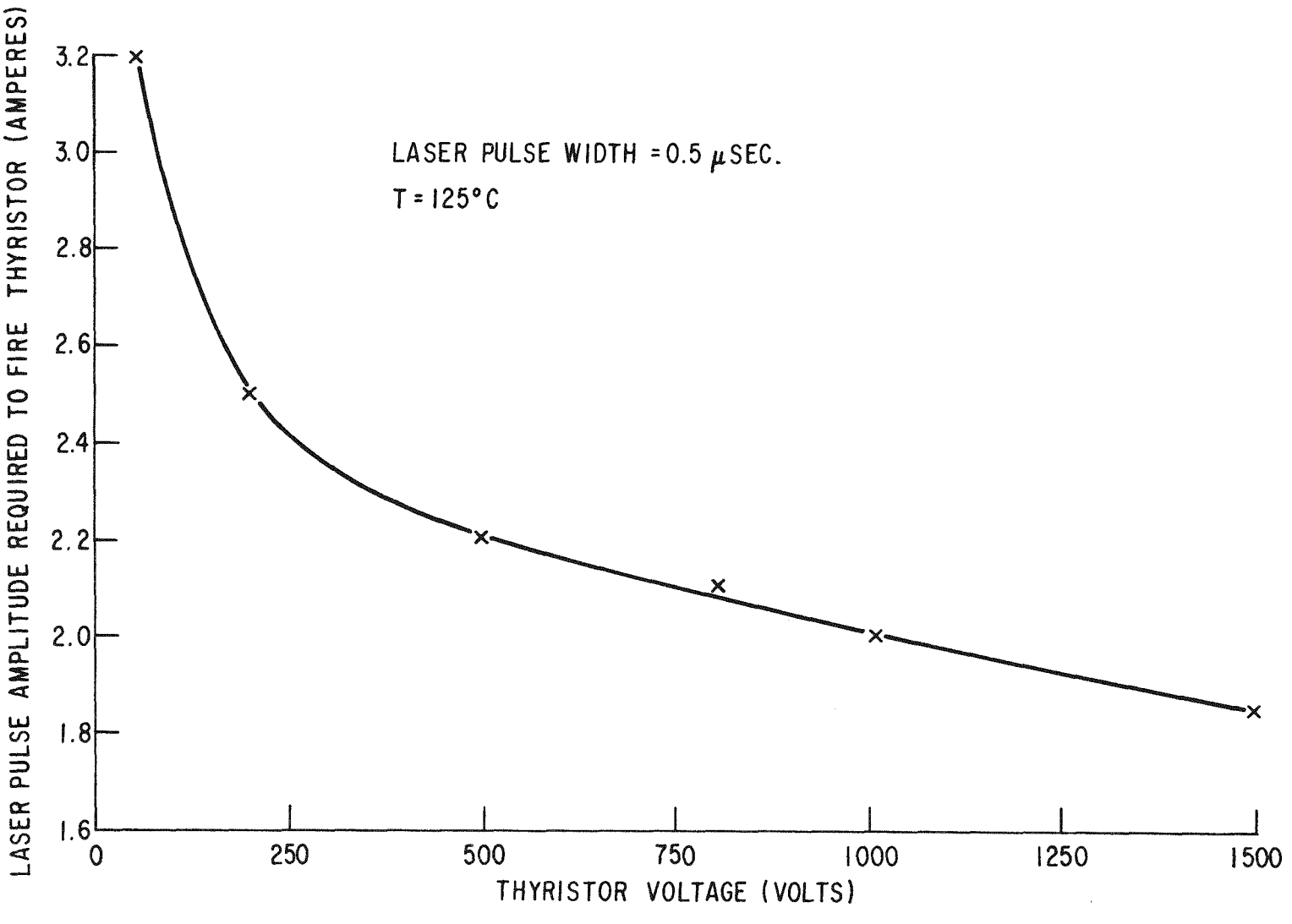


Figure 5-21. Threshold laser current for causing turn-on of device 2-1 at 125°C. The light source is the LD-168 laser at 77°K.

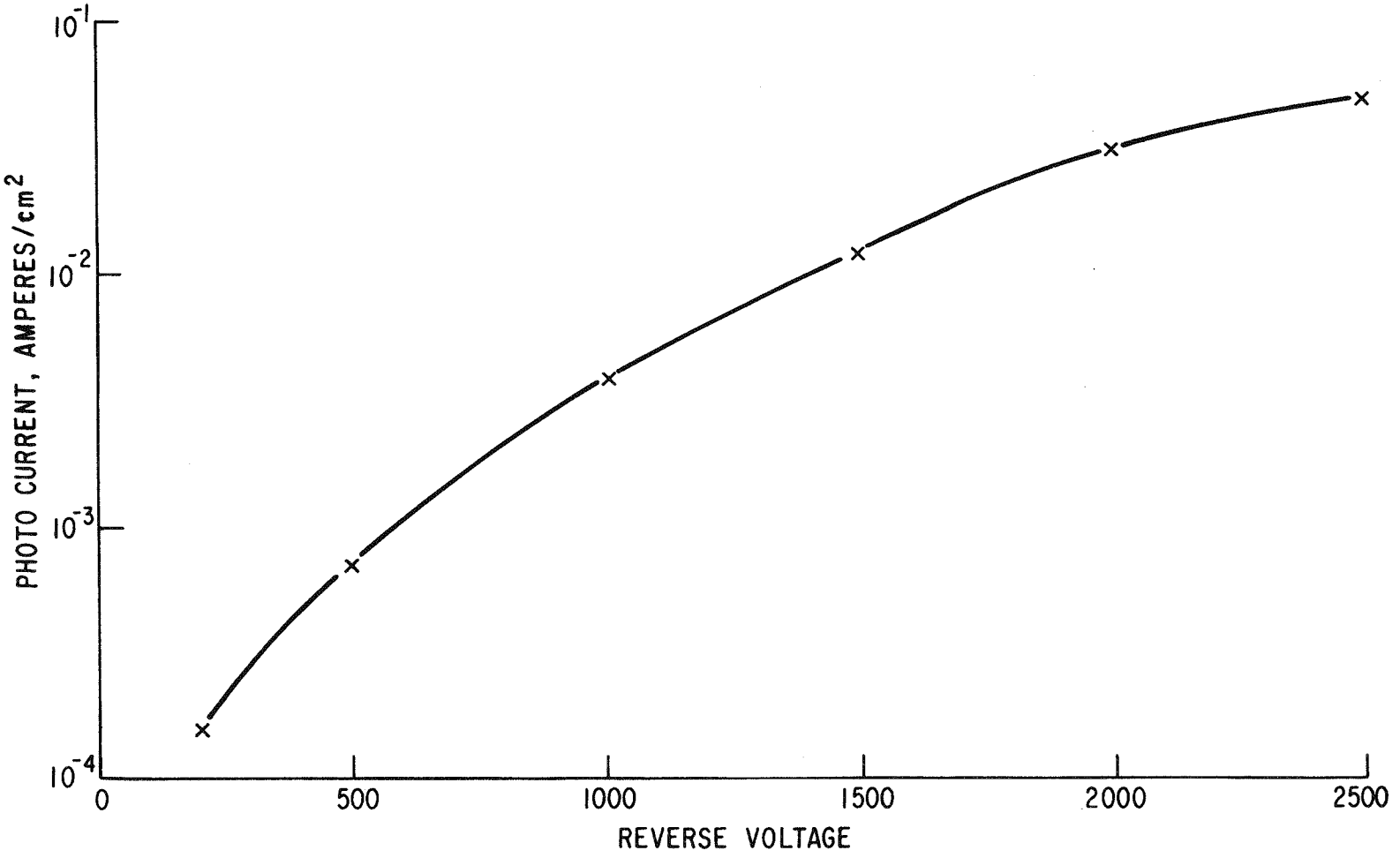
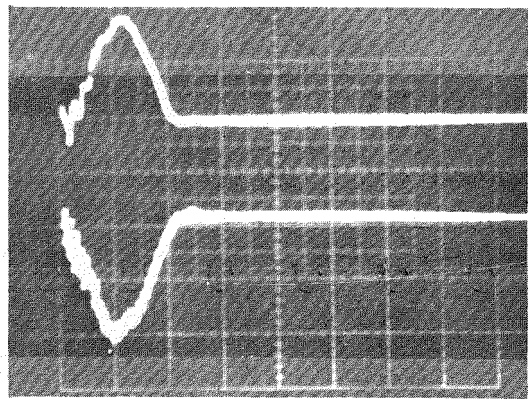


Figure 5-22. Calculated photocurrent as a function of reverse bias for a light source at 9000Å of ∿ 60 m watts.

.5μsec/div.



PIN Detector
40 ma/div.

Laser Current
4A/div.

Figure 5-23. Light pulse used in the reverse bias tests.

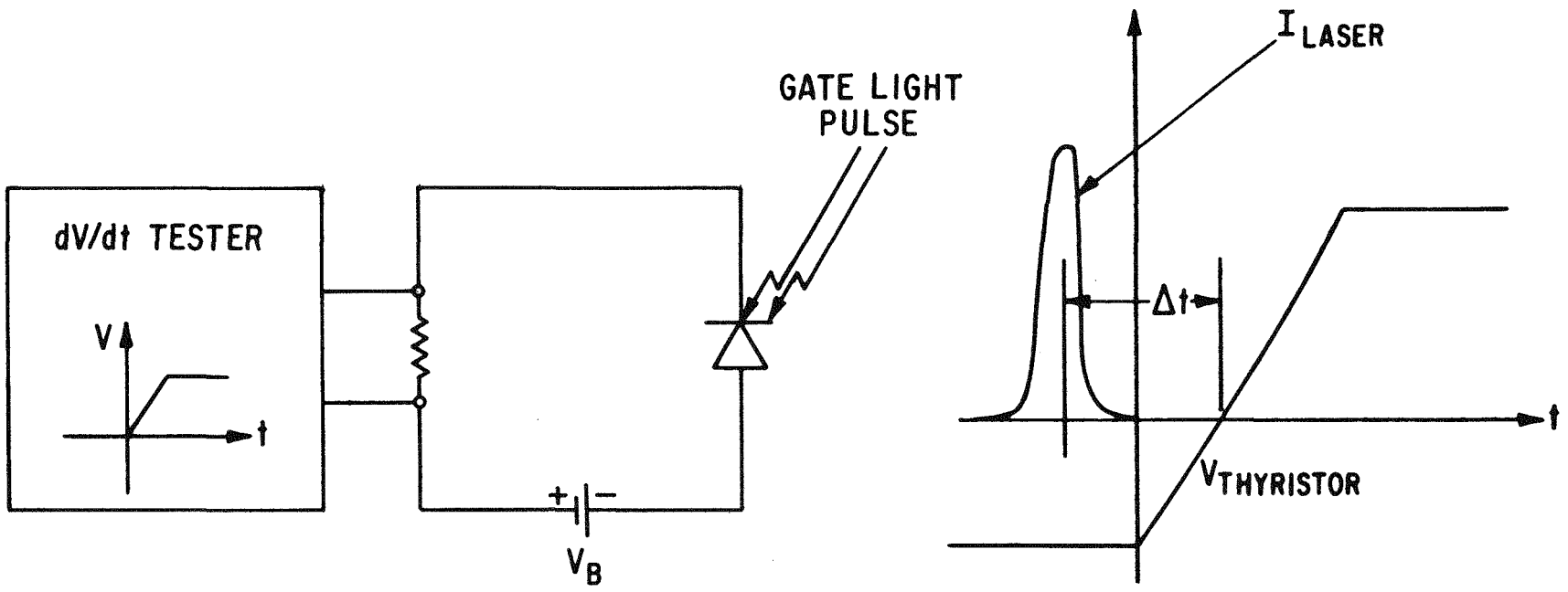


Figure 5-24. Reverse firing test apparatus.

Section 6

EPRI-GE1 DEVICE EVALUATION - RUN #1

INTRODUCTION

During the fourth quarter of this program approximately 25 devices were fabricated jointly at SPCO (Static Power Components Operation) and at CRD (Corporate Research and Development) using the mask set shown in Fig. 5-1, masks 1, 2 and 3 being required for a light fired device with a "large" (40 mil)diameter light sensitive area and masks 4, 5, and 6 being required for a light fired device with a "small" (25 mil)diameter light sensitive area. These devices, for the sake of simplicity, will be termed L or S depending on the light sensitive area being large or small. A number in brackets after the device designation specifies the depth of the mask 1 sensitivity pre-etch in microns. For some comparative testing, L devices could be converted to double amplifying gate electrically fired devices using mask 7 rather than mask 3. Likewise S devices could be converted to double amplifying gate electrically fired devices using mask 8 rather than mask 6. These special test devices were termed LE (for Large Electrically Fired) and SE (for Small Electrically fired) devices respectively. For example #1S(7) identified the number 1 wafer and indicates it to be a device with a small light sensitive region which has been pre-etched 7 microns in the gate thyristor region.

Figure 6-1 shows a schematic radial cross section of one of the finalized devices, device 18L(15). Proceeding radially outward, we encounter first the light sensitive region with its collecting ring, then the gate thyristor with its two levels of n^+ emitter, then the shorted pilot thyristor and finally the shorted main thyristor. The laterial base resistance values, shown schematically in the figure, were obtained from curve tracer characteristics such as those shown in Fig. 6-2.

Upon completion of the devices, a series of tests were performed to establish device characteristics. These tests are arranged in two categories in the following section of the report: those tests which involved actual light fired turn-on and those that did not.

NON-TURN-ON TEST RESULTS

This section shows results of measurements performed at SPCO using standard HVDC tests plus some measurements performed at CRD relating to device turn-on sensitivity. These results are tabulated in Tables 6-1 and 6-2. Column 2 of Table 6-1 lists the etch depth of the "pre-etch" step which can be varied to increase turn-on sensitivity. Columns 3-5 show, in turn, the threshold gate current of the gate, pilot and main thyristor stages as determined by the current break points in I-V measurements such as those shown in Fig. 6-2. Figure 6-3 shows the relationship between etch depth, measured by microscope as the difference in focal distance between the metal covering the two n^+ regions of the gate thyristor, and gate thyristor sensitivity. The large scatter is due to the combined effect of non-uniform starting p-base thickness, etch depth measurement accuracy and an error of $\pm$ 1 ma from selection of the threshold current from the I-V breakpoint. However, the data is able to predict that an etch of 15 μ causes gate sensitivity to approximately double.

Room temperature blocking voltage is shown in columns 6 and 7 of Table 6-1 as measured at 10ma leakage on a 60Hz sinewave. Leakage current at elevated temperatures is shown in columns 8 and 9 at 2600 volts using a 20 μsecond square wave voltage pulse. Figure 6-4 shows theoretical calculations of leakage current originating in the n^- substrate region assuming only n_i, the intrinsic concentration, to be temperature dependent. To predict actual current flow, we must multiply by the thyristor gain which varies with voltage and also with temperature. For example, at 50 volts the appropriate multiplicative factor is approximately 2. This increases rapidly with voltage just as seen in Fig. 5-4 which showed the effective photoresponse with voltage as a parameter.

The final column of Table 6-1 shows the results of a standard dV/dt test. This test consisted of a ramp voltage at 2000V/μsecond up to the voltage shown in the table, followed by a d.c. voltage 10% smaller for 20 μseconds. The ambient temperature was 105°C. Test results showed that the devices could be rated in dV/dt within 10% of 2000V/μsecond.

Table 6-2 shows forward drop measurements made at SPCO at 1000 Amperes in the standard test facility. The measured values compare well to the standard electrically triggered HVDC cell having the same doping profile and main emitter short density.

TURN-ON TEST RESULTS

With the exception of the dV/dt tests, which required no gate, and the forward drop test, which measured a steady state conditon, the results discussed in the previous section did not involve thyristor turn-on and required only standard test apparatus. The results reported in this section involve turn-on measurements which will be discussed under the headings of delay time, turn-on threshold energy, and di/dt capability. The latter category is a bit of a misnomer since it is not yet clear whether initial and follow-on di/dt ratings are sufficient to guarantee reliable turn-on. This will be amplified later in this report.

Turn-on Threshold Energy

In Section V of this report, threshold anode voltage was plotted as a function of pulse length in μseconds for a 1.06 μ YAG laser light source. Data presented there was taken at fixed gate pulse amplitude by setting the pulse width and then increasing anode voltage until the device fired. In the work described in this section, it was attempted to establish a threshold incident photon beam energy which would result in thyristor turn-on. With a fixed pulse half width, the light pulse amplitude was increased at each anode voltage until the device fired. The corresponding rectified photocurrent of a UDT PIN 25 3759 detector was used to calibrate the experiment. In plotting the data in the figures in which photocurrent amplitude is given, the amplitude, unless so specified, is that obtained from the PIN detector. Likewise, the threshold energy is the product of pulse half width, PIN detector current and silicon bandwith. This

means that threshold energy as given in Figs. 6-5 and 6-6 is really that part of the initial incident photon energy that results in rectified photocurrent, I_R^o, in the PIN detector. Equations (6-1) and (6-2) below relate net thyristor gate current I_G, incident photon flux, $F(\lambda)$ and I_R^o.

$$I_G = K\, I_R^o/(1-\alpha_{PNP}M) \qquad (6\text{-}1)$$

$$I_R^o = q\, Q_E\, (1-R)F \qquad (6\text{-}2)$$

where Q_E is the effective quantum efficiency of the light active area of the silicon and R the reflection coefficient, α_{PNP} the current gain of the three lower thyristor layers, M the avalanche multiplication factor and 1 - K the loss due to the misalignment of the light pipe and light active area. From the relationship between detector current and incident photo-power, .3 μa/μw, specified for the PIN 25 detector, it is clear the PIN detector current readings indicate a three times larger incident photo-power. Assuming, as we do, that $Q_E(1-R)$ is approximately the same for the detector and the upper thyristor p-n junction, we can expect photo-gate (I_G) values up to 1.5 to 10 times larger than I_R^o depending on $(1-\alpha_{PNP}M)^{-1}$ which is a strong function of voltage as remarked earlier. For "S" type devices, we have in practice found that there is a variation in I_G for equal I_R^o PIN detector readings due to K being as low, for example, as .3. For "L" devices, K was close to unity for the 14 mil diameter light pipe bundle. It was also unity for the large area PIN detector.

In Figs. 6-5 and 6-6, I_R^o as measured by the PIN detector was multiplied by the bandgap energy and pulse length to convert it into an energy quantity, this being a more appropriate measure of the threshold condition for short pulses. Threshold energy, as measured in this fashion, is plotted against anode voltage for 4 difference pulse widths for device 7S(7) which was one of the least sensitive of all the devices tested, its gate threshold current being 6ma (see Table 6-1). Therefore, the threshold energy plotted in Fig. 6-6 should be viewed as a conservative upper bound. Note that the shorter the gate pulse amplitude, the smaller the net energy required. This is as expected. Note also that regardless of the actual anode voltage, the threshold energies bear a fixed ratio from one pulse width to another. Comparing corresponding curves in Figure 6-5, in which the

thyristor temperature is 25°C and Fig. 6-6, in which the thyristor temperature is 125°C, shows generally lower energy required for the 125°C cases. At V_A = 500 volts and 125°C, for example, it required 25% less energy to turn on with the 200 nsecond pulse and 60% less energy to turn-on with the 1.25 μ second pulse than it did for corresponding pulse widths at 25°C, largely due to a factor of approximately 2 increase in gate sensitivity. From this test we conclude that with the room temperature GaAs laser (pulse width of 200 n sec), the 25°C threshold energy is 14 nj and at 100°C volts it is 6.5 nj.

If electrical turn-on is used, as in device 27SE, or even using the gate ring of device 7S, a much larger gate current is required for the same pulse width since there is no transistor gain as in the light fired device. This threshold current was directly measured and plotted in Fig. 6-7 for V_A = 50 and T = 25°C.

Delay Time Measurements

Turn-on delay time was measured on a large number of devices with different light pulse shapes and ambient temperatures up to 125°C for voltages ranging up to 2000 volts. Figures 6-8 to 6-10 show delay time as a function of photocurrent amplitude (as measured on the PIN detector) for anode voltages from 50 to 2000 volts for device 3S. For a delay time at 50 volts equal to 3 microseconds, approximately 100ma are required. Figure 6-5 shows the threshold for this gate pulse width to be 28 ma (35nj/1.24μsec) indicating a factor of ~4 times threshold to be satisfactory, with respect to delay time, for the 1.25 μsec gate pulse if delay time is to be held below 3μsecs. For a less than 2 μsecond delay time, approximately 7 times the threshold is needed to fire at 50 volts. Corresponding delay times at 4T and 7T (T being the threshold energy) for 1000 volts are 1.7 μseconds and 1.1 μseconds, about half the 50 volt delay times at the same gate amplitude.

Figures 6-11 and 6-12 show similar plots but with a pulse width of 200 nsec. In Fig. 6-11 the energy required for a 3 μsecond delay time is just greater than the threshold. At a 2 μsecond delay time, it is ~1.2T and at a 1 μsecond delay time it is ~1.5T. The corresponding 1000 volt delay times lie between .4 and .6 μseconds.

Results for device 7S are shown in Fig. 6-13. For the 25°C data at V_A = 50 volts and a pulse width of 200 nseconds, a 3 μsecond delay time requires an energy of ~1.3T and a 1 μsecond delay time an energy of 1.6T. Corresponding 1000 volt delay times were between .75 and 1 μsecond. These latter values are much more reliable than the data for devices 3S and 6S since in all cases threshold data was taken from Figs. 6-5 and 6-6 which was also the case for device 7S. The indication, then, is that a short delay time with a 200 nsecond pulse would require a factor of about 2 times the threshold energy. Note that this means a current amplitude 20 times the threshold current (infinite pulse length) listed in Table 6-1.

Figures 6-14 to 6-16 show delay time for device 20. The much larger threshold values indicate very bad light pipe-light active area alignment which was estimated to cause a loss factor of ~5. Similar alignment problems in other devices caused us to make a minor change in the light pipe locator design.

Figure 6-17 shows delay time for device 29. Here the gate pulse width was 1.5 μseconds and it appears that a factor of 5 times the threshold energy is needed for a 3 μsecond delay time turning on from 50 volts.

Turn-on di/dt Tests

Turn-on di/dt was measured for the same range of variables as delay time and for the same devices. One extra variable, however, must be considered, that of snubber design, both resistance which limits the peak current flowing in the device for the "initial turn-on period" and capacitance which, with the resistance, determines the time during which the snubber delivers energy to the thyristor. Most thyristors are rated in di/dt capability at several temperatures and often at several frequencies(9). Sometimes there are two di/dt ratings, an initial di/dt rating which is related to the area of the initial turn-on and a follow-through di/dt rating related to the subsequent spreading of the on-region.

The di/dt measurements and values given in this report are in the nature of initial di/dt such as would be present in snubber circuit discharge. Follow-on di/dt measurements were later made on fully packaged devices on test equipment at SPCO in Collingdale.

The measurements taken do, however, represent fairly definitive tests of the device regions that we were most concerned about - the turn-on area in the very small gate thyristor (first amplifying stage), the turn-on area in the somewhat smaller than normal pilot thyristor (second amplifying stage) and the initial turn-on region (plus some small spreading) of the main thyristor. Figure 6-18 liiustrates the turn-on process with an I vs. t sketch for a turn-on in which the individual portions were sufficiently clear as to be able to assign individual slopes and breakpoints. From t = 0 to t = A photocurrent is causing a build up of holes in the p-base which, under the gate thyristor, is augmented by further hole build up through injection. At t = A the gate thyristor is on. From A to B the current increases through spreading of the n-region in the gate thyristor. In the absence of the amplifying stages the current would tend to increase with a slope asymptotic to that between A and B. This would indeed mean a low di/dt capability. However, during the period between A and B the hole concentration under the pilot emitter (in particular its turn-on line) has been increasing. At B the pilot thyristor has taken over and a jump in the observed di/dt results, reflecting the tenfold increase in turn-on line length. Without the amplifying stage this tenfold jump in current handling would not occur. Just as important is the fact that point B marks the beginning of current cutoff in the gate thyristor, effectively limiting total gate thyristor power dissipation. In a similar fashion the main thyristor begins to turn-on once it has built up a sufficient hole density in the p-base. At point C current flowing in the main thyristor turn-on region is dominant and we find a further jump in di/dt by a factor of about 4, very closely approximating the increase in turn-on line length. Again note that, due to series impedance between each amplifying stage, the pilot thyristor will begin to turn off at point C. At point D, di/dt is limited by the spreading velocity of the turn-on region from the turn-on line of the main emitter. Note that in the EPRI-GE1 design this turn-on line length is twice that of the normal design and, consequently, we predicted a doubling in follow-on di/dt

capability. As stated previously, measuring the "follow-on" di/dt which begins at D requires extremely powerful power supplies and this has not yet been done.

Generally the voltage characteristic has a shape like that of Fig. 6-19. Prior to point A, the snubber resistance and the total base resistances make a voltage divider which sets the anode-cathode potential to 260/260+10) x V_A, 260 Ω being the base resistance between the gate ring and the cathode, as illustrated in Fig. 6-1, and 10 Ω being the snubber impedance. Once the gate thyristor is turned on, the anode-cathode voltage approaches a value determined by base resistance from the gate thyristor metallization to the cathode and snubber impedance, e.g., 50/(50+10) x V_A. At B the pilot thyristor turns on and the voltage falls toward 6/(10+6) V_A. After point D, the voltage drop is governed by the spreading of the on-region. Note that the above analysis is predicated on the rapid fall off in the resistance of the gate and pilot thyristor stages below values of the series p-base resistance. This is only partly true. In fact, in the actual voltage vs. time curves, we can only identify three parts of the curve, the slope betwen 0 and A, a single slope between B and D and than a new slope at D which is more pronounced for low resistance snubbers with a sufficiently large discharge time constant. Also marked in Fig. 6-19 is the conventional delay time as determined by the 90% anode-cathode voltage point. As can be seen, this point occurs shortly after the turn-on of the gate thyristor. Firing at lower voltages, the 90% voltage point is occasionally on the 0-A slope.

Figure 6-20 gives additional insight into the turn-on process, Fig. 6-20(a) showing current for turn-on at 1000 volts and Fig. 6-20(b) voltage for turn-on from 1000, 1500 and 2000 volts. The initial current peak in Fig. 6-20(a) coincides with the gate pulse. The PIN detector current reading was 210 ma, about twice that of Figs. 6-18 and 6-19. Therefore, it is likely to suppose that the current is largely the result of direct conduction. The voltage minimum is just what would be expected on the basis of direct modulated turn-on in the light active region alone.

Figures 6-21 to 6-27 represent an immense number of turn-on measurements made with different temperatures,different gate pulse amplitudes and pulse lengths and different snubber circuits for voltages ranging up to 2000 volts. Most devices were tested to failure. Most commonly its cause was excess leakage current in the light sensitive region following turn-on from 2000 volts at 125^{o}C, actually a much stiffer test than that usually performed on HVDC cells and with a smaller resistance in the snubber. Table 6-3 gives a fairly complete tabulation of the high di/dt device tests.

Figures 6-21 and 6-22 show the effect on di/dt (measured on the BDC portion of the anode current as shown in Fig. 6-18) of increasing the temperature. This is to decrease the turn-on speed in the usual fashion, usually a factor of 2 for every 75^{o}C temperature increase.

Figure 6-23 shows similar di/dt values to those of Figs. 6-22 and 6-23. Despite having a larger pulse width, Fig. 6-24 shows that gate pulse amplitude does not affect the di/dt slope to any large extent as would be expected once the gate thyristor has turned on the next amplifying stage. Figures 6-25 and 6-26 show di/dt values for snubbers with a larger capacitance. The turn-on speed, however, seems to be controlled by the resistor value, that of Fig. 6-24 being 1.6Ω and that of Fig. 6-25 being 20Ω. The 20Ω di/dt values are much the same as the 10Ω cases shown in the previous figures while the 1.6Ω case shows about a threefold increase in turn-on speed.

Looking again at Table 6-3, it is apparent that an initial di/dt (snubber di/dt) of about 300A/μsecond at 1800 volts and 100^{o}C is possible with the light active region and the gate thyristor being the weak link. Follow on di/dt ratings were expected to be higher than normal because of the long turn-on line of the main thyristor and the amplifying gate action.

At this point it was decided to fabricate a second run of devices and to concentrate on further and more complete di/dt testing. A number of devices were, therefore, packaged at SPCO in Collingdale and tested. These results are described in the following section.

TESTS OF PACKAGED DEVICES

Device Packaging

To get a more realistic picture of the di/dt capability of the EPRI-GE1, 7 samples were packaged with three alternative methods. The three variations considered are shown in Fig. 6-28. Note that, with the exception of the O-ring sample, that the main sealing material was an epoxy whose temperature rating was above 150°C. In fact, because the packaging process requires an hour bake at 125 to 150°C before cold welding, a sealant with a higher temperature rating would be desirable. After packaging, the devices were retested for blocking capability with the results shown in Table 6-4.

Devices 2, 13 and 8 were measurably degraded. In fact, devices 2 and 8 were considered unsuitable for further testing because of their low breakdown voltage at elevated temperature. However, all devices were given the manufacturing leak test after electrical testing with the results shown in Table 6-5. The indications from the tests indicated that about 50% of the epoxy seals were leaky. The addition of RTV was not proven to help. A reexamination of the packaging process revealed a likely reason for the 50% failure to seal. While the manufacturer claims high temperature capability, in fact the epoxy softens. In the curing and welding process, this could lead to movement of the locator and a rehardening without an effective seal. For example, on examining device 10 the locator was noticeably moved off center after the welding step. The O-ring sealing was successful but only when the cathode-anode was under pressure so that this sealing technique is impractical.

Device di/dt Tests

Di/dt tests on devices 2, 13, 14, 23, 10, 12 and 1 were performed with only one device passing the one-minute room temperature manufacturing di/dt test. For comparative purposes this test was made using the same equipment and tests as would be made on the electrically triggered device (G.E.'s 6RT101) being used in HVDC systems presently under construction. Normally, close to 100% of the 6RT101 devices would pass this test. However, as can be seen from Table 6-6, not all of the failures were due to di/dt. For example, devices 12, 23 and 13 failed due to a packaging problem associated with the extension of

the pilot metallization finger (this finger can be seen in Figures 4-2 and 5-1) under the main cathode contact. Unfortunately devices 23, 13, 2, 12,1 and 10 were all packaged with this finger unprotected by any isolation. Thus, to a large extent the di/dt test results merely revealed the finger-to-cathode arc voltage. This was certainly true of the results for devices 23, 13 and 12. In all of the cases, the light intensity falling on the surface was only of the order of 2-4 times the threshold value. In devices 1 and 10, this low gate signal gave undesirable jitter in the turn-on. Tests with these devices were not continued to failure because of the already identified finger-to-cathode arc problem.

Devices 2 and 14 failed destructively at the pilot turn-on line at relatively large di/dt values. In device 2, the failure was at 500A/μsecond at a voltage below the finger-to-cathode arc voltage so that this result can be credited. In device 14, the finger was protected with polyimide passivation and was therefore the only device to be truly tested for di/dt capability. The results obtained on this device in the manufacturing test facility were similar to those obtained at CR&D* in the sense that marginally satisfactory room (and slightly above) temperature di/dt results were obtained while elevated temperature results were unsatisfactory.

Light Pipe Centering vs. Sensitivity

One of the weaknesses of the epoxy seal for the light pipe locator was its tendency to soften and move during the packaging process. This, it is felt, could lead to lower di/dt capability because of the possibility of local turn-on at one part of the turn-on periphery of the gate thyristor. This effect was investigated using a light pipe with a single fiber, moving the fiber across the light sensitive region of the thyristor and measuring the threshold energy needed to turn the device on as a function of position. The results are shown in Fig. 6-29 which also shows, in cross-section, the center region of the thyristor which was, in this case, a type S device. Note the relatively constant threshold for the light pipe positioned interior to the gate ring and the otherwise almost four times lower threshold which occurs when the gate ring is no longer able to distribute the flow of photo-current evenly along the gate thyristor turn-on line.

* General Electric Corporate Research & Development Center, Schenectady, New York.

From the results in Fig. 6-30, it would seem that variations in delay time could easily result from misaligned light pipes.

CONCLUSION

All of the tests performed to this point indicated a substantial degree of success in achieving an HVDC prototype light fired thyristor. Measurements showed excellent light sensitivity with threshold light triggering at 10 to 30 nanojoules and with a 2000V/μsecond dV/dt capability, that is, a device with almost a two order of magnitude increase in gate sensitivity but with the same dV/dt rating as the original electrically fired device. Blocking voltage and forward drop were similar to the electrically fired device while delay times were somewhat reduced, even at relatively low gate overdrive factors.

What is somewhat disappointing but not totally unexpected was the degree of dependence of the device di/dt rating with ambient temperature. In Table 6-3, light fired devices withstood di/dt's of the order of thousands of amperes per microsecond at room temperature. The higher temperature di/dt ratings are not yet established but are certainly inferior to those of the electrically fired device. Therefore, a second run of EPRI-GE1 thyristors was fabricated and a further study of the EPRI-GE1 undertaken to understand this dependence. At the same time, a computer program was developed to model the turn-on of multi-amplifying gate thyristors. These efforts have been largely successful and point to a new design and new design concepts for improved di/dt capability which will be elaborated upon in the next section of this report.

Table 6-1

EPRI-GE1 THYRISTOR PROPERTIES

Device #		Etch Depth (μ)	Threhold Turn-on (1) Gate (ma)	Pilot (ma)	Main (ma)	Room Temp. Blocking Voltage (2) Forward, Reverse (Volts)		125°C 2600 Volt Leakage (3) Forward, (ma)	Rev. (ma)	2000V/μsec 105°C dV/dt test (4) (Volts)
1	S	10	4	35	300	2680	2930	30	12	2250
2	S	13	4	30	350	2760	2940	50	20	2250
3	S	9	4.5	35	300	2820	2970	40	17	2200
4	S	17	2.5	25	250	2730	3060	40	15	1980
6	S	12	3.5	35	280	2800	3080	40	18	2100
7	S	7	6	30	300	2700	2860	50	23	2350
8	S	17	3	30	300	2500	2790	55	25	2000
10	S	7	4	25	300	2760	2900	40	10	1950
11	S	13	3.5	30	300	2770	2970	50	15	2000
12	L	9	5	50	250	2800	3050	30	15	2100
13	L	10	4.5	25	280	2480	2340	35	25	2000
14	L	9	4	25	350	2750	3160	50	30	1950
16	LE	4	4.4	25	260	2690	3140	30	10	2000
17		15	4	28	300	2680	2970	30	15	2100
19	S	12	4	30	300	2740	3160	40	35	2100
20	L	7	5	30	300	2700	2930	25	8	2100
23	L	10	7	30	330	2850	2920	30	12	2300
24	S	11	4	22	260	2800	3030	30	7	1900
25	L	7	6	25	300	2700	2850	25	10	1850
26	L	14	3.5	22	240	2800	2900	30	10	1650
27	SE	9	4.5	30	350	2700	2880	25	8	2100
28	S	17	3	30	300	2690	2920	10	8	2100
29	L	10	5.5	30	240	2760	3020	10	10	2000
33	S	8	4.5	30	330	2760	3030	14	12	2150
35	L	15	3.5	25	280	2790	2900	30	8	1900

NOTES:
1) Breakpoints of gate-cathode I-V (anode open) to an accuracy of 1, 5, 25ma respectively.
2) Measured with a 60Hz sinusoidal waveform to a 10ma leakage current.
3) Measured with a 60Hz 20μsecond wide pulse to 2600 Volts.
4) Measured with a 2000V/μsecond signal to the voltage shown.

Table 6-2

TYPICAL FORWARD DROP AT 1000 A
(in volts)

DEVICE #	FORWARD DROP
5	1.223
12	1.256
15	1.275
18	1.266
21	1.254
26	1.235
30	1.261
31	1.270
32	1.302

Table 6-3

DEVICES LIGHT TESTED WITH HIGH di/dt

DEVICE #	TEST PROCEDURE	SNUBBER	MAXdi/dt	FAILURE MODE
3* S(9)	25°C,75°C at 2000V	.1μf,10Ω	950	None observed
	125°C at 1800V	"	300	Leakage current turn-on at 1500V
	100°C at 1800V	"	350	Increased forward & reverse leakage.
25* L(7)	25°C at 2000V	2μf,1.6Ω	2000	Greatly reduced blocking voltage both forward & reverse.
29* L(10)	25°C at 2000V	2μf,1.6Ω	2000	None observed
	75°C at 1500V	"	1000	Leakage turn-on.
35**L(15)	25°C at 2000	.1μf,10Ω	1000	Leakage turn-on.
26**L(14)	25°C at 2000	.1μf,10Ω	1000	None observed
	75°C at 2000	"	800	Leakage turn-on at 1500V (100°C) and 1650V (25°C)
7* S(7)	25°C at 2000	.1μf,10Ω	1000	None observed
	100°C at 1850	"	300	"
	125°C at 1300	"	115	"
	25°C at 2000	"	1000	Slightly higher leakage current
20**L(7)	Same as device 7	--------	------	----------
4**S(17)	Same as device 7	--------	------	----------
	25°C at 2500V	.1μf,10Ω	------	Leakage turn-on at 1300V
6**S(12)	25°C at 2000V	.1μf,10Ω	1000	None observed
	100°C at 2000V	"	400	Failure with marginal gate drive.

* Devices fired with 1/2μsecond risetime, ** with 50nsecond risetime.

Table 6-4

BLOCKING CAPABILITY AFTER PACKAGING

DEVICE #	SEALING TECHNIQUE	RT(25°C) V_{DM}/I_{DM} (V/mA)	RT(25°C) V_{RM}/I_{RM} (V/mA)	125°C V_{DM}/I_{DM} (V/mA)	125°C V_{RM}/I_{RM} (V/mA)
2	EPOXY	2790/.4	2400/1 UNSTABLE	2000/25	2050/16.5BKDWN 1100/9.5
13	EPOXY & RTV	2480/5	2280/5	2600/33	2570/25LOOP
23	O-RING	2800/2	2800/5	2600/40	2600/12.8
10	EPOXY & RTV	2735/1.4	2865/.5	2500/30	2600/13
1	EPOXY	2740/1.9	2910/1	2500/27	2600/11
12	EPOXY	2600/N	2790	2350/28	2600/18
8	O-RING	2535/.5	2150 DRIFT	1350/20	1800/20 FLOAT

(PRESSURE HAD TO BE INCREASED TO MAKE CONTACT.)

Table 6-5

RESULTS OF LEAK TESTS

DEVICE #	SEALING TECHNIQUE	RESULT	COMMENT
2	Epoxy	Passed	
13	Epoxy and RTV	Passed	RTV does not look fully cured.
23	O-Ring	Leaky	Not effective unless device under pressure.
10	Epoxy	Leaky	Leaks both inside and outside of tube.
12	Epoxy	Passed	
1	Epoxy	Small Leak	Very small leak on both inside and outside of tube.
8	O-Ring	Leaky	Leak inside tube (i.e. in epoxy seal).
14	Locator broke free before packaging.		

Table 6-6

di/dt TEST RESULTS

DEVICE #	TEST CONDITION	di/dt	FAILURE MECHANISM
23	-------	-----	Finger not protected with isolation.
13	1000V, 70A snubber	240A/μsec	Finger not protected with isolation.
2*	1000V, 70A snubber	500A/μsec	Failed destructively at the pilot turn-on line.
12	-------	-----	Finger not protected with isolation.
1**	700 to 800 Volts No snubber	-----	Turn-on delay jitter.
10**	(i) 1250V, no snubber	-----	Turn-on delay jitter.
	(ii) 1000V	75A/μsec	
14***	(i) 1500V, no snubber	110A/μsec	-------
	(ii) 1500V	110A/μsec	Passes room temperature test.
	(iii) 1300V, T_J elevated	90A/μsec	Failed destructively at the pilot turn-on line.

* (a) This device before testing was below standard in breakdown voltage. (b) The epoxy seal was found to be pliable when the package was opened.

** This turn-on is deemed undesirable. It is believed to be caused, in part, by poor light pipe centering and in part by the absence of the snubber. Device #10 was fired by a gate pulse barely above threshold which also contributes to delay time jitter.

*** This device was the only device with proper finger isolation protection.

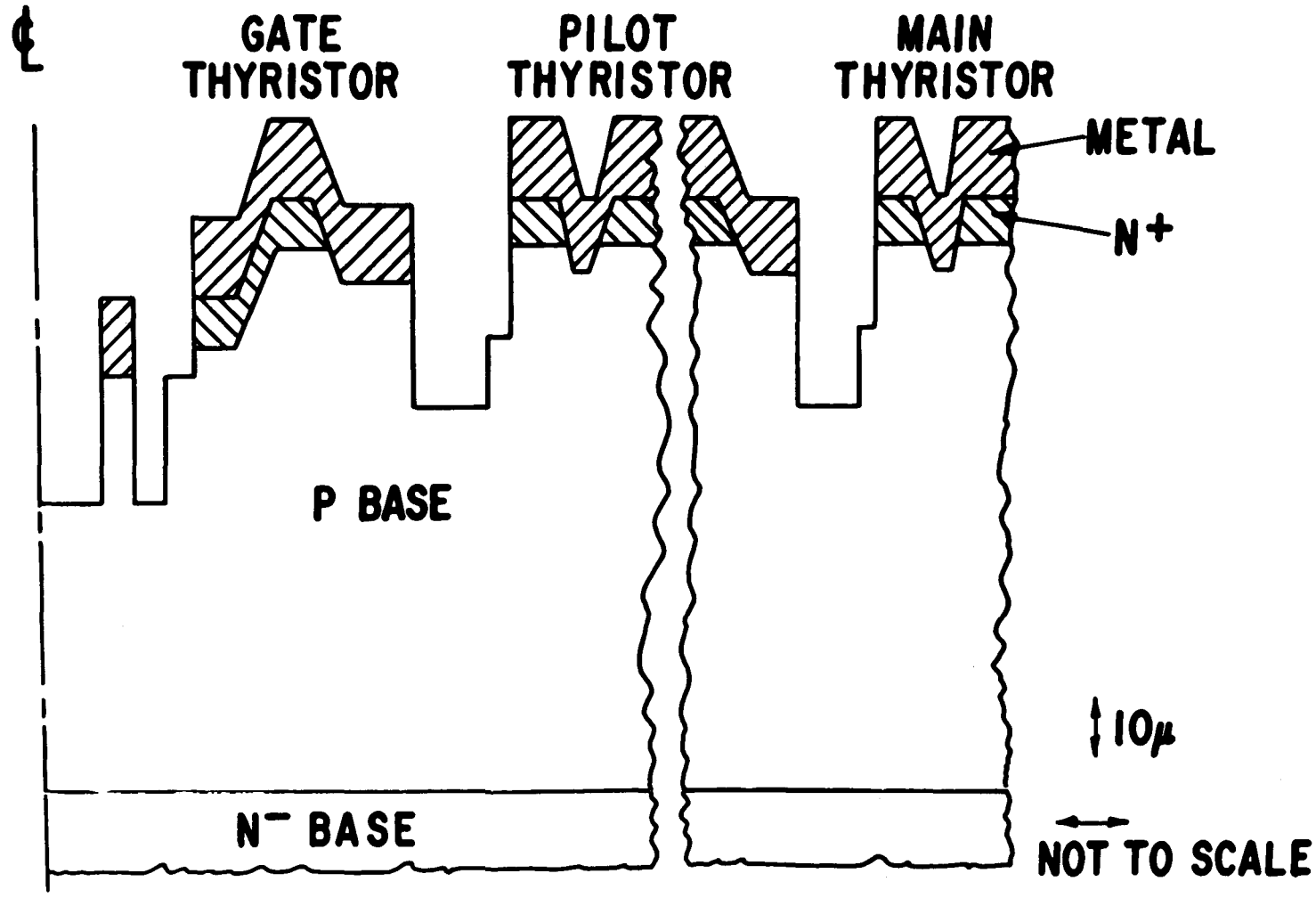
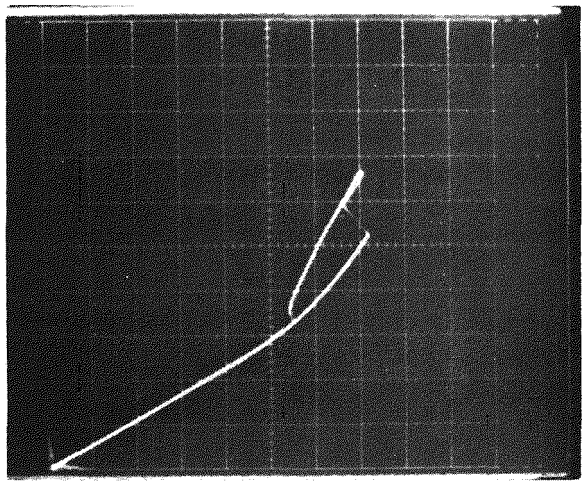


Figure 6-1. Partial radial cross section of an EPRI-GE1 thyristor showing gate ring, two-level gate thyristor stage, and shorted pilot and main emitter stages.

SIMPLE TURN-ON THRESHOLD MEASUREMENT



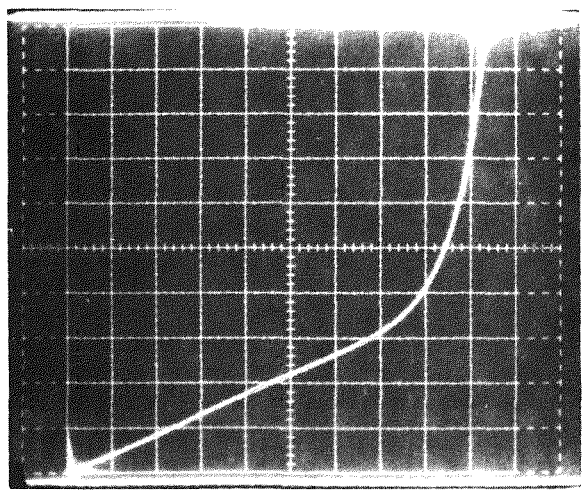


Figure 6-2. Measurement of thyristor turn-on thresholds and lateral base resistance.

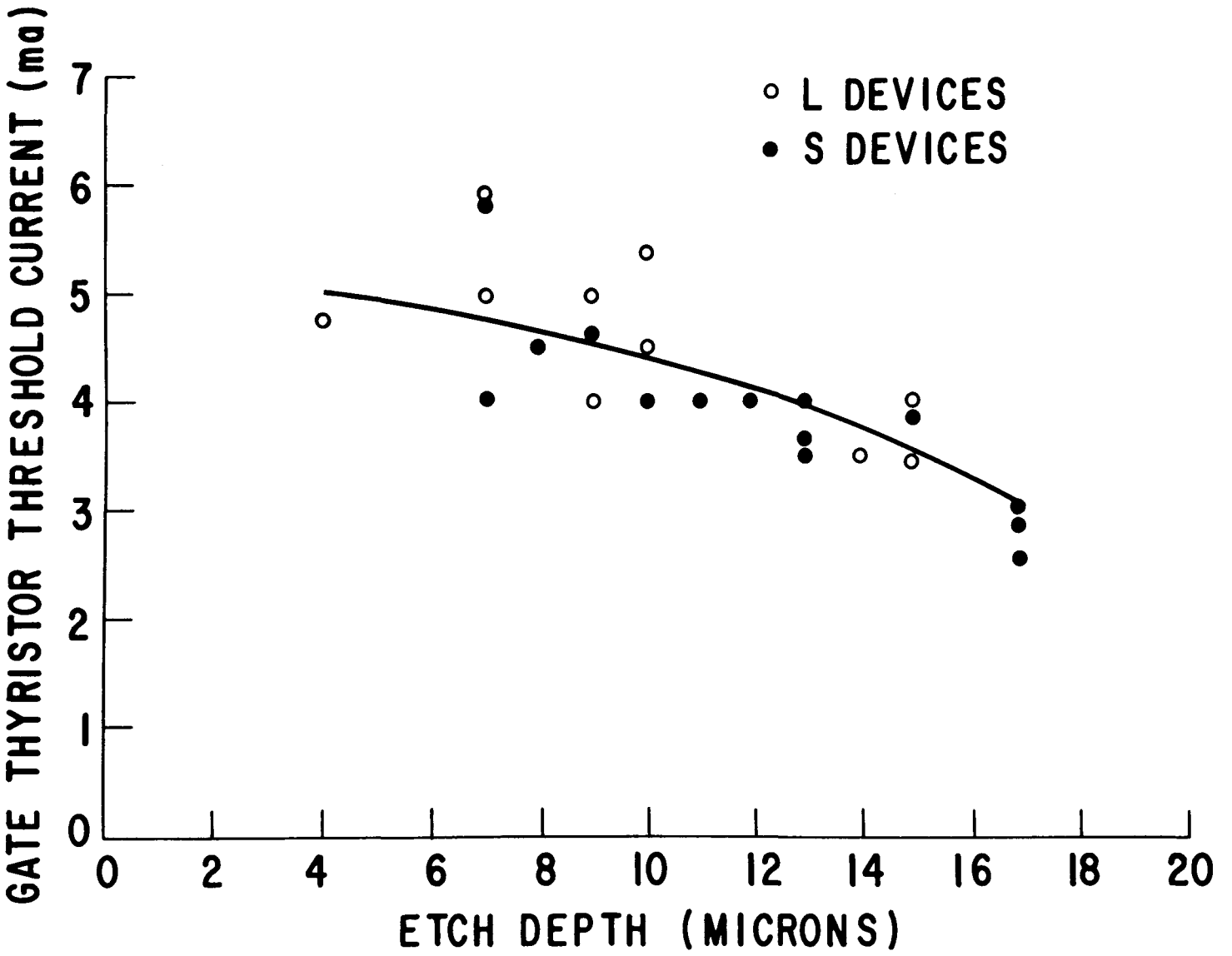


Figure 6-3. Measured gate threshold currents as a function of the pre-etch step depth.

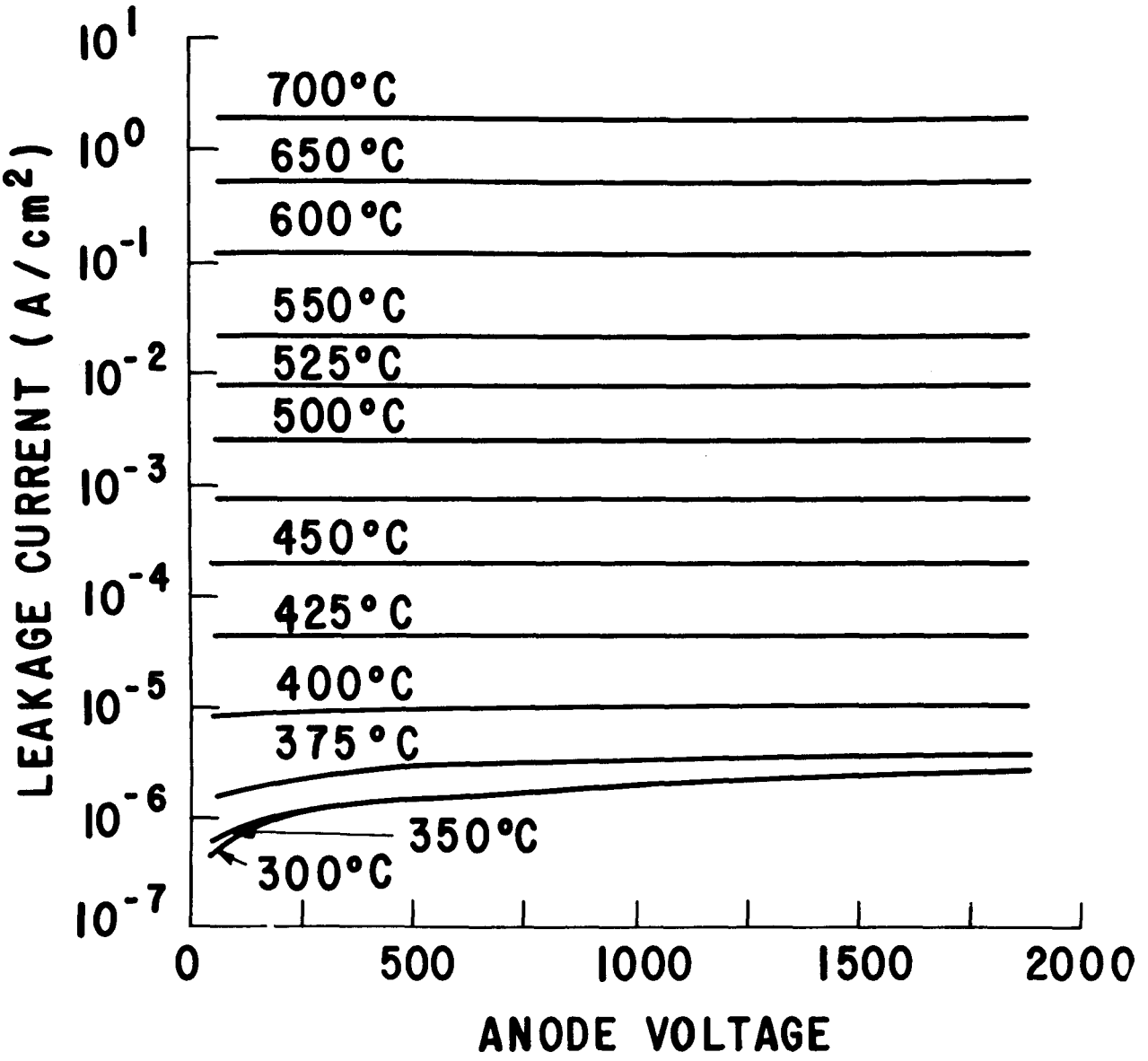


Figure 6-4. Approximate leakage current of a p-n diode having the same doping profile as the p_{base}-n_{base} region of the EPRI-GE1 thyristor.

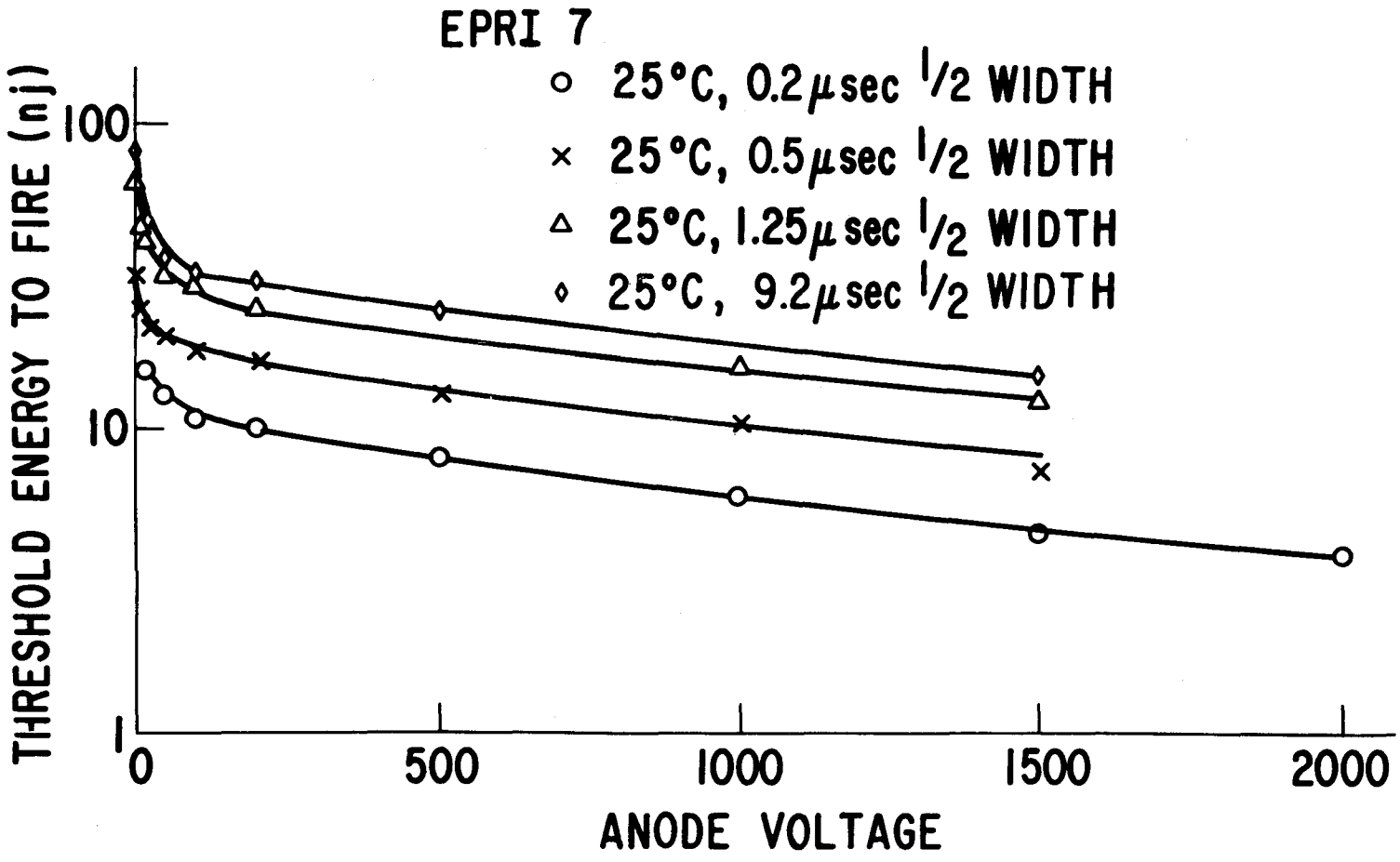


Figure 6-5. Threshold energy for room temperature thyristor turn-on (see text) for different light pulse lengths. The light pulse was provided by a solid-state GaAs laser (9000°A) operated at 77°K for the 0.5, 1.25, and 0.2 μsecond half widths.

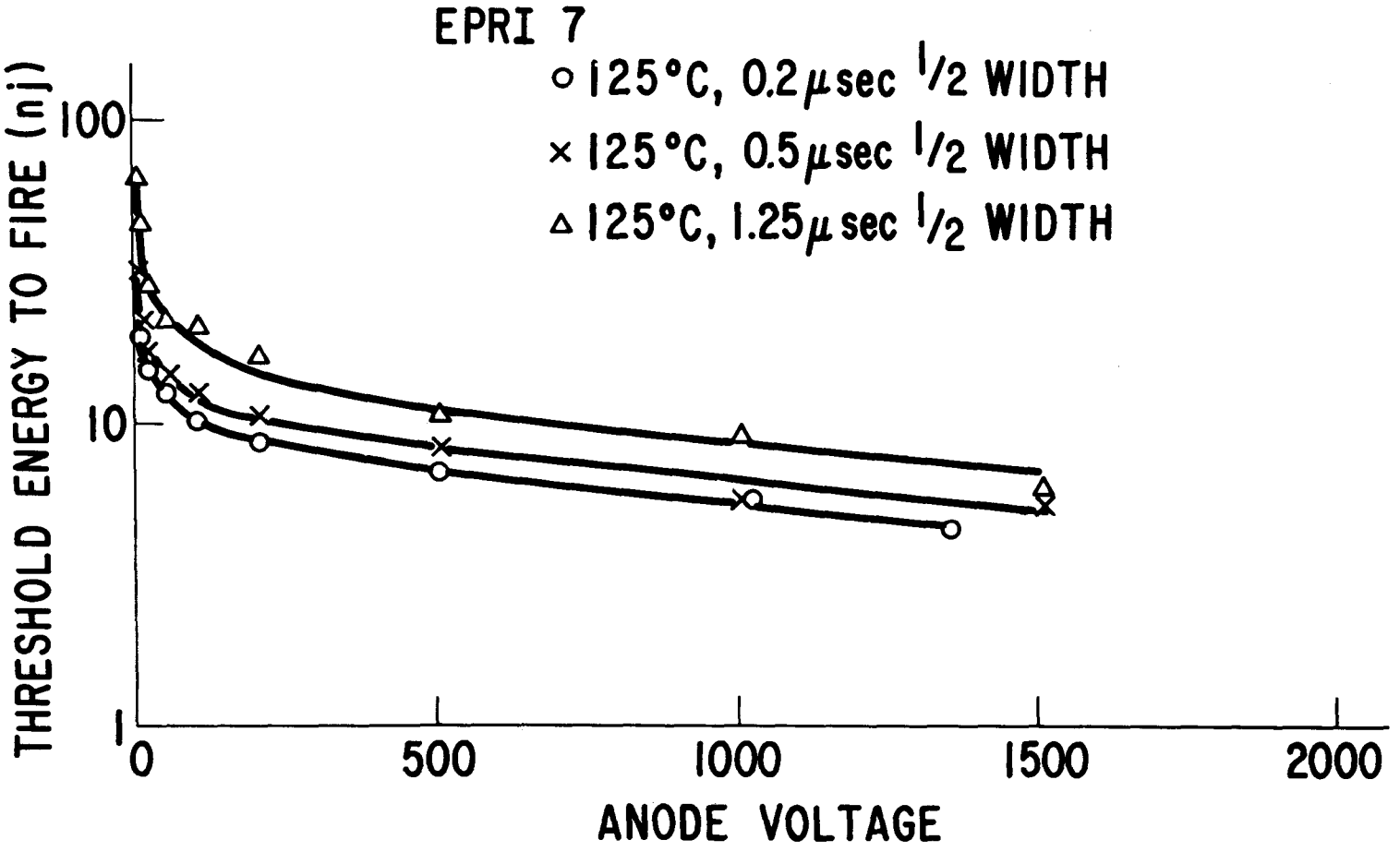


Figure 6-6. Threshold energy for elevated temperature thyristor turn-on for different light pulse lengths.

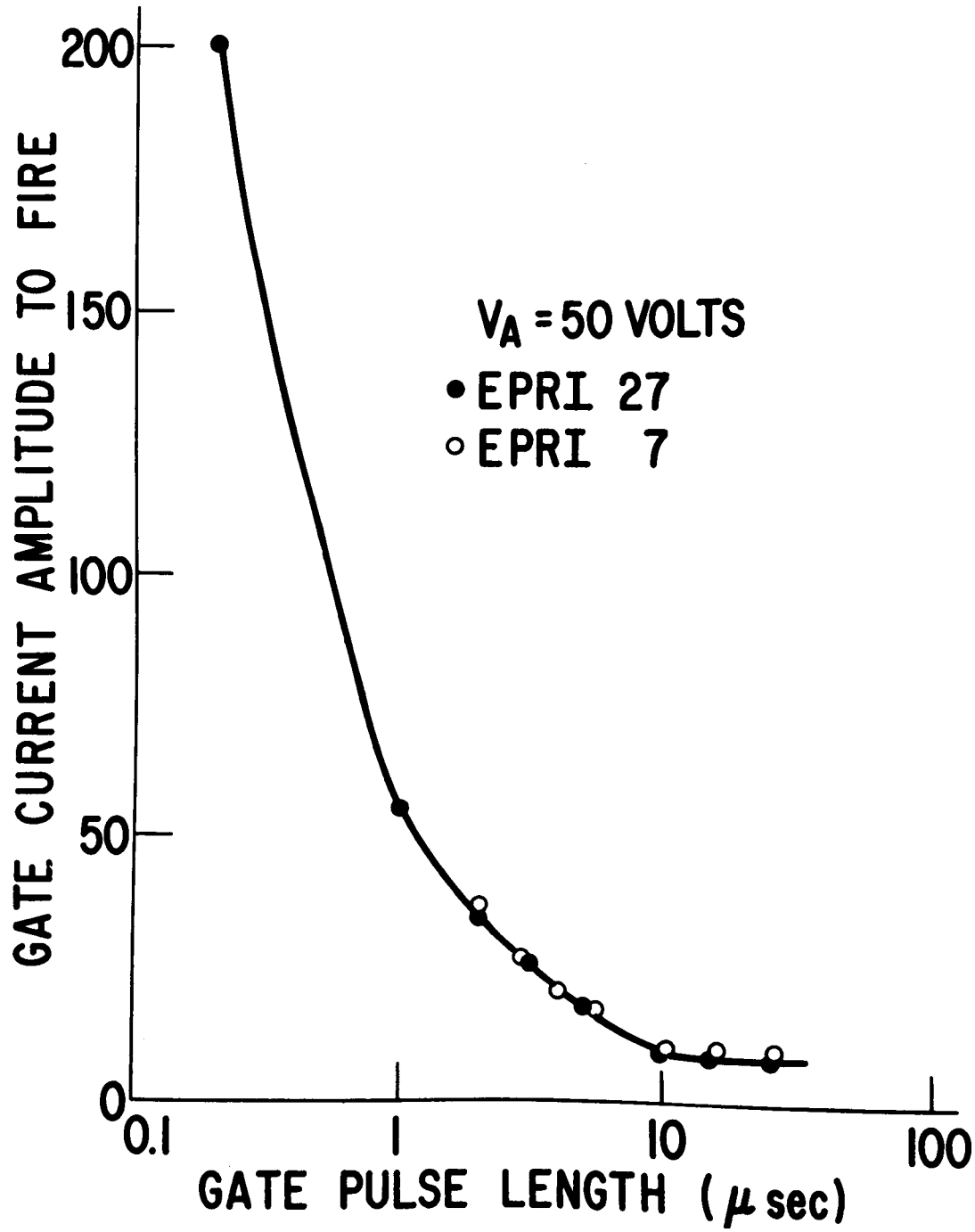


Figure 6-7. Threshold electrical gate current to fire as a function of pulse half width.

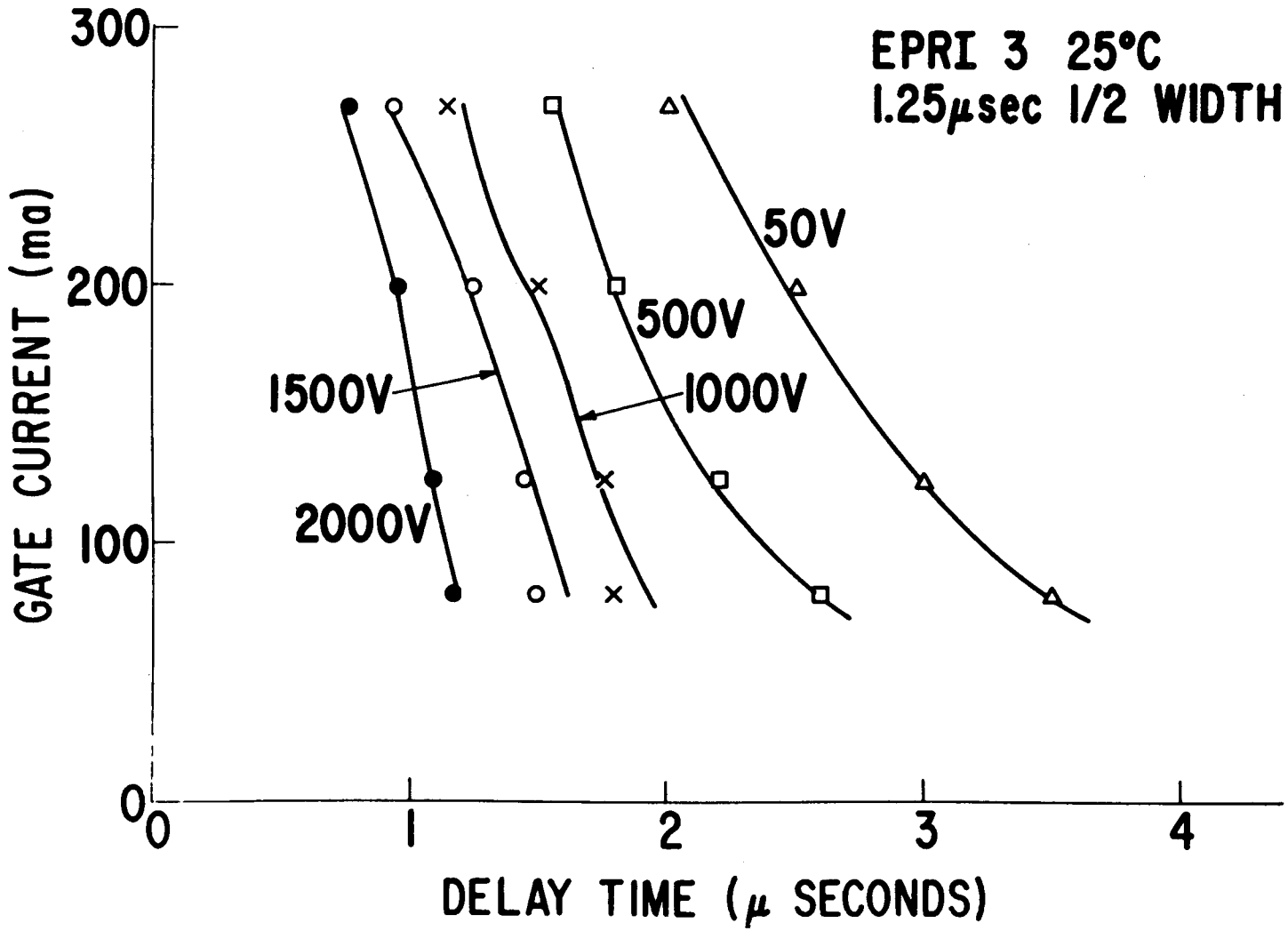


Figure 6-8. Variation of 25°C turn-on delay time vs. gate pulse amplitude for different anode voltages. Gate pulse width - 1.25 μseconds.

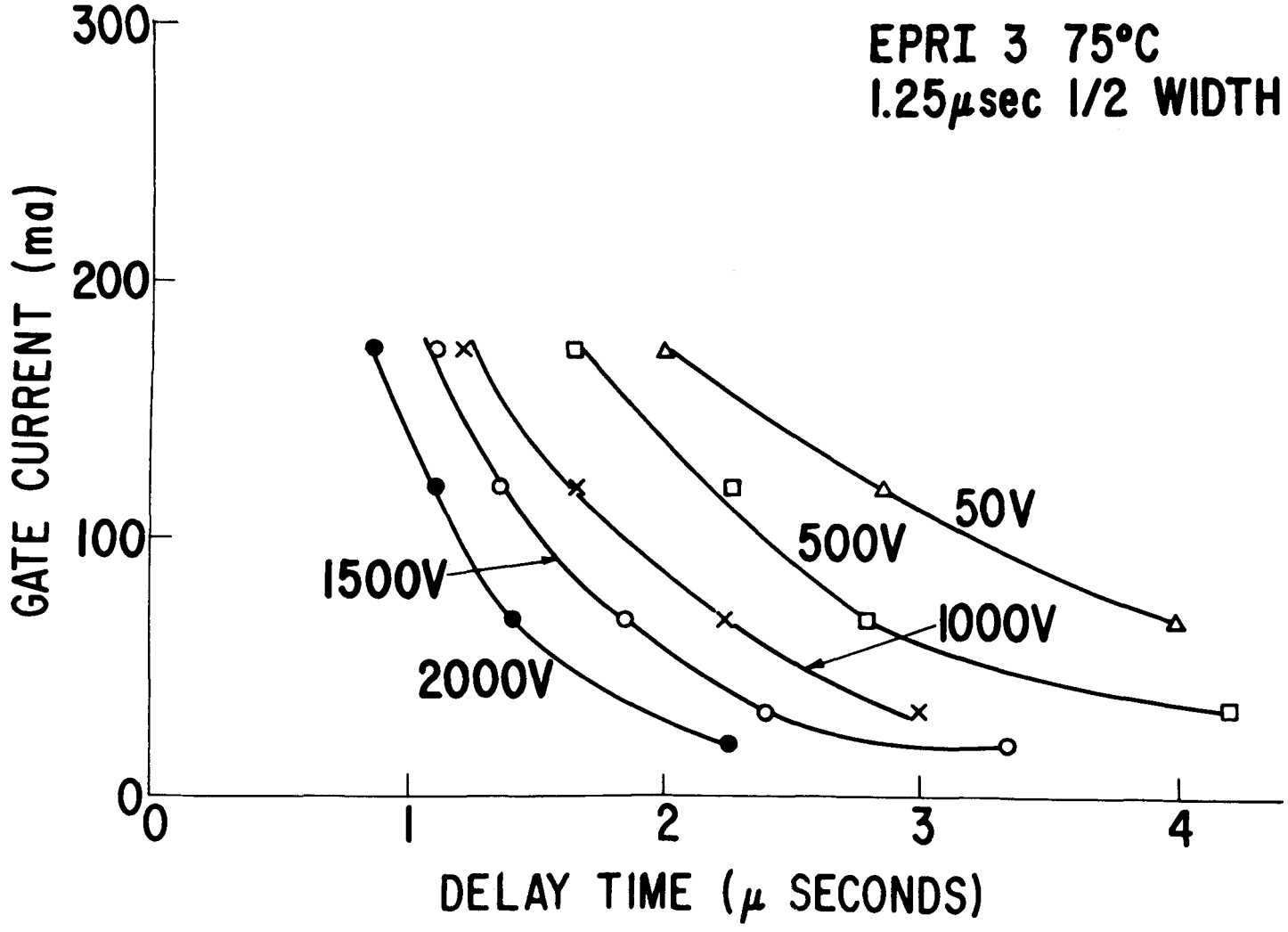


Figure 6-9. Variation of 75°C turn-on delay time vs. gate pulse amplitude for different anode voltages. Gate pulse width = 1.25 μseconds.

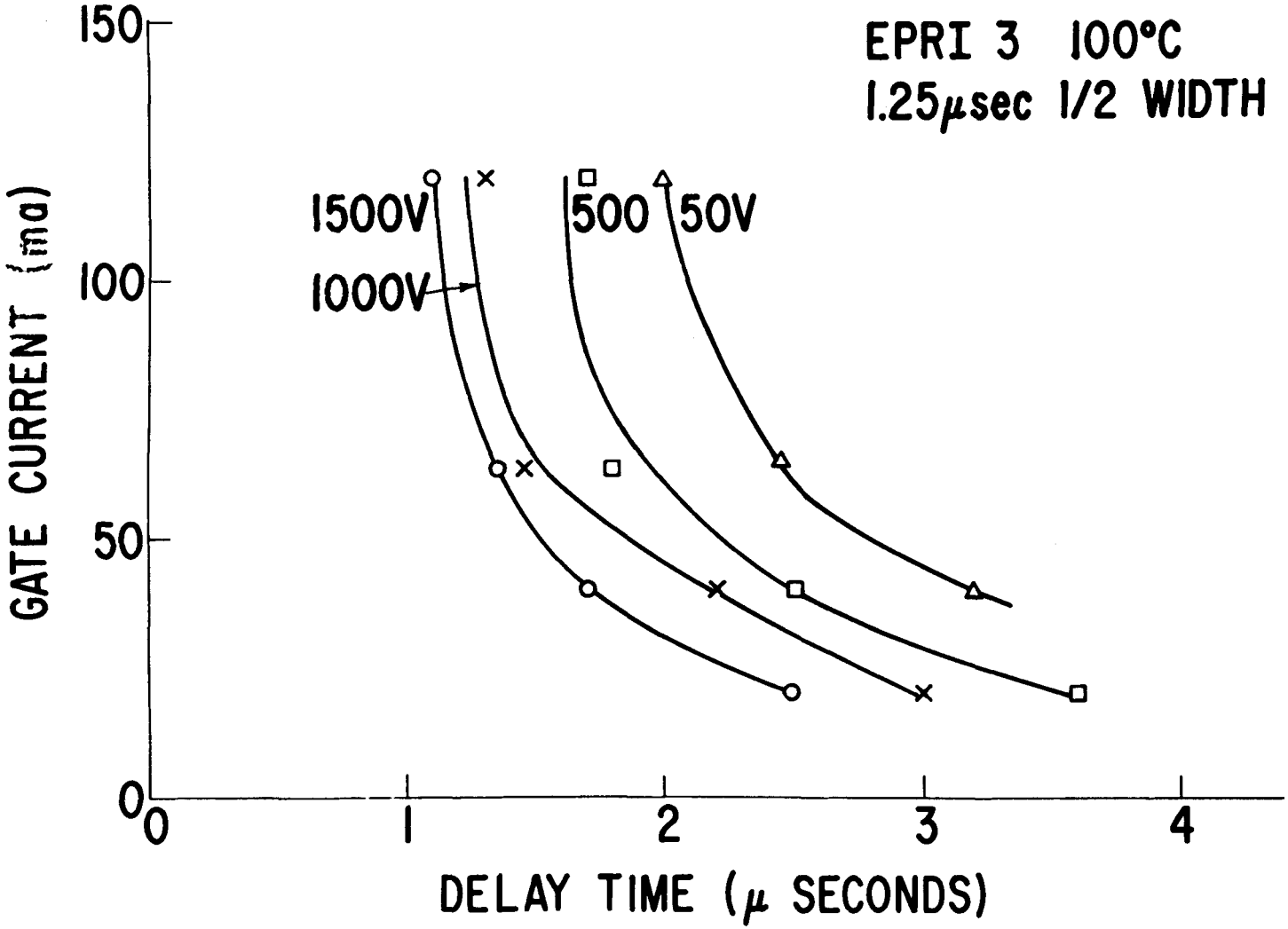


Figure 6-10. Variation of 100°C turn-on delay time vs. gate pulse amplitude for different anode voltages. Gate pulse width = 1.25 μseconds.

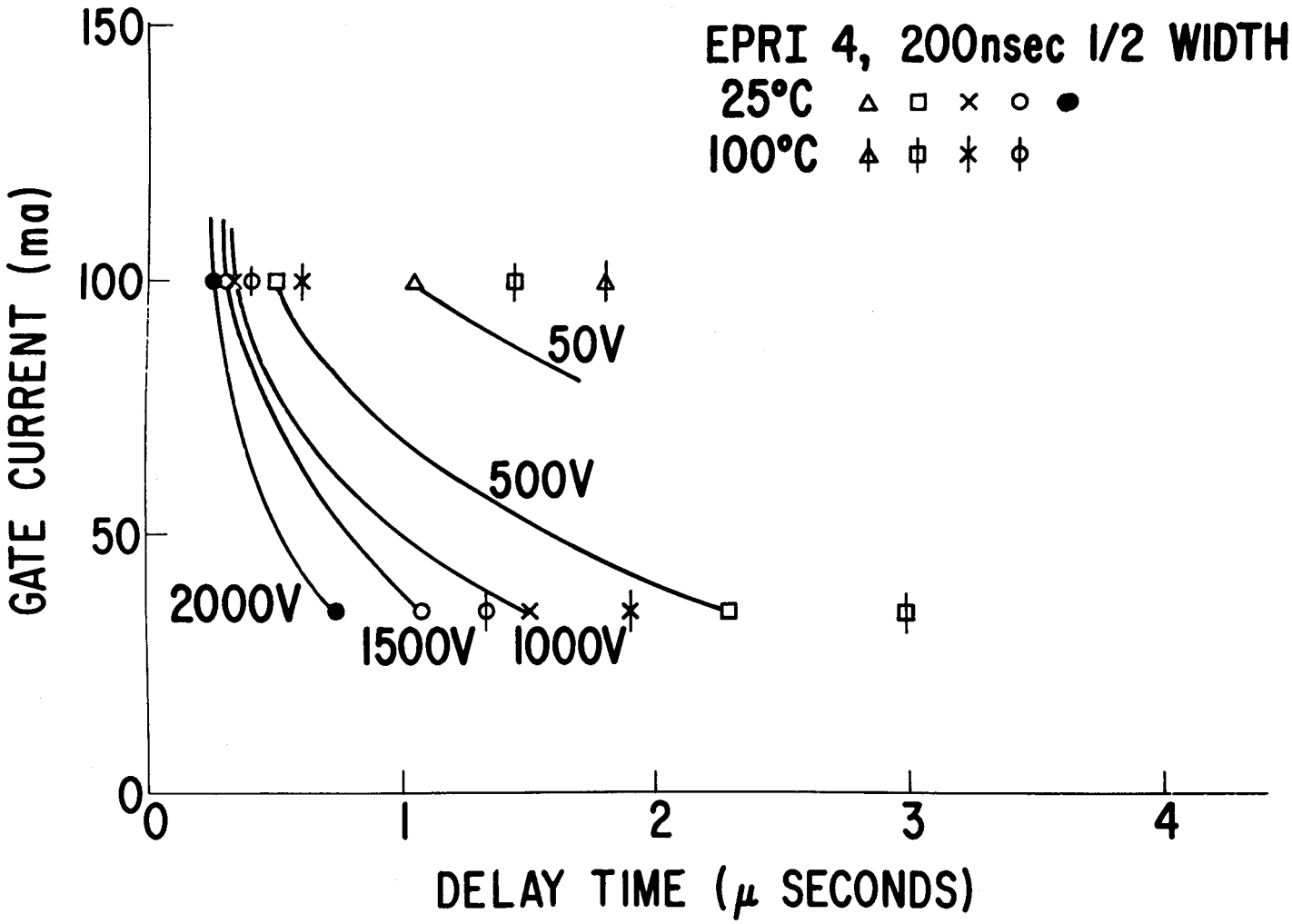


Figure 6-11. Variation of delay time at 25°C and at 100°C vs. gate pulse amplitude for different anode voltages. Gatepulse width = 200n seconds.

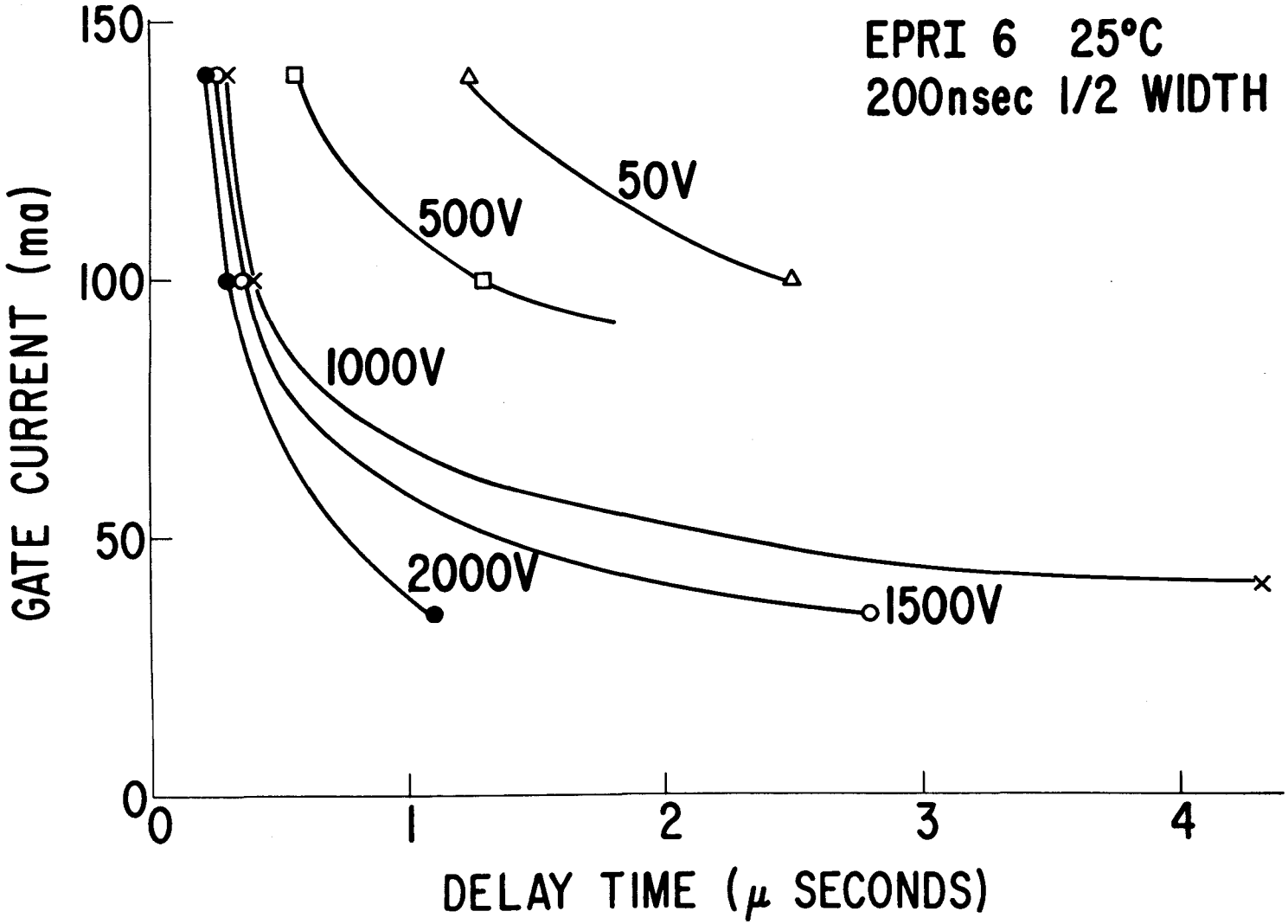


Figure 6-12. Variation of delay time at 25°C vs. gate pulse amplitude for different anode voltages. Gate pulse width = 200n seconds.

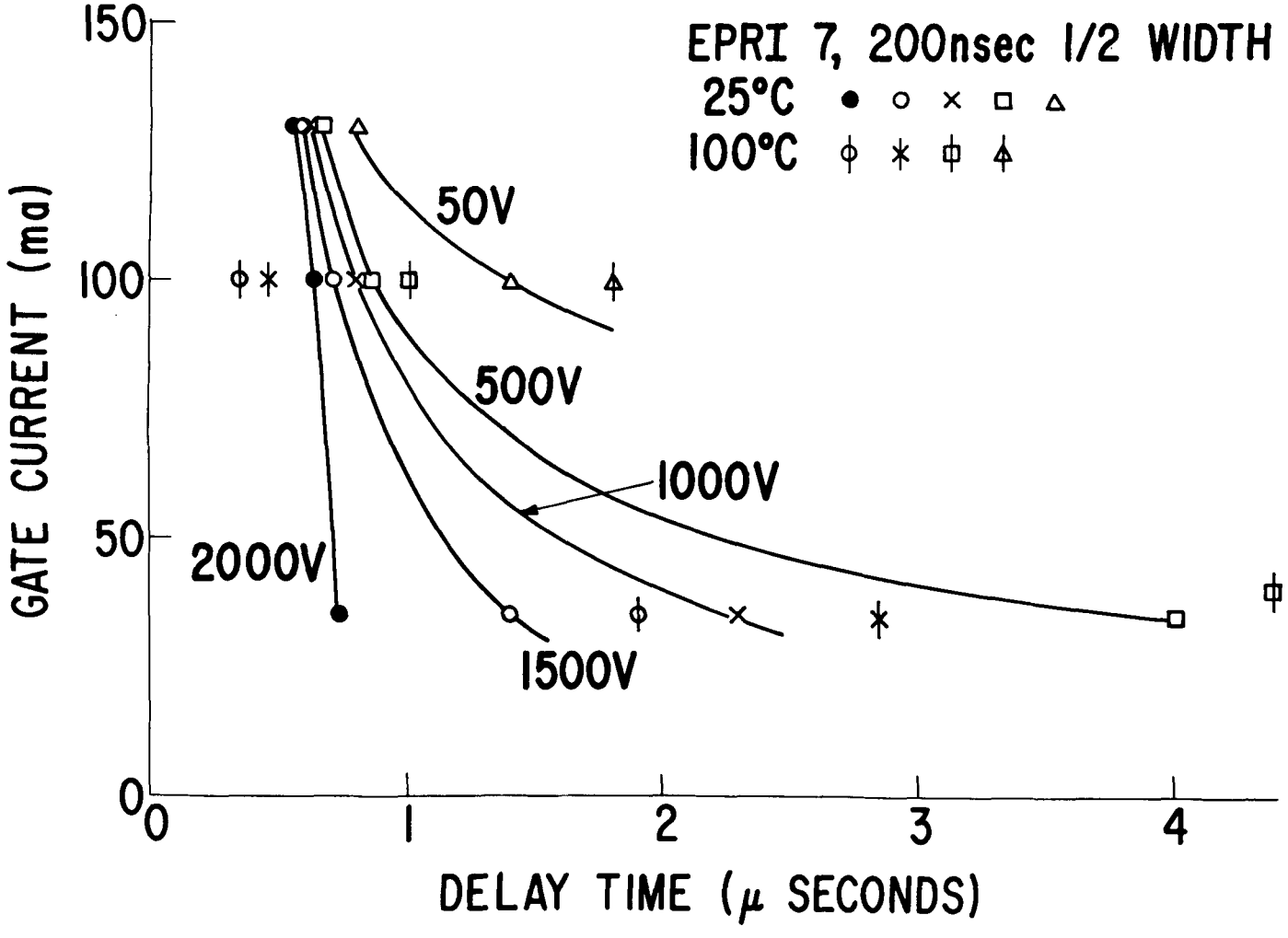


Figure 6-13. Variation of delay time at 25°C and 100°C vs. gate pulse amplitude for different anode voltages. Gate pulse width = 200n seconds.

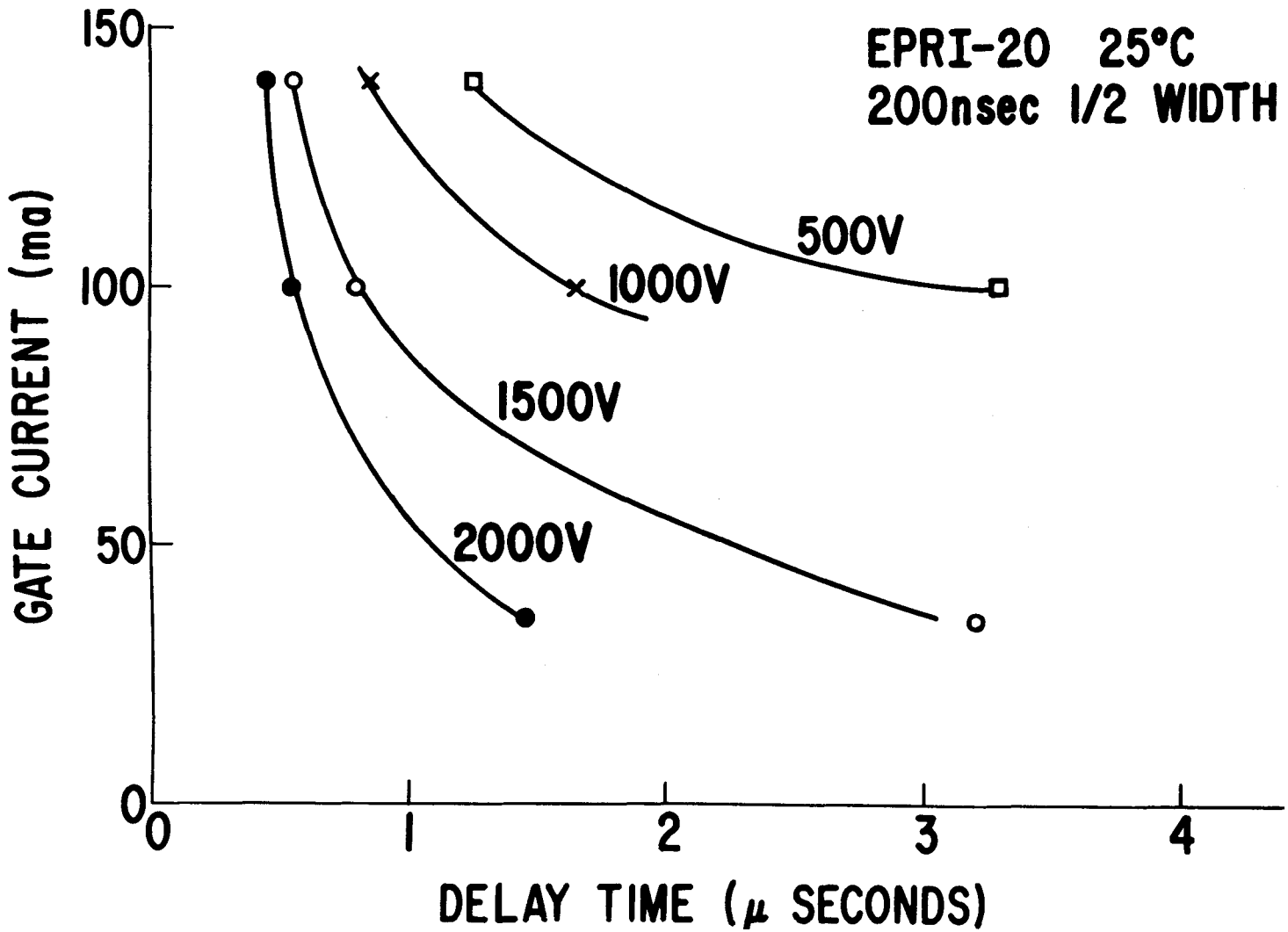


Figure 6-14. Variation of delay time at 15°C vs. gate pulse amplitude for different anode voltates. Gate pulse width = 200n seconds.

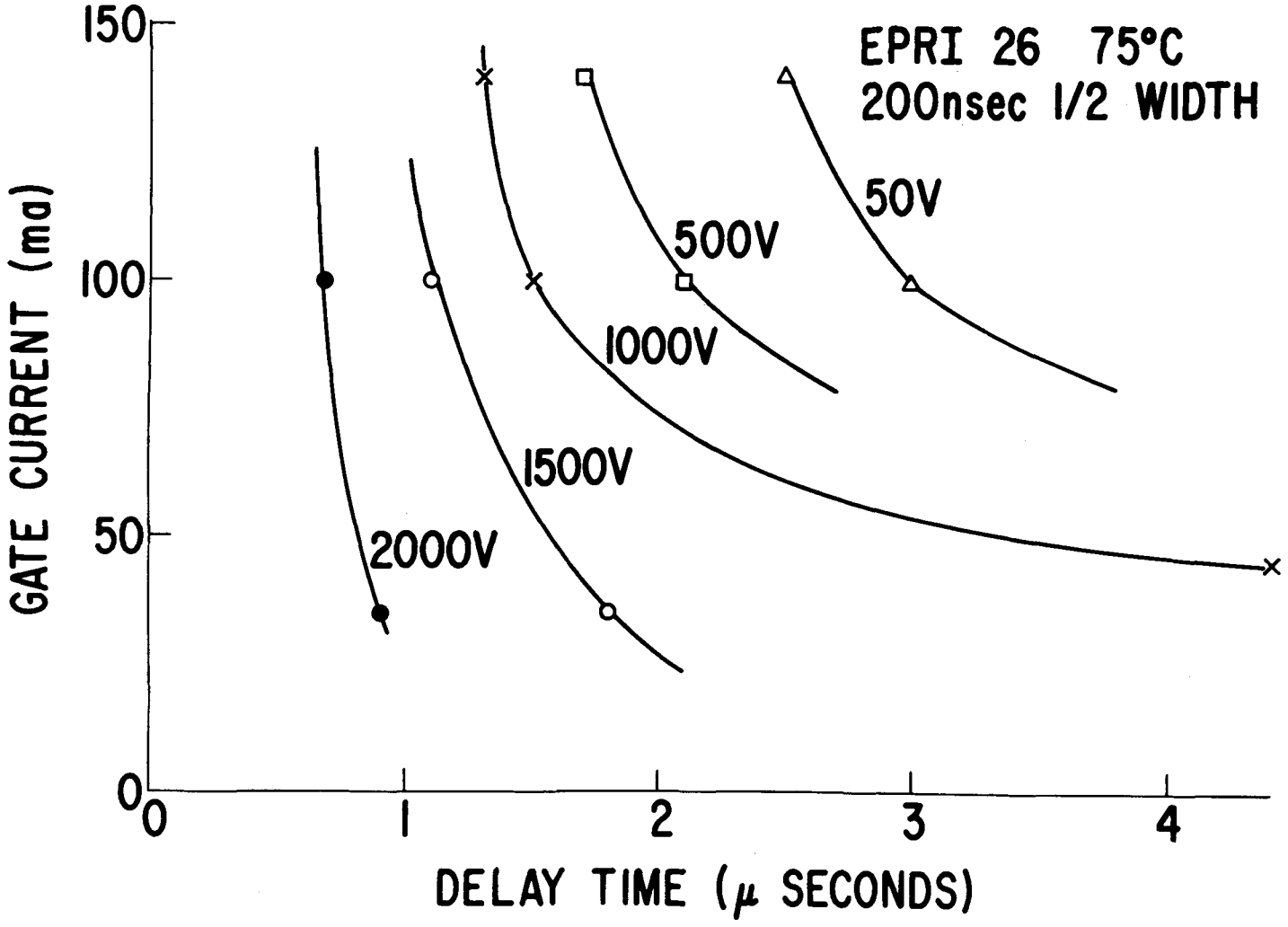


Figure 6-15. Variation in delay time at 75°C vs. gate pulse amplitude for different anode voltages. Gate pulse width - 200n seconds.

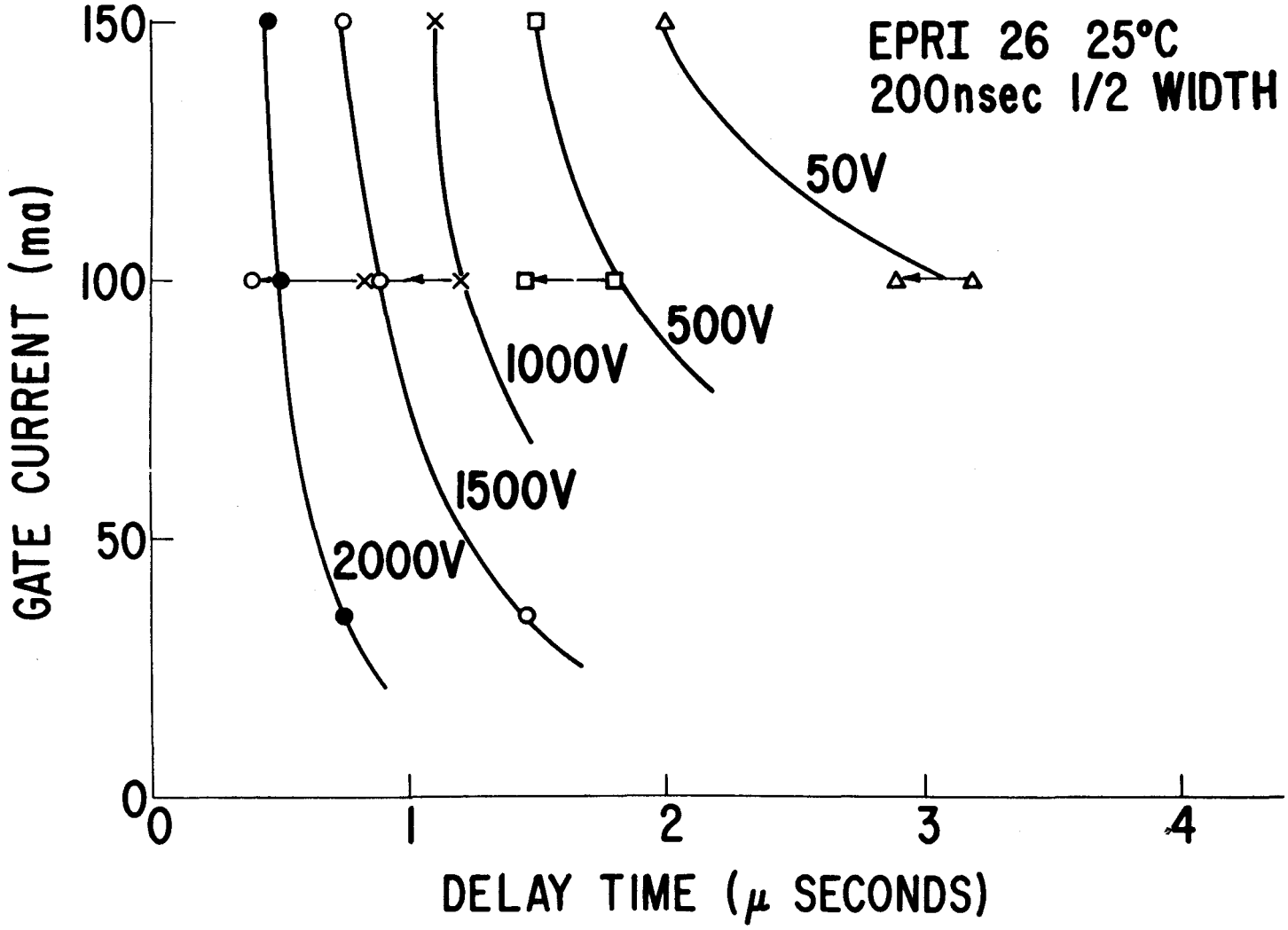


Figure 6-16. Variation in delay time at 25°C vs. gate pulse amplitude for different anode voltages. Gate pulse width = 200n seconds. Arrows indicate 100°C values.

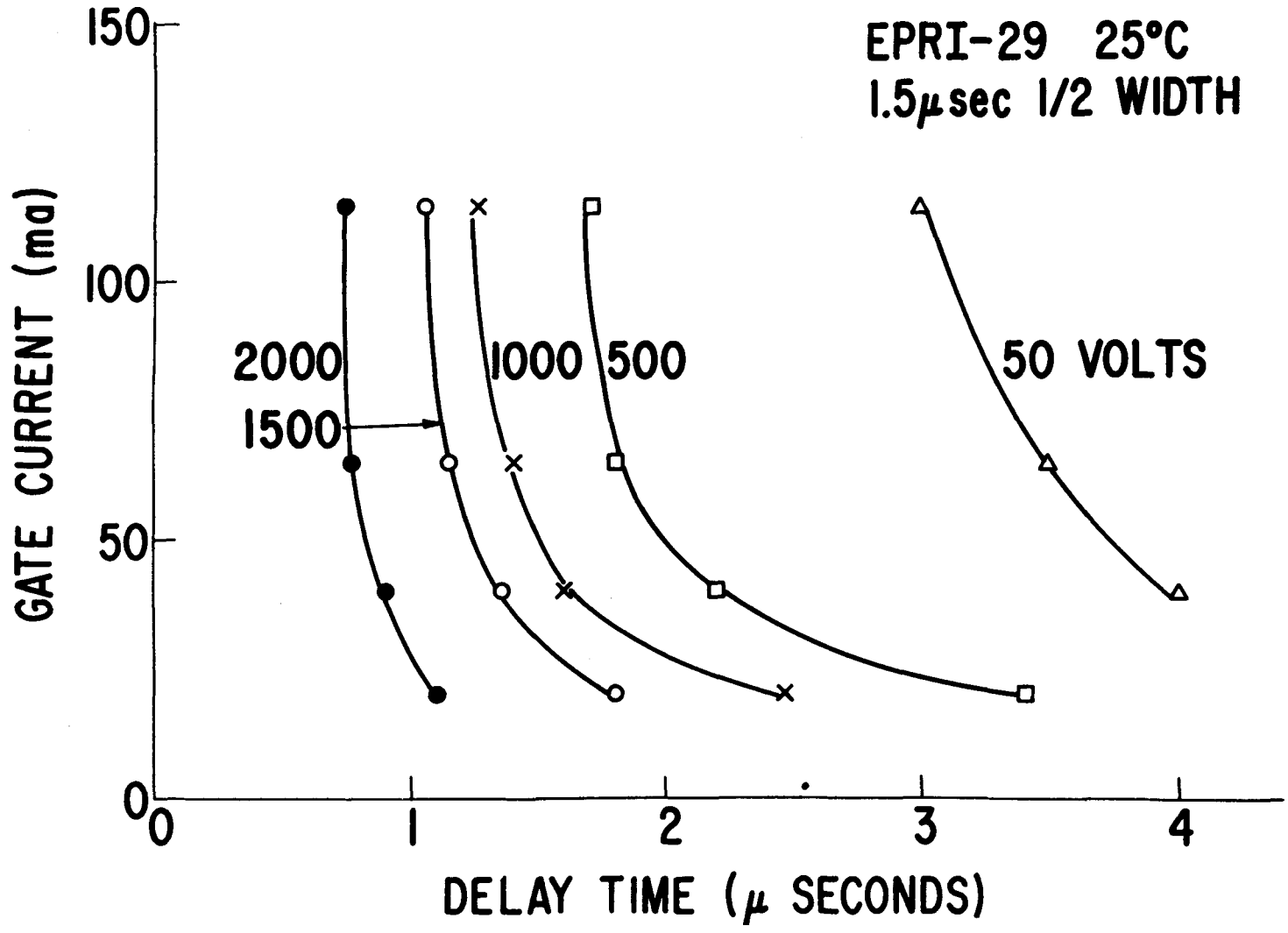


Figure 6-17. Variation in delay time at 25°C vs. gatepulse amplitude for different anode voltages. Gate pulse width = 1.5 μseconds.

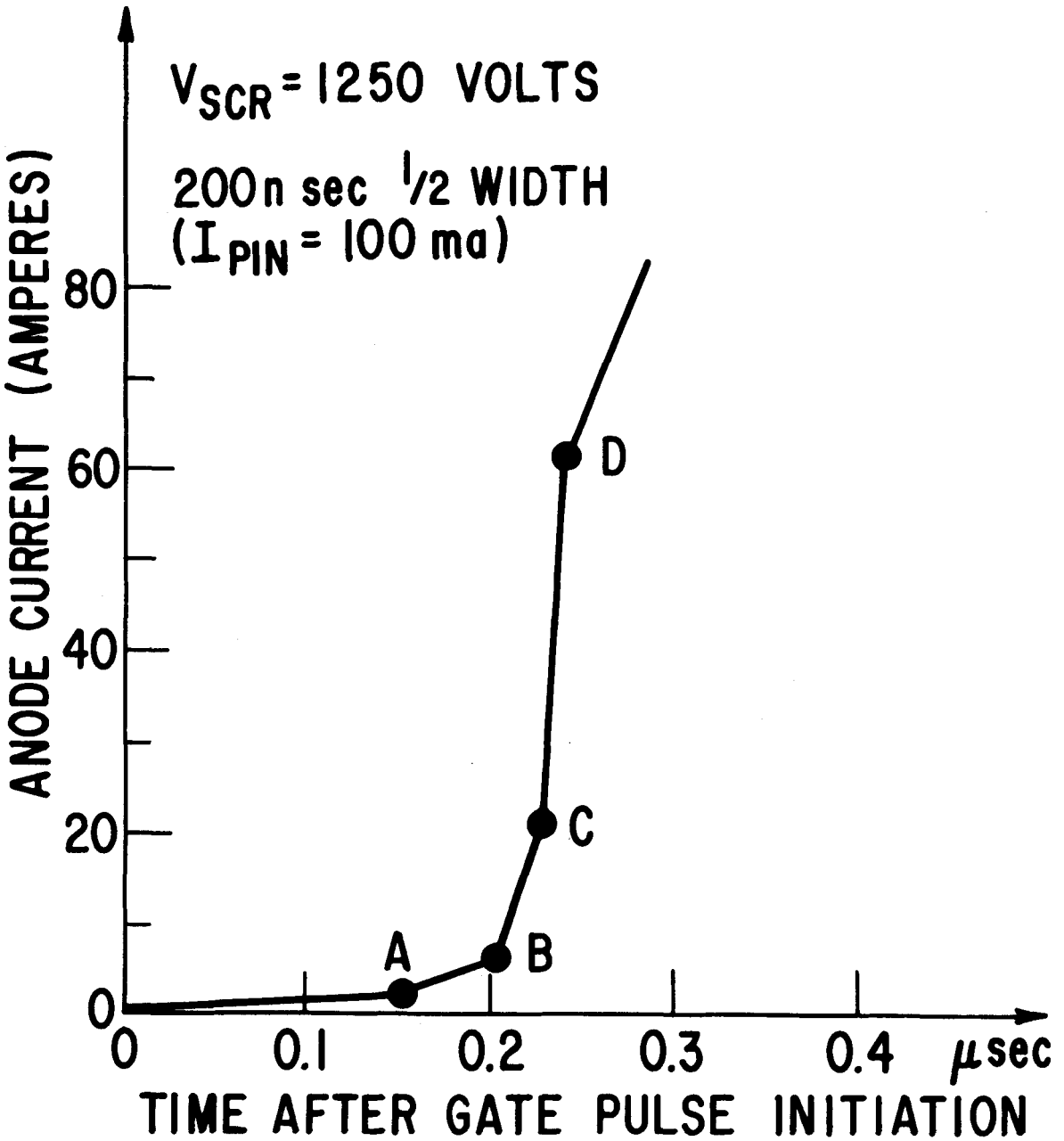


Figure 6-18. Anode current turn-on stages observed in device 7S (photos of Dec. 7, 8, 1976) during turn-on from V_A = 1250 V at room temperature.

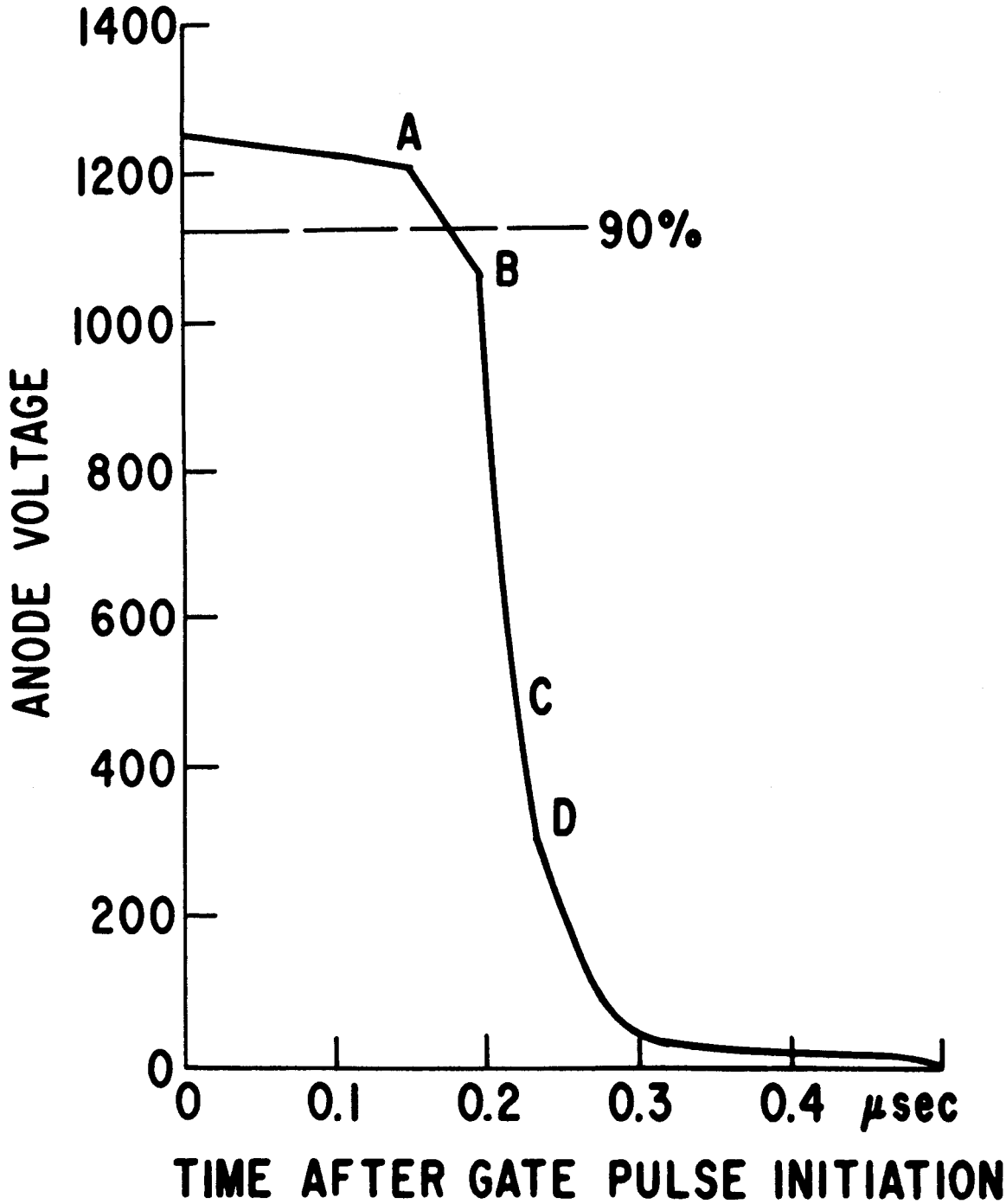


Figure 6-19. Anode voltage turn-on stages corresponding to the schematic current turn-on shown in Figure 6-18.

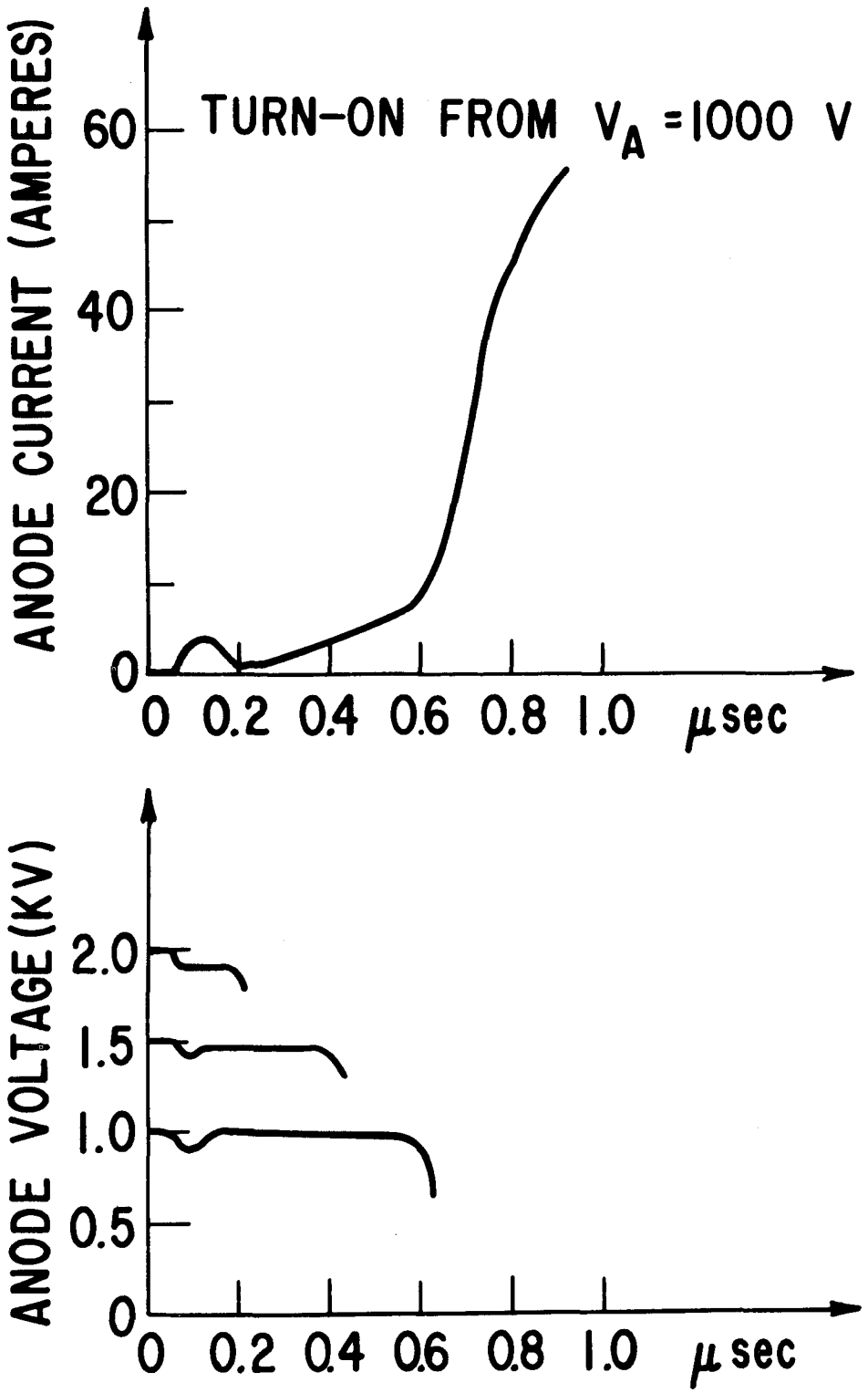


Figure 6-20. Turn-on behavior observed in device 20L in turning on from voltages $\geq$ 1000 volts. (From photos taken Dec. 8, 9, 1976.)

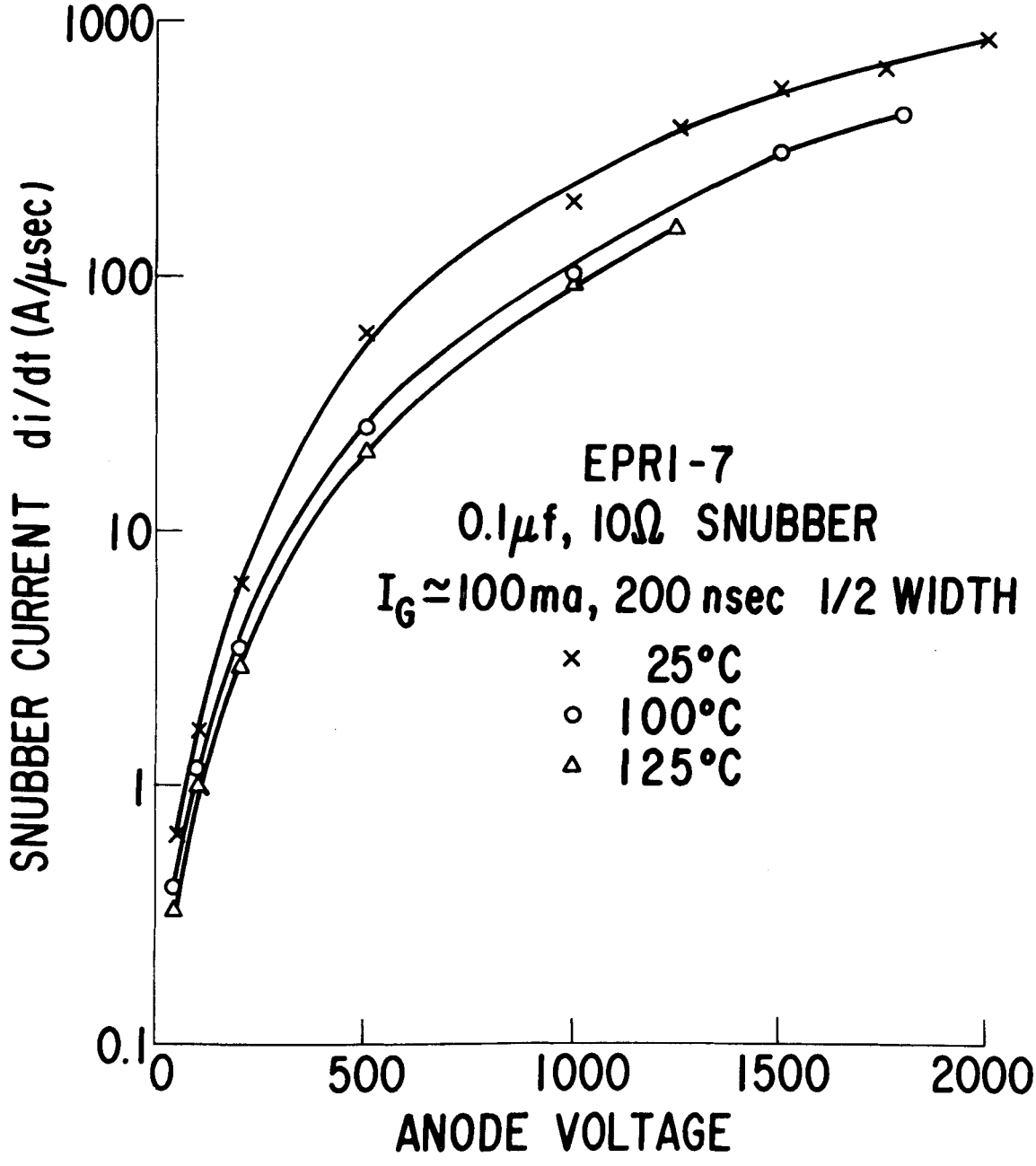


Figure 6-21. Turn-on di/dt vs. anode voltage for different ambient temperatures. Snubber - 0.1 μf, 10Ω. Gate pulse = 200n seconds, 100 ma.

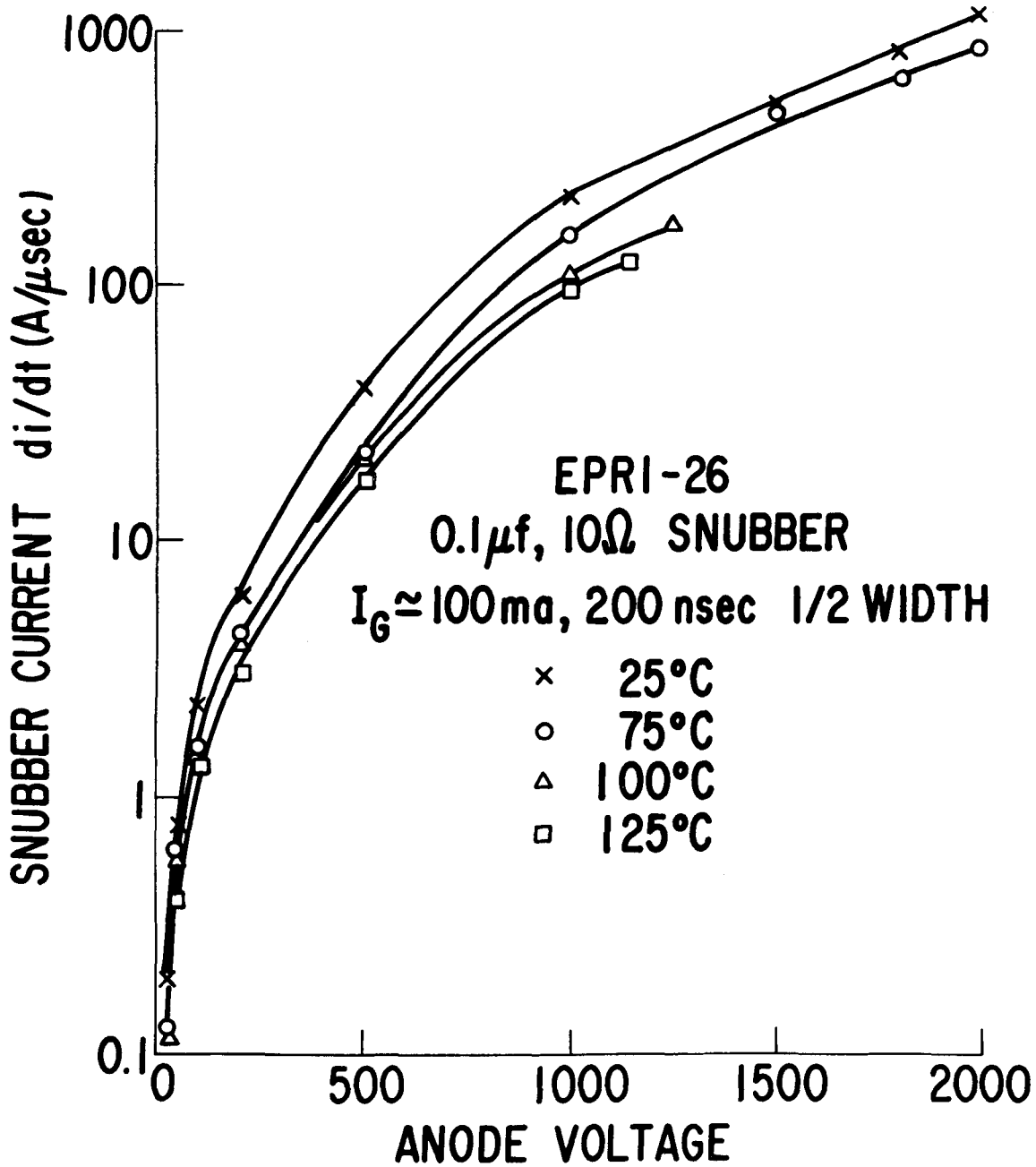


Figure 6-22. Turn-on di/dt vs. anode voltage for different ambient temperatures. Snubber = 0.1 μf, 10Ω. Gate pulse = 200n seconds, 10 ma.

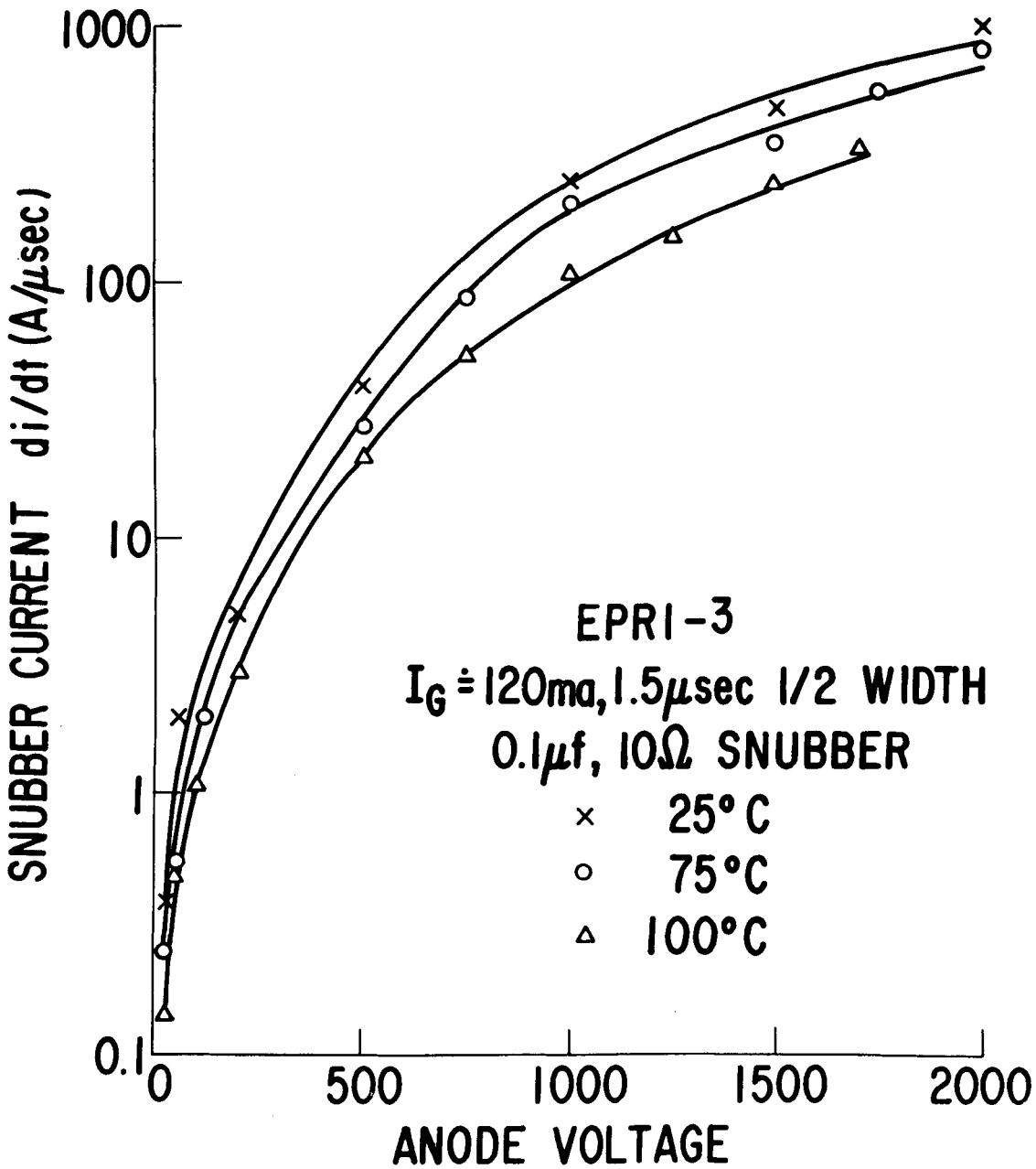


Figure 6-23. Turn-on di/dt vs. anode voltage for different ambient temperatures. Snubber = 0.1 μf, 10Ω. Gate pulse = 1.5 μseconds, 120 ma.

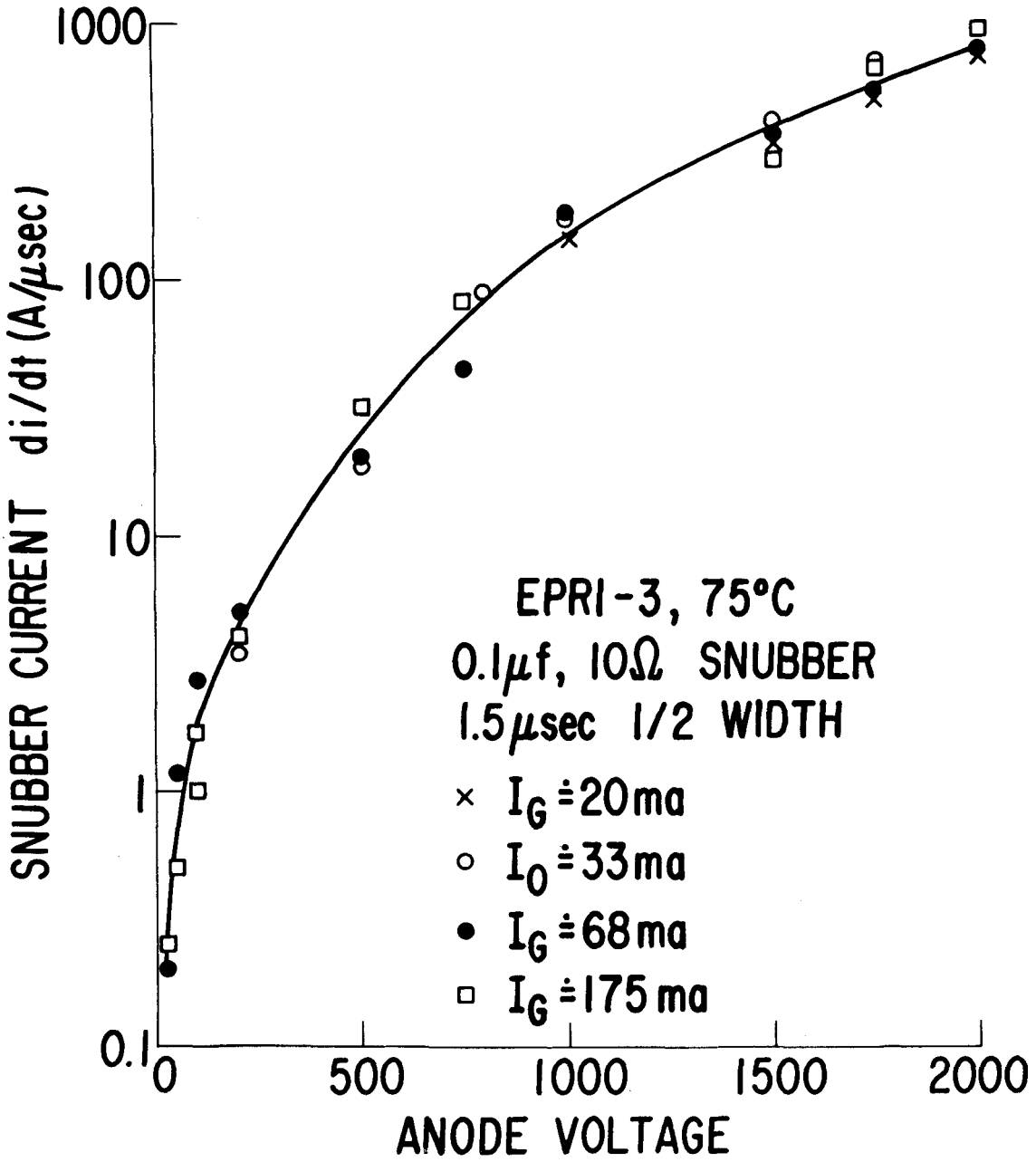


Figure 6-24. Turn-on di/dt at 75°C vs. anode voltage for different gate pulse amplitudes. Snubber = 0.1 μf, 10Ω. Gate pulse width = 1.5 μseconds.

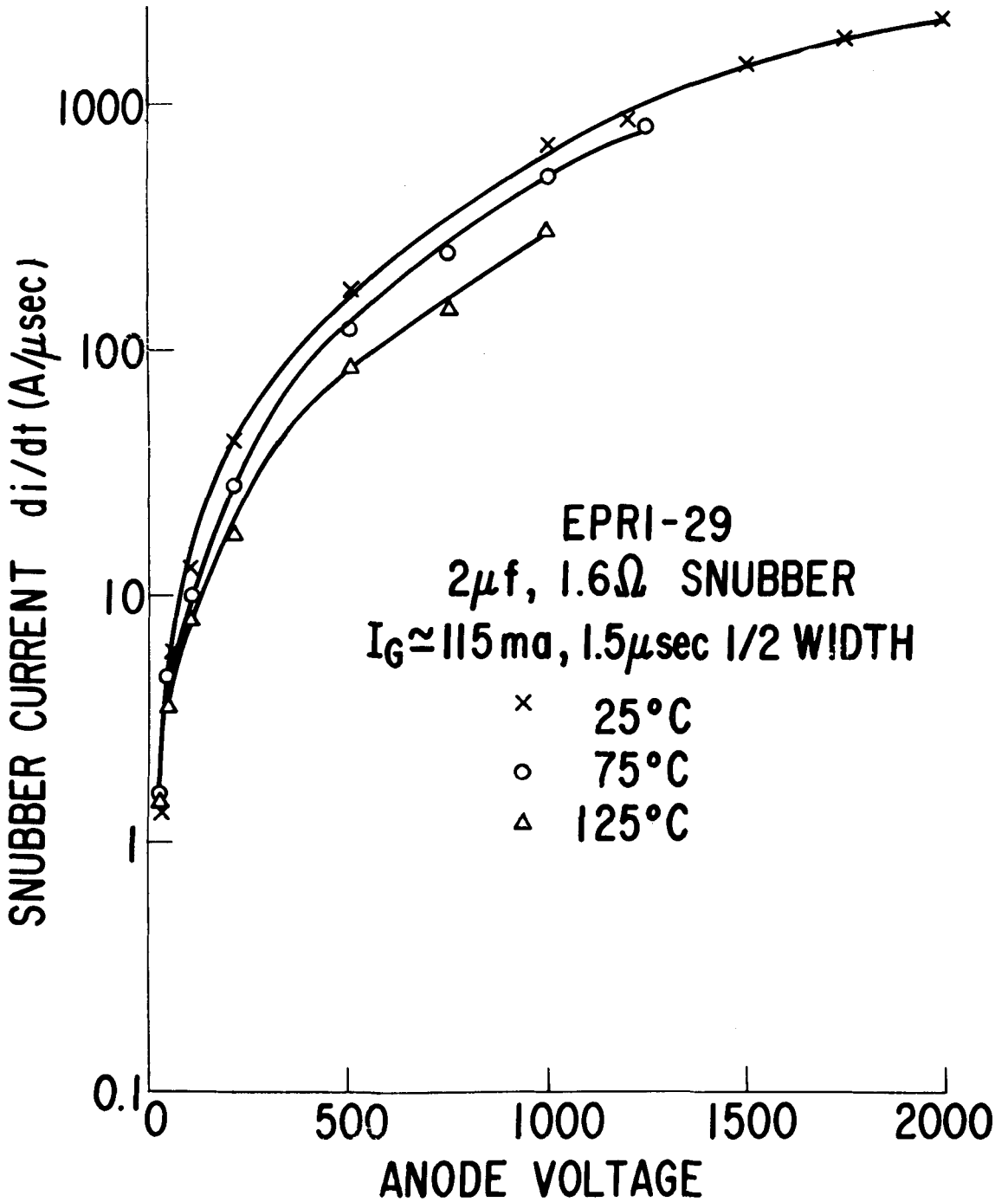


Figure 6-25. Turn-on di/dt vs. anode voltage for different ambient temperatures. Snubber = 2 μf, 1.6Ω. Gate pulse, 1.5 μseconds, 115 ma.

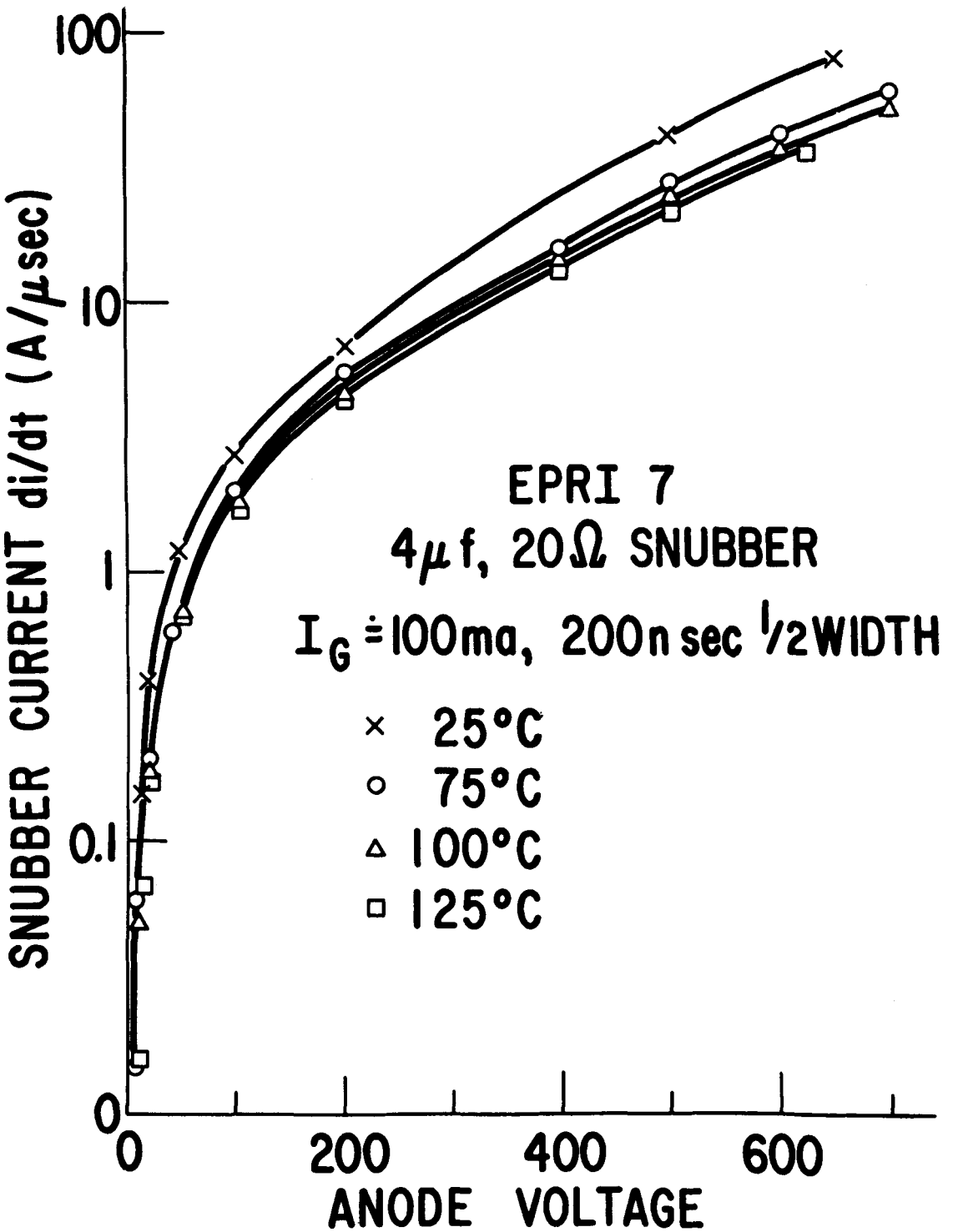


Figure 6-26. Turn-on di/dt vs. anode voltage for different ambient temperatures. Snubber = 4 μf, 20Ω. Gate pulse = 200n seconds, 100 ms.

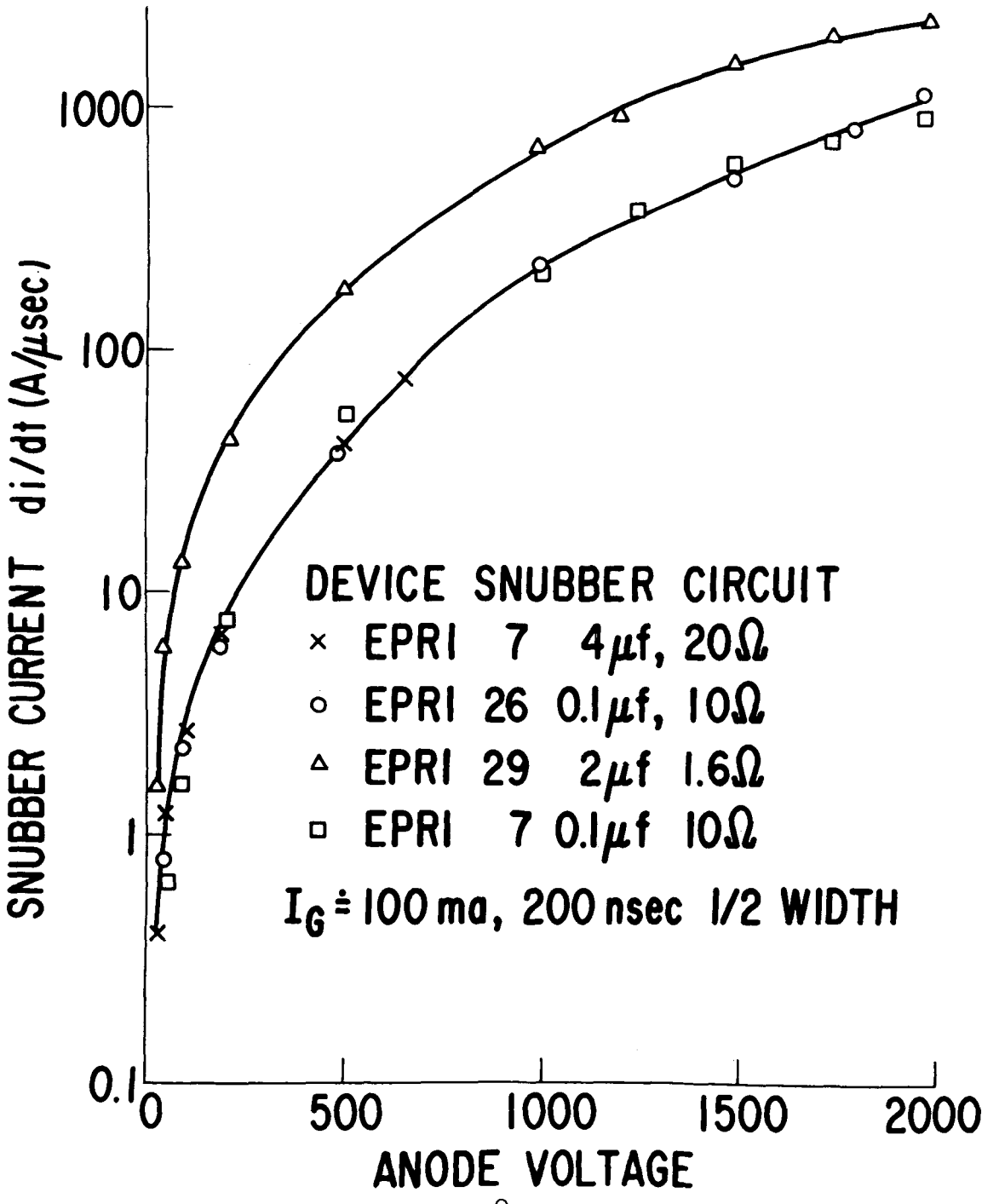


Figure 6-27. Turn-on di/dt at 25°C vs. anode voltage for different snubbers. Gate pulse = 100 ma, 200n seconds.

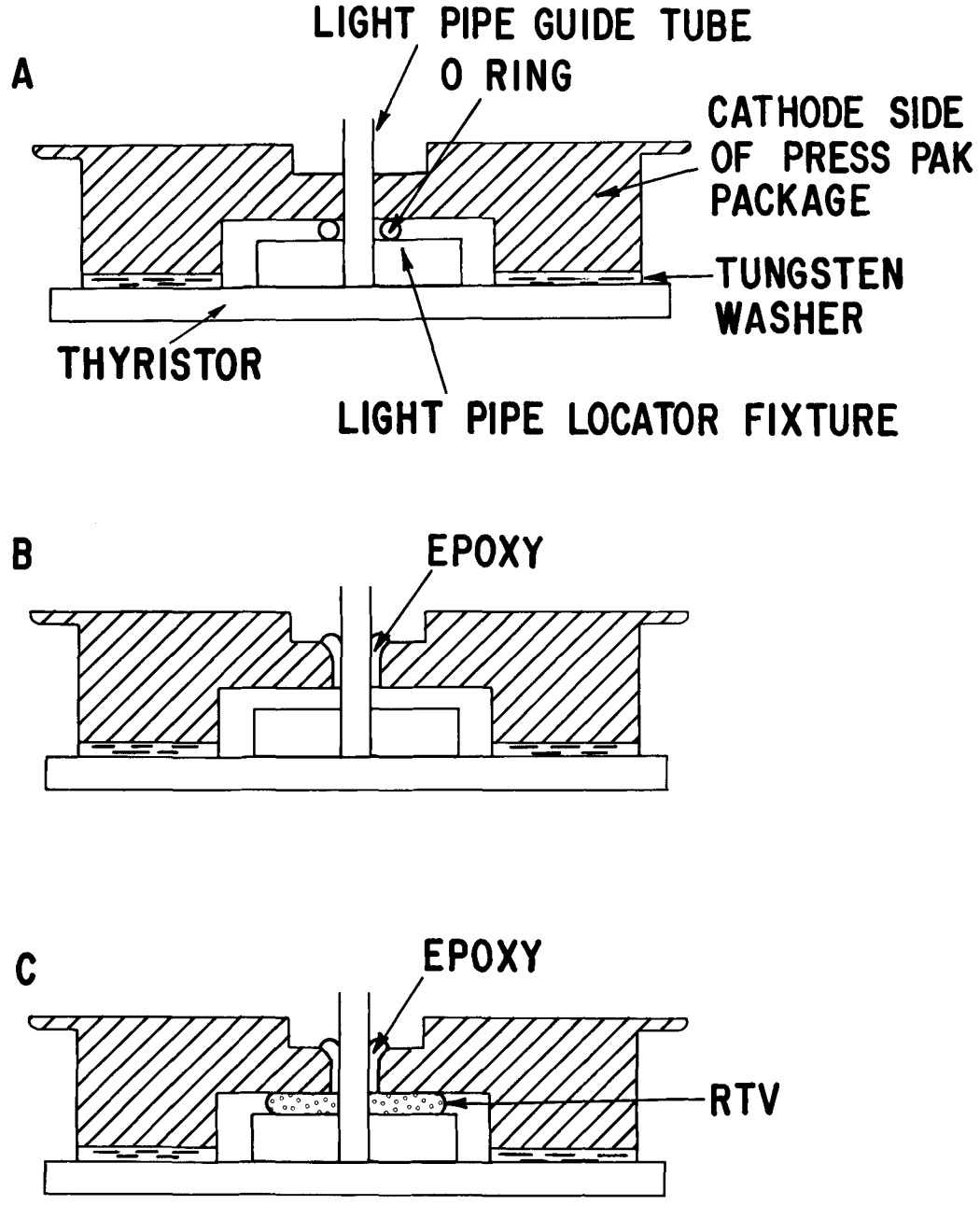


Figure 6-28. The three alternative packages (shown without the anode part of the press-pak package) tested to date.

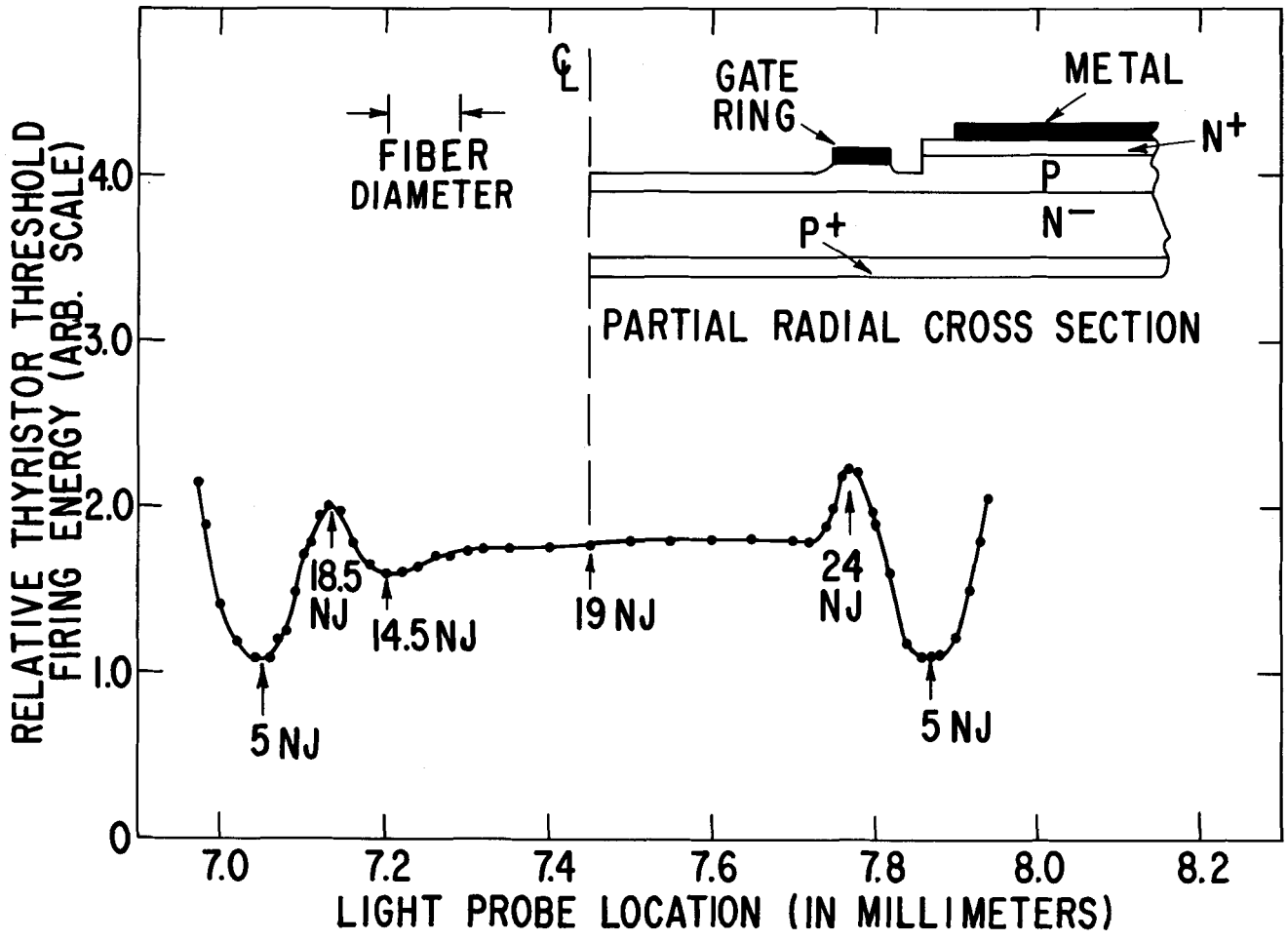


Figure 6-29. Relative triggering sensitivity of an S-type EPRI-GE1 light-triggered thyristor as a function of the location of a single fiber light source. The inset radial cross section is included as a reference. The device tested was device #1. Its actual sensitivity is shown in Figure 6-30.

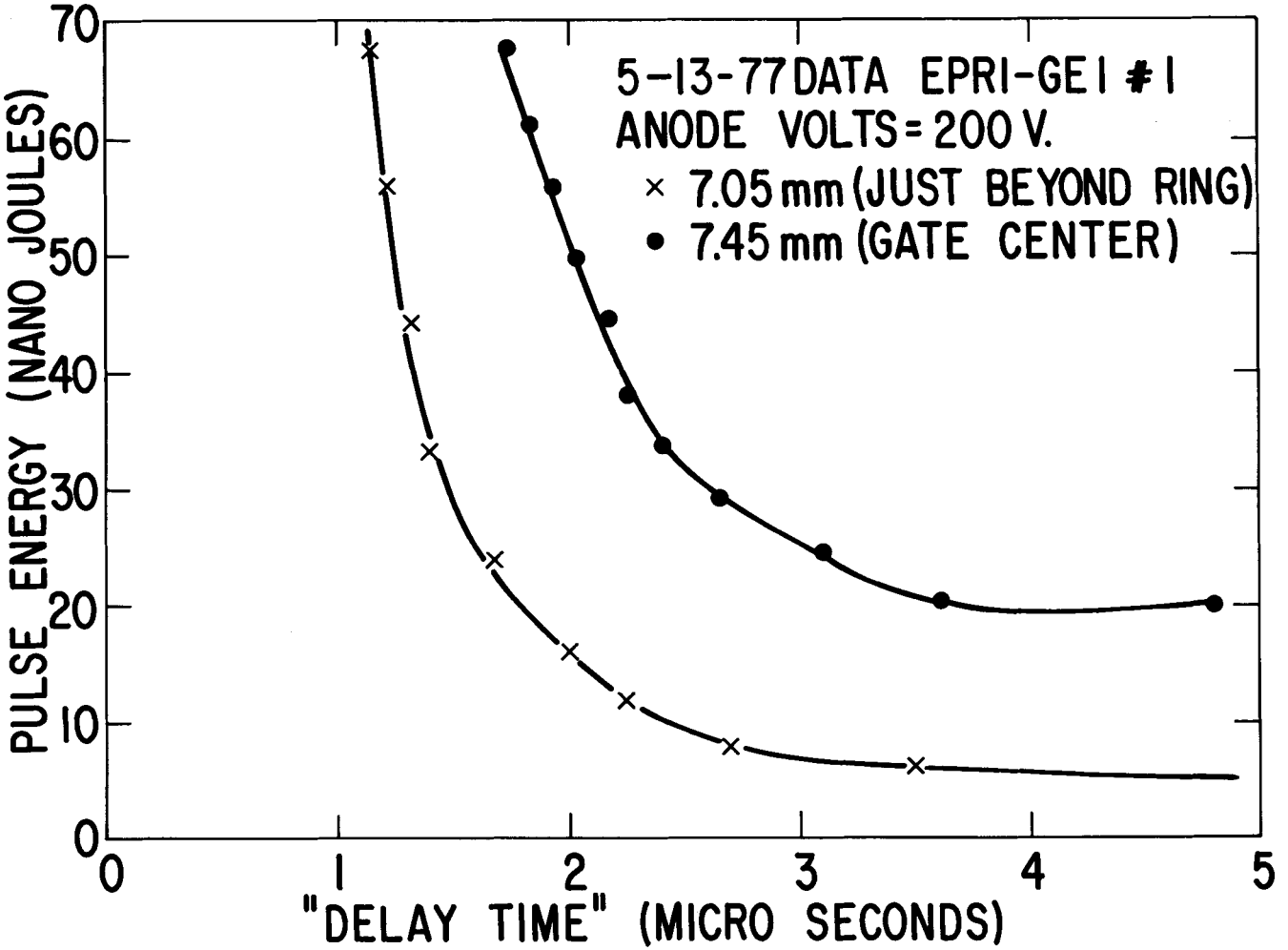


Figure 6-30. Turn-on delay time as a function of incident gate pulse energy for two locations of the light pipe. See Figure 6-29.

Section 7

TESTS FOR DI/DT CAPABILITY

EPRI-GE1 RUN #2 DEVICE TESTING

The work covered in this section of the report deals almost exclusively with device di/dt capability.

Non-Turn-On Test Results

During the last quarter of this contract, a second run of EPRI-GE1 devices was fabricated from slightly lower resistivity material, with a consequently lower breakdown voltage. These devices, like the Run 1 devices, were fabricated in S, L and SE and LE variations. Breakdown voltage, leakage current, dV/dt test results, forward drop and sensitivity are given in Table 7-1.

New di/dt Tests

Because of the short turn-on periphery of the gate amplifying stage, less than a sixth of the turn-on periphery of the amplifying gate stage of the electrically fired device, the initial turn-on area is subjected to very high current densities during turn-on. In the light fired thyristor, this small turn-on line is the price paid for high gate sensitivity. To retain as high a di/dt rating as possible, a double amplifying gate structure was used in which even the intermediate or pilot stage was two to three times more sensitive than the single amplifying stage of the regular electrically fired 6RT101. At room temperatures, di/dt measured during turn-on was higher than in the electrically fired device, and this could rightly be credited to the extra amplifying gate action as described in Section 6 of this report. At high temperatures the device would measurably degrade in blocking capability over a period of time depending on the oven temperature, the di/dt and the snubber design. The failures, often just a temporary device degradation, pointed to an excessive local temperature rise under the gate thyristor emitter or under the pilot thyristor emitter. This was supported by the accompanying increase in leakage current. In the test circuit, a series resistance

prevents device destruction from occurring by ultimately limiting the current through the device after the snubber discharge.

The major purpose of the test circuit shown in Fig. 7-1 was to be able to examine di/dt in the gate and pilot amplifying stages with some degree of control over the power dissipated in the light fired thyristor under test. This thyristor was connected at K1 and A1 with the main thyristor region bypassed as shown in Fig. 7-2/ Instead, the main thyristor stage was replaced by the regular electrically fired 6RT101, properly packaged and mounted. All of the elements except R1 and the power supply were put inside an oven whose temperature could be regulated. A series of tests were performed at different anode voltages, different oven temperatures and with different snubber resistances and different combinations of R and L. Table 7-2 lists the results of a series of tests carried out on two devices which were found to be typical of the entire group tested in this fashion. As one would expect, the larger the L value, the smaller the initial di/dt seen by the snubber. However, the larger the L value, the longer the current flow persisted. The effect of R was to limit the size of the current flowing through the thyristor under test. Thus, the net effect of the R-L series network was to limit di/dt through the gate stage as well as the peak current. This is generally advantageous but there are two drawbacks which call for careful tradeoffs. One is a reduced gating signal for the next stage which increases delay time and minimum firing voltage.* The second drawback is related to the slower turn-off of the gate stage after turn-on of the main stage due to the finite R-L time constant. Looking at the results in Table 7-2, it is apparent that at 1800 volts the turn-on di/dt of the main thyristor stage is not affected to any great extent by our choice of R and/or L.

In the so-called hybrid firing scheme, which the test configuration in Fig. 7-1 effectively is, more complex circuit elements could be included between K1 and G2 and between K1 and K2 to tailor both the current-voltage seen by the light fired gate device and the current-voltage applied to the gate of the electrically fired device.

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* The combination of thyristor 1 and thyristor 2 is considered "off" until both are on.

After consideration of the above experiments a new set of experiments were undertaken using the test set-up of Fig. 7-1, but the L = 0 and R having such values as could be included into an integrated light fired thyristor device. In this set of experiments, a thermocouple was attached to the thyristor approximately in the center of the pilot thyristor emitter. Turn-on tests were performed from 1200 and 1800 volts at 25, 50 and 70°C oven temperatures with R = 0, 10 or 100Ω. The tests were continued until the thermocouple temperature reading stabilized. A similar experiment will be performed with the thermocouple on the gate thyristor stage as soon as special new fixtures are fabricated.

The results of these experiments are shown in Figs. 7-3 to 7-11. Each figure shows the temperature rising above the oven temperature as a function of time, first firing at 1200 volts and then firing at 1800 volts. The photographs included in each figure show the currents, I_1 and I_2, and the voltage, V_{K1-A1} and V_{K2-A2}, across the two thyristors. In all cases, the top trace is the current I_1 (positive downward) and the bottom trace, I_2 (positive upward). V_{K1-A1} can be distinguished from V_{K2-A2} as it is slightly displaced vertically and falls off in voltage first.

There are a number of useful observations which can be made based on Figs 7-3 to 7-11 and Table 7-3. Typically the results can be compared at low and high temperature and at low and high R value. For example, at 25°C oven temperature, the R = 11 case (Fig. 7-3) shows I_1 limited to 10 Amperes while the R = 0 case (Fig. 7-5) shows, I_1 rising to 170 Amperes. Naturally the temperature rise for the R = 0 case is much higher, almost three times larger. At 50°C oven temperature, the R = 0 temperature rise is closer to 5 times greater than that of the R = 100 case and about twice that of the R = 10 case. In all cases, the 1800 volt turn-on produced higher temperature rises as measured over the pilot stage emitter by the thermocouple. However, as one would expect, the main device turns on more rapidly after the gating device which, to some extent, reduces the thermal stress on thyristor 1. This can be seen most clearly in Fig. 7-3 by comparing I_1 in the inset photographs, P1 (1200 volts) and P2 (1800 volts).

The higher temperature results show that the best performance in terms of highest stabilized average device temperature was the 100Ω case shown in Fig. 7-9 in which the 1800 volt turn-on test stabilized at approximately 85°C. Changing the temperature, besides lowering the main device di/dt also affected the delay time in the turn-on of the main device. Looking at the inset photographs in Figs. 7-6 and 7-9, shows an increase in delay time of 0.3μseconds at 50°C and 0.5μseconds at 70°C for turn-on from 1800 volts. Note also that with increasing R and increasing temperature, the time between the turn-on of the gating thyristor and the main thyristor also increases wihile the di/dt of the turn-on decreases. For R = 0 and R = 10Ω, no temperature stabilization was obtained at the 70°C oven temperature although the devices operatued successfully for several minutes.*

What was usually observed at that point would be an increase in leakage current and a drop off in anode firing voltage as marked along the curve in Fig. 7-10. There, each 100 volt drop marks an increase in leakage current of about 2.5ma. If the process had not gone too far, the device would recover on removal of the photo-gate pulse and the temperature would fall due to the removal of the turn-on energy dissipation stress. If the process had gone further, it would require a reduction in voltage for the thyristor to recover. It is very possible that the observed behavior was caused by the following sequence of events. First, there is a rise in average temperature in the device caused by turn-on power dissipation. Second, during each cycle the initial turn-on lines of the gate and pilot stages undergo a junction temperature excursion.(9,10,11) Evidently large R values and fast turn-on of the next stage should both act to reduce the thermal dissipation contributing to the peak junction temperature. Finally, because turn-on losses go up with average temperatures there is a possibility of thermal runaway in the vicinity of the turn-on line. Note in Fig. 7-10, a case of thermal runaway at 1800 volts, that there is an inflection point at T ≃ 85°C, perhaps indicating that the junction excursions were reaching 125°C at that point.

* The standard di/dt test is of one minute duration.

The answer to the problem is to limit both junction excursions and average temperature increases. This could be done in part by a larger snubber resistance and smaller snubber capacitance and reduced follow-on di/dt. However such accomodations may not be possible since snubber design is largely fixed by commutation transient control requirements.

SUMMARY

Turn-on experiments confirm that excessive energy is being dissipated in the gate and pilot thyristor stages. The nature of the turn-on transients point to this excessive energy as being dissipated in the first few microseconds of turn-on. Increased series impedance between the gate and pilot stages or between the pilot and main stages, if judiciously selected, should reduce this dissipation without noticeably degrading other performance characteristics. This approach will be investigated in follow-on work.

Table 7-1

EPRI-GE1 THYRISTOR PROPERTIES

Device #	Etch Depth (μ)	Threshold Turn-on (1) Gate (ma)	Pilot (ma)	Main (ma)	Room Temp. Blocking Voltage (2) Forward (Volts)	Reverse (Volts)	125°C 2600 Volt Leakage (3) Forward (ma)	Rev. (ma)	2000V μsec 105°C dv/dt test (4) (Volts)	R_1T_1 Forward Drop at 1000A (Volts)
41L	10	4	32	180	2880	1740	50	600V	1800	1.19
42S	11	4	27	250	2550	2650	50	12	2000	1.20
43S	16	3	25	230	2800	2440	35	8	2100	1.22
44S	10	4	25	250	2470	2440	50	15	1900	1.25
45S	15	2.5	28	280	2640	2830	50	1200V	1750	1.28
46S	10	4.5	30	260	2470	2640	35	20	> 2200	1.28
47LE	9	6	30	300	2480	2700	50	15	2100	1.27
48S	14	5	28	250	2560	2720	30	10	1900	1.21
49L	20	2.4	22	200	2600	2620	700V	short	1700	1.22
50L	10	7	25	215	2600	2630	35	7	1700	1.21
51LE	29	3	29	250	2340	2200	900V	2400V	500	1.21
52S	19	2.5	20	200	2600	2600	30	16	1500	1.21
53L	27	3	28	250	2580	2800	2400V	20	1500	1.19
54L	10	6	25	230	2560	2600	50	15	1850	1.21
55S	25	2.4	31	270	2520	2630	60	1900V	——	——
56SE	29	2	24	205	2380	2600	2500V	20	——	——
57S	29	1.8	26	250	2650	2600	2000V	15	——	not ——
58L	11	5.5	25	220	2540	2640	30	10	——	measured ——
59L	20	3.5	28	240	2550	2720	30	15	——	——
60L	20	2.6	30	250	2620	2540	25	20	——	——
61S	10	4	26	230	2750	1600	25	1750V	——	——
62L	26	2.5	24	200	2750	2740	30	10	——	——
63S	28	1.5	25	210	2740	2780	35	25	——	——
64L	10	5	27	260	2650	2770	35	10	——	——
65SE	26	2.7	26	240	2600	2650	30	15	——	——
66S	26	2.1	27	240	2680	1500	35	1600V	——	——
67SE	29	1.6	25	220	2470	2620	25	15	——	——
68LE	23	3.6	28	250	2550	2800	35	10	2100	1.19

NOTES: 1) Breakpoints of gate-cathode I-V (anode open) to an accuracy of 1, 5, 25ma respectively.
2) Measured with a 60Hz sinusoidal waveform to a 10ma leakage current.
3) Measured with a 60Hz 20μsecond wide pulse to 2600 Volts.
4) Measured with a 2000V/μsecond signal to the voltage shown.

Table 7-2

HYBRID FIRING TEST RESULTS FROM 1800 VOLTS

DEVICE #	Oven Temp. (°C)	R/L (Ω/μh)	di/dt*(I_1,I_2) (A/μsec)	COMMENTS
29L	25	100/10	64, 2000	t_d = .59μsec
		100/100	12, 1500	t_d = .61μsec
	100	100/10	44, 1200	
		100/100	7, 1000	
	25	0/10	110, 2000	
		0/100	15, 1500	
	100	0/10	78, 1200	
		0/100	24, 900	
		0/0	320, 1200	degraded after 12 hours.
44S	25	10/10	150, 2000	
		100/10	75, 2000	
		100/100	100, 2000	
		10/100	300, 1800	
		0/100	400, 2000	
		0/100	175, 1800	
		100/0	300, 2000	
	100	10/10	120, 1400	
		100/10	105, 1200	
		100/100	56, 1200	
		10/100	70, 1000	temp. degraded** on overnight test
		0/100	100, 900	degraded in several minutes.
		0/10	60, 1000	degraded in several minutes.
		100/0	52, 1200	degraded in ∿ 20 minutes.
		10/0	240, 1000	degraded in ∿ 10 minutes.

* Because of the time scale on the photos (See Figures 7-3 to 7-11, for example) it was difficult to determine di/dt values greater than 200A/μsec to better than 20% accuracy.

** Temporary loss of full blocking voltage capability.

Table 7-3

TEMPERATURE RISE DURING PROLONGED TURN-ON TESTING FOR DIFFERENT VALUES OF R FOR V_A = 1200 VOLTS AND V_A = 1800 VOLTS. (see figures 7-8 to 7-11)

OVEN TEMP. SETTING	ΔT(R=0) 1200V, 1800V	ΔT(R=1Ω) 1200V, 1800V	ΔT(R=100Ω) 1200V, 1800V
25°C	14°C, 19°C	7.5°C 12.5°C	5°C, 8°C
50°C	12°C 15.5°C	4.5°C 7°C	1.8°C 3.3°C
70°C	9°C, --	9°C --	4°C, 14°C

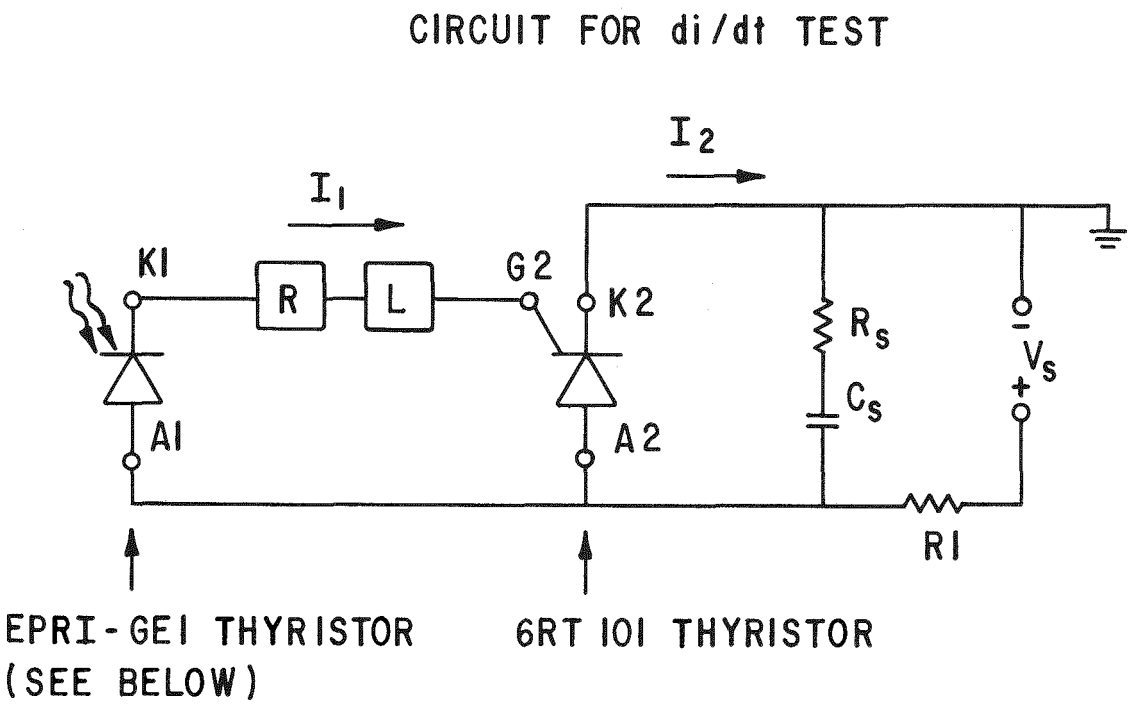

Figure 7-1. The test circuit for the inset photographs in Figures 7-3 to 7-11. Incident photons trigger the light sensitive device at A1-K1. Current I_1 subsequently triggers the main device which was chosen to be the regular 6RT101 electrically-fired thyristor.

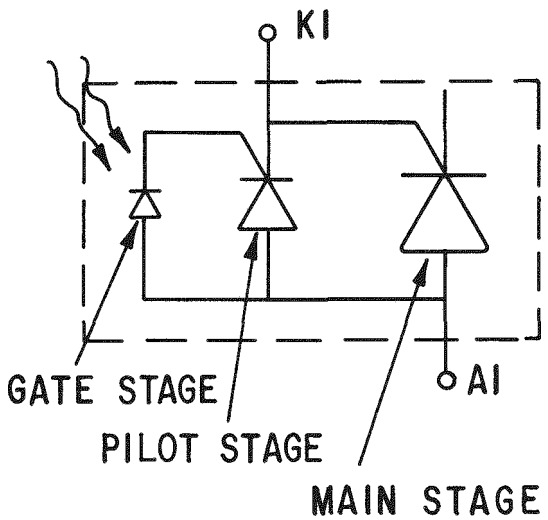

Figure 7-2. Electrical analog of the EPRI-GE1 thyristor showing the pilot stage being used for the cathode.

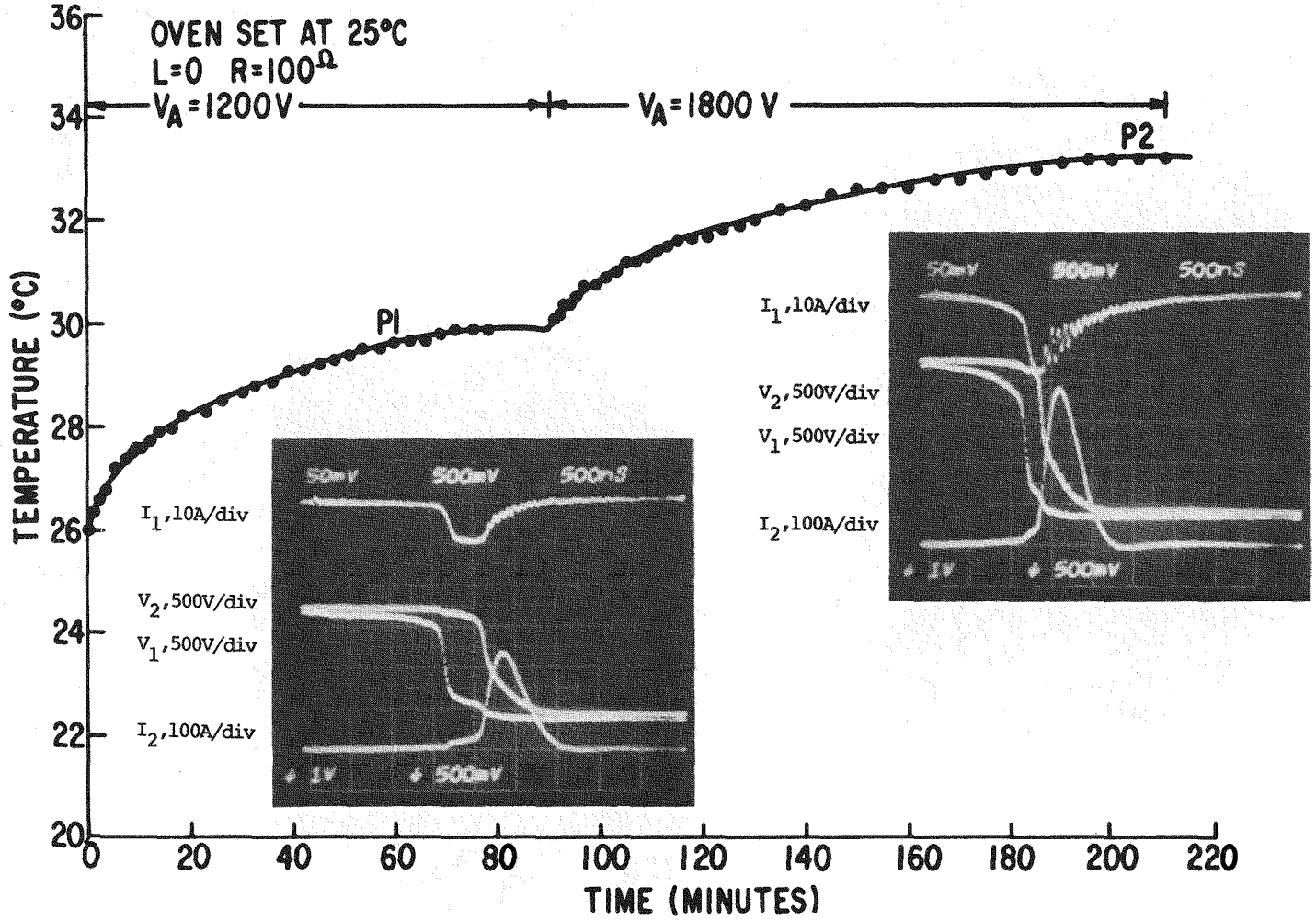

Figure 7-3. Prolonged di/dt test using the test circuit in Figure 7-1. P1 and P2 indicate the points at which the inset photographs were taken. The oven temperature was 25°C. A series resistance of 100Ω was used. The snubber was 0.1 μf, 1.25Ω. The time scale is 0.5 μsec/div.

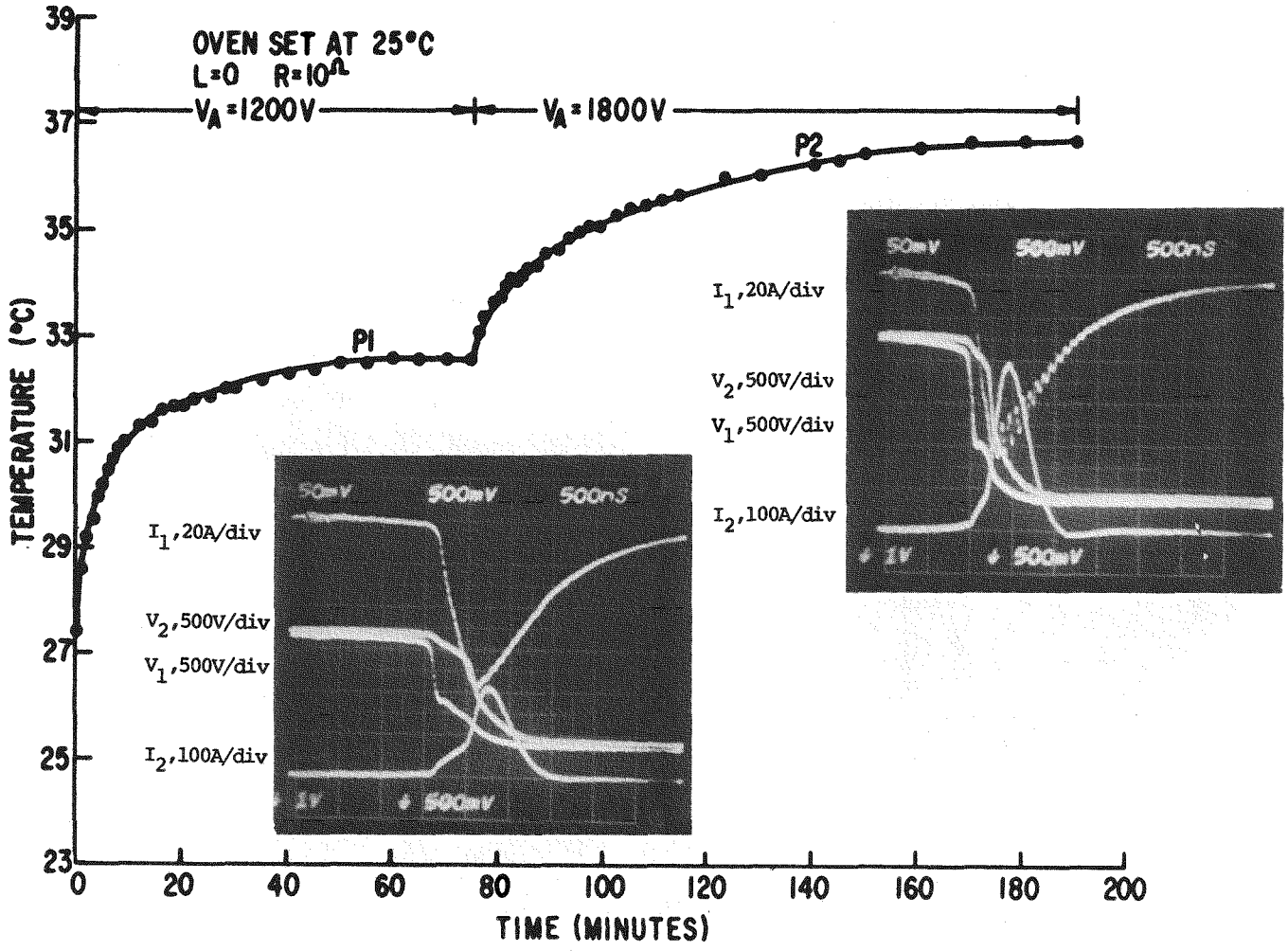

Figure 7-4. Prolonged di/dt test using the test circuit in Figure 7-1. P1 and P2 indicate the points at which the inset photographs were taken. The oven temperature was 25°C. A series resistance of 10Ω was used. The snubber was 0.1 μf, 1.25Ω. The time scale is 0.5 μsec/div.

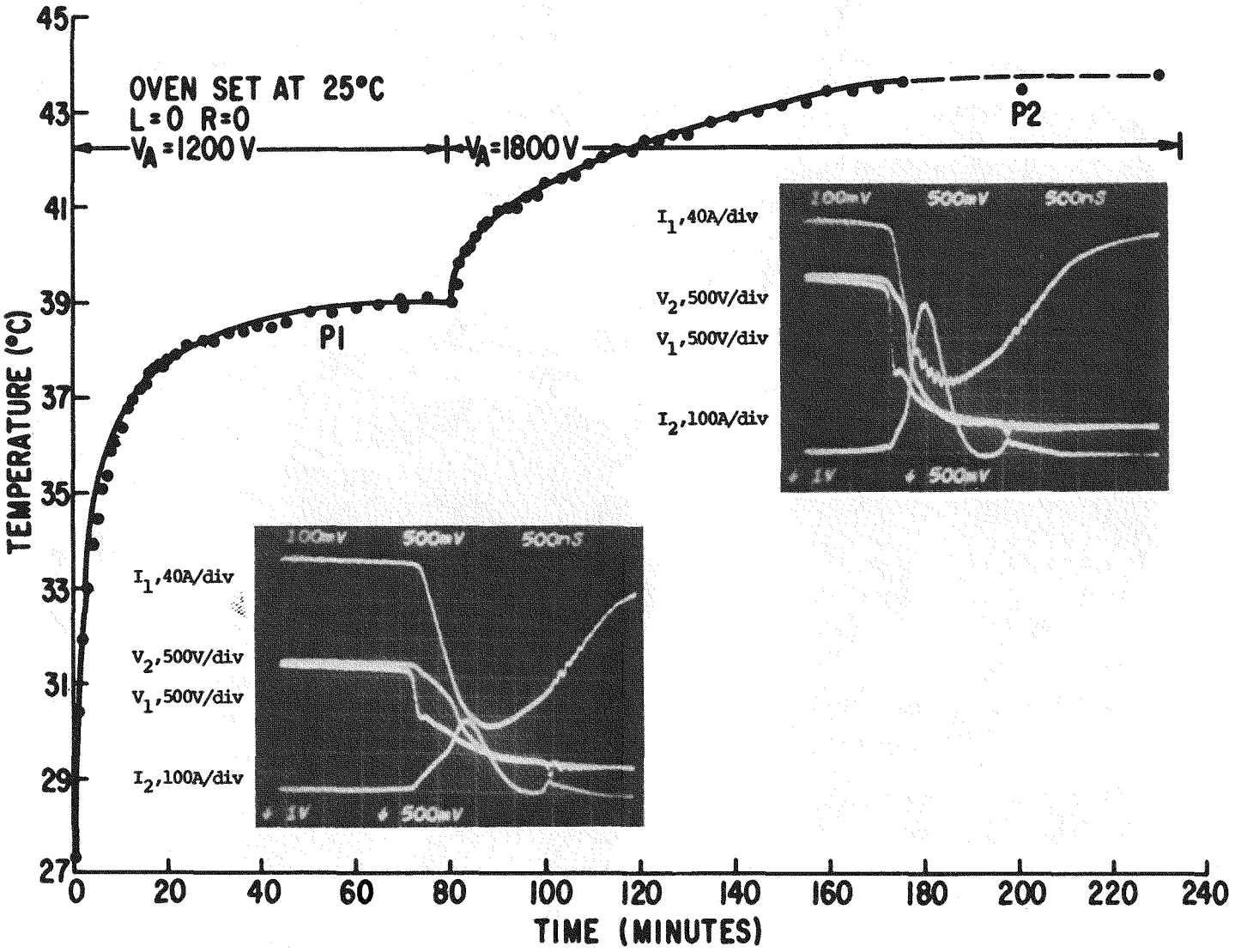

Figure 7-5. Prolonged di/dt test using the test circuit in Figure 7-1. P1 and P2 indicate the points at which the inset photographs were taken. The oven temperature was 25°C. A series resistance of zero Ω was used. The snubber was 0.1 μf, 1.25Ω. The time scale is 0.5 Ωsec/div.

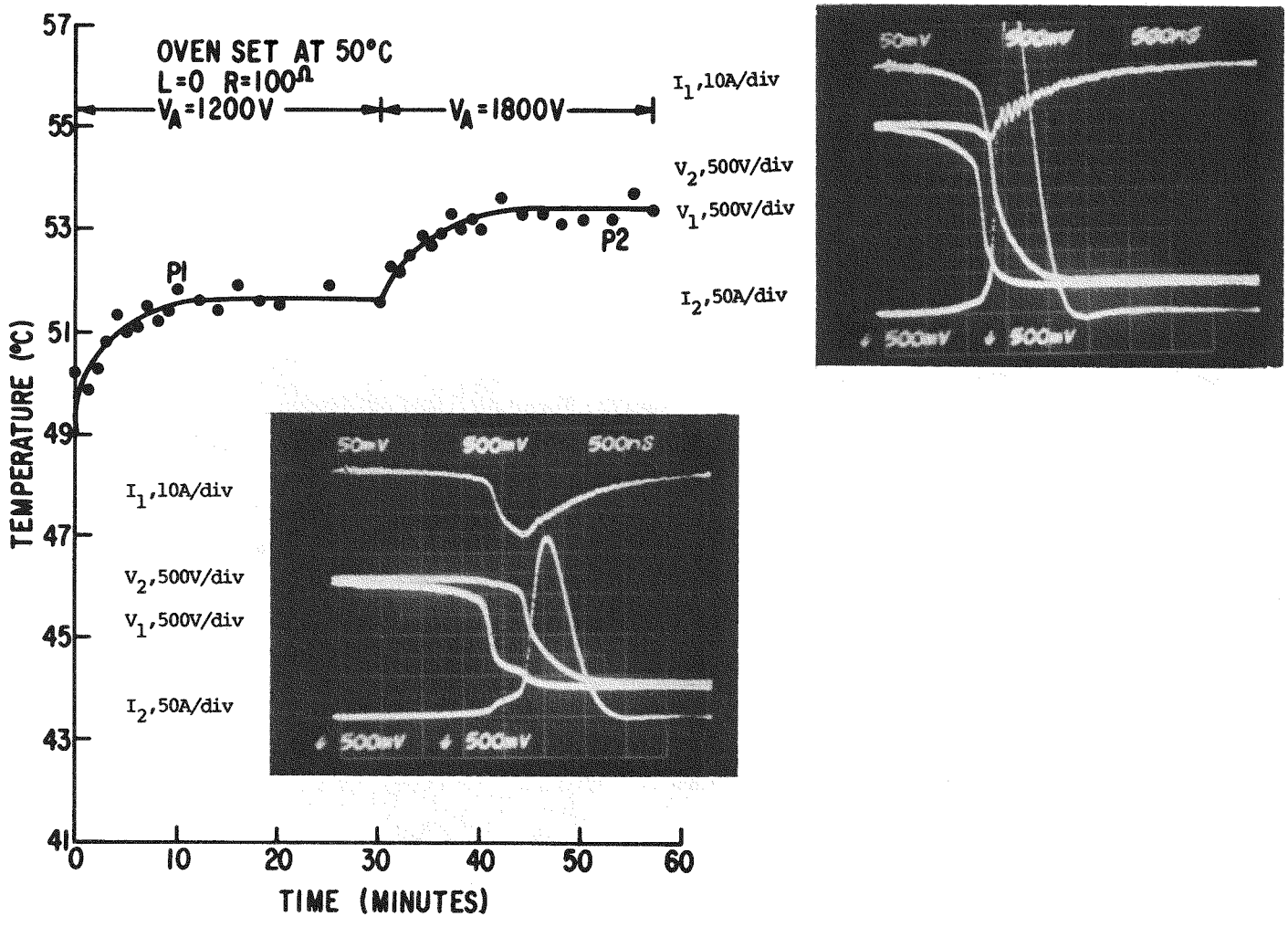

Figure 7-6. Prolonged di/dt test using the test circuit in Figure 7-1. P1 and P2 indicate the points at ehich the inset photographs were taken. The oven temperature was 50°C. A series resistance of 100Ω was used. The snubber was 0.1 μf, 1.25Ω. The time scale is 0.5 μsec/div.

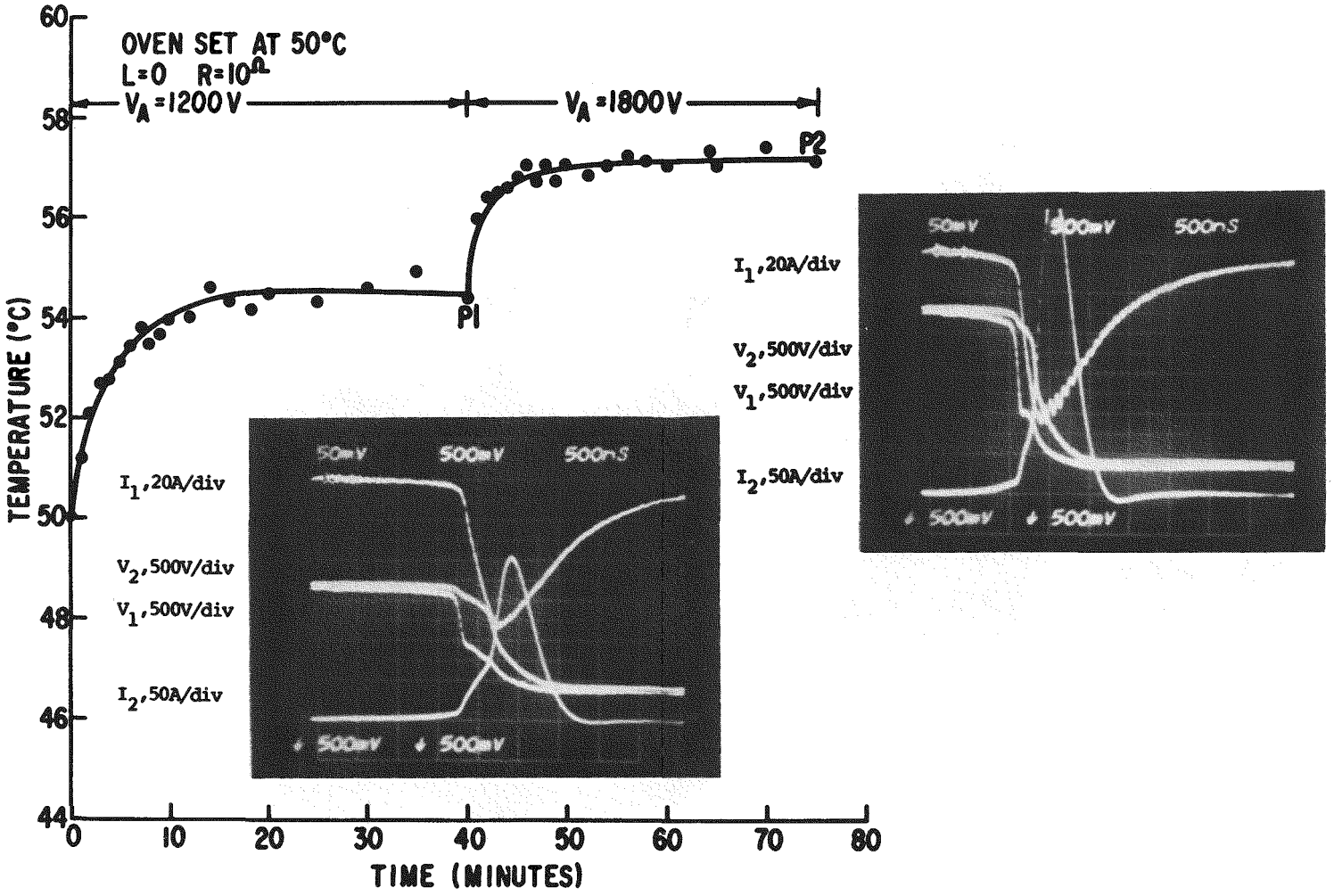

Figure 7-7. Prolonged di/dt test using the test circuit in Figure 7-1. P1 and P2 indicate the points at which the inset photographs were taken. The oven temperature was 50°C. A series resistance of 10Ω was used. The snubber was 0.1 μf, 1.25Ω. The time scale is 0.5 μsec/div.

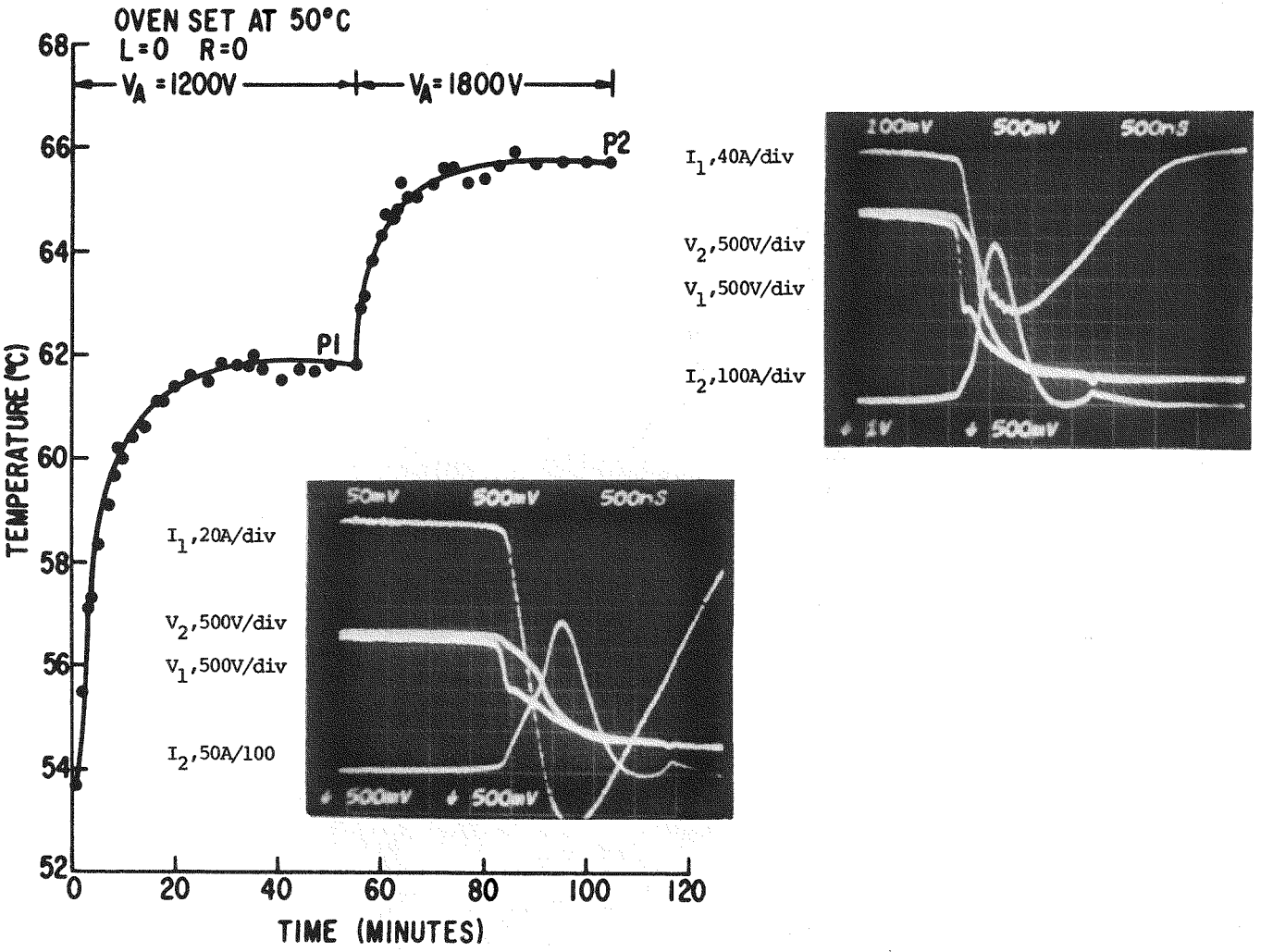

Figure 7-8. Prolonged di/dt test using the test circuit in Figure 7-1. P1 and P2 indicate the points at which the inset photographs were taken. The oven temperature was 50°C. A series resistance of zero Ω was used. The snubber was 0.1 μf, 1.25Ω. The time scale is 0.5 μsec/div.

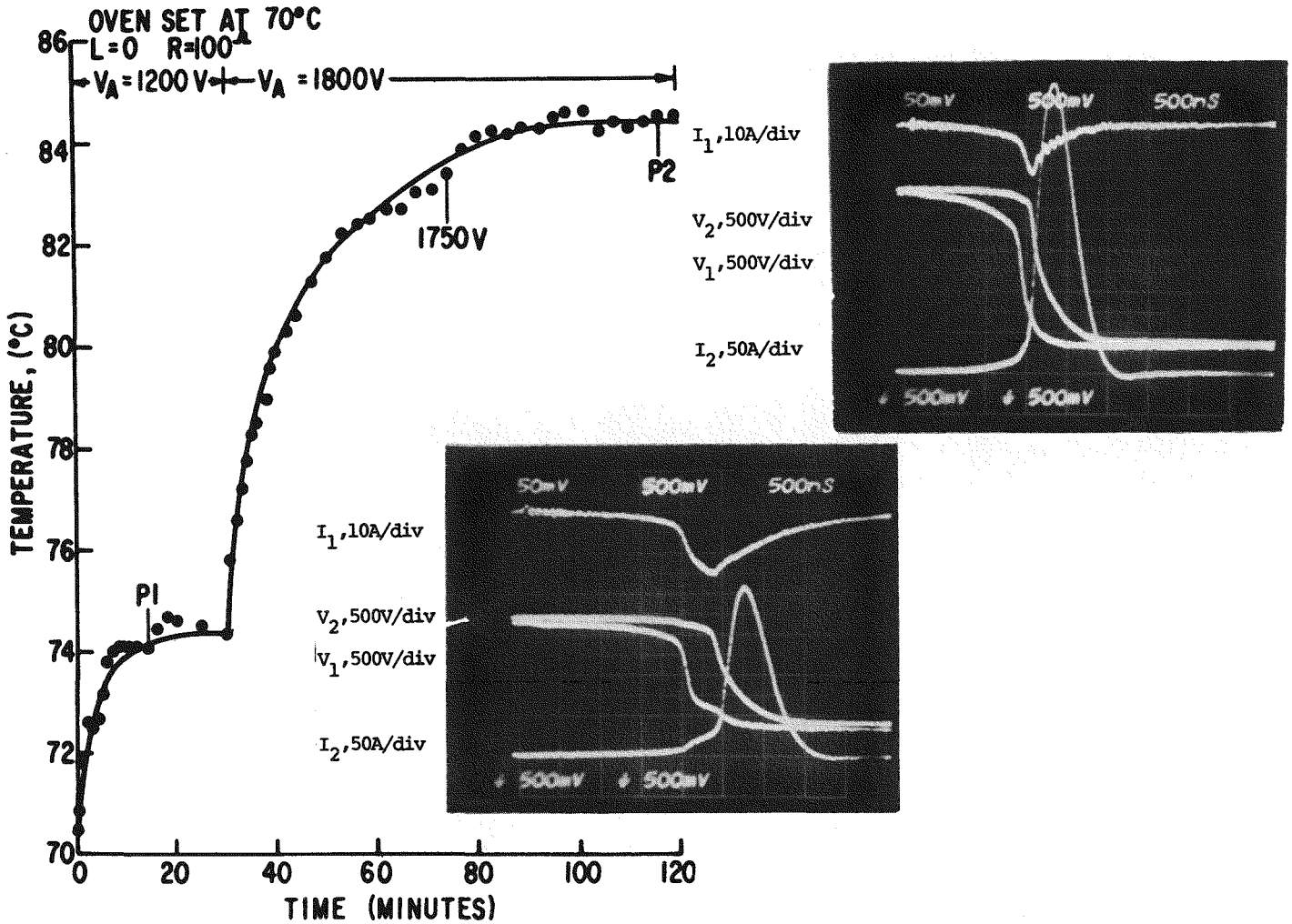

Figure 7-9. Prolonged di/dt test using the test circuit in Figure 7-1. P1 and P2 indicate the points at which the inset photographs were taken. The oven temperature was 70°C. A series resistance of 100Ω was used. The snubber was 0.1 μf, 1.25Ω. The time scale is 0.5 μsec/div.

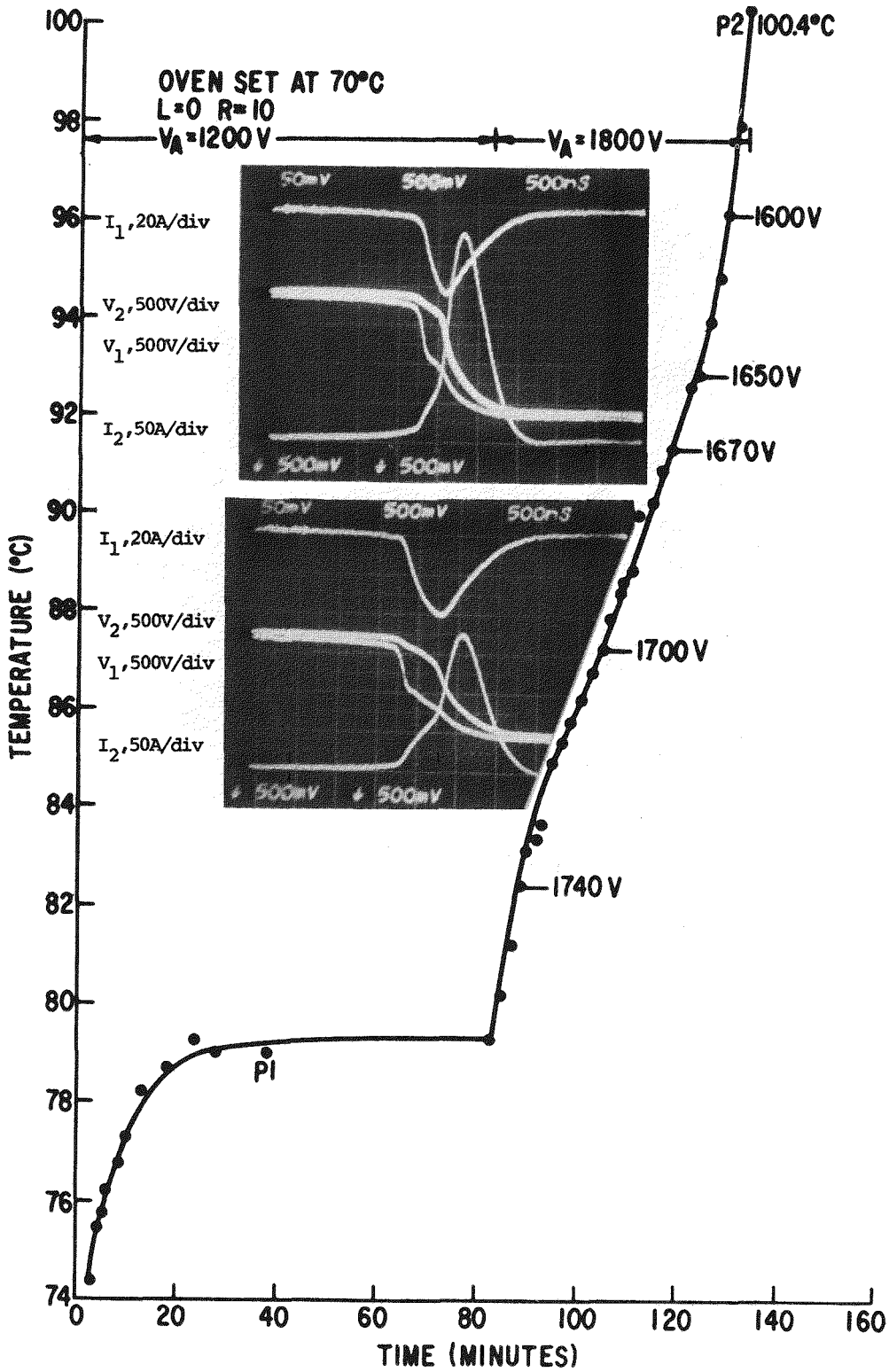

Figure 7-10. Prolonged di/dt test using the test circuit in Figure 7-1. P1 and P2 indicate the points at which the inset photographs were taken. The oven temperature was 70°C. A series resistance of 10Ω was used. The snubber was 0.1 μf, 1.25Ω. The time scale is 0.5 μsec/div.

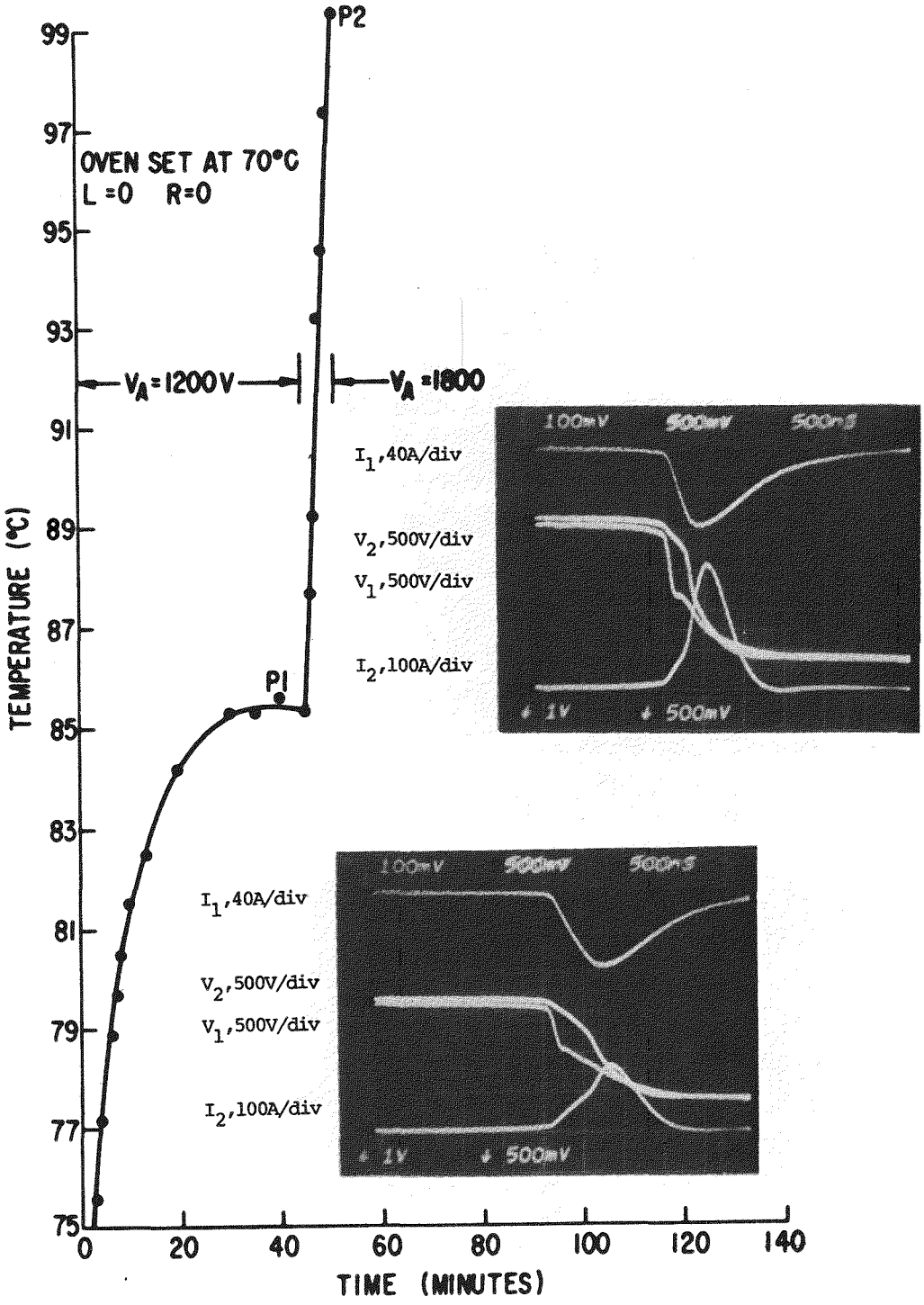

Figure 7-11. Prolonged di/dt test using the test circuit in Figure 7-1. P1 and P2 indicate the points at which the inset photographs were taken. The oven temperature was 70°C. A series resistance of zero Ω was used. The snubber was 0.1 μf, 1.25Ω. The time scale is 0.5 μsec/div.

Section 8

CONCLUSION

A high power directly light triggered thyristor has been developed with high sensitivity to light, firing at as low as 10 njoules of incident photo-energy, and high dV/dt capability, 2000V/μsecond. At room temperature, the device exhibits a very high di/dt capability, approximately 2000A/μsecond, when 5 to 10 times the gate threshold energy is used to turn the device on. This high di/dt capability is partly derived through the internal amplifying gate action of two amplifying stages and partly from the high current densities which occur during turn-on in the gate amplifying stage. However, these high current densities, it has been found, cause undesirable thermal excursions which prevent the present device from having a similarly high di/dt rating at elevated temperatures. Experiments were performed in a hybrid light fired thyristor configuration where the present device was tested successfully provided the average junction temperature of the light fired device was held below 85°C.

Several accomplishments in this phase of the program in addition to device results will facilitate future light fired thyristor development. First is a three dimensional design program which accurately predicts photocurrent turn-on thresholds and dV/dt capability - even in complex interdigitated designs. Second, possible light source-light pipe combinations and a possible package and a possible light source-light pipe system suitable for HVDC application have been identified.

Section 9

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