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TITLE A SIMPLIFIED EXTENSION OF THE LSI-11 Q-BUS FOR A HIGH ENERGY LASER CONTROL APPLICATION

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A SIMPLIFIED EXTENSION OF THE LSI-11 Q-BUS FOR A HIGH ENERGY LASER CONTROL APPLICATION*

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Abstract

Antares, a large, experimental laser fusion facility under construction at Los Alamos National Laboratory in New Mexico, is controlled by a network of PDP-11 minicomputers and microprocessors. The remote nodes of the Antares control network are based on an LSI-11/2 microcomputer interfaced to an STD Bus. This "machine interface" or "MI" forms the intelligent process controller located directly adjacent to the many diverse laser subsystem devices. The STD Bus, linked to the LSI-11/2 microcomputer, offers a standardized, cost effective means for the development of the specialized interface functions required for the high energy laser environment.

1.0 INTRODUCTION

Antares, named after the bright red star in the constellation Scorpio, is a 92,000 square foot experimental laser fusion facility under construction at Los Alamos National Laboratory for the study of inertial confinement fusion. Fusion is the basic energy source of the universe including the sun and the stars. It occurs when two light elements, subjected to extreme heat and pressure, combine to form a heavier element and, in the process, release energy. In 1983, the 40 terrawatt laser will send a 1 ns, 40 kJ pulse of laser energy to a tiny (several tenths of a millimeter diameter) glass microballoon target containing isotopes of hydrogen, deuterium, and tritium. The target will be heated and compressed by 24 beams. A fusion reaction will occur and energy will be released. (The energy equivalent of 300 gallons of gasoline could be produced by reacting the natural deuterium in one gallon of water).

2.0 BASIC ANTARES LASER OPERATION

The path of a single beam through Antares is depicted in Figure 1.0. A low energy pulse generated in an oscillator, preamplified by a pair of CO_2 laser amplifiers, is amplified by an electron-beam-controlled driver amplifier in the Front End room on the lower level of Antares. Produced are two 90-J annular laser beams with an outside diameter of 15-cm. Each of the 90-J beams are directed upward from the lower-level Front End area through an LSI-11 microcomputer-based alignment station into the electron-beam controlled power amplifier. As it enters the power amplifier, the 15 cm driver beam is split into 12 sectors. During the first pass through the power amplifier the 12 beams expand in area by a factor of 200 and are amplified from 2 to 250 J. The power amplifier reflects the beams for a second pass increasing energy of each beam to 1670 J. Steering of the beams through both passes of the power amplifier is accomplished by alignment stations under the control of the Antares computer network.

The center of the power amplifier, the electron gun, generates 12 beam sectors with electron energy of 500 kilovolts and current density of 50 mA/cm^2. The total discharge current of 800 kA for each power amplifier is delivered by four 300-kJ Marx generators that produce an open circuit voltage of 1.2 MV. The simultaneous charging and firing sequence of the four Marx generators is executed by a dedicated section of the Antares control network under the supervision of the beamline PDP-11/60 minicomputer.

Following the second pass through the power amplifier, the 12 sector, high energy beams leave the laser hall and pass through underground evacuated beam tubes on their way to the target building. Entering a device called the turning chamber, the 12 beam sectors are split into 3 groups of 4 beams each by an array of microcomputer-controlled turning mirrors. Folding and focusing

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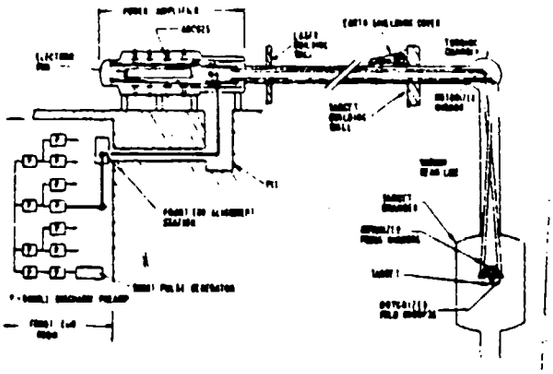

Figure 1.0 Path of a single beam through Antares.

mirrors, also under microcomputer control, allow the total of 24 beams to uniformly illuminate the final destination, the target.

3.0 ANTARES COMPUTER NETWORK HIERARCHY

Operation of the Antares Laser facility is fully automated, and controlled entirely from a central control area. The Antares computer control network hierarchy is generalized in Figure 2.0. The PDP-11/70, three of the four PDP-11/60's, and the PDP-11/34 are located in the central control area. One PDP-11/60 is situated on the lower level of the facility in the Front End control room. LSI-11/2 microcomputers are positioned throughout the 3 major sections of the laser facility.

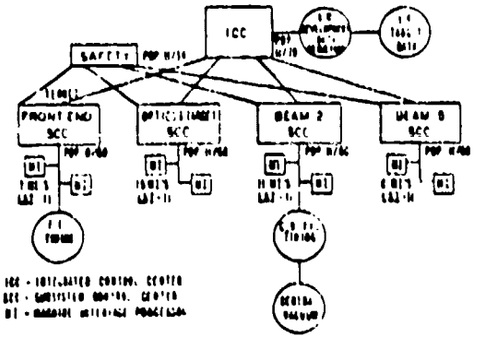

Figure 2.0 Antares control system network hierarchy.

Hardware network interconnections between the levels of the hierarchy are implemented with full-duplex fiber optic communications links.

The central, highest level computer in the Antares computer network is a PDP-11/70 minicomputer running under the UNIX operating system. This supervisory PDP-11/70 provides intergrated control of the four PDP-11/60 minicomputers located at the second level of the network hierarchy.

Implementation of the 4 PDP-11/60's corresponds to the four major subsystems of the laser facility: the Front-End, Alignment and Target, and each of the two main beamlines. Each of the four PDP-11/60's supervise a group of LSI-11/2 bit microcomputers which serve as the most remote nodes in the control network. The UNIX operating system is also implemented on each of the PDP-11/60's. The remote LSI-11/2 microcomputers are downline loaded with application software written in the C programming language. Dynamic, integrated operation of the control network is performed by TENNET, a networking package developed in-house by the Antares software group.

4.0 THE REMOTE MACHINE INTERFACE (MI)

The most remote node of the Antares computer network is the LSI-11/2 based machine interface (MI). Typically, as shown in Figure 3.0, it is located close to the particular laser subsystem device it controls. The machine interface is divided into 2 major subsections: the computer end and the laser end. At the computer end is the LSI-11/2 micro-computer interfaced to a 32 slot STD Bus. The LSI-11/2 microcomputer configuration is standard throughout Antares. Five modules, the cpu, memory, serial I/O, parallel I/O, and power-fail make up the Antares "universal" microcomputer. An optional sixth module, a Camac Crate controller interface, is implemented as required. Connection between the LSI-11/2 and the STD Bus is made through the DRV11 general purpose parallel interface. The DRV11 parallel interface consists of 16 latching outputs (DROUTBUF), 16 nonlatching TTL inputs (DRINBUF), and 6 TTL control/status bits (CSR). The application of these three DRV11 registers for STD Bus control is shown in Figures 4.0, 4.1, and 4.2.

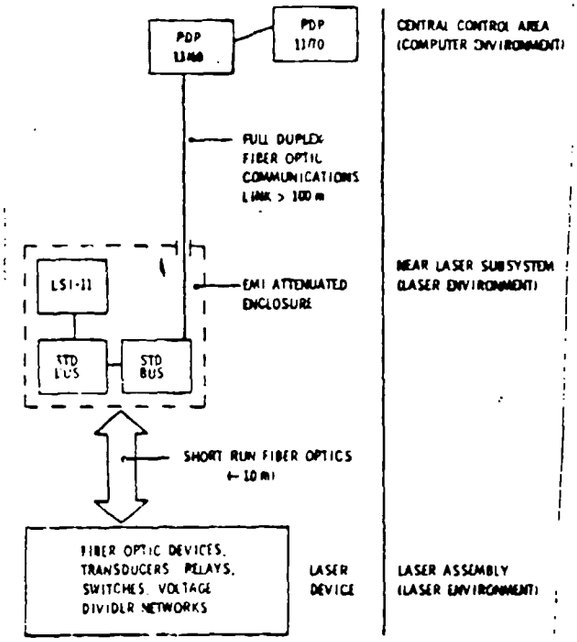

Figure 3.0 Antares machine interface (MI).

4.1 DROUTBUF register.

DROUTBUF, the output register of the DRV11 illustrated in Figure 4.0, allows the LSI-11/2 to address and write data to the STD Bus. The basic addressing scheme uses 8 bits: 5 for the STD module address, and 3 for the port addresses within each module. Such an arrangement allows 32 STD cards with 8 registers each to be addressed directly. If each register is 8 bits wide, control for a total of 2048 elements on a single STD Bus is possible (32 X 8 X 8).

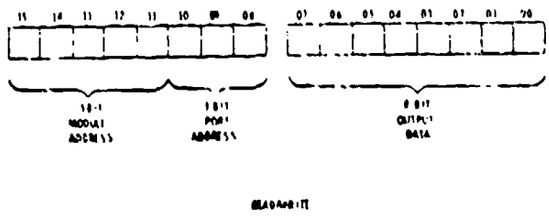

Figure 4.0 DRV11 output buffer bit assignments for the STD Bus.

DROUTBUF also contains the 8 bit wide data word for writing data to the 8 bit STD data bus. Since DROUTBUF is a read/write register, both the address and data written to the STD Bus by the DRV11 can be read back to the LSI-11/2 by simple interrogation of the DRV11 register.

4.2. DRINBUF register.

DRINBUF, the parallel input register of the DRV11, is shown in Figure 4.1. DRINBUF permits 16 bit wide data words to be read from the STD Bus in a single operation. This allows STD modules with 10 or 12 bit analog-to-digital converters to be serviced with one parallel read from the DRV11.

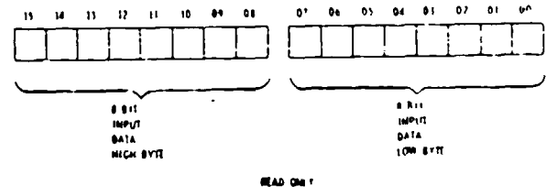

Figure 4.1 DRV11 input buffer bit assignments for the STD Bus.

4.3 CSR register.

Figure 4.2 illustrates the implementation of the DRV11 control status register (CSR) on the STD Bus. Two bits of the CSR register are utilized in the present interface. Bit 00 permits read or write operations on the STD Bus: 0 = Read, 1 = Write. Bit 01 allows the basic 8 bit STD Bus addressing scheme to be expanded. This bit is interfaced to the IOEXP* (I/O Expansion) control line on the STD Bus allowing a second group of 32 STD modules to be addressed by the same DRV11. Two 32 slot STD Bus card racks are daisy-chained in applications requiring more than 32 slots. Address selection of the first or second STD Bus is accomplished with the IOEXP* control bit.

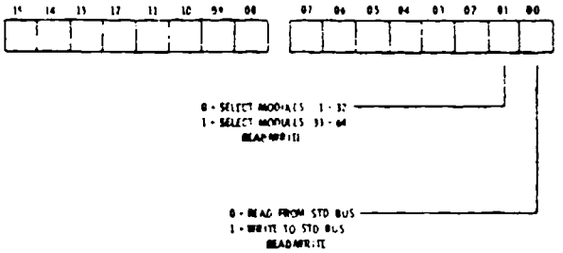

Figure 4.2 DRV11 control/status register bit assignments for the STD Bus.

5.0 THE STD BUS

The Std Bus standardizes the mechanical and electrical aspects of the Antares control and instrumentation modules. The basic mechanical dimensions for the STD module are shown in Figure 5.0. The STD Bus motherboard approach allows any module to operate in any slot; the module address is set on-card and is slot independent. Note that not all of the pins available on the STD Bus are utilized in the current STD/LSI-11 interface. Figure 6.0 illustrates the actual interconnection between the LSI-11 and the STD Bus. The functional relationship of the LSI-11 Q-Bus and the STD Bus is shown in Figure 7.0.

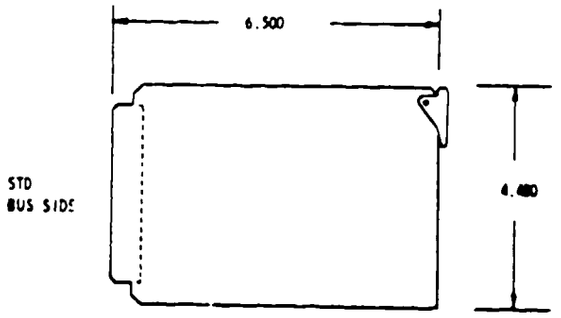

Figure 5.0 Basic STD Bus mechanical dimensions.

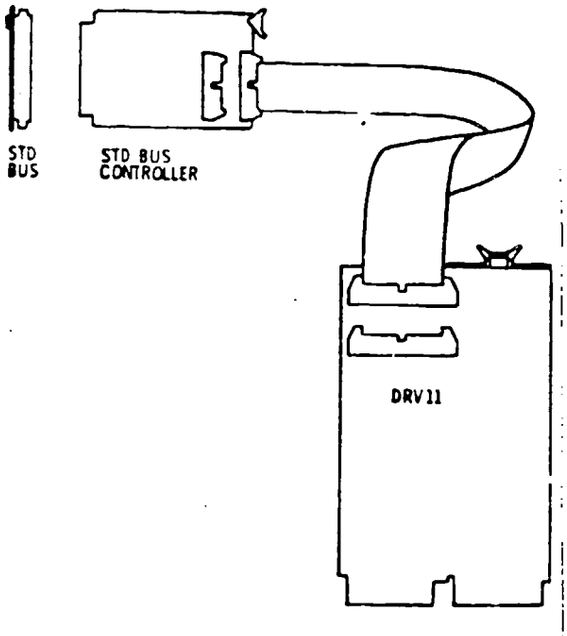

Figure 6.0 DRV11 to STD Bus interconnection scheme.

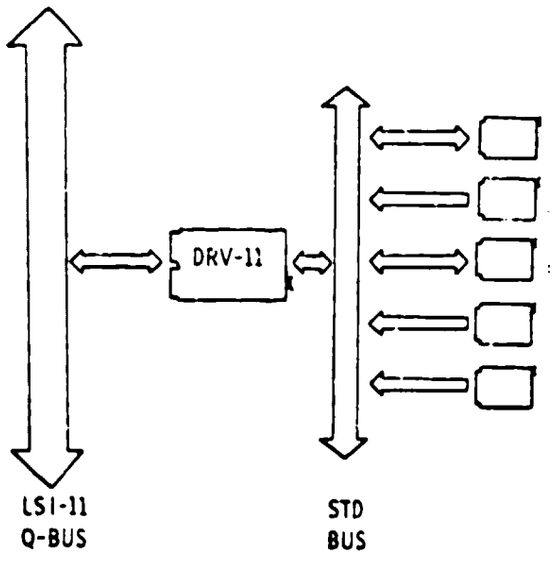

Figure 7.0 Q-Bus control of the STD Bus.

6.0 ANTARES STD BUS MODULES

All connections between the MI STD bus modules and the Antares laser subsystem devices are made with fiber optic technology. The severe EMI environment created by operation of the Marx generators and the Antares Power Amplifiers restricts the use of metal conductor control connections. The basic function therefore, of the Antares STD Bus modules, is to transmit and receive some type of signal at optical levels.

Wavelength of the transmitters and bandwidth of the receivers depend upon the particular application. Transmitters presently implemented include incandescert lamps, L.E.D.'s, and laser diodes. P-I-N diodes and integrated photodiode-preamplifier-schmitt detector circuits are typical receivers. The two general categories of Antares STD Bus modules are shown in Figure 8.0.

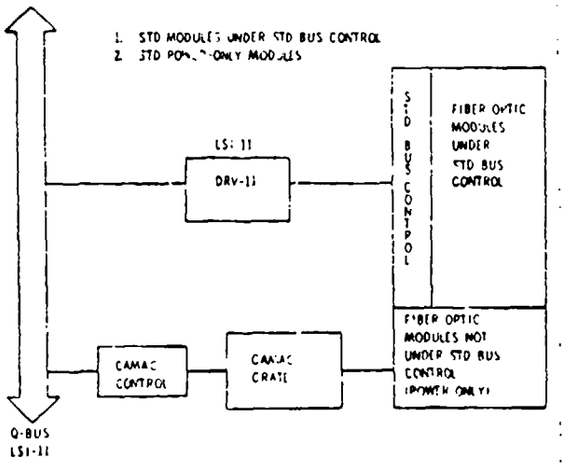

Figure 8.0 Two basic categories of Antares STD Bus modules.

The first category includes modules under STD Bus control; those that communicate with the LSI-11 through the DRV11 interface. Cards that implement relatively low speed binary and analog monitor-control functions are included in this first category. High speed functions, such as Camac waveform digitizer fiber optic interfaces, make up the second category. Both categories reside in the STD Bus; the second category makes use of the power connections only. Utilization of the same standardized STD Bus mechanical dimensions for the second category eliminates the need for an additional, specialized chassis with separate power supplies, development guidelines, etc. Even though the modules in the second category do not use the STD Bus for address, data, and control, the standardized features of the STD Bus chassis offer a convenient solution for location of the interface functions.

6.1 AN ANTARES CATEGORY 1 STD BUS MODULE.

Figure 8.1 is a generalized block diagram of an Antares STD Bus module under STD Bus control. The illustration represents a low speed analog monitor interface function.

A voltage divider network within an Antares high voltage Marx generator provides a μA current proportional to the 0 to 60 kV Marx charge voltage. As the Marx generator is charged, the μA reference current is converted at the laser end to a 0 to 25.6 kHz square wave by a voltage-to-frequency converter circuit. The output of the converter circuit provides drive current for a fiber optic transmitter. The optical pulse train leaving the laser-end circuit travels over a 10 meter fiber optic cable to the computer-end STD Bus module. Here, a fiber optic detector converts the optical level signal to a TTL pulse train. The basic function of the computer-end STD Bus module is to serve as a frequency counter; the 0 to 25.6 kHz signal is gated, counted, and stored in a continuous manner. New data is available to the LSI-11/2 via the STD Bus at a rate of 50 times per second. Four complete channels of this interface function are implemented on a single STD Bus module.

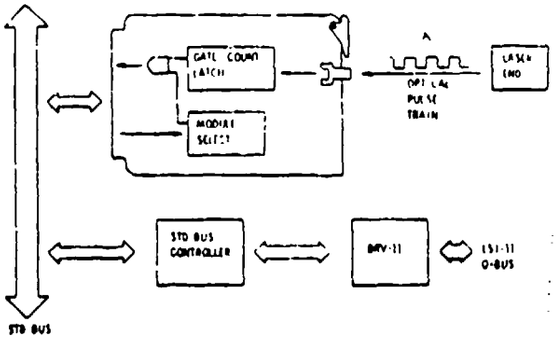

Figure 8.1 An example of Antares STD Bus module, category 1.

6.2 AN ANTARES CATEGORY 2 STD BUS MODULE.

Figure 8.2 is a block diagram of an Antares STD Bus module not under STD Bus control. The figure illustrates a high speed analog monitor function.

When the Antares Marx generators are discharged into the power amplifier, the characteristics of the microsecond range discharge waveforms are relevant subsystem performance data. A transient-protected fiber optic L.E.D. transmitter located within the Marx generator is powered by current from the signal it monitors.

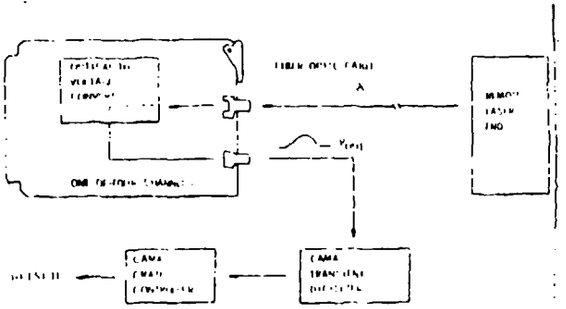

Figure 8.2 An example of Antares STD Bus module, category 2.

When the Marx generator discharges, the L.E.D. launches light into a fiber optic cable at a level proportional to the input signal. The opposite end of the fiber is connected to a high speed analog monitor module located in the STD Bus. The primary function of the module is to convert the optical level pulse to an analog voltage. The converted pulse is then sent directly to a waveform digitizer in an adjacent Camac chassis. The pulse waveform is digitized and stored by the Camac module. The LSI-11/2 reads the digitizer by means of the Camac controller interface module. In this example, the STD module provides conversion of a signal from optical levels to analog voltage levels. The only connection to the STD Bus is for DC power requirements. The STD Bus provides a modular approach towards the implementation of this interface function.

7.0 SUMMARY

Antares, a laser fusion facility under construction at Los Alamos National Laboratory, provides a challenging environment in which to apply a computer-based control network. The specialized requirements of the many diverse laser subsystems necessitates a modular, building-block approach for instrumentation and control functions. The STD Bus offers a well defined, standardized set of mechanical and electrical specifications. Engineering and development of specialized interface functions is facilitated by the standard framework within which to work.