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ABSTRACT

Thin-film polycrystalline silicon solar cells offer a potential low-cost alternative to single crystal silicon. This paper reviews the progress in polycrystalline silicon solar cell research in areas of thin-film material and cell development, and in the basic understanding of the effects of grain boundaries and the passivation of these effects. Current concerns in this area include the scalability of the more promising approaches, the reliability and stability of the cells and modules, and an assessment of the low-cost potential of the technologies. Recent progress in addressing these important problem areas is described.

INTRODUCTION

Thin-film polycrystalline silicon solar cells offer a potential low-cost alternative to single crystal silicon solar cells, while maintaining the attributes associated with silicon: viz., abundance, relatively high efficiency, stability, and the existence of a broad technology base. In the past decade, there has been considerable interest in the development of polycrystalline silicon solar cells for terrestrial use by researchers in the United States as well as in other countries (1-3). The low-cost potential of the thin-film technologies lies in lower material utilization and in more economical fabrication processes than for single crystal or bulk polycrystalline silicon technologies.

Questions which frequently arise in connection to thin-film polycrystalline silicon solar cells pertain to the definition of the term "thin film" and to the effects of grain size. Since both the performance and the cost of the solar cell involve, in a rather complicated manner, the variables of film thickness and grain size, a clear answer to these questions is not possible. Theoretical modelling (4) has indicated that, for 100 μm film thickness, grain sizes of at least 200 μm will be required for >10% efficient solar cells; smaller grain sizes will require some form of passivation of grain boundary effects. Preliminary cost/performance considerations suggest that film thicknesses of <100 μm will be optimum for efficient, low-cost solar cells.

Polycrystalline silicon is one of the thin-film technologies supported under the Department of Energy's (DOE) Photovoltaics Advanced R&D program (5). The objectives of this program, managed by the Solar Energy Research Institute (SERI), are to identify and develop methods for fabricating polycrystalline silicon solar cells with photovoltaic conversion efficiencies of 10% or greater by 1980, and to demonstrate a module cost feasibility of less than $500/peak kWe (in 1980 $). The research efforts over the past several years have resulted in the achievement of the first of these objectives; viz., relatively efficient (>10%, AM1), large area (>1 cm^2) solar cells have been produced by a number of potentially low-cost approaches. Based on the demonstrated results on cell efficiency, cell area, stability and low-cost potential, SERI has initiated during 1980 the "Exploratory Development of Thin-Film Polycrystalline Silicon Photovoltaic Devices." The objective of this Exploratory Development (ED) program, and of a subsequent Technology Development (TD) phase, is to demonstrate the module cost feasibility goal. The activities are expected to provide experimental proof that laboratory-type cells exhibit reproducibility, stability, encapsulability, and adequate size, and meet photovoltaic program efficiency and cost goals to enhance material transition from research and development to technology development.

In addition to the ED program, the polycrystalline silicon program at SERI includes a subtask on Research and Development; the latter is concerned with R&D on materials, cells and the basic studies of grain boundary effects in polycrystalline silicon. The goal of the R&D programs is to identify and develop alternate promising low-cost technologies, and to provide basic research support for the advanced development efforts. Currently, the ED program consists of three subcontracts and the R&D program consists of twenty-four subcontracts; the annualized level of funding of these programs is approximately seven million dollars. The program involves participation by both large and small business, as well as by Universities and National Laboratories. In addition, in-house R&D efforts at SERI contribute to the program.

This paper reviews the progress in polycrystalline silicon solar cell research which has occurred under the DOE/SERI program in the areas of thin-film material and cell development, and in the basic understanding of the effects of grain boundaries and the passivation of these effects. Progress under the ED and R&D subprograms is reviewed in the next two sections. We conclude with an overview of outstanding technical concerns and problems which guide some of the current and future research directions.

EXPLORATORY DEVELOPMENT PROGRAMS

Polycrystalline silicon is the first advanced material/thin-film technology which has satisfied the criteria for transition from advanced R&D toward technology development. A material technology is ready to enter this transitional or ED phase when (5): (a) it has demonstrated a cell efficiency that indicates it will be a cost-effective technology; (b) it possesses a capability for inherent cell stability; and (c) there is an understanding of the basic principles governing the technology. Further transition into the TD phase will require experimental proof indicating that: (a) the technology through encapsulation will be life-cycle cost effective; (b) there is a demonstrable understanding of the techniques necessary to engineer the technology; (c) there is adequate materials availability; and (d) no significant adverse environmental effects are known.

As a result of a competitive solicitation during 1980, SERI awarded three subcontracts for ED in polycrystalline silicon. The participating organizations in the program are: Honeywell Corporate Technology Center, Motorola, Inc., and RCA Laboratories; the respective technologies are discussed below. Although specific technical goals are different for each subcontractor, the overall goals of the ED program are to: (a) utilize a semiconductor-grade (sg) silicon thickness of less than 100 μm ; (b) reproducibly demonstrate a solar cell efficiency of >11%, AM1 on a cell area 20 cm^2; (c) demonstrate a module efficiency of >9%, AM1 on a module area >900 cm^2; (d) show a module cost potential of <\$500/peak kWe (1980 \$); (e) establish scalability, reliability and reproducibility of the processes; and (f) transfer a technology to the TD phase.

In the following, we describe briefly the technical approaches, and review the status of each of the ED programs. A brief discussion of the low-cost potentials of the technologies is also given.

Honeywell's EPI/SOC Approach

In their ED program, Honeywell is extending the silicon-on-ceramic (SOC) technology (6) to prepare low-cost substrates for the epitaxial deposition of thin-film polycrystalline silicon (hence the term EPI/SOC). The SOC layers are prepared by the silicon-coating-by-inverted-meniscus or SCIM technique shown schematically in Fig. 1. In the process, a carbon-coated mullite substrate is passed over a trough containing molten silicon at an angle with respect to the horizontal of 15 to 20 degrees to achieve growth stability. Thin (~ 100 μm) silicon layers are obtained on the carbon-coated side of the slotted substrate; the slots are necessary to allow back contact access to the silicon layer. Solar cell efficiencies of 10.5% on 5 cm^2 area have been reported on dip-

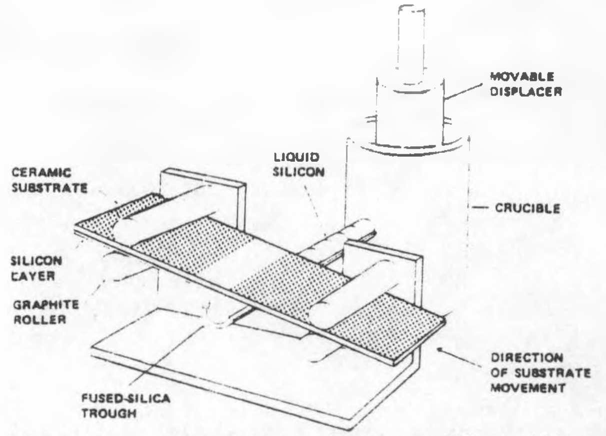

Figure 1: Schematic of Honeywell's silicon-coating-by-inverted-meniscus (SCIM) technique (Ref. 7).

coated (6) SOC layers obtained from sg-silicon feedstock.†

In an attempt to increase the cell efficiency and to reduce the cost, the EPI/SOC approach involves metallurgical-grade (mg) silicon as the feedstock material for SCIM coating. A thin (~ 30 μm) active layer of sg-silicon in then grown epitaxially by chemical vapor deposition. The heavily doped SOC layer offers several potential advantages over the sg-SOC: e.g., the high-low junction between the SOC layer and the lightly doped epitaxial layer provides a back-surface-field (BSF) effect. The heavy doping also reduces the problems with series resistance at the back contact; slots could be more widely spaced than in the current sg-SOC approach. In the ED program, Honeywell is attempting to identify the most effective of the three options utilizing the SOC technology: viz., EPI/mg-SOC, EPI/heavy-doped sg-SOC, and solar cells fabricated directly in sg-SOC.

Currently, 1 m long x 10 cm wide slotted ceramic substrates are routinely SCIM coated with both heavily and lightly doped sg-silicon. Silicon layer thicknesses of 100 μm are achieved at coating speeds of 4 to 5 cm/min; at these speeds, there is a strong tendency toward dendrite formation in the layers. Growth at lower speeds (<2 cm/min) reduces dendrite formation, but produces thicker layers. The attainment of nearly uniform coating thicknesses has resulted from resolution of the two major problems experienced in SCIM coating: viz., the uniformity of the transverse temperature profile along the trough; and problems with the substrate transport mechanism. Initial experiments with mg-silicon coatings, using dip-coating (6),

†Standard measurements of solar cell efficiency at air-mass-one (AM1) illumination are carried at SERI by the Photovoltaic Measurements and Evaluations (PV M&E) Laboratory. Throughout this paper, the term "AM1" is used to designate SERI-measured efficiencies; efficiency values without the designation have been measured and reported by the subcontractors.

gave satisfactory results; the morphology of the SOC layers was similar to that obtained with sg-silicon feedstock.

SCIM-coated sg-SOC material has resulted in 7.6% efficient solar cells (5 cm^2 area); this is a promising result since the carbon parts in the growth system were not purified. Cells fabricated by ion implantation on dip-coated sg-SOC showed efficiencies of up to 8.7%. Baseline epitaxial solar cells on single crystal silicon substrates have resulted in 12.2% efficiency, which indicates that the epitaxial growth process is under control. Initial results on EPI/SOC cells, with heavily and lightly doped sg-SOC substrates, gave poor results; the best cell to date is 4.11% efficient with an anti-reflection (AR) coating. Somewhat better results (4.6% best efficiency without AR coating) were reported by RCA Laboratories for epitaxial solar cells on sg-SOC material. The poor cell efficiencies are believed to result from auto-doping of the epitaxial layer by the ceramic substrate. Other work on Honeywell's ED program involves studies on low-cost metallization and cost-effective module fabrication technologies for sg-SOC and EPI/SOC materials.

Motorola's EB/RTR Approach

Motorola's mainline approach in the ED program involves the ribbon-to-ribbon (RTR) recrystallization of thin microcrystalline silicon sheets by a scanned electron beam (EB). A schematic of the EB/RTR process is shown in Fig. 2. The microcrystalline feedstock is obtained by chemical vapor or high pressure plasma deposition (CVD or HPP) of silicon from $SiCl_4$ or $SiHCl_3$ unto a temporary molybdenum substrate, followed by thermal expansion shear separation (TESS) of the silicon film from the substrate. The molybdenum substrate is reused in subsequent depositions; the silicon film is lightly etched (~ 5 µm) to remove Mo contamination from the substrate interface prior to recrystallization. In the RTR process shown in Fig. 2, the molten zone extends across almost the entire width of the sheet; the "rigid edges" provide more stable growth than in the case where the edges are melted.

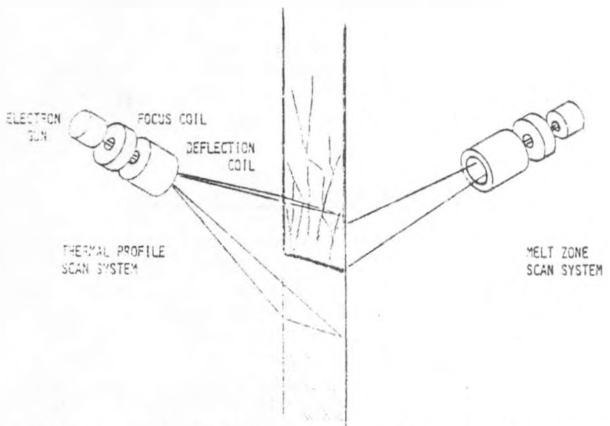

Figure 2: Schematic of Motorola's electron-beam ribbon-to-ribbon (EB/RTR) recrystallization technique.

The EB/RTR process offers several advantages over the laser beam recrystallization (or LB/RTR) process developed previously (8). The EB is lower cost and higher efficiency than the LB; also, the desired temperature profiles in the ribbon are easily achieved using scanned EB. On the other hand, EB requires vacuum, and it does not provide inherent stability of the molten zone (as is the case with LB/RTR). Thus, EB/RTR requires the development of sophisticated electro-optic monitoring and control systems.

Microcrystalline ribbons have been routinely grown on Mo substrates by both the CVD and HPP processes; deposition rates are typically 5 µm/min. Shear separation of large area (5 cm wide x 30 cm long), thin (50 to 300 µm) ribbons has been achieved. In a previous SERI-funded program (9), the mechanism of TESS was identified to be related to void growth at the $MoSi_2$-Si interface. Removal of the $MoSi_2$ was found to be necessary after 6 or 7 deposition/shear separation cycles to obtain reliable TESS. In the ED program, the recyclability of the Mo substrates has been demonstrated using either surface grinding or electropolishing after 6 deposition/separation experiments. At present, electropolishing appears to offer advantages in controllable removal of the $MoSi_2$. Motorola has also completed design of a semicontinuous CVD system for the simultaneous deposition of four ribbons. Continuous deposition is required to obtain uniform thickness ribbons; this would also improve the reliability of shear separation. After initial testing in the CVD mode, the system will be operated in the more material-efficient HPP mode. The semicontinuous operation of HPP deposition has already been demonstrated (9).

The basic feasibility of EB/RTR has been experimentally demonstrated; major effort on the program to date has been on development of the computer/EB system interface for melt shape analysis and control, and for thermal profile control in the ribbon. LB/RTR has been used routinely to provide material for cell fabrication experiments. Growth rates of 2 to 4 cm/min yield flat, stress-free ribbons; previously, rates of up to 7.5 cm/min and multiple ribbon growth have been demonstrated using LB/RTR (8).

Large area solar cells are routinely fabricated in the LB/RTR material using CVD ribbon feedstock. The highest efficiency obtained to date on 32 cm^2 area is 11.6%; the reported solar cell parameters are J_{sc}=26.2 mA/cm^2, V_{oc}=0.585V and FF=75.8%. The best efficiency obtained on 48 cm^2 area is 10.3%. Efficiencies of up to 13.7% were reported on small area (2 cm^2) cells. Solar cells have also been fabricated from HPP-deposited ribbons following LB/RTR (9); an efficiency of 10.6%, AM1 has been measured on a 9.8 cm^2 area solar cell. Studies on cells fabricated on high quality, single crystal materials, which have been LB recrystallized, have shown that dislocation density rather than impurities or grain boundaries is limiting the efficiency of the polycrystalline RTR solar cells. This implies that future work on improving the cell efficiency should be directed at controlling the thermal profiles during RTR; this task should be easier with the EB/RTR approach.

RCA's EPI/HEM Approach

The RCA program is based on recent DOE/SERI supported research (10-13) which showed that relatively high efficiency (>10%) thin-film solar cells can be fabricated by the epitaxial growth of a 15 to 30 µm silicon layer on a large grain size polycrystalline silicon substrate. A schematic of RCA's basic approach is shown in Fig. 3. The epitaxial films are usually grown by CVD; the p/n junction can be formed either by changing the doping during CVD or by conventional techniques (diffusion, ion implantation, etc.). The low-cost potential of this approach lies in the fact that the polycrystalline silicon substrate may be of a much lower purity (e.g., mg-silicon) than the sg-silicon used in conventional ingot and ribbon approaches to low-cost silicon photovoltaics. As discussed in the next section, extensive investigations have been carried out, under the R&D subprogram, on techniques to purify mg-silicon and to produce low-cost polycrystalline silicon substrates for epitaxial growth.

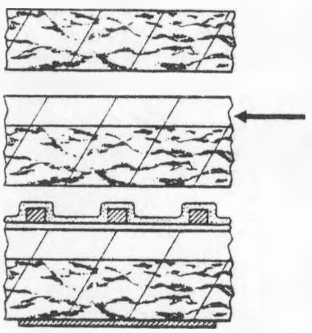

Figure 3: Schematic of basic approach in RCA's EPI/HEM process.

The mg-silicon substrates on this program are prepared by a directional solidification process referred to as the Heat Exchanger Method (HEM), under a subcontract from RCA to Crystal Systems, Inc., and the subsequent sectioning and slicing of the cast ingot (14). The substrate development task involves identification of suitable commercially available mg-silicon feedstock, and development of low-cost HEM solidification and purification processes. The major emphasis at RCA is on furthering the development of the epitaxial growth process. A laboratory-scale horizontal reactor, and a baseline epitaxial growth process, are used to qualify the HEM substrates. The questions of substrate area scale-up, throughput and reproducibility are being examined in RCA's High Throughput Reactor (HTR). Theoretical studies are being carried out to delineate the advantages and disadvantages of batch epitaxial-process approaches, such as HTR, compared to conceptual, continuous epitaxial-process approaches to solar cell fabrication. Such studies are necessary to guide future developmental work.

In the program to date, various mg-silicon sources have been used to prepare the HEM substrates. A major problem which has been uncovered is the existence of particles/precipitates throughout the HEM ingot which subsequently lead to shunting in large area EPI/HEM devices. The particles appear to be SiC, and often have various impurities (Fe, Ca, etc.) associated with them. A high level of carbon in the mg-silicon is believed to be the cause of the precipitates; the problem is worse for some of the mg-silicon sources (e.g., Union Carbide). A solution to this particle problem is crucial for large area solar cells, since the shunting reduces both the efficiency and the yield.

On selected, small area HEM substrates, relatively efficient epitaxial solar cells have been fabricated. The highest reported efficiency is 11% on 2.3 cm^2 area and 9.7% on 10.2 cm^2 area. Variations of cell efficiency with substrate position in the HEM ingot were also examined; in general, the bottom and central portions of the ingot gave the best results. The fabrication of larger area devices is awaiting completion of the necessary modifications to the HTR. Baseline epitaxial growth runs in the HTR, using 7.5 cm diameter, low-resistivity single crystal substrates, have shown good results. Uniform thickness and resistivity epitaxial layers (i.e., less than 10% variation) and uniform quality, large area solar cells were obtained for a batch of 42 wafers. Another significant result in the epitaxial growth studies has been the demonstration that the HCl etching step can be done in a separate reactor, rather than in-situ, without degrading solar cell performance. This finding is important in possible designs of continuous epitaxial reactors.

The compatibility of potentially low-cost cell fabrication processes with the thin epitaxial films has been demonstrated. Screen-printed Ag metallization has been successfully applied to the 7.5 cm diameter baseline epitaxial cells from the HTR. A spray-on TiO_2 AR-coating, applied to several 10.2 cm^2 area EPI/HEM solar cells, has resulted in an average increase in J_{sc} of 42%. The percentage improvement in solar cell efficiency is even greater; it would appear that the spray-on process improves the device characteristics in addition to providing an AR-coating effect.

Low-Cost Potentials of the ED Technologies

The goal of the ED programs described above is to demonstrate a module cost potential of <\$0.50/W_p (1980 \$). Although only preliminary cost estimates have been performed to date, it is expected that a major part of the cost savings will be realized through lower material and substrate fabrication costs. In all three ED technologies, the cell and module fabrication processes are essentially based on techniques being developed under the JPL/LSA Project (15). The compatibility of these processes with the thin-film materials under development is continually being tested in the programs.

RESEARCH AND DEVELOPMENT PROGRAMS

A major objective of the R&D programs in polycrystalline silicon is to provide the necessary low-cost materials development, cell fabrication and grain boundary research support for the more advanced technologies. In addition, there are a number of promising approaches, albeit at a less developed stage currently than the ED options, which show the potential to meet the overall program goals. The discussion of the R&D programs in the following is divided into the elements of Materials R&D, Cell R&D and Basic Studies.

Materials R&D

With the major cost savings expected to come from low-cost materials and processes, the materials R&D efforts are concerned with various ways of purifying mg-silicon, the development of low-cost polycrystalline silicon substrates, thin-film deposition on both epitaxial and foreign substrates, and various novel film and sheet growth techniques.

A silicon purification process based on tribromosilane is under investigation by J. C. Schumacher Co. (16). Potential advantages of this process over the chlorosilanes are a lower temperature of operation, greater energy and material efficiencies, and easier retrieval of the silicon product. To date, the operation of a closed-loop "mini-plant", consisting of a module for the preparation of $SiHBr_3$ from mg-silicon, a distillation module for purification of $SiHBr_3$, and a product module in which $SiHBr_3$ is thermally decomposed to give Si product, has been demonstrated. Both $SiHBr_3$ and Si product have been obtained for analysis; the system operated at approximately 85% theoretical efficiency.

The development of low-cost techniques for the direct purification of mg-silicon has been of interest to several researchers in recent years (17-19). Mg-silicon is readily available at a low cost ($1 to 2/kg) with purity levels of about 98%. The major impurities are Fe and Al (typically 0.1 to 1%), but several other impurities such as B, P, Cu, Ni, Ti, V and W are present in the tens to hundreds parts per million range. The approach in the research is to purify the mg-silicon to some acceptable level for substrate preparation, then deposit an epitaxial film on the substrate for solar cell fabrication. The purification efforts can be categorized into areas of acid leaching, vacuum evaporation, reactive gas treatment, slagging, and directional solidification. Table 1 summarizes the results of the purification experiments and lists the organizations performing the research.

The effectiveness of acid leaching is a function of the mg-silicon particle size (typically 0.5 mm), the reactivity of the acids, temperature and leaching duration. Recent work (17) has shown that leaching with aqua regia at 200° C under a pressure of 20 to 30 atmospheres can lead to lower Fe and Al concentrations in about one-sixth the time it takes at the normal boiling temperature (~80°C) of the acid. Vacuum evaporation and slag removal from the top of the molten silicon have been found to be effective in removing Al, and transition metal impurities with the exception of Fe. Reactive gas treatments (e.g., HCl, SiF_4, H_2/H_2O, $H_2/H_2O + Cl_2$) of molten silicon have been found to be ineffective. Immiscible oxide slags (e.g., CaO/SiO_2, MgO/SiO_2) in molten silicon have been useful in removing Al. Directional solidification (e.g., Czochralski or HEM ingot growth) is the most effective of all the approaches examined; the technique relies on the very low values of equilibrium segregation coefficients (k_o) of the impurities in silicon. With the exception of B and P, the k_o-values are in the 10^{-3} to 10^{-6} range.

Table I: Results of Metallurgical-Grade Silicon Purification Studies.

Technique	Organization	Assessment
Acid Leaching	Motorola Poly Solar	Effective in removal of most impurities under elevated temperature and pressure. Environmental safety is questionable for large production.
Vacuum Evaporation	Crystal Systems Motorola	Effective in removal of Al, Ca, and Mg.
Reactive Gas Treatment	Crystal Systems Motorola	Inconsistent results obtained; not effective.
Slagging	Crystal Systems Motorola	Effective in removal of Al, Mg, Sr. Crucibles cannot be reused.
Directional Solidification	Crystal Systems Motorola Poly Solar	Effective in removal of most impurities except Al, B, Ge, P, and Ti. This technique is desirable if combined with Vacuum Evaporation and/or Acid Leaching

The purified mg-silicon has been used in low-cost substrate preparation and solar cell fabrication studies. Results on EPI/HEM solar cells were described earlier; the researchers have also reported 7.2% efficient, 4 cm^2 area n^+/p solar cells in a directly diffused HEM substrate (19). Czochralski growth of large diameter (15 cm) ingots from purified mg-silicon has resulted in large area and grain size substrates. Several 9-10%, AM1 efficient, 100 cm^2 area solar cells have been fabricated on 50 μm thick epitaxial layers grown on the substrates (18). The use of graphite (17) to support a recrystallized mg-silicon film for epitaxial growth has been de-emphasized recently. The major concern is the availability of suitable quality low-cost graphite for the process.

While the growth of thin films on polycrystalline silicon substrates has been extremely successful, the vapor growth of silicon on various foreign substrates has shown disappointing results. Although heteroepitaxial growth by CVD of thin (~20 μm) silicon films on large grain size (up to 125 μm) alumina substrates has been demonstrated, the films exhibited poor electrical quality (20). Solar cell efficiencies were typically less than 2%. Electron-beam evaporation of silicon has resulted in large grain size (~40 μm) films on TiB_2-coated alumina substrates (21). The TiB_2 served both as a back contact material and as the substrate for silicon growth. The electrical quality of the films appeared to be limited by purity, even at 10^{-9} torr background pressure, rather than by grain size. Chemical analysis has indicated a high concentration (~80 ppm) of Ta in the films. Small area solar cells of 3.6%

efficiency were fabricated. The results of these programs lead to the conclusion that significant generic problems exist in the area of physical or chemical vapor deposition at high temperatures on foreign substrates. Clearly, a much better understanding of grain size and chemistry control in such systems will be required before they will result in useful photovoltaic devices.

Various novel silicon sheet and film growth techniques have evolved recently which show a potential for low cost. One of the more promising approaches is Low Angle Silicon Sheet (LASS) growth (22) which is an extension of horizontal ribbon growth techniques (23). LASS growth has the potential of high rate of sheet area productivity, and the growth of high quality silicon sheets for solar cells. As shown in Fig. 4, the LASS process uses a shallow trough-crucible to reduce convection in the melt, and various passive thermal control elements for growth interface and ribbon shape control. This simple approach contrasts with the complex active heating and cooling elements required in the Japanese work on horizontal ribbon growth (23). To date, research on LASS has resulted in the continuous growth of 5 m long x 3 cm wide x 0.5 mm thick ribbons at a growth speed of about 40 cm/min. A total of 21 m of ribbon was obtained from the same run with intermittent melt replenishment. Ribbon widths of 7.5 cm, thicknesses of 0.3 mm and growth rates of 60 cm/min have also been demonstrated. Several solar cells of greater than 10% efficiency have been fabricated on LASS material; the best measured efficiency is 11%, AM1. Current concerns in the LASS process which are being addressed include: understanding of seeding and steady-state growth, thickness and width control, and the dendritic structure of the ribbons.

Electrohydrodynamic deposition, in which charged droplets of molten silicon are sprayed onto a low-cost substrate, has been used to coat large substrate areas (10 cm x 15 cm) with fine-grain (~10 um) polycrystalline silicon (24). The rate of deposition is several μm /sec and fairly uniform over the substrate. Purity of the film does not appear to be a problem, but efforts to increase the grain size (e.g., recrystallization) are needed. Large grain sizes, up to 350 μm in ~35 μm thick films, have been obtained by electrodeposition of silicon (25) from molten salt solutions (e.g., $KF:LiF:K_2SiF_6$ or KF:LiF with mg-

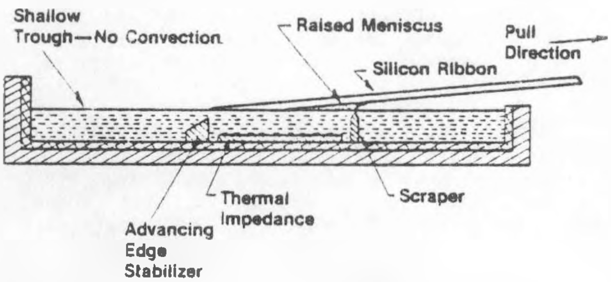

Figure 4: Schematic of Low Angle Silicon Sheet (LASS) Growth (Energy Materials Corporation).

silicon source) on substrates such as Ag, Ta, Ni, graphite, and p-type dendritic-web silicon. Films have been generally n-type and contained metallic impurities in the few ppm range. Efforts to improve the purity of the electrodeposited material are in progress.

Innovative research in the Photovoltaics Research Branch at SERI is impacting future research directions in the polycrystalline silicon program. The Edge-Supported Pulling (ESP) process, described elsewhere in these proceedings (26), is a novel silicon ribbon growth technique which has shown promising results. Ribbons of 5 cm width and 70 μm thickness have been grown at rates of up to 9 cm/min; the current maximum length of 0.2 m is limited by the fixed-stroke puller. Growth has also been demonstrated from mg-silicon feedstock (26). The highest efficiency obtained on seeded ESP ribbon is 13.8% using sg-silicon. Based on these results, SERI solicited proposals during 1980 to transfer the ESP technology to industry and to investigate further its low-cost potential. Negotiations are now underway for subcontract award. Another area actively pursued in-house at SERI is silicon purification by various electrochemical means. Electrowinning of silicon from silica using a molten salt electrolyte (e.g., Na_3AlF_6: LiF) has been demonstrated; a novel approach, using a molten tin cathode, has resulted in mm-size silicon crystallite product (27). Recently, electrorefining of mg-silicon has been shown to result in very pure silicon product (3 to 5 ppm total impurities, including B and P). The novel approach involves an alloy of copper and mg-silicon as the anode, a $LiF:KF:SiF_4$ electrolyte, and various materials (e.g., graphite, single crystal silicon, etc.) for the cathode in the electrolytic cell (27). These efforts are analogous to approaches used in the aluminum industry, and thus hold the potential for low-cost production of solar grade silicon.

Cell R&D

Research efforts in polycrystalline silicon solar cells are concerned mainly with the development of device structures (e.g., MIS, SIS, heterojunction and homojunction) which are compatible with the polycrystalline structure to give high conversion efficiency. The studies involve the development of junction fabrication techniques, the applicability of various low-cost processes to the thin-film materials of interest, analyses of stability and degradation mechanisms, and the development of novel cell fabrication processes and cell structures. The cell R&D efforts are closely related to studies of basic mechanisms in polycrystalline silicon solar cells described in the next section. Here we present the status of cell efficiencies on the various polycrystalline materials, and highlight some recent results related to cell fabrication and stability.

The efficiencies of p/n junction solar cells for the various thin-film materials were discussed, in part, in the previous sections. Figure 5 shows the improvement in efficiency which has been achieved over the past few years. Clearly, there has been

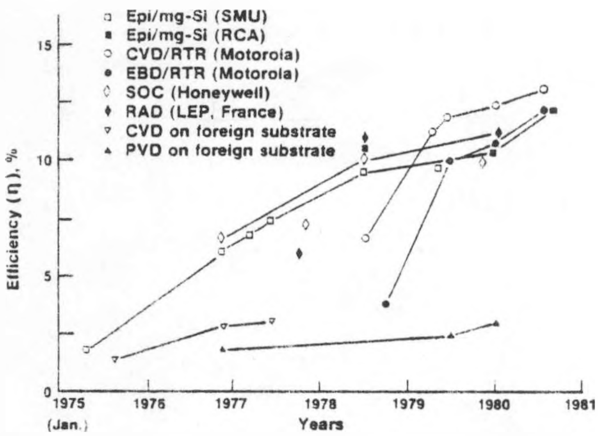

Figure 5: Efficiencies of p/n junction solar cells on thin-film polycrystalline silicon.

very little progress in the efficiencies of films obtained by chemical or physical vapor deposition on foreign substrates. The other curves in the figure show the evolution in cell efficiency for technologies which either constitute or form the basis of the current ED programs. Best reported efficiencies fall in the range from 10.5% (for SOC) to 13.7% (for RTR). Table II summarizes the best reported cell parameters for the various thin-film poly-crystalline silicon materials investigated under the SERI programs. Bulk polycrystalline materials, such as Wacker/Silso and Semix, have been excluded from the table (for p/n junctions). Cell parameters which have been measured by the PV M&E Laboratory at SERI are also listed in the table. It should be noted that, unless otherwise indicated, the samples which were measured correspond to those on which the reported values were obtained.

MIS and SIS-type solar cells on polycrystalline silicon offer the potential of better performance (e.g., enhanced short wavelength response and avoidance of impurity diffusion at grain boundaries by low-temperature processing) and lower cost (e.g., high throughput spray deposition of oxide semiconductors) than p/n junction solar cells. However, to date, the performance advantages of MIS/SIS have not been realized. Additionally, there are serious questions as to the stability of these cell types on polycrystalline silicon and as to the actual cost advantages which may be realized. The paper by Cheek and Mertens (28) in these Proceedings reviews the current status and problems of MIS/SIS silicon solar cells.

The evolution of MIS/SIS cell efficiencies is depicted graphically in Fig. 6. Table II lists the best reported and measured cell parameters for these devices. To date, most of the MIS/SIS devices have been fabricated on single crystal and bulk polycrystalline silicon (e.g., Wacker/Silso) with best efficiencies in the range 13-14% for single crystal and 10-11% for polycrystal. There have been very few investigations of MIS/SIS cells on thin-film materials; some recent results on RTR, SOC and EPI/mg-silicon are shown in Table II. Recently, SERI has initiated a program to assess the viability and compatibility of MIS/SIS devices on thin-film polycrystalline silicon. Preliminary results from this study, in which side-by-side comparisons of p/n and MIS/SIS devices are carried out, appear elsewhere in these Proceedings (29). Other noteworthy advances in this technology include the initiation of a program on inversion layer grating MIS cells at the Joint Center for Graduate Studies (University of Washington) and some recent results by researchers at Penn State University regarding the anomalous rectifying behavior of ITO/Si junctions (30). The inversion layer MIS work is based on some recent reports (31) of high V_{oc} (0.642V) and high active area efficiency (17.6%) achieved with this structure. The Penn State work showed that ion-beam sputtering damages the silicon surface and causes the silicon band edges to bend downwards at the surface. For this reason, ion-beam sputtered ITO leads to an ohmic contact on n-Si and a rectifying barrier on p-Si. Spray-deposited or vacuum-evaporated ITO, on the other hand, is known to yield a rectifying junction on n-Si and an ohmic contact on p-Si. To prove their theory, the researchers demonstrated a rectifying barrier on sprayed-ITO/p-Si by neutral ion-beam sputtering the silicon substrate prior to ITO deposition.

Stability, reproducibility and scalability of MIS/SIS-type devices continue to be unresolved issues (28). Sprayed SIS cells (e.g., SnO_2/n-Si and ITO/n-Si) degrade ~5% in V_{oc} as a result of exposure to UV light (32). Further degradation is thermally activated, and is believed to be associated with the migration of negative oxygen ions across the insulating barrier. Under normal temperatures and operating conditions (i.e., cells forward biased), this latter degradation does not appear to be of concern. Detailed studies of MIS cell fabrication procedures on sequential Wacker/Silso wafers have shown that the reproducibility of MIS cell performance is very sensitive to the nature of the polycrystalline material and to tight control of the processing

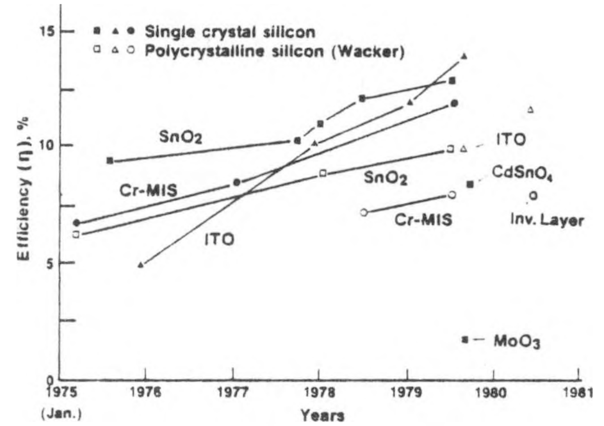

Figure 6: Efficiencies of MIS/SIS junction silicon solar cells.

TABLE II : Solar Cell Parameters under DOE/SERI Polycrystalline Silicon Program.

ORGANIZATION	CELL STRUCTURE	SUBSTRATE MATERIAL	BEST REPORTED VALUES Eff. %	Isc mA/cm²	Voc mV	FF %	AREA cm²	BEST MEASURED VALUES[a] Eff %	Isc mA/cm²	Voc mV	FF %	AREA cm²
Honeywell	p/n	sg-SOC (Dip)	10.54	25.16	573	73.1	5.00					
	p/n	sg-SOC (SCIM)	7.64	20.16	548	69.2	5.00					
	p/n	EPI/mg-SOC	4.11	21.26	433	44.6	11.90					
Motorola	p/n	LB/RTR (CVD)	11.60	26.20	585	75.8	32.00					
	p/n	LB/RTR (HPP)	10.30	23.20	587	75.4	9.80	10.61	25.73	589	70.0	9.80
	p/n	LB/RTR (HPP)	12.00	28.30	582	73.0	4.00					
RCA Lab.	p/n	EPI/mg-HEM	11.89	25.50	582	80.0	2.20	10.01	22.20	574	78.6	2.45
	p/n	EPI/mg-HEM	9.70	21.85	590	75.4	10.20					
Energy Mat'ls	p/n	LASS	11.50	27.10	586	75.0	3.91	10.95	26.97	563	72.0	3.78
SERI/PVR	p/n	ESP	13.80	31.90	585	74.6	4.00					
Poly Solar	p/n	EPI/mg-Si/Graphite	9.10	20.08	570	71.0	35.70	7.57	18.43	575	72.0	35.70
Motorola	p/n	EPI/mg-CZ						9.39	23.67	549	72.3	98.70
Johns Hopkins	p/n	$Si/TiB_2/Alumina$	3.60	18.80	361	53.0	0.02					
Rockwell	p/n	Si/Sapphire	1.60	12.80	348	35.0	0.06					
Exxon[d]	SnO_2/SIS	Single Crystal	13.20	30.40	610	71.3	3.78	12.67	29.60	616	69.4	3.78
	ITO/SIS	Single Crystal	14.10	29.60	625	76.5	3.78	13.36	29.20	625	73.2	3.84
	SnO_2/SIS	Wacker/Silso	10.10	26.60	560	68.0	4.00					
	ITO/SIS	Wacker/Silso	11.20	29.80	557	67.0	1.00	10.54[b]	27.20	550	70.5	1.03
SUNY	Cr-MIS	Single Crystal	13.00	34.00	570	68.0	2.00					
	Cr-MIS	Wacker/Silso	9.50	29.00	540	67.0	2.00					
	Cr-MIS	LB/RTR	7.50	18.00	540	77.0	2.00	6.30	15.90	540	73.8	2.00
	Cr-MIS	EPI/mg-CZ	[illegible]	18.90	560	67.0	2.12	6.79	17.99	515	73.2	2.12
CSU[e]	ITO/SIS	Wacker/Silso	11.50	28.11	522	79.0	11.46	10.24[c]	28.75	521	68.4	11.30
	ITO/SIS	Wacker/Silso	9.50	26.04	522	70.0	18.64	9.19[c]	25.50	514	70.2	18.49
UCCS	AL/MIS	Single Crystal	12.50	29.80	597	69.0	4.00					

(a) Standard AM1 measurements carried out by Photovoltaic Measurements and Evaluations Laboratory at SERI.
(b) Measured cell is different from cell for reported values.
(c) Measured by NASA Lewis Research Center.
(d) SnO_2 and ITO are spray-deposited.
(e) ITO is ion-beam sputter deposited.

NOTE: All solar cells in the table have an anti-reflection coating.

parameters (33). This would tend to question the viability of large area MIS/SIS devices on low-cost polycrystalline silicon materials using low-cost cell fabrication procedures.

Novel cell fabrication techniques which have been investigated under the program include diamond-like carbon AR-coatings (34) and applications of microwave heating (35,36). Rf-plasma deposited i-carbon films from methane and propane have resulted in 35-40% increase in J_{sc} and in cell efficiency over uncoated samples. Low absorption films have also been deposited from butane and ethane; the lower absorbing films generally contain more hydrogen. The i-carbon films are also mechanically resistant, and thus may obviate the need for encapsulating the solar cells. Microwave thermal processing techniques have also shown promising results. The motivation here is to reduce the process cycle times and energy requirements for p/n junction diffusion, back-surface-field (BSF) formation and metallization steps in cell fabrication. To date, the feasibility of simultaneous junction and BSF formation, and metallization sintering has been demonstrated (35,36). The power consumption for the junction diffusion step has been estimated to be one-tenth of that in a conventional diffusion furnace.

Basic Studies

Basic studies of polycrystalline silicon solar cells are concerned with three general areas: (i) the characterization of the structural, compositional, electrical and optical properties and correlations to cell performance; (ii) theoretical modelling of photovoltaic mechanisms in various solar cell structures; and (iii) development of techniques for reducing or eliminating the deleterious effects of grain boundaries. The major objectives of these efforts are to determine the fundamental limitations to polycrystalline silicon cell efficiency, and to provide the appropriate feedback to improve and optimize solar cell efficiencies through improved material and cell fabrication procedures and cell structures. A review by the authors of the influence of grain boundaries on solar cell performance in polycrystalline silicon appears elsewhere in these Proceedings (37). This section describes briefly some of the highlights of the SERI-supported programs in the three areas described above.

In addition to the experimental techniques which are used normally to characterize grain boundaries (e.g., X-rays, SEM, DLTS, EBIC, laser or light spot scan, SIMS, etc.), a number of novel techniques have been developed under the program to examine grain boundary properties. The relative orientation of grains in texture-etched polycrystalline materials can be determined rapidly, and with a resolution of about 15 μm , by a laser diffraction technique (38) which is analogous to the well-known X-ray Laue method. Electrical activity of grain boundaries prior to device fabrication can be observed, for example, by a "liquid crystal" technique (in which the substrate is coated with a liquid crystal and is observed visually as a current is passed laterally along the surface (39)), or by the "transverse photovoltage" technique (in which the voltage generated across ohmic contacts placed on opposite sides of a grain boundary is observed as a laser beam is scanned across the grain boundary region (38)). Electrochemical techniques have been applied to characterize grain boundary states at the polycrystalline silicon/electrolyte interface (40). The use of metal ionic complexes having well-defined energy levels (e.g., $Fe(CN)_6^{4-}$ and

Fe^{+}(EDTA)) in solution has provided some data on the energy states by electronic transport measurements. There have been many correlations of the various grain boundary properties, such as structure and chemistry, to solar cell performance. A predictive model of defect density and type versus cell efficiency in RTR ribbons has been experimentally verified (38).

Theoretical studies have been aimed at developing a fundamental understanding of polycrystalline silicon device mechanisms and performance limitations in terms of physical parameters (e.g., grain size, interface states, etc.). Empirical modelling of cell performance has predicted that grain sizes in excess of 200 μm will be required for >10% efficiency in 100 μm thick polycrystalline silicon (4). Small areal inhomogeneities in junction or transport properties have been predicted to cause severe degradation in p/n junction solar cell performance (41). Further studies of loss mechanisms in p/n junction solar cells have shown that minority carrier recombination at the intersection of grain boundaries with the junction space-charge region is a major cause for low V_{oc} and FF in these devices (42). The predicted dependence of this recombination current (i.e., exp(qV/2kT)) has been experimentally verified. The theoretical models have also resulted in useful engineering guidelines for fabrication of efficient p/n junction cells (42). Modelling of loss mechanisms in MIS solar cells has also led to improved fabrication procedures and efficiency (43).

Passivation of grain boundary effects in polycrystalline silicon has been demonstrated by a number of approaches. Researchers at Sandia Laboratories have shown that H-plasma treatment leads to a reduction in the potential barrier at grain boundaries (44); experiments on SOC solar cells have resulted in reductions in dark current of 3 orders of magnitude (45). Enhanced diffusion of phosphorus dopant at grain boundaries has been observed in n^{+}/p-structured solar cells on Wacker/Silso substrates by a bevel/stain technique. Laser scanning experiments showed that boundaries with phosphorus diffusion spikes were not electrically active (39). Work is also proceeding on the examination of lithium as a passivating agent in polycrystalline silicon. Preliminary data suggest that thermally-diffused lithium acts to increase V_{oc}, probably by decreasing the resistivity of the silicon, but it also appears to result in a decrease in J_{sc} and in the minority carrier diffusion length (46). To date, there has not been a single demonstration of significant improvement in solar cell efficiency with any of the passivation methods tried.

CONCLUSIONS

Although progress in polycrystalline silicon solar cell research has been significant over the past few years, there are a number of outstanding problems and issues which need to be resolved. Addressing these concerns is an important element of not only the current and future SERI programs, but of the worldwide research interest in this area. In the following, we outline some of the more relevant issues which have emerged as a result of past research.

A foremost concern is the low-cost potential of the various ED and R&D technologies. This issue is under continuous assessment, both by SERI and by the subcontractors, using the costing methodologies developed under the JPL/LSA Project (15). Examinations of the scalability and reproducibility of the more promising approaches are key elements of the ED programs. These programs also address the important questions of the stability and reliability of thin-film polycrystalline silicon solar cells and modules.

Mg-silicon feedstock plays a major role in many of the technical approaches. However, there are serious questions as to the variations in purity among the different mg-silicon sources and the reproducibility of the feedstock quality. The cost and effectiveness of various purification techniques (e.g., acid leaching, slagging, etc.) are unresolved issues. Furthermore, there are no clear indications as to the purity requirements for the mg-silicon feedstock either before or after purification. Clearly, these are a function of the intended use of the mg-silicon (e.g., method of substrate preparation, epitaxial growth versus direct diffusion into the substrate, etc.). The unreliability of impurity detection techniques further compounds these problems.

Based on past research experience, the viability of thin-film growth on foreign (i.e., non-epitaxial) substrates by various CVD or PVD processes must be questioned. The quality of the polycrystalline silicon films has been limited both by grain size and by impurities in the films. To date, a viable, low-cost approach to recrystallize small grain-size films has not surfaced. The potentials of controlled nucleation during film growth and of graphoepitaxy approaches (47) have not been fully explored, however. A serious basic issue in all these techniques is the cost and availability of the foreign substrates. This issue also affects some of the non-vapor deposition approaches (e.g., electrodeposition and electrohydrodynamic deposition) currently under investigation.

Questions relating to the viability of MIS and SIS devices on polycrystalline silicon were discussed earlier and are reviewed elsewhere (28). Important elements of future research in this area include the comparative study of MIS/SIS and p/n junction solar cells on potentially low-cost thin-film materials (29), and investigations of the potential of inversion layer MIS cells.

Finally, studies of grain boundary effects and passivation in polycrystalline silicon probably have resulted in more questions than answers to date, as reviewed elsewhere (37). Further work is needed both in basic studies aimed at understanding the mechanisms governing grain boundary electrical activity, and of the methods which can be used to passivate the effects of grain boundaries. The mechanisms and stability of passivation, and the effects of passivation on solar cell efficiency are totally unanswered questions. A weakness in many of the researches is that the material studied is bulk polycrystalline silicon rather than the thin-film materials of interest. A passivated, small grain-size, thin silicon film, on a low-cost substrate such as glass or stainless steel, may yet evolve as the ultimate thin-film technology in polycrystalline silicon.

In summary, thin-film polycrystalline silicon is the most advanced of the DOE/SERI-supported thin-film technologies. With further development, it is expected to become the first advanced material to challenge, in a commercial sense, the single crystal or bulk polycrystalline silicon options which are the mainstream of the current and near-term photovoltaic industry.

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