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High-Efficiency, Thin-Film and Multijunction Solar Cells

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CONTENTS

ABSTRACT

Epitaxial GaAs layers with a reduced dislocation density have been grown on Ge-coated Si substrates by using a new technique involving multiple growth interrupts and thermal cycles. The open circuit voltage of shallow-homojunction solar cells fabricated in these GaAs layers was found to increase with the number of interrupts and thermal cycles. Small-area cells with conversion efficiencies up to 14% (AM1) have been obtained. In addition, monolithic tandem cells composed of a GaAs top cell and a Si bottom cell that are connected by a thin epitaxial Ge layer have been fabricated.

I. INTRODUCTION

Shallow-homojunction $n^+/p/p^+$ GaAs solar cells with conversion efficiencies exceeding 20% (AM1) have been fabricated on GaAs (1) and Ge (2) substrates. With the objective of reducing the cost of such cells, we have been investigating the use of Si as a substrate material. We previously reported (3,4) the fabrication of shallow-homojunction cells with conversion efficiency of 12% (AM1) on Ge-coated p^+ Si substrates. In this paper we report recent advances in GaAs/Ge/Si material preparation that have resulted in an improvement in cell performance. Small-area cells with conversion efficiencies up to 14% have been achieved. We also describe the fabriction of tandem cells composed of a shallow-homojunction GaAs top cell and a Si bottom cell that are connected by a thin epitaxial Ge layer. These are the first monolithic tandem cells in which Si is used as the low bandgap material. The cells exhibit open-circuit voltages of ~1.2 V and good fill factors (0.75-0.8), but the photocurrent density is limited because the difference in bandgap between Si and GaAs is too small. This result suggests the possibility of developing low-cost, high-efficiency monolithic tandem cells that utilize Si for the bottom cell and a material with a higher bandgap than GaAs for the top cell.

II. MATERIAL PREPARATION

To form the GaAs/Ge/Si structures, the Si substrate is first coated with a Ge epilayer deposited by e-beam evaporation, (5) and GaAs epilayers are then grown by chemical vapor deposition (CVD) in an $AsCl_3$-GaAs-H_2

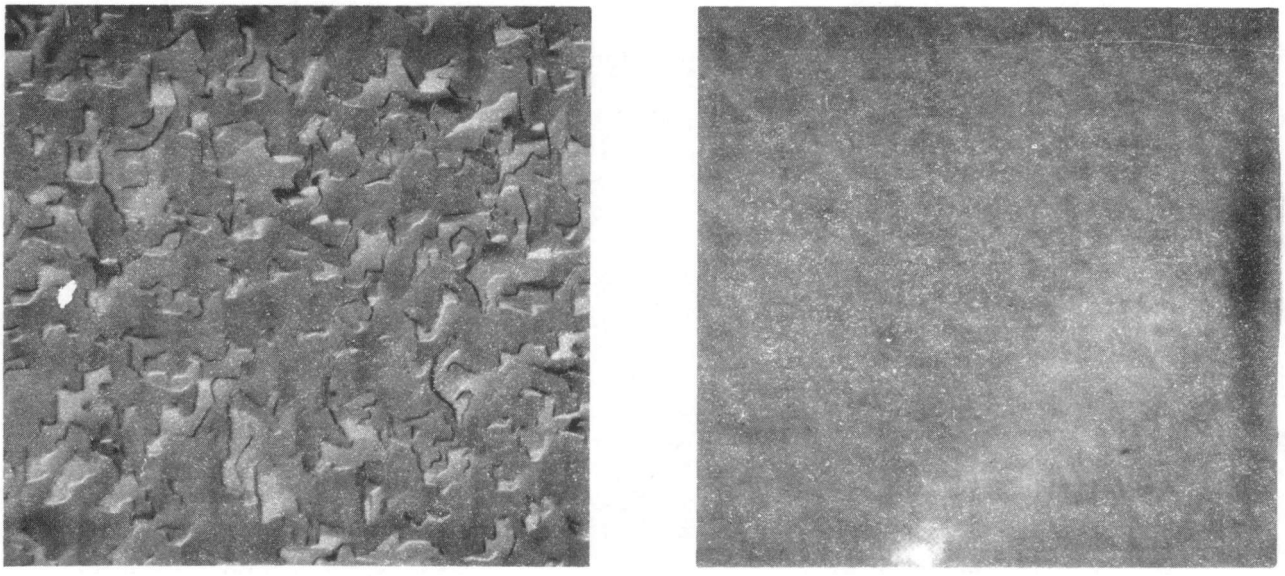

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Figure 1. Optical micrographs showing (a) antiphase domains in GaAs layer grown on Ge-coated Si (100) substrate and (b) domain-free GaAs Layer grown on Ge-coated Si Substrate oriented 2° off (100) toward (011).

system. The surface morphology and crystal quality of the epilayers have been significantly improved by using several new growth procedures.

Surface Morphology

As described previously (3,4) mirror-smooth GaAs epilayers have been grown on Ge-coated Si substrates oriented 2° off (100) toward (011). If (100)-oriented Si substrates are used, the GaAs layers display irregular surface morphology, as shown in Fig. 1(a), due to the formation of antiphase domains. These domains, which have also been observed in layers of GaP on Si and GaAs on Ge (6), result from the symmetry difference between the GaAs and Ge lattices. Nucleation of GaAs on (100) Ge may occur in either of two orientations, (100) or $(\bar{1}00)$, which are not equivalent for GaAs because of its polar nature. GaAs epilayers without domains have been grown on Ge-coated Si substrates oriented 2-3° off (100) toward either (011) or (111). The surface morphology of such a domain-free layer is shown in Fig. 1(b).

Although the surfaces of domain-free GaAs layers are specular over most of their area, both hillocks and pits are observed. These defects originate from small pits, 1-10 μm in diameter, that are present in the underlying Ge layers. These pits can cause faceting of the GaAs layer, which results in hillock formation [Fig. 2(a)], or by exposing the Si substrate they can inhibit GaAs nucleation and therefore produce pits [Fig. 2(b)].

The Ge pits result from spitting of the Ge source during e-beam evaporation. Spitting can be greatly reduced by decreasing the beam power which also reduces the Ge depositon rate. By using a rate of ~100 Å/min the Ge

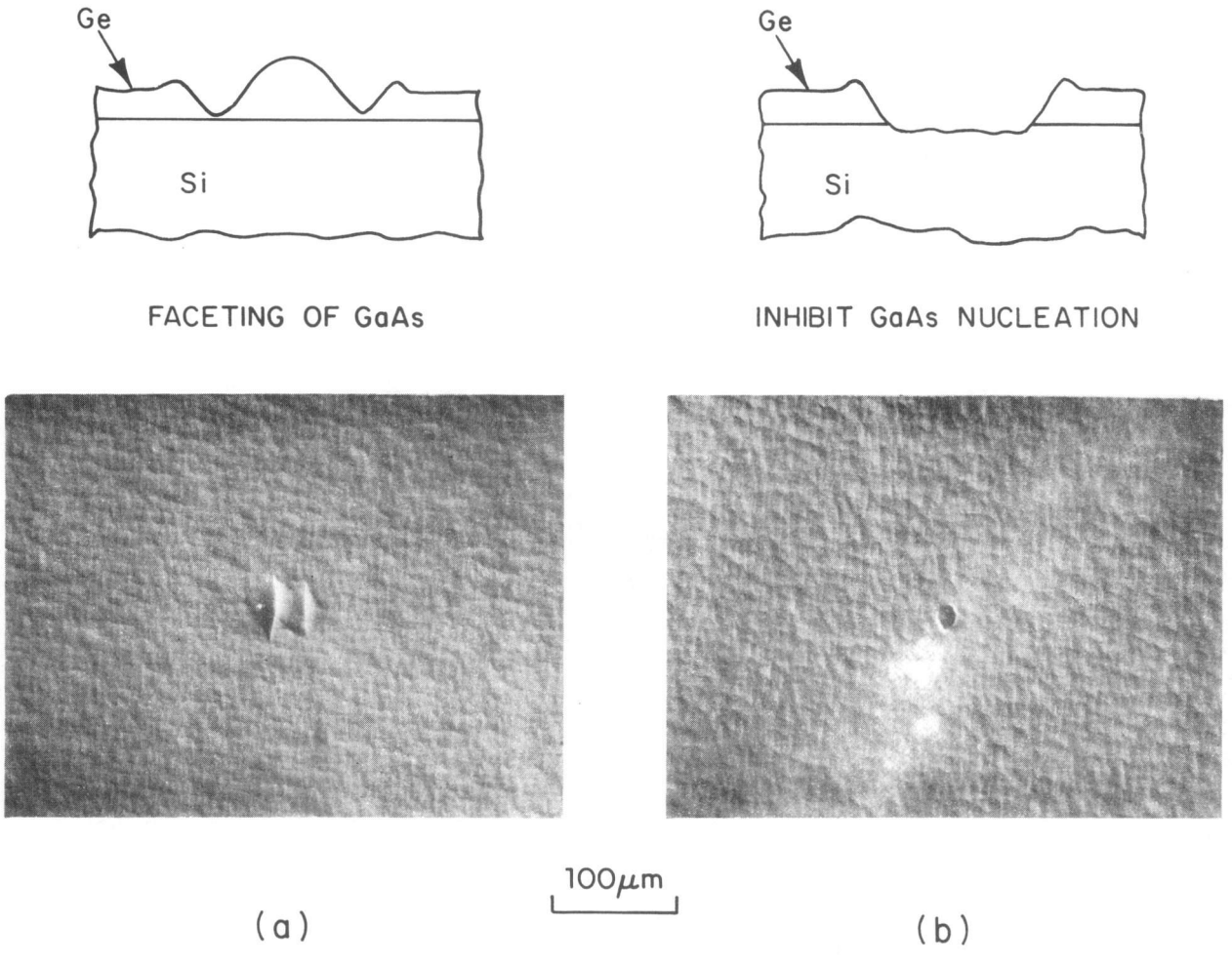

Figure 2. Optical micrographs of GaAs layers grown on Ge/Si substrates that have micropits in the Ge layers. The micropits can (a) produce GaAs faceting, causing hillock formation or (b) inhibit GaAs nucleation, causing pit formation.

surface pit density has been reduced to less than 10 cm^{-2}, compared to ~10^4 cm^{-2} for the rate of ~600 Å/min used in previous experiments (5).

Reducing the Ge pit density has two important benefits for the GaAs layers: (1) reduction of cracks and (2) reduction of autodoping. Since thes layers are under a large tensel stress due to differential thermal contraction between GaAs and Si, they have a tendency to crack. Cracking frequently originates from hillocks, where the material is fragile and the local stress is large. By reducing hillock density, decreasing the pit density in the Ge layers therefore reduces cracking in the GaAs layers.

During the growth of GaAs layers on Ge/Si substrates, they are doped with Si and Ge donors, which compensate the p and p^+ layers of the solar cell structure. If a sufficient area of the Si substrate is exposed by pits in the Ge layer, the donor concentration may reach 10^{17} - 10^{18} cm^{-3}, resulting in carrier lifetime degradation and poor junction characteristics. For the Ge layers with low pit densities autodoping is limited to 2-5 x 10^{16} cm^{-3}, which is low enough for the growth of structures.

Dislocations

The GaAs layers previously grown on Ge/Si substrates contain a high density (> 10^7 cm^{-2}) of dislocations (3,4). These dislocations originate from the Ge epilayers, which contain more than 10^9 cm^{-2} dislocations due to the large lattice mismatch (~4%) between Ge and Si. The high dislocation density in the GaAs results in a high junction leakage current and hence significant reduction of open-circuit voltage of solar cells. We have

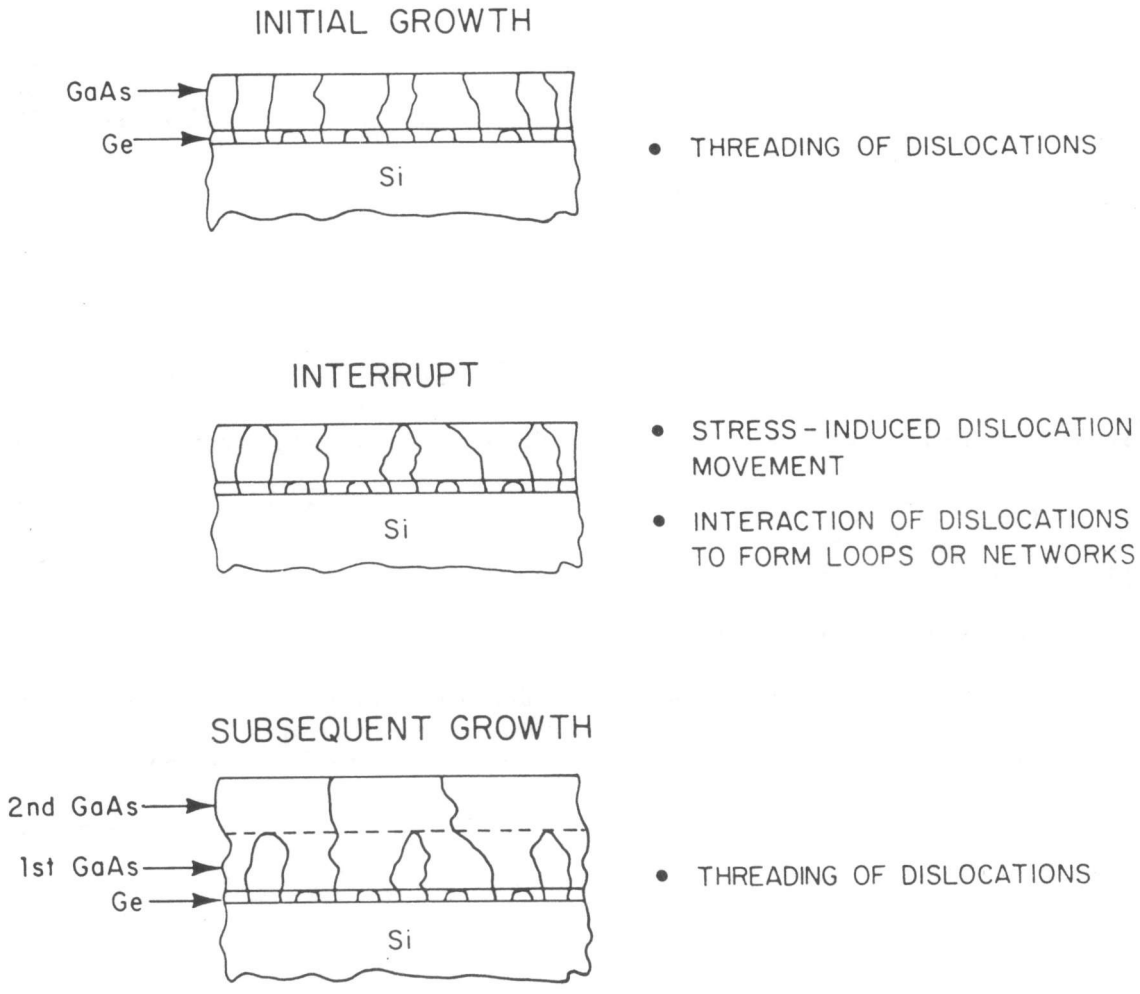

Figure 3. Schematic diagram showing the use of growth interrupt and thermal cycling technique to reduce dislocation density in GaAs layers grown on Ge/Si substrates.

investigated a new growth technique (7) for GaAs that greatly reduces the propagation of dislocations into the junction region and therefore produces a marked increase in open-circuit voltages.

The basic principle of the new growth technique is illustrated in Fig. 3. In the initial GaAs growth many dislocations threading from the Ge layer are incorporated in to the GaAs layer. After the GaAs layer becomes ~0.1 μm thick, growth is interrupted and the sample is cooled from the growth temperature of ~700°C to about room temperature. During cooling, since the GaAs layer is subjected to a large thermal stress the dislocations tend to move and interact with each other to form loops and networks. When growth is resumed, the loops and networks reduce the dislocations available for threading into the next GaAs layer. If the sequence of interrupted growth and thermal cycling is repeated, the process of dislocation interaction can lead to a progressively lower dislocation density in the successive GaAs layers. Figure 4 is a cross-section micrograph, obtained by transmission electron microscopy (TEM), of a GaAs sample deposited on a Ge/Si substrate with ten growth interrupts and thermal cycles. The dislocation density in the final GaAs layer is estimated to be one to two orders of magnitude lower than this density in samples grown without interruption (see Fig. 5).

In an number of runs for preparing GaAs $n^+/p/p^+$ solar cell structures on Ge/Si substrates, we have grown the p^+ region by the new technique, using up to 20 growth interrupts and thermal cycles per run. In any one run, the individual p^+ layers were of the same thickness, which was chosen to make

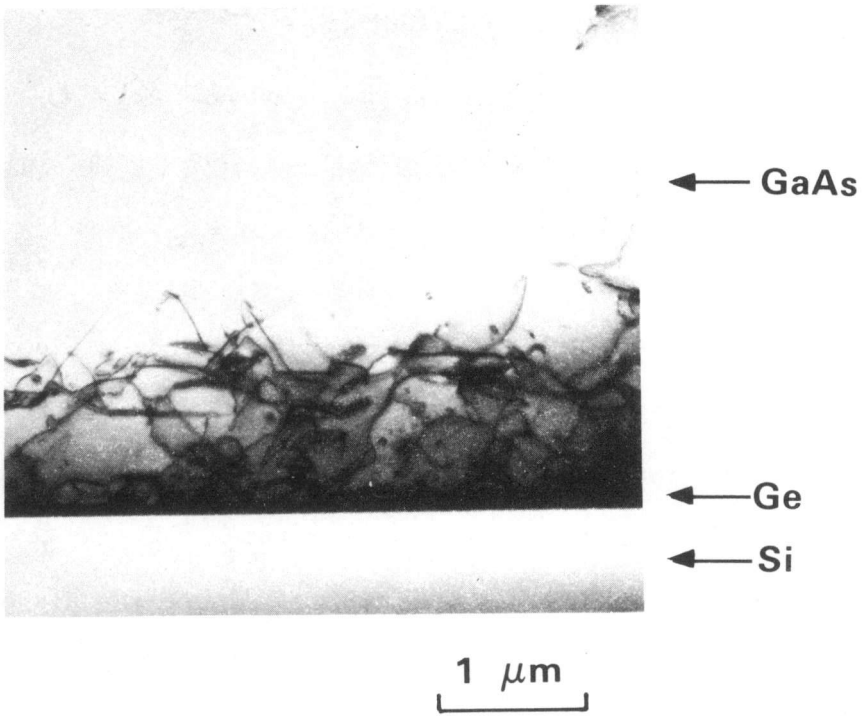

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Figure 4. Cross-section TEM micrograph of a GaAs layer grown on Ge/Si substrate with 10 growth interrupts and thermal cycles.

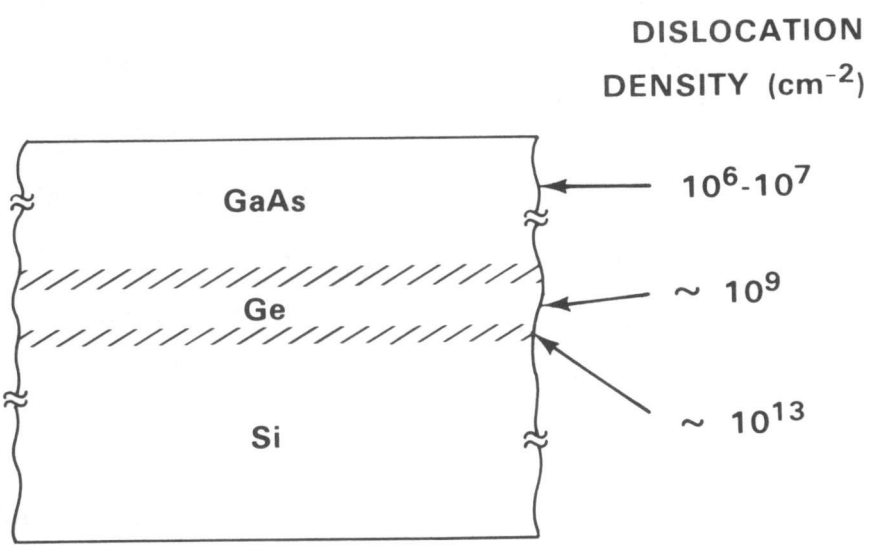

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Figure 5. Schematic of GaAs/Ge/Si cross section summarizing the dislocation densities measured by transmission electron microscopy.

the total thickness of the p^+ layer region about 4 μm. The p and n^+ layers, which were grown without interruption, were 4.0 and 0.15 μm thick, respectively.

III. SOLAR CELL CHARACTERISTICS

Small-area solar cells 0.6 mm in diameter have been fabricated from the GaAs structures by procedures similar to those used for cells on bulk single-crystal GaAs on Ge substrates (1,2). For cells without an antireflection (AR) coating, the short-circuit current density J_{sc} is ~14 mA/cm^2. Figure 6 shows the open-circuit voltage V_{oc} of these cells as a function of the number of p^+ growth interrupts. Each data point represents an average of values measured for more than 50 devices, and the error bars indicate the range of measured values. The value of V_{oc} increases from ~0.67 V with no interrupt to ~0.75 V with 20 interrupts. After the n^+ layer is thinned to 500-600 Å by anodization and stripping and the cells are AR coated by anodization, J_{sc} increases to ~24 mA/cm^2, close to that of single-crystal GaAs cells, and the V_{oc} values each increase by ~0.05 V. Figure 7 shows the I-V characteristics under AM1, one-sun illumination of a typical AR-coated cell that was fabricated from a GaAs structure with 10 p^+ growth interrupts. The cell has V_{oc} ~0.79 V, $J_{sc} \simeq$ 24 mA/cm^2 and fill factor of ff = 0.75, giving an efficiency of ~14%.

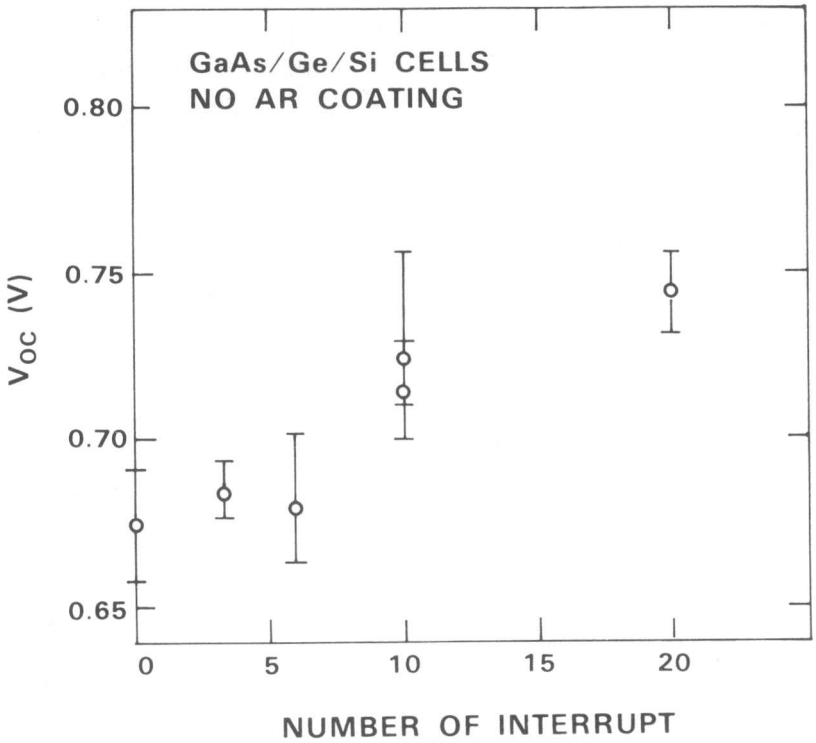

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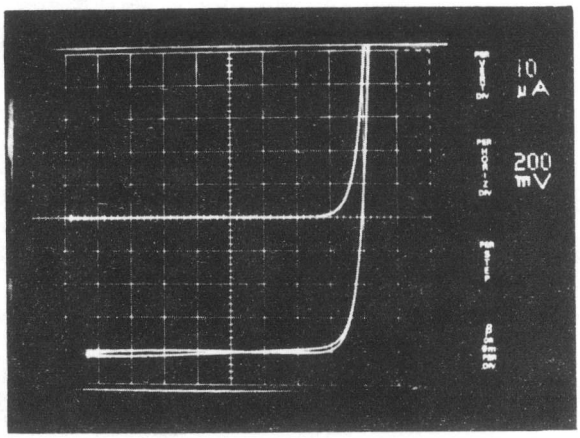
Figure 6. Open-circuit voltage V_{OC} as a function of number of GaAs growth interrupts for solar cell fabricated in GaAs layers grown on Ge/Si substrates.



$V_{oc} = 0.79\ V$

$ff = 0.75$

$J_{sc} = 24.5\ mA/cm^2$

$\eta \sim 14.5\ \%$

AM1

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Figure 7. I-V characteristic (at AM1) of small-area GaAs/Ge/Si solar cell fabricated in GaAs layer with 10 growth interrupts.

IV. OTHER METHODS FOR REDUCING DISLOCATIONS IN GaAs

An addition to the growth interrupt and thermal cycling technique, we have investigated two other possible methods for reducing the dislocation density in GaAs layers grown on Ge/Si substrates: (1) multiple heterostructure growth and (2) lateral epitaxial overgrowth.

The possiblity of using multiple heterostructure to suppress dislocation propagation was suggested by the multilayer studies of Matthews and Blakeslee (8). In an initial investigation of the distribution of dislocations in such a structure, we have prepared the sample shown schematically in Fig. 8, which consists of the Ge/Si substrate, a 1-μm-thick GaAs layer, a 0.3-μm Ge layer, and a 2-μm GaAs top layer. The GaAs and Ge layers were deposited in separate systems, so that some contamination may be present at the interfaces between these layers. As shown in the cross-section TEM micrograph of Fig. 8, the first GaAs layer contains the expected high density of dislocations. Some of these dislocations terminate or bend over at the interface between this GaAs layer and the following Ge layer. Consequently, this Ge layer and the top GaAs layer have much lower dislocation counts. The dislocation density in the top GaAs layer is estimated to be $\sim 10^6$ cm^{-2}. The dislocation density should be further reduced by growth of additional Ge and GaAs layers.

Another promising method for reducing dislocation densities in GaAs layers on Ge/Si substrates is the lateral epitaxial overgrowth technique. The overgrowth technique was developed for growth on reusable substrates by means of the CLEFT (cleavage of lateral epitaxial films for transfer)

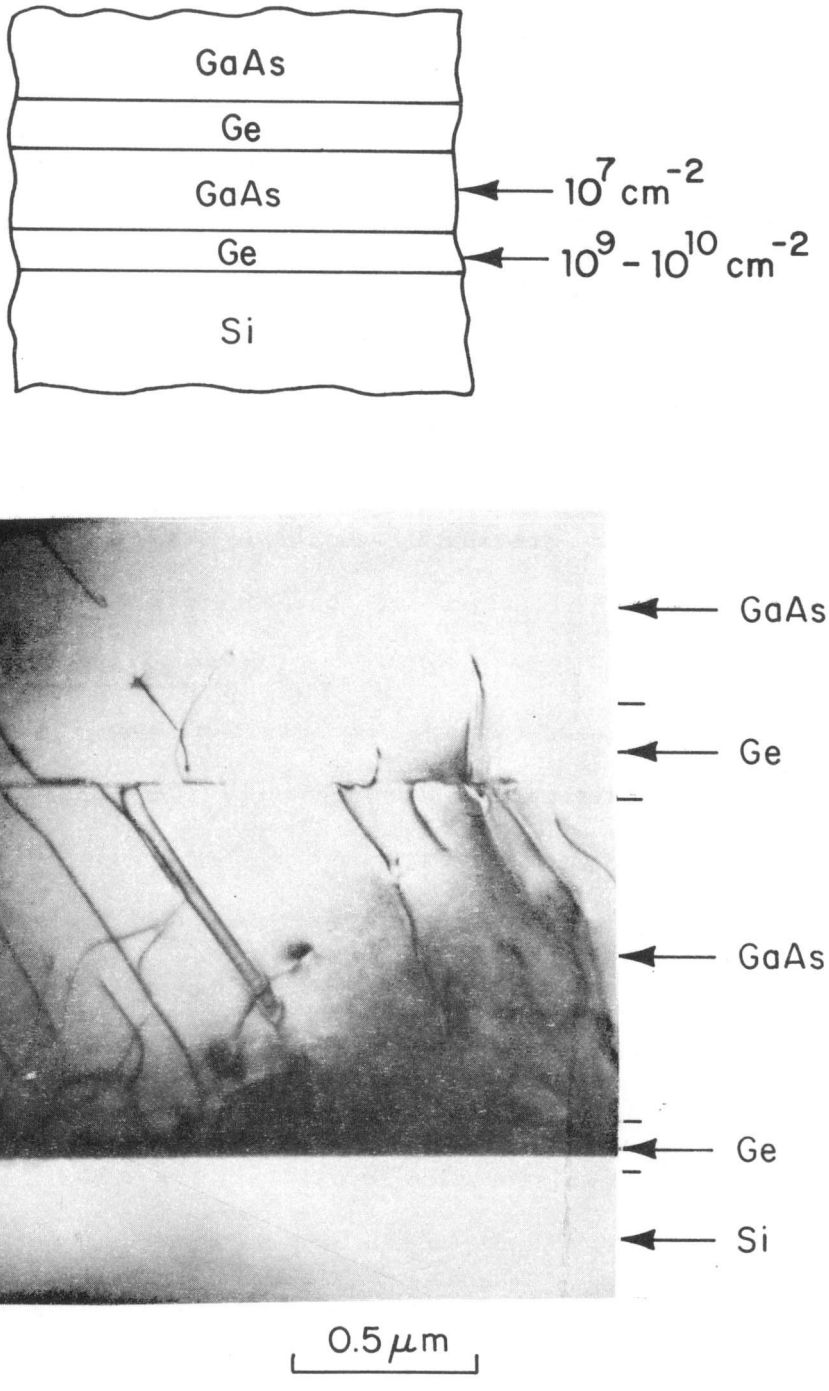

Figure 8. Schematic diagram and cross-section TEM micrograph showing the use of alternating GaAs and Ge layers to reduce dislocation propagation.

process (9). The principle of this technique is illustrated by the top portion of Fig. 9, which is a schematic cross-sectional diagram of a sample at an intermediate stage of overgrowth. After an initial GaAs layer is grown on the Ge/Si substrate, this layer is masked with a film of SiO_2, narrow stripe openings are etched in the SiO_2 film, and GaAs is then grown under conditions such that nucleation takes place only on the regions of the first layer exposed by the openings. The epitaxial GaAs deposits formed on these exposed regions seed lateral growth over the SiO_2. If this growth is allowed to proceed for a sufficient time, the growth fronts from adjacent openings merge to form a continuous GaAs layer with the same orientation as the Si substrate. By using this technique we have grown (10) GaAs layers with dislocation densities of less than 10^4 cm^{-2}. Figure 9 is a cross-section TEM micrograph showing a typical laterally overgrown region. In this region, there are no dislocation in the overgrown GaAs layer, although as usual the layer grown directly on the Ge/Si substrate contains a high density of dislocations. In fact, the only dislocations that we have observed in the overgrown layers are a small numer that originate within the stripe openings but quickly bend over and do not propagate. Initial experiments (10) indicate that the electrical properites of the laterally overgrown layers are comparable to those of conventional GaAs epilaye s grown on single-crystal GaAs substrates.

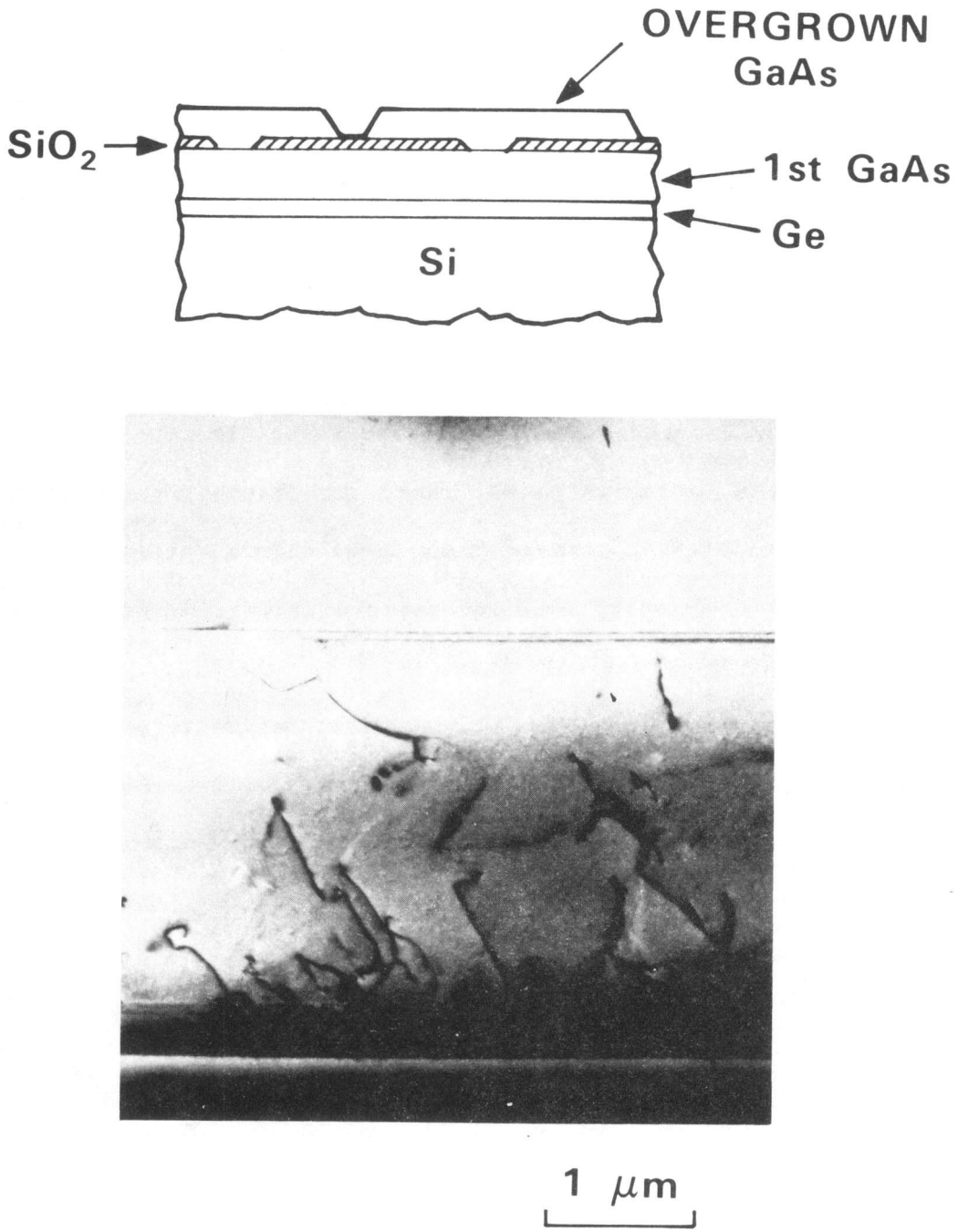

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Figure 9. Schematic diagram and cross-section TEM micrograph showing the lateral overgrowth technique used to produce low-dislocation-density GaAs layers.

V. GaAs-Si MONOLITHIC TANDEM CELLS

In a few experiments, GaAs $n^+/p/p^+$ structures were grown with 10 p^+ growth interrupts on Ge-coated Si substrates that were lightly doped (0.1 - 1 Ω cm p-type). An n-p junction as formed in the vicinity of the Ge/Si interface as a result of As diffusion through the Ge layer during GaAs growth. The presence of this junction is indicated by the photovoltaic response shown at the lower left of Fig. 10, which was obtained for a cell that was fabricated in the Ge/Si substrate after etching away the GaAs layers. A V_{oc} value of 0.45 - 0.5 V is observed. The I-V characteristics of a typical small-area (0.6 mm in diameter) GaAs-Si monolithic tandem cell are shown at the lower right of Fig. 10. Although the tandem cells have relatively low values of J_{sc} (~7 mA/cm^2, without AR coating), they exhibit a V_{oc} of 1.2 V and good fill factors (0.75-0.8), indicating that the Ge layer forms a low-resistance interconnect between the p^+-GaAs and n^+-Si.

Nevertheless, the important result of these experiments is that the Ge layer serves not only as a barrier against the propagation of misfit dislocations but also as a low-resistance interconnect between the GaAs and Si cells. We believe that the defects in the Ge layer produce high leakage currents between the heterojunctions formed at the GaAs-Ge and Ge-Si interfaces, so that no tunnel junction is needed. This is an important observation since there are two traditional approaches in forming interconnects in monolithic tandem cells. One is to use heavily doped tunnel junctions, and the other is to use superlattice structures. The use

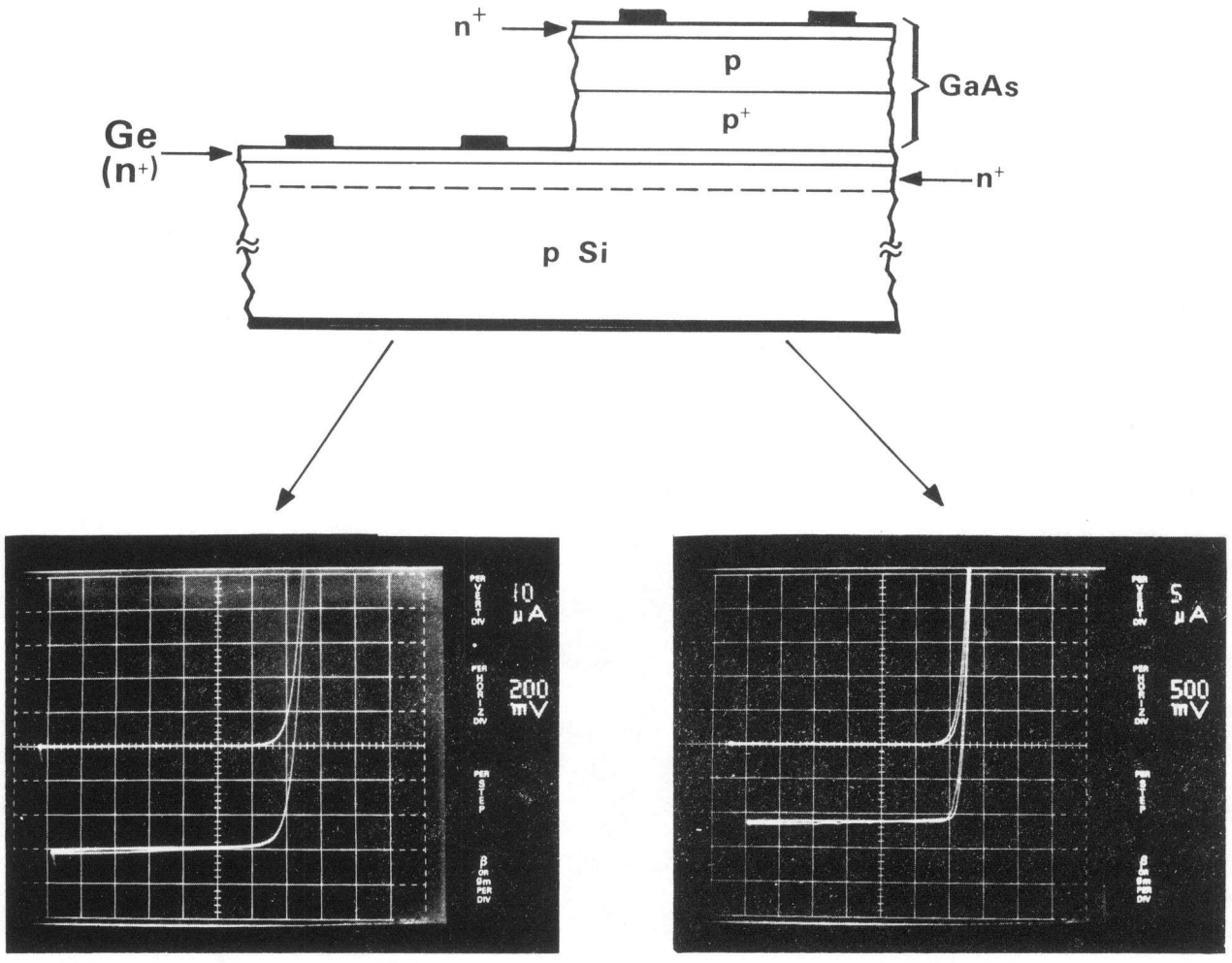

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Figure 10. Schematic cell structure and I-V characteristics for monolithic GaAs-Si tandem cells.

of defect junctions such as those beteen GaAs-Ge and Ge-Si represents a simple alternative technique (see Fig. 11).

The current density of the tandem cells is limited by the photocurrent generated in the bottom Si cell. In the GaAs-Si monolithic structure this photocurrent is small because only a small fraction of the solar spectrum lies between the bandgaps of GaAs and Si. At AM1, Si can only generate about 11 mA/cm^2 after the solar spectrum is filtered by GaAs. Therefore the maximum theoretical combined efficiency of the monolithic structure is only about 15% at AM1 (11). However, we propose a novel design that would greatly increase the photocurrent. The key idea is to etch away part of the GaAs cell, exposing the Si cell underneath. The photocurrent in the Si cell will disproportionately increase, and the combined efficiency will greatly increase. We have calculated that if 32% of the area of the GaAs cell is removed, the photocurrents generated in the GaAs and Si cells will be equal, and the theoretical combined efficiency will be increased to nearly 30% at AM1.

For two-terminal monolithic tandem structures composed of a bottom Si cell (E_g = 1.1 eV) and top cell with energy gap E_{g1}, Fig. 12 shows the increase in theoretical combined efficiency at AM1 and 27°C that can be achieved by removing a fraction r of the area of the top cell. The lower curve gives the efficiency as a function of E_{g1} for r = 0, while the upper curve gives the efficiency obtained for the optimal value of r, the value for which the photocurrents of the two cells are equal. The difference is greatest at the lowest values of E_{g1}, where the optimal value of r is

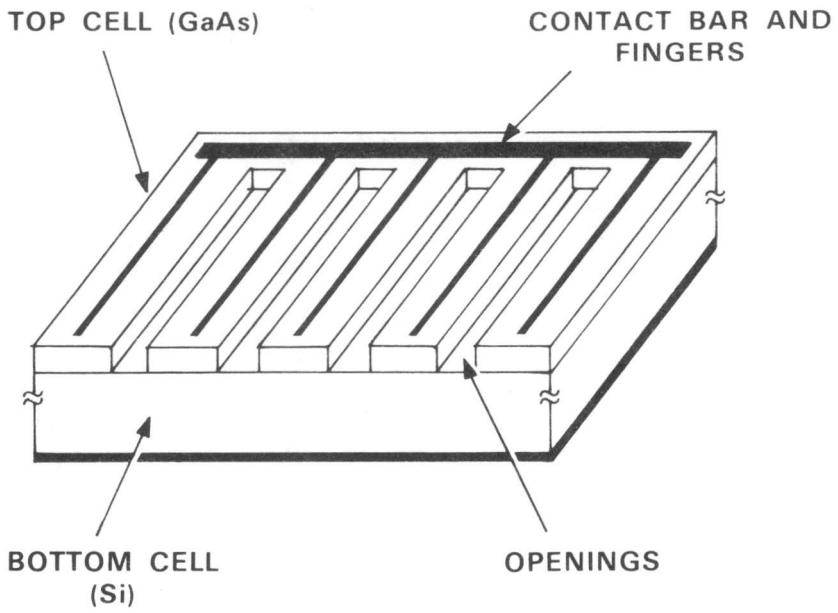

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Figure 11. Schematic diagam showing a GaAs-Si monolithic tandem cell with openings etched in the GaAs layers.

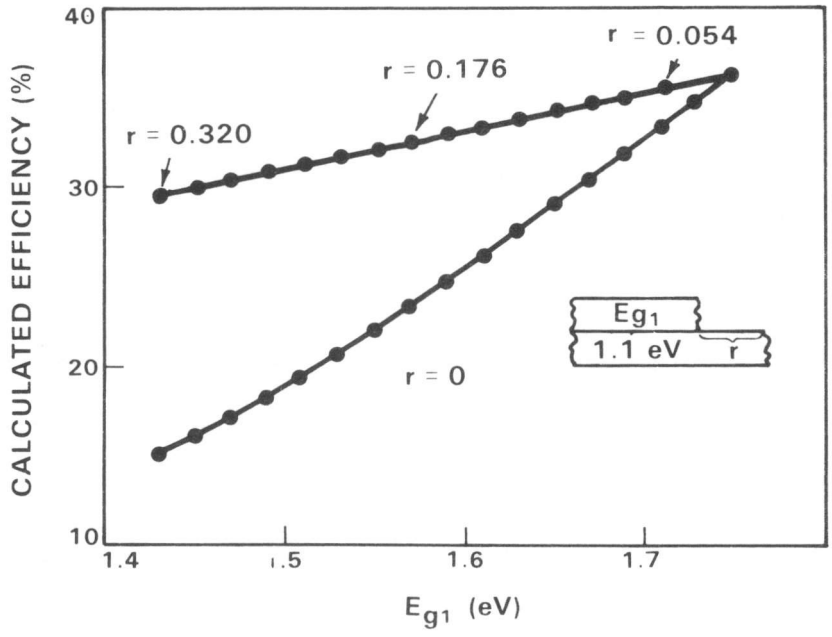

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Figure 12. Plots of calculated AMI conversion efficiencies of a two-cell, two terminal tandem cell as a function of the top-cell bandgap energy. The bottom-cell bandgap energy is 1.1 eV. By removing optimal top-cell areas, the conversion efficiencies would be greatly increased.

greatest. The two curves meet at E_{g1} = 1.75 eV, the optimum value of E_{g1} given by the calculations discussed above, since all those calculations assume r = 0.

VI. CONCLUSION

We have used several techniques to improve the quality of GaAs epilayers grown on Ge-coated Si substrates. Much better surface morphology and lower autodoping are achieved by decreasing the density of pits in the Ge coating layer. The growth interrupt and thermal cycling technique causes the dislocations in the initial GaAs layer to form loops and networks that reduce the propagation of dislocations into the junction region. Methods utilizing multiple heterostructures and lateral overgrowth are also quite effective in reducing the dislocation density of the GaAs layers. Small-area solar cells with conversion efficiency of ~14% (AM1) have been obtained by using the growth interupt and thermal cycling technique. Further improvment in cell performance should be achieved by further reducing the GaAs dislocation density. We have fabricated monolithic tandem cells that are composed of a GaAs top cell and a Si bottom cell connected by a thin epitaxial Ge layer. The characteristics of these cells justify further development of monolithic multiple junction cells using Si as the low bandgap material.

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