DOE/JPL/954898-3

PHASE 2, AUTOMATED ARRAY ASSEMBLY, TASK IV
LOW COST SILICON SOLAR ARRAY PROJECT

Quarterly Report No. 3

July 1978

Work Performed Under Contract No. NAS-7-100-954898

Lockheed Missiles and Space Company, Incorporated
Sunnyvale, California

U.S. Department of Energy

Solar Energy

DISCLAIMER

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Prepared By

LOCKHEED MISSILES & SPACE COMPANY, INC.
1111 Lockheed Way
Sunnyvale, CA 94086

The JPL Low-Cost Silicon Solar Array Project is sponsored by the U.S. Department of Energy and forms part of the Solar Photovoltaic Conversion Program to initiate a major effort toward the development of low-cost solar arrays. This work was performed for the Jet Propulsion Laboratory California Institute of Technology by agreement between NASA and DoE.

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FOREWORD

The results described herein represent the work performed from May 1, 1978 to July 31, 1978 by the Manufacturing Research Organization of Lockheed Missiles & Space Company, Inc. in Sunnyvale, California. The project team, headed by Mike Lopez, is staffed with the following key personnel:

Dean Housholder, Semiconductor and Device Technology

Jerry Katzeff, Laser Technology (Annealing)

Bob Casey, Automation Processes

Harold Weinstein, R&D Staff, Photovoltaic Devices, International Rectifier Corporation

Other principal contributors include John Knudson, Ion Implantation; and Cheryl Bostwick, Screen Printing of Contacts.

The JPL Contract Technical Manager is B. D. Gallagher.

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SECTION 1

SUMMARY

Functional 3-inch diameter reference cells were fabricated using conventional processes consisting of: $POCL_3$ diffusion, electroless nickel plating, solder dipping, and evaporated SiO AR coating. Both flash and texture-etched surface wafers were used. The flash-etched cells yielded output efficiencies of 10.3%, whereas the texture-etched cells were considerably lower.

Other flash and texture-etched cells were processed by ^{31}P ion implantation 25 KeV and 3×10^{15} ions/cm^2, thermal annealing, and electroless nickel plating, resulting in 7% AM1 efficiencies. Problems were experienced in the nickel plating process which contributed to poor ohmic contact adherence and the resulting low efficiencies.

Laser annealing was performed by Quantronix with an Nd:YAG laser on our texture-etched, flash-etched, and polished ion implanted wafers. A programmed X-Y positioning stage was used for precise traversing across the wafer surface. Best results of 7.3% AM1 efficiencies were attained on .5 x .5 cm size cells with polished surfaces. These cells had evaporated Ti/Ag contacts but not sintered nor AR coated. I_{sc} of these small cells was 5 ma. This represents a 27 ma/cm^2 output based on active area only, and compares with 32 ma/cm^2 for a conventionally processed cell of 11% AM1 efficiency.

A cost analysis was prepared which reflects potential cost savings of laser annealing over thermal annealing in excess of $35 million. This savings is due to a projected cell efficiency improvement of 2%, resulting in reduced quantities of cells for the 500 megawatt capability.

Spraying of tantalum solutions was performed on 2 x 4 cm space cells using the Zicon Autocoater. Cells were electrically tested at the outset in the "as received" condition with SiO AR coating. This was followed by stripping of the SiO, retesting, Ta solution sprayed and again retested. After spray coated,

I_{sc} output comparisons from bare to coated, exhibited 15% to 31% increased outputs. Coating thickness uniformity on these cells ranged from 1100Å to 1240Å, as determined with a Gaertner Ellipsometer.

SECTION 2

INTRODUCTION

This is the 3rd Quarterly Report on a process development contract to verify the technological readiness of a selected process sequence from the "as-sawn" Czochralski grown silicon wafers to the module assembly. The contract, started November 1, 1977, is of a 12 month duration. Our selected process sequence consists of working with 3-inch diameter cells, evaluating the following steps: texturizing, ion implanting, laser annealing, screen printing contacts, sprayed-on AR coating and module assembly.

The previous two quarters' work addressed technology and economic evaluations and critical reviews. Process verifications got underway resulting in the fabrication of cells using steps of our selected process sequence including texture etching and ion implantation. Laser annealing of ion implanted cells was performed on small wafer areas yielding good surface activation. Screen printing of ohmic contacts was also performed resulting in good line definition, but poor cell response due to a high series resistance, indicative of poor contacting. Baseline functional cells were fabricated which were texture etched, ion implanted, thermal annealed, electroless nickel plated and solder coated. These cells exhibited 9% AM1 efficiencies. Also, during this period a high volume production process for texture etching was conceptualized for the 1986 objective.

This report discusses the work performed on additional baseline reference cells, as well as process verifications of our selected sequence including ion implantation, laser annealing, screen printing of ohmic contacts and spray-on AR coating. High volume production concepts are also addressed for the balance of our process sequence.

SECTION 3

TECHNICAL DISCUSSION

3.1 PROCESS VERIFICATION

3.1.1 Functional Reference Cells

Two cell runs were processed through the fabrication cycle by International Rectifier yielding cells with 10% AM1 efficiencies. The process sequence for the two runs consisted of:

Starting Material - As-sawn, 3 in. diameter Cz Silicon, 1:0:0

Run No. 117	Run No. 118
Flash-Etched Surface Prep	Texture-Etched (Flash-Etch Pretreat)
$POCL_3$ Diffused	$POCL_3$ Diffused
Sand Blast Back	Sand Blast Back
Electroless Ni Plate (front & back)	Electroless Ni Plate (front & back)
Solder Dip	Solder Dip
SiO Evaporation (AR)	SiO Evaporation (AR)
Qty. Processed: 6	Qty. Processed: 4

One cell from both runs was hand spray-coated using the Allied Chemical Ta solution instead of SiO evaporation. The flash-etched (from Run 117) sprayed cell resulted in an output efficiency of 10.3% which is consistent with those SiO evaporated. The texture-etched sprayed cell was considerably lower than the respective SiO coated cells. Figures 1 through 4 show the I-V curves of cell Run Nos. 117 and 118, as well as the 3-inch diameter standard cell.

3.1.2 Ion Implantation

Cells were ion implanted by International Rectifier and completed through the fabrication cycle by thermal annealing, electroless nickel plating ohmic con-

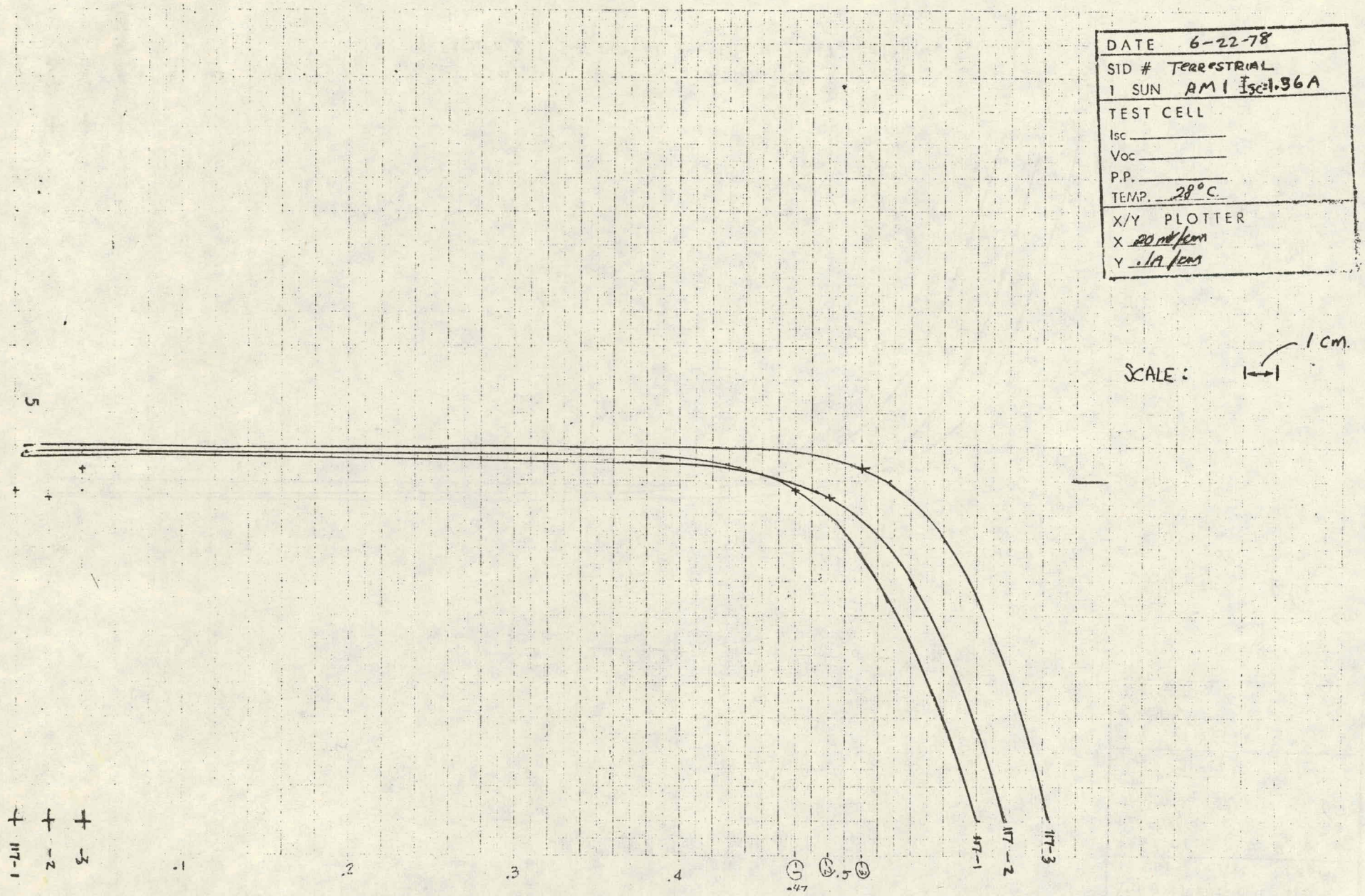


Figure 1. I-V Output for Run No. 117, Cells 1, 2, and 3

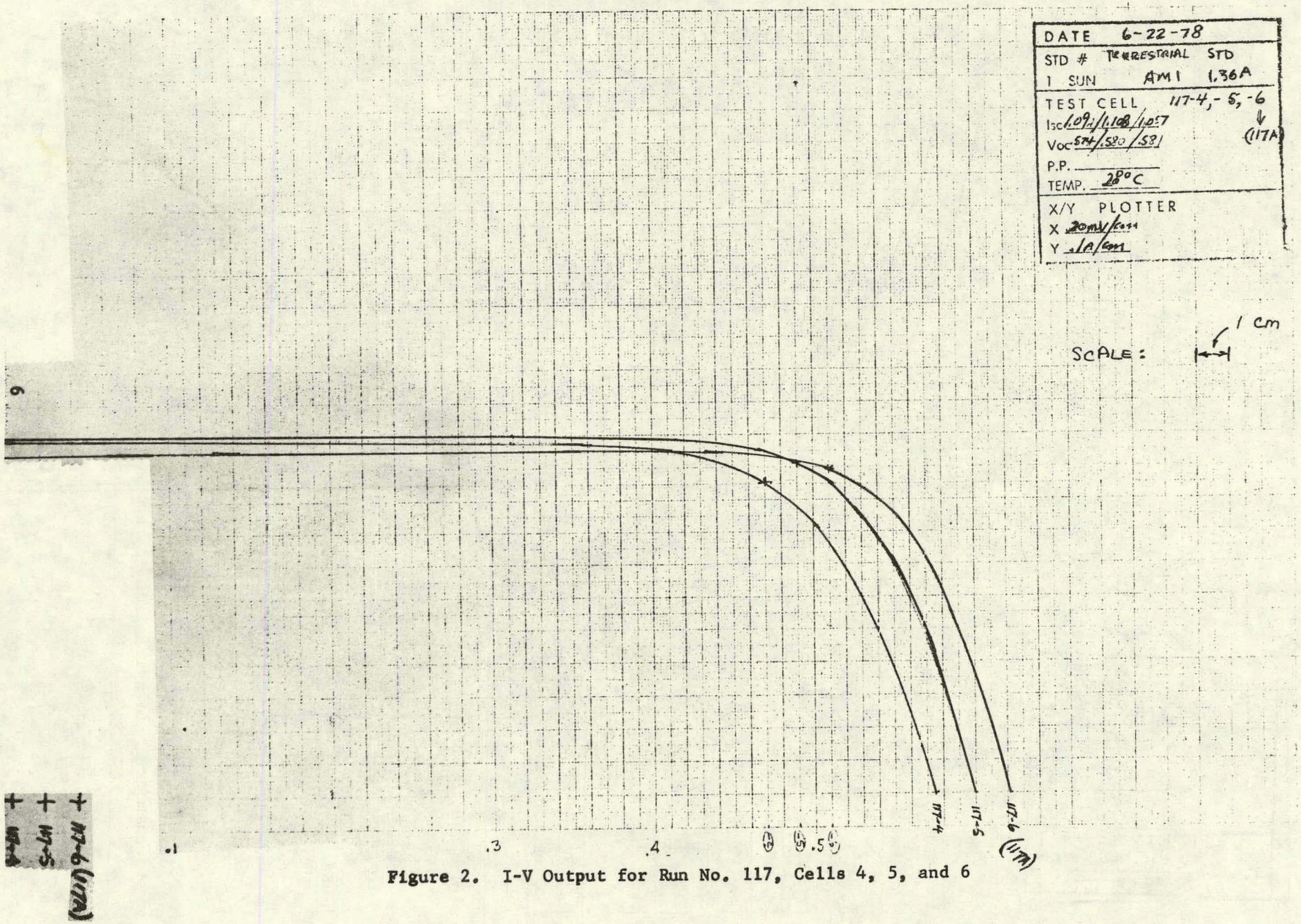


Figure 2. I-V Output for Run No. 117, Cells 4, 5, and 6

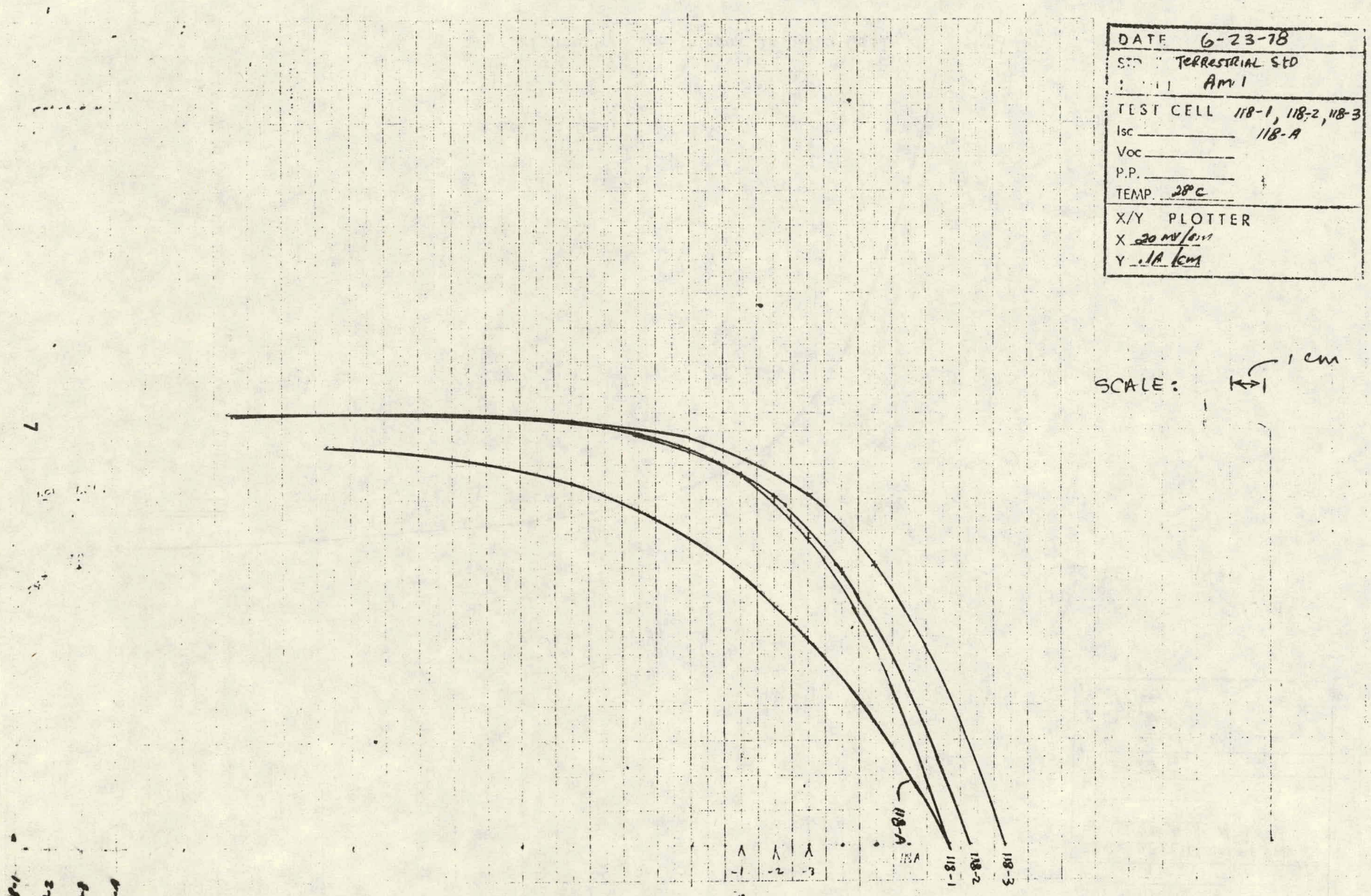


Figure 3. I-V Output for Run No. 118, Cells 1, 2, 3, and A

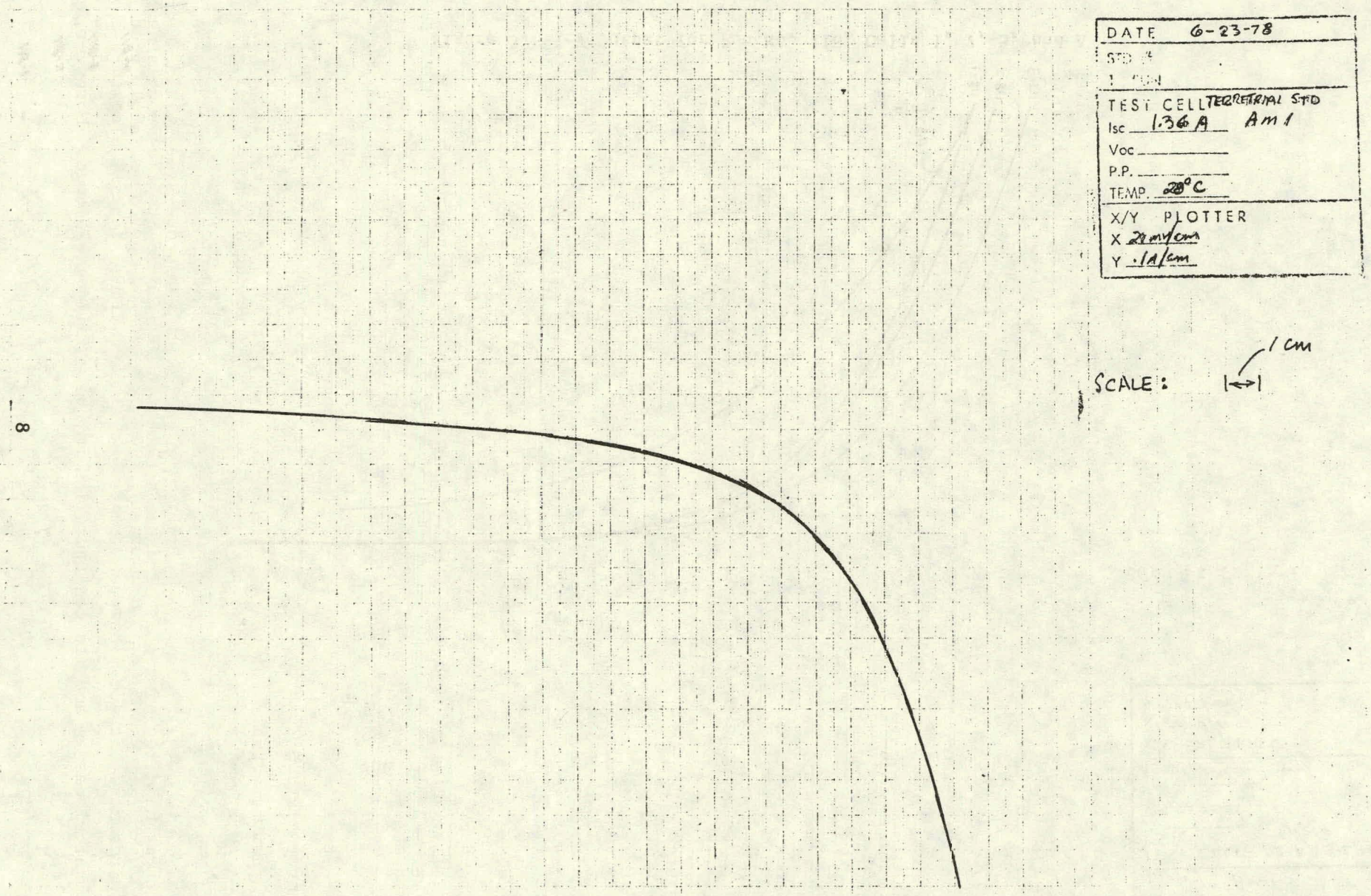


Figure 4. I-V Output for STD Cell

tacts, and evaporating SiO AR coatings. Both flash and texture-etched wafers were used. Electrical outputs were in the 7% AM1 efficiency range. It is believed that the low output is attributed to the nickel plated contact where a problem of poor adhesion was reported by production personnel. Ion implanting with ^{31}P was at 25 KeV and 3×10^{15} ions/cm^2.

Other cell runs have been started through the ion implantation process and will be closely followed through the process steps.

3.1.3 Laser Annealing

Contacts were made with Quantronix Corporation, Smithtown, New York, and Quantel International Corporation, Sunnyvale, California, as part of a survey of manufacturers whose lasers appeared to be applicable to annealing of silicon wafers.

To evaluate the manufacturer's product line, a number of wafers were shipped to Quantronix for performance of the required annealing work. The shipment contained one flash-etched, two texture-etched, and one polished wafer. The wafers were implanted at 25 KeV with a fluence level of 1×10^{15} ions/cm^2, 3×10^{15} ions/cm^2, 1×10^{15} ions/cm^2, and 2.5×10^{15} ions/cm^2, respectively. These wafers were annealed with a Model 116 Nd:YAG laser. After annealing, the wafers were subjected to electrical (four-point probe) evaluation. Good readings were obtained on a number of subject samples. Table I summarizes the results of this evaluation.

At the conclusion of electrical testing, the wafers were processed into 1 x 1 cm cells for the flash and texture-etched samples and into .5 x .5 cm cells for the polished specimen. Electrical outputs of subject cells were low with the exception of the polished cell which yielded a 7.3% AM1 efficiency, Figure 5. The cell was neither AR coated nor sintered, consequently, increase in the efficiency is anticipated following these operations. In terms of I_{sc} per unit area, the laser annealed cells demonstrated fairly good

TABLE I

SUMMARY OF LASER ANNEALING WORK AT QUANTRONIX

Run No./ Surface	Implantation Parameters	Energy Density (J/cm^2)	Pulse Duration/ Pulse Repetition Rate	Annealed Spot Diameter (Mils)	Center-Center Spacing (X&Y Axes) Mils	V/I	
						Front	Back
109/Flash Etched	25 KeV $1x10^{15}/cm^2$	4.9 3.9	140 nsec/ 4 kHz	2.9 2.4	1.0 1.0	14.8-15.5	25
114/Texture Etched	25 KeV $3x10^{15}/cm^2$	2.9 2.4		4.3 3.5	2.0 2.0	9.1-9.5 Inc. Annealing	19.6
105/Texture Etched	25 KeV $1x10^{15}/cm^2$	2.9 2.4		3.9 3.4	2.0 2.0	18.1-19.7 Unannealed	23
102/Polished	25 KeV $2.5x10^{15}/cm^2$	2.9 3.4		3.2 4.0	1.5 1.5	9.0 8.4	23

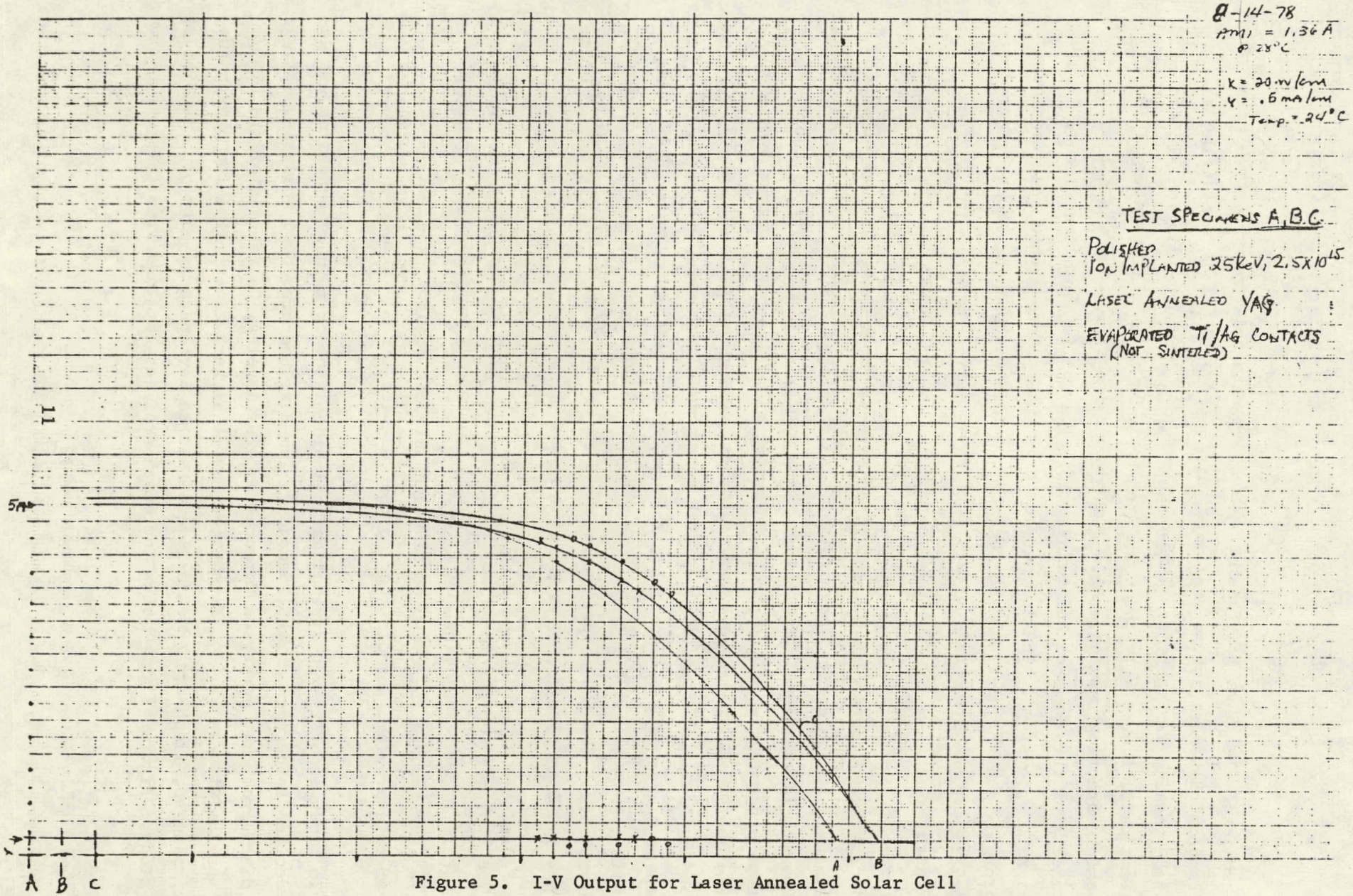


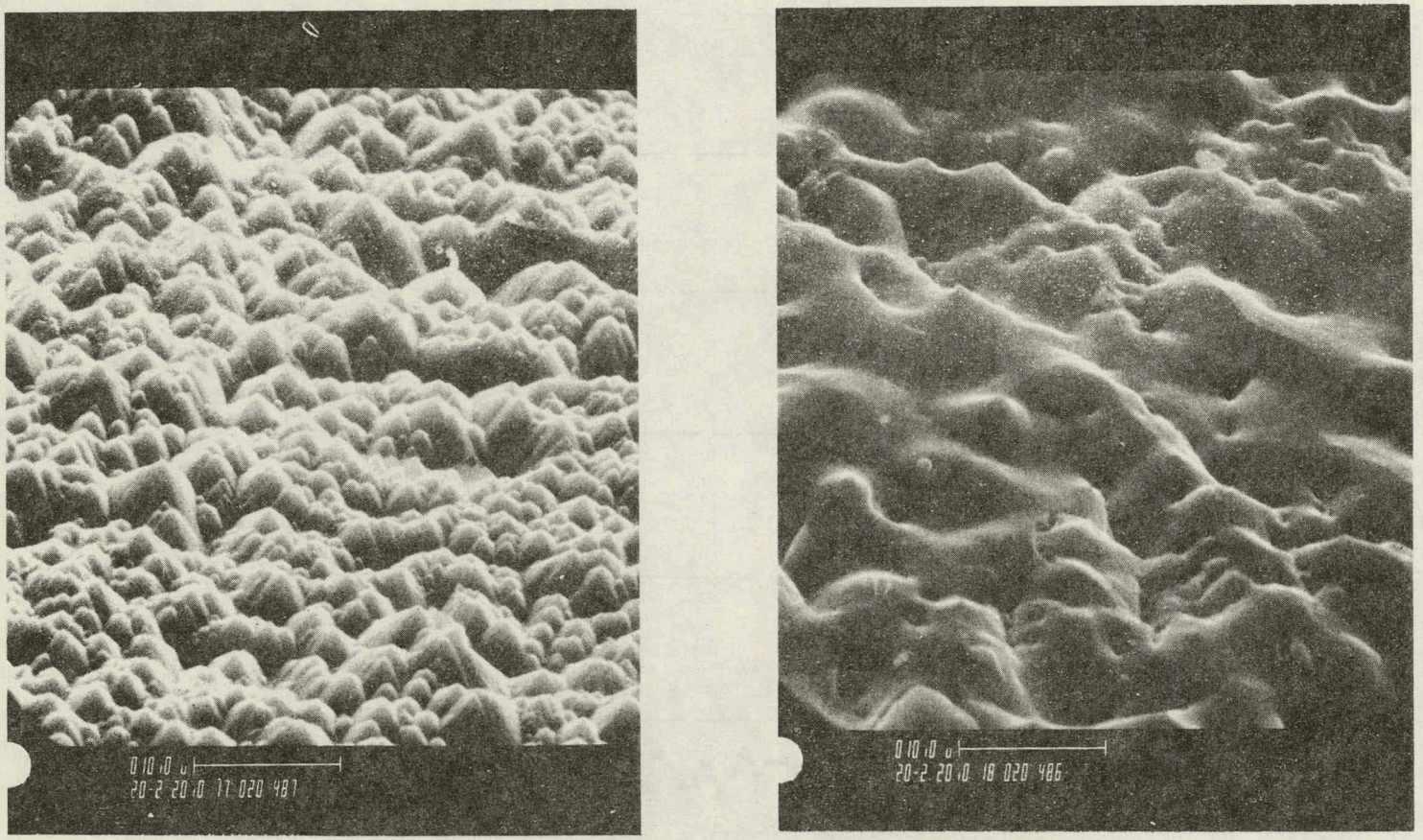
Figure 5. I-V Output for Laser Annealed Solar Cell

responses. The 5 ma I_{sc} for the .5 x .5 cm size cell converts to a value of 27 ma/cm^2 based on active area only, discounting the ohmic contacting and probe masking during test. This compares to a diffused junction 11% efficient cell, Figure 4, with an I_{sc} output of 32 ma/cm^2, discounting a 7% ohmic contacting masking area. High conversion efficiency was not anticipated from the flash-etched wafer due to low ion implantation fluence level -1 x 10^{15} ions/cm^2. The low outputs from the texture-etched specimens were probably due to junction disorientation. This was brought about by severe melting of the pyramidal surface during the laser annealing operation, Figure 6.

In making contacts with Quantel International Corporation, it was hoped to evaluate a high energy laser rather than a scriber such as used by Quantronix. Quantel International manufactures high energy lasers as part of their NGMO type product line. In the past, Q-switch glass lasers of output energy in the 30-100 joules category were delivered to various agencies in the U.S. and Europe. Unfortunately, as with other manufacturers (Korad, Apollo), these lasers were not available for evaluation. In fact, only a low energy unit (100 millijoules) Model YG-482 with a second harmonic generator, was available. The low output energy of this laser and lack of required optics precluded performance of meaningful tests.

The ruby rod for our in-house laser has been refurbished by Korad/Union Carbide. When installed and fired, however, there was evidence of water leakage through the clamp housing and into the front of the rod. Notified of this problem, Korad requested the rod back for additional servicing.

To study impurity redistribution following laser or furnace annealing, it was decided to perform a SIMS (Secondary Ion Mass Spectroscopy) analysis. It was discovered that Aerospace Corporation, Los Angeles, California offers SIMS service with an ARL Ion Microprobe Mass Analyzer. Initially, two phosphorus implanted, flash-etched wafers were sent to Aerospace as part of a feasibility study. Figures 7 and 8 show the depth profiles obtained from this evaluation.



(A) (B)

Figure 6. SEM photos (2000X/60° Tilt) of the Surface of a Texture-Etched/Ion Implanted Silicon Wafer before (A) and after Laser Annealing (B)

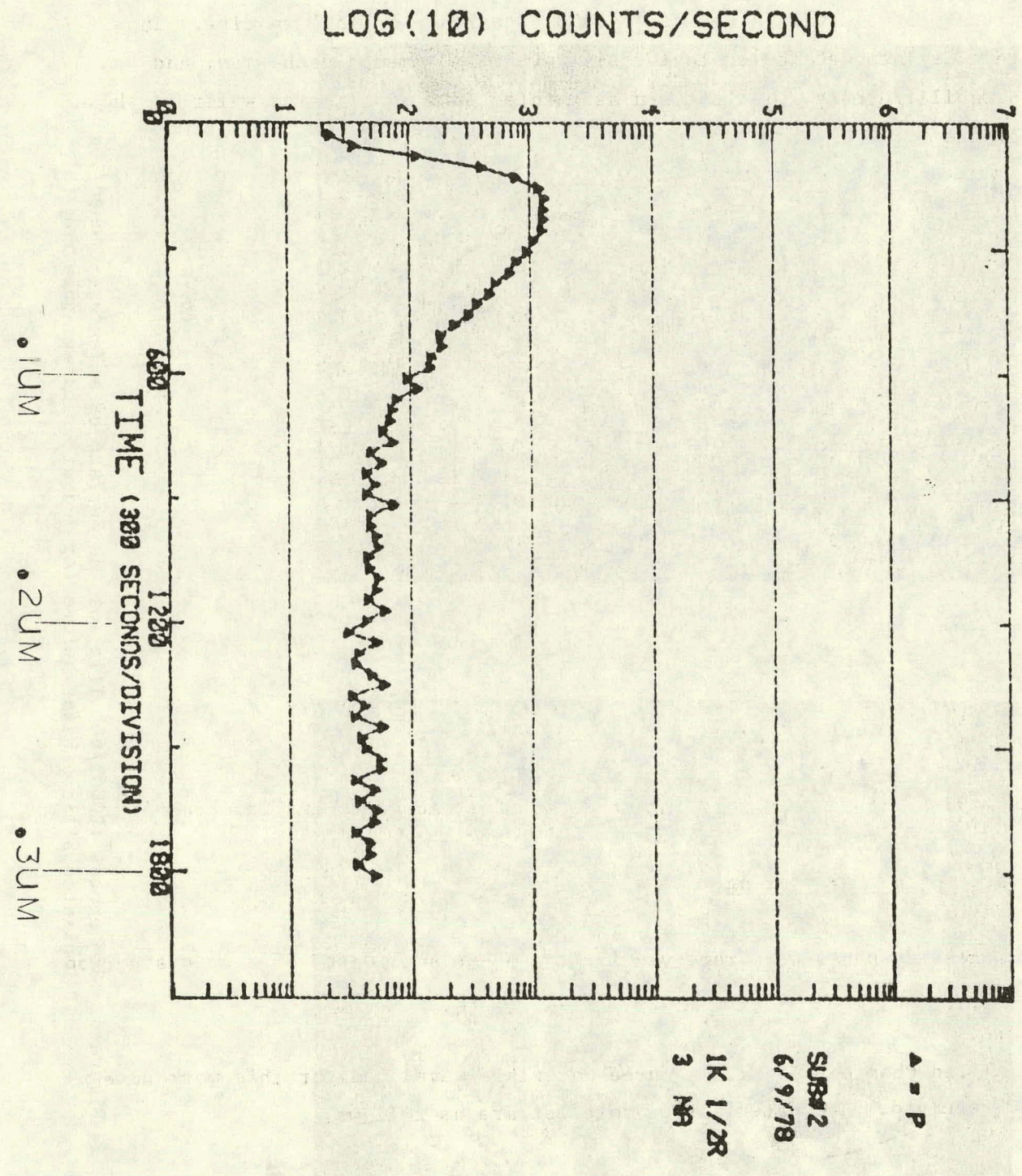


Figure 7. Profile of the Distribution of Phosphorus Atoms in Flash-Etched Si Sample Implanted at E=25KeV and D=$1x10^{15}$ ions/cm^2

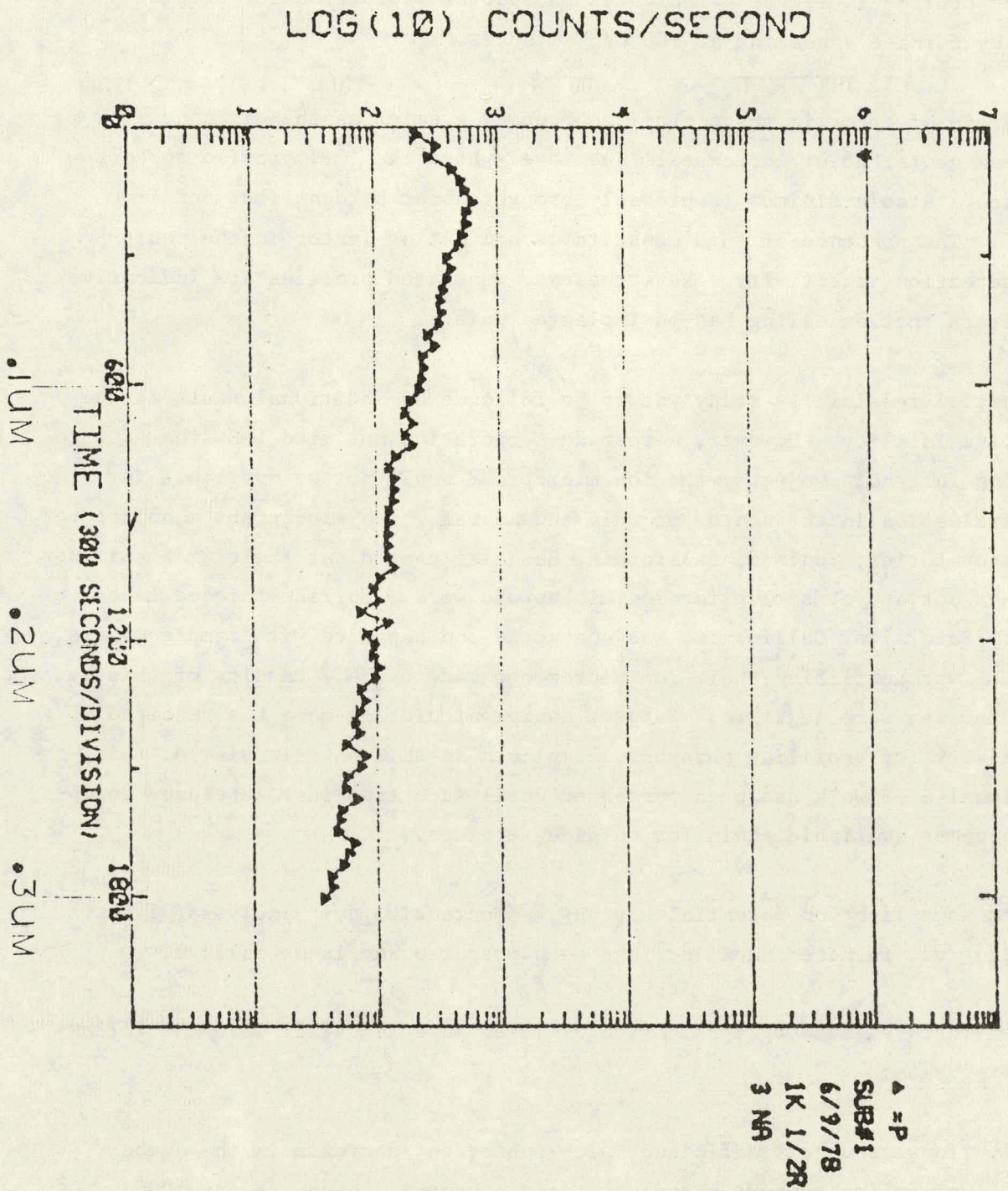


Figure 8. Profile of the Distribution of Phosphorus Atoms in Flash-Etched Si Implanted at E=25KeV and D=$1x10^{15}$ ions/cm^2 and Furnace Annealed at 900°C/30 Minutes

The sharp peak in Figure 7 is typical for an ion implanted sample. The broader profile in Figure 8 indicates phosphorus redistribution brought about by furnace annealing at 900°C/30 minutes.

The margin of error in these profiles becomes greater as the distance from the peak center point increases. The level where the $^{31}P+$ profile appears to reach a stable minimum is probably brought about by contributions from $^{30}SiH^{+}$. The presence of this constitutes a limiting factor in the equipment detection sensitivity. Nevertheless, generated profiles are indicative of effects that annealing has on implanted wafers.

The initial feasibility study was to be followed by additional tests at the Aerospace facility. However, Aerospace Corporation notified LMSC that due to pressing internal projects, the ion microprobe would not be available for SIMS evaluation in the months of July and August. Ion microprobe manufacturer, ARL Laboratories, Sunland, California, has also phased out their QMAS analyzer and was not as yet set up for ion microprobe work. Surface Science Laboratories, Palo Alto, California, was contacted and supplied with sample wafers for SIMS work utilizing their ion microprobe made by 3M. Results of this study however were negative. Subject equipment did not have the required sensitivity for profiling phosphorus implants in silicon. In view of this, additional SIMS work has been postponed until such time that Aerospace equipment becomes available again for outside services.

To shed some light on potential savings, an extensive cost analysis, laser annealing vs. furnace annealing, has been prepared and is as follows.

Cost savings realized by application of laser annealing fall into the following categories:

1. Increased cell efficiency with subsequent decrease in the number of cells, support structures, and associated hardware for 500 megawatt production rate

2. Decrease in energy consumption realized by using laser annealing techniques as opposed to furnace annealing

Savings realized from item 1 above are as follows:

- Area of 3-inch diameter cell = 45.6 cm^2
- Illumination Intensity = 100 mW/cm^2
- Total Incident Irradiation = (45.6 cm^2) x (100 mW/cm^2) = 4.56 watts
- A 12% conversion efficiency cell yields an output of ~.55 watts
- Assuming that laser annealing can yield a 2% conversion efficiency increase or a 14% cell, the yield will be ~.64 watts
- Projected into 1986, 500 MW/yr production capability at $.50/watt, the savings represent

$$\left[\left(\frac{500\ MW}{.55\ W/cell}\right) - \left(\frac{500\ MW}{.64\ W/cell}\right)\right] \times .55\ \frac{W}{cell} \times \$.5/W = \underline{\underline{\$35,156,250}}$$

Savings realized from item 2 are as follows:

Preliminary theoretical and experimental data indicates that for a ruby or frequency doubled glass laser, an energy density of approximately 1.5 joules/cm^2 is required to attain annealing of ion implanted silicon wafers. This translates to an energy of approximately 68 joules for single pulse annealing of a 3-inch diameter wafer. A Q-switched glass laser capable of operating at this energy level with a pulse repetition rate of 1 pps has a conversion efficiency of approximately .5%. This system offers the following savings:

- Resistance Furnace Power Requirements*
  1.88 KW to maintain 900°C annealing temperature

*Thermo-Brute American Furnace, 4-1/2 inch O.D. Tube Size

125 3-inch diameter wafers per run @ 30 min/run
1.88 KW x 5 hr = .94 KW hr to anneal 125 cells or
7.52 W hr/cell

- Laser Power Requirements
  68 joules required to anneal a 3-inch diameter wafer
  At .5% conversion efficiency, the laser requires 68/.005 = 13,600 joules = 3.78 watt x hr to supply the 68 joules

- 7.52/3.78 ≈ 2 or half as much energy is required for laser annealing as compared to furnace annealing

- For 500 MW/yr production capability

$$\left(\frac{500\ MW}{.55W} \times 7.52\ W\ hr\right) - \left(\frac{500\ MW}{.64W} \times 3.78\ W\ hr\right) \approx 3{,}900\ MW\ hr/yr \text{ savings}$$

3.1.4 Screen Printed Contacts

Screen printing using DuPont 7095 Ag paste for the grid pattern shows excellent 0.005 to 0.008-inch line resolution. DuPont 4021 Ag/B paste was used for the back. Problems have been encountered in firing the 7095 grid material. Cells ion implanted similar to a 7% efficient nickel plated run were screen printed and fired using schedules recommended in the published reports of other project contractors, namely, 45 seconds at 650°C. Output IV curves reflect a high series resistance. DuPont technical representatives in Wilmington, Delaware indicated performing experimental work with the 7095 at a 580° to 600°C temperature, 2 to 5 minute firing temperature range, with sporadic results. Our work will continue in the use of this material making only slight variations from the manufacturer's published data in attempting verification of this process segment.

As a parallel effort, evaporated Ag/Ti contacts will be formed as a control for evaluating the screen printed units and to allow fabrication and evaluation of laser annealed units.

A screen was made with a series of .150" squares and .150" spacing. This pattern is intended for contact resistance measurements, adhesion, and solderability tests. The pattern as printed on a 3" diameter wafer is shown in Figure 9.

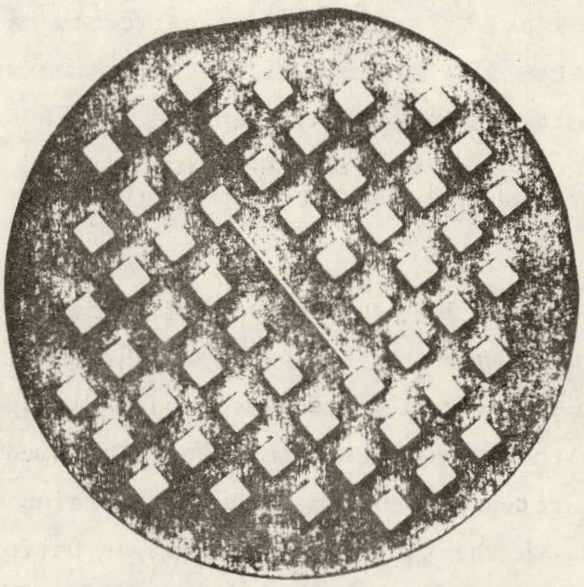


Figure 9. Test Pattern for Contact Resistance, Adhesion and Solderability Tests

3.1.5 Sprayed AR Coating

All accessory parts were received for the Zicon Autocoater during this period and the equipment made operational.

The Allied Chemical Tantalum source materials developed for this work were also received. The materials of interest are as follows:

- Solution No. 482 - All Ta, developed for Spin-On Applications
- Solution No. 201 - All Ta, developed for Spray-On Applications
- Solution No. 702 - Ta/Si, developed for Spray-On Applications

The above materials are all low viscosity and low solids systems. They are supposed to yield films that when deposited and cured, will be essentially all Ta_2O_5. When applied to silicon wafers by spinning at 2000 rpm and followed by baking at 175°C, a film with thicknesses of 500 to 1000 Å results.

Spraying of the Allied Chemical Ta solutions was performed on polished wafer surfaces using the Zicon Autocoater. Initial thickness measurements made using a Gaertner Ellipsometer showed coatings on the 3-inch diameter wafers ranging from 500Å to 1200Å. Later work resulted in improved uniformity on a 3/4" width band of 1100Å to 1240Å.

A test plan was devised followed by experimentation to determine the adequacy of materials and processing. Space cells 2 x 4 cm in size with chem polished surfaces were used. The cells used, as-received, have an SiO coating. Measurements were made in the as-received condition, followed by stripping of the SiO with buffered HF, retested, coated with the tantalum solutions, and again retested. Coating with the tantalum solution was performed by both spinning and spraying. Spinning is a proven process and over this small area, good thickness uniformity was assured for comparison with the spray-on process. Tables II and III show the results of this experimentation for spin-on and spray-on, respectively.

Reasonably good uniformity was attained on the sprayed specimens as evidenced by the light blue coloring across the cell area. The as-sprayed values as shown in Table III ranged from 1 to 6% lower than the as-received SiO. This could be attributable to the index of refraction differences between SiO and TaO.

Some spray work was performed by International Rectifier using metallo-organic resinates supplied by Englehart. A tantalum #7522 base material (8.2% Ta) was applied on blank texture-etched silicon wafers and fired in air at 500°C for 5 minutes. Relative reflectivity measurements were made using the reflectance tester described in Quarterly Report No. 1. Table IV shows these preliminary results. Data was normalized to a flat black paint surface.

TABLE II

SPUN-ON Ta SOLUTIONS

Specimen: 2 x 4 cm Space Cells with SiO Coat, Chem Polished

Process Parameters: 2000 rpm/10 sec

Specimen No.	Ta Solution	Output I_{sc} (mA)		
		As-Received	After SiO Strip	After Coated
AR 1	201	273	212	245
AR 2	201	267	207	265
AR 10	482	270	213	265
AR 13	482	269	199	236

TABLE III

SPRAY-ON Ta SOLUTIONS

Specimen: 2 x 4 cm Space Cells with SiO Coat, Chem Polished

Process Parameters: Zicon Autocoater, 1 pass, 22 inches/sec travel, 4.25 inches nozzle HI, 9 mil orifice, 2 psi source, 40 pso nozzle (both N_2), baked 175°C/2 min

Specimen No.	Ta Solution	Output I_{sc} (mA)			% Increase From Bare Cell
		As-Received	After SiO Strip	After Coated	
SPY 1	482	286	215	274	27
SPY 2	482	273	223	257	15
SPY 3	482	275	214	258	21
SPY 4	482	272	221	259	17
SPY 5	482	280	224	262	17
SPY 6	201	283	216	266	23
SPY 7	201	283	219	274	25
SPY 8	201	277	207	268	29
SPY 9	201	290	220	287	30
SPY 10	201	295	222	292	31
SPY 11	201	278	219	271	24

TABLE IV

RELATIVE REFLECTIVITY MEASUREMENTS

Condition	Reflectivity		
	Flat Black Surface (ref)	As Text-Etch	As Coated
Ta Resinate (Modified to Spraying Consistency)	1.0	2.4	.9
Ta Resinate - #650 Glass Resin Mixture	1.0	2.3	1.3
Ta Resinate + Acrylic Coat	1.0	2.4	<.6

The relative reflectivity numbers shown indicate a measure of some potential. More work is necessary in this area using the metallo-organic resinates.

3.2 HIGH VOLUME PRODUCTION

3.2.1 Ion Implantation

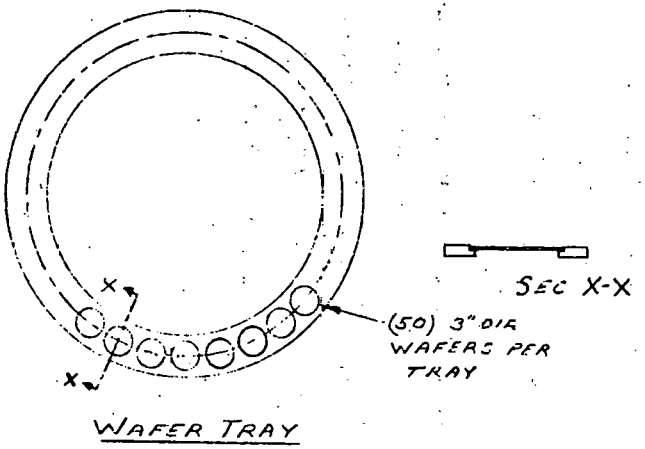
Ion implantation of silicon wafers has been proven practical in equipments which are not configured for high quantity production rates. It has been determined that an ion implanter with a 10 mA beam current will be able to scan a single wafer in approximately one second. If we accept this scan rate as realistic, then the task of achieving 1986 solar cell production rates centers on the presentation of wafers to the beam with a minimum of interruption to its continuous productive operation. Ion beams at the proposed current levels do not respond to electrostatic scanning methods and it is therefore necessary to plan for a fixed position beam used in conjunction with mechanical scanning equipment.

In addition to maximum beam utilization, the other major problem in high production ion implantation is the presentation of wafers to the beam in a

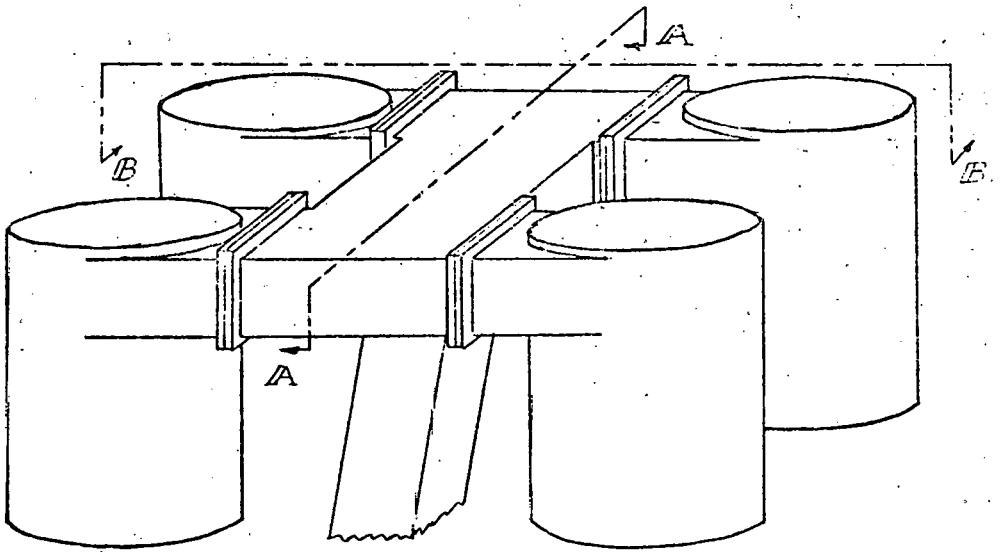
high vacuum environment. Two basic approaches are available. One of these feeds the wafers individually through a series of gated chambers of progressively higher vacuum to a central chamber for implantation. They are then carried out of the system in a similar manner. This method presents some problems in the necessity for high frequency cycling of the gate valves. The other option is an extension of the conventional method where a number of wafers are mounted in one or more carousels and placed in a chamber which is then evacuated. Provision is made to either scan the wafers individually in relation to the ion beam, indexing the carousel, or to rotate the carousel, scanning all of the wafers in a batch mode.

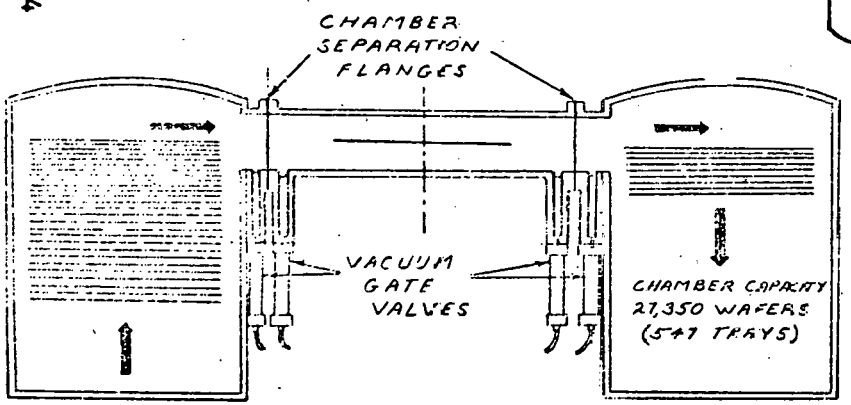
We propose a concept based on the more conventional method. This is represented schematically in Figure 10. In this approach, the fixed beam enters an implantation chamber through the bottom and at an angle of 7 degrees from the vertical. Four cylindrical chambers are arranged in a rectangular pattern and secured to gated flanges on the implantation chamber. Two of these contain wafers awaiting processing and two are used to store implanted wafers. The cylindrical chambers are also gated at the separation flange so that they may be individually removed for loading, unloading, and evacuation. A fifth chamber is provided so that these operations may be accomplished while the other four are in operation. These cylindrical units are fitted with air cushion pallets at the base to facilitate guided movement to and from the load/unload/evacuation station. Internal, electrically operated elevator and transfer devices are required to feed or receive flat trays, each containing 50, 3-inch diameter wafers, to and from the implantation chamber.

The LMSC process specifies that the wafers be edge masked for ion implantation. This permits the use of counterbored wafer pockets in flat ring-shaped trays, with the ion beam positioned at an angle to preclude channeling. The wafers may be automatically transferred to the trays from the cassettes used in the texture etching operation and may either be left in the trays for the next operation of laser annealing or transferred to a conveyor belt for that operation.

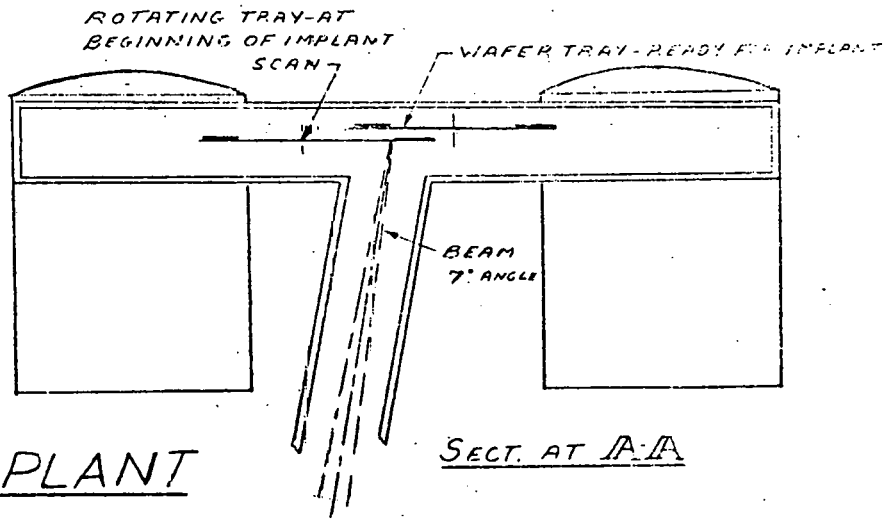


WAFER TRAY





SECT. AT B-B



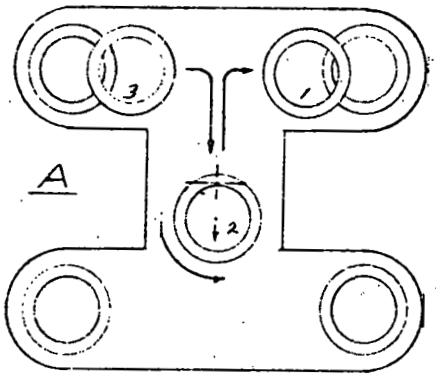
SECT. AT A-A

SCHEMATIC-ION IMPLANT SYSTEM

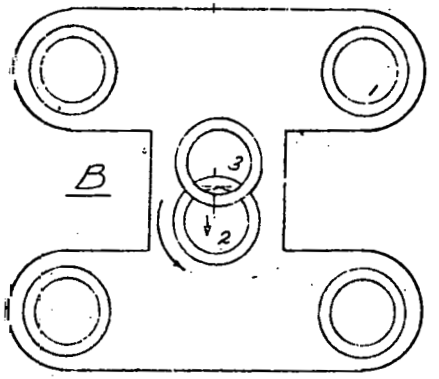
Figure 10

The sequence of processing steps within the ion implantation chamber is represented, in part, in the schematic diagram of Figure 11. Diagram A shows one processed tray being moved to a storage chamber, one tray scanning over the beam and a third tray being moved out of the supply chamber. The scanning of tray No. 2 is accomplished by rotation of the tray while its axis is moving laterally. The resulting beam path is a flat spiral which impinges on the exposed underside of all wafers in the tray. Diagram B shows tray No. 3 in a waiting position above tray No. 2. A rise and fall mechanism is included in the tray handling system for this purpose. As tray No. 2 is completing its scan with the beam at its outer periphery, tray No. 3 begins rotation and lateral movement. When tray No. 2 is processed, it is immediately withdrawn and tray No. 3 is then scanning over the beam. In Diagram C, tray No. 3 is shown still scanning. During this period, it is lowered to the level originally occupied by tray No. 2. The distance of vertical travel is small and should not affect the characteristics of the ion implantation process. Tray No. 2 in this diagram is in position at the end of the central chamber where a ring of 50 small platens are brought into contact with the underside of the individual wafers, raising them slightly. These may be opposed by additional lightly weighted pads which are free to rotate as they contact the top sides of the wafers. The lower platens are rotated 90° causing the wafers to be repositioned without leaving their respective pockets. The platens and opposing pads are retracted and tray No. 2 is moved back into the raised waiting position as shown in Diagram D. Upon completion of the scan of tray No. 3, it moves to the other end of the central chamber for wafer indexing while tray No. 2 is scanning and being lowered. This is represented in Diagram E. This process is continued until each tray has been scanned four times to expose the beam to all flanks of the pyramidal surfaces of the etched wafers. Upon completion of the processing of a tray, it is replaced by a new tray, as in Diagram A, within the time period of one tray scan. No interruption of beam utilization should occur.

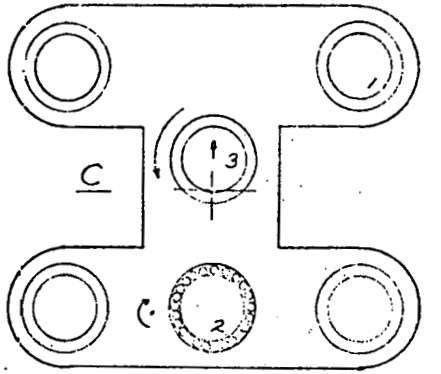
The tray handling system is necessarily complex to accommodate the processing requirements. It does, however, represent a conventional task in electromechanical design and its configuration may be readily envisioned. Moreover,



TRAY #
#1 IMPLANTED WAFERS MOVING TO STORAGE
#2 ROTATING SCAN OVER BEAM
#3 MOVING FROM STORAGE TO SCAN POSITION

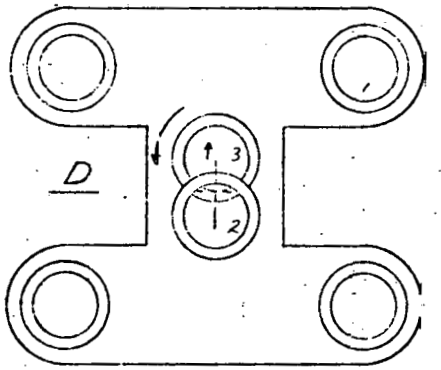


TRAY
#1 IN STORAGE CHAMBER
2 CONTINUING SCAN
3 IN RAISED POSITION - WAITING

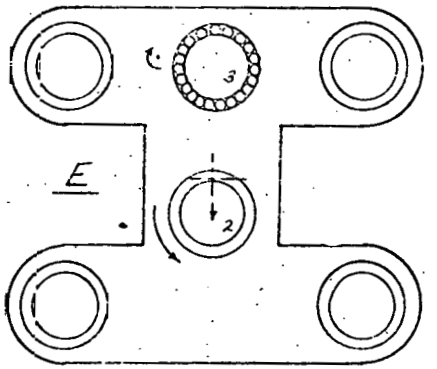


TRAY
#2 IN WAFER INDEX POSITION
#3 LOWERED TO IMPLANT POSITION
ROTATING SCAN OVER BEAM

NOTE: SHOWING
PLAN VIEWS OF SECTION THROUGH
IMPLANT AND STORAGE CHAMBERS



TRAY
#2 IN RAISED POSITION - WAITING
#3 CONTINUING SCAN



TRAY
#2 LOWERED TO IMPLANT POSITION
ROTATING SCAN OVER BEAM
#3 IN WAFER INDEX POSITION

SCHEMATIC - ION IMPLANT STEP SEQUENCE

Figure 11

the system is cycled at a considerably lower frequency than would be required forindividually processed cells.

A micro computer control system should be incorporated. This will allow flexibility in programming of the various elements of the process to maximize the throughput.

The production rate of the system described is predicated on an ion implantation time per wafer of 1.048 seconds, or 52.4 seconds for a tray of 50 wafers. An edge-to-edge spacing between wafers in a tray is assumed at 1/2-inch and therefore we allow 60 seconds of processing time per tray. This is divided into 4 scans of 15 seconds each, which also is the time available for wafer indexing and/or tray exchange. Lost time within the cycle is limited to the period necessary to withdraw a tray from the beam area on completion of a scan. This is assumed to be very small and should be accommodated within the allotted 15 second scan period.

A tray holding 50 cells at 1/2-inch edge spacing will be about 60 inches in diameter. One-eighth inch allowance is made for tray thickness, but 1/16 inch should be adequate.

At 50 wafers per minute, the throughput rate is 3000 per hour, or 24,000 per shift. This represents 480 trays. On the assumption that some improvement in rate may be possible, we would suggest that provision be made for 600 trays per shift. To minimize the downtime for replacement of cylindrical chambers in the system, we suggest that this be planned for one occurrence per shift. With the dual gates provided at the separation flanges, and with the tanks pumped down in advance, changeover should be accomplished in minutes.

Two chambers are always in use supplying fresh trays; therefore, if each holds the equivalent of one shift's production, it will be emptied in 16 hours. The empty chamber is left in place to receive processed trays by reversing their

direction of travel and the full chamber is replaced. Using a staggered schedule, one chamber is replaced every 8 hours. If the schedule is not staggered and their capacity is halved, then both full chambers are replaced every 8 hours. We will assume the first condition, and configure the chambers to hold 600 trays. At .125" thickness per tray, this represents a stack height of 75 inches. Allowing room for the internal handling devices, the chamber will be about 84 inches in height and about 66 inches in diameter. This is a considerable mass, but can be moved readily with an air cushion device and guide tracks.

In summary, the proposed system presents a risk to the JPL program objectives only in the scale up of the ion beam current levels. The balance of the system employs current technology. Multiple systems will of course be necessary to achieve the target production rate. To some extent, this is a desirable condition to safeguard against total production stoppage in the event of unit shutdown. Downtime necessary for the servicing of the ion beam has not been addressed, although this factor must be considered in a final assessment of production capability.

3.2.2 Laser Annealing

Laser annealing has been demonstrated to be a practical alternate for furnace annealing. This process offers definite advantages for high volume production of solar cells. These are: reduced energy consumption, operation in normal atmosphere and fast throughput. The specifics of the laser equipment recommended for this process have been discussed elsewhere in this report. For the purpose of this projection, it is sufficient to note that the laser will emit a uniform, 3-inch diameter pulse with a pulse duration of less than 100 nanoseconds at a repetition rate of 60 pulses per minute. Given these premises, the adaptation to production capability requires only the transport of wafers to and from the workstation under the laser beam.

The previous operation in our process sequence is ion implantation. At the completion of that process, the wafers are nested in pockets near the periphery of circular trays. A quantity of these trays will constitute a stock float to supply the annealing process. The first step in wafer handling will be to transfer the wafers from the trays to similar stations on a turntable. A tray handling mechanism similar to that described for use within the ion implant chamber will be used to present individual wafers in rapid sequence to a "pick and place" arm fitted with a vacuum chuck. The wafers will be positioned on elevated platform work stations arranged in a circle on the turntable. They will be initially held in place by light vacuum pressure until they are precisely centered on the station at the first index of the table. The vacuum will then be increased to maximum holding power. At the next index, the wafers will be positioned under the laser and the beam will be triggered. The wafers will be allowed to cool through several indexes of the table and then a V/I reading will be taken by contacts which are brought to the top surface of the wafer. A microcomputer will receive the readings and signal adjustment or shutdown of the operation as appropriate. It will also trigger removal of the wafer from the line at a subsequent station. The final step in this operation will utilize a second "pick and place" device to place the wafers on a conveyor belt which feeds the following screen printing operation. A 12-inch diameter turntable, holding 8 wafers and indexing at 1 cycle per second will be adequate for this operation. The take-off conveyor belt will travel at 16 feet per minute.

3.2.3 Screen Printing of Ohmic Contacts

The screen printing of conductive pastes of the front and back surfaces of the wafer can be accomplished at an acceptably high rate of speed on presently available equipment. The Universal Instruments Corporation Autofeed 4000 Thick Film System is capable of 1500 cycles per hour. This equipment, as presently sized, can screen print six 3-inch diameter wafers per cycle for a throughput rate of 9000 wafers per hour. The system is entirely automated and includes the capability to unload wafers from cassettes and reload these

cassettes upon completion of the operation. As an alternative, wafers could be transferred directly to the screen printer from the take-off conveyor belts of the preceding laser anneal operation. A minimal penalty occurs in stoppage of automatic laser operation. Since several lasers will be producing annealed wafers to feed several screen printers and these workpieces can be cross-fed from any laser to any printer, it seems more reasonable to plan on this basis. The necessity of loading and unloading cassettes between these operations can be eliminated. Shutdown of any one machine in either operation will not have serious impact on the production flow.

Two automatic screening machines are contemplated, each with an integral drying oven. A firing oven to fuse the conductive paste will complete the system. Wafers will be processed automatically through all three units in line.

The process sequence envisioned for screen printing of conductive pastes on both front and back faces of the wafers for 1986 production is as follows:

1. Wafers received from laser anneal on a conveyor belt will pass through a turnover device to position them back-face up.

2. Six wafers, in 2 rows of 3 wafers each, are positioned on vacuum chucks and screen printed.

3. The wafers are transferred in rows of 3 to a conveyor belt and passed through an infra-red drying oven. At 1500 screening cycles per hour, the conveyor belt speed must be 12.5 feet per minute. At 30 seconds drying time, the oven length will be approximately 7 feet. Oven temperature is expected to be at 150°C.

4. The wafers are then passed through a second turnover device to place them front side up.

5. The front side of the wafers is screen printed as before with the required grid pattern.

6. The wafers are then passed through the second drying oven at the same speed and temperature.

7. The final operation is the fusion of the conductive pastes. For this step, the wafers are transferred to another conveyor belt in line and are passed through another oven at 650°C for 45 seconds. Oven length for this exposure is approximately 10 feet.

This screen printing operation has been defined in terms of currently available equipment, and therefore represents no requirement for new technology. The conductive pastes are similarly available. Silver/Alum Paste has been specified for the back surface of the wafer and DuPont Silver Paste #7095 is planned for the front face grid pattern. These selections are based on developmental work by LMSC and by other JPL contractors. The risk in the silk screening operation defined is in the fact that no provision is made for conditioning of the wafers before they enter this step in the process. A dilute HF acid wash has been used at this point in the current developmental work, but it is assumed that this will not be required in a straight line continuous production set up.

3.2.4 Production Spray of Anti-Reflective Coating

The laboratory development of a process for spray coating of anti-reflective material on 3-inch diameter solar cells has been extrapolated to a preliminary plan for high production operations. The anticipated production process and equipment are described in the following.

The process sequence under study by LMSC specifies that the two operations immediately preceding spray coating are laser annealing and screen printing. Both of these are considered highly reliable, continuous processes and are unlikely to be subject to frequent line stoppage. In addition, both operations are capable of accepting interruptions to their continuous function without penalty. We therefore propose that the laser anneal, screen printing and spray coating operations should be set up with connecting conveyors and

without a stock float between process steps. This will eliminate considerable handling of the wafers and attendant costs.

It is practical to establish the conveyor speed of the spray coating operation at approximately 1/4 that of the preceding screen printing equipment. Therefore, with the addition of a cross conveyor transfer unit, it will be possible to match their throughput rates and set up duplicate sets of these equipments as production requirements are increased.

Wafers are received from the screen printing operation at a rate of 150 per minute (9000 per hour) arranged in rows of 3 on a 10-inch wide conveyor belt, traveling at 13 feet per minute. A transfer device, fitted with 12 vacuum chucks in line, will be used to pick up 3 cells from the conveyor in each of 4 index positions. The vacuum chucks should not exceed 2 inches in diameter and are to be mounted on small motor shafts. The grid pattern on the top surface of the cells will be visible to photo-reflective sensing devices mounted adjacent to the vacuum chucks. The chucks will be rotated until the "N" contact area of the grid patterns is properly aligned as sensed by the photocell. When all 12 cells are radially aligned, the transfer device will move laterally to a fifth index position over an inclined 40-inch wide conveyor belt. The 12 cells will then be deposited in a row on this belt which is fitted with offset projecting tabs to serve as spray masks for the "N" contact areas of the cell grid pattern. Motion of the transfer device will be coordinated with the travel of the belt. Inclination of the belt will assure that cells remain nested in their locators and under the masking tabs while passing through the spray. Speed of the belt will be at about 4 feet per minute, slightly faster than required, to provide a 1-inch space between rows and eliminate the chance for spray overlap on successive passes of the spray head. As presently defined, the spray process requires that the spray nozzle orifices are .009" diameter, are positioned 4 inches away from the workpieces and that the heads traverse at 4 inches per second. A fan-shaped spray is used and a single pass is made. The resultant coating is 700 angstroms in thickness.

A number of spray nozzles are to be fixed in relative position on a traversing head. The total width of the spray pattern should be 12 inches and the traverse patch across the width of the 40-inch belt should be angled so that the spray pattern follows across the same 3 rows of cells as they progress forward on the conveyor belt. At 4 inches per second, the head will make a single pass in 10 seconds. Since 1 foot of belt travel at 4 feet per minute will take 15 seconds, the remaining 5 seconds are available for rapid return of the head to the starting position for the next pass.

After leaving the spray chamber, the coated cells are transferred to another conveyor belt on which they are carried through a baking oven to polymerize the coating. The present process specifies a 20 minute exposure at 175°C which would require an oven 80 feet in length. It is expected that a significant reduction in bake time can be achieved by reformulation of the coating material. For the purpose of this exercise, we assume an oven length of 30 feet.

In summary, the basic coating application method is considered to have been demonstrated at the laboratory level. The application of the process in high production equipment utilizes existing technology. Although some refinements in process detail will be required, these can readily be accommodated at minimum penalty in pilot production equipment. The principal area of risk exposure is in the assumption of a reduced baking time.

3.3 SAMICS

SAMICS Format A's based on the high volume production projection for 1986 were completed and submitted to JPL on the following processes:

- Texture Etching
- Ion Implantation
- Laser Annealing
- Screen Printed Contacts

SECTION 4

CONCLUSIONS

4.1 Laser annealing was demonstrated to produce cells with reasonable output performances based on these initial efforts.

4.2 Laser annealing can significantly reduce costs of solar arrays due to a reduction of cell quantities based on cell efficiency increases over thermal anneal processing.

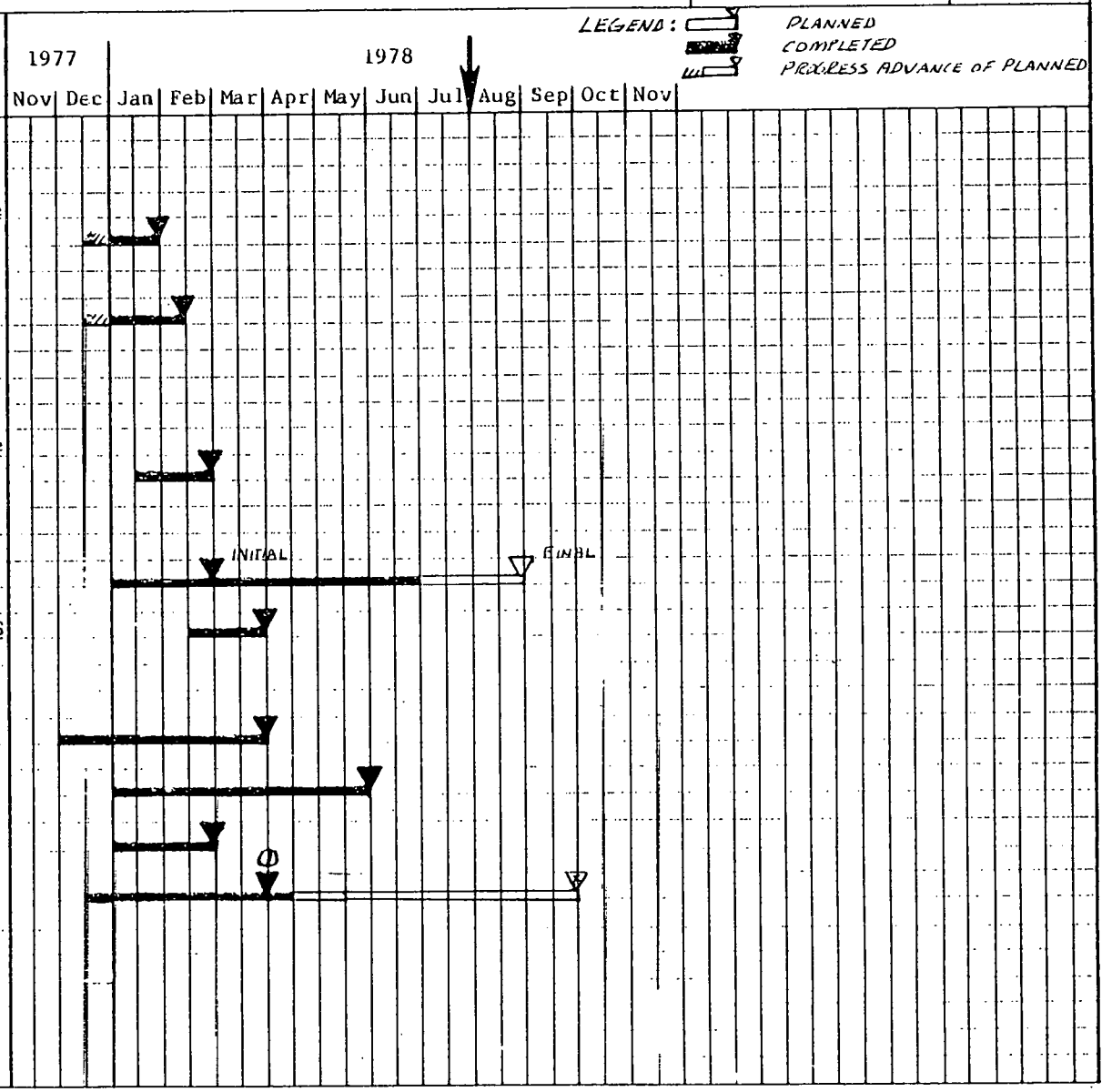
4.3 Spraying of reasonably uniform thickness (1100Å - 1240Å), low viscosity, AR coatings was demonstrated to be effective over 3/4-inch width patterns using our existing autocoater. However, some nozzle and spreader redesign will be necessary to accommodate larger width patterns.

PROGRAM PLAN STATUS

Progress to date is shown in the following Program Plan Chart.

PROGRAM PLAN

MODEL	PLAN	TITLE	PREPARED BY:	DATE
		PH 2, AUTOMATED ARRAY ASSEMBLY - Contract 954898	M. Lopez	12-6-77
ISSUE NO.	REFERENCE		APPROVED BY:	DATE
Rev. A 7/28/78	CDRL Item 2(a)			



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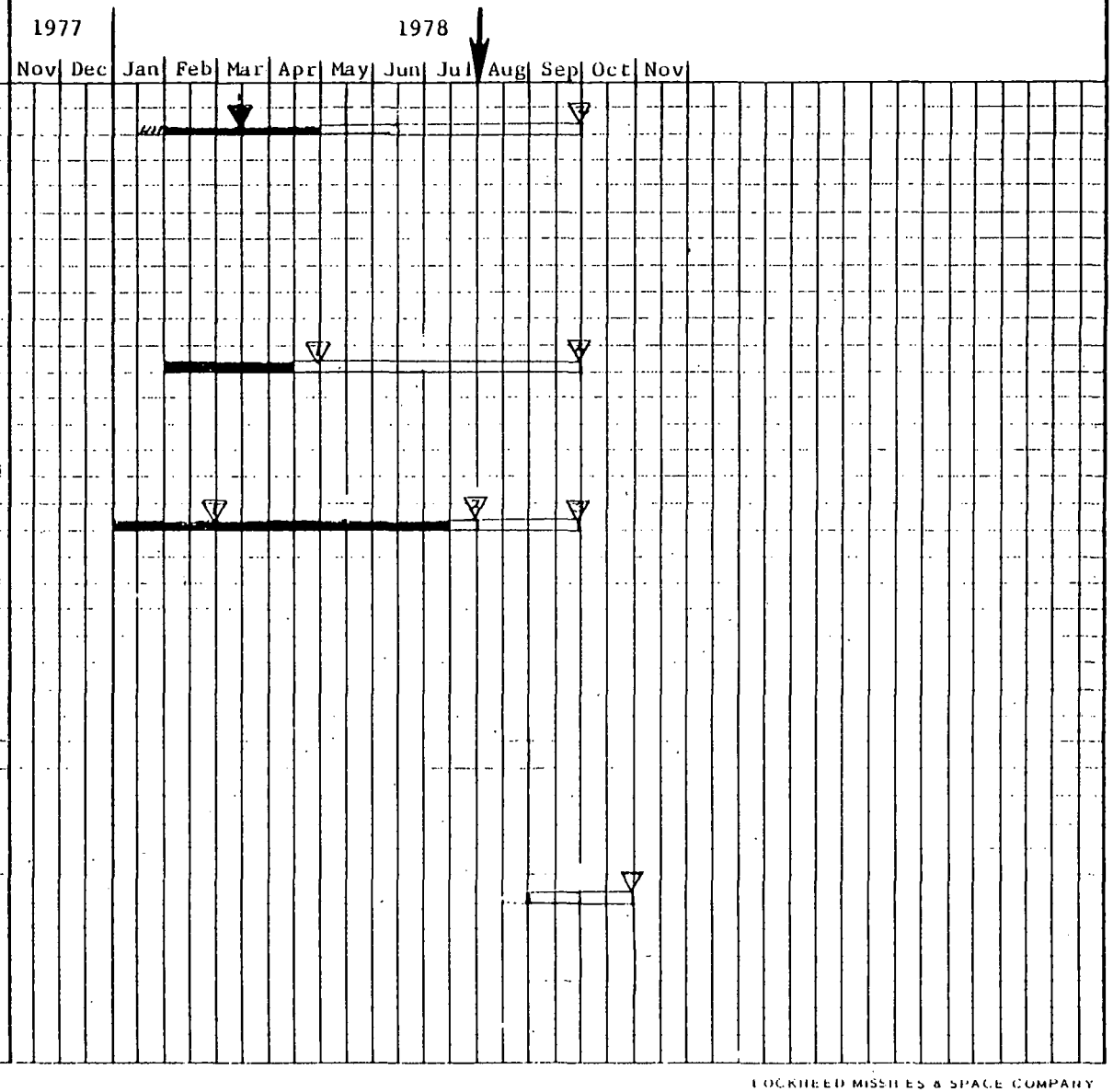
PROGRAM PLAN

MODEL	PLAN	TITLE	PREPARED BY:	DATE
		PH 2, AUTOMATED ARRAY ASSEMBLY - Contract 954898	M. Lopez	12-6-77
ISSUE NO.	REFERENCE		APPROVED BY:	DATE
Rev. A 7/28/78	CDRL Item 2(a)			



PROGRAM PLAN

MODEL	PLAN	TITLE	PREPARED BY:	DATE
ISSUE NO. Rev. A 7/28/78	REFERENCE CDRL Item2(a)	PH 2, AUTOMATED ARRAY ASSEMBLY - Contract 954898	M. Lopez APPROVED BY:	12-6-77 DATE