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High-Level Neutron Coincidence Counter Maintenance Manual

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Los Alamos, New Mexico 87545

DISCLAIMER

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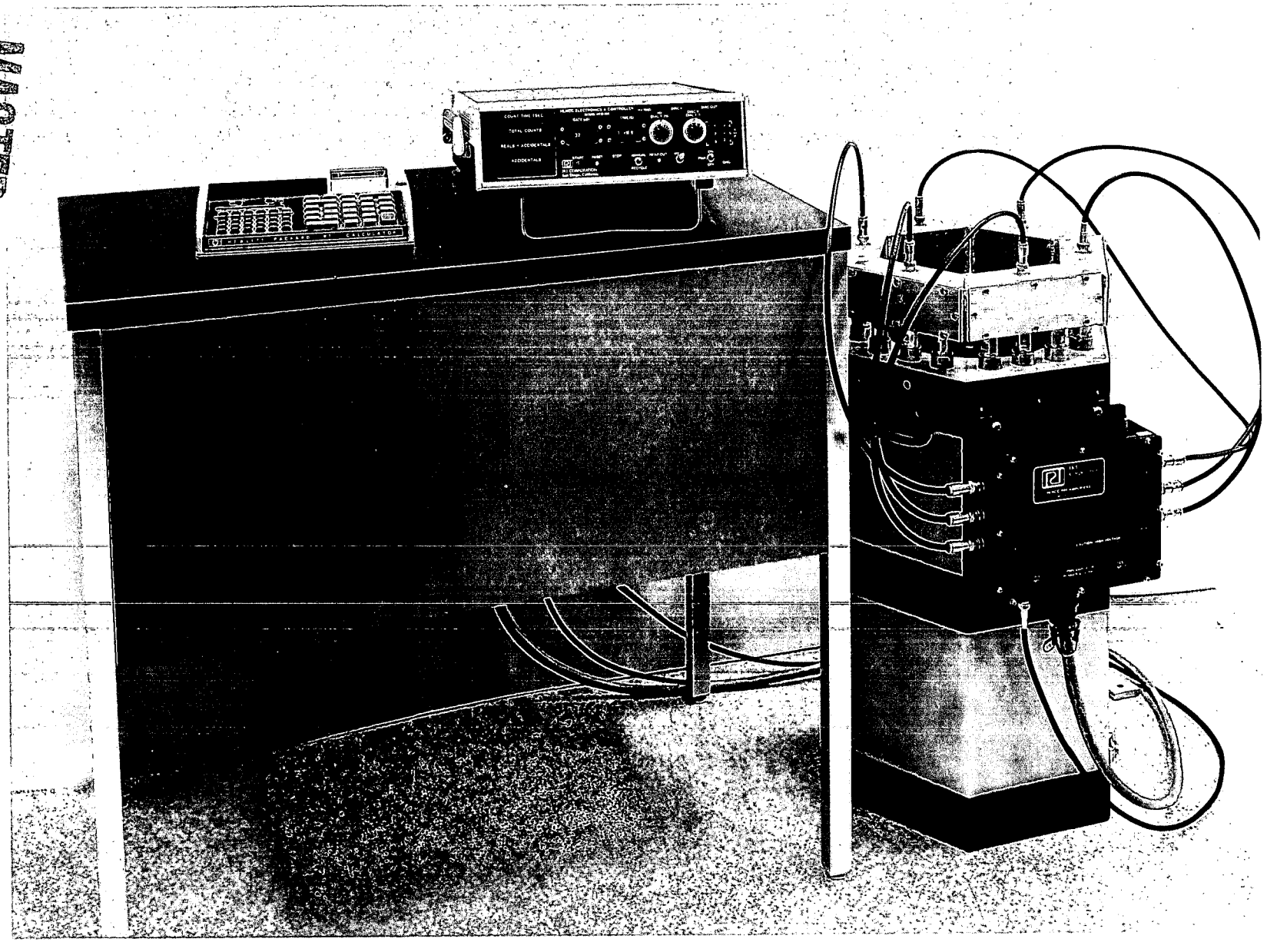
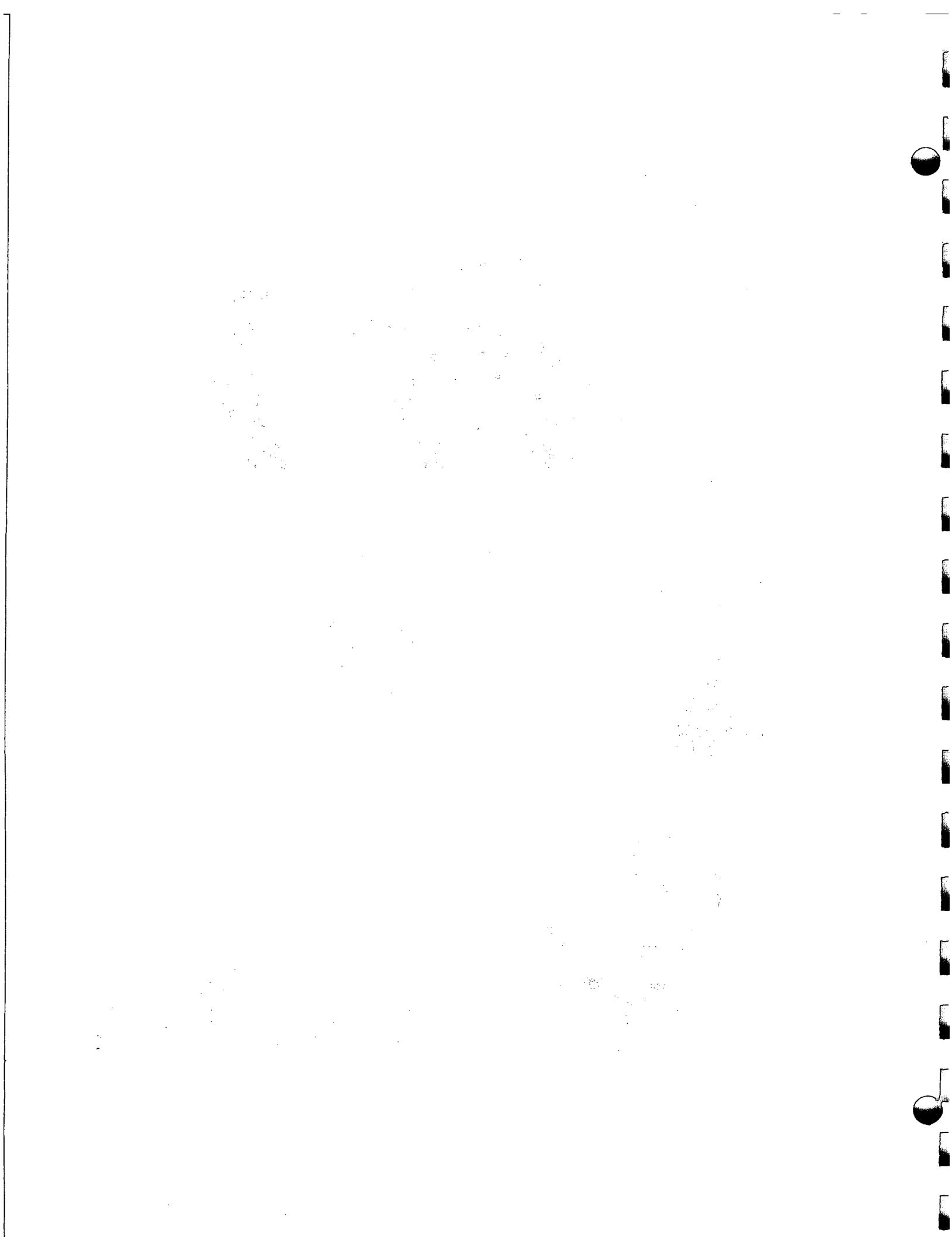


HLNCC assembled for measurement.



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HIGH-LEVEL NEUTRON COINCIDENCE COUNTER MAINTENANCE MANUAL

by

J. Swansen and P. Collinsworth

ABSTRACT

High-level neutron coincidence counter operational (field) calibration and usage is well known. This manual makes explicit basic (shop) check-out, calibration, and testing of new units and is a guide for repair of failed in-service units. Operational criteria for the major electronic functions are detailed, as are adjustments and calibration procedures, and recurrent mechanical/electromechanical problems are addressed. Some system tests are included for quality assurance. Data on nonstandard large-scale integrated (circuit) components and a schematic set are also included.

I. INTRODUCTION

During the past few years several reports and manuals[1-6] have been written for the High-Level Neutron Coincidence Counter (HLNCC) electronics package. Much of this information is duplicative. These reports give adequate information on what is in the HLNCC shift-register electronics and how to use it for normal applications, but they do not address the problem of checking out a new unit or repairing a failed unit.

The present manual gives maintenance and check-out procedures for a new or failed HEC-100 electronics unit. We assume that the basic information in Refs. 1, 3, and 5 is available to the user. This report is addressed to the electronics maintenance personnel rather than the normal HLNCC user, and it is

assumed that the reader is familiar with the instrument; for example, attendees of a Los Alamos HLNCC maintenance school would usually have the requisite familiarity with the instrument.

This manual primarily deals with checking out a HLNCC electronics package (HEC-100 counter/controller, HP-100 high-voltage junction and preamplifier box, and accessory items) for proper operation. Secondarily, the information in the manual is arranged to assist maintenance personnel in isolating problems to major subcircuits. Illustrations of component locations are included as are illustrations of selected waveforms; a schematic package is included to aid in detailed troubleshooting.

II. VISUAL AND MECHANICAL INSPECTION

A visual and electromechanical inspection of incoming HLNCC systems is of critical importance. Our experience has shown that operational problems can be reduced, or avoided altogether, by simple inspection and remedial action. Among the problems, in approximate order of importance, are

- improper shielding and discontinuous or high-impedance grounding, particularly in the preamplifier box, but also at other locations in the analog section of the complete HLNCC system;
- noise because of failure to maintain cleanliness in the high-voltage and high-impedance signal section of the preamplifier box;
- loose, missing, or improperly installed components, circuit boards, connectors, and wiring harnesses;
- poor solder connections (that is, cold solder joints);
- improper component values; and
- faulty cable assemblies.

All six problem areas have been seen both in newly manufactured units and in field (in-service) instruments.

A. Initial Steps

1. Unpack and check contents of shipping containers (Fig. 1).
2. Rotate and shake HEC-100 to check for loose components.
3. Rotate and shake HP-100 (preamplifier box).

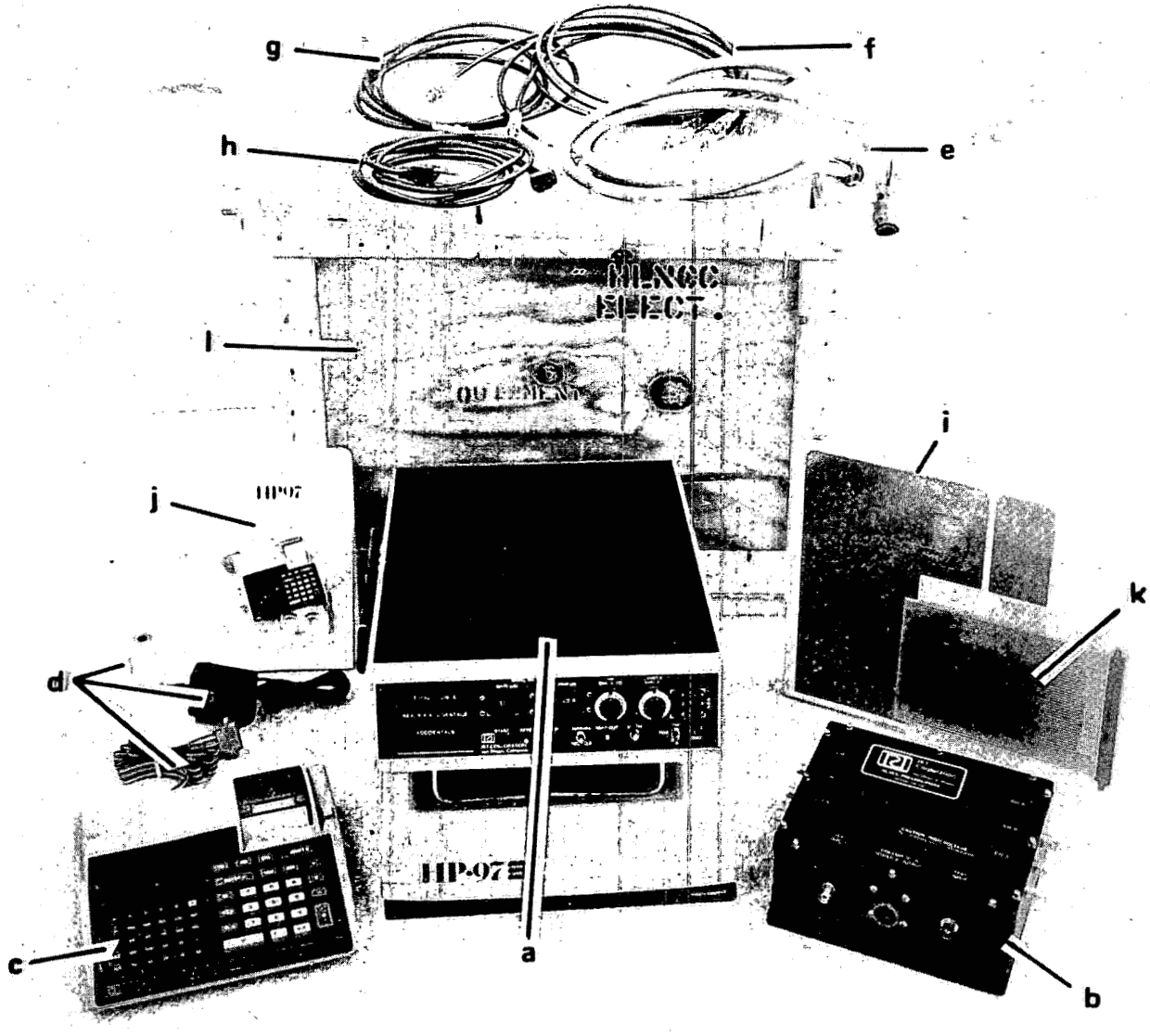

Fig. 1.
Major HLNCC components and accessories as received, from manufacturer.

a. HEC-100 counter/controller
b. HP-100 high-voltage junction and preamplifier box
c. HP-97 calculator (modified)
d. HP-97 accessories (attached interface cable, recharger, paper tape)
e. HEC-100/HP-100 interconnecting cable
f. HP-100/HEXAPUS (detector) high-voltage cables
g. HEC100/HP-100 high-voltage supply cable
h. ac power cord
i. Manufacturer's HLNCC manual
j. HP-97 User's Manual
k. Extender board
l. Shipping crate

B. HEC-100

1. Remove top cover from HEC-100. Release clamp at rear of board assembly.
2. Rotate and lock board assembly in vertical position (Fig. 2).
3. Remove boards. Boards (from front to back) are amplifier board, shift-register board, and microprocessor board (Fig. 2).
4. Inspect boards for cleanliness, good solder connections, and missing components.
5. Check the following shift-register board components (Fig. 3):

Component	Should Be
C5	68-120 pF
C22	220 pF

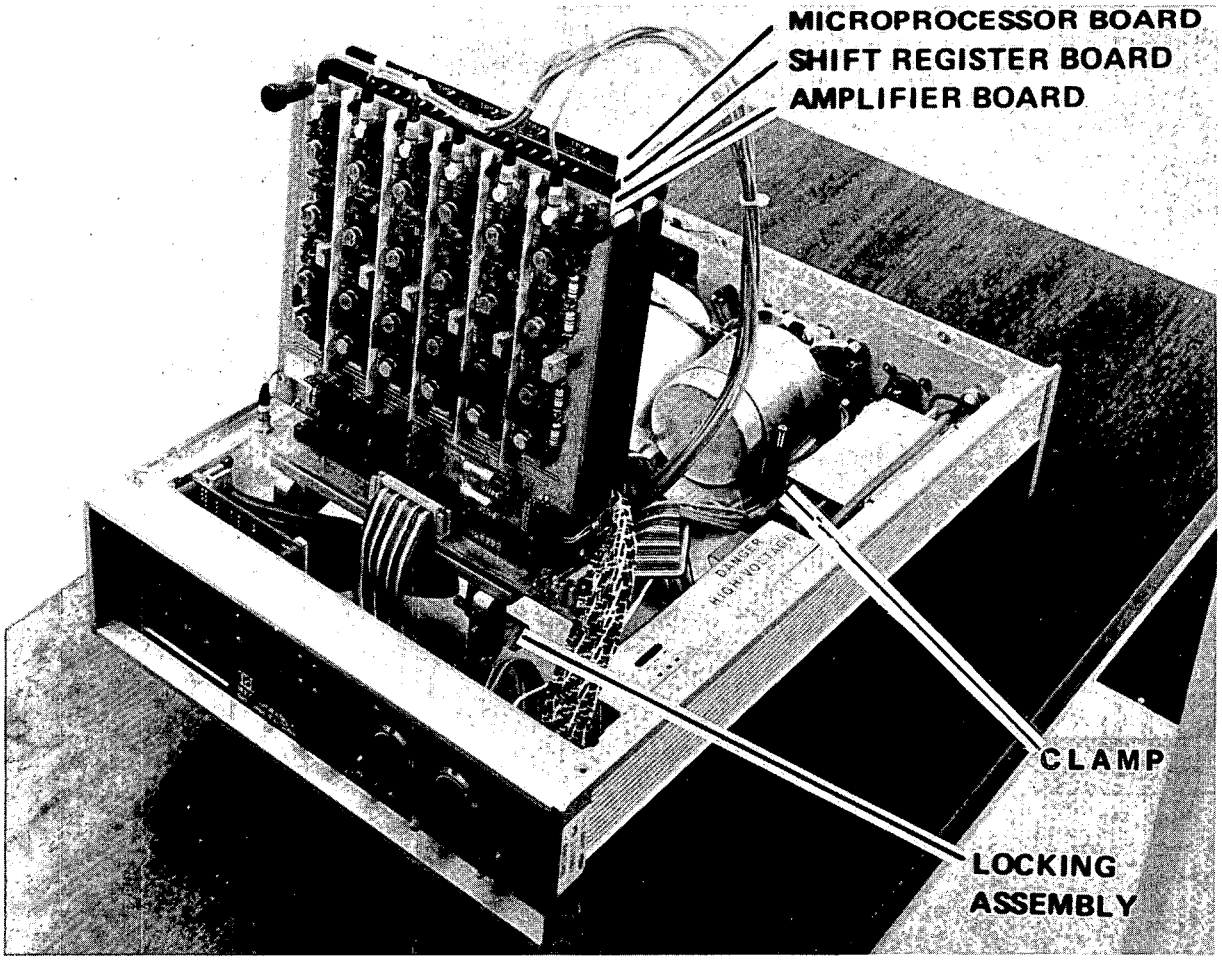

Fig. 2.
HLNCC with boards in upright locked position.

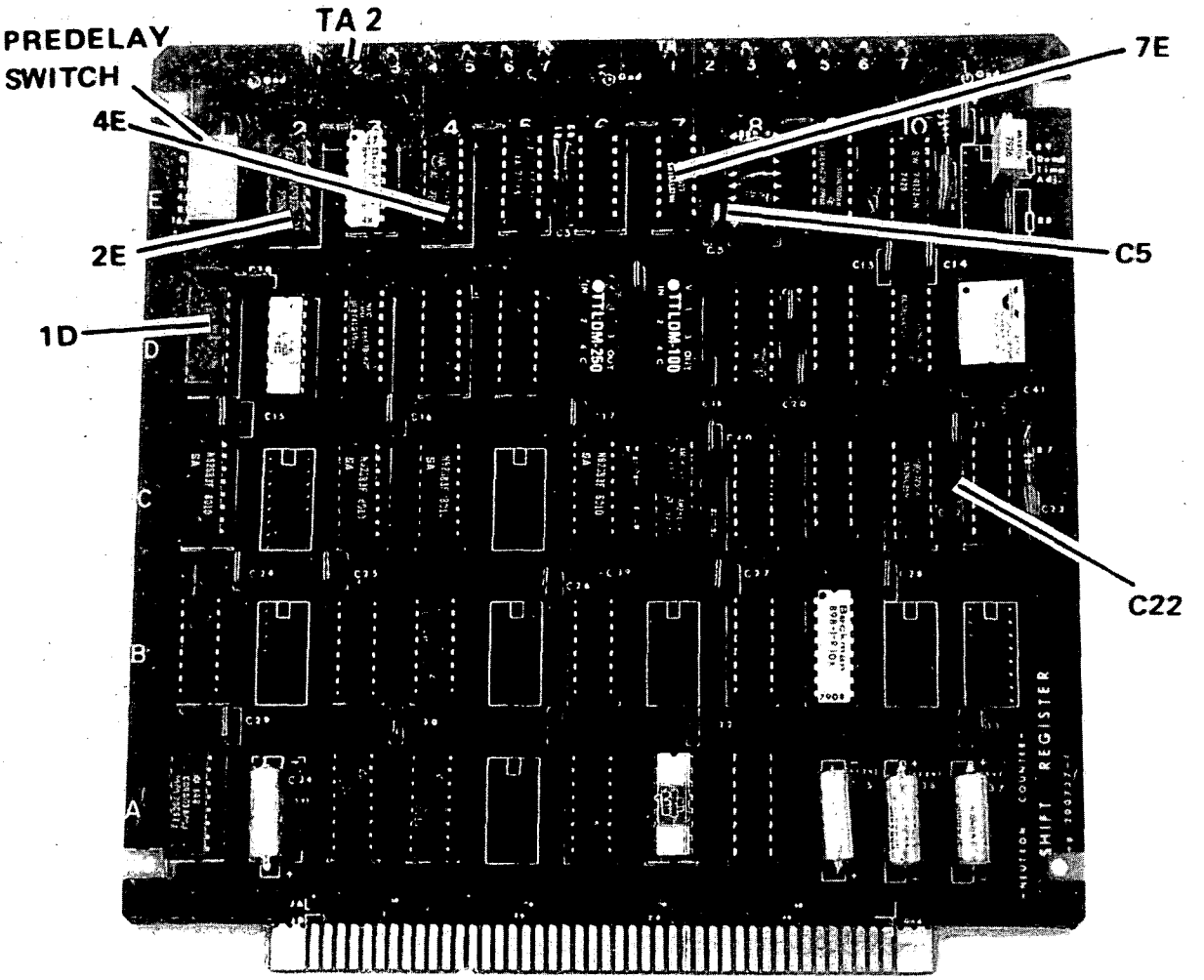

Fig. 3.
Shift-register board.

7E (chip location)	Texas Instrument 74LS74
4E (chip location)	Motorola MC14557 AL or BAL (not CP)
2E, 1D (chip location)	Motorola MC14517 AL or BAL (not CP)

6. Check microprocessor clock (microprocessor board location 5E) frequency label; clock frequency must be 921.6 kHz.
7. Check the chassis interior for loose or missing screws and components.
8. Check the front and rear panels for loose or missing controls and components.
9. Reinstall the amplifier, shift-register, and microprocessor boards.

   NOTE: Use caution in inserting boards because socket pins are easily bent.

10. Check continuity from front panel ground test point to rear panel "AMP INPUT" (J15) pins G and F.

C. HP-100 Preamplifier Box

CAUTION: High voltage may be present inside the box when disconnected from high-voltage supply; there is no high-voltage bleeder resistor in the box. If it is necessary to connect and operate the box with the cover removed, caution must be taken.

1. Remove top cover from HP-100 (preamplifier box) (Fig. 4).
2. Short the high-voltage input connector (SHV) on the HP-100 preamplifier box to ground while working in the box interior (see preceding cautionary note).

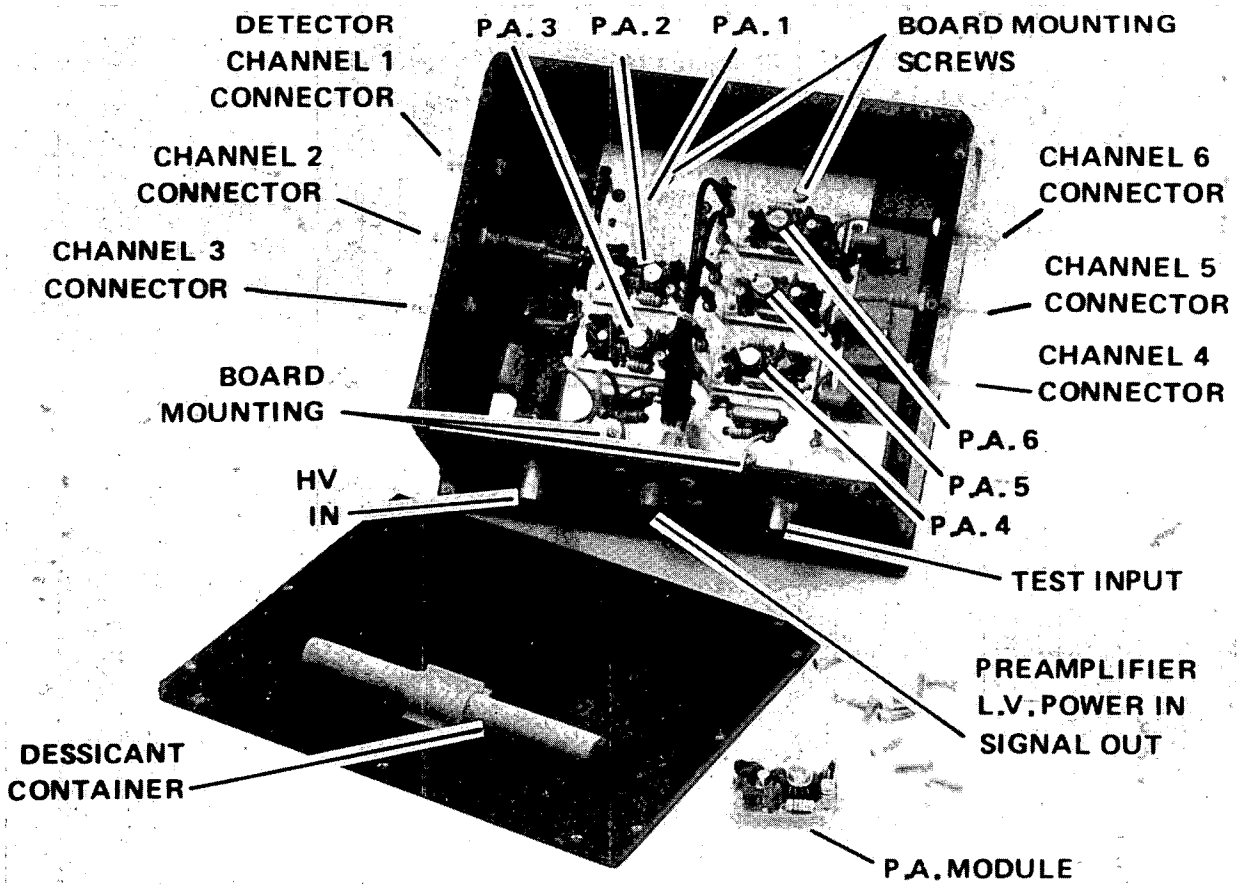

Fig. 4.
High voltage junction and preamplifier box, HP-100.

3. Check for (solder flux) residue on preamplifiers and main board; boards must be clean.
4. Check main board mounting screws and box connectors (Fig. 4) for looseness; check to see that preamplifiers are seated firmly.
5. Check for continuity from main board ground plane to connector shells.
6. Check desiccant for appropriate color (deep blue) and replace/reactivate, if necessary.
7. Reinstall plastic foam keeper(s) and box cover.

D. Accessory Cables

1. Check the power cord for electrical and mechanical integrity.
2. Check grey (multiconductor) cable assembly strain reliefs and ground lugs.
3. Check high-voltage cables for proper connector assembly (SHV) and cable type.

Cable	Type
High-voltage supply cable	RG59 or RG71
High-voltage detector cable	RG71

III. DIGITAL SECTION CHECKS

There are seven procedures to test the digital section of the HEC-100. The following are the major features tested:

- power supplies, HP-97, data transmission, and display;
- input synchronizer and TOTALS (T) scaler;
- reals + accidentals (R+A) and accidentals (A) gate functions and scaling;
- scaler display;
- timer;
- predelay function;
- accidental gate delay shift register.

The coincidence circuitry test relies heavily on the use of a random pulse generator and correctly interpreting the resulting data. Periodic sources, while useful, are inadequate for testing the R+A and A-coincidence gates. Data

generated during the test should be recorded and logged for future reference; a brief HP-97 program is provided in Sec. III.A for recording HEC-100 display data. A second, more comprehensive test program referred to in Sec. III.E is found in Appendix A, page 33.

The following test equipment is used in the digital section checks (Fig. 5).

Tektronix TM506 (mainframe)
Tektronix SC504 oscilloscope (module)
Tektronix PG508 pulse generator (module)
Tektronix DC503A counter (module)
Tektronix DM502A DVM (module)
Los Alamos/Q-1 RP501.

A. Initial Setup and Power-On Check

This procedure provides initial tests of the power supplies, HEC-100 display, and microprocessor board. Two versions of resident (microprocessor) software are available for the HEC-100 (PROM chip location E2, microprocessor board). At power-on or microprocessor RESET, the software will transmit a test

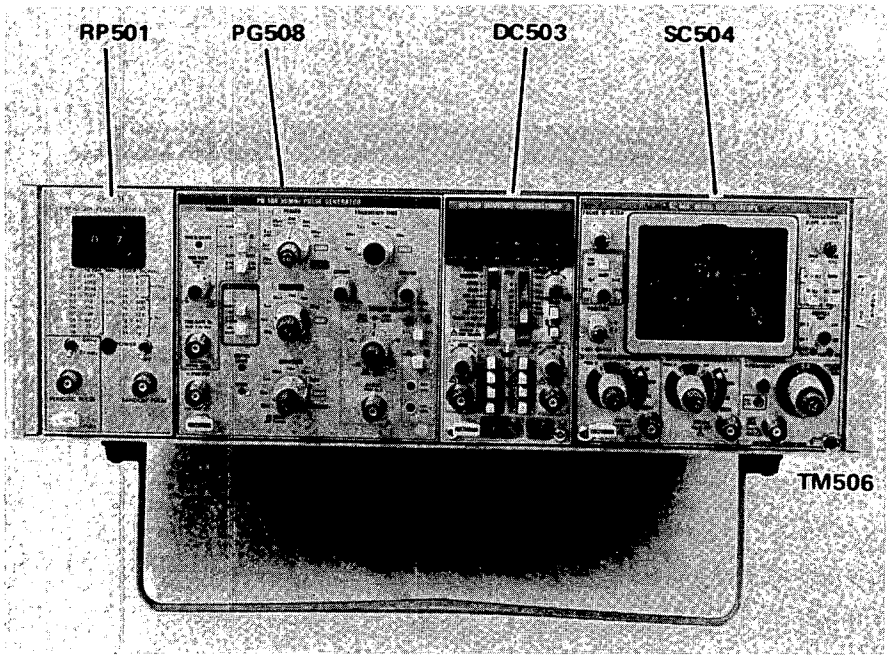

Fig. 5.
Digital section test set.

message to the HP-97; the message consists of simulated scaler data (TIME, TOTALS, R+A, and A), which are loaded in HP-97 registers 1 through 4, followed by an "A" command that will start an HP-97 program at "LBLA." A test message message occurs on the RS232 port at power-on/microprocessor RESET, if the original software is resident. Below is a table of test messages.

	HP-97 MESSAGE	RS-232 MESSAGE
VERSION 1.2	444444	HLNCC
(original version)	3333333333	V 1.2
	2222222222	12 JUL 78
	1111111111	
	1111111111	
VERSION 2.1	543210	(NONE)
(remote control	9876543210	
version)	9876543210	
	9876543210	
	0	

The following are the RS-232 port requirements for a remote receiving device:

DATA RATE	300 BAUD
BITS/CHARACTER	7
STOP BIT	1
PARITY	EVEN
MODE	FULL DUPLEX for V 2.1; HALF DUPLEX (receive only) for V 1.2

1. HEC-100 initial conditions (Fig. 6).

LINE VOLTAGE SWITCH	(REAR PANEL)	110 or 220 (Vac)
POWER	(FRONT PANEL)	OFF
HV	(FRONT PANEL)	OFF
POWER CORD		UNPLUGGED

2. Measure continuity from power-cord ground to the HEC-100 chassis before connecting to ac power.

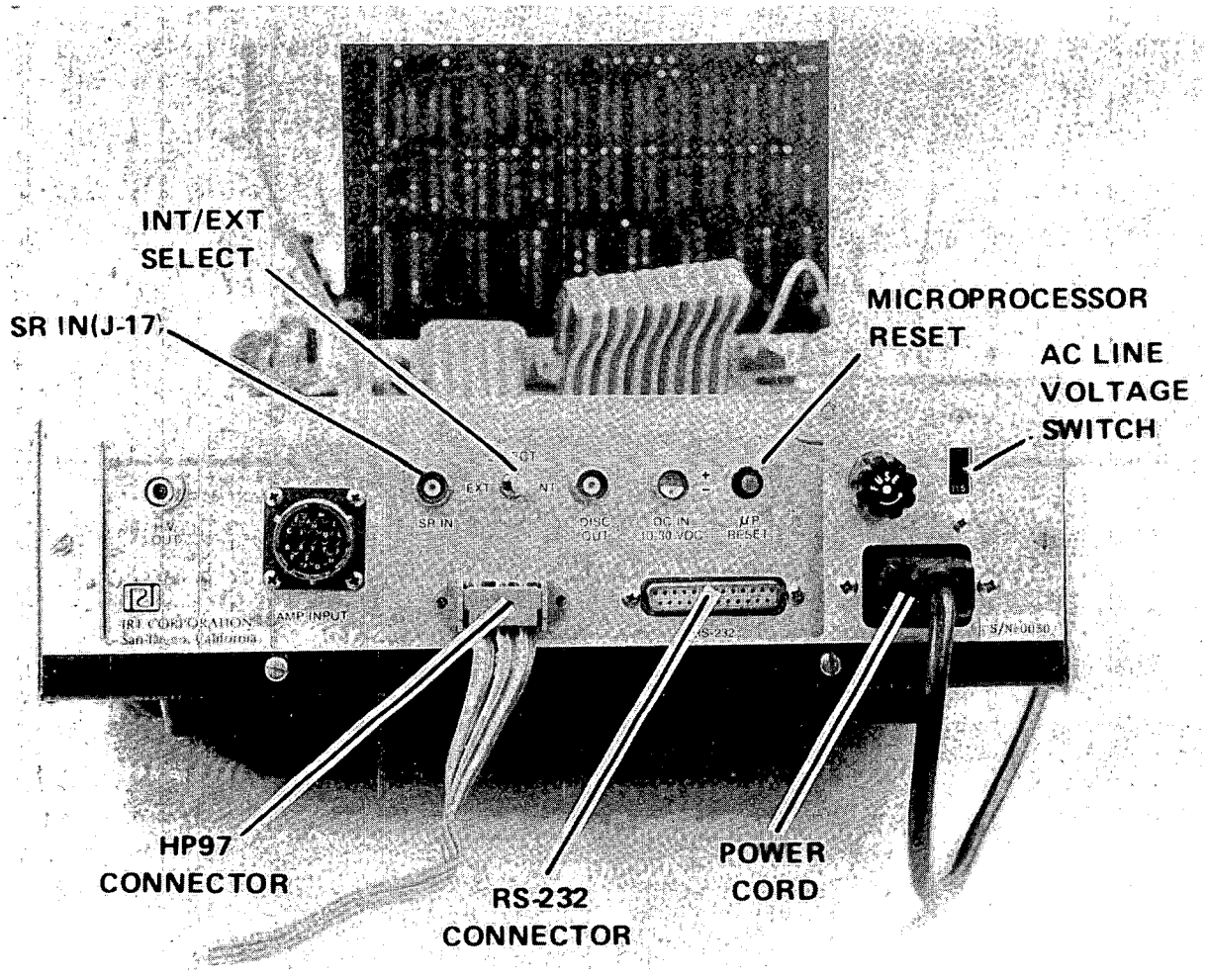

Fig. 6.
HEC-100 rear panel.

3. Connect HP-97 to HEC-100 (HP-97, J-14, rear panel).
4. Connect HP-97 to charger.
   NOTE: Do not run HP-97 without charger when it is connected to HEC-100.
5. HP-97 initial conditions.

POWER	ON
RUN/PROGRAM	PRGM
MAN/TRACE	MAN

6. Enter the following program into the HP-97:

```
LBL A
FIX
DSP 0
```

RCL 1
PRINT X
RCL 2
PRINT X
RCL 3
PRINT X
RCL 4
PRINT X
RCL 3
RCL 4
- (Subtraction)
PRINT X
f SPACE

7. Switch HP-97 from PRGM to RUN.
8. Turn on HEC-100 power. Observe that during test transmission the HEC-100 readout light is on, that the HP-97 prints a valid test message, and that the HEC-100 display shows zeros in the two least significant digit positions.
9. Measure between front panel controls and screws and ground-test point for extraneous power supply voltages (±15 V, ±12 V, 5 V); presence of voltage indicates wiring error.
10. If a low-voltage dc power supply failure appears to have occurred, the voltages may be measured on the "mother board" (as indicated on Fig. 7).

B. Input Synchronizer Check

This check tests synchronizer circuit performance. This circuit synchronizes input pulses to the HEC-100 clock. C5 is selected to minimize synchronizer deadtime and prevent loading of an input pulse into adjacent clock cycles. The check verifies that C5 is greater than the minimum value necessary to prevent double pulsing and also tests TOTALS scaling and timer operation.

1. HEC-100 setup.

TIME (s)	1×10^{1}	(front panel)
MANUAL/RECYCLE	MANUAL	(front panel)
SELECT	EXT.	(rear panel, SW 10)

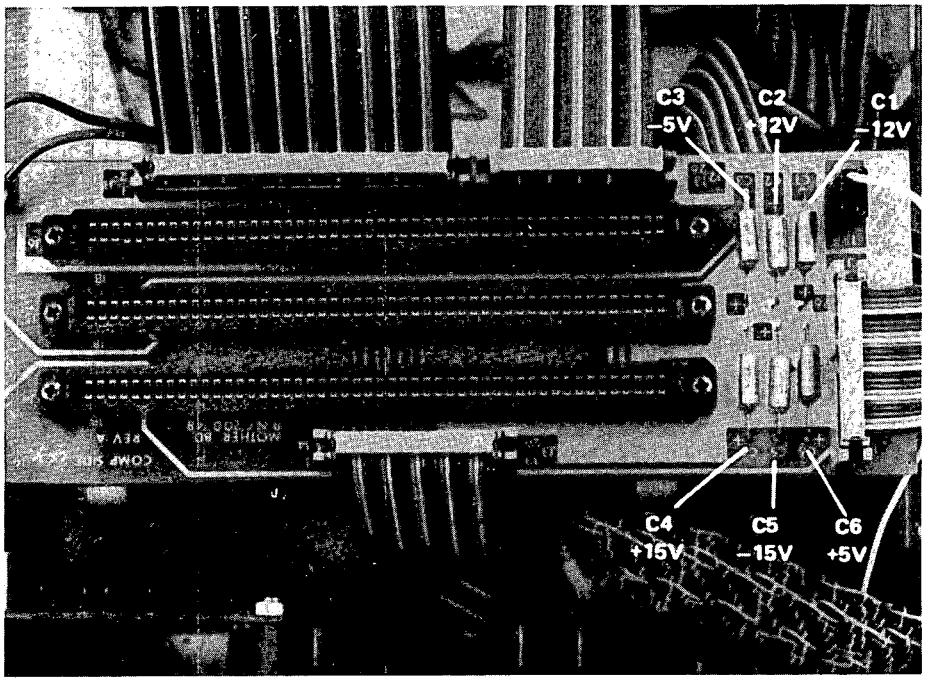

Fig. 7.
HEC-100 mother board: low-voltage dc power supply test points.

2. Los Alamos/Q-1 RP501 module setup.
   PERIODIC PULSE sw. 0.1 MHz
3. Connect RP501 "PERIODIC PULSE" BNC to HEC-100 "SR IN" (J-17)(Fig. 6.
4. Start the HEC-100 (depress RESET push button, then START push button).
5. Observations at completion of run.

SCALER	DISPLAYED VALUE	COMMENTS
TOTALS	1000000 (counts)	±100 counts
COUNT TIME	10 (seconds)	--

C. Scaler Check

This check tests that the nine digits of the TOTALS, R+A, and A scalers count and display. Reconnect "SR IN" (J-17) to the RP501 "RANDOM PULSE" output. Switch the Los Alamos pulser to 00 and start the HEC-100. Count for a sufficient period of time to observe count accumulation in all digits of the three scalers.

D. Timer Check

This check tests that the HEC-100 TIME switches properly control timer operation.

1. Set the HEC 100 TIME to 0 x 10° and press the START push button. The HEC-100 should immediately switch to STOP and the displayed time should remain at 0.
2. Set the HEC-100 TIME to 1 x 10°.
3. Start the HEC-100 and observe that it stops at and displays the set time.
4. Repeat for 2 x 10° through 9 x 10°.
5. Repeat for 1 x 10^1, 1 x 10^2, and 1 x 10^3. (Check 10^4 and 10^5 setting if time allows).

E. Gate and Adder Check

This check tests the HEC-100 coincidence circuit consisting of the shift-register gate, gate length selector, gate up/down counter, R+A and A gate adders and latches, and associated logic. It also provides testing of R+A and A scaling and additional testing of the TOTALS scaler, timer, synchronizer, and HP-97 operation.

HEC-100 coincidence data are ultimately reduced to the difference between the R+A and A scalers. When the instrument is checked with a random (non-fissioning) source, the difference should be zero $\pm\sqrt{2A}$ (1σ) and any consistent offset is bias. For a random source, bias is defined as $\{[(R+A)-A]/A\} \times 100$, a percentage quantity that may be positive or negative. A properly functioning instrument should have a measured bias of 0.01% or less.

A Los Alamos developed random pulser[7] (module RP501) is used in this check. Tests have shown that its effect on the HEC-100 digital section closely matches the predicted effect of a true random source. About 3% rate difference between the pulser setting and the TOTALS scaler will be observed at 128 kHz because of the input synchronizer 0.5-μs deadtime.

Enter the HP-97 program referenced in this check and listed in Appendix A, page 33. Its purpose is to expedite a go/no-go decision by reducing the data variance to a level less than or equal to ±10. Ten lines of numerical data are printed.

Lines 1 through 5: Raw scaler data [TIME, TOTALS, R+A, A, and (R+A)-A].

Line 6 : Gate width calculated from TIME, TOTALS and A.

Lines 7 through 9: Percentage deviations of the measured data rates from a random-pulser-based reference rate expressed in tenth per cent units.

Line 10 : A Reals vs Reals-error figure expressed in units of sigma (σ).

This program requires a minimum count TIME setting of 1×10^2 s.

1. Change random pulser setting to 07 (128 kHz).
2. HEC-100 setup.

TIME	1×10^2	(front panel)
GATE	8 μs	(front panel)
MANUAL/RECYCLE	MANUAL	(front panel)

3. Start the HEC-100. When HEC-100 stops, press READOUT to print the result (NOTE: The printout will not correspond to the sample printout below if the Appendix A program is not entered). Acquire and print several counting intervals if time allows.
4. The following is a typical example of the results printed on the HP-97 (8-μs gate).

HP-97 Printout	Quantity	Tolerance/Comment
100	COUNT TIME (t_c)	Should agree with TIME setting.
12441158	TOTALS (T)	Should agree with TOTALS display.
12388376	R+A	Should agree with R+A display.
12380938	A	Should agree with A display.
7438	(R+A)-A (R)	$\sim \pm\sqrt{2A}$
(space)		
8	GATE WIDTH (t_g)	Should agree with GATE setting.
(space)		
0	D_T*	0 ± 5 (tenths per cent)
0	D_{R+A}*	0 ± 10 (tenths per cent)
-1	D_A*	0 ± 10 (tenths per cent)
1	D_R*	0 ± 3 (units of sigma)

*Refer to Appendix A for detailed description.

5. Repeat 3 and 4 for the other GATE settings. R+A and A should increase in proportion to the GATE setting, and the calculated gate width (t_g) should agree with the GATE setting.

F. Predelay Check

This check tests the predelay circuitry that provides a delay between the R+A strobe and the R+A gate. The delay is necessary to prevent amplifier dead-time from effectively shortening the R+A gate. The predelay is produced by a variable length (64-stage) shift register and is set by a binary-coded switch mounted on the shift-register board. Each predelay shift-register stage equals 0.5-μs delay. There is an internal fixed 1-μs offset that is added to the switch setting. Total predelay (in μs) = (sum of open switch settings) + 1.

The predelay is measured by putting a pulse pair into the instrument input, observing the appearance of counts in the R+A scaler as the second pulse is slowly separated from the first, and measuring the time delay between the two pulses in clock-cycle (0.5 μs) increments at the synchronizer output (TA2, shift-register board). This measurement will be facilitated by aligning the pulse leading edge transitions with the oscilloscope graticule lines. The accidental scaler may be ignored during this check.

1. PG508 pulser setup.

MODE	DOUBLE PULSE (delay and undelay push-button switches IN)
DURATION	0.1 μs (CALIBRATED)
DELAY	<1 μs
PERIOD (rate)	0.1 ms (50% UNCALIBRATED)
OUTPUT (volts)	+3 to +5 V

Check pulse pair on scope (Fig. 8).

Connect the pulser output to HEC-100 "SR IN" (J 17).

2. SC504 oscilloscope setup.

VERTICAL	2 V/div.
HORIZONTAL	0.5 to 2 μs/div.

Connect oscilloscope probe to TA2 (shift-register board)(Figs. 9 and 10).

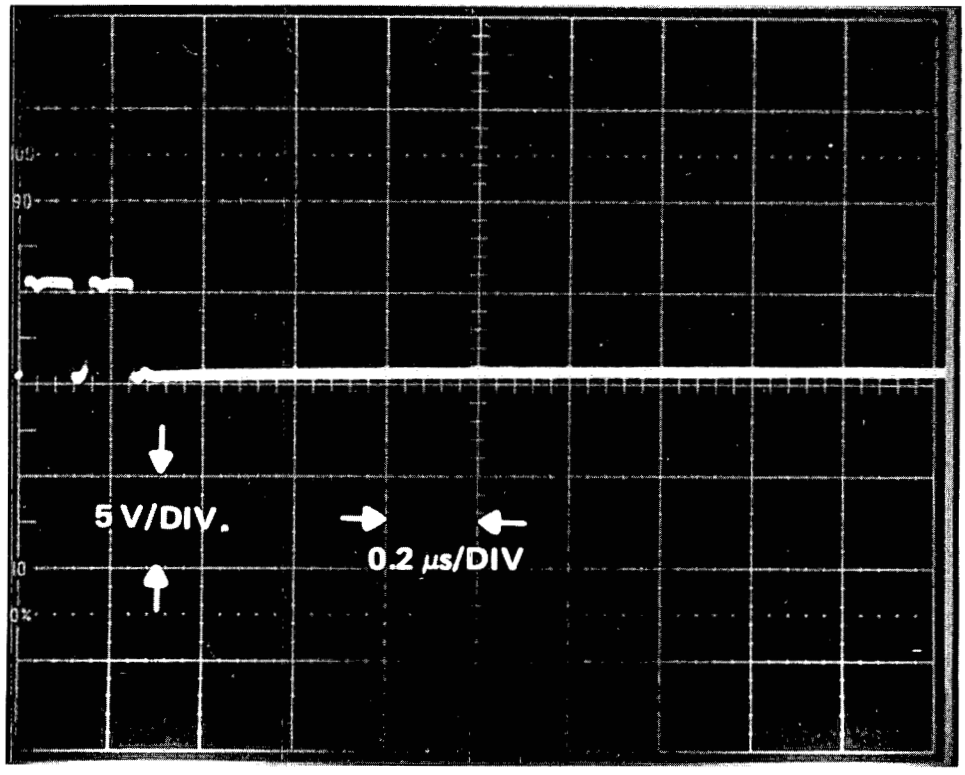

Fig. 8.
Predelay check step 1; PG508 output.

3. HEC-100 setup.

TIME	Arbitrarily long initially
MANUAL/RECYCLE	MANUAL
PREDELAY	All closed (initially) (shift-register board)

4. (a) START HEC-100.
   (b) Slowly increase PG508 "DELAY" until R+A scaler just begins to count.
   (c) The delayed pulses should now begin to fall in the third 0.5-μs cycle (Fig. 11).
5. (a) Increase the delay until all delayed pulses fall in the third or fourth cycle (Fig. 12).
   (b) Set HEC-100 time to 1 x 10° s.
   (c) Restart HEC-100 and count for 1 s.
   (d) Observe that Totals = 2(R+A) precisely.
   (e) This tests the 1-μs internal minimum predelay.

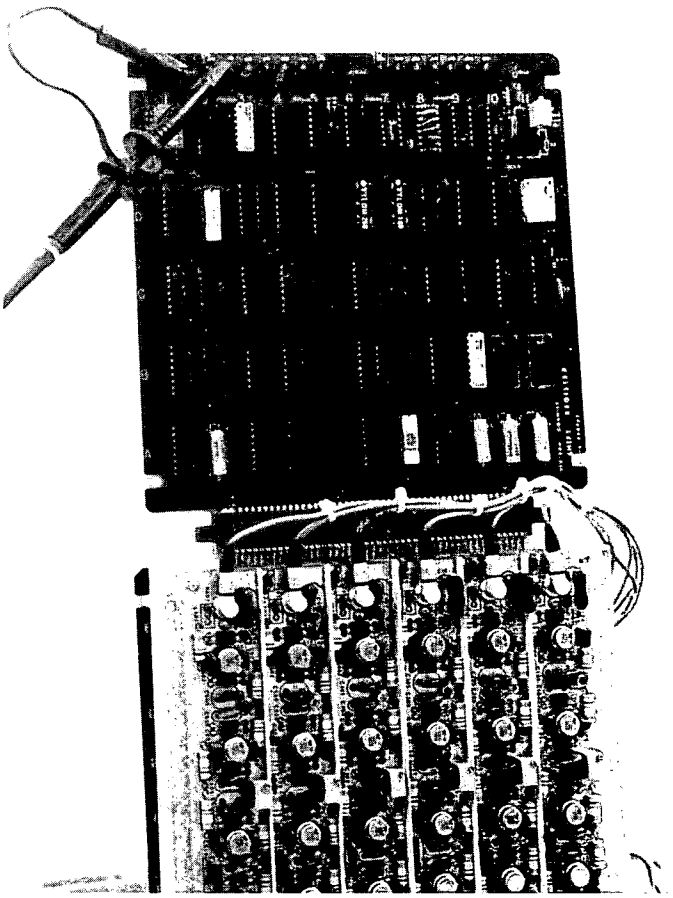

Fig. 9.
Predelay check step 2: SC504 connected to TA2.

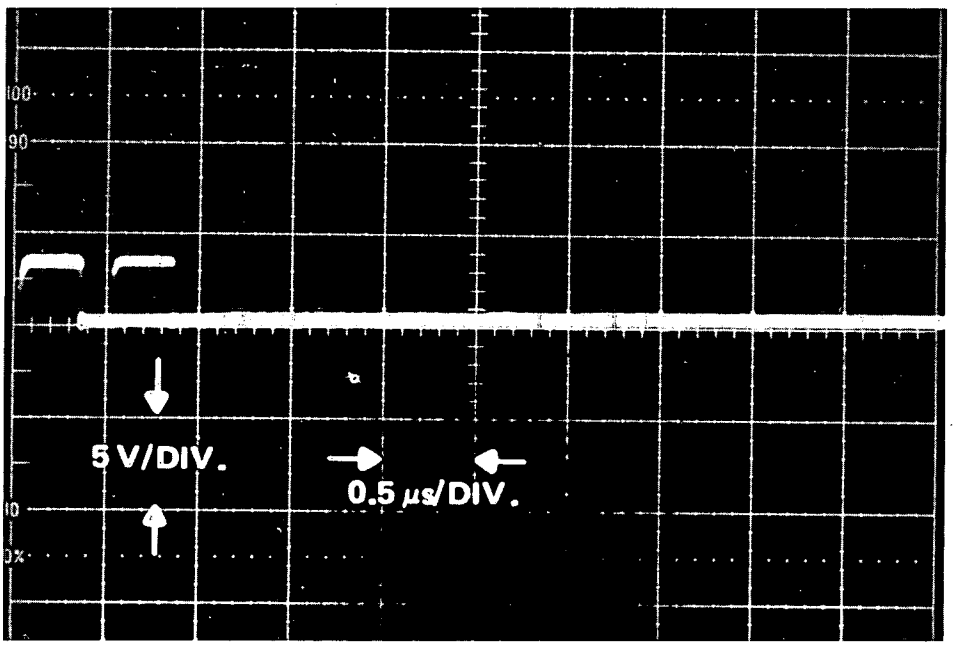

Fig. 10.
Predelay check step 2: synchronizer output at minimum predelay; no R+A counts.

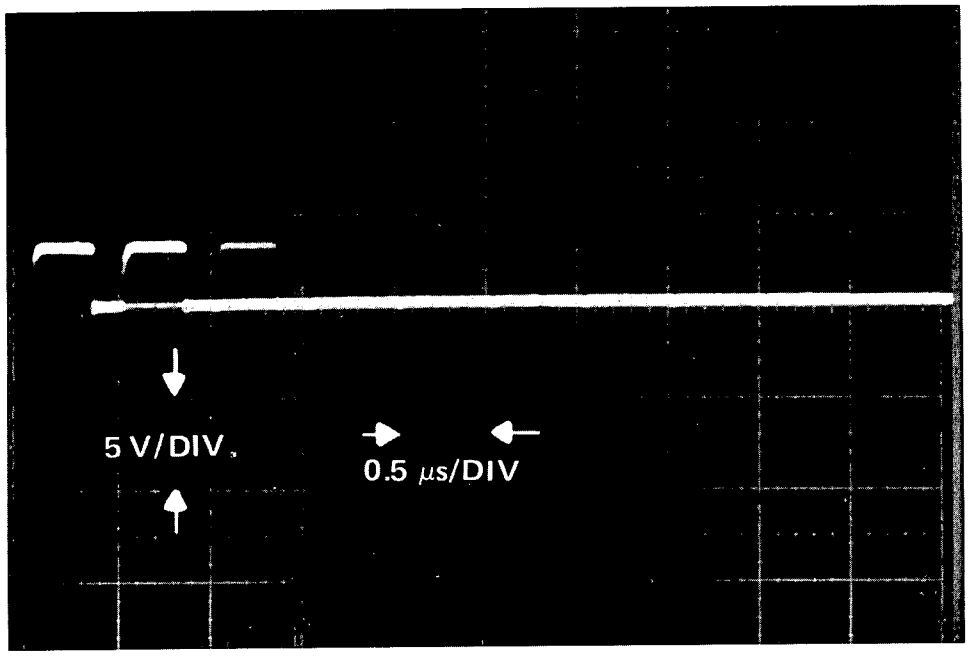

Fig. 11.
Predelay check step 4(c): synchronizer output at slightly increased delay; R+A scaler starting to count.

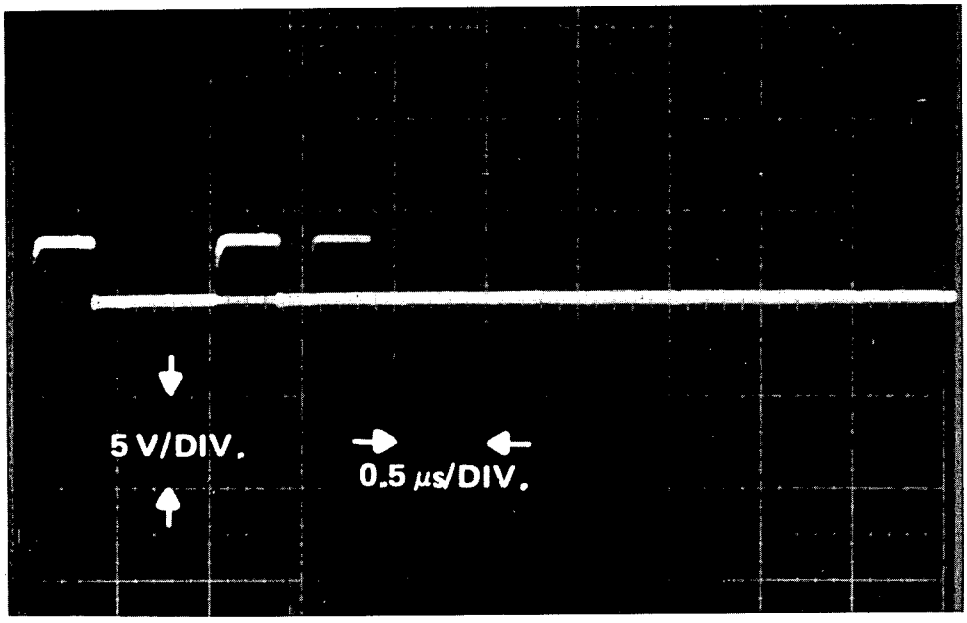

Fig. 12.
Predelay check step 5(a): synchronizer output with all delay pulses in third/fourth clock cycle; R+A count equals one-half totals count.

6. Repeat steps 4 and 5, opening the predelay switches (0.5 to 16 μs) in turn and increasing the PG508 delay to satisfy 4(b). Further increase the delay as was done in 5(a) and observe that the condition in 5(d) is met. The increase in delay will be precisely two clock cycles per microsecond of switch setting.
7. Return the predelay switch setting to 3.5 μs for a total of 4.5 μs of predelay (Figs. 13 and 14). This completes the predelay check.

G. Accidental Delay Check

This check tests the 1024-μs delay between the R+A and A gate strobes by direct measurement. The DC503 counter/timer module is used for the measurement and the instrument input is supplied by the PG508 pulser. The HEC-100 must be counting during this test.

1. PG508 pulser setup.

MODE	Undelayed (single pulse)
PERIOD (rate)	20 ms (50 Hz)

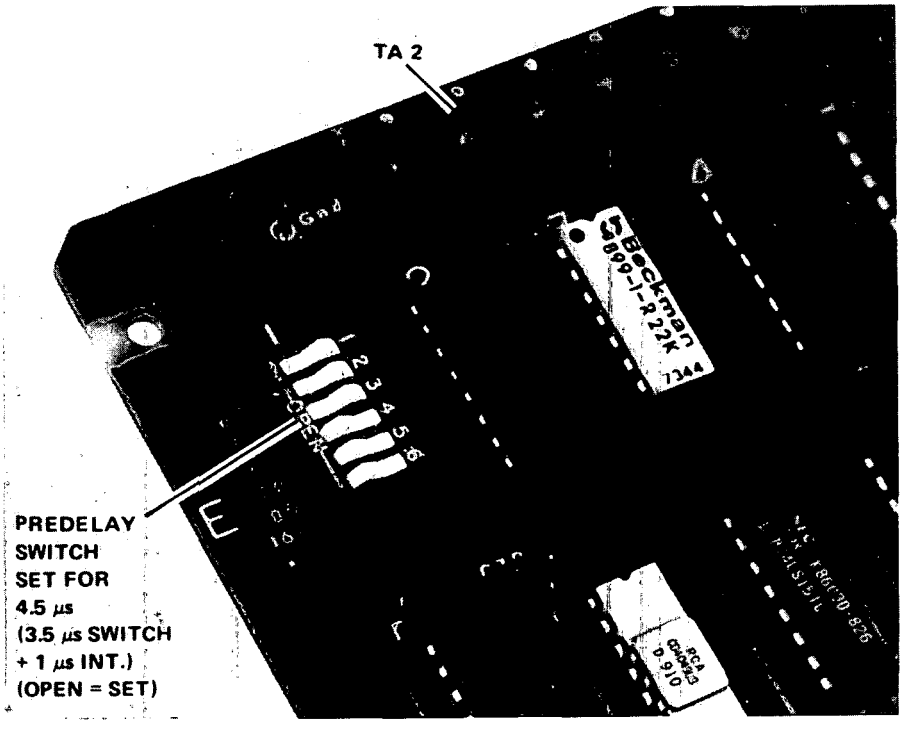

Fig. 13.
Predelay check step 7; predelay switch setting at end of predelay check.

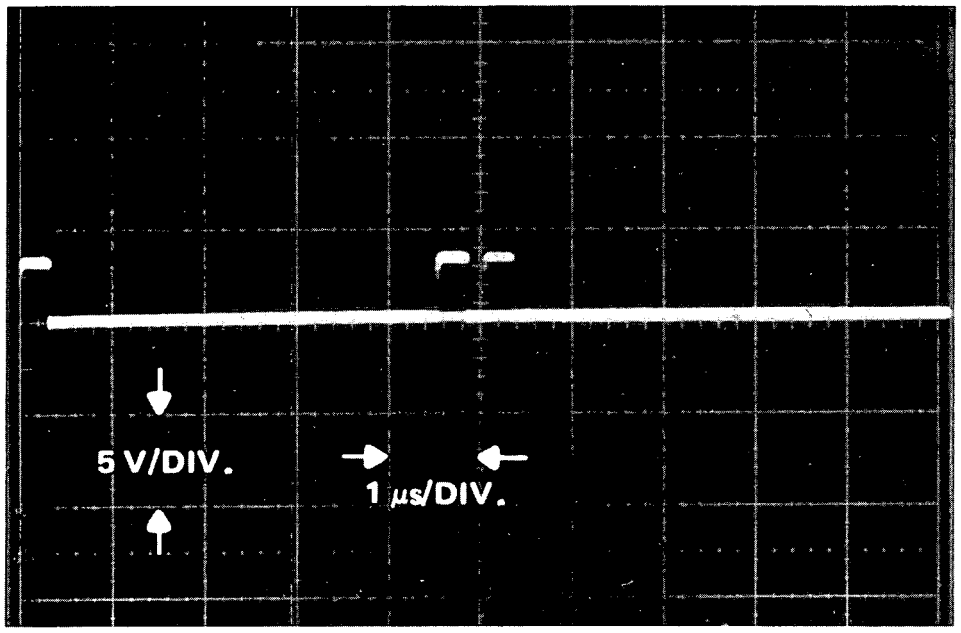

Fig. 14.
Predelay check step 7; SC504 presentation of delay pulse at 4.5 μs and predelay set for 4.5 μs..

DURATION	10 μs
OUTPUT (volts)	+3 to +5 V

Connect pulser output to HEC-100 "SR IN" (J17).

2. DC503 counter/timer setup.

FUNCTION	TIM A → B
TIMING	100 ns
Ch. A and Ch. B SLOPE	+
Ch. A and Ch. B ATTEN	x1
Ch. A and Ch. B COUPLING	DC
Ch. A and Ch. B SOURCE	EXT
START/STOP	START

Using oscilloscope probes (x1 probe, if available), connect Ch. A to TB5 (shift-register board) and Ch. B to TB7 (shift-register board).

3. START the HEC-100 (with a "long" TIME setting).
4. Temporarily switch to "freq. A" on the DC503; find the minimum (ccw) and maximum (cw) A LEVEL settings at which the DC503 properly counts (~50 Hz); set A LEVEL midway between these points. Temporarily

switch to "Period B" on the DC503 and set B LEVEL using the same procedure (measuring ~20 ms). Return the DC503 function switch to TIM A → B.

5. Observe a time interval of 1024.0 ± 0.1 μs on the DC503.

This completes the digital section checks.

IV. ANALOG SECTION CHECK-OUT AND CALIBRATION

Several procedures are detailed for testing, calibrating, and verifying the operation of the HEC-100 analog section and the HP-100 preamplifier box. The major subsections and parameters of interest are

- high-voltage power supply — voltage calibration, noise, breakdown
- detectors (6 each) — noise, breakdown
- preamplifiers (6 each) — noise, gain, pulse shaping
- amplifiers (6 each) — noise, gain, pulse shaping
- discriminator/OR gate — pulse timing and voltage levels

The usual practice is to calibrate and check the system as a whole. Changing any of the above elements may necessitate recalibration.

Noise control is of prime importance for proper operation of the instrument; noise problems have been a major source of instrument downtime. The following types of noise have been encountered:

- electromagnetic radiation (RFI, line transients, etc.);
- high-voltage breakdown (faulty components);
- printed circuit board surface leakage (dirty boards, humidity, etc.);
- ground loops and power supply noise.

The major sources of these problems have been improper grounding and shielding, and failures in maintaining board cleanliness. Several figures illustrating noise have been included on page 23.

Because detector sensitivity is about 1%/V, high-voltage calibration requires care.

The following test equipment (Fig. 15) is used in the analog section procedure:

Tektronix	TM506 mainframe
Tektronix	SC504 oscilloscope module
Tektronix	DM502A DVM module
Los Alamos high-voltage supply module	

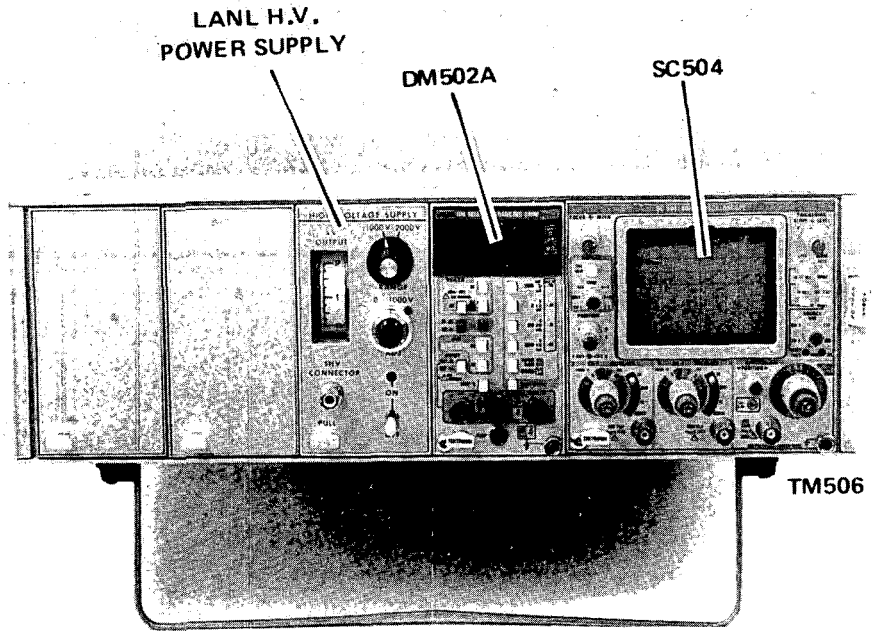

Fig. 15.
Analog section test set.

A. Setup and Mechanical Adjustment

1. With ac power (PWR sw., front panel) off, interconnect ^{3}He detector, HP-100 (preamplifier box), and HEC-100 with supplied cables.
2. Rotate HV and DISC V knobs (front panel) to minimum and observe dial reading of 0.00. If dial is not at zero, loosen the knob(s) set screw(s), set the indicator to 0.00, and retighten the set screw(s).
3. Set the HV and DISC V knobs to 7.50 (1500 V) and 3.00 (1.5 V), respectively. Switch POWER to ON. Switch SELECT (sw. 10, rear panel) to INT.

B. Noise Check

1. Using the SC504 oscilloscope, check each amplifier front panel test point. Observe that base-line noise is less than 1 V peak-to-peak (Figs. 16 and 17). Noise greater than 0.5 to 1 V peak-to-peak is usually a result of loose mounting screws in the HP-100 preamplifier box or other grounding problems.

C. Discriminator Calibration

1. Connect the DM502 (DVM) between the (front panel) DISC V test point and the ground-test point. Observe a reading of 1.500 V on the DVM.

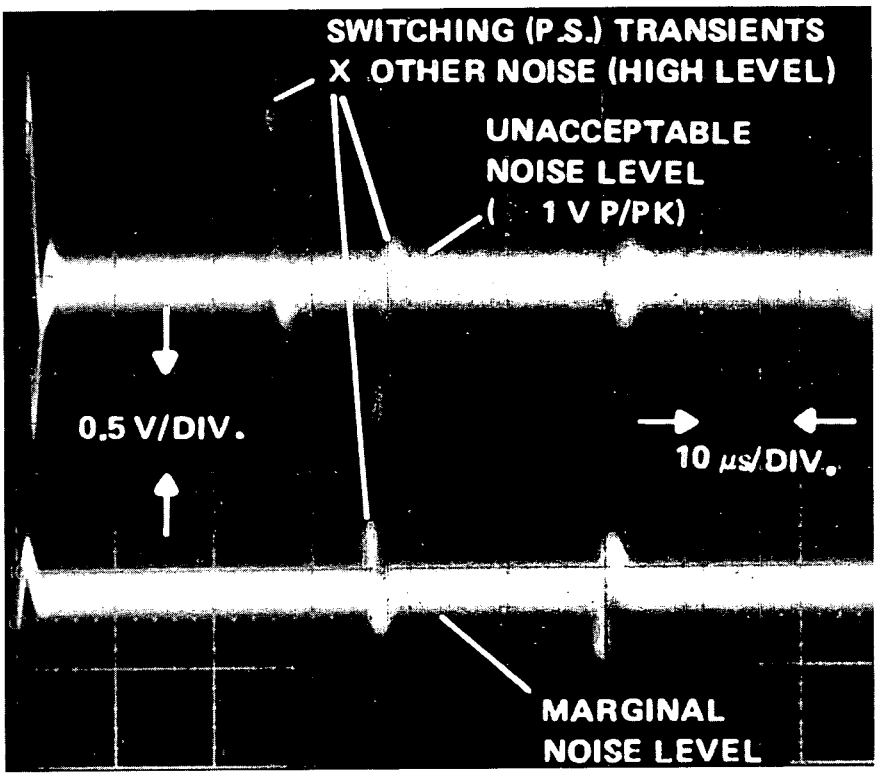

Fig. 16.
Analog check B: unacceptable and marginally acceptable noise levels.

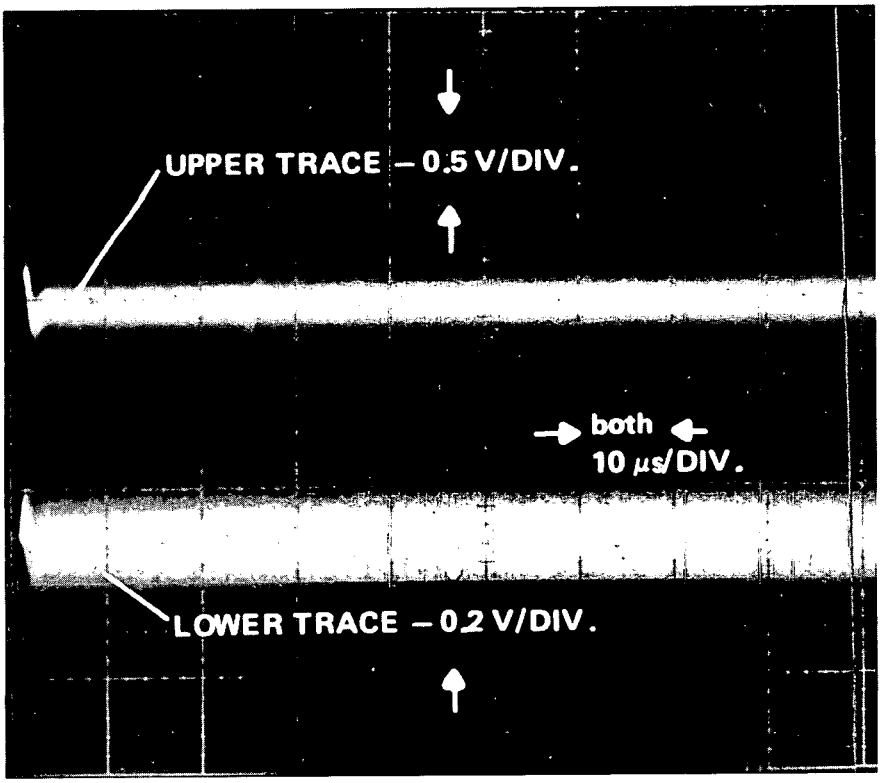

Fig. 17.
Analog check B: acceptable noise level.

If DVM reading is not 1.500 V, do step 2; otherwise, go to D.

2. Adjust R1, the forward potentiometer on the HEC-100 high-voltage supply board, for 1.500 V ± 0.001 V at the DISC V test point (Fig. 18).

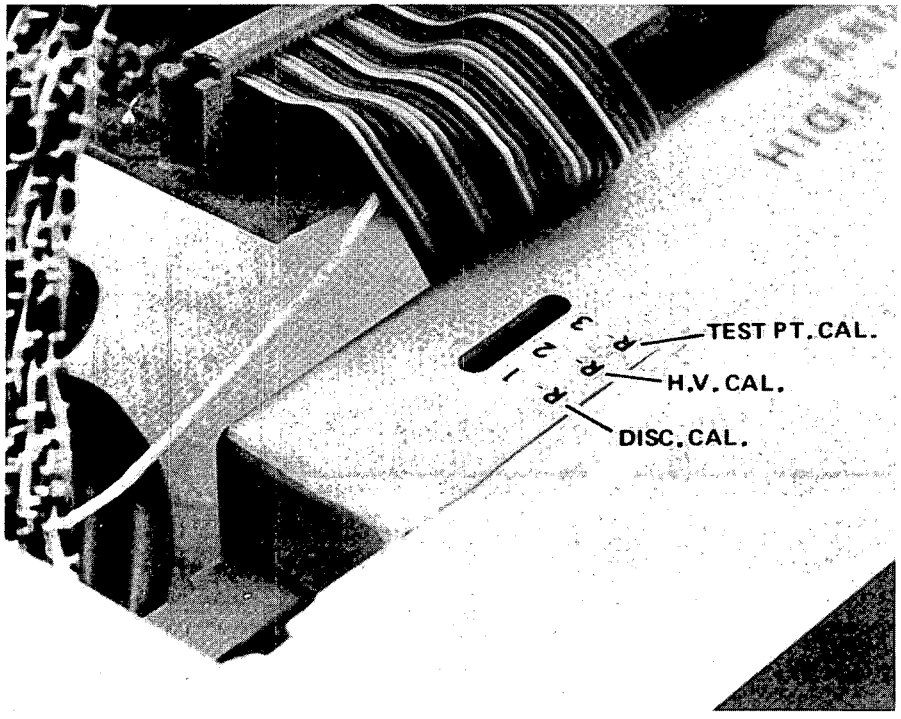

Fig. 18.
Discriminator, high voltage, and high-voltage test point calibration potentiometers.

D. High-Voltage Power Supply Calibration

NOTE: Two procedures are provided for high-voltage calibration: Procedure 1 uses a neutron source and Procedure 2 does not use a neutron source. In addition, Procedure 1 incorporates amplifier gain calibration as an integral part of the procedure, whereas Procedure 2 requires a separate gain calibration. Procedure 1 is recommended strongly as the preferred method (assuming that a source is available) because of accuracy.

Procedure 1: High-Voltage and Amplifier Calibration with Neutron Source

1. Connect Los Alamos high-voltage power supply module to HV IN on HP-100 (preamplifier box) and set to 1500 V. Switch high-voltage module on.

2. Place (neutron) source in detector.
3. Adjust pole zero potentiometers (Fig. 19) to maximum in direction that gives bipolar pulse at amplifier front panel test points (Fig. 20).

   NOTE: Maximum may be either cw or ccw, depending on the instrument. Later models have no pole zero adjustment.
4. Adjust each amplifier gain potentiometer (at midsection of analog board (Fig. 19) to center the amplifier peak pulses at 6 V (Fig. 20).

   NOTE: Observe the amplitude level carefully as it is the reference level for high-voltage calibration.

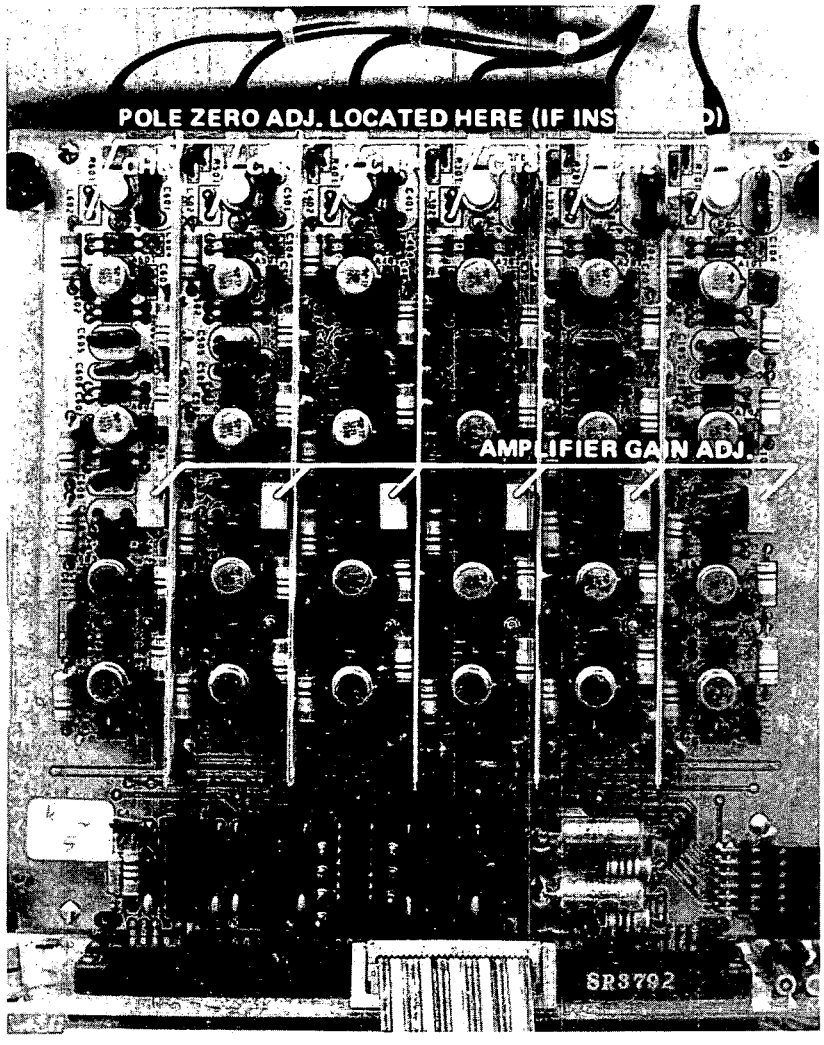

Fig. 19.
Location of gain and pole zero adjustment potentiometers (amplifier board).

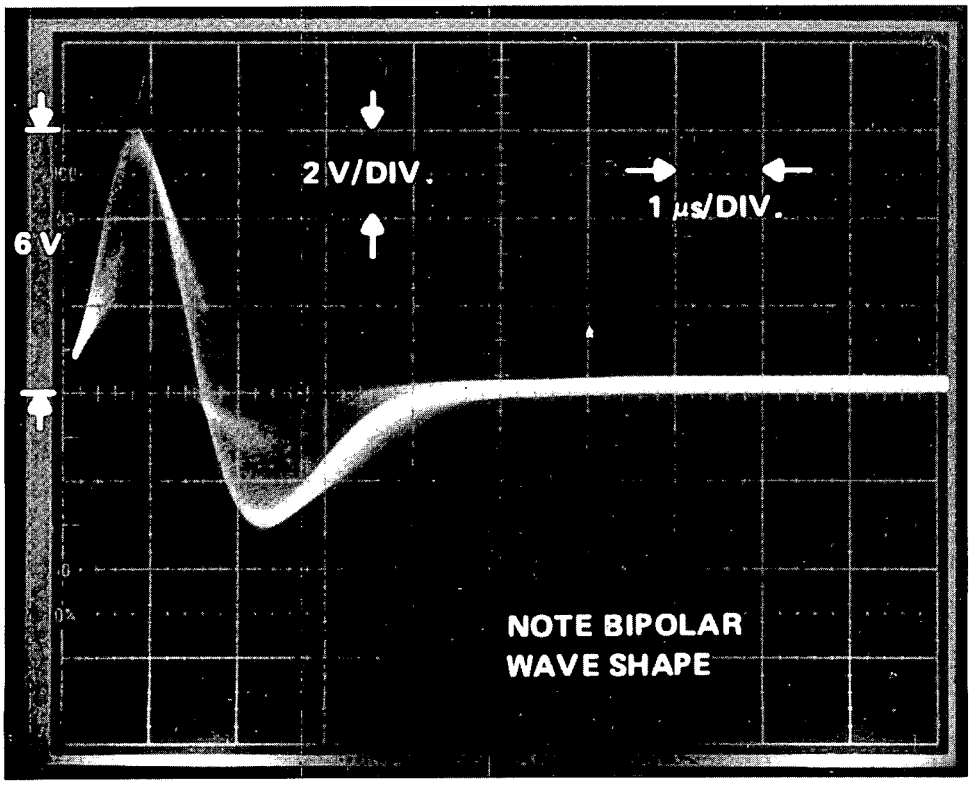

Fig. 20.
Properly adjusted amplifier output front panel test point presentation on SC504. (vertical scale = 2 v/div.)

5. Switch HEC-100 high-voltage switch ON, disconnect high-voltage cable from high-voltage module, and immediately connect it to HEC-100 HV OUT (SHV, rear panel).
6. Observe amplifier pulse level. If it has changed, adjust R2 on high-voltage board (center potentiometer, Fig. 18) to bring the level back to 6 V. Switch the high-voltage cable back and forth from the HEC-100 high-voltage output to the Los Alamos high-voltage module output several times, observing an amplifier test point and adjusting R2 until no gain change is seen. Final high-voltage connection should be from HEC-100 internal supply.
7. Connect the DM502A (DVM) to HV/1000 and ground-test points.
8. Adjust R3 on high-voltage board (rear potentiometer, Fig. 18) to give a reading of 1.500 V ± 0.001 V on the DVM.
9. Recheck gain on all amplifier channels and readjust to 6 V, if necessary. Base-line noise should not exceed 0.5 V peak-to-peak at this time (Fig. 17).

Procedure 2: High-Voltage Calibration Without Neutron Source

1. Turn HEC-100 PWR switch ON.
2. Turn high-voltage switch OFF.
3. Connect high-voltage cable from Los Alamos high-voltage module to HEC-100 HV OUT.
4. Set Los Alamos high-voltage module to 1500 V and turn on.
5. Connect DM502A (DVM) to HV/1000 (front panel) test point and ground-test point.
6. Adjust R3, on high-voltage board (rear potentiometer, Fig. 18) for a DVM reading of 1.500 V ± 0.001 V.
7. Disconnect the Los Alamos power supply from HEC-100; turn on HEC-100 HV.
8. Adjust R2 [middle potentiometer, HEC-100 HV board, (Fig. 18)] until DVM again reads 1.500 V ± 0.001 V.

Procedure 3: Amplifier Calibration Without Source

USAGE NOTE: The following procedure is not recommended for field usage at this time. Due to detector gain variations, an absolute system gain calibration is not possible using a pulser. It is possible, however, to match the gains of the 6-channel amplifier board; the gains can then be raised or lowered simultaneously by adjusting the high voltage. This method is under investigation for system calibration.

PROCEDURAL NOTE: This amplifier gain calibration is done by injecting a calibrated charge into each preamplifier input with a battery-operated pulser. It has been calibrated to provide the appropriate input for a 6-V amplifier pulse. Battery condition is determined by output pulse rate; when the rate drops to ∿2500 Hz, the battery should be replaced.

1. Turn high-voltage switch off.
2. Disconnect six SHV cables from detectors.
3. Connect six SHV cables to pulser box.
4. Connect oscilloscope to Ch. 1 "AMP" test point.

5. Adjust gain potentiometer (center of board on right-hand side) for a 6-V output.
6. Repeat 4 and 5 for Ch. 2 through 6, using the appropriate "AMP" test point and gain potentiometer.

E. One-Shot and OR Gate Check

Using either a source input or the amplifier gain calibration pulser and the SC504 oscilloscope, verify that a 150-ns transistor-transistor logic (TTL) pulse is present at TEST POINTS 1 through 7 (Figs. 21 and 22), bottom of amplifier board. TEST POINTS 1 through 6 are the individual channel one-shots and are inverted (TTL) logic; TEST POINT 7 is the OR gate output and is positive (TTL) logic.

This completes the analog section calibration and check procedures.

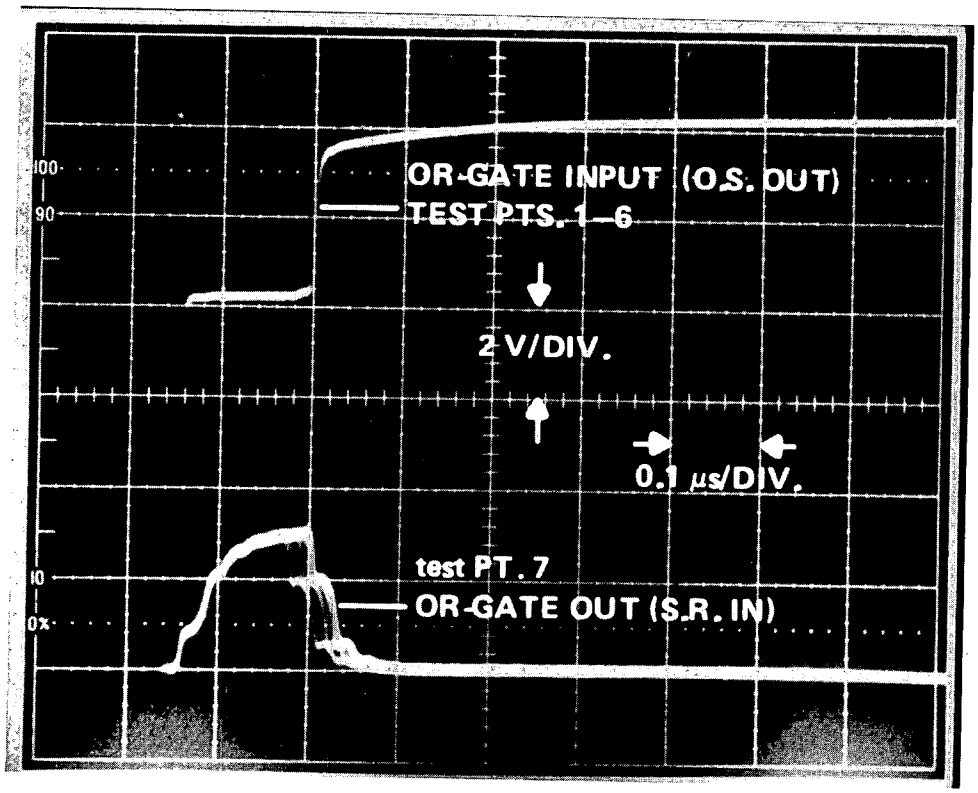

Fig. 21.
One shot and/or gate pulse presentation on SC504; amp board test points 1 through 7.

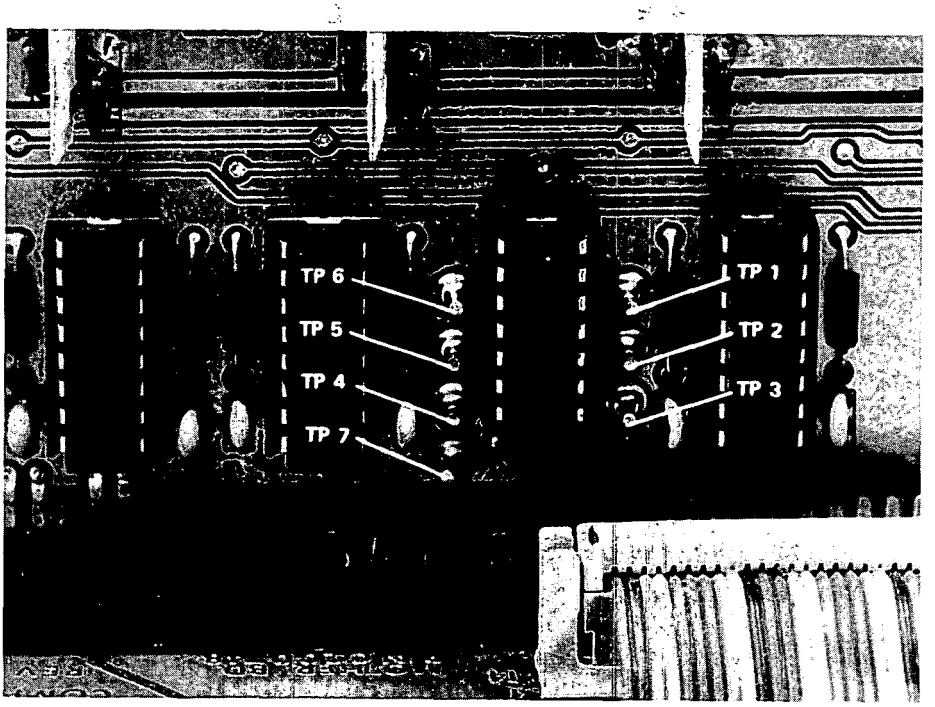

Fig. 22.
Amplifier board one shot and/or gate test points.

V. SYSTEM OPERATIONAL CHECKS

These checks should be done when possible; the results of the tests should be recorded for each system for reference (and to compare present with past performance).

A. Efficiency Check

1. For each system, using a detector complete with end caps/plugs, and with HEC-100 GATE at 32 μs and predelay at 4.5 μs, measure:
   a. background totals rate ($\dot{B}$) (no source present),
   b. totals rate ($\dot{T}$) (using ^{252}Cf source), and
   c. reals coincidence rate ($\dot{R} = (\dot{R+A})-\dot{A}$) (using ^{252}Cf source).
2. Compute $\dot{R}/(\dot{T}-\dot{B})$. This is a system efficiency measure and it should be recorded for future reference and compared with previous results (if any).

B. Bias Check

For each system, measure a (known random) AmLi source for a period long enough to determine system bias. Bias = R/A x 100. (For a 0.01% level of bias, the statistical error must be smaller than 0.01% to make the determination valid. This requires at least 1×10^9 accidental counts.) Once again, record (and compare) the test results.

C. Electromagnetic Interference (EMI) Check

Perform an EMI test using the Los Alamos supplied noise source or other source (Tesla coil, etc.). The test checks cable and preamplifier shielding integrity. It has been useful in finding faulty cables, anodizing on connector holes, etc. Basically, the test consists of attempting to induce spurious counts in the instrument by generating high levels of transient (EM) field around the instrument, particularly around the detector/preamplifier box assembly and the associated cables. At present, only comparative tests will produce meaningful results, and relatively great tolerance must be used in interpreting the results. To perform the test, start the HEC-100; move the "noise" source along each detector cable at a close distance ($\sim$1 cm) while observing a totals scaler. Ignore both R+A and A scalers during this test. Differences in induced rate, channel to channel, of less than 10 to 1 should be ignored, particularly if not repeatable. If large (repeatable) differences are observed, substitute another cable, component, or HP-100 preamplifier box in an attempt to isolate the problem. The preceding test procedure is an example; the technician may devise alternative procedures that produce useful results. It should be emphasized that the results of these procedures can be and often are ambiguous. Practice will improve the technician's ability to determine whether the results indicate a real problem and to determine the appropriate corrective action.

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4. John E. Foley, "Field Manual for the High Level Neutron Coincidence Counter (HLNCC)," Los Alamos Scientific Laboratory draft report (February 1979). This document is available from Los Alamos Group Q-1.

5. W. F. Lindsay, "Instructions for Use of High Level Neutron Coincidence Counter" International Atomic Energy Agency report IAEA-IMI #29 (Vol. 1, September 1980; Vol. 2, April 1981).

6. J. Swansen, P. Collinsworth, and M. Krick, "Shift-Register Coincidence Electronics System for Thermal Neutron Counters," Nucl. Instrum. Methods 176, 555-565 (1980).

7. J. Swansen, "A Digital Random Pulser for Testing Nuclear Instrumentation," Nucl. Instrum. Methods 188, 83-91 (1981).

APPENDIX A

RP501 GATE AND ADDER TEST PROGRAM

This program, in conjunction with the RP501 random pulser, provides a method for rapid testing of the TOTALS, R+A, and A counting, and the readout circuitry. To eliminate the need to interpret counting statistics, the minimum recommended counting time is 1×10^2 s.

At a thumbswitch setting of 07 (128 kHz), the RP501 should count 124461 $\pm 1\sigma$ TOTALS counts/s in a properly operating HEC-100. This reference constant (M) is already stored in the program. Measured data are compared with data that are calculated using this reference.

Shown below is an example of a printout from this program.

HP-97 Printout		Quantity	
100.	***	t_c	= count time
12441158.	***	T	= TOTALS scaler count
12388376.	***	R+A	= REALS + ACCIDENTALS scaler count
12380938.	***	A	= ACCIDENTALS scaler count
7438.	***	R	= (R+A) - A
8.	***	t_g	= $(At_c/T^2) \times 10^6$; calculated GATE WIDTH in microseconds
0.	***	D_T	= 1000[(T/M)-1]; fractional T deviation expressed in 0.1% units
0.	***	D_{R+A}	= 1000{[(R+A)/M^2 t_g(s)]-1}; fractional R+A deviation expressed in 0.1% units
-1.	***	D_A	= 1000{[A/M^2t_g(s)]-1}; fractional A deviation expressed in 0.1% units
1.	***	D_R	= $R/\sqrt{(R+A)+A}$; fractional error in R expressed in 1-σ units

Normally, the last four lines of the printout are sufficient to determine if the counter is functioning properly. The last four numbers of the printout should be 0 or within the following tolerances:

$D_T = \pm 5$
$D_{R+A} = \pm 10$
$D_A = \pm 10$
$D_R = \pm 3$

These tolerances were determined empirically from experience and are necessary to allow for the influence of capacitor C5 on the digital deadtime. If D_T, D_{R+A}, and D_A are consistently outside of tolerance, check capacitor C5 on the shift-register board first; it should have a value of 68 to 120 pF. An integrated circuit (7E) on the same board should be a Texas Instrument 74LS74.

If D_R is consistently outside of tolerance, check D_A and t_g, or D_{R+A}, to determine whether the R+A or the A scaler is counting incorrectly.

Program Listing -- GATE and ADDER Test

001	*LBLA	21 11	Reference constant (M)
002	1	01	
003	2	02	
004	4	04	
005	4	04	
006	6	06	
007	1	01	
008	STO7	35 07	Stored in R-7
009	FIX	-11	Fix display to show integers only
010	DSP0	-63 00	
011	RCL1	36 01	Printout of raw data
012	PRTX	-14	t_c
013	RCL2	36 02	
014	PRTX	-14	T
015	RCL3	36 03	
016	PRTX	-14	R+A
017	RCL4	36 04	
018	PRTX	-14	A

019	RCL3	36 03	
020	RCL4	36 04	
021	-	-45	
022	PRTX	-14	(R+A) - A
023	SPC	16-11	Space
024	RCL4	36 04	
025	RCL1	36 01	Calculate GATE width
026	x	-35	
027	RCL2	36 02	
028	x^2	53	
029	÷	-24	t_g (μs) = A $t_c/T^2 \times 10^6$
030	EEX	-23	
031	6	06	
032	x	-35	
033	PRTX	-14	Print t_g in microseconds
034	RND	16 24	
035	EEX	-23	
036	CHS	-22	Round off
037	6	06	
038	x	-35	Convert t_g to seconds, that is, t_g (s)
039	STO8	35 08	Store it in R-8
040	SPC	16-11	Space
041	RCL1	36 01	Convert measured T, R+A, and A to RATES and
042	STO÷2	35-24 02	store in R-2, R-3, and R-4, respectively
043	STO÷3	35-24 03	
044	STO÷4	35-24 04	
045	RCL7	36 07	Calculate reference "R+A" and "A" rates (with
046	RCL7	36 07	random source--they are the same)
047	RCL8	36 08	
048	x	-35	
049	x	-35	(R+A) or A = M^2 t_g
050	STO9	35 09	store result in R-9
051	RCL2	36 02	Calculate D_T = 1000[(T/M)-1]
052	RCL7	36 07	
053	GSBB	23 12	Print D_T expressed in 0.1% units

054	RCL3	36 03	Calculate $D_{(R+A)} = \{[(R+A)/M^2t_g(s)]-1\}$
055	RCL9	36 09	
056	GSBB	23 12	
			Print $D_{(R+A)}$ expressed in 0.1% units
057	RCL4	36 04	Calculate $D_A = \{[A/M^2t_g(s)]-1\}$
058	RCL9	36 09	
059	GSBB	23 12	
			Print D_A expressed in 0.1% units
060	RCL3	36 03	
061	RCL4	36 04	Calculate
062	-	-45	
063	RCL3	36 03	
064	RCL4	36 04	$D_R = R/\sqrt{(R+A)+A}$
065	+	-55	
066	$\sqrt{X}$	54	
067	÷	-24	
068	RCL1	36 01	
069	$\sqrt{X}$	54	
070	x	-35	
071	RND	16 24	Print D_R expressed in 1-σ units
072	PRTX	-14	
073	SPC	16-11	
074	SPC	16-11	
075	R/S	51	
076	*LBLB	21 12	
077	÷	-24	
078	1	01	Convert ratios of x and y to 0.1% increments
079	0	00	and print
080	0	00	
081	0	00	
082	x	-35	
083	1	01	
084	0	00	
085	0	00	

086	0	00
087	-	-45
088	RND	16 24
089	PRTX	-14
090	RTN	24
091	R/8	51

Switch calculator back to Run after entering Program. Then record program on card for future use.

APPENDIX B

NEW 1-K PROM FOR COINCIDENCE COUNTER ELECTRONICS PACKAGE

This document was produced by J. E. Swansen in conjunction with a new 1-K PROM that offers the operator of the HLNCC the capability of controlling the instrument by computer in addition to the previously used control methods, which were simple manual and recycling control modes.

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A New 1-k PROM for the Coincidence Counter Electronics Package

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CONTENTS

A NEW 1-k PROM FOR THE COINCIDENCE COUNTER ELECTRONICS PACKAGE

by

J. E. Swansen

ABSTRACT

A new programmable read-only memory (PROM) for the Los Alamos-designed neutron coincidence electronics package is described. The new 1-k PROM allows remote control of the electronics by a computer or a remote terminal through an RS-232 serial data port. No modifications of the existing unit are required.

I. INTRODUCTION

The portable high-level neutron coincidence counter (HLNCC), the active well coincidence counter (AWCC), and a variety of in-plant neutron counters have been accepted as useful tools for the nondestructive assay of fissionable materials. The electronics package used to operate these detectors consists of a high-voltage power supply, six amplifiers, a shift-register coincidence circuit, and four scalers. This package was designed at Los Alamos National Laboratory and is commercially available through IRT Corporation, San Diego, California.

Although the electronics package was originally designed as a stand-alone instrument with only a front-panel display, modifications were added after several users showed interest in controlling the instrument remotely. The instrument was first modified to send data to a Hewlett Packard HP-97 programmable calculator for local data processing. This modification was implemented by interfacing a small Motorola MC6800 microprocessor system to the existing hardware. In addition to providing data readout capability, this interface allows processor control of the basic hardware functions: start, stop, and reset. A recycle mode was added, and an RS-232 serial data port was also

provided for auxiliary data output. Both of these features are under the control of the MC6800 software. When originally implemented, the RS-232 port was set up only to output data, but hardware was provided so that this port could later be used to input data. The new 1-k programmable read-only memory (PROM) described in this report takes advantage of this provision. Remote control is accomplished by inputting ASCII command characters and outputting data through the RS-232 port. Remote control is possible from any RS-232-compatible device, such as a stand-alone data terminal or a computer that has been configured to accept a second terminal.

Section II of this report provides a brief description of the front-panel, computer, and terminal control modes. The computer and terminal control modes are described more fully in Secs. III and IV. Installation of the new PROM and additional details on its use are given in Appendix A. Appendix B shows a flow chart of the microprocessor program, and Appendix C provides an assembly language listing. Appendix D lists a FORTRAN-callable driver and a FORTRAN test program to illustrate operation of the new PROM under computer control.

II. BRIEF DESCRIPTION OF THE NEW OPERATING MODES

A. Front-Panel Control Mode

This mode is the default mode when the power is turned on. The front-panel control mode operates in a similar manner as it did with the previous PROM, with minor exceptions as noted in Appendix A. The front panel controls the operation of the counter. Readout is directed to both the HP-97 calculator and the RS-232 serial port. The instrument must be in the front-panel control mode to enter either the computer control mode or the terminal control mode. While becoming familiar with the new PROM, the user can always return to front-panel control by pressing the restart push button on the rear panel or by turning the power off momentarily.

B. Computer Control Mode

This mode allows remote control of the electronics package through the RS-232 serial port. The serial port setup is described in Appendix A. The following functions may be controlled remotely.

S - Start
H - Stop (halt)
Z - Clear scalers and timer
R - Readout data to computer
P - Readout to HP-97 calculator
X - Request status
I - Set status interrupt flag (I flag)
F - Return to front-panel control.

The control functions are achieved by transmitting the appropriate command from the computer to the electronics package. Computer control is designed for ease of control from the remote computer. The electronics package may be operated in a passive mode where information is returned to the computer only when requested or in a pseudo-interrupt mode where a flag (I flag) signals the computer when there is a change in status. Commands from the computer are not echoed back to the computer. All data sent to the computer are terminated by a carriage return/line feed (CRLF).

C. Terminal Control Mode

This mode allows a terminal to function as a remote front panel for the electronics package. The terminal control mode operates similarly to the computer control mode but provides more information to the operator. Commands to the electronics package are the same as listed above for the computer control mode, but are all ASCII control characters (the CTRL key and letter key are depressed simultaneously). Commands echoed back to the terminal are preceded by T and followed by CRLF. Invalid control characters are echoed in the same manner, but are followed by a question mark and bell. All ASCII printing characters are echoed as is, allowing the operator to type identification or other text on the terminal without inadvertently interfering with operation of the electronics package.

III. OPERATING INSTRUCTIONS FOR COMPUTER CONTROL MODE

To enter the computer control mode, transmit ^ from the computer while in the front-panel mode. The electronics package will respond by returning to the computer: CRLF version number CRLF. This is followed by an 8-character status

word CRLF (see Sec. V). The electronics package then waits for one of the following commands from the computer.

S - Start
H - Stop (halt)
Z - Clear scalers and timer
R - Readout data to computer
P - Readout data to HP-97 calculator
X - Request status
I - Set status interrupt flag (I flag)
F - Return to front-panel control

All other inputs are ignored. Also, the electronics package will not echo command characters back to the computer while in the computer control mode. Upon receiving one of the above commands, the electronics package will execute it with the following conditions.

(1) The I command allows the computer to be advised of changes in status. When the I flag is set, the next status change causes the electronics package to send a single character with CRLF to the computer. This character has a numerical value between 0 and 8, representing the status bit that has changed. A numerical value of 0 indicates no status change; it is transmitted only after an HP-97 calculator readout. The other status values are defined in Sec. V. Normally, the I command would be used only before a timeout or a data readout to the HP-97 calculator. The I flag is cleared after a status change. The I command must be sent again before the next desired status change.

(2) If the electronics package had previously timed out, it must be reset (Z) before it can be restarted (S).

(3) Readout commands R and P are operable only when the scalers are stopped; otherwise, they are ignored.

(4) The F command allows the computer to return control to the front panel.

Four types of data are sent to the computer:

(1) Version number: CRLF V 2.1 17 Dec 80 CRLF (19 characters). This occurs only once upon entering the computer control mode.

(2) I flag response: a single ASCII digit 0 through 8 CRLF (3 characters). This occurs only if the I flag has been set and there is a status change.

(3) Status word: xxxxxxxx CRLF (10 characters). (See Sec. V for detailed description.) This status word is sent to the computer under the following conditions.

(a) Immediately after version number upon entering computer control mode.

(b) When requested by the X command.

(4) Data String: time, totals, R+A, A CRLF (57 characters). Data are all numeric or space characters. This data string is sent to the computer if an R readout command has been received by the electronics package when it is stopped. Note that (R+A)-A is not sent in the computer control mode.

The format for these four types of data is given in Table I.

TABLE I

DATA FORMAT FOR COMPUTER CONTROL MODE[a]

Data Type		Total Character Count
Version Number:		
CRLF V-2.1-12-DEC-80 CRLF		19
I Flag:		
x CRLF	x = any value 0 through 8	3
Status Word:		
xxxxxxxx CRLF	x = 1 or 0	10
Data Readout:[b]		
xxx-xxx---x-xxx-xxx-xxx---x-xxx-xxx-xxx---x-xxx-xxx-xxx CRLF		57
Time / Totals / R+A / A		

[a] x denotes a numeric character; - denotes a space character.
[b] Leading zeroes are replaced by spaces.

5

IV. OPERATING INSTRUCTIONS FOR TERMINAL CONTROL MODE

The terminal control mode is used for remotely controlling the electronics package from a terminal only. It differs from the computer control mode in that the control characters are used as commands from the terminal to the electronics.

To enter the terminal control mode, type CTRL T on the keyboard while in the front-panel mode. The electronics package responds by returning CRLF V 2.1 12 Dec 80 CRLF and an 8-character status word CRLF. The electronics package then waits for one of the following input commands from the terminal.

CTRL S - Start
CTPL H - Stop (halt)
CTPL Z - Clear scalers, timer, and fault condition
CTRL R - Readout data to terminal
CTRL P - Readout data to HP-97 calculator
CTRL X - Request status
CTRL F - Return to front-panel control
CTRL I - Set status interrupt flag (I flag)

Valid commands are echoed preceded by T and followed by CRLF. Invalid control characters are echoed in the same manner, but are followed by a question mark and bell. Printing characters do not affect operation of the electronics package, allowing typing of headings or other text on the terminal.

Upon receiving one of the above commands, the electronics package will execute it with the following conditions.

(1) The operator may be advised of changes in status, if desired, by setting the status interrupt flag (CTRL I) before any anticipated status change, such as completion of count time or calculator readout. (These two operations require time to complete; if the terminal is located some distance away, the operator will know when to continue.) When the I flag is set, the next status change causes the status character to be printed on the terminal and the I flag to be cleared. See Sec. III, item (1), for additional details on the I command.

(2) If the scalers had previously timed out, the electronics package must be reset (CTRL Z) before it can be started (CTRL S). If stopped for any other reason it may be restarted with a CTRL S.

(3) Readout commands CTRL R and CTRL P are operable only when the electronics package is stopped.

(4) The command CTRL F causes the terminal to return control to the front panel of the electronics package.

(5) The command CTRL R causes data to be printed on the terminal in the following format.

Time, totals, R+A, A, (R+A)-A

Leading zeros are suppressed and digits are separated into groups of three by spaces for ease in reading.

V. STATUS WORD DESCRIPTION

The status word may be requested by the X command at any time except during readout. It is an 8-character word, each character being either an ASCII 1 or 0. Each character's position (1-8, reading from left to right) within the word determines its function, as shown in Table II. The status word is terminated by CRLF.

TABLE II

STATUS WORD DEFINITIONS

Character Position[a] and Function	Status
1 - Run/stop	1 = stopped, 0 = counting
2 - Time out	1 = count terminated by time out
3 - Fault	1 = fault condition set
4 - Stop push button	1 = button is depressed
5 - Reset push button	1 = button is depressed
6 - Start push button	1 = button is depressed
7 - Manual/recycle switch	1 = manual, 0 = recycle
8 - Readout push button	1 = button is depressed

[a]Character position within word (12345678 CRLF).

VI. ACKNOWLEDGMENTS

Parts of the microprocessor program described in this report were developed by M. S. Krick of Los Alamos for the stand-alone version of the electronics package. S. Johnson provided the FORTRAN-callable driver and the FORTRAN test program. Discussions with N. Ensslin of Los Alamos were also helpful.

APPENDIX A

INSTALLATION AND ADDITIONAL DETAILS ON USE OF THE NEW PROM

I. INSTALLATION

This operation requires no modification of the existing circuit board.

(1) Remove ac power cord from instrument.

(2) Remove top cover.

(3) Remove screw from clamp at rear of printed circuit board assembly on right side, then swing clamp back out of the way.

(4) Remove plastic pin from hinge assembly.

(5) Pivot board assembly to upright position and reinstall plastic pin to hold boards in this position. Save packing material, if any.

(6) Remove knurled screw and spacer on each side of board assembly.

(7) Unplug microprocessor board (rear board of three) from its connector.

(8) Carefully remove old PROM (located directly under TP1 at top of board) and place it in protective foam.

(9) Locate pin 1 of new PROM and plug it in with pin 1 nearest C1 on the board. Verify that all pins enter the socket properly.

(10) For reassembly, follow steps 1-7 in reverse order. Use care when plugging in the microprocessor board to prevent damage to the connector. If foam packing material is provided, reinstall it at the end of the printed circuit board assembly.

After installing the PPOM, verify its operation with the following procedure.

(1) Connect HP-97 and charger.

(2) When the power is turned on, the readout light will turn on and the following test message will be loaded into the HP-97 storage registers R1-R4.

R1 = 543210 = time
R2 = 9876543210 = totals
R3 = 9876543210 = R+A
R4 = 9876543210 = A

The readout light will then turn off. Ignore the ERROR message displayed on the HP-97 calculator.

II. DIFFERENCE BETWEEN OLD AND NEW PROM: FRONT-PANEL CONTROL MODE

(1) The test message to the RS-232 serial port has been eliminated.
(2) The test message to the HP-97 calculator has been changed to include all digits (0-9).
(3) Column headings for the data readout have been removed.
(4) The commas between groups of three digits in data readout have been replaced by spaces.
(5) A CL X is sent to the HP-97 calculator before data are sent.
(6) The manual/recycle switch on the front panel is tested at the end of the data readout, allowing the operator to terminate the recycle mode during readout.
(7) If the electronics package is connected to a terminal either directly or indirectly through a computer, it will echo back any characters received from the terminal or computer while it is operating under the front-panel control mode. Exceptions are:
    (a) ^ is not echoed but will transfer control to computer mode.
    (b) CTRL T is not echoed but will transfer control to terminal mode.
    (c) CR or LF is echoed as both; that is, CRLF.
    (d) Characters received during data readout are not echoed.

III. RS-232 SERIAL INTERFACE REQUIREMENTS

Full duplex
Baud rate: 300
Data format: 7 bits, even parity, 1 stop bit
Electronics package rear-panel connector: 25-pin "D" type DBM - 25S
Pin connections:
  2 - Receive data from computer or terminal
  3 - Transmit data to computer or terminal
  4 - 8 (4 and 8 are tied together)
  7 - Data common
  All other pins: no connection

IV. EXAMPLE OF COMPUTER INTERFACE

Shown below is an example of a Digital Equipment Corp. (DEC) DLV11-J serial interface board configuration for use with LSI-11 computers. This is a 4-channel serial port board. Port 3 is configured for the console terminal; port 1 is configured to interface with the electronics package. (Refer to DEC publication "Memorys and Peripherals"* for more details; see page 2-149 for port 1 jumper locations).

Baud rate selection: port 1 to T = 300 baud

Data parameters:

D x to 0 = 7 bits

S x to 0 = 1 stop bit

P x to 0 = parity enabled

E x to 1 = even parity

Figure A-1 shows the cable connections to the electronics package and the cable numbers of the Berg connector as viewed from the end of the board.

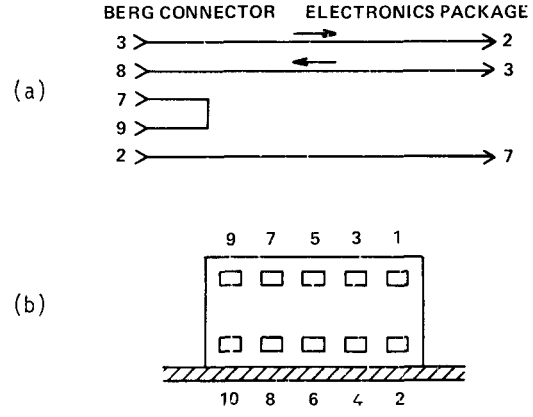
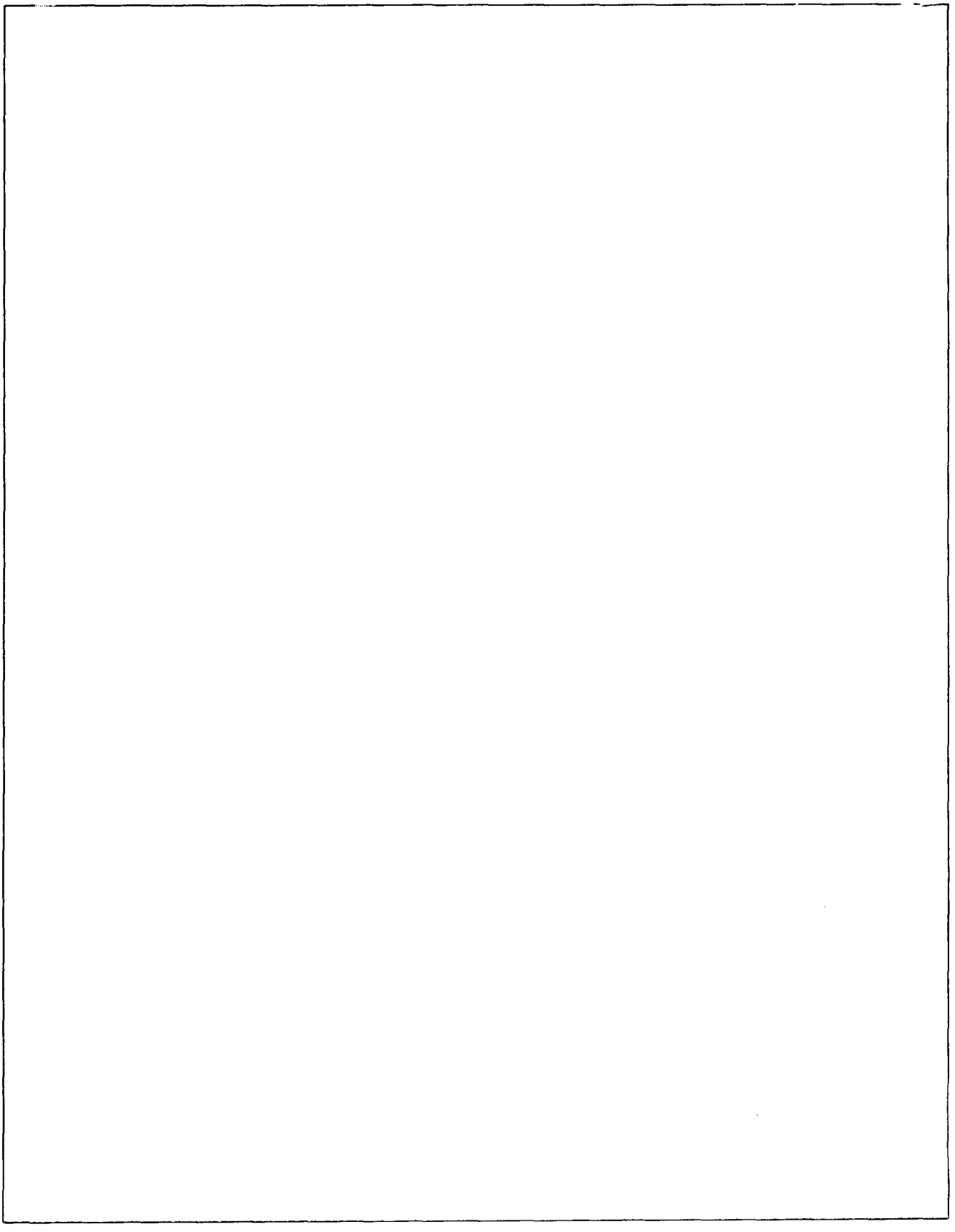


Fig. A-1.
(a) Cable between DLV11-J interface board and electronics.
(b) View of Berg connector from end of board.

*Digital Equipment Corp., Maynard, MA 01574



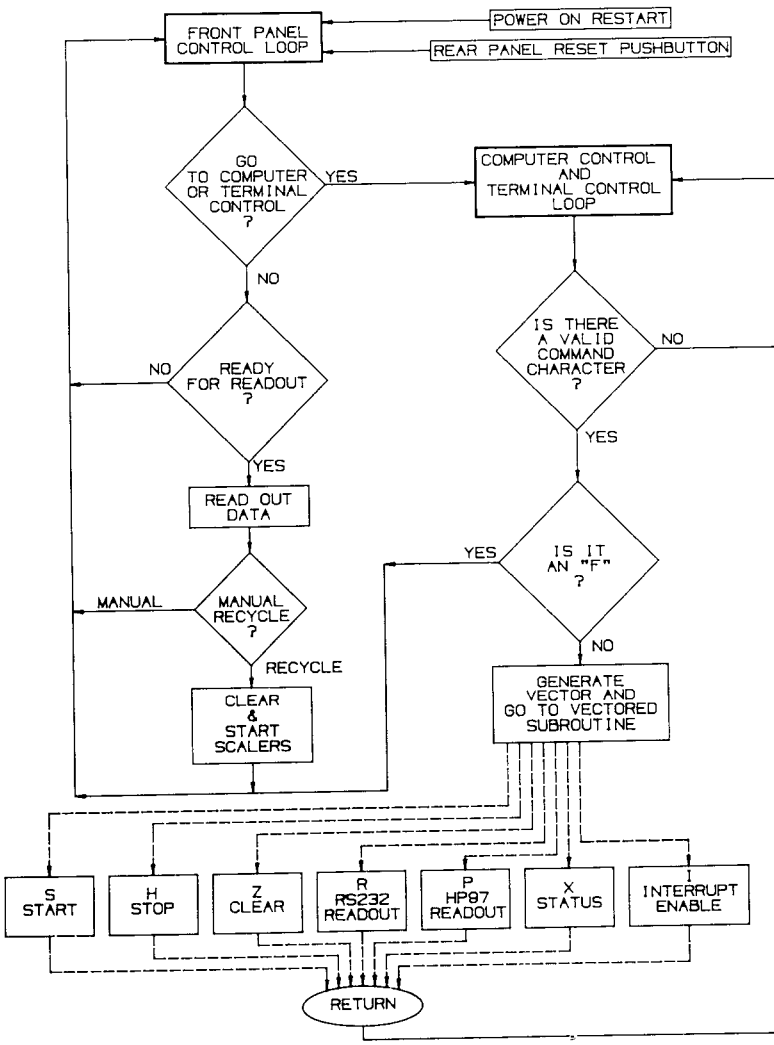
APPENDIX B

MICROPROCESSOR PROGRAM FLOW CHART

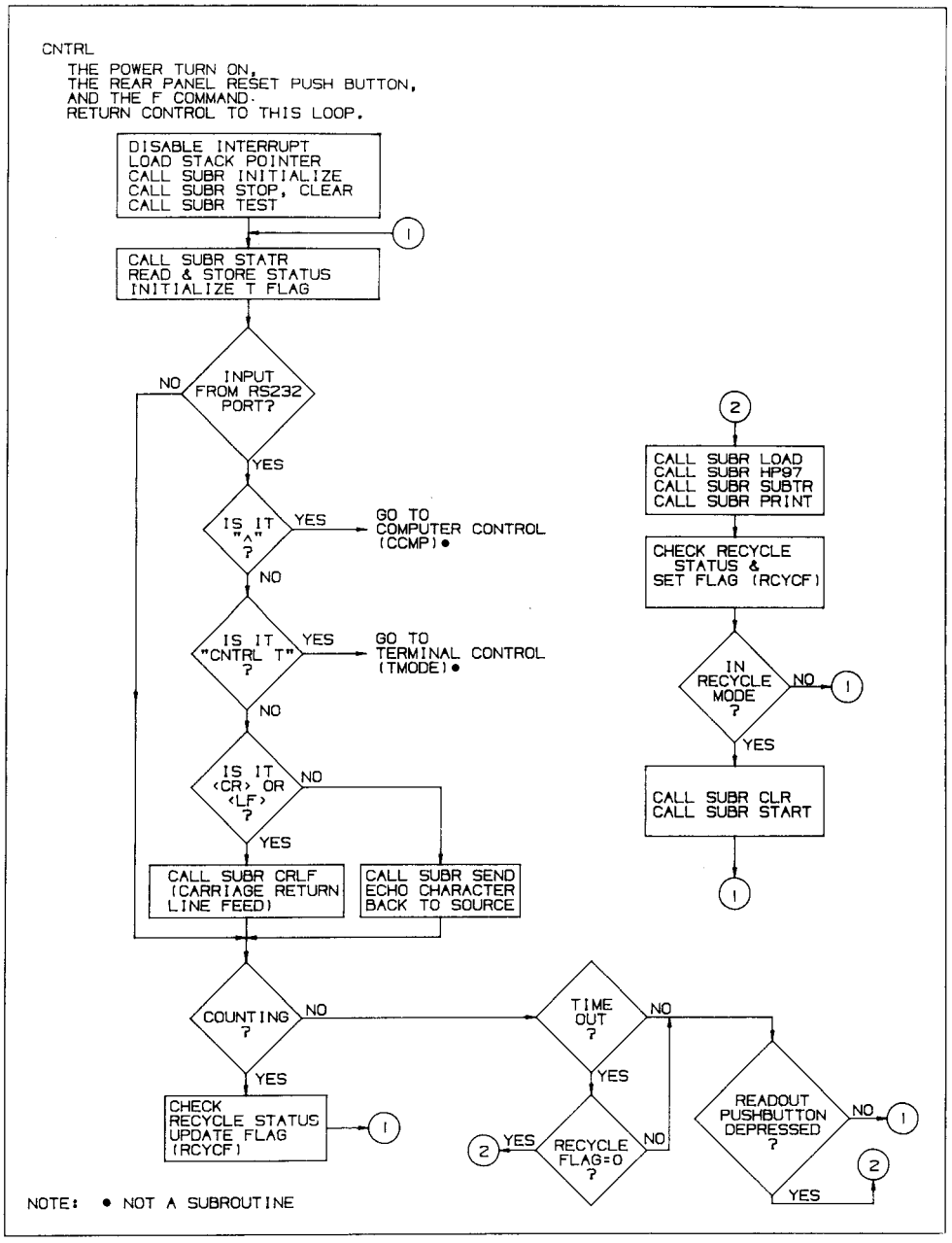
13

1-k PROM FOR REMOTE CONTROL: FUNCTIONAL BLOCK DIAGRAM

V 2.1 12 DEC 80
DISK FILENAME: RG7K11



14


CNTRL
THE POWER TURN ON,
THE REAR PANEL RESET PUSH BUTTON,
AND THE F COMMAND.
RETURN CONTROL TO THIS LOOP.
DISABLE INTERRUPT
LOAD STACK POINTER
CALL SUBR INITIALIZE
CALL SUBR STOP, CLEAR
CALL SUBR TEST
1
CALL SUBR STATR
READ & STORE STATUS
INITIALIZE T FLAG
INPUT FROM RS232 PORT?
NO
YES
IS IT "^" ?
YES
GO TO COMPUTER CONTROL (CCMP)•
NO
IS IT "CNTRL T" ?
YES
GO TO TERMINAL CONTROL (TMODE)•
NO
IS IT <CR> OR <LF> ?
NO
YES
CALL SUBR CRLF (CARRIAGE RETURN LINE FEED)
CALL SUBR SEND ECHO CHARACTER BACK TO SOURCE
COUNTING ?
NO
YES
CHECK RECYCLE STATUS UPDATE FLAG (RCYCF)
1
TIME OUT ?
NO
YES
RECYCLE FLAG=0 ?
YES
2
NO
READOUT PUSHBUTTON DEPRESSED ?
NO
1
YES
2
2
CALL SUBR LOAD
CALL SUBR HP97
CALL SUBR SUBTR
CALL SUBR PRINT
CHECK RECYCLE STATUS & SET FLAG (RCYCF)
IN RECYCLE MODE ?
NO
1
YES
CALL SUBR CLR
CALL SUBR START
1
NOTE: • NOT A SUBROUTINE

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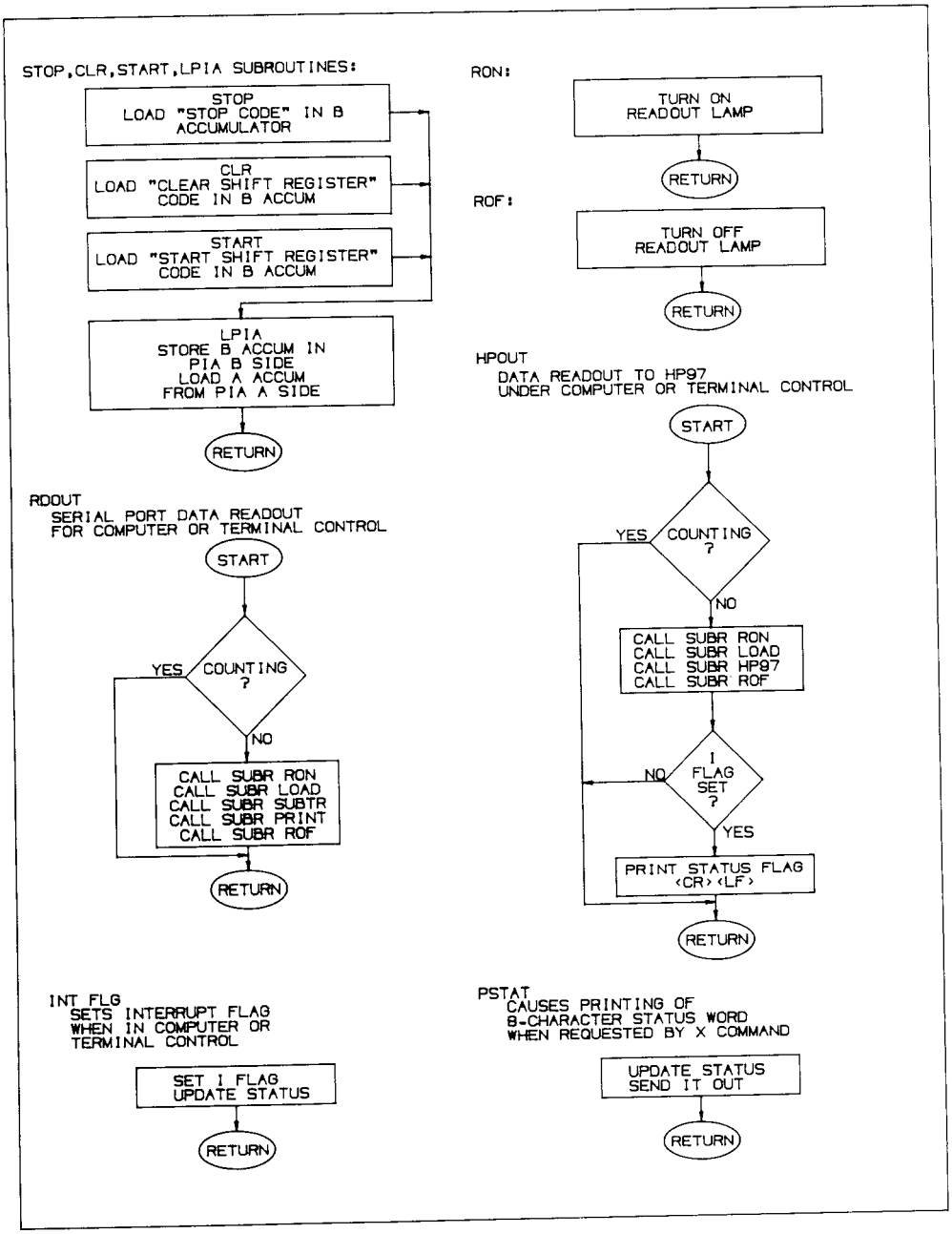
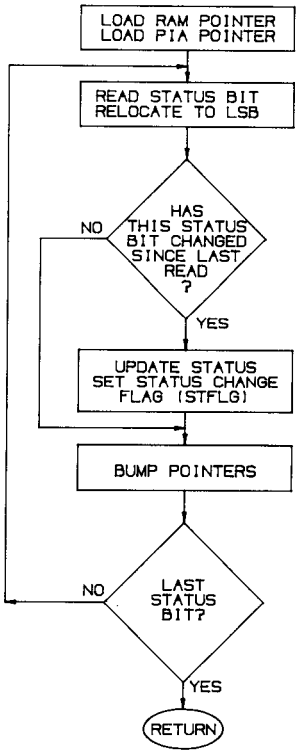

STOP,CLR,START,LPIA SUBROUTINES:
STOP
LOAD "STOP CODE" IN B ACCUMULATOR
CLR
LOAD "CLEAR SHIFT REGISTER" CODE IN B ACCUM
START
LOAD "START SHIFT REGISTER" CODE IN B ACCUM
LPIA
STORE B ACCUM IN PIA B SIDE
LOAD A ACCUM FROM PIA A SIDE
RETURN
RON:
TURN ON READOUT LAMP
RETURN
ROF:
TURN OFF READOUT LAMP
RETURN
HPOUT
DATA READOUT TO HP97 UNDER COMPUTER OR TERMINAL CONTROL
START
YES
COUNTING ?
NO
CALL SUBR RON
CALL SUBR LOAD
CALL SUBR HP97
CALL SUBR ROF
NO
I FLAG SET ?
YES
PRINT STATUS FLAG
<CR> <LF>
RETURN
RDOUT
SERIAL PORT DATA READOUT FOR COMPUTER OR TERMINAL CONTROL
START
YES
COUNTING ?
NO
CALL SUBR RON
CALL SUBR LOAD
CALL SUBR SUBTR
CALL SUBR PRINT
CALL SUBR ROF
RETURN
INT FLG
SETS INTERRUPT FLAG WHEN IN COMPUTER OR TERMINAL CONTROL
SET I FLAG
UPDATE STATUS
RETURN
PSTAT
CAUSES PRINTING OF 8-CHARACTER STATUS WORD WHEN REQUESTED BY X COMMAND
UPDATE STATUS
SEND IT OUT
RETURN

16

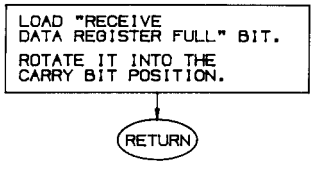
STATR

LOADS STATUS BITS INTO
A REGISTER FORMED BY
RAM LOCATIONS
1E (HEX) THROUGH 25

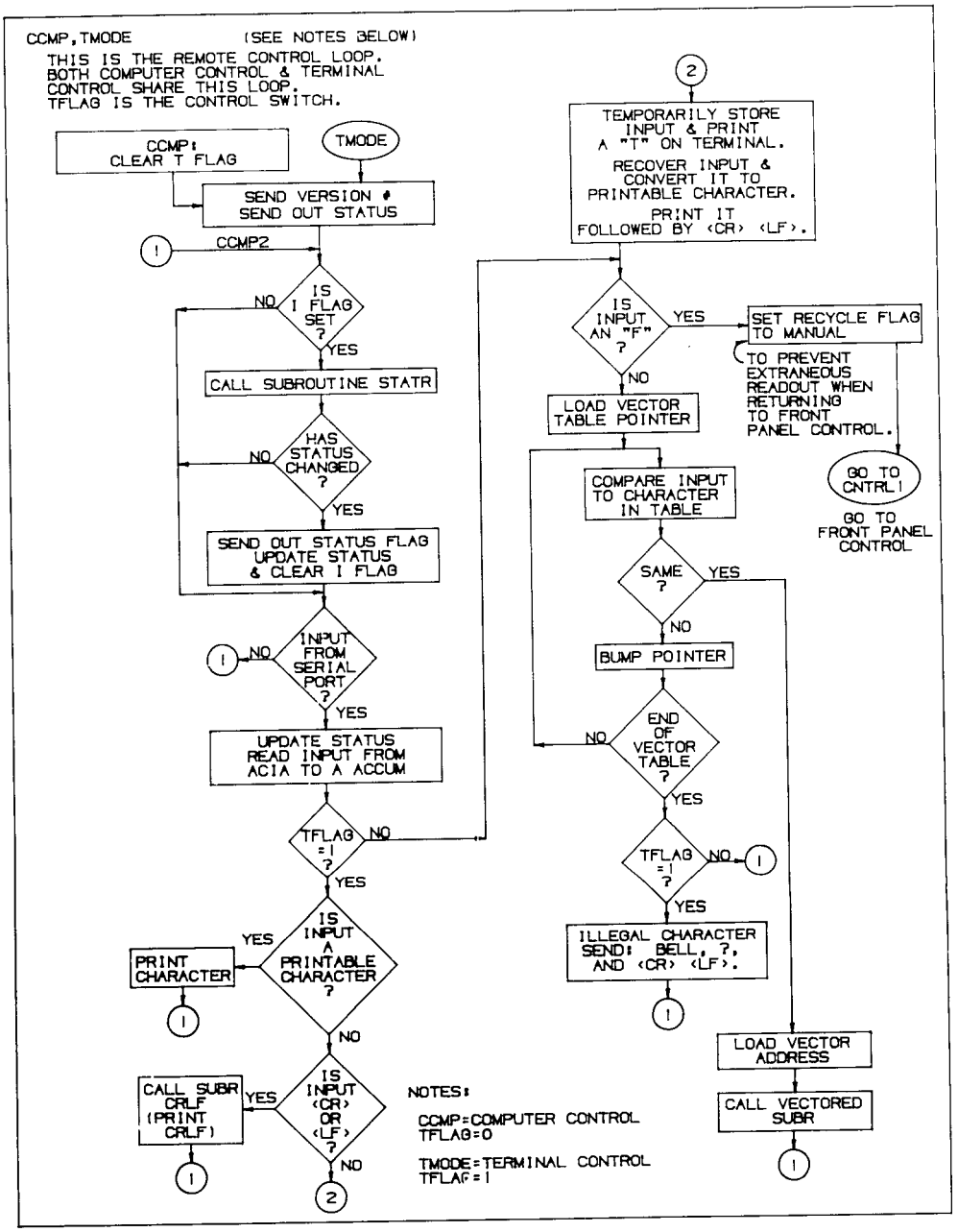


INTST

LOADS ACIA STATUS REGISTER
& PREPARES IT FOR TESTING
FOR INPUT FROM SERIAL PORT



17


CCMP,TMODE (SEE NOTES BELOW)
THIS IS THE REMOTE CONTROL LOOP.
BOTH COMPUTER CONTROL & TERMINAL
CONTROL SHARE THIS LOOP.
TFLAG IS THE CONTROL SWITCH.
CCMP: CLEAR T FLAG
TMODE
SEND VERSION # SEND OUT STATUS
CCMP2
IS I FLAG SET ?
NO
YES
CALL SUBROUTINE STATR
HAS STATUS CHANGED ?
NO
YES
SEND OUT STATUS FLAG UPDATE STATUS & CLEAR I FLAG
INPUT FROM SERIAL PORT ?
NO
YES
UPDATE STATUS READ INPUT FROM ACIA TO A ACCUM
TFLAG =1 ?
NO
YES
IS INPUT A PRINTABLE CHARACTER ?
YES
PRINT CHARACTER
NO
IS INPUT <CR> OR <LF> ?
YES
CALL SUBR CRLF (PRINT CRLF)
NO
2
TEMPORARILY STORE INPUT & PRINT A "T" ON TERMINAL.
RECOVER INPUT & CONVERT IT TO PRINTABLE CHARACTER.
PRINT IT FOLLOWED BY <CR> <LF>.
IS INPUT AN "F" ?
YES
SET RECYCLE FLAG TO MANUAL
TO PREVENT EXTRANEOUS READOUT WHEN RETURNING TO FRONT PANEL CONTROL.
GO TO CNTRL!
GO TO FRONT PANEL CONTROL
NO
LOAD VECTOR TABLE POINTER
COMPARE INPUT TO CHARACTER IN TABLE
SAME ?
YES
NO
BUMP POINTER
END OF VECTOR TABLE ?
NO
YES
TFLAG =1 ?
NO
YES
ILLEGAL CHARACTER SEND: BELL, ?, AND <CR> <LF>.
LOAD VECTOR ADDRESS
CALL VECTORED SUBR
NOTES:
CCMP=COMPUTER CONTROL
TFLAG=0
TMODE=TERMINAL CONTROL
TFLAG=1

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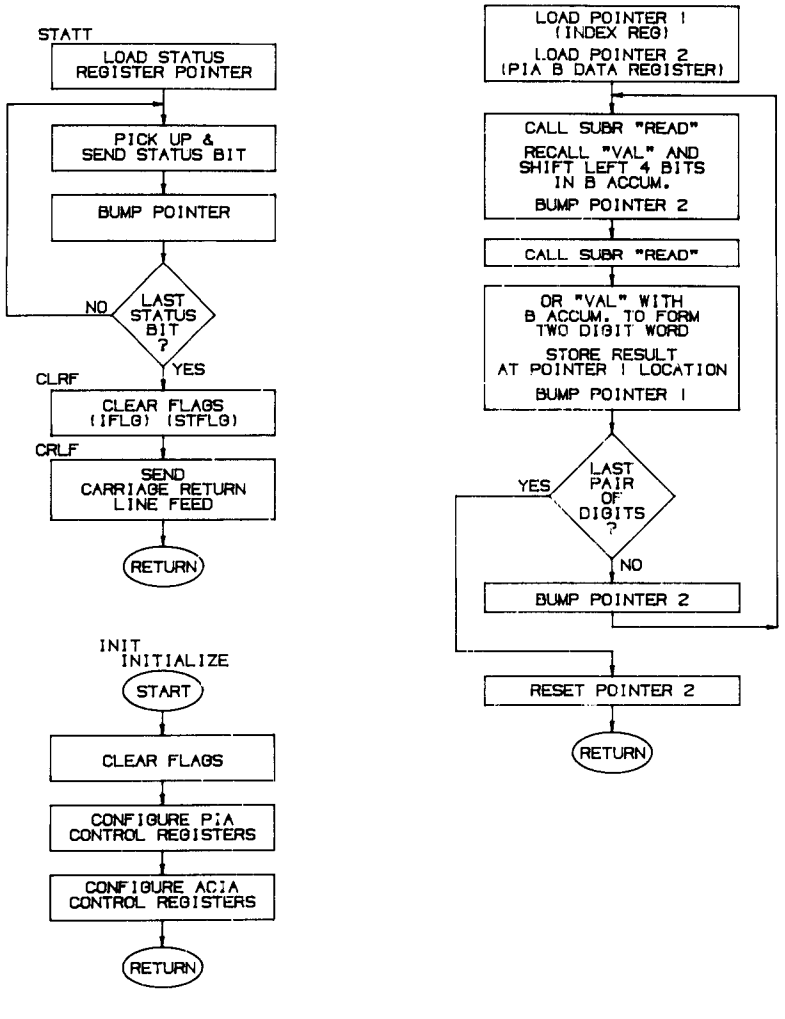
STATT:
TRANSMITS STATUS TO
REMOTE CONTROL DEVICE.

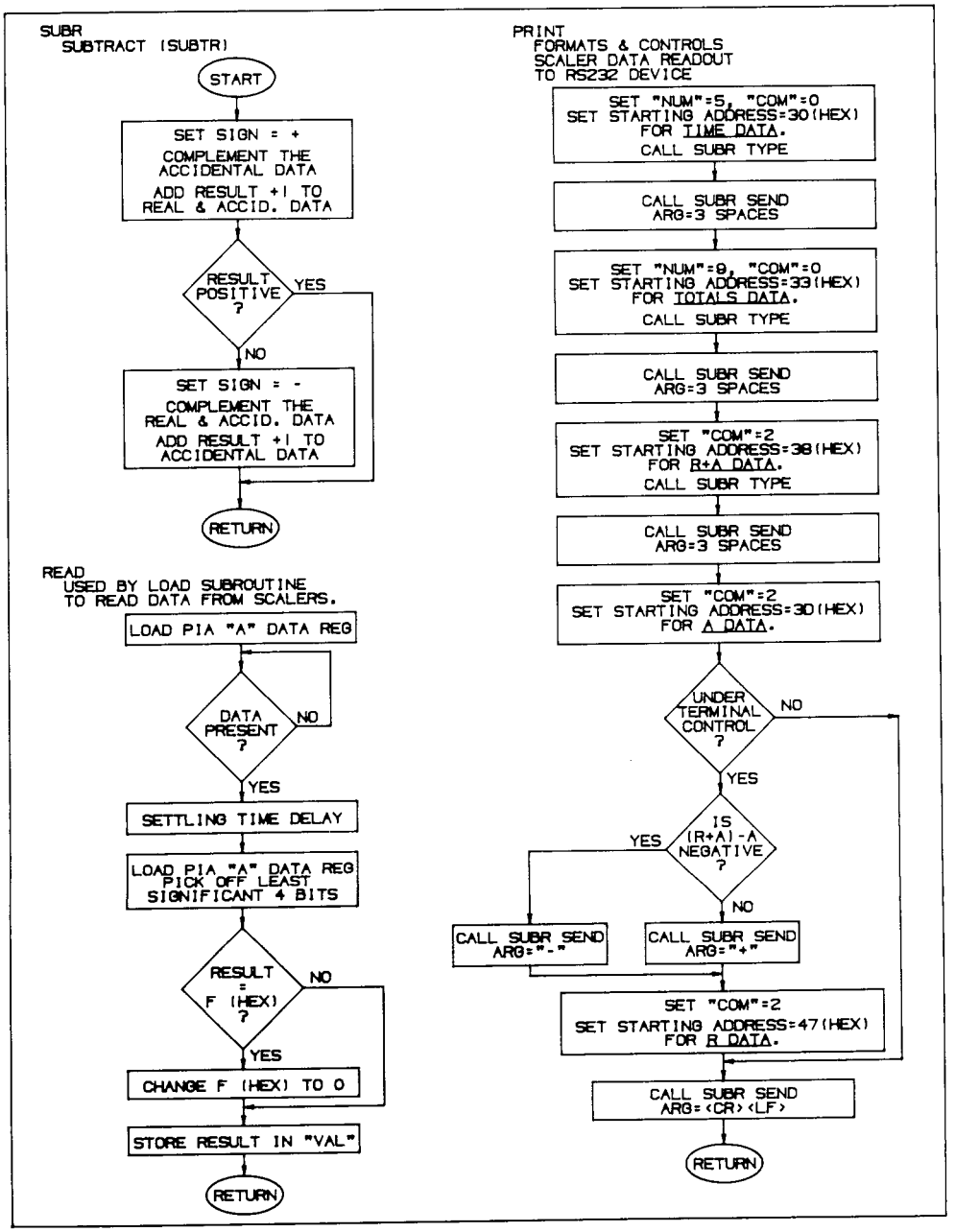
CLRF:
CLEARS INTERRUPT FLAG
(IFLG) AND
STATUS CHANGE FLAG (STFLG).

CRLF:
SENDS A CARRIAGE RETURN
AND LINE FEED.

LOAD
TAKES DATA FROM SCALERS
& LOADS INTO MEMORY.
TWO BCD DIGITS PER WORD
BEGINNING AT RAM LOCATION
30 AND ENDING AT LOCATION
42 (HEX).



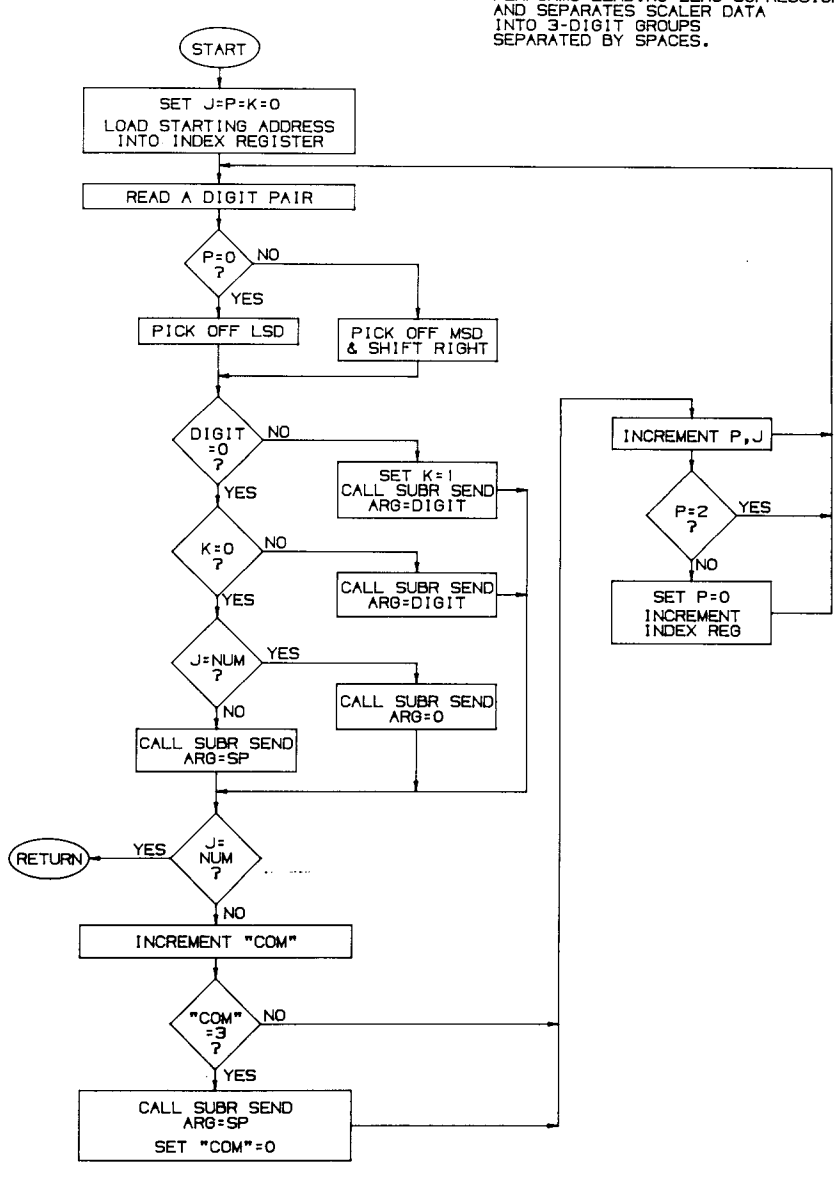
19


SUBR
SUBTRACT (SUBTR)
START
SET SIGN = +
COMPLEMENT THE ACCIDENTAL DATA
ADD RESULT +1 TO REAL & ACCID. DATA
RESULT POSITIVE ?
YES
NO
SET SIGN = -
COMPLEMENT THE REAL & ACCID. DATA
ADD RESULT +1 TO ACCIDENTAL DATA
RETURN
READ
USED BY LOAD SUBROUTINE TO READ DATA FROM SCALERS.
LOAD PIA "A" DATA REG
DATA PRESENT ?
NO
YES
SETTLING TIME DELAY
LOAD PIA "A" DATA REG PICK OFF LEAST SIGNIFICANT 4 BITS
RESULT = F (HEX) ?
NO
YES
CHANGE F (HEX) TO 0
STORE RESULT IN "VAL"
RETURN
PRINT
FORMATS & CONTROLS SCALER DATA READOUT TO RS232 DEVICE
SET "NUM"=5, "COM"=0
SET STARTING ADDRESS=30(HEX) FOR TIME DATA.
CALL SUBR TYPE
CALL SUBR SEND ARG=3 SPACES
SET "NUM"=9, "COM"=0
SET STARTING ADDRESS=33(HEX) FOR TOTALS DATA.
CALL SUBR TYPE
CALL SUBR SEND ARG=3 SPACES
SET "COM"=2
SET STARTING ADDRESS=38(HEX) FOR R+A DATA.
CALL SUBR TYPE
CALL SUBR SEND ARG=3 SPACES
SET "COM"=2
SET STARTING ADDRESS=30(HEX) FOR A DATA.
UNDER TERMINAL CONTROL ?
NO
YES
IS (R+A)-A NEGATIVE ?
YES
NO
CALL SUBR SEND ARG="-"
CALL SUBR SEND ARG="+"
SET "COM"=2
SET STARTING ADDRESS=47(HEX) FOR R DATA.
CALL SUBR SEND ARG=<CR><LF>
RETURN

20

TYPE:

UNPACKS DIGITS FROM MEMORY,
PERFORMS LEADING ZERO SUPRESSION,
AND SEPARATES SCALER DATA
INTO 3-DIGIT GROUPS
SEPARATED BY SPACES.

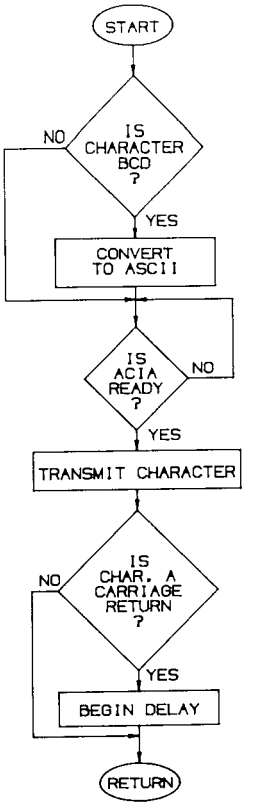


21

SEND:

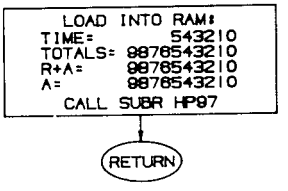
CONVERTS CHARACTERS TO ASCII AND SENDS THEM THROUGH ACIA TO REMOTE DEVICE WHEN READY.

ALSO GENERATES CARRIAGE RETURN DELAY.



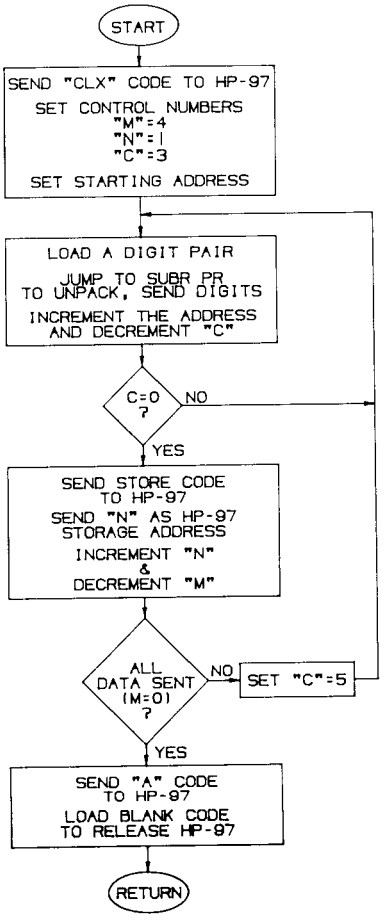
TEST:

LOADS TEST MESSAGE INTO MEMORY, AND THEN SENDS IT TO HP97.



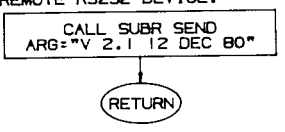
HP-97:

PREPARES AND SENDS SCALER DATA TO HP97 CALCULATOR THROUGH HP97 INTERFACE.



VNO:

SENDS PROM VERSION # TO REMOTE RS232 DEVICE.



APPENDIX C

ASSEMBLY LANGUAGE LISTING

```
00001                                NAM    HLNCC    *12-18-80 NEW CONTROL
00002                                OPT    O
00003                                OPT    S
00004          5000  A PIAI   EQU    $5000    *PIA A DATA REGISTER ADDRE
00005          5002  A PIAO   EQU    $5002    *PIA B DATA REGISTER ADDRE
00006          5001  A PIACA  EQU    $5001    *PIA A CONTROL REG. ADDR.
00007          5003  A PIACB  EQU    $5003    *PIA B CONTROL REG. ADDR.
00008          4000  A ACIAS  EQU    $4000    *ACIA STATUS ADDRESS
00009          4001  A ACIAT  EQU    $4001    *ACIA TRANSMIT ADRESS
00010          4001  A ACIAR  EQU    $4001    *ACIA RECEIVE ADRESS
00011          007F  A STACK  EQU    $7F
00012          000B  A RAMB   EQU    $B       *BEGIN RANDOM ACESS MEMORY
00013                *
00014                ************************************
00015                *
00016A 000B                    ORG    RAMB     *BEGIN RAM LOCATIONS
00017A 000B    0001  A DLY     RMB    1
00018A 000C    0001  A VAL     RMB    1
00019A 000D    0001  A SIGN    RMB    1        *(P+A)-A SIGN
00020A 000E    0001  A NUM     RMB    1
00021A 000F    0001  A COM     RMB    1
00022A 0010    0002  A F       RMB    2
00023A 0012    0001  A J       RMB    1
00024A 0013    0001  A K       RMB    1
00025A 0014    0001  A P       RMB    1
00026A 0015    0001  A DEL1    RMB    1        *CR DELAY
00027A 0016    0001  A DEL2    RMB    1
00028A 0017    0002  A R       RMB    2
00029A 0019    0001  A T       RMB    1
00030A 001A    0001  A N       RMB    1
00031A 001B    0001  A C       RMB    1
00032A 001C    0001  A M       RMB    1
00033A 001D    0001  A TEM     RMB    1
00034A 001E    0001  A RUN     RMB    1        *RUN=0/STOP=1 STATUS BIT
00035A 001F    0001  A TOUT    RMB    1        *TIME OUT=1
00036A 0020    0001  A FAULT   RMB    1        *FAULT=1
00037A 0021    0001  A STOPB   RMB    1        *STOP P.B. 1 IF DEPRESSED
00038A 0022    0001  A RESPB   RMB    1        *RESET P.B. 1 IF DEPRESSED
00039A 0023    0001  A STAPB   RMB    1        *START P.B. 1 IF DEPRESSED
00040A 0024    0001  A RCYC    RMB    1        *MANUAL=1/RECYCLE=0
00041A 0025    0001  A ROPB    RMB    1        *READOUT P.B. 1 IF DEPRESS
00042A 0026    0001  A STFLG   RMB    1        *STATUS CHANGE FLAG =1
00043A 0027    0001  A RCYCF   RMB    1        *RECYCLE FLAG
00044A 0028    0001  A TFLAG   RMB    1        *TERMINAL MODE =1/COMP MOD
00045A 0029    0001  A IFLG    RMB    1        *STATUS INTERUPT FLAG
00046A 002A    0001  A CHAR    RMB    1        *STORE A ACUM TEMPORARILY
00047          0030  A RAM     EQU    $30
00048          0038  A SST     EQU    $38
00049                *
00050                ************************************
00051                *
00052A 73FE                    ORG    $73FE    *RESTART ADRESS
00053A 73FE    7028  A RSTRT   FDB    CNTRL    *POINTER TO CONTROL PROGRA
00054                *
00055                ************************************
00056                *
00057A 7000                    ORG    $7000
00058A 7000    53    A VTBL    FCC    /S/
```

```
PAGE  002  RG7K11  .SA:1  HLNCC

00059A 7001     70A1  A          FDB     START     *VECTORS FOR COMAND CHAR'S
00060A 7003     48    A          FCC     /H/
00061A 7004     7099  A          FDB     STOP
00062A 7006     5A    A          FCC     /Z/
00063A 7007     709D  A          FDB     CLR
00064A 7009     52    A          FCC     /R/
00065A 700A     70BC  A          FDB     RDOUT     *READOUT VIA RS232
00066A 700C     50    A          FCC     /P/
00067A 700D     70CE  A          FDB     HPOUT     *READOUT VIA HP97
00068A 700F     58    A          FCC     /X/
00069A 7010     70F3  A          FDB     PSTRT     *REQUEST STATUS
00070A 7012     49    A          FCC     /I/
00071A 7013     70E9  A          FDB     INTFLG    *SET STATUS INTERUPT FLAG
00072                    *******
00073                    *CARRIAGE RETURN = CR
00074                    *LINE FEED = LF
00075A 7015     0D0A  A S1       FDB     $0D0A     *CR,LF
00076A 7017     56    A          FCC     'S.V 2.1 12 DEC 80*VERSION NO.
00077A 7026     0D0A  A          FDB     $0D0A     *CR,LF*
00078                    ****************************************
00079                    *
00080A 7028 0F           CNTRL   SEI               *DISABLE INTERRUPT
00081A 7029 8E 007F   A          LDS     #STACK    *LOAD STACK POINTER
00082A 702C BD 71C1   A          JSR     INIT      *JUMP TO INITIALIZE ROUTIN
00083A 702F 8D 68 7099           BSR     STOP      *STOP SR
00084A 7031 8D 6A 709D           BSR     CLR       *CLEAR SR
00085A 7033 BD 70B0   A          JSR     RON       *TURN ON READOUT LIGHT
00086A 7036 BD 73AE   A          JSR     TEST      *JUMP TO TEST SUBROUTINE
00087A 7039 BD 70B6   A          JSR     ROF       *TURN OFF READOUT LIGHT
00088A 703C BD 70F9   A CNTRL1   JSR     STATR     *READ/STORE STATUS
00089A 703F 86 01     A          LDAA    #1        *SET T FLAG
00090A 7041 97 28     A          STAA    TFLAG
00091A 7043 BD 7116   A          JSR     INTST     *IS THERE AN INPUT
00092A 7046 24 10 7065           BCC     TERM3     *NO INPUT,BRANCH
00093A 7048 B6 4001   A          LDAA    ACIAR
00094A 704B 81 5E     A          CMPA    ##5E      *IS IT A "^" ?
00095A 704D 26 03 7052           BNE     TERM0     *NO ,BRANCH
00096A 704F 7E 711C   A          JMP     COMP      *YES, JMP TO COMPUTER CONT
00097A 7052 81 14     A TERM0    CMPA    ##14      *IS IT CONTROL T
00098A 7054 26 03 7059           BNE     TERM1     *IF YES JMP TO TERM MODE
00099A 7056 7E 711F   A          JMP     TMODE
00100A 7059 81 0E     A TERM1    CMPA    ##0E
00101A 705B 2E 05 7062           BGT     TERM2     *ECHO IT
00102A 705D BD 71B2   A          JSR     CRLF      *ECHO CR AND LF
00103A 7060 20 03 7065           BRA     TERM3
00104A 7062 BD 7326   A TERM2    JSR     SEND
00105A 7065 96 1E     A TERM3    LDAA    RUN       *BRANCH IF STOPPED
00106A 7067 26 06 706F           BNE     CNTRL2    *BRANCH IF STOPPED
00107A 7069 96 24     A          LDAA    RCYC      *RECYCLE STATUS
00108A 706B 97 27     A          STAA    RCYCF     *RECYCLE FLAG
00109A 706D 20 CD 703C           BRA     CNTRL1
00110A 706F 96 1F     A CNTRL2   LDAA    TOUT      *TEST FOR TIME OUT
00111A 7071 27 04 7077           BEQ     CNTRL3    *BRANCH IF NO TIME OUT
00112A 7073 96 27     A          LDAA    RCYCF     *RECYCLE MODE ?
00113A 7075 27 04 707B           BEQ     CNTRL4    *BRANCH IF IN RECYCLE
00114A 7077 96 25     A CNTRL3   LDAA    ROPB      *IS R.O. BUTTON DEPRESSED
00115A 7079 27 C1 703C           BEQ     CNTRL1    *BRANCH IF NOT
00116A 707B 8D 33 70B0 CNTRL4    BSR     RON       *TURN ON R.O. LIGHT
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00117A 707D BD 71DE  A          JSR     LOAD      *READ THE SCALERS
00118A 7080 BD 734B  A          JSR     HP97      *SEND RESULTS TO HP-97
00119A 7083 BD 7221  A          JSR     SUBTR     *SUBTRACT A FROM R+A
00120A 7086 BD 726C  A          JSR     PRINT     *PRINT RESULTS
00121A 7089 8D 2B 70B6           BSR     ROF       *TURN OFF READOUT LIGHT
00122A 708B 8D 6C 70F9           BSR     STATR
00123A 708D 96 24    A           LDAA    RCYC
00124A 708F 97 27    A           STAA    RCYCF
00125A 7091 26 A9 703C           BNE     CNTRL1    *BRANCH IF MANUAL
00126A 7093 8D 08 709D           BSR     CLR       *CLEAR SR
00127A 7095 8D 0A 70A1           BSR     START     *START SR
00128A 7097 20 A3 703C           BRA     CNTRL1    *RETURN TO WAIT LOOP
00129                      ***
00130A 7099 C6 28    A STOP      LDAB    #$28      *PIA STOP CODE
00131A 709B 20 06 70A3           BRA     LPIA
00132A 709D C6 29    A CLR       LDAB    #$29      *PIA CLEAR CODE
00133A 709F 20 02 70A3           BRA     LPIA
00134A 70A1 C6 2A    A START     LDAB    #$2A      *PIA START CODE
00135A 70A3 F7 5002  A LPIA      STAB    PIAC      *SEND OUT STATUS CODE
00136A 70A6 B6 5000  A           LDAA    PIAI
00137A 70A9 B6 5000  A           LDAA    PIAI      *READ STATUS
00138A 70AC 7F 5002  A           CLR     PIAC      *RELEASE PIA CONTROL
00139A 70AF 39                   RTS               *RETURN
00140                      ***
00141A 70B0 86 3C    A RON       LDAA    #$3C      *LOAD CONTROL REG. CODE
00142A 70B2 B7 5003  A           STAA    PIACB     *SEND IT OUT
00143A 70B5 39                   RTS               *RETURN
00144A 70B6 86 34    A ROF       LDAA    #$34      *LOAD CONTROL REG. CODE
00145A 70B8 B7 5003  A           STAA    PIACB     *SEND IT OUT
00146A 70BB 39                   RTS               *RETURN
00147A 70BC 96 1E    A RDOUT     LDAA    RUN       *IS IT RUNNING?
00148A 70BE 27 0D 70CD           BEQ     RDOUT1    *RETURN IF YES
00149A 70C0 8D EE 70B0           BSR     RON       *RS232 OUTPUT ROUTINE
00150A 70C2 BD 71DE  A           JSR     LOAD
00151A 70C5 BD 7221  A           JSR     SUBTR
00152A 70C8 BD 726C  A           JSR     PRINT
00153A 70CB 8D E9 70B6           BSR     ROF
00154A 70CD 39           RDOUT1  RTS
00155                      ***
00156A 70CE 96 1E    A HPOUT     LDAA    RUN       *HP97 OUTPUT ROUTINE
00157A 70D0 27 16 70E8           BEQ     HPOUT1
00158A 70D2 8D DC 70B0           BSR     RON
00159A 70D4 BD 71DE  A           JSR     LOAD
00160A 70D7 BD 734B  A           JSR     HP97
00161A 70DA 8D DA 70B6           BSR     ROF
00162A 70DC 96 29    A           LDAA    IFLG      *IS STATUS INTERUPT FLAG S
00163A 70DE 27 08 70E8           BEQ     HPOUT1    *IF NOT BRANCH
00164A 70E0 96 26    A           LDAA    STFLG     *PRINT STATUS FLAG
00165A 70E2 BD 7326  A           JSR     SEND
00166A 70E5 BD 71AD  A           JSR     CLRF
00167A 70E8 39           HPOUT1  RTS
00168                      ***
00169A 70E9 86 01    A INTFLG    LDAA    #1
00170A 70EB 97 29    A           STAA    IFLG
00171A 70ED 8D 0A 70F9           BSR     STATR
00172A 70EF 7F 0026  A           CLR     STFLG
00173A 70F2 39                   RTS
00174                      ***
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00175A 70F3 8D 04 70F9 PSTAT  BSR    STATR    *REQUEST STATUS
00176A 70F5 BD 719F  A        JSR    STATT
00177A 70F8 39                RTS
00178                  ***
00179A 70F9 CE 001E  A STATR  LDX    #RUN     *LOAD RAM STATUS POINTER
00180A 70FC C6 30    A        LDAB   #$30     *LOAD PIA STATUS POINTER
00181A 70FE 8D A3 70A3 STATR1 BSR    LPIA
00182A 7100 84 80    A        ANDA   #$80     *MASK ALL BITS BUT 7
00183A 7102 49                ROLA           *MOVE TO BIT 0
00184A 7103 49                ROLA
00185A 7104 A1 00    A        CMPA   0,X      *IS BIT SAME AS BEFORE
00186A 7106 27 06 710E        BEQ    STATR2   *BRANCH IF SAME
00187A 7108 A7 00    A        STAA   0,X      *STORE IF NOT
00188A 710A 5C                INCB
00189A 710B D7 26    A        STAB   STFLG    *SET STAT. CHANGE FLAG
00190A 710D 5A                DECB
00191A 710E 5C           STATR2 INCB           *BUMP POINTER
00192A 710F 08                INX
00193A 7110 8C 0026  A        CPX    #STFLG   *LAST STATUS BIT ?
00194A 7113 26 E9 70FE        BNE    STATR1
00195A 7115 39                RTS
00196                  ***
00197A 7116 4F           INTST CLRA
00198A 7117 B6 4000  A        LDAA   ACIAS
00199A 711A 46                RORA
00200A 711B 39                RTS
00201                  *
00202                  ************
00203                  *
00204A 711C 7F 0028  A CCMP   CLR    TFLAG
00205A 711F 8D 72C7  A TMODE  JSR    VNO      *PRINT VERSION NO.
00206A 7122 8D 7B 719F CCMP1  BSR    STATT    *PRINT STATUS
00207A 7124 96 29    A CCMP2  LDAA   IFLG     *IS STATUS INTERUPT SET?
00208A 7126 27 0D 7135        BEQ    CCMP3    *BRANCH IF NOT
00209A 7128 8D CF 70F9        BSR    STATR    *READ/STORE STATUS
00210A 712A 96 26    A        LDAA   STFLG    *HAS STATUS CHANGED?
00211A 712C 27 07 7135        BEQ    CCMP3    *IF NO BRANCH
00212A 712E BD 7326  A        JSR    SEND     *IF YES SEND OUT STATUS FL
00213A 7131 8D C6 70F9        BSR    STATR    *REDUNDANT STATUS READ
00214A 7133 8D 78 71AD        BSR    CLRF
00215A 7135 8D DF 7116 CCMP3  BSR    INTST
00216A 7137 24 EB 7124        BCC    CCMP2
00217A 7139 8D BE 70F9        BSR    STATR
00218A 713B B6 4001  A        LDAA   ACIAR    *REDUNDANT LOAD
00219A 713E B6 4001  A        LDAA   ACIAR    *LOAD INPUT
00220A 7141 D6 28    A        LDAB   TFLAG
00221A 7143 27 28 716D        BEQ    CCMP6
00222A 7145 81 1F    A        CMPA   #$1F     *IS IT PRINTING CHAR?
00223A 7147 2E 1F 7168        BGT    CCMP5    *BRANCH IF YES
00224A 7149 81 0D    A        CMPA   #$0D     *IS IT A CR?
00225A 714B 27 17 7164        BEQ    CCMP4    *BRANCH IF YES
00226A 714D 81 0A    A        CMPA   #$0A     *IS IT A LF?
00227A 714F 27 13 7164        BEQ    CCMP4
00228A 7151 97 2A    A        STAA   CHAR
00229A 7153 86 54    A        LDAA   #$54     *T=TERMINAL MODE PROMPT
00230A 7155 BD 7326  A        JSR    SEND
00231A 7158 96 2A    A        LDAA   CHAR
00232A 715A 8A 40    A        ORAA   #$40     *MAKE PRINTING CHAR.
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00233A 715C BD 7326  A          JSR     SEND      *PRINT IT
00234A 715F BD 71B2  A          JSR     CRLF      *ECHO CR AND LF
00235A 7162 20 09 716D          BRA     COMP6
00236A 7164 8D 4C 71B2 COMP4    BSR     CRLF
00237A 7166 20 BC 7124          BRA     COMP2
00238A 7168 BD 7326  A COMP5    JSR     SEND
00239A 716B 20 B7 7124          BRA     COMP2
00240A 716D 81 46    A COMP6    CMPA    #$46      *IS IT A "F"?
00241A 716F 26 07 7178          BNE     VECT      *IF NO BRANCH TO VECT
00242A 7171 86 01    A          LDAA    #1
00243A 7173 97 27    A          STAA    RCYCF
00244A 7175 7E 703C  A          JMP     CNTRL1    *IF YES RETURN TO MANUAL C
00245                    ***
00246A 7178 CE 7000  A VECT     LDX     #VTBL     *LOAD VECTOR POINTER
00247A 717B A1 00    A VECT1    CMPA    0,X
00248A 717D 27 1A 7199          BEQ     VECT3     *IF YES LOAD VECTOR
00249A 717F 08                  INX               *IF NO BUMP POINTER
00250A 7180 08                  INX
00251A 7181 08                  INX
00252A 7182 8C 7015  A          CPX     #VTBL+21 *LAST ONE ?
00253A 7185 26 F4 717B          BNE     VECT1
00254A 7187 96 28    A          LDAA    TFLAG
00255A 7189 27 0C 7197          BEQ     VECT2     *IN COMPUTER MODE DON'T
00256                    *ACKNOWLEGE ILLEGAL CHARACTERS
00257A 718B 86 07    A          LDAA    #$07      *ASCII "BELL"
00258A 718D BD 732C  A          JSR     SEJP1     *SEND BELL CODE
00259A 7190 86 3F    A          LDAA    #$3F      *IF NOT VALID CHARACTOR
00260A 7192 BD 7326  A          JSR     SEND      *PRINT "?"
00261A 7195 8D 1B 71B2          BSR     CRLF      *PRINT CR,LF
00262A 7197 20 8B 7124 VECT2    BRA     COMP2     *RETURN TO WAITING LOOP
00263A 7199 EE 01    A VECT3    LDX     1,X
00264A 719B AD 00    A          JSR     0,X       *JUMP TO VECTORED ROUTINE
00265A 719D 20 F8 7197          BRA     VECT2
00266                    ***
00267A 719F CE 001E  A STATT    LDX     #RUN      *TRANSMIT STATUS
00268A 71A2 A6 00    A STATT1   LDAA    0,X
00269A 71A4 BD 7326  A          JSR     SEND
00270A 71A7 08                  INX
00271A 71A8 8C 0026  A          CPX     #RUN+8
00272A 71AB 26 F5 71A2          BNE     STATT1
00273A 71AD 4F           CLRF   CLRA
00274A 71AE 97 29    A          STAA    IFLG
00275A 71B0 97 26    A          STAA    STFLG
00276A 71B2 97 2A    A CRLF     STAA    CHAR      *STORE A ACUM TEMPORARILY
00277A 71B4 86 0D    A          LDAA    #$0D
00278A 71B6 BD 7326  A          JSR     SEND
00279A 71B9 86 0A    A          LDAA    #$0A
00280A 71BB BD 7326  A          JSR     SEND
00281A 71BE 96 2A    A          LDAA    CHAR      *RESTORE A ACUMM
00282A 71C0 39                  RTS
00283                    *
00284                    ************************************
00285                    *
00286A 71C1 4F           INIT   CLRA              *CLEAR ACCUMULATOR A
00287A 71C2 97 26    A          STAA    STFLG     *CLEAR STATUS FLAG
00288A 71C4 B7 5000  A          STAA    PIAI      *DEFINE A SIDE AS INPUT
00289A 71C7 43                  COMA
00290A 71C8 B7 5002  A          STAA    PIAO      *DEFINE B SIDE AS OUTPUT
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00291A 71CB 86 04    A          LDAA   #$4
00292A 71CD B7 5001  A          STAA   PIACA     *CHANGE FROM DATA DIRECTIO
00293                *                           REGISTER TO DATA REGISTER
00294
00295A 71D0 B7 5003  A          STAA   PIACB     *DITTO
00296A 71D3 86 03    A          LDAA   #$3       *MASTER RESET
00297A 71D5 B7 4000  A          STAA   ACIAS
00298A 71D8 86 09    A          LDAA   #$9       *SET UP DATA FORMAT
00299A 71DA B7 4000  A          STAA   ACIAS
00300A 71DD 39                  RTS
00301                *
00302                ************************************
00303                *
00304A 71DE CE 0030  A LOAD     LDX    #RAM      *LOAD INDEX REGISTER WITH
00305                *                           FIRST STORAGE LOCATION
00306A 71E1 86 01    A          LDAA   #1        *LOAD CONTROL CODE "1" INT
00307                *                           PIA B DATA REGISTER
00308A 71E3 B7 5002  A          STAA   PIAO
00309A 71E6 8D 1E 7206 LLP1     BSR    READ      *READ DIGIT; STORE IN VAL
00310A 71E8 D6 0C    A          LDAB   VAL       *MOVE DIGIT LEFT
00311A 71EA 58                  ASLB
00312A 71EB 58                  ASLB
00313A 71EC 58                  ASLB
00314A 71ED 58                  ASLB
00315A 71EE 7C 5002  A          INC    PIAO      *INCREMENT CONTROL CODE
00316                *                           FOR NEXT DIGIT
00317A 71F1 8D 13 7206          BSR    READ      *READ THE DIGIT
00318A 71F3 DA 0C    A          ORAB   VAL       *FORM A 2-DIGIT PAIR
00319A 71F5 E7 00    A          STAB   0,X       *STORE RESULT AT POINTER
00320A 71F7 08                  INX              *INCREMENT POINTER
00321A 71F8 8C 0042  A          CPX    #RAM+18   *POINTER=42?
00322A 71FB 27 05 7202          BEQ    LJP1      *YES, GO TO LJP1
00323A 71FD 7C 5002  A          INC    PIAO      *NO, INCREMENT CONTROL COD
00324A 7200 20 E4 71E6          BRA    LLP1      *BRANCH TO READ NEXT
00325                *                           PAIR OF DIGITS
00326A 7202 7F 5002  A LJP1     CLR    PIAO      *REMOVE CONTROL CODE
00327A 7205 39                  RTS              *RETURN FROM SUBROUTINE
00328A 7206 B6 5000  A READ     LDAA   PIAI      *LOAD THE PIA A DATA REGIS
00329A 7209 2B FB 7206          BMI    READ      *PROCEED IF POSITIVE
00330                *                           (DATA PRESENT)
00331A 720B 86 FF    A          LDAA   #$FF      *ALLOW DELAY FOR
00332                *                           SETTLING TIME
00333A 720D 97 0B    A          STAA   DLY
00334A 720F 7A 000B  A LLP2     DEC    DLY
00335A 7212 26 FB 720F          BNE    LLP2
00336A 7214 B6 5000  A          LDAA   PIAI      *LOAD THE PIA A DATA
00337                *                           REGISTER REDUNDANTLY
00338A 7217 84 0F    A          ANDA   #$F       *STRIP OFF LEAST
00339                *                           SIGNIFICANT 4 BITS
00340A 7219 81 0F    A          CMPA   #$F       *DATA=F?
00341A 721B 26 01 721E          BNE    LJP2      *NO, PROCEED
00342A 721D 4F                  CLRA             *YES, CHANGE TO ZERO
00343A 721E 97 0C    A LJP2     STAA   VAL       *STORE RESULT IN VAL
00344A 7220 39                  RTS              *RETURN FROM SUBROUTINE
00345                *
00346                ************************************
00347                *
00348A 7221 7F 000D  A SUBTR    CLR    SIGN      *CLEAR SIGN CONTROL
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00349                          *                          CONSTANT (0 FOR +; 1 FOR
00350A 7224 CE 0038  A         LDX    #SST       *LOAD STARTING ADDRESS
00351A 7227 C6 05    A         LDAB   #5         *LOAD CONTROL CONSTANT
00352A 7229 86 99    A SLP1    LDAA   #$99       *LOAD $99
00353A 722B A0 09    A         SUBA   9,X        *SUBTRACT TO COMPLEMENT
00354A 722D A7 0E    A         STAA   $E,X       *STORE COMPLEMENT
00355A 722F 09                 DEX               *DECREMENT ADDRESS
00356A 7230 5A                 DECB              *DECREMENT CONTROL NUMBER
00357A 7231 26 F6 7229         BNE    SLP1       *RECYCLE UNTIL ALL DIGITS
00358                          *                          ARE COMPLEMENTED
00359A 7233 0D                 SEC               *SET THE CARRY
00360A 7234 C6 05    A         LDAB   #5         *LOAD CONTROL NUMBER
00361A 7236 CE 0038  A         LDX    #SST       *LOAD STARTING ADDRESS
00362A 7239 A6 04    A SLP2    LDAA   4,X        *LOAD PAIR OF DIGITS
00363                          *                          FOR ADDITION
00364A 723B A9 0E    A         ADCA   $E,X       *ADD WITH CARRY
00365A 723D 19                 DAA               *DECIMAL ADJUST
00366A 723E A7 13    A         STAA   $13,X      *STORE SUM
00367A 7240 09                 DEX               *DECREMENT ADDRESS
00368A 7241 5A                 DECB              *DECREMENT CONTROL NUMBER
00369A 7242 26 F5 7239         BNE    SLP2       *RECYCLE UNTIL ADDITION
00370                          *                          IS COMPLETE
00371A 7244 24 01 7247         BCC    SJP1       *BRANCH TO SJP1 IF
00372                          *                          CARRY IS CLEAR
00373A 7246 39                 RTS               *RETURN TO CONTROL PROGRAM
00374                          *                          IF CARRY IS SET
00375A 7247 86 01    A SJP1    LDAA   #1         *CHANGE SIGN TO -
00376A 7249 97 0D    A         STAA   SIGN
00377A 724B CE 0038  A         LDX    #SST       *REVERSE SUBTRAHEND AND
00378                          *                          MINUEND AND REPEAT
00379A 724E C6 05    A         LDAB   #5
00380A 7250 86 99    A SLP4    LDAA   #$99
00381A 7252 A0 13    A         SUBA   $13,X
00382A 7254 A7 13    A         STAA   $13,X
00383A 7256 09                 DEX
00384A 7257 5A                 DECB
00385A 7258 26 F6 7250         BNE    SLP4
00386A 725A 0D                 SEC
00387A 725B C6 05    A         LDAB   #5
00388A 725D CE 0038  A         LDX    #SST
00389A 7260 86 00    A SLP5    LDAA   #0
00390A 7262 A9 13    A         ADCA   $13,X
00391A 7264 19                 DAA
00392A 7265 A7 13    A         STAA   $13,X
00393A 7267 09                 DEX
00394A 7268 5A                 DECB
00395A 7269 26 F5 7260         BNE    SLP5
00396A 726B 39                 RTS
00397                          *
00398                          ************************************
00399                          *
00400A 726C 86 05    A PRINT   LDAA   #$5        *SET NUM=5
00401A 726E 97 0E    A         STAA   NUM
00402A 7270 86 30    A         LDAA   #RAM       *LOAD STARTING ADDRESS
00403                          *                          ($0030) AT F, F+1
00404A 7272 97 11    A         STAA   F+1
00405A 7274 4F                 CLRA
00406A 7275 97 10    A         STAA   F
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00407A 7277 97 0F     A          STAA   COM       *SET COM=0
00408A 7279 8D 4F 72CA           BSR    TYPE      *TYPE OUT TIME
00409A 727B 8D 40 72BD           BSR    SP        *PRINT 3 SPACES
00410A 727D 86 09     A          LDAA   #$9       *SET NUM=9
00411A 727F 97 0E     A          STAA   NUM
00412A 7281 86 33     A          LDAA   #RAM+3    *SET START ADDR = $0033
00413A 7283 97 11     A          STAA   F+1
00414A 7285 86 02     A          LDAA   #$2       *SET COM=2
00415A 7287 97 0F     A          STAA   COM
00416A 7289 8D 3F 72CA           BSR    TYPE      *TYPE OUT TOTALS
00417A 728B 8D 30 72BD           BSR    SP        *PRINT 3 SPACES
00418A 728D 86 38     A          LDAA   #RAM+8    *SET START ADDR = $0038
00419A 728F 97 11     A          STAA   F+1
00420A 7291 8D 37 72CA           BSR    TYPE      *TYPE OUT R+A
00421A 7293 8D 28 72BD           BSR    SP        *PRINT 3 SPACES
00422A 7295 86 3D     A          LDAA   #RAM+13   *SET START ADDR = $003D
00423A 7297 97 11     A          STAA   F+1
00424A 7299 8D 2F 72CA           BSR    TYPE      *TYPE OUT ACCIDENTALS
00425A 729B 96 28     A          LDAA   TFLAG     *PRINT (R+A)-A IF TERM MOD
00426A 729D 27 1A 72B9           BEQ    PRJP3     *DONT PRINT IF COMPUTER MO
00427A 729F 8D 1C 72BD           BSR    SP        *TYPE 3 SPACES
00428A 72A1 86 01     A          LDAA   #1        *IS (R+A)-A POSITIVE?
00429A 72A3 91 0D     A          CMPA   SIGN
00430A 72A5 27 07 72AE           BEQ    PRJP1     *NO, GO TO PRJP1
00431A 72A7 86 2B     A          LDAA   #$2B      *YES, PRINT +
00432A 72A9 BD 7326   A          JSR    SEND
00433A 72AC 20 05 72B3           BRA    PRJP2     *GO TO PRJP2
00434A 72AE 86 2D     A PRJP1    LDAA   #$2D      *PRINT -
00435A 72B0 BD 7326   A          JSR    SEND
00436A 72B3 86 47     A PRJP2    LDAA   #RAM+23   *SET START ADDR = $0047
00437A 72B5 97 11     A          STAA   F+1
00438A 72B7 8D 11 72CA           BSR    TYPE      *TYPE OUT (R+A)-A
00439A 72B9 BD 71B2   A PRJP3    JSR    CRLF      *PRINT CARRIAGE RTN,LINE F
00440A 72BC 39                   RTS              *RETURN TO CONTROL PROGRAM
00441A 72BD 86 20     A SP       LDAA   #$20      *PRINT 3 SPACES
00442                  *                           SUBROUTINE
00443A 72BF 8D 65 7326           BSR    SEND
00444A 72C1 86 20     A          LDAA   #$20
00445A 72C3 8D 61 7326           BSR    SEND
00446A 72C5 86 20     A          LDAA   #$20
00447A 72C7 8D 5D 7326           BSR    SEND
00448A 72C9 39                   RTS              *RETURN
00449                  *
00450                  ************************************
00451                  *
00452A 72CA 4F           TYPE    CLRA             *CLEAR CONTROL #'S J,P, &
00453A 72CB 97 12     A          STAA   J
00454A 72CD 97 14     A          STAA   P
00455A 72CF 97 13     A          STAA   K
00456A 72D1 DE 10     A          LDX    F         *LOAD STARTING ADDRESS IN
00457A 72D3 A6 00     A TYLP1    LDAA   0,X       *LOAD A PAIR OF DIGITS
00458A 72D5 D6 14     A          LDAB   P         *NEED LEAST SIG. DIGIT?
00459A 72D7 27 04 72DD           BEQ    B1        *NO, GO TO B1
00460A 72D9 84 0F     A          ANDA   #$F       *YES, GET LEAST SIG. 4 BIT
00461A 72DB 20 06 72E3           BRA    B2        *GO TO B2
00462A 72DD 84 F0     A B1       ANDA   #$F0      *PICK OFF MOST SIG. 4 BITS
00463A 72DF 46                   RORA             *MOVE RIGHT 4 BITS
00464A 72E0 46                   RORA
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00465A 72E1 46                 RORA
00466A 72E2 46                 RORA
00467A 72E3 4D          B2     TSTA              *DIGIT=0?
00468A 72E4 27 08 72EE         BEQ     B3        *YES, GO TO B3
00469A 72E6 C6 01     A        LDAB    #1        *NO, SET K=1
00470A 72E8 D7 13     A        STAB    K
00471A 72EA 8D 3A 7326 B5      BSR     SEND      *PRINT THE CHARACTER
00472A 72EC 20 0F 72FD         BRA     B4        *GO TO B4
00473A 72EE 7D 0013   A B3      TST     K         *K=0?
00474A 72F1 26 F7 72EA         BNE     B5        *NO, PRINT THE DIGIT
00475A 72F3 D6 0E     A        LDAB    NUM       *YES, IS THIS THE LAST DIG
00476                  *                          IN THE NUMBER?
00477A 72F5 D1 12     A        CMPB    J
00478A 72F7 27 F1 72EA         BEQ     B5        *YES, PRINT THE ZERO
00479A 72F9 86 20     A        LDAA    #$20      *NO, PRINT A SPACE
00480A 72FB 20 ED 72EA         BRA     B5
00481A 72FD 96 0E     A B4     LDAA    NUM       *IS THIS THE LAST DIGIT
00482                  *                          IN THE NUMBER?
00483A 72FF 91 12     A        CMPA    J
00484A 7301 26 01 7304         BNE     B6        *NO, GO TO B6
00485A 7303 39                 RTS               *YES, RETURN FROM SUBROUTI
00486A 7304 7C 000F   A B6      INC     COM       *INCREMENT COM
00487A 7307 86 03     A        LDAA    #3        *COM=3?
00488A 7309 91 0F     A        CMPA    COM
00489A 730B 26 07 7314         BNE     B7        *NO, GO TO B7
00490A 730D 86 20     A        LDAA    #$20      *PRINT A SPACE
00491A 730F 8D 15 7326         BSR     SEND
00492A 7311 7F 000F   A B9      CLR     COM       *SET COM=0
00493A 7314 7C 0012   A B7      INC     J         *INCREMENT J AND P
00494A 7317 7C 0014   A        INC     P
00495A 731A 86 02     A        LDAA    #2        *P=2?
00496A 731C 91 14     A        CMPA    P
00497A 731E 26 B3 72D3         BNE     TYLP1     *NO, GO TO TYLP1
00498A 7320 7F 0014   A        CLR     P         *YES, SET P=0
00499A 7323 08                 INX               *STEP TO NEXT PAIR OF DIGI
00500A 7324 20 AD 72D3         BRA     TYLP1
00501                  *
00502                  ****************************************
00503                  *
00504A 7326 81 09     A SEND   CMPA    #9        *CHARACTER>9?
00505A 7328 2E 02 732C         BGT     SEJP1     *YES, PROCEED
00506A 732A 8A 30     A        ORAA    #$30      *NO, FORM ASCII CODE
00507A 732C F6 4000   A SEJP1  LDAB    ACIAS     *LOAD STATUS OF ACIA
00508A 732F 56                 RORB
00509A 7330 56                 RORB
00510A 7331 24 F9 732C         BCC     SEJP1     *PROCEED IF ACIA IS READY
00511A 7333 B7 4001   A        STAA    ACIAT     *SEND OUT CHARACTER
00512                  *                          TO TERMINAL
00513A 7336 81 0D     A        CMPA    #$0D      *IS IT A CR?
00514A 7338 26 10 734A         BNE     DL2
00515A 733A C6 5F     A        LDAB    #$5F      *IF YES START A DELAY
00516A 733C D7 15     A DL0    STAB    DEL1
00517A 733E D7 16     A        STAB    DEL2
00518A 7340 7A 0015   A DL1    DEC     DEL1      *BEGIN DELAY
00519A 7343 26 FB 7340         BNE     DL1
00520A 7345 7A 0016   A        DEC     DEL2
00521A 7348 26 F6 7340         BNE     DL1       *DELAY FINISHED?
00522A 734A 39          DL2    RTS               *YES, RETURN
```

```
PAGE  010  RG7K11   SA:1  HLNCC

00523                    *
00524                    ****************************************
00525                    *
00526A 734B 86 4D     A HP97    LDAA   #$4D      *HP97 "CLRX"
00527A 734D 8D 4D 739C          BSR    OUT
00528A 734F 86 04     A         LDAA   #4        *SET M=4
00529A 7351 97 1C     A         STAA   M
00530A 7353 86 01     A         LDAA   #1        *SET N=1
00531A 7355 97 1A     A         STAA   N
00532A 7357 86 03     A         LDAA   #3        *SET C=3
00533A 7359 97 1B     A         STAA   C
00534A 735B CE 0030   A         LDX    #RAM      *LOAD STARTING ADDRESS
00535A 735E A6 00     A HPLP1   LDAA   0,X       *LOAD A PAIR OF DIGITS
00536A 7360 8D 25 7387          BSR    PR        *JUMP TO UNPACKING ROUTINE
00537A 7362 08                  INX              *INCREMENT THE ADDRESS
00538A 7363 7A 001B   A         DEC    C         *DECREMENT THE CONTROL NUM
00539A 7366 27 02 736A          BEQ    HPJP1
00540A 7368 20 F4 735E          BRA    HPLP1     *LOOP IF NOT ZERO
00541A 736A 86 4F     A HPJP1   LDAA   #$4F      *LOAD STORE CODE
00542A 736C 8D 2E 739C          BSR    OUT       *SEND IT OUT
00543A 736E 96 1A     A         LDAA   N         *FORM CODE FOR STORAGE
00544                    *                        ADDRESS ("OR" N WITH $40)
00545A 7370 8A 40     A         ORAA   #$40
00546A 7372 8D 28 739C          BSR    OUT       *SEND IT OUT
00547A 7374 7C 001A   A         INC    N         *INCREMENT STORAGE ADDRESS
00548                    *                        CONTROL NUMBER
00549A 7377 7A 001C   A         DEC    M         *ALL NUMBERS SENT OUT?
00550A 737A 27 06 7382          BEQ    HPJP2     *YES, LEAVE LOOP
00551A 737C 86 05     A         LDAA   #5        *NO, SET C=5 & RECYCLE
00552A 737E 97 1B     A         STAA   C
00553A 7380 20 DC 735E          BRA    HPLP1
00554A 7382 86 4A     A HPJP2   LDAA   #$4A      *LOAD CODE FOR LABEL A
00555A 7384 8D 16 739C          BSR    OUT       *SEND IT OUT
00556A 7386 39                  RTS              *RETURN TO CONTROL PROGRAM
00557A 7387 97 1D     A PR      STAA   TEM       *SAVE CONTENTS OF A IN TEM
00558A 7389 84 F0     A         ANDA   #$F0      *PICK OFF MOST SIG. BYTE
00559A 738B 44                  LSRA             *MOVE IT OVER
00560A 738C 44                  LSRA
00561A 738D 44                  LSRA
00562A 738E 44                  LSRA
00563A 738F 8A 40     A         ORAA   #$40      *FORM CODE FOR HP-97
00564A 7391 8D 09 739C          BSR    OUT       *SEND IT OUT
00565A 7393 96 1D     A         LDAA   TEM       *RECOVER DATA
00566A 7395 84 0F     A         ANDA   #$0F      *PICK OFF LEAST SIG. BYTE
00567A 7397 8A 40     A         ORAA   #$40      *FORM PROPER CODE
00568A 7399 8D 01 739C          BSR    OUT       *SEND IT OUT
00569A 739B 39                  RTS              *RETURN
00570A 739C B7 5002   A OUT     STAA   PIAO      *SEND CODE TO HP-97
00571                    *                        INTERFACE
00572A 739F C6 19     A         LDAB   #$19      *LOAD DELAY ARGUMENT
00573A 73A1 BD 733C   A         JSR    DL0       *GO TO DELAY LOOP
00574A 73A4 4F                  CLRA             *LOAD BLANK CODE TO
00575                    *                        RELEASE HP-97
00576A 73A5 B7 5002   A         STAA   PIAO
00577A 73A8 C6 20     A         LDAB   #$20
00578A 73AA 8D 733C   A         JSR    DL0       *GO TO DELAY LOOP
00579A 73AD 39                  RTS
00580                    *
```

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PAGE  011  RG7K11   SA 1  HLNCC

00581                    ****************************************
00582                    *
00583A 73AE CE 0041   A TEST   LDX    #RAM+17   *LOAD STARTING ADDRESS
00584A 73B1 0C          TEST1  CLC               *CLEAR CARRY
00585A 73B2 86 10     A        LDAA   #$10      *DECIMAL "10"
00586A 73B4 A7 00     A TEST2  STAA   0,X
00587A 73B6 8B 22     A        ADDA   #$22      *DECIMAL "22"
00588A 73B8 19                 DAA              *CONVERT SUM TO DECIMAL
00589A 73B9 09                 DEX              *DECRIMENT POINTER
00590A 73BA 8C 002F   A        CPX    #RAM-1    *LAST LOCATION
00591A 73BD 27 04 73C3         BEQ    TEST3
00592A 73BF 25 F0 73B1         BCS    TEST1     *START SEQUENCE 0123456 ET
00593A 73D1 20 F1 73B4         BRA    TEST2
00594A 73C3 BD 734B   A TEST3  JSR    HP97      *JUMP TO HP-97 OUTPUT ROUT
00595A 73C6 39                 RTS
00596                    ****
00597A 73C7 CE 7015   A VNO    LDX    #S1       *LOAD STARTING ADDRESS
00598A 73CA A6 00     A TELP1  LDAA   0,X       *LOAD VERSION NUMBER
00599A 73CC BD 7326   A        JSR    SEND      *PRINT IT
00600A 73CF 08                 INX              *INCREMENT ADDRESS
00601A 73D0 8C 7028   A        CPX    #S1+19    *HAS LAST CHAR. BEEN PRINT
00602A 73D3 26 F5 73CA         BNE    TELP1     *NO. GET NEXT CHARACTER
00603A 73D5 39                 RTS              *YES. RETURN
00604                          END
TOTAL ERRORS 00000--00000


   4001 ACIAR  00010*00093 00218 00219
   4000 ACIAS  00008*00198 00297 00299 00507
   4001 ACIAT  00009*00511
   72DD B1     00459 00462*
   72E3 B2     00461 00467*
   72EE B3     00468 00473*
   72FD B4     00472 00481*
   72EA B5     00471*00474 00478 00480
   7304 B6     00484 00486*
   7314 B7     00489 00493*
   7311 B9     00492*
   001B C      00031*00533 00538 00552
   711C CCMP   00096 00204*
   7122 CCMP1  00206*
   7124 CCMP2  00207*00216 00237 00239 00262
   7135 CCMP3  00208 00211 00215*
   7164 CCMP4  00225 00227 00236*
   7168 CCMP5  00223 00238*
   716D CCMP6  00221 00235 00240*
   002A CHAR   00046*00228 00231 00276 00281
   709D CLR    00063 00084 00126 00132*
   71AD CLRF   00166 00214 00273*
   7028 CNTRL  00053 00080*
   703C CNTRL1 00088*00109 00115 00125 00128 00244
   706F CNTRL2 00106 00110*
   7077 CNTRL3 00111 00114*
   707B CNTRL4 00113 00116*
   000F COM    00021*00407 00415 00486 00488 00492
   71B2 CRLF   00102 00234 00236 00261 00276*00439
   0015 DEL1   00026*00516 00518
```

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PAGE  012  RG7K11   SA:1  HLNCC

0016 DEL2    00027*00517 00520
733C DL0     00516*00573 00578
7340 DL1     00518*00519 00521
734A DL2     00514 00522*
000B DLY     00017*00333 00334
0010 F       00022*00404 00406 00413 00419 00423 00437 00456
0020 FAULT   00036*
734B HP97    00118 00160 00526*00594
736A HPJP1   00539 00541*
7382 HPJP2   00550 00554*
735E HPLP1   00535*00540 00553
70CE HPOUT   00067 00156*
70E8 HPOUT1  00157 00163 00167*
0029 IFLG    00045*00162 00170 00207 00274
71C1 INIT    00082 00286*
70E9 INTFLG  00071 00169*
7116 INTST   00091 00197*00215
0012 J       00023*00453 00477 00483 00493
0013 K       00024*00455 00470 00473
7202 LJP1    00322 00326*
721E LJP2    00341 00343*
71E6 LLP1    00309*00324
720F LLP2    00334*00335
71DE LOAD    00117 00150 00159 00304*
70A3 LPIA    00131 00133 00135*00181
001C M       00032*00529 00549
001A N       00030*00531 00543 00547
000E NUM     00020*00401 00411 00475 00481
739C OUT     00527 00542 00546 00555 00564 00568 00570*
0014 P       00025*00454 00458 00494 00496 00498
5001 PIACA   00006*00292
5003 PIACB   00007*00142 00145 00295
5000 PIAI    00004*00136 00137 00288 00328 00336
5002 PIAO    00005*00135 00138 00290 00308 00315 00323 00326 00570
             00576
7387 PR      00536 00557*
726C PRINT   00120 00152 00400*
72AE PRJP1   00430 00434*
72B3 PRJP2   00433 00436*
72B9 PRJP3   00426 00439*
70F3 PSTAT   00069 00175*
0017 R       00028*
0030 RAM     00047*00304 00321 00402 00412 00418 00422 00436 00534
             00583 00590
000B RAMB    00012*00016
0024 RCYC    00040*00107 00123
0027 RCYCF   00043*00108 00112 00124 00243
70BC RDOUT   00065 00147*
70CD RDOUT1  00148 00154*
7206 READ    00309 00317 00328*00329
0022 RESPB   00038*
70B6 ROF     00087 00121 00144*00153 00161
70B0 RON     00085 00116 00141*00149 00158
0025 ROPB    00041*00114
73FE RSTRT   00053*
001E RUN     00034*00105 00147 00156 00179 00267 00271
7015 S1      00075*00597 00601
732C SEJP1   00258 00505 00507*00510
```

```
7326 SEND    00104 00165 00212 00230 00233 00238 00260 00269 00278
             00280 00432 00435 00443 00445 00447 00471 00491 00504*
             00599
000D SIGN    00019*00348 00376 00429
7247 SJP1    00371 00375*
7229 SLP1    00352*00357
7239 SLP2    00362*00369
7250 SLP4    00380*00385
7260 SLP5    00389*00395
72BD SP      00409 00417 00421 00427 00441*
0038 SST     00048*00350 00361 00377 00388
007F STACK   00011*00081
0023 STAPB   00039*
70A1 START   00059 00127 00134*
70F9 STATR   00088 00122 00171 00175 00179*00209 00213 00217
70FE STATR1  00181*00194
710E STATR2  00186 00191*
719F STATT   00176 00206 00267*
71A2 STATT1  00268*00272
0026 STFLG   00042*00164 00172 00189 00193 00210 00275 00287
7099 STOP    00061 00083 00130*
0021 STOPB   00037*
7221 SUBTR   00119 00151 00348*
0019 T       00029*
73CA TELP1   00598*00602
001D TEM     00033*00557 00565
7052 TERM0   00095 00097*
7059 TERM1   00098 00100*
7062 TERM2   00101 00104*
7065 TERM3   00092 00103 00105*
73AE TEST    00086 00583*
73B1 TEST1   00584*00592
73B4 TEST2   00586*00593
73C3 TEST3   00591 00594*
0028 TFLAG   00044*00090 00204 00220 00254 00425
711F TMODE   00099 00205*
001F TOUT    00035*00110
72D3 TYLP1   00457*00497 00500
72CA TYPE    00408 00416 00420 00424 00438 00452*
000C VAL     00018*00310 00318 00343
7178 VECT    00241 00246*
717B VECT1   00247*00253
7197 VECT2   00255 00262*00265
7199 VECT3   00248 00263*
73C7 VNO     00205 00597*
7000 VTBL    00058*00246 00252
```

APPENDIX D

FORTPAN-CALLABLE DRIVER AND FORTRAN TEST PROGRAM

```
        .LIST   TTM
;*****************************************************************************
; DLV11.MAC
;
;       DLV11 FORTRAN-CALLABLE DRIVER
;
;       CALL INITDL(ENDRD,ENDWR,BUFFER,BUFSIZ)          INITIALIZES
;
;               ENDRD:  LOGICAL*1  END OF INPUT LINE CHARACTER
;               ENDWR:  LOGICAL*1  END OF OUTPUT LINE CHARACTER
;               BUFFER: LOGICAL*1  BUFFER (ARRAY) FOR USE BY THIS HANDLER
;               BUFSIZ: INTEGER*2  BUFFER SIZE
;                       BUFSIZ >= M+1 WHERE M IS THE # OF CHARACTERS IN
;                       THE LONGEST MESSAGE (INCLUDING ENDWR)
;                       (BUFFER SHOULD BE LONG ENOUGH TO HANDLE ANY
;                        STACKING OF MESSAGES WHICH MAY OCCUR)
;
;
;       CALL CLRDL                      CLEARS BUFFER OF ANY OLD INPUT
;
;
;       N = READDL(INLINE,IWAIT)                READS INPUT LINE
;                                       (DECLARE READDL INTEGER*2 !)
;
;               INLINE: LOGICAL*1 ARRAY WHERE CHARACTERS ARE STORED
;                       (NOT INCLUDING ENDRD CHARACTER)
;               IWAIT: INTEGER*2  WAIT INDICATOR
;                       0 - DO NOT WAIT FOR INPUT
;                       1 - WAIT FOR INPUT (INDEFINITELY)
;               N     : INTEGER*2   NUMBER OF CHARACTERS READ IN,
;                       NOT INCLUDING ENDRD
;                       0 - NO INPUT HAS OCCURRED
;
;
;       CALL WRITDL(OUTLIN)             WRITES OUTPUT LINE
;
;               OUTLIN: LOGICAL*1  ARRAY CONTAINING CHARACTERS
;                       TO BE SENT (ENDWR CHARACTER AT END IS NOT SENT)
;
;               NOTE: WRITDL HAS A POTENTIAL PROBLEM IN THAT OUTPUT IS
;                       NOT BUFFERED, BUT IS UNDER INTERRUPT CONTROL
;                       AFTER THE FIRST CHARACTER.  HENCE THE USER COULD
;                       CHANGE THE CONTENTS OF AN OUTPUT LINE WHILE IT IS
;                       BEING OUTPUT. TO CIRCUMVENT THIS, DO NOT USE
;                       THE SAME OUTLIN IN TWO CONSECUTIVE WRITDL CALLS.
;
;
;       SSJ 09-FEB-81
;       REV. SSJ 04-NOV-81  0935
;
;*****************************************************************************
```

```
;
        .TITLE  DLV11
        .GLOBL  INITDL,CLRDL,READDL,WRITDL
;
;
; REGISTER DEFINITIONS AND SPECIAL ADDRESSES
;
;
;
        RVEC=310                ;RECEIVE VECTOR
        XVEC=314                ;TRANSMIT VECTOR
        RCSR=176510             ;RECEIVE CONTROL/STATUS REGISTER
;
        RVEC2=RVEC+2            ;RECEIVE PSW
        XVEC2=XVEC+2            ;TRANSMIT PSW
        RBUF=RCSR+2             ;RECEIVE BUFFER
        XCSR=RCSR+4             ;TRANSMIT CONTROL/STATUS
        XBUF=RCSR+6             ;TRANSMIT BUFFER
;
        PARAM=R5                ;PARAMETER REGISTER
        SAVPTR=R4               ;SAVE POINTER REGISTER
        COUNT=R0                ;COUNT OF INPUT CHARACTERS
        WAIT=R1                 ;WAIT FLAG
;
;
;
;  INITIALIZATION ROUTINE - SET UP INTERRUPTS,
;  GET PARAMETERS
;
INITDL: CLR     @#RCSR          ;CLEAR RECEIVE STATUS
        CLR     @#XCSR          ;CLEAR TRANSMIT STATUS
        MOV     #RINTER,@#RVEC  ;SET UP RECEIVE INTERRUPT VECTOR
        MOV     #340,@#RVEC2    ;DISABLE ALL OTHER INTERRUPTS
        MOV     #XINTER,@#XVEC  ;SET UP TRANSMIT INTERRUPT VECTOR
        MOV     #340,@#XVEC2    ;DISABLE ALL OTHER INTERRUPTS
        MOVB    @2(PARAM),RENB  ;GET END-OF-INPUT CHARACTER
        MOVB    @4(PARAM),XENB  ;GET END-OF-OUTPUT CHARACTER
        MOV     6(PARAM),BUFFER ;GET ADDRESS OF BUFFER
        MOV     @10(PARAM),BUFEND       ;GET BUFFER SIZE
        ADD     BUFFER,BUFEND   ;GET LAST ADDRESS OF BUFFER (+1)
        JSR     PC,CLRDL        ;SET UP POINTERS
        MOV     #100,@#RCSR     ;ENABLE THE RECEIVE INTERRUPT NOW
        RTS     PC              ;RETURN
;
;
;  CLEAR BUFFER ROUTINE
;
CLRDL:  MOV     BUFFER,RCPTR    ;SET RECEIVE POINTER TO BEGIN OF BUFFER
        MOV     BUFFER,RDPTR    ;SAME WITH READ POINTER
        MOV     BUFFER,LNPTR    ;SAME WITH LINE POINTER
        RTS     PC              ;RETURN
```

```
;
;
;  READ ROUTINE
;
READDL: CLR     COUNT           ;RESET COUNT OF INPUT CHARACTERS
        MOV     2(PARAM),INPTR  ;GET ADDRESS FOR FIRST CHARACTER
        MOV     @4(PARAM),WAIT  ;GET WAIT FLAG
9$:     CMP     LNPTR,RDPTR     ;HAVE WE READ THE LATEST LINE ALREADY?
        BNE     3$              ;NO - A NEW LINE HAS COME IN
        TST     WAIT            ;YES - SHOULD WE WAIT?
        BEQ     7$              ;NO - USER WANTS AN IMMEDIATE RETURN
        BR      9$              ;YES - WAIT FOR A NEW LINE
3$:     INC     RDPTR           ;BUMP POINTER TO NEXT CHARACTER
        CMP     RDPTR,BUFEND    ;ARE WE AT THE END OF THE BUFFER?
        BNE     1$              ;NO
        MOV     BUFFER,RDPTR    ;YES - START AT BEGINNING OF BUFFER
1$:     CMPB    @RDPTR,REND     ;IS THIS THE END OF MESSAGE?
        BEQ     7$              ;YES - DONE, DON'T INCLUDE THIS CHAR
        MOVB    @RDPTR,@INPTR   ;NO - MOVE THE CHARACTER TO USER'S LINE
        INC     COUNT           ;ADD 1 TO CHARACTER COUNT
        INC     INPTR           ;BUMP POINTER TO USER'S LINE
        BR      3$              ;REPEAT
7$:     RTS     PC              ;RETURN
;
;
;  RECEIVE INTERRUPT ROUTINE
;  OCCURS WHEN A CHARACTER HAS COME IN AND IS READY TO BE READ
;
RINTER: INC     RCPTR           ;BUMP RECEIVE POINTER
        CMP     RCPTR,BUFEND    ;HAVE WE REACHED THE END OF BUFFER?
        BNE     1$              ;NO
        MOV     BUFFER,RCPTR    ;YES - START AT BEGINNING AGAIN
1$:     MOVB    @#RBUF,@RCPTR   ;PUT CHARACTER IN BUFFER
        CMPB    @RCPTR,REND     ;IS THIS THE LAST CHAR IN LINE?
        BNE     3$              ;NO
        MOV     RCPTR,LNPTR     ;YES - MARK THE END OF THE LINE
3$:     RTI                     ;RETURN
;
;
;  OUTPUT ROUTINE
;  USES TRANSMIT READY INTERRUPT FEATURE
;  NOTE: EXPERIENCE WITH DLV11J SHOWS THAT THE READY INTERRUPT
;        OCCURS IMMEDIATELY AFTER THE ENABLE
;
WRITDL: BIT     @#XCSR,#100     ;IS PREVIOUS OUTPUT FINISHED?
                                ; (IE, IS INTERRUPT DISABLED?)
        BNE     WRITDL          ;NO - JUST WAIT HERE TILL IT IS
        MOV     2(PARAM),SAVPTR ;GET ADDRESS OF FIRST CHARACTER
        MOV     SAVPTR,TRPTR    ;SAVE FIRST ADDRESS FOR USE LATER
        MOV     #100,@#XCSR     ;ENABLE TRANSMIT READY INTERRUPTS
        NOP                     ;WAIT A BIT
        NOP
        CMP     TRPTR,SAVPTR    ;HAS READY INTERRUPT OCCURRED JUST NOW?
        BNE     5$              ;YES - OUTPUT HAS STARTED ALREADY
        JSR     PC,SEND         ;NO - SEND OFF FIRST CHARACTER
5$:     RTS     PC              ;RETURN
;
```

```
;
;   TRANSMIT READY INTERRUPT ROUTINE
;   OCCURS WHEN TRANSMITTER IS READY TO PUT OUT ANOTHER CHARACTER
;
XINTER: JSR     PC,SEND         ;SEND NEXT CHARACTER
        RTI                     ;RETURN
;
;
;   SEND A CHARACTER SUBROUTINE
;
SEND:   CMPB    @TRPTR,XEND     ;IS THIS THE END OF MESSAGE?
        BNE     7$              ;NO - SEND THIS CHARACTER
        CLR     @#XCSR          ;YES - DISABLE INTERRUPT
        BR      5$              ;AND DON'T SEND CHAR, BUT BUMP PTR
7$:     MOVB    @TRPTR,@#XBUF   ;MOVE CHARACTER OUT
5$:     INC     TRPTR           ;BUMP POINTER TO NEXT CHARACTER
        RTS     PC              ;RETURN
;
;
;   CONSTANTS AND VARIABLES
;
;
REND:   .BYTE                   ;END-OF-INPUT CHARACTER
XEND:   .BYTE                   ;END-OF-OUTPUT CHARACTER
RCPTR:  .WORD                   ;RECEIVE POINTER (IN BUFFER)
RDPTR:  .WORD                   ;READ POINTER (IN BUFFER)
LNPTR:  .WORD                   ;END OF LAST LINE POINTER (IN BUFFER)
INPTR:  .WORD                   ;INPUT POINTER (IN USER'S INLINE)
TRPTR:  .WORD                   ;TRANSMIT POINTER (IN USER'S OUTLIN)
BUFFER: .WORD                   ;FIRST BUFFER ADDRESS
BUFEND: .WORD                   ;LAST BUFFER ADDRESS + 1
;
;
        .END
```

```
FORTRAN IV      V02.1-10   Wed 11-Feb-81                         PAGE 001
      CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
      C HLNCC
      C
      C      TEST INPUT AND OUTPUT TO HLNCC
      C      FOR SWANSEN/ENSSLIN
      C
      C      JOHNSON  04-FEB-81
      C      REV. 11-FEB-81  1130
      C
      CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
      C
0001        IMPLICIT INTEGER (A-Z)
      C
0002        LOGICAL*1 CHAR(80),INLINE(80)
0003        LOGICAL*1 BUFFER (500)
0004        LOGICAL*1 LINEFD,BLANK
      C
0005        DATA LINEFD/"12/,BLANK/' '/
      C
      C
      C  USE THE NEW FORTRAN-CALLABLE DLV11 HANDLER
      C
0006   5    CALL INITDL(LINEFD,BLANK,BUFFER,500)
0007        GO TO 20
      C
      C  LIST THE OPTIONS
      C
0008   10   TYPE 1000
0009   1000 FORMAT(/' ^ - BEGIN COMMUNICATIONS'/
          X             ' S - START'/
          X             ' H - HALT'/
          X             ' Z - CLEAR SCALERS AND TIMER'/
          X             ' R - READ DATA TO COMPUTER'/
          X             ' P - READ OUT DATA TO HP97'/
          X             ' X - REQUEST STATUS'/
          X             ' I - SET INTERRUPT FLAG'/
          X             ' F - RETURN TO FRONT PANEL CONTROL'//
          X             ' T - TEST FOR INPUT'/
          X             ' W - WAIT FOR INPUT'/
          X             ' Q - REINITIALIZE INPUT'/
          X             ' O - LIST OPTIONS'//)
      C
      C  GET OPERATOR INPUT
      C
0010   20   TYPE 1001
0011   1001 FORMAT(/'$OPTIONS -> ')
0012        ACCEPT 1002,CHAR
0013   1002 FORMAT(80A1)
      C
      C  TEST FOR SPECIAL CHARACTERS
      C
0014        IF(CHAR(1) .EQ. 'O') GO TO 10
0016        IF(CHAR(1) .EQ. 'T') GO TO 50
0018        IF(CHAR(1) .EQ. 'W') GO TO 40
```

```
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0020          IF(CHAR(1) .EQ. 'Q') GO TO 5
      C
      C  ASSUME CHARACTER ARE GOOD - SEND TO HLNCC
      C
0022          CALL WRITDL(CHAR)
0023          GO TO 20
      C
      C  READ IN RESPONSE FROM THE HLNCC
      C
0024   40     IWAIT = 1
0025          GO TO 55
      C
0026   50     IWAIT = 0
0027   55     N = READDL(INLINE,IWAIT)
      C
      C  CHECK THE RESPONSE
      C
0028          IF(N .EQ. 0) TYPE 1007
0030   1007 FORMAT(/' NO INPUT FROM HLNCC'/)
0031          IF(N .EQ. 0) GO TO 20
      C
      C  SEE IF THIS RESPONSE IS AN INTERRUPT FOR STATUS CHANGE
      C
0033          IF(N .EQ. 2) GO TO 100
      C
      C  THIS IS A DATA LINE - NOT AN INTERRUPT
      C
0035          TYPE 1008,(INLINE(I),I=1,N-1)
0036   1008 FORMAT(/' DATA FROM HLNCC:'//1X,80A1/)
0037          GO TO 20
      C
      C  THIS IS AN INTERRUPT
      C
0038   100    TYPE 1009,INLINE(1)
0039   1009 FORMAT(/' STATUS INTERRUPT FROM HLNCC:'//1X,A1/)
0040          GO TO 20
      C
0041          END


FORTRAN IV      Storage Map for Program Unit .MAIN.

Local Variables, .PSECT $DATA, Size = 001240 (  336. words)

Name   Type  Offset     Name   Type  Offset     Name   Type  Offset
BLANK  L*1   001225     I      I*2   001234     IWAIT  I*2   001230
LINEFD L*1   001224     N      I*2   001232

Local and COMMON Arrays:

Name     Type   Section Offset  -------Size------ Dimensions
BUFFER L*1      $DATA   000240  000764 (  250.) (500)
CHAR   L*1      $DATA   000000  000120 (   40.) (80)
INLINE L*1      $DATA   000120  000120 (   40.) (80)

Subroutines, Functions, Statement and Processor-Defined Functions:

Name    Type    Name    Type    Name    Type    Name    Type    Name    Type
INITDL  I*2     READDL  I*2     WRITDL  I*2

                                                                  43

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APPENDIX C

HLNCC (PROM) VERSION 1.2; ORIGINAL PROM LISTING

The software in this PROM was developed to provide the following capabilities for the HLNCC:

(a) Transmit data and control statements to a HP-97 calculator.

(b) Transmit data by RS-232 serial port (to a terminal, for "hard copy").

(c) Implement a software "recycle mode" to allow continuous data collection.

This version (V 1.2) does <u>not</u> provide for remote control of the HLNCC.

```
PAGE  001   CONTROL
00001                          NAM     CONTROL
00002                          OPT     O
00003 7000                     ORG     $7000
00004 7000 0F                  SEI                 *DISABLE INTERRUPT
00005 7001 8E 007F             LDS     $STACK      *LOAD STACK POINTER
00006 7004 BD 70B5             JSR     INIT        *JUMP TO INITIALIZE ROUTINE
00007 7007 86 29               LDA A   #$29        *LOAD RESET CODE INTO PIA
00008 7009 B7 5002             STA A   PIAO
00009 700C BD 70A9             JSR     RON         *TURN ON READOUT LIGHT
00010 700F BD 7394             JSR     TEST        *JUMP TO TEST SUBROUTINE
00011 7012 BD 70AF             JSR     ROF         *TURN OFF READOUT LIGHT
00012 7015 86 28               LDA A   #$28        *LOAD STOP CODE INTO PIA
00013 7017 B7 5002             STA A   PIAO
00014 701A 7F 0017 LP3         CLR     S           *SET S=0
00015 701D 7F 0018             CLR     T           *SET T=0
00016 7020 20 2E               BRA     JP4         *GO TO WAITING LOOP
00017 7022 86 30   LP1         LDA A   #$30        *WAIT FOR SR TO STOP
00018 7024 BD 709F             JSR     CHECK
00019 7027 2A F9               BPL     LP1
00020 7029 86 31               LDA A   #$31        *DID THE SR TIME OUT?
00021 702B BD 709F             JSR     CHECK
00022 702E 2B 05               BMI     JP1         *YES, GO TO JP1
00023 7030 7F 0018             CLR     T           *NO, SET T=0
00024 7033 20 05               BRA     JP2
00025 7035 C6 01   JP1         LDA B   #1          *SET T=1
00026 7037 F7 0018             STA B   T
00027 703A 86 36   JP2         LDA A   #$36        *IS SR IN RECYCLE MODE?
00028 703C BD 709F             JSR     CHECK
00029 703F 2B 0C               BMI     JP3         *NO, GO TO JP3
00030 7041 C6 01               LDA B   #1          *YES, SET R=1
00031 7043 F7 0016             STA B   R
00032 7046 F1 0018             CMP B   T           *T=1?
00033 7049 27 1A               BEQ     JP5         *YES
00034 704B 20 03               BRA     JP4         *NO
00035 704D 7F 0016 JP3         CLR     R           *SET R=0
00036 7050 86 30   JP4         LDA A   #$30        *IS SR STOPPED?
00037 7052 BD 709F             JSR     CHECK
00038 7055 2A CB               BPL     LP1         *NO, GO TO LP1
00039 7057 86 34               LDA A   #$34        *YES; IS SR RESET DEPRESSED?
00040 7059 BD 709F             JSR     CHECK
00041 705C 2B BC               BMI     LP3         *YES, GO TO LP3
00042 705E 86 37               LDA A   #$37        *NO; IS SR READOUT DEPRESSED
00043 7060 BD 709F             JSR     CHECK
00044 7063 2A EB               BPL     JP4         *NO, GO TO WAIT LOOP
00045 7065 BD 70A9 JP5         JSR     RON         *TURN ON READOUT LIGHT
00046 7068 BD 7136             JSR     LOAD        *READ THE DISPLAY
00047 706B BD 730B             JSR     HP97        *SEND RESULTS TO HP-97
00048 706E BD 7189             JSR     SUBTR       *SUBTRACT A FROM R+A
00049 7071 4F                  CLR A               *S=0?
00050 7072 B1 0017             CMP A   S
00051 7075 26 06               BNE     JP6         *NO, GO TO JP6
00052 7077 BD 70D0             JSR     TITLE       *YES, PRINT THE TITLE
00053 707A 7C 0017             INC     S           *SET S=1
00054 707D BD 71DF JP6         JSR     TYPE        *PRINT RESULTS
00055 7080 BD 70AF             JSR     ROF         *TURN OFF READOUT LIGHT
00056 7083 4F                  CLR A               *T=0?
00057 7084 B1 0018             CMP A   T
00058 7087 27 C7               BEQ     JP4         *YES, GO TO WAITING LOOP
```

```
00059 7089 B1 0016          CMP A  R        *NO; R=0?
00060 708C 27 C2            BEQ    JP4      *YES, GO TO JP4
00061 708E 86 29            LDA A  #$29     *NO, RESET THE SR
00062 7090 B7 5002          STA A  PIA0
00063 7093 86 2A            LDA A  #$2A     *START THE SR
00064 7095 B7 5002          STA A  PIA0
00065 7098 86 2B            LDA A  #$2B     *LOAD UNUSED CONTROL NUMBER
00066                  *                     TO REMOVE MICROPROCESSOR
00067                  *                     CONTROL
00068 709A B7 5002          STA A  PIA0
00069 709D 20 83            BRA    LP1      *WAIT FOR SR TO STOP
00070 709F B7 5002 CHECK    STA A  PIA0     *SEND OUT STATUS CODE
00071 70A2 B6 5000          LDA A  PIAI     *READ STATUS
00072 70A5 B6 5000          LDA A  PIAI     *REDUNDANT READ STATUS
00073 70A8 39               RTS             *RETURN
00074 70A9 86 3C    RON     LDA A  #$3C     *LOAD CONTROL REG. CODE
00075 70AB B7 5003          STA A  PIACB    *SEND IT OUT
00076 70AE 39               RTS             *RETURN
00077 70AF 86 34    ROF     LDA A  #$34     *LOAD CONTROL REG. CODE
00078 70B1 B7 5003          STA A  PIACB    *SEND IT OUT
00079 70B4 39               RTS             *RETURN
00080       0016    R       EQU    $16
00081       0017    S       EQU    $17
00082       0018    T       EQU    $18
00083       007F    STACK   EQU    $7F
00084       7394    TEST    EQU    $7394
00085       70B5    INIT    EQU    $70B5
00086       7136    LOAD    EQU    $7136
00087       70D0    TITLE   EQU    $70D0
00088       71DF    TYPE    EQU    $71DF
00089       7189    SUBTR   EQU    $7189
00090       5000    PIAI    EQU    $5000
00091       5002    PIA0    EQU    $5002
00092       5003    PIACB   EQU    $5003
00093       730B    HP97    EQU    $730B
00094               END

TOTAL ERRORS 00000
```

```
PAGE  001   INITIALI
00001                       NAM    INITIALIZE
00002                       OPT    O
00003       5000    PIAI    EQU    $5000    *PIA A DATA REGISTER ADDRESS
00004       5002    PIAO    EQU    $5002    *PIA B DATA REGISTER ADDRESS
00005       5001    PIACA   EQU    $5001    *PIA A CONTROL REG. ADDR.
00006       5003    PIACB   EQU    $5003    *PIA B CONTROL REG. ADDR.
00007       4000    ACIAS   EQU    $4000    *ACIA STATUS ADDRESS
00008       7000    CNTRL   EQU    $7000    *CONTROL PROGRAM ADDRESS
00009       73FE    RSTRT   EQU    $73FE    *RESTART ADDRESS
00010 73FE                  ORG    RSTRT
00011 73FE 7000     RSTRT   FDB    CNTRL    *POINTER TO CONTROL PROGRAM
00012 70B5                  ORG    $70B5
00013 70B5 4F               CLR A           *CLEAR ACCUMULATOR A
00014 70B6 B7 5000          STA A  PIAI     *DEFINE A SIDE AS INPUT
00015 70B9 43               COM A
00016 70BA B7 5002          STA A  PIAO     *DEFINE B SIDE AS OUTPUT
```

```
00017 70BD 86 04          LDA A  #$4
00018 70BF B7 5001        STA A  PIACA     *CHANGE FROM DATA DIRECTION
00019                     *                 REGISTER TO DATA REGISTER
00021 70C2 B7 5003        STA A  PIACB     *DITTO
00022 70C5 86 03          LDA A  #$3       *MASTER RESET
00023 70C7 B7 4000        STA A  ACIAS
00024 70CA 86 09          LDA A  #$9       *SET UP DATA FORMAT
00025 70CC B7 4000        STA A  ACIAS
00026 70CF 39             RTS
00027                     END

TOTAL ERRORS 00000



PAGE  001   TITLE
00001                     NAM    TITLE
00002 70D0                ORG    $70D0
00003                     OPT    O
00004 70D0 CE 70DF        LDX    #S        *LOAD STARTING ADDRESS
00005 70D3 A6 00    LP1   LDA A  O,X       *LOAD A CHARACTER
00006 70D5 BD 72DB        JSR    SEND      *PRINT IT
00007 70D8 08             INX              *INCREMENT ADDRESS
00008 70D9 8C 712D        CPX    #E+6      *LAST CHARACTER?
00009 70DC 26 F5          BNE    LP1       *NO, LOOP UNTIL DONE
00010 70DE 39             RTS              *YES, RETURN TO
00011               *                       CONTROL PROGRAM
00012               *CARRIAGE RETURN = CR
00013               *LINE FEED = LF
00014               *SPACE = SP
00015 70DF 0D0A     S     FDB    $0D0A,$2054,$494D,$4528,$5345,$4329
      70E1 2054
      70E3 494D
      70E5 4528
      70E7 5345
      70E9 4329
00016               *CR,LF,SP,TIME(SEC)
00017 70EB 2020           FDB    $2020,$2020,$2020,$2020,$2020,$544F
      70ED 2020
      70EF 2020
      70F1 2020
      70F3 2020
      70F5 544F
00018               * 10SP,TO
00019 70F7 5441           FDB    $5441,$4C53,$2020,$2020,$2020,$2020
      70F9 4C53
      70FB 2020
      70FD 2020
      70FF 2020
      7101 2020
00020               * TALS,8SP
00021 7103 2020           FDB    $2020,$2020,$2052,$2B41,$2020,$2020
      7105 2020
      7107 2052
      7109 2B41
      710B 2020
      710D 2020
00022               * 5SP,R+A,4SP
00023 710F 2020           FDB    $2020,$2020,$2020,$2020,$2020,$2041
```

```
      7111 2020
      7113 2020
      7115 2020
      7117 2020
      7119 2041
00024                 * 11SP,A
00025 711B 2020       E       FDB     $2020,$2020,$2020,$2020,$2020,$2020
      711D 2020
      711F 2020
      7121 2020
      7123 2020
      7125 2020
00026                 * 12SP
00027 7127 2020       E       FDB     $2020,$2020,$5220
      7129 2020
      712B 5220
00028                 * 4SP,R,SP
00029       72DB      SEND    EQU     $72DE
00030                         END

TOTAL ERRORS 00000
```

```
PAGE  001   LOAD
00001                         NAM     LOAD
00002                         OPT     O
00003       7136      LOAD    EQU     $7136
00004       0030      RAM     EQU     $30       *SET UP LOCATION FOR DATA
00005                 *                          STORAGE
00006 7136                    ORG     LOAD
00007 7136 CE 0030            LDX     #RAM      *LOAD INDEX REGISTER WITH
00008                 *                          FIRST STORAGE LOCATION
00009 7139 86 01              LDA A   #1        *LOAD CONTROL CODE "1" INTO
00010                 *                          PIA B DATA REGISTER
00011 713B B7 5002            STA A   $5002
00012 713E BD 7162 LP1        JSR     READ      *READ DIGIT; STORE IN VAL
00013 7141 F6 000C            LDA B   VAL       *MOVE DIGIT LEFT
00014 7144 58                 ASL B
00015 7145 58                 ASL B
00016 7146 58                 ASL B
00017 7147 58                 ASL B
00018 7148 7C 5002            INC     $5002     *INCREMENT CONTROL CODE
00019                 *                          FOR NEXT DIGIT
00020 714B BD 7162            JSR     READ      *READ THE DIGIT
00021 714E FA 000C            ORA B   VAL       *FORM A 2-DIGIT PAIR
00022 7151 E7 00              STA B   0,X       *STORE RESULT AT POINTER
00023 7153 08                 INX               *INCREMENT POINTER
00024 7154 8C 0042            CPX     #$42      *POINTER=42?
00025 7157 27 05              BEQ     JP1       *YES, GO TO JP1
00026 7159 7C 5002            INC     $5002     *NO, INCREMENT CONTROL CODE
00027 715C 20 E0              BRA     LP1       *BRANCH TO READ NEXT
00028                 *                          PAIR OF DIGITS
00029 715E 7F 5002 JP1        CLR     $5002     *REMOVE CONTROL CODE
00030 7161 39                 RTS               *RETURN FROM SUBROUTINE
00031 7162 B6 5000 READ       LDA A   $5000     *LOAD THE PIA A DATA REGISTE
00032 7165 2B FB              BMI     READ      *PROCEED IF POSITIVE
00033                 *                          (DATA PRESENT)
00034 7167 86 FF              LDA A   #$FF      *ALLOW DELAY FOR
```

```
00035                    *                              SETTLING TIME
00036 7169 B7 000B            STA A  DLY
00037 716C 7A 000B LP2        DEC    DLY
00038 716F 26 FB              BNE    LP2
00039 7171 B6 5000            LDA A  $5000        *LOAD THE PIA A DATA
00040                    *                              REGISTER REDUNDANTLY
00041 7174 84 0F              AND A  #$F          *STRIP OFF LEAST
00042                    *                              SIGNIFICANT 4 BITS
00043 7176 81 0F              CMP A  #$F          *DATA=F?
00044 7178 26 01              BNE    JP2          *NO, PROCEED
00045 717A 4F                 CLR A               *YES, CHANGE TO ZERO
00046 717B B7 000C JP2        STA A  VAL          *STORE RESULT IN VAL
00047 717E 39                 RTS                 *RETURN FROM SUBROUTINE
00048      000B     DLY       EQU    $B
00049      000C     VAL       EQU    $C
00050                         END

TOTAL ERRORS 00000
```

```
PAGE  001   SUBTRACT
00001                         NAM    SUBTRACT
00002                         OPT    0
00003 7189                    ORG    $7189
00004 7189 7F 000D            CLR    SIGN         *CLEAR SIGN CONTROL
00005                    *                              CONSTANT (0 FOR +; 1 FOR -)
00006 718C CE 0038            LDX    #S           *LOAD STARTING ADDRESS
00007 718F C6 05              LDA B  #5           *LOAD CONTROL CONSTANT
00008 7191 86 99   LP1        LDA A  #$99         *LOAD $99
00009 7193 A0 09              SUB A  9,X          *SUBTRACT TO COMPLEMENT
00010 7195 A7 0E              STA A  $E,X         *STORE COMPLEMENT
00011 7197 09                 DEX                 *DECREMENT ADDRESS
00012 7198 5A                 DEC B               *DECREMENT CONTROL NUMBER
00013 7199 26 F6              BNE    LP1          *RECYCLE UNTIL ALL DIGITS
00014                    *                              ARE COMPLEMENTED
00015 719B 0D                 SEC                 *SET THE CARRY
00016 719C C6 05              LDA B  #5           *LOAD CONTROL NUMBER
00017 719E CE 0038            LDX    #S           *LOAD STARTING ADDRESS
00018 71A1 A6 04   LP2        LDA A  4,X          *LOAD PAIR OF DIGITS
00019                    *                              FOR ADDITION
00020 71A3 A9 0E   JP5        ADC A  $E,X         *ADD WITH CARRY
00021 71A5 19                 DAA                 *DECIMAL ADJUST
00022 71A6 A7 13              STA A  $13,X        *STORE SUM
00023 71A8 09                 DEX                 *DECREMENT ADDRESS
00024 71A9 5A                 DEC B               *DECREMENT CONTROL NUMBER
00025 71AA 26 F5              BNE    LP2          *RECYCLE UNTIL ADDITION
00026                    *                              IS COMPLETE
00027 71AC 24 01              BCC    JP1          *BRANCH TO JP1 IF
00028                    *                              CARRY IS CLEAR
00029 71AE 39                 RTS                 *RETURN TO CONTROL PROGRAM
00030                    *                              IF CARRY IS SET
00031 71AF 86 01   JP1        LDA A  #1           *CHANGE SIGN TO -
00032 71B1 B7 000D            STA A  SIGN
00033 71B4 CE 0038            LDX    #S           *REVERSE SUBTRAHEND AND
00034                    *                              MINUEND AND REPEAT
00035 71B7 C6 05              LDA B  #5
00036 71B9 86 99   LP4        LDA A  #$99
```

```
00037 71BB A0 13          SUB A  $13,X
00038 71BD A7 13          STA A  $13,X
00039 71BF 09             DEX
00040 71C0 5A             DEC B
00041 71C1 26 F6          BNE    LP4
00042 71C3 0D             SEC
00043 71C4 C6 05          LDA B  #5
00044 71C6 CE 0038        LDX    #S
00045 71C9 86 00    LP5   LDA A  #0
00046 71CB A9 13          ADC A  $13,X
00047 71CD 19             DAA
00048 71CE A7 13          STA A  $13,X
00049 71D0 09             DEX
00050 71D1 5A             DEC B
00051 71D2 26 F5          BNE    LP5
00052 71D4 39             RTS
00053      0038    S      EQU    $38
00054      000D    SIGN   EQU    $D
00055                     END

TOTAL ERRORS 00000


PAGE  001   PRINT
00001                     NAM    PRINT
00002                     OPT    O
00003      000D    SIGN   EQU    $D
00004      000E    NUM    EQU    $E
00005      000F    COM    EQU    $F
00006      0010    F      EQU    $10
00007      72DB    SEND   EQU    $72DB
00008      725A    TYPE   EQU    $725A
00009 71DF                ORG    $71DF
00010 71DF 86 0D          LDA A  #$D      *PRINT CARRIAGE RETURN (CR)
00011 71E1 BD 72DB        JSR    SEND
00012 71E4 86 0A          LDA A  #$A      *PRINT LINE FEED (LF)
00013 71E6 BD 72DB        JSR    SEND
00014 71E9 BD 7240        JSR    SP       *PRINT 3 SPACES
00015 71EC 86 05          LDA A  #$5      *SET NUM=5
00016 71EE 97 0E          STA A  NUM
00017 71F0 86 30          LDA A  #$30     *LOAD STARTING ADDRESS
00018                *                     ($0030) AT F, F+1
00019 71F2 97 11          STA A  F+1
00020 71F4 7F 0010        CLR    F
00021 71F7 7F 000F        CLR    COM      *SET COM=0
00022 71FA BD 725A        JSR    TYPE     *TYPE OUT TIME
00023 71FD BD 7240        JSR    SP       *PRINT 3 SPACES
00024 7200 86 09          LDA A  #$9      *SET NUM=9
00025 7202 97 0E          STA A  NUM
00026 7204 86 33          LDA A  #$33     *SET STARTING ADDRESS = $003
00027 7206 97 11          STA A  F+1
00028 7208 86 02          LDA A  #$2      *SET COM=2
00029 720A 97 0F          STA A  COM
00030 720C BD 725A        JSR    TYPE     *TYPE OUT TOTALS
00031 720F BD 7240        JSR    SP       *PRINT 3 SPACES
00032 7212 86 38          LDA A  #$38     *SET STARTING ADDRESS = $003
00033 7214 97 11          STA A  F+1
00034 7216 BD 725A        JSR    TYPE     *TYPE OUT R+A
```

```
00035 7219 BD 7240         JSR     SP        *PRINT 3 SPACES
00036 721C 86 3D           LDA A   #$3D      *SET STARTING ADDRESS = $003
00037 721E 97 11           STA A   F+1
00038 7220 BD 725A         JSR     TYPE      *TYPE OUT ACCIDENTALS
00039 7223 BD 7240         JSR     SP        *TYPE 3 SPACES
00040 7226 86 01           LDA A   #1        *IS (R+A)-A POSITIVE?
00041 7228 91 0D           CMP A   SIGN
00042 722A 27 07           BEQ     JP1       *NO, GO TO JP1
00043 722C 86 2B           LDA A   #$2B      *YES, PRINT +
00044 722E BD 72DB         JSR     SEND
00045 7231 20 05           BRA     JP2       *GO TO JP2
00046 7233 86 2D    JP1    LDA A   #$2D      *PRINT -
00047 7235 BD 72DB         JSR     SEND
00048 7238 86 47    JP2    LDA A   #$47      *SET STARTING ADDRESS = $004
00049 723A 97 11           STA A   F+1
00050 723C BD 725A         JSR     TYPE      *TYPE OUT (R+A)-A
00051 723F 39              RTS               *RETURN TO CONTROL PROGRAM
00052 7240 86 20    SP     LDA A   #$20      *PRINT 3 SPACES
00053                      *                  SUBROUTINE
00054 7242 BD 72DB         JSR     SEND
00055 7245 86 20           LDA A   #$20
00056 7247 BD 72DB         JSR     SEND
00057 724A 86 20           LDA A   #$20
00058 724C BD 72DB         JSR     SEND
00059 724F 39              RTS               *RETURN
00060                      END

TOTAL ERRORS 00000
```

```
PAGE  001   TYPE
00001                      NAM     TYPE
00002                      OPT     O
00003 725A                 ORG     $725A
00004 725A 7F 0012 TYPE    CLR     J         *CLEAR CONTROL #'S J,P, & K
00005 725D 7F 0014         CLR     P
00006 7260 7F 0013         CLR     K
00007 7263 FE 0010         LDX     F         *LOAD STARTING ADDRESS IN X
00008 7266 A6 00    LP1    LDA A   0,X       *LOAD A PAIR OF DIGITS
00009 7268 7D 0014         TST     P         *NEED LEAST SIG. DIGIT?
00010 726B 27 04           BEQ     B1        *NO, GO TO B1
00011 726D 84 0F           AND A   #$F       *YES, GET LEAST SIG. 4 BITS
00012 726F 20 06           BRA     B2        *GO TO B2
00013 7271 84 F0    B1     AND A   #$F0      *PICK OFF MOST SIG. 4 BITS
00014 7273 46              ROR A             *MOVE RIGHT 4 BITS
00015 7274 46              ROR A
00016 7275 46              ROR A
00017 7276 46              ROR A
00018 7277 4D       B2     TST A             *DIGIT=0?
00019 7278 27 0A           BEQ     B3        *YES, GO TO B3
00020 727A C6 01           LDA B   #1        *NO, SET K=1
00021 727C F7 0013         STA B   K
00022 727F BD 72DB B5      JSR     SEND      *PRINT THE CHARACTER
00023 7282 20 11           BRA     B4        *GO TO B4
00024 7284 7D 0013 B3      TST     K         *K=0?
00025 7287 26 F6           BNE     B5        *NO, PRINT THE DIGIT
00026 7289 F6 000E         LDA B   NUM       *YES; IS THIS THE LAST DIGIT
00027                      *                  IN THE NUMBER?
```

```
00028 728C F1 0012        CMP B  J
00029 728F 27 EE          BEQ    B5        *YES, PRINT THE ZERO
00030 7291 86 20          LDA A  #$20      *NO, PRINT A SPACE
00031 7293 20 EA          BRA    B5
00032 7295 B6 000E B4     LDA A  NUM       *IS THIS THE LAST DIGIT
00033                     *                 IN THE NUMBER?
00034 7298 B1 0012        CMP A  J
00035 729B 26 01          BNE    B6        *NO, GO TO B6
00036 729D 39             RTS              *YES, RETURN FROM SUBROUTINE
00037 729E 7C 000F B6     INC    COM       *INCREMENT COM
00038 72A1 86 03          LDA A  #3        *COM=3?
00039 72A3 B1 000F        CMP A  COM
00040 72A6 26 16          BNE    B7        *NO, GO TO B7
00041 72A8 86 01          LDA A  #1        *YES; K=1?
00042 72AA B1 0013        CMP A  K
00043 72AD 26 07          BNE    B8        *NO, GO TO B8
00044 72AF 86 2C          LDA A  #$2C      *YES, PRINT A COMMA
00045 72B1 BD 72DB        JSR    SEND
00046 72B4 20 05          BRA    B9        *GO TO B9
00047 72B6 86 20    B8    LDA A  #$20      *PRINT A COMMA
00048 72B8 BD 72DB        JSR    SEND
00049 72BB 7F 000F B9     CLR    COM       *SET COM=0
00050 72BE 7C 0012 B7     INC    J         *INCREMENT J AND P
00051 72C1 7C 0014        INC    P
00052 72C4 86 02          LDA A  #2        *P=2?
00053 72C6 B1 0014        CMP A  P
00054 72C9 26 9B          BNE    LP1       *NO, GO TO LP1
00055 72CB 7F 0014        CLR    P         *YES, SET P=0
00056 72CE 08             INX              *STEP TO NEXT PAIR OF DIGITS
00057 72CF 20 95          BRA    LP1
00058       72DB    SEND  EQU    $72DB
00059       000E    NUM   EQU    $E
00060       000F    COM   EQU    $F
00061       0010    P     EQU    $10
00062       0012    J     EQU    $12
00063       0013    K     EQU    $13
00064       0014    P     EQU    $14
00065                     END

TOTAL ERRORS 00000
```

```
PAGE  001   SEND
00001                     NAM    SEND
00002                     OPT    O
00003 72DB                ORG    $72DB
00004 72DB 81 09          CMP A  #9        *CHARACTER>9?
00005 72DD 2E 02          BGT    PT        *YES, PROCEED
00006 72DF 8A 30          ORA A  #$30      *NO, FORM ASCII CODE
00007 72E1 C6 01    PT    LDA B  #1        *SET DELAY CONSTANT = 1
00008 72E3 F7 0015        STA B  DEL
00009 72E6 81 0D          CMP A  #$0D      *IS CHARACTER<$0E?
00010 72E8 2E 05          BGT    JP1       *NO, PROCEED
00011 72EA C6 08          LDA B  #8        *YES, SET DELAY CONSTANT = 8
00012 72EC F7 0015        STA B  DEL
00013 72EF F6 4000 JP1    LDA B  ACIAS     *LOAD STATUS OF ACIA
00014 72F2 56             ROR B
```

```
00015 72F3 56              ROR B
00016 72F4 24 F9           BCC     JP1       *PROCEED IF ACIA IS READY
00017 72F6 B7 4001         STA A   ACIAT     *SEND OUT CHARACTER
00018                 *                      TO TERMINAL
00019 72F9 86 7F           LDA A   #$7F      *LOAD UNUSED CODE
00020 72FB 7A 0015         DEC     DEL       *IS DELAY FINISHED?
00021 72FE 26 EF           BNE     JP1       *NO, LOOP TO JP1
00022 7300 39              RTS               *YES, RETURN
00023      4000    ACIAS   EQU     $4000     *(ACIA STATUS ADDRESS)
00024      4001    ACIAT   EQU     $4001     *(ACIA DATA ADDRESS)
00025      0015    DEL     EQU     $15
00026              END

TOTAL ERRORS 00000
```

```
PAGE  001   HP97
00001              NAM     HP97
00002              OPT     O
00003 730B         ORG     $730B
00004 730B 86 04   LDA A   #4        *SET M=4
00005 730D B7 001B STA A   M
00006 7310 86 01   LDA A   #1        *SET N=1
00007 7312 B7 0019 STA A   N
00008 7315 86 03   LDA A   #3        *SET C=3
00009 7317 B7 001A STA A   C
00010 731A CE 0030 LDX     #$30      *LOAD STARTING ADDRESS
00011 731D A6 00   LP1     LDA A   0,X       *LOAD A PAIR OF DIGITS
00012 731F BD 7350 JSR     PR        *JUMP TO UNPACKING ROUTINE
00013 7322 08      INX               *INCREMENT THE ADDRESS
00014 7323 7A 001A DEC     C         *DECREMENT THE CONTROL NUMBE
00015 7326 27 02   BEQ     JP1
00016 7328 20 F3   BRA     LP1       *LOOP IF NOT ZERO
00017 732A 86 4F   JP1     LDA A   #$4F      *LOAD STORE CODE
00018 732C BD 7369 JSR     OUT       *SEND IT OUT
00019 732F B6 0019 LDA A   N         *FORM CODE FOR STORAGE
00020              *                      ADDRESS ("OR" N WITH $40)
00021 7332 8A 40   ORA A   #$40
00022 7334 BD 7369 JSR     OUT       *SEND IT OUT
00023 7337 7C 0019 INC     N         *INCREMENT STORAGE ADDRESS
00024              *                      CONTROL NUMBER
00025 733A 7A 001B DEC     M         *ALL NUMBERS SENT OUT?
00026 733D 27 07   BEQ     JP2       *YES, LEAVE LOOP
00027 733F 86 05   LDA A   #5        *NO, SET C=5 & RECYCLE
00028 7341 B7 001A STA A   C
00029 7344 20 D7   BRA     LP1
00030 7346 86 4A   JP2     LDA A   #$4A      *LOAD CODE FOR LABEL A
00031 7348 BD 7369 JSR     OUT       *SEND IT OUT
00032 734B 4F      CLR A             *LOAD BLANK CODE TO
00033              *                      RELEASE HP-97
00034 734C BD 7369 JSR     OUT       *SEND IT OUT
00035 734F 39      RTS               *RETURN TO CONTROL PROGRAM
00036 7350 B7 001C PR      STA A   TEM       *SAVE CONTENTS OF A IN TEM
00037 7353 84 F0   AND A   #$F0      *PICK OFF MOST SIG. BYTE
00038 7355 44      LSR A             *MOVE IT OVER
00039 7356 44      LSR A
```

```
00040 7357 44              LSR A
00041 7358 44              LSR A
00042 7359 8A 40           ORA A  #$40     *FORM CODE FOR HP-97
00043 735B BD 7369         JSR    OUT      *SEND IT OUT
00044 735E B6 001C JP3     LDA A  TEM      *RECOVER DATA
00045 7361 84 0F           AND A  #$0F     *PICK OFF LEAST SIG. BYTE
00046 7363 8A 40           ORA A  #$40     *FORM PROPER CODE
00047 7365 BD 7369         JSR    OUT      *SEND IT OUT
00048 7368 39        JP4   RTS             *RETURN
00049 7369 B7 5002 OUT     STA A  $5002    *SEND CODE TO HP-97
00050                      *                INTERFACE
00051 736C BD 7377         JSR    D        *GO TO DELAY LOOP
00052 736F 4F              CLR A           *LOAD BLANK CODE TO
00053                      *                RELEASE HP-97
00054 7370 B7 5002         STA A  $5002
00055 7373 BD 7377         JSR    D        *GO TO DELAY LOOP
00056 7376 39              RTS
00057 7377 86 FF    D      LDA A  #$FF     *LOAD $FF AS TIMING CONTROL
00058 7379 BD 7380 LP2     JSR    DLY      *JUMP TO SECOND DELAY LOOP
00059 737C 4A              DEC A           *DECREMENT CONTROL NUMBER
00060 737D 26 FA           BNE    LP2      *RECYCLE IF NONZERO
00061 737F 39              RTS             *RETURN TO OUTPUT SUBROUTINE
00062 7380 C6 26    DLY    LDA B  #$26     *LOAD $26 AS TIMING CONTROL
00063 7382 5A       LP3    DEC B           *DECREMENT B
00064 7383 26 FD           BNE    LP3      *RECYCLE IF NONZERO
00065 7385 39              RTS             *RETURN TO PRIMARY DELAY LOO
00066      0019    N      EQU    $19
00067      001A    C      EQU    $1A
00068      001B    M      EQU    $1B
00069      001C    TEM    EQU    $1C
00070                     END

TOTAL ERRORS 00000
```

```
PAGE  001   TEST
00001                     NAM    TEST
00002                     OPT    O
00003 7394                ORG    $7394
00004 7394 CE 0030        LDX    #$30     *LOAD STARTING ADDRESS
00005 7397 C6 03          LDA B  #$3      *LOAD CONTROL NUMBER
00006 7399 86 44          LDA A  #$44     *STORE 444444 FOR TIME
00007 739B BD 73DE        JSR    ST
00008 739E 86 33          LDA A  #$33     *STORE 3333333333 FOR TOTALS
00009 73A0 BD 73DE        JSR    ST
00010 73A3 86 22          LDA A  #$22     *STORE 2222222222 FOR R+A
00011 73A5 BD 73DE        JSR    ST
00012 73A8 86 11          LDA A  #$11     *STORE 1111111111 FOR A
00013 73AA BD 73DE        JSR    ST
00014 73AD BD 730B        JSR    HP       *JUMP TO HP-97 OUTPUT ROUTIN
00015 73B0 CE 73BF        LDX    #S1      *LOAD STARTING ADDRESS
00016 73B3 A6 00    LP1   LDA A  0,X      *LOAD A CHARACTER
00017 73B5 BD 72DB        JSR    SEND     *PRINT IT
00018 73B8 08             INX             *INCREMENT ADDRESS
00019 73B9 8C 73DE        CPX    #ST      *HAS LAST CHAR. BEEN PRINTED
00020 73BC 26 F5          BNE    LP1      *NO, GET NEXT CHARACTER
00021 73BE 39             RTS             *YES, RETURN
```

```
00022                    *CARRIAGE RETURN = CR
00023                    *LINE FEED = LF
00024                    *SPACE =SP
00025 73BF 0D0A     S1   FDB    $0D0A,$0A0A
      73C1 0A0A
00026                    *CR,LF,LF,LF
00027 73C3 484C          FDB    $484C,$4E43
      73C5 4E43
00028 73C7 43            FCB    $43
00029                    *HLNCC
00030 73C8 0D0A          FDB    $0D0A
00031                    *CR,LF
00032 73CA 5620          FDB    $5620,$312E
      73CC 312E
00033 73CE 32            FCB    $32
00034                    *V,SP,1.2
00035 73CF 0D0A          FDB    $0D0A
00036                    *CR,LF
00037 73D1 3132          FDB    $3132,$204A,$554C,$2037
      73D3 204A
      73D5 554C
      73D7 2037
00038 73D9 38            FCB    $38
00039                    *12,SP,JUL,SP,78
00040 73DA 0D0A          FDB    $0D0A,$0A0A
      73DC 0A0A
00041                    *CR,LF,LF,LF
00042 73DE A7 00    ST   STA A  0,X       *STORE $44,33,22, OR 11
00043 73E0 08            INX              *INCREMENT STORAGE ADDRESS
00044 73E1 5A            DEC B            *DECREMENT CONTROL NUMBER
00045 73E2 26 FA         BNE    ST        *REPEAT IF NOT ZERO
00046 73E4 C6 05         LDA B  #$5       *LOAD NEW CONTROL NUMBER
00047 73E6 39            RTS              *RETURN
00048      730B     HP   EQU    $730B
00049      72DB     SEND EQU    $72DB
00050                    END

TOTAL ERRORS 00000
```

PROM LISTING

HLNCC V 1.2 12 July 1978

```
7000 0F 8E 00 7F BD 70 B5 86 29 B7 50 02 BD 70 A9 BD
7010 73 94 BD 70 AF 86 28 B7 50 02 7F 00 17 7F 00 18
7020 20 2E 86 30 BD 70 9F 2A F9 86 31 BD 70 9F 2B 05
7030 7F 00 18 20 05 C6 01 F7 00 18 86 36 BD 70 9F 2B
7040 0C C6 01 F7 00 16 F1 00 18 27 1A 20 03 7F 00 16
7050 86 30 BD 70 9F 2A CB 86 34 BD 70 9F 2B BC 86 37
7060 BD 70 9F 2A EB BD 70 A9 BD 71 36 BD 73 0B BD 71
7070 89 4F B1 00 17 26 06 BD 70 D0 7C 00 17 BD 71 DF
7080 BD 70 AF 4F B1 00 18 27 C7 B1 00 16 27 C2 86 29
7090 B7 50 02 86 2A B7 50 02 86 2B B7 50 02 20 83 B7
70A0 50 02 B6 50 00 B6 50 00 39 86 3C B7 50 03 39 86
70B0 34 B7 50 03 39 4F B7 50 00 43 B7 50 02 86 04 B7
70C0 50 01 B7 50 03 86 03 B7 40 00 86 09 B7 40 00 39
70D0 CE 70 DF A6 00 BD 72 DB 08 8C 71 2D 26 F5 39 0D
70E0 0A 20 54 49 4D 45 28 53 45 43 29 20 20 20 20 20
70F0 20 20 20 20 20 54 4F 54 41 4C 53 20 20 20 20 20
7100 20 20 20 20 20 20 20 20 52 2B 41 20 20 20 20 20
7110 20 20 20 20 20 20 20 20 20 20 41 20 20 20 20 20
7120 20 20 20 20 20 20 20 20 20 20 20 52 20
7130                     CE 00 30 86 01 B7 50 02 BD 71
7140 62 F6 00 0C 58 58 58 58 7C 50 02 BD 71 62 FA 00
7150 0C E7 00 08 8C 00 42 27 05 7C 50 02 20 E0 7F 50
7160 02 39 B6 50 00 2B FB 86 FF B7 00 0B 7A 00 0B 26
7170 FB B6 50 00 84 0F 81 0F 26 01 4F B7 00 0C 39
7180                           7F 00 0D CE 00 38 C6
7190 05 86 99 A0 09 A7 0E 09 5A 26 F6 0D C6 05 CE 00
71A0 38 A6 04 A9 0E 19 A7 13 09 5A 26 F5 24 01 39 86
71B0 01 B7 00 0D CE 00 38 C6 05 86 99 A0 13 A7 13 09
71C0 5A 26 F6 0D C6 05 CE 00 38 86 00 A9 13 19 A7 13
71D0 09 5A 26 F5 39                                 86
71E0 0D BD 72 DB 86 0A BD 72 DB BD 72 40 86 05 97 0E
71F0 86 30 97 11 7F 00 10 7F 00 0F BD 72 5A BD 72 40
7200 86 09 97 0E 86 33 97 11 86 02 97 0F BD 72 5A BD
7210 72 40 86 38 97 11 BD 72 5A BD 72 40 86 3D 97 11
7220 BD 72 5A BD 72 40 86 01 91 0D 27 07 86 2B BD 72
7230 DB 20 05 86 2D BD 72 DB 86 47 97 11 BD 72 5A 39
7240 86 20 BD 72 DB 86 20 BD 72 DB 86 20 BD 72 DB 39
7250                           7F 00 12 7F 00 14
7260 7F 00 13 FE 00 10 A6 00 7D 00 14 27 04 84 0F 20
7270 06 84 F0 46 46 46 46 4D 27 0A C6 01 F7 00 13 BD
7280 72 DB 20 11 7D 00 13 26 F6 F6 00 0E F1 00 12 27
7290 EE 86 20 20 EA B6 00 0E B1 00 12 26 01 39 7C 00
72A0 0F 86 03 B1 00 0F 26 16 86 01 B1 00 13 26 07 86
72B0 2C BD 72 DB 20 05 86 20 BD 72 DB 7F 00 0F 7C 00
72C0 12 7C 00 14 86 02 B1 00 14 26 9B 7F 00 14 08 20
72D0 95                                 81 09 2E 02 8A
72E0 30 C6 01 F7 00 15 81 0D 2E 05 C6 08 F7 00 15 F6
72F0 40 00 56 56 24 F9 B7 40 01 86 7F 7A 00 15 26 EF
7300 39                                 86 04 B7 00 1B
7310 86 01 B7 00 19 86 03 B7 00 1A CE 00 30 A6 00 BD
7320 73 50 08 7A 00 1A 27 02 20 F3 86 4F BD 73 69 B6
7330 00 19 8A 40 BD 73 69 7C 00 19 7A 00 1B 27 07 86
7340 05 B7 00 1A 20 D7 86 4A BD 73 69 4F BD 73 69 39
7350 B7 00 1C 84 F0 44 44 44 44 8A 40 BD 73 69 B6 00
7360 1C 84 0F 8A 40 BD 73 69 39 B7 50 02 BD 73 77 4F
7370 B7 50 02 BD 73 77 39 86 FF BD 73 80 4A 26 FA 39
7380 C6 26 5A 26 FD 39
7390                  CE 00 30 C6 03 86 44 BD 73 DE 86 33
73A0 BD 73 DE 86 22 BD 73 DE 86 11 BD 73 DE BD 73 0B
73B0 CE 73 BF A6 00 BD 72 DB 08 8C 73 DE 26 F5 39 0D
73C0 0A 0A 0A 48 4C 4E 43 43 0D 0A 56 20 31 2E 32 0D
73D0 0A 31 32 20 4A 55 4C 20 37 38 0D 0A 0A 0A A7 00
73E0 08 5A 26 FA C6 05 39
73F0                                                70 00
```

Note: Blank areas are unused memory locations that may contain random hexadecimal codes.

APPENDIX D

NONSTANDARD LSI AND HYBRID COMPONENTS DATA

The data sheets in this section were selected primarily on the basis of whether or not the described component was a standard series component. For instance, most of the 74xx TTL and 4xxx/14xxx metal oxide semiconductor (MOS) components in the HLNCC are listed in manufacturers' and second source data books, so the data should be readily available. Within the three sections of this appendix, the components are listed, first, alphabetically, and then by the initial digits in the device number.

TELEDYNE PHILBRICK

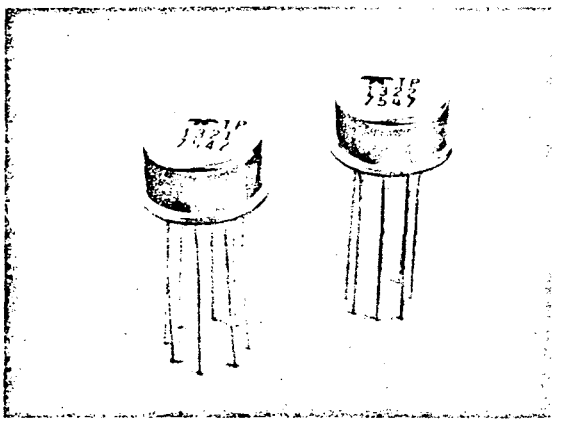
1321/1322 WIDEBAND, HIGH SLEW RATE OPERATIONAL AMPLIFIERS

The 1321 and 1322 are amplifiers packaged in TO-99 cases which are second to none in low cost, high frequency, high speed, and precision performance. Each has been optimized for a particular set of applications.

These are true differential input amplifiers with stable 6 dB per octave gain vs frequency plots from maximum open loop gain to closed loop gains between 3 and 10.

The 1321 should be used for precision settling (to 0.01%), high frequency precision closed loop gain, or low bias current. Applications include a low cost, fast 12-bit voltage DAC from a fast current DAC, fast integrators, and high gain precision differential input video amplifiers.

The 1322 should be used when the 120 V/μsec slew rate, or 1.6 MHz full power frequency is required (both @ ±10 V into 500 Ω).



APPLICATION

As with all high frequency devices, optimum performance from the 1321 and 1322 demands care in lead length, bypassing, and stray capacity. When operating at closed loop gains of less than 10, compensation techniques may be required at the bandwidth control pin (pin 8) for stable operation. They are mandatory with closed loop gains below 3.

Most applications operating at a gain of less than 10 are stabilized by connecting a 20 pF capacitor between pin 8 and ground. The effect on the amplifier's Bode plot by the stabilizing capacitor is shown in Figure 2. When gains of greater than 10 are used, care should be taken to minimize stray capacity to pin 8. When maximum speed/frequency response is required, pin 8 should be cut off close to the TO-99 case.

When optimum response and settling time are required at gains of less than 10, the amplifier must be "fooled" and operated at a gain greater than 10 at high frequency as shown in Figure 1.

These amplifiers will usually operate better with a 50 pF load capacitor and 5 to 20 pF in parallel with the feedback resistor. Short, individual lines should be run from the power supply to $\pm V_{CC}$ and to circuit power common. In addition, + and $-V_{CC}$ pins should be bypassed to common at the device with 1 μF tantalum capacitors in parallel with 0.01 μF ceramic discs.

Maximum initial E_{OS} is 10 mV for the 1322 and 5 mV for the 1321, so most low gain high frequency circuits do not require zero trim components. However, an optional potentiometer may be used as shown. Note, the wiper of potentiometer is connected to $+V_{CC}$.

A feature of both amplifiers is their ability to drive a ±10 V high frequency signal into a 500 Ω to 1 kΩ load. This high output current is available with a quiescent current of less than 4 mA in the 1321 and 6 mA in the 1322.

FEATURES

- Low Cost
- Fast Settling – 0.01% in < 1 μsec
- Slew Rate – 120 V/μsec
- Full Power – 1.6 MHz
- Open Loop Gain – 100 dB
- Unity Gain BW – 100 MHz
- E_{out} – ±18 V @ ±20 mA

APPLICATIONS

- Fast – High Frequency
  - Current to Voltage Converters
  - Video Amplifiers
  - Differential Amplifiers
  - Line Drivers
- Wideband Precision

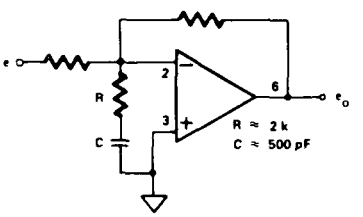


Figure 1. Optional Stabilizing Scheme (for unity gain stability at high speed)

1321/1322

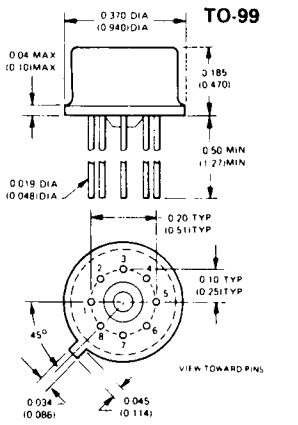
SPECIFICATIONS (at 25°C, V_{CC} = ±15 V, R_L = 2K, unless otherwise indicated.)

	1321		1322	
	Typical	Guaranteed	Typical	Guaranteed
OUTPUT RANGE (R_L = 1K)				
Voltage	±12 V	±10 V	±12 V	±10 V
Current	±20 mA	±10 mA	±20 mA	±10 mA
VOLTAGE GAIN (dc Open Loop)	100 dB	98 dB	84 dB	76 dB
FREQUENCY RESPONSE (Inverting)				
Small Signal (Unity Gain, Open Loop)	100 MHz ① ②	70 MHz	20 MHz ①	---
Max Peak to Peak Out (Triangle Wave)	600 kHz ④	320 kHz	1.6 MHz ③	1.2 MHz
Slew Rate	35 V/µsec ④	20 V/µsec	120 V/µsec	80 V/µsec
Settling Time 0.1%	400 nsec	---	200 nsec	---
Settling Time 0.01%	1.0 µsec	---	3.0 µsec	---
INPUT VOLTAGE RANGE				
Common Mode (dc Linear Operation)	±12 V	±11 V	±12 V	±10 V
Differential (between inputs)	±12 V	---	±15 V	---
Common Mode Rejection Ratio (dc)	100 dB	---	90 dB	---
INPUT OFFSET VOLTAGE				
Initial (without External Trim)	±3 mV	±5 mV	±5 mV	±10 mV
Zero Adjustment (Optional)	---	100 kΩ pot	---	20 kΩ pot
Vs. Temperature	30 µV/°C ⑤	---	30 µV/°C ⑤	---
Vs. Power Supply	30 µV/V	---	30 µV/V	---
INPUT BIAS CURRENT				
Initial at 25°C	±5 nA	±25 nA	100 nA	250 nA
Offset (Tracking)	5 nA	25 nA	20 nA	50 nA
Offset vs. Temperature	±0.5 nA/°C ⑤	±0.8 nA/°C ⑤	±0.1 nA/°C ⑤	±0.5 nA/°C ⑤
INPUT IMPEDANCE				
Differential	300 MΩ	40 MΩ	100 MΩ	40 MΩ
Common Mode (either Input to Common)	1000 MΩ	---	1000 MΩ	---
NOISE (Referred to Input)				
Voltage rms				
Flicker (0.016 Hz to 1.6 Hz)	4 µV (p/p)	---	---	---
Midband (1.6 Hz to 160 Hz)	0.6 µV (rms)	---	---	---
Highband (160 Hz to 16 kHz)	0.8 µV (rms)	---	---	---
Wideband (10 Hz to 10 kHz)	1 µV (rms)	---	1 µV (rms)	---
POWER REQUIREMENTS				
Voltage Range	±8 V to ±22 V	---	±8 V to +20 V	---
Current: Quiescent	±3 mA	±4 mA	±4 mA	±6 mA
TEMPERATURE RANGE				
Operating (°C)	---	0 to 70	---	0 to 75
Operating (1321-01 · 1322-01) (°C)	---	-55 to +125	---	-55 to +125
Storage (°C)	---	-65 to +150	---	-65 to +150

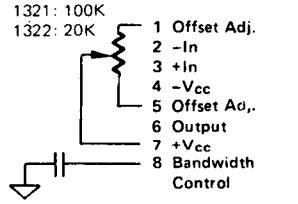
① G x BW @ A = 10
② @ A_{CL} = 1, f_t = 10 MHz (Typical)
③ $A_{CL} \geq 3$
④ $A_{CL} \geq 5$
⑤ Average 0 to +70°C for 1321, average -55 to +125°C for 1321-01.
⑥ Average 0°C to 75°C for 1322, average -55°C to +125°C for 1322-01.

The input circuits of these units are protected to ±Vcc. Output circuits are short-circuit protected to ground.

Recommended Power Supply: Teledyne Philbrick Model 2211



Optional Eos Trim
1321: 100K
1322: 20K



20 pF stabilizing capacitor for closed loop gains less than 10

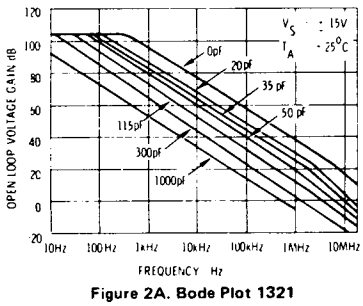


Figure 2A. Bode Plot 1321

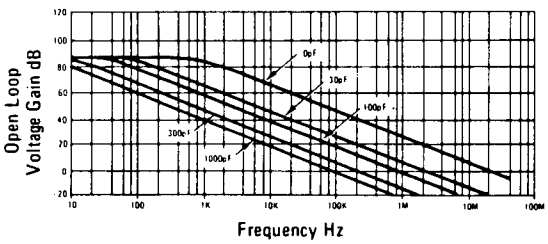


Figure 2B. Bode Plot 1322

TELEDYNE PHILBRICK
Allied Drive @ Rte. 128, Dedham, Massachusetts 02026
Tel: (617) 329-1600, TWX: (710) 348-6726, Tlx: 92-4439

2M Reprinted in U.S.A. 4/81

Am0026/Am0026C
5MHz Two-Phase MOS Clock Driver

Distinctive Characteristics

- 20 ns rise and fall times with 1000 pF load
- 20 V output voltage swing
- ±1.5 amps output current drive
- High speed 5 to 10 MHz depending on load
- 100% reliability assurance testing in compliance with MIL-STD-883
- Mixing privileges for obtaining price discounts. Refer to price list.

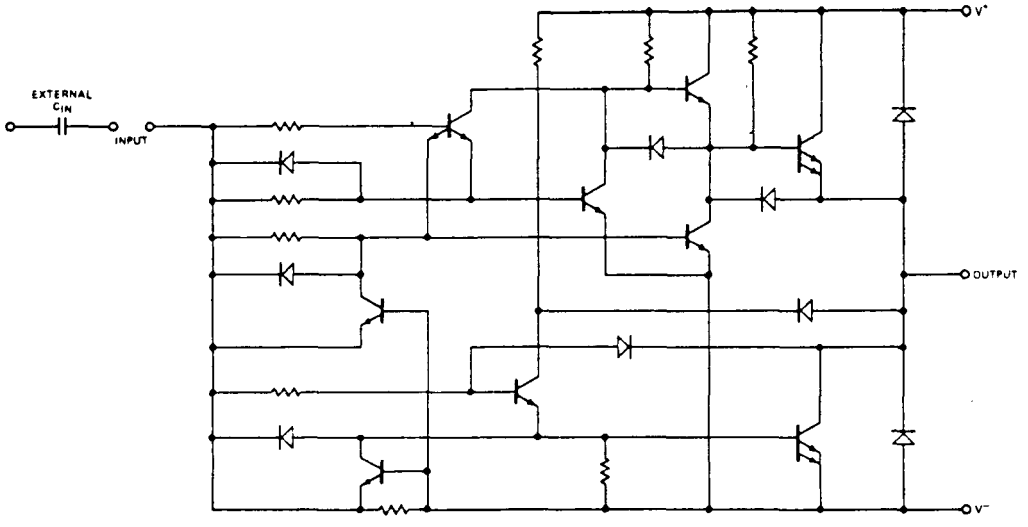
FUNCTIONAL DESCRIPTION

The Am0026 is a dual high speed MOS clock driver and interface circuit. The device is particularly suitable for driving two phase MOS circuits and can provide high speed operation even when driving into high capacitive loads. The device accepts standard TTL/DTL outputs and converts them to MOS logic levels. The output pulse width of the device is determined by the input pulse width.

The Am0026 can operate with a variety of MOS circuits. A popular application is a two-phase clock timer for driving long silicon gate shift registers such as the Am1402/3/4 series. A single clock driver is able to drive 10k bits at 5MHz. The device can also be used with standard dynamic MOS RAMS such as the 1103 to provide address and precharge drive for memories up to 8k by 16-bits.

The device is available in an 8-lead TO-5, one watt copper lead frame 8-pin mini-DIP, a one and one-half watt TO-8 package, and a 14-pin ceramic package.

SCHEMATIC DIAGRAM
(One Driver Shown)

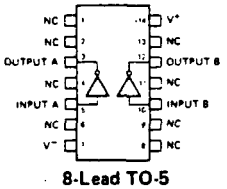


ORDERING INFORMATION

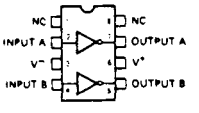
Package Type	Temperature Range	Order Number
8-Pin TO-5	0°C to 85°C	MH0026CH
8-Pin Mini-DIP	0°C to 85°C	MH0026CN
12-Pin TO-8	0°C to 85°C	MH0026CG
14-Pin Ceramic DIP	0°C to 85°C	MMH0026CL
Dice	0°C to 85°C	AM0026XC
8-Pin TO-5	−55°C to +125°C	MH0026H
12-Pin TO-8	−55°C to +125°C	MH0026G
14-Pin Ceramic DIP	−55°C to +125°C	MMH0026L
Dice	−55°C to +125°C	AM0026XM

CONNECTION DIAGRAMS
Top Views

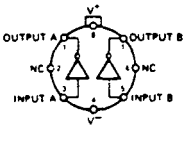
14-Pin Ceramic DIP



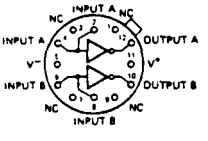
8-Pin Mini DIP



8-Lead TO-5



12-Lead TO-8



MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
$V^+ - V^-$ Differential Voltage	22 V
Input Current	100 mA
Input Voltage ($V_{IN} - V^-$)	5.5 V
Peak Output Current	1.5 A
Power Dissipation	See curves

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am0026C T_A = 0°C to 85°C (COM Range) $V^+ - V^-$ = 10 V to 20 V
Am0026 T_A = −55°C to +125°C (MIL Range) Unless Otherwise Specified

Parameter	Description	Test Conditions (Note 1)	Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V^+ = +5.0 V, V^- = −12.0 V, V_{IN} = −9.5 V		−11.5	−11.0	Volts
		$V_{IN} - V^-$ = 2.5 V		V^- +0.5	V^- +1.0	
V_{OL}	Output LOW Voltage	V^+ = +5.0 V, V^- = −12.0 V, V_{IN} = −11.6 V	4.0	4.3		Volts
		$V_{IN} - V^-$ = 0.4 V	V^+ −1.0	V^+ −0.7		
V_{IH}	Input HIGH Level	V_{OUT} = V^- +1.0 V	2.5	1.5		Volts
V_{IL}	Input LOW Level	V_{OUT} = V^+ −1.0 V		0.6	0.4	Volts
I_{IL}	Input LOW Current	$V_{IN} - V^-$ = 0 V, V_{OUT} = V^+ −1.0 V		−0.005	−10	μA
I_{IH}	Input HIGH Current	$V_{IN} - V^-$ = 2.5 V, V_{OUT} = V^- +1.0 V		10	15	mA
$I_{CC\,ON}$	"ON" Supply Current	$V^+ - V^-$ = 20 V, $V_{IN} - V^-$ = 2.5 V		30	40	mA
$I_{CC\,OFF}$	"OFF" Supply Current	$V^+ - V^-$ = 20 V, $V_{IN} - V^-$ = 0.0 V		1.0	100	μA

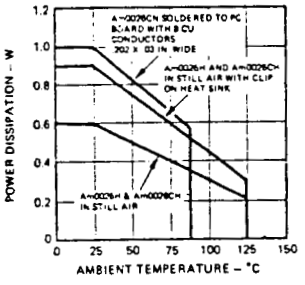
Notes: 1. These specifications apply for $V^+ - V^-$ = 10 V to 20 V, C_L = 1000 pF, over the temperature range −55°C to +125°C for the Am0026 and 0°C to +85°C for the Am0026C.
2. All typical values for T_A = 25°C.

Switching Characteristics (Notes 1 and 2 Above)

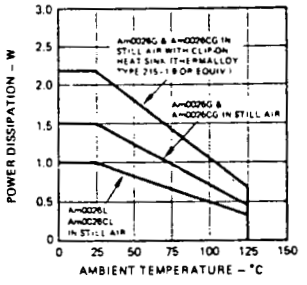
Parameter	Description	Test Conditions	Min.	Typ.	Max.	Units
t_{PHL}	Turn On Delay		5.0	7.5	12	ns
t_{PLH}	Turn Off Delay		5.0	12	15	ns
t_r	Rise Time (Note 3)	$V^+ - V^-$ = 17 V, C_L = 250 pF		12		ns
		$V^+ - V^-$ = 17 V, C_L = 500 pF		15	18	
		$V^+ - V^-$ = 17 V, C_L = 1000 pF		20	35	
t_f	Fall Time (Note 3)	$V^+ - V^-$ = 17 V, C_L = 250 pF		10		ns
		$V^+ - V^-$ = 17 V, C_L = 500 pF		12	16	
		$V^+ - V^-$ = 17 V, C_L = 1000 pF		17	25	

TYPICAL PERFORMANCE CHARACTERISTICS

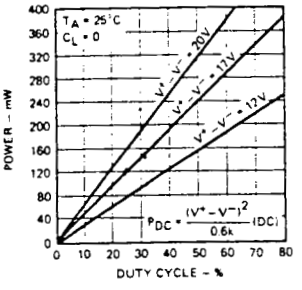
Power Ratings
TO-5 & 8-Pin DIP



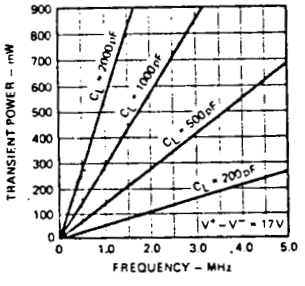
Power Rating
TO-8 & 14-Pin DIP



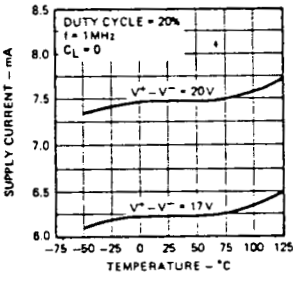
DC Power (P_{DC})
Versus Duty Cycle



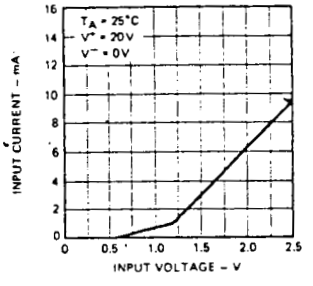
Transient Power (P_{AC})
Versus Frequency



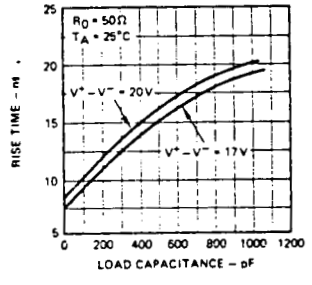
Supply Current
Versus Temperature



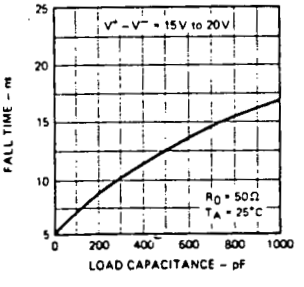
Input Current
Versus Input Voltage



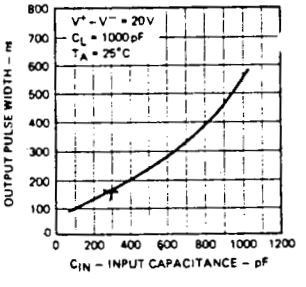
Rise Time
Versus Load Capacitance



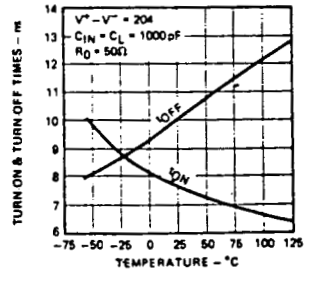
Fall Time
Versus Load Capacitance



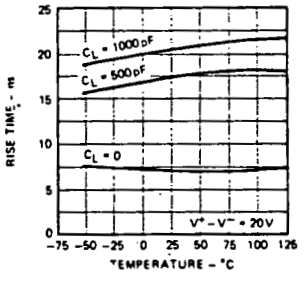
Optimum Input Capacitance
Versus Output Pulse Width



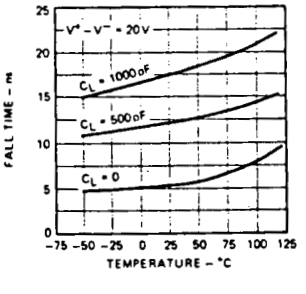
Turn-On & Turn-Off Time
Versus Temperature



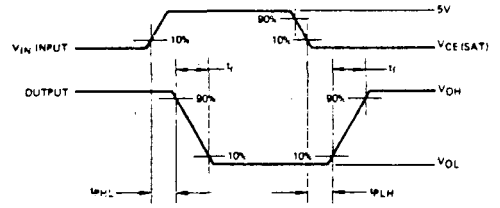
Rise Time
Versus Temperature



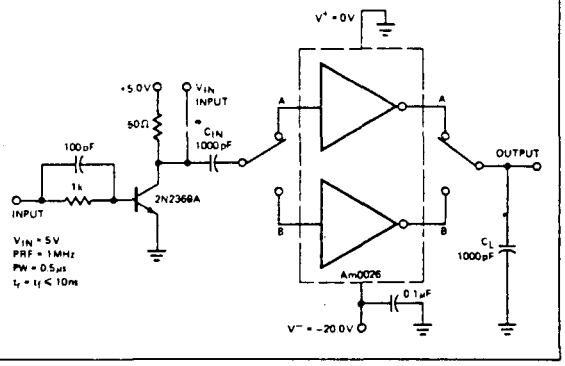
Fall Time
Versus Temperature



SWITCHING TIME WAVEFORMS



AC TEST CIRCUIT



APPLICATION INFORMATION

POWER DISSIPATION

The total average power dissipation of the Am0026 is the sum of the DC power and AC transient power. This total must be less than the given package power rating.

$$P_{DISS} = P_{AC} + P_{DC} \leq P_{MAX.}$$

With the device dissipating only 2 mW when the output is at a HIGH voltage (MOS logic "0"), the dominant factor in average DC power is the duty cycle or fraction of the time the output is at a LOW voltage level (MOS logic "1"). For the shift register driving where the duty cycle is less than 25%, P_{DC} is usually negligible. For RAM address line driver applications P_{DC} dominates since duty cycle can exceed 50%.

DC Power per driver:

DC power is given by,

$$P_{DC} = (V^+ - V^-) \times I_{S(LOW)} \times \text{Duty Cycle}$$

where $I_{S(LOW)}$ is $I_{SUPPLY(ON)}$ at $(V^+ - V^-)$

$$I_{SUPPLY(ON)} \text{ is } 40\text{ mA} \times \frac{(V^+ - V^-)}{20\text{ V}} \text{ worst case}$$

$$\text{or } 30\text{ mA} \times \frac{(V^+ - V^-)}{20\text{ V}} \text{ typically}$$

AC transient power per driver:

AC transient power is given by,

$$P_{AC} = (V^+ - V^-)^2 \times C_L \times f \times 10^{-3} \text{ in mW}$$

where f = frequency of operation in MHz and C_L = load capacitance including all strays and wiring in pF.

PACKAGE SELECTION

Power ratings are based on a maximum junction rating of 175°C. The following guidelines are suggested for package selection. Graphs shown in the Performance Curves illustrate derating for various operating temperatures.

TO-5 ("H") Package: Rated at 600 mW in still air (derate at 4.0 mW/°C above 25°C) and rated at 900 mW with clip-on heat sink (derate at 6.0 mW/°C above 25°C). This popular hermetic package is recommended for small systems. Low cost (about 10¢) clip-on-heat sink increases driving power dissipation capability by 50%.

8-pin ("N") Molded Mini-DIP: Rated at 600 mW still air (derate at 4.0 mW/°C above 25°C) and rated at 1.0 watt soldered to PC board (derate at 6.6 mW/°C). Constructed with a special copper lead frame, this package is recommended for medium size commercial systems particularly where automatic insertion is used. (Please note for prototype work, that this package is only rated at 600 mW when mounted in a socket and not one watt until it is soldered down.)

$$C_L \text{ (max.)} = \frac{10^3}{n} \frac{(P_{max.} \text{ Req} - 10^3 (V^+ - V^-)^2 \text{ Duty Cycle})}{\text{Req } (V^+ - V^-)^2 \times f}$$

where n is the number of drivers used in the package.

$P_{max.}$ is the package power rating in milliwatts for given package, heat sink, and maximum ambient temperature.

Req is the equivalent resistance $(V^+ - V^-)/I_{S(LOW)} = 500\Omega$ (worst case over temperature or 600 Ω (typically).

Duty cycle is the fraction of the time that the output signal is in the LOW state.

f is the input signal frequency in MHz.

$C_{L(max.)}$ is the maximum load capacitance per driver in picofarads which can be driven without exceeding device power limits.

When used as a non-overlapping two phase driver with each side operating at the same frequency and duty cycle, and with $(V^+ - V^-)$ -17 V, the above equation simplifies to

$$C_L = \frac{10^3}{f} \left[\frac{P_{max.}}{578} - \text{Duty Cycle} \right]$$

Table I gives maximum drive capability for various system conditions using the above equation.

PULSE WIDTH CONTROL

The Am0026 is intended for applications in which the input pulse width sets the output pulse width; i.e., the output pulse width is logically controlled by the input pulse. The output pulse width is given by:

$$(PW)_{OUT} = (PW)_{IN} + t_r + t_f = PW_{IN} + 25\text{ ns}$$

Two external input coupling capacitors are required to perform the level translation between TTL/DTL and MOS logic levels. Selection of the capacitor size is determined by the desired output pulse width. Minimum delay and optimum performance is attained when the voltage at the input of the Am0026 discharges to just above the devices threshold (about 1.5 V). If the input is allowed to discharge below the threshold, t_r and t_f will be degraded. The graph in the Performance Curves shows optimum values for C_{IN} versus desired output pulse width. The value for C_{IN} may be roughly predicted by:

$$C_{IN} = (2 \times 10^{-3}) \ (PW)_{OUT}$$

For an output pulse width of 500 ns, the optimum value for C_{IN} is:

$$C_{IN} = (2 \times 10^{-3}) \ (500 \times 10^{-9}) = 1000\text{ pF}$$

RISE AND FALL TIME CONSIDERATIONS (Note 3)

The Am0026's peak output current is limited to 1.5 A. The peak current limitation restricts the maximum load capacitance which the device is capable of driving and is given by:

$$I = C_L \frac{dv}{dt} \leq 1.5\,A$$

The rise time, t_r, for various loads may be predicted by:

$$t_r = (\Delta V)\ (250 \times 10^{-12} + C_L)$$

Where: ΔV = the change in voltage across C_L

$$\cong V^+ - V^-$$

C_L = The load capacitance

for $V^+ - V^- = 20V$, $C_L = 1000pF$, t_r is:

$$t_r \cong (20\ V)\ (250 \times 10^{-12} + 1000 \times 10^{-12})$$

$$= 25\ ns$$

For small values of C_L, the equation above predicts optimistic values for t_r. The graph in the performance curves shows typical rise times for various load capacitances.

The output fall time (see Graph) may be predicted by:

$$t_f \cong 2.2\,R\left(C_S + \frac{C_L}{h_{FE}+1}\right)$$

CLOCK OVERSHOOT

The output waveform of the Am0026 can overshoot. The overshoot is due to finite inductance of the clock lines. It occurs on the negative going edge when Q_7 saturates, and on the positive edge when Q_3 turns OFF as the output goes through $V^+ - V_{be}$. The problem can be eliminated by placing a small series resistor in the output of the Am0026. The critical valve for $R_S = 2L\ C_L$ where L is the self-inductance of the clock line. In practice, determination of a value for L is rather difficult. However, R_S is readily determined emperically, and values typically range between 10 and 51Ω. R_S does reduce rise and fall times as given by:

$$t_r = t_f \cong 2.2 R_S\ C_L$$

CLOCK LINE CROSS TALK

At the system level, voltage spikes from ϕ_1 may be transmitted to ϕ_2 (and vice-versa) during the transition of ϕ_1 to MOS logic "1". The spike is due to mutual capacitance between clock lines and is, in general, aggravated by long clock lines when numerous registers are being driven. Transistors Q_3 and Q_4 on the ϕ_2 side of the Am0026 are essentially "OFF" when ϕ_2 is in the MOS logic "0" state since only micro-amperes are drawn from the device. When the spike is coupled to ϕ_2, the output has to drop at least $2\,V_{BE}$ before Q_3 and Q_4 come on and pull the output back to V^+. A simple method for eliminating or minimizing this effect is to add bleed resistors between the Am0026 outputs and ground causing a current of a few milliamps to flow in Q_4. When a spike is coupled to the clock line Q_4 is already "ON" with a finite h_{fe}. The spike is quickly clamped by Q_4. Values for R depend on layout and the number of registers being driven and vary typically between 2 k and 10 kΩ.

POWER SUPPLY DECOUPLING

Adequate power supply decoupling is necessary for satisfactory operation. Decoupling of V^+ to V^- supply lines with at least 0.1 μF noninductive capacitors as close as possible to each Am0026 is strongly recommended. This decoupling is necessary because otherwise 1.5 ampere currents flow during logic transition in order to rapidly charge clock lines.

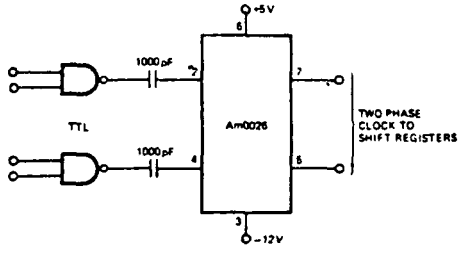
TABLE I – WORST CASE MAXIMUM DRIVE CAPABILITY FOR Am0026*

Package Type		TO-8 with Heat Sink		TO-8 Free Air		Mini-DIP Soldered Down		TO-5 and Mini-DIP Free Air		14-Pin DIP Soldered Down
Max. Operating Frequency	Duty Cycle / Max. Ambient Temp.	60°C	85°C	60°C	85°C	60°C	85°C	60°C	85°C	70°C
100kHz	5%	30k	24k	19k	15k	13k	10k	7.5k	5.1k	11k
500kHz	10%	6.5k	5.1k	4.1k	3.2k	2.5k	1.9k	1.4k	1.1k	2k
1MHz	20%	2.9k	2.2k	1.8k	1.4k	1.1k	840	600	420	860
2MHz	25%	1.4k	1.1k	850	650	540	400	280	190	390
5MHz	25%	620	470	380	290	220	160	110	75	165
10MHz	25%	280	220	170	130	110	79	55	37	90

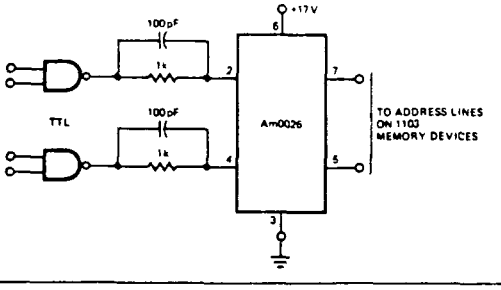
*Note: Values in pF and assume both sides in use as non-overlapping 2 phase driver; each side operating at same frequency and duty cycle with $(V^+ - V^-) = 17V$.

TYPICAL APPLICATIONS

AC Coupled MOS Clock Driver



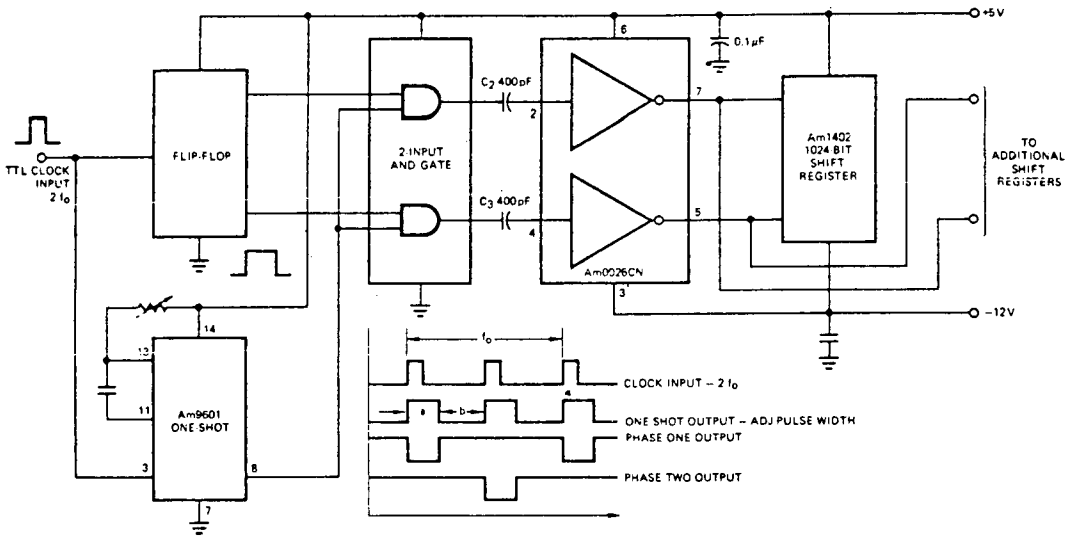
DC Coupled RAM Memory Address or Precharge Driver (Positive Supply Only)



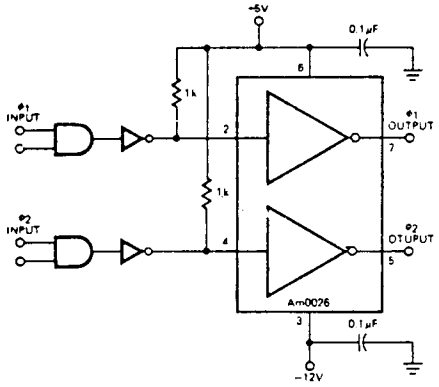
4-5

TYPICAL APPLICATIONS (Cont.)

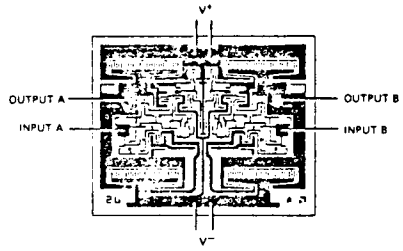
Logically Controlled AC Coupled Clock Driver



DC Coupled MOS Clock Driver



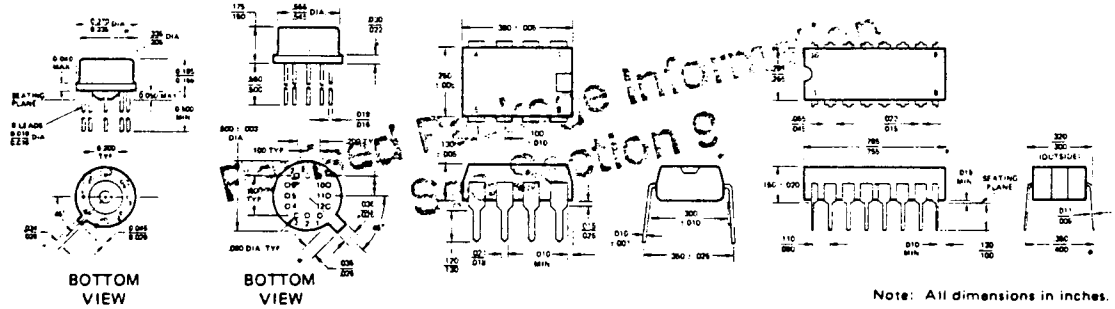
Metallization and Pad Layout



DIE SIZE 0.063" X 0.078"

PHYSICAL DIMENSIONS

8-Lead Metal Can (H) | 12-Lead Metal Can (G) | 8-Pin Molded Mini-Dual-In-Line (N) | 14-Pin Ceramic Dual-In-Line (L)



BOTTOM VIEW | BOTTOM VIEW

Note: All dimensions in inches.

Am1402A/1403A/1404A
Am2802/2803/2804
1024-Bit Dynamic Shift Registers

Distinctive Characteristics

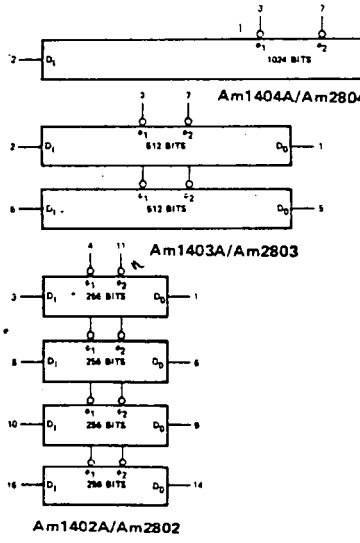
- Quad 256-bit, dual 512-bit, single 1024-bit
- 10 MHz frequency operation guaranteed for Am2802, Am2803 and Am2804.
- Low power dissipation of 0.1 mW/bit at 1 MHz
- DTL and TTL compatible
- Both military and commercial grade devices available
- 100% reliability assurance testing in compliance with MIL-STD-883.
- Electrically tested and optically inspected die for the assemblers of hybrid products

FUNCTIONAL DESCRIPTION

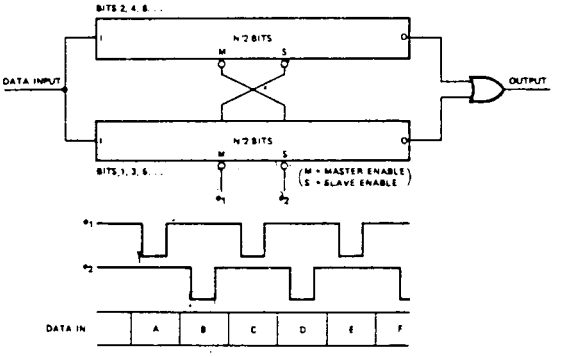
The Am1402A, 3A, and 4A are 1024-bit silicon gate dynamic shift registers. The low threshold characteristics of this technology allow high-speed operation and DTL and TTL compatibility. The Am1402A is a quad 256-bit device; the Am1403A is a dual 512-bit register; and the Am1404A is a single 1024-bit register. All three devices require two-phase non-overlapping clocks, and provide a one-bit shift on each clock pulse. The Am2802, 3, and 4 registers are functionally identical to the Am1402A, 3A, and 4A, but are guaranteed to operate over frequencies from 400 Hz to 10 MHz.

BLOCK DIAGRAMS

Am1402A/1403A/1404A Shift Registers



Functional Equivalent of Each Register



Since the two registers shift on opposite clock pulses, a new data bit is entered on both ϕ_1 and ϕ_2. Data entering the register on ϕ_1 will appear at the output on ϕ_1 (from the negative edge of ϕ_1 to the negative edge of ϕ_2).

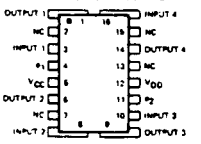
ORDERING INFORMATION

Part Number	Package Type	Temperature Range	Standard Speed Range Order Number	Extended Speed Range Order Number
Am1402A/ 2802	Hermetic DIP	0°C to +70°C	AM1402A	AM2802DC
	Hermetic DIP	−55°C to +125°C	AM1402ADM	AM2802DM
	Molded DIP	0°C to +70°C	AM1402APC	AM2802PC
Am1403A/ 2802	TO-99	0°C to +70°C	AM1403A	AM2803HC
	TO-99	−55°C to +125°C	AM1403AHM	AM2803HM
	Molded DIP	0°C to +70°C	AM1403APC	AM2803PC
AM1404A/ 2804	TO-99	0°C to +70°C	AM1404A	AM2804HC
	TO-99	−55°C to +125°C	AM1404AHM	AM2804HM
	Molded DIP	0°C to +70°C	AM1404APC	AM2804PC

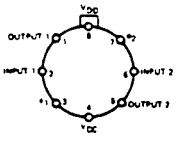
CONNECTION DIAGRAMS

Top View

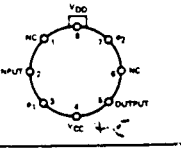
Am1402A/Am2802



Am1403A/Am2803



Am1404A/Am2804



MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +160°C
Temperature Under Bias	−55°C to +125°C
Power Dissipation (Note 1)	600 mW
Data and Clock Input Voltages with respect to most Positive Supply Voltage, V_{CC}	0.3 V to −20 V
Power Supply Voltage, V_{DD} with respect to V_{CC}	0.3 V to −20 V

OPERATING RANGE

Part Number	V_{CC}	V_{DD}	Temperature Range
Am1402A, Am1403A, Am1404A	5V ±5%	−4.75V to −9.45V	0°C to +70°C
Am1402ADM, Am1403AHM, Am1404AHM	5V ±5%	−4.75V to −9.45V	−55°C to +125°C
Am2802DC, Am2803HC, Am2804HC	5V ±5%	−5V ±5%	0°C to +70°C
Am2802DM, Am2803HM, Am2804HM	5V ±5%	−5V ±5%	−55°C to +125°C

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

Parameters	Description	Test Conditions		Am1402A, 3A, 4A Min.	Typ.	Max.	Am2802, 3, 4 Min.	Typ.	Max.	Units
V_{IH}	Input HIGH Voltage			V_{CC}−2.0			V_{CC}−2.0			V
V_{IL}	Input LOW Voltage			V_{CC}−10		V_{CC}−4.2	V_{CC}−10		V_{CC}−4.2	V
I_I	Input Current	T_A = 25°C			<10	500		<10	500	nA
I_O	Output Leakage Current	T_A = 25°C, V_{OUT} = 0V			<10	1000		<10	1000	nA
$I_{\phi L}$	Clock Leakage Current	T_A = 25°C, V_ϕ = −12V			10	1000		10	1000	nA
V_{OH}	Output HIGH Voltage Driving TTL	R_L = 3k to V_{DD}, V_{DD} = −5V ±5%		2.4	3.5		V_{CC}−1.9	V_{CC}−1		V
	Output HIGH Voltage Driving MOS	R_L = 4.7k to V_{DD}, V_{DD} = −5V ±5%		V_{CC}−1.9	V_{CC}−1		V_{CC}−1.9 (Note 2)	V_{CC}−1 (Note 2)		V
	Output HIGH Voltage Driving TTL	R_L = 4.7k to V_{DD}, V_{DD} = −9V ±5%		2.4	3.5					
	Output HIGH Voltage Driving MOS	R_L = 6.2k to V_{DD}, 3.9k to V_{CC} V_{DD} = −9V ±5%		V_{CC}−1.9	V_{CC}−1					
V_{OL}	Output LOW Voltage	V_{DD} = −5V ±5%, R_L = 3k to V_{DD}, I_{OL} = −1.6mA			−0.3	0.5		−0.3	0.5	V
		R_L = 4.7k to V_{DD} V_{DD} = −9V ±5%, I_{OL} = −1.6mA			−0.3	0.5				
$V_{\phi H}$	Clock Input HIGH Level			V_{CC}−1		V_{CC}+0.3	V_{CC}−1		V_{CC}+0.3	V
$V_{\phi L}$	Clock Input LOW Level	V_{DD} = −5V ±5%		V_{CC}−15		V_{CC}−17	V_{CC}−15		V_{CC}−17	V
		V_{DD} = −9V ±5%		V_{CC}−12.6		V_{CC}−14.7				
I_{DD}(−5) (Note 1)	V_{DD} Current, V_{DD} = −5V ±5%	5MHz Data Rate, 33% Duty Cycle, $V_{\phi L}$ = V_{CC}−17V	T_A = 25°C		40	50		40	50	mA
			T_A = 0°C			56			56	
	V_{DD} Current, V_{DD} = −5V ±5%		T_A = −55°C						70	
		10MHz Data Rate, 40% Duty Cycle, $V_{\phi L}$ = V_{CC}−17	T_A = 25°C					50	60	mA
			T_A = 0°C						68	
			T_A = −55°C						80	
I_{DD}(−9) (Note 1)	V_{DD} Current, V_{DD} = −9V ±5%	3MHz Data Rate, 26% Duty Cycle, $V_{\phi L}$ = V_{CC}−14.7V	T_A = 25°C		30	40		30	40	mA
			T_A = 0°C			45			45	
			T_A = −55°C						60	

SWITCHING CHARACTERISTICS AND OPERATING CONDITIONS (Over Operating Range)

Am1402A/Am1403A/Am1404A

Parameter	Description	Test Conditions	$V_{DD} = -5\ V \pm 5\%$ (Test Load 1) Min.	Typ.	Max.	$V_{DD} = -9\ V \pm 5\%$ (Test Load 2) Min.	Typ.	Max.	Units
f_c	Clock Frequency Range		(Note 1)		2.5	(Note 1)		1.5	MHz
f_d	Data Repetition Rate		(Note 1)		5.0	(Note 1)		3.0	MHz
$t_{\phi PW}$	Clock Pulse Width		0.13	1.0		0.17		10	μs
$t_{\phi d}$	Clock Pulse Delay (Note 2)	$t_{\phi PW}$ = 130 ns	10		(Note 2)	10		(Note 2)	ns
t_f, t_r	Clock Pulse Rise/Fall Time				1000			1000	ns
t_s	Data Set Up Time	$t_r = t_f \leq 50$ ns	30		30	60		60	ns
t_h	Data Hold Time	$t_r = t_f \leq 50$ ns	20		20	20		20	ns
t_{pd+}, t_{pd-}	Clock to Data Out Delay				90			110	ns
C_{IN}*	Input Capacitance	@ 1 MHz, 250 mVPP		5	10		5	10	pF
C_{OUT}*	Output Capacitance	@ 1 MHz, 250 mVPP		5	10		5	10	pF
C_ϕ*	Clock Capacitance	@ 1 MHz, 250 mVPP		110	140		110	140	pF

SWITCHING CHARACTERISTICS AND OPERATING CONDITIONS (Over Operating Range)

Am2802/Am2803/Am2804 Clock Pulse Width = 70nsec; Clock LOW Level = (V_{CC}-15); $V_{DD} = -5\ V \pm 5\%$ (Test Load 1)

Parameter	Description	Test Conditions	Min.	Typ.	Max.	
f_c	Clock Frequency Range	$t_r = t_f = 10$ ns	(Note 1)		5.0 (Note 4)	MHz
f_d	Data Repetition Rate (Note 1)		(Note 3)		10.0 (Note 4)	MHz
$t_{\phi PW}$	Clock Pulse Width		0.07		10	μs
$t_{\phi d}$	Clock Pulse Delay	$t_{\phi PW}$ = 70 ns	10		(Note 2)	ns
t_f, t_r	Clock Pulse Rise/Fall Time				1000	ns
t_s	Data Set Up Time		30			ns
t_h	Data Hold Time		20			ns
t_{pd+}, t_{pd-}	Clock to Data Out Delay				90	ns

Notes:
1. See minimum operating frequency graph for low limits on data rep. rate.
2. Upper limit on $t_{\phi d}$ is determined by minimum frequency.
3. See max clock pulse delay graph for guarantee.
4. For additional information on 10MHz operation (5MHz clock rate) see AMD application note dated July 1973 on "Applications of Dynamic Shift Registers."

DESCRIPTION OF TERMS

OPERATIONAL TERMS

V_{OH} Minimum logic HIGH output voltage with output HIGH current I_{OH} flowing out of output.

V_{OL} Maximum logic LOW output voltage with output LOW current I_{OL} into junction of output and load resistor.

V_{IH} Logic HIGH input voltage.

V_{IL} Logic LOW input voltage.

V_{OL} Clock LOW input voltage.

V_{OH} Clock HIGH input voltage.

I_I Input leakage current.

I_O Output leakage current.

I_{DD} Power supply current.

C_{IN} Input capacitance.

C_ϕ Input clock capacitance.

C_{OUT} Output capacitance.

FUNCTIONAL TERMS

ϕ_1, ϕ_2 The two clock phases required by the dynamic shift register.

f_c The clock frequency of the shift register.

f_d The input data repetition rate.

SWITCHING TERMS

$t_{\phi d}$ The delay between the LOW to HIGH transition of a clock phase to the HIGH to LOW transition of the other clock phase.

$t_{\phi PW}$ The clock pulse widths necessary for correct operation.

t_f, t_r The clock pulse rise and fall times necessary for correct operation.

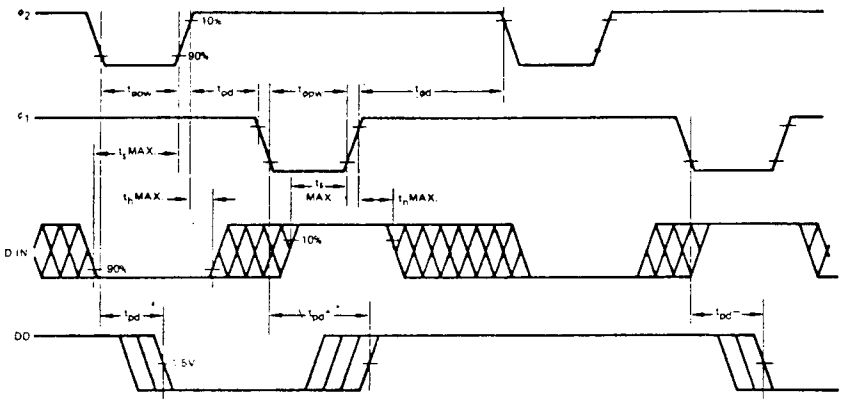
t_s The time required for the input data to be present prior to the LOW to HIGH transition of the clock phase to ensure correct operation.

t_h The time required for the input data to remain present after the LOW to HIGH transition of the clock phase to ensure correct operation.

t_{pd+} The propagation delay from the HIGH to LOW clock phase ϕ_1 transition to the output LOW to HIGH transition.

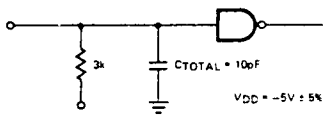
t_{pd-} The propagation delay from the HIGH to LOW clock phase ϕ_2 transition to the output HIGH to LOW transition.

SWITCHING WAVEFORMS

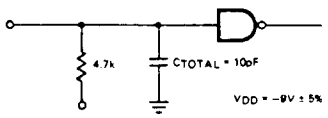


Clock Rise Time 10 ns
Clock Fall Time 10 ns
Output Load 1 TTL Load

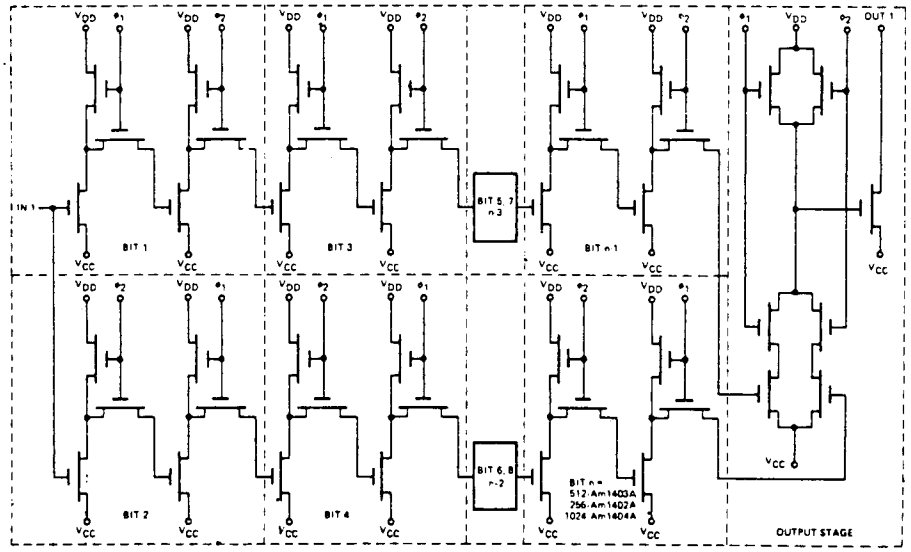
Test Load 1



Test Load 2

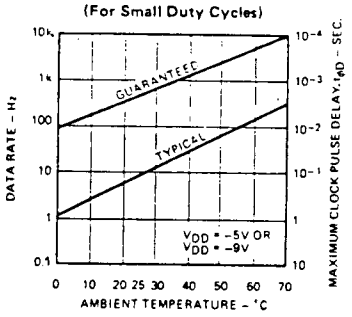


CIRCUIT DIAGRAM

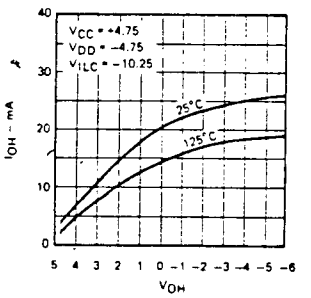


POWER CHARACTERISTICS

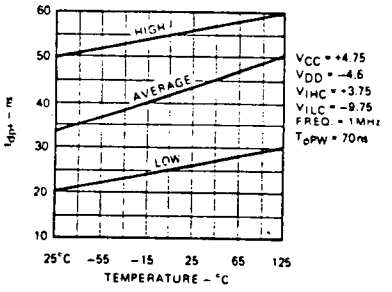
Minimum Operating Data Rate or Maximum Clock Pulse Delay Versus Temperature
(For Small Duty Cycles)



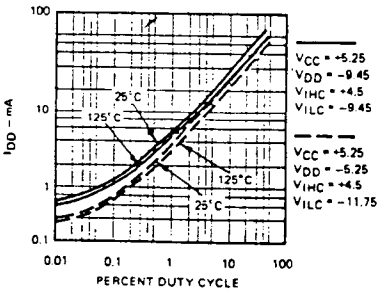
I_{OH} Versus V_{OH}



Typical Range of t_{pd+} Versus Temperature



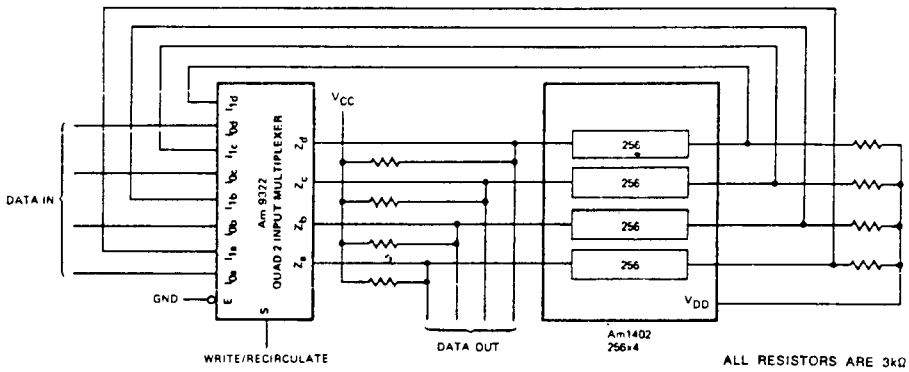
I_{DD} Versus Clock Duty Cycle



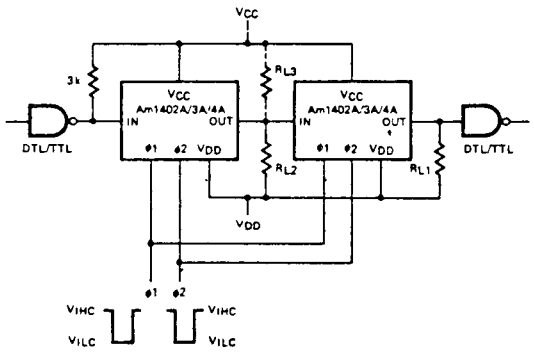
APPLICATIONS

256-Bit Delay

Write Recirculate Logic



DTL/TTL To MOS To DTL/TTL Interface

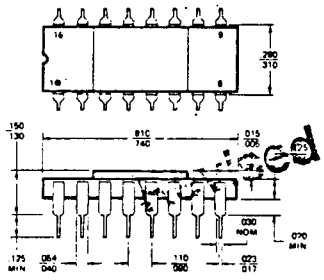


R_L Load Resistor Values for Different V_{DD} Supplies

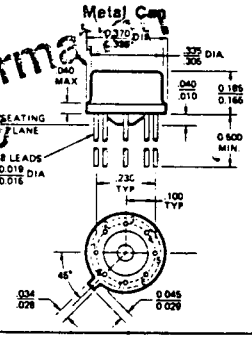
	$V_{CC} = 5$ V $V_{DD} = -5$ V	$V_{CC} = 5$ V $V_{DD} = -9$ V
R_{L1}	3.0 k	4.7 k
R_{L2}	4.7 k	6.2 k
R_{L3}	Not required	3.9 k

PHYSICAL DIMENSIONS

Dual-In-Line

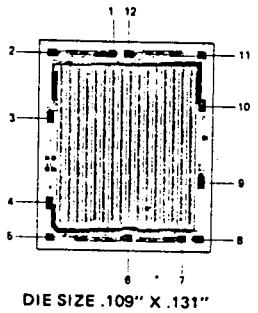


Metal Can



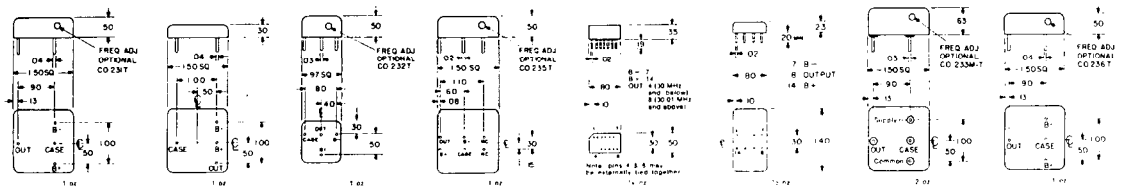
PAD	1402A/2802 PIN	1402A/2802 SIGNAL	1403A/2803 PIN	1403A/2803 SIGNAL	1404A/2804 PIN	1404A/2804 SIGNAL
1	1	OUT 1				
2	3	IN 1	2	IN 1	2	IN
3	4	ϕ 1	3	ϕ 1	3	ϕ 1
4	5	V_{CC}	4	V_{CC}	4	V_{CC}
5	6	OUT 2	5	OUT 2	5	OUT
6	8	IN 2				
7	9	OUT 3				
8	10	IN 3	6	IN 2	7	ϕ 2
9	11	ϕ 2	7	ϕ 2		
10	12	V_{DD}	8	V_{DD}		
11	14	OUT 4	1	OUT 1	8	V_{DD}
12	16	IN 4				

Metallization and Pad Layout



DIE SIZE .109" X .131"

ADVANCED MICRO DEVICES INC.
901 Thompson Place
Sunnyvale
California 94086
(408) 732-2400
TWX: 910-339-9280
TELEX: 34-6306

	VERSATILE (Broad range of frequencies and options)	LOW PROFILE (only 0.3" high with frequencies as low as 200 KHz)	SMALL (only ½ cu. in.)	DIP COMPATIBLE (Plugs into 14 pin DIP with frequency as low as 20 KHz)	MINIATURE DIP COMPATIBLE (Only .35" high and consumes space of single 14 pin DIP)	LOW PROFILE DIP COMPATIBLE (only .225" high)	DRIVES ECL (Up to 200 MHz)	DRIVES CMOS (With 1-2 ma typical current drain)
MODEL	CO-231	CO-231L	CO-232	CO-235	CO-238	CO-239	CO-233M	CO-236
OUTPUT	TTL/DTL COMPATIBLE Fan Out: 10 TTL loads Logic 0: 0.4V max, sink 16 ma Logic 1: 2.4V min, source 2 ma Symmetry: 50/50 ± 15% (improved symmetry optional) (Above 50 MHz, drive capability of CO-231 decreases; at 100 MHz it drives 2 Schottky TTL loads)						ECL COMPATIBLE	CMOS COMPATIBLE
FREQUENCY	1 Hz thru 100 MHz	200 KHz thru 30 MHz	3 MHz thru 30 MHz	20 KHz thru 30 MHz	3 MHz thru 100 MHz	4 MHz thru 100 MHz	1 MHz thru 200 MHz	01 Hz thru 10 MHz
INPUT	5 VDC ±5%	5 VDC ±5%	5 VDC ±5%	5 VDC ± 5%	5 VDC ±5%	5 VDC ±5%	CO-233M: −15 VDC ±10% CO-233ME: −5.2 VDC ±5% (to −30 VDC optional)	5-15 VDC to 6 MHz (5-15 VDC for refined stability types below 500 KHz)
SIZE	1½" x 1½" x ½"	1½" x 1½" x 0.3"	1" x 1" x ½"	1½" x 1½" x ½"	0.5" x 0.8" x 0.35"	1.4" x 8" x .225"	1½" x 1½" x ⅝"	1½" x 1½" x ½"
ACCURACY (Maximum error at 25°C)	CO-231: ±.001% *CO-231T: ±.0001%	CO-231LA: ±.005% CO-231LB: ±.001%	CO-232: ±.001% *CO-232T: ±.0001%	CO-235: ±.001% *CO-235T: ±.0001%	CO-238A: ±.005% CO-238B: ±.001%	CO-239A: ±.005% CO-239B: ±.001%	CO-233M: ±.001% *CO-233MT: ±.0001%	CO-236: ±.001% *CO-236T: ±.0001%
TUNING OPTION*	YES*	NO	YES*	YES*	NO	NO	YES*	YES*
	*Models with "T" suffix include tuning adjustment with nominal range of ±50 ppm below 25 MHz and ±15 ppm above 25 MHz — setability is ≤±.0001%							
TEMPERATURE STABILITY	Standard: +20°C to +30°C: ±.0005% and 0°C to +70°C: ±.0025% −1 Option: −55°C to +85°C: ±.005% (−40°C to +85°C for CO-236-1, and for CO-231-1 below 8 KHz) −2 Option: −55°C to +125°C: ±.005% −3 Option: 0°C to +50°C: ±.0003% (not available for CO-231 below 8 KHz, CO-238 below 4 MHz or CO-236 below 2 MHz) −4 Option: 0°C to +50°C: ±.0001% (only for CO-231 in 3-20 MHz range) −6 Option: 0°C to +50°C: ±.001% −8 Option: 0°C to +70°C: ±.01% (includes initial accuracy)							
OPTIONS	Other stability specifications Other mechanical configurations and alternative pin patterns Fully solder sealed units Ruggedized types for high shock and vibration Multiple output units Voltage frequency control (VCXO) in CO-231 Type							
MOUNTING								

(Markings do not appear on units - for reference only)

VECTRON Clock Oscillators

NATIONAL

DS8973, DS8974, DS8976 LED 9-digit drivers

general description

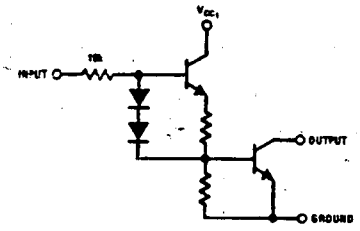
The DS8973, DS8974, and DS8976 are 9-digit drivers designed to operate from 4 cell (DS8973) or 3 cell (DS8974) or 6 cell (DS8976) battery supplies. Each driver will sink 100 mA to less than 0.5V when driven by only 0.1 mA. Each input is blocked by diodes so that the input can be driven below ground with virtually no current drain. This is especially important in calculator systems employing a dc-to-dc converter on the negative side of the battery. If the converter were on the positive side of the battery, the converter would have to handle all of the display current, as well as the MOS calculator chip current. But if it is on the negative side, it only has to handle the MOS current. The DS8973 and DS8974 are designed for the more efficient operating mode.

features

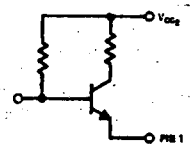
- Nine complete digit drivers
- Built-in low battery indicator
- High current outputs—100 mA
- Choice of 3 or 4-cell operation
- Straight through pin out for easy board layout

equivalent circuit and connection diagrams

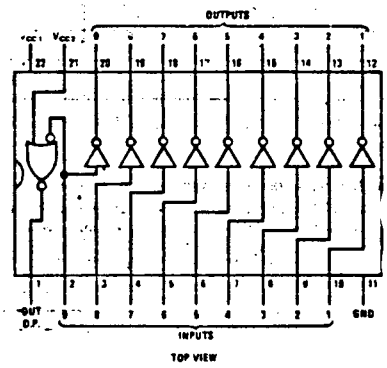
Typical Driver Circuit



Typical D.P. Out Circuit



Dual-In-Line Package



Order Number DS8973N, DS8974N or DS8976N

typical applications

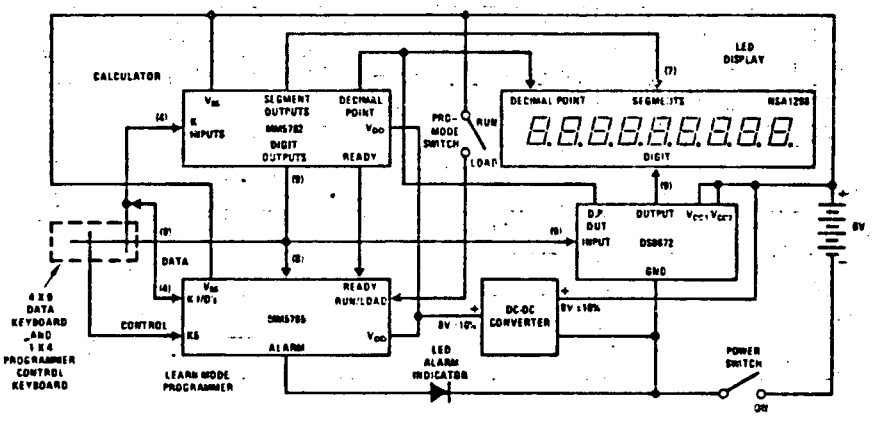


FIGURE 1. 6V Programmable Statistical Calculator

absolute maximum ratings (Note 1)

Supply Voltage	10V
Input Voltage	10V
Output Voltage	10V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DS8973	4.4	10.0	V
DS8974, DS8976	3.3	4.5	V
Temperature (T_A)	0	70	°C

electrical characteristics

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	Logical "1" Input Voltage	V_{CC} = Max		3.9			V
I_{IH}	Logical "1" Input Current	V_{CC} = Max, V_{IH} = 3.9V		0.1		0.3	mA
V_{IL}	Logical "0" Input Voltage	V_{CC} = Max				0.5	V
I_{IL}	Logical "0" Input Current	V_{CC} = Max, V_{IL} = 0.5V				40	μA
V_{TH}	High Low Battery Threshold	V_{OT} (Pin 1) = 1V, $I_{OT} \leq -50\mu A$, $T_A = 25°C$	DS8973	3.5			V
		V_{IH} (Pin 2) = 3.9V	DS8974	4.6			V
			DS8976	7.0			V
V_{TL}	Low Low Battery Threshold	V_{OT} (Pin 1) = 2.3V, $I_{OT} \geq -6$ mA, $T_A = 25°C$	DS8973			3.1	V
		V_{IH} (Pin 2) = 3.9V	DS8974			4.2	V
			DS8976			6.2	V
I_{CEX}	Logical "1" Output Current	V_{CC} = Min, V_{OH} = 9.5V, V_{IL} = 0.5V				50	μA
V_{OL}	Logical "0" Output Voltage	V_{CC} = Min, I_{OL} = 100 mA, V_{IH} = 3.9V				0.5	V
I_{OL}	Logical "0" Output Current	V_{CC} = Min, V_{OL} = 0.5V, V_{IH} = 3.9V		100			mA
I_{CC_1}	Supply Current	V_{CC} = Max, One Input "ON"				6	mA
I_{CC_2}	Pin 21 (Low Battery Supply)	V_{CC} = Max, $V_{CC_2} = V_{CCMAX}$				1.2	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operations.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range. All typicals are given for $T_A = 25°C$.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

typical applications (con't)

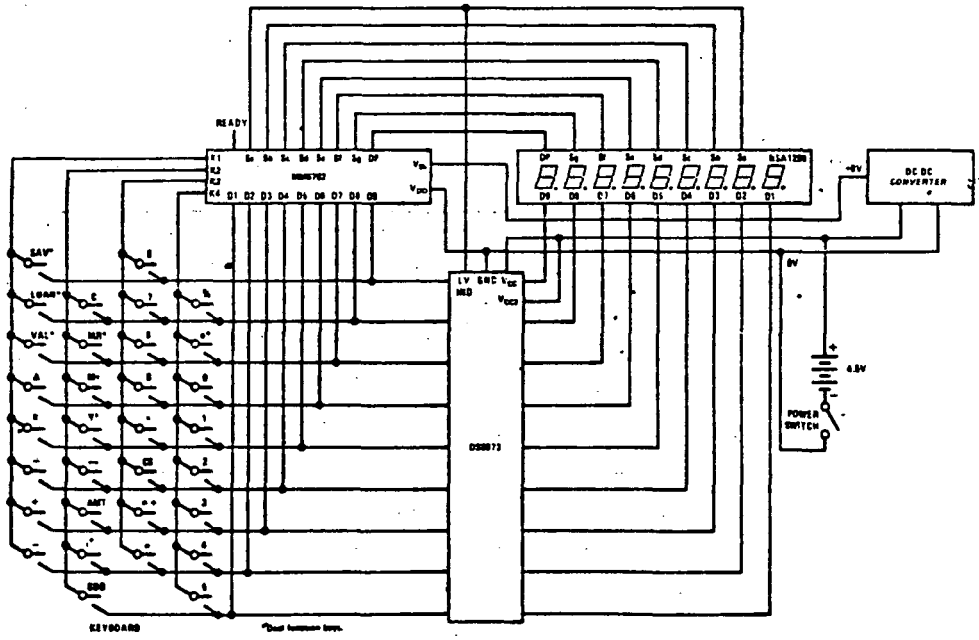


FIGURE 2. Complete Calculator Schematic For 3-Cell System

DESCRIPTION

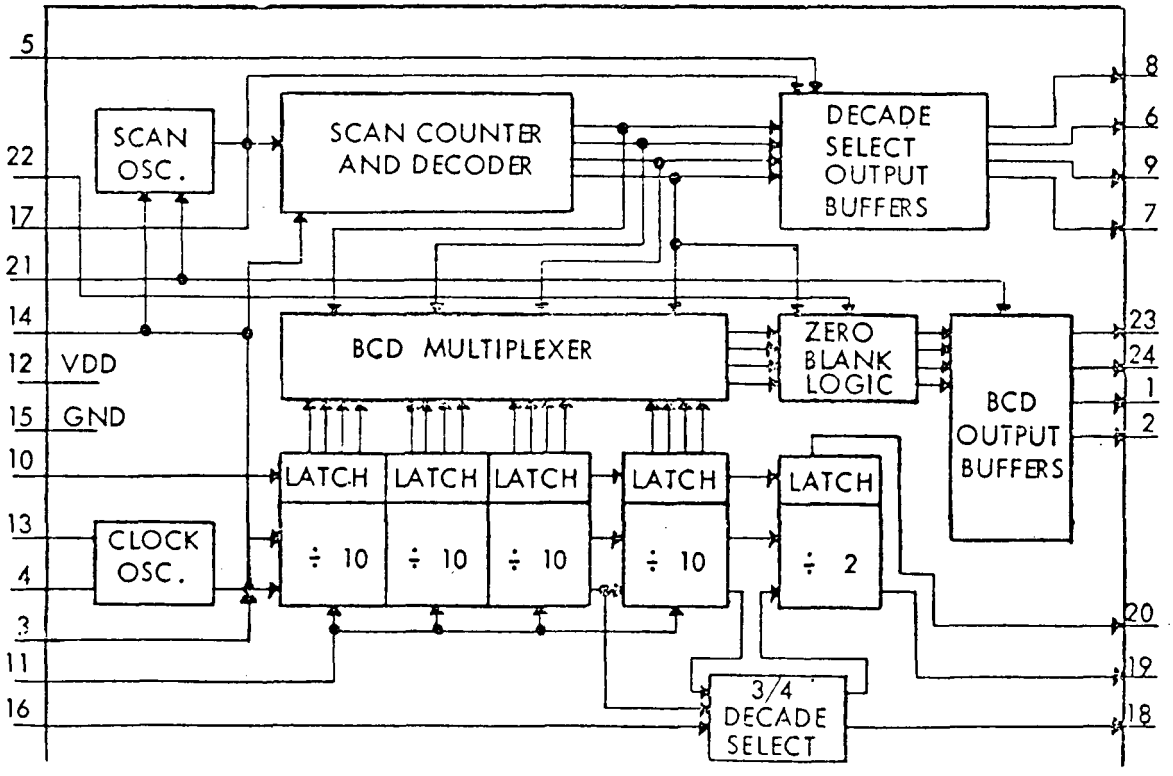
The Hughes HCTR4010 is a TTL compatible CMOS LSI circuit containing four sychronous decade up/down counters and their associated storage latches. Information from the latches is multiplexed to the BCD outputs, to drive readily available TTL display decoder-drivers.

FEATURES

CMOS technology for low power
Up/down-counting capability
Internal scan and clock oscillators
All inputs and outputs
TTL compatible (V_{DD} = 4.5 to 5.5 volts)
Optional 3 or 4 Decade Operation
Independent latches on each decade & overflow
> 1 MHz operation @ VDD > 4.5 volts
Multiplexed BCD outputs with automatic or manual leading zero unblanking
Capability of floating BCD outputs
3 to 10 volts operation

PINS

1. BCD 4 Out
2. BCD 8 Out
3. Int. Clock enable or external clock in
4. Int. Clock frequency control or external clock disable
5. Decade Strobe True/Comp
6. Decade 2 Strobe
7. Decade 4 Strobe
8. Decade 1 Strobe
9. Decade 3 Strobe
10. Hold/Load Latches
11. Up/Down Control
12. + VDD
13. Osc. Disable
14. Master Reset
15. Ground (-V)
16. 3/4 Decade Select
17. Scan Frequency Control
18. Clock Out
19. Overflow
20. Stored Overflow
21. Chip Enable
22. Unblank
23. BCD 1 Out
24. BCD 2 Out



QUAD DECADE CLOCK CONTROL

External Clock Mode ("1" on Oscillator Disable Input):

Frequency Control/ External Clock Disable	1	Disables External Clock (Internal Clock Enable/External Clock In must be "0" when disable is energized).
	0	Enables External Clock.
Internal Clock Enable/ External Clock In	1→0	Advances counter to next state on "1" to "0" transition of External Clock applied at this input.

Internal Clock Mode ("0" on Oscillator Disable Input):

Frequency Control/ External Clock Disable	-	Capacitor connected from this input to V_{DD} or GROUND controls Internal Clock Frequency. If no capacitor is connected, the oscillator will have a free-running frequency of typically 300 KHz.
Internal Clock Enable/ External Clock In	1	Enables internal oscillator to counter.
	0	Disables internal oscillator to counter.

QUAD DECADE INPUTS

Strobe True/Complement	1	Positive true.
	0	Negative true.
Chip Enable	1	Enables BCD information to BCD lines.
	0	Floats BCD lines and turns off scan oscillator and turns off all strobe outs. Rest of counter still works.
Unblank	1	Displays all decades.
	Strobe 1	Displays from first non-zero decade or just decade 1.
	Strobe 2	Displays from first non-zero decade or just decades 1 & 2.
	Strobe 3	Displays from first non-zero decade or just decades 1 & 2 & 3.
	0	Displays from first non-zero decade.
Hold/Load Latches	1	Stores data in counters (data at 0→1 transition is stored).
	0	Accepts data from counters.
Up/Down	1	Counter counts up.
	0	Counter counts down.
	NOTE:	Up/Down Input should only be changed with External Clock = 0 or with External Clock Disable = 1, otherwise can get false count.
3/4 Decade Select	1	Clock Out and overflow driven by output of decade 3.
	0	Clock Out and overflow driven by output of decade 4.

QUAD DECADE INPUTS (continued..)

Master Reset	1	Resets counter and overflow to zero (latches also reset if HOLD/LOAD = 0). Drives BCD to 1111, drives strobes off, and resets strobe counter to decade 4.
	0	Allows counter to operate.

QUAD DECADE OUTPUTS

BCD 1, 2, 4 and 8	BCD information from decade selected by strobe outputs. Blanked information represented by state 1111. Open state is high impedance to both +V and -V.
Overflow	Q from a divide by 2 stage driven by Clock Out.
Stored Overflow	Stored overflow information output (controlled by HOLD/LOAD input).
Clock Out	A positive pulse with leading edge coincident with first 0→1 transition of external (or internal) clock following count 999 or 9999. The trailing edge is coincident with the 1→0 transition of the external (or internal) clock which drives the counter into state 1000 or 10000 (determined by 3/4 Select input).
Decade (1, 2, 3, 4) Strobe	Tells which decade is being displayed on BCD lines Sequence is 4, 3, 2, 1 with Decade 4 as MSB and decade 1 as LSB. Can be either positive true or negative true depending on state of Strobe T/C input. Scan rate determined by scan frequency control input. When scan frequency control = 0 strobes are driven off, this characteristic can be used to control duty cycle of displays.

QUAD DECADE SCAN OSCILLATOR CONTROL

External Scan Oscillator Mode

Scan Frequency Control	1	Enables strobe out.
	1→0	Advances strobe counter.
	0	Disables strobe out and drives BCD out to 1111.

Internal Scan Oscillator Mode

Scan Frequency Control	Capacitor connected from this input to V_{DD} or GROUND controls Internal Scan Oscillator Frequency. If no capacitor is connected, the oscillator will have a free-running frequency of typically 300KHz

DESCRIPTION

The 6010 series of monolithic CMOS LSI four decade counters is designed for use in digital panel meters, digital voltmeters and other counting applications.

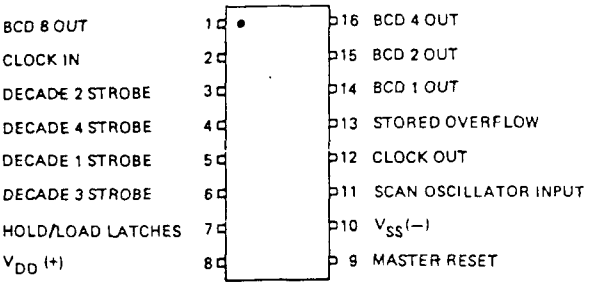
Four synchronous decade counters and a divide by two overflow stage are included in the 6010 devices to provide a counting range from 0 through 19999. The counting range can be further extended by cascading devices. Quad latches for each decade and a latch for overflow permit storage of any count in a BCD Format.

An "on chip" scan oscillator and scan counter/decoder generate the timing signals for time division multiplexing of the latched BCD count of each decade to the BCD outputs. The multiplex frequency is controlled by an external capacitor connected to the Scan Oscillator input. The decade strobe duty cycle of the HCTR6010A can be changed from the nominal 12 percent by connecting a resistor to the appropriate supply voltage.

The HCTR6010B is identical to the HCTR6010A except the scan oscillator has been designed for applications requiring a decade strobe duty cycle of nearly 25%.

In the HCTR6010, an internal delay circuit is placed in series with the Hold/Load Latches input. The delay is sufficiently long to ensure that a count "rippling" through the counter will be stabilized and correctly loaded into the latches even if Hold Latches and clock advance signals are applied simultaneously. This delay circuit is not included on the HCTR6010A and HCTR6010B devices. The HCTR6010 decade strobe duty cycle is similar to that of the HCTR6010B; however, a different range of capacitor values is used for control of the scan frequency.

16 PIN DIP
PIN CONNECTIONS
(TOP VIEW)



ORDERING INFORMATION:

USE D SUFFIX FOR CERAMIC PACKAGE:
HCTR6010D, HCTR6010AD, HCTR6010BD

USE P SUFFIX FOR PLASTIC PACKAGE:
HCTR6010P, HCTR6010AP, HCTR6010BP

- On Chip Scan Oscillator with adjustable duty cycle and frequency
- Cascadable
- Output latches for four decades plus overflow
- 1 MHZ operation at 5V (0 to 75°C)

ABSOLUTE MAXIMUM RATINGS

RATING	SYMBOL	VALUE	UNIT
DC Supply Voltage	V_{DD}	* +10.5 to-0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} + 0.5 to -0.5	Vdc
DC Current Drain Per Pin, All Inputs	I	10	mAdc
DC Current Drain Per Pin, All Outputs	I	20	mAdc
Operating Temperature Range	T_A	0 to 75	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Power Dissipation	PD	600 (plastic pkg) 700 (ceramic pkg)	mW

* CONSULT FACTORY FOR DEVICES WITH HIGHER V_{DD} RATINGS

GENERAL OPERATING NOTES

1. All high impedance inputs of this device have an input protection circuit to prevent damage due to high static voltage or electric fields. It is advisable, however, to use normal MOS handling precautions to prevent damage to the inputs resulting from application of voltages in excess of the maximum rated voltages for the device.
2. Erroneous operation may result if unused inputs are allowed to "float". All unused inputs should be terminated to a known logic level such as V_{DD} or V_{SS}.

TRUTH TABLE NO. 1

INPUTS			INTERNAL COUNTER RESPONSE	BCD & STORED OVERFLOW OUTPUT RESPONSE
MASTER RESET	CLOCK IN	HOLD/LOAD LATCHES		
0	↓	0	Advances 1 Count	Indicates New Count
0	↑	0	No Change	No Change
0	↓	1	Advances 1 Count	Retains Prior Count
1	X	0	Resets entire Counter (See note 1)	Outputs go to Zero
1	X	1	Resets entire Counter (See note 1)	Retains Prior Count

NOTE 1: A master reset has no effect on the scan counter.

TRUTH TABLE NO. 2

SCAN FREQUENCY CONTROL INPUT	INTERNAL SCAN COUNTER	DECADE STROBE OUTPUTS	BCD OUTPUTS
↓	Decrements one Count (see note 2)	All strobe outputs set to Zero	Output changes to data from next lower decade (see note 2)
0	No change	All strobe outputs at Zero	Output data from decade corresponding to Scan Counter Value
↑	No change	Reflects count of Internal Counter	No change
1	No change	Decade Strobe corresponding to Scan Counter Value will be "One" level	Output data from decade corresponding to Scan Counter Value

NOTE 2: Decade strobe scanning sequence is from the most significant decade to the least significant decade; i.e., 4-3-2-1, 4-3-2-1, etc.

DC CHARACTERISTICS Unless otherwise specified T_A = 0–75°C and V_{DD} Tolerance = ±5%

Characteristic	Symbol	V_{DD} (Vdc)	Value Min	Value Typ	Value Max	Unit
Output Voltage BCD, Decade Strobe, Clock Out and Stored Overflow Outputs						
"0" Level @ I_L = 1.6 mA (sink)	V_{OL}	5	...	0.16	0.4	Vdc
"1" Level @ I_L = 100 uA (source)	V_{OH}	5	V_{DD} - .5	4.8	...	
"0" Level @ I_L = 1.6 mA (sink)	V_{OL}	10	...	0.11	0.4	
"1" Level @ I_L = 100 uA (source)	V_{OH}	10	V_{DD} - .5	9.8	...	
Input Voltage (except Scan Oscillator Input)						
"0" Level	V_{IL}	5	0.0	1.5	0.8	Vdc
"1" Level	V_{IH}	5	V_{DD}-2.1	2.7	V_{DD}	
"0" Level	V_{IL}	10	0.0	2.0	0.5	
"1" Level	V_{IH}	10	V_{DD}-0.5	2.9	V_{DD}	
Scan Oscillator Input						
"0" Level	V_{IL}	5	0.0	2.0	0.5	Vdc
"1" Level	V_{IH}	5	V_{DD}-0.5	2.9	V_{DD}	
"0" Level	V_{IL}	10	0.0	4.0	1.0	
"1" Level	V_{IH}	10	V_{DD}-1.0	5.6	V_{DD}	
Input Current (Except Scan Oscillator Input)	I_{IN}	5/10	...	...	500	n Adc
Scan Oscillator Input Current †						
"0" Level Current (requires sinking by signal source)	I_{IL}	5	...	17.0* 350.0**	30.0* 560.0**	μA
		10	...	76.0* 1360.0**	160.0* 2700.0**	
"1" Level Current (requires sourcing by signal source)	I_{IH}	5	...	19.0	30.0	
		10	...	85.0	170.0	
("0" Level = V_{SS}, "1" Level = V_{DD})						
Quiescent Power Supply Current						
With Scan OSC Input = V_{SS}	I_Q	5	...	65.0* 400.0**	240.0* 825.0**	μA
		10	...	135.0* 1420.0**	500.0* 3100.0**	
With Scan OSC Input = V_{DD}		5	...	75.0	120.0	
		10	...	150.0	300.0	
Power Supply Current						
Clock Freq. = 1 MHz, Scan Freq. = 10 KHz (Scan Osc. Free Running)	I_D	5	...	.18* .20**	.42* .48**	m A
		10	...	.45* .47**	1.05* 1.10**	
Clock Freq. = 1 MHz, Scan Freq. = 10 KHz (Scan Osc. Driven) †		5	...	.18* .36**	.40* .75**	
		10	...	.43* 1.17**	1.00* 2.50**	
Clock Stopped, Scan Freq. = 10 KHz (Scan Osc. Free Running)		5	...	.059* .075**	.18* .20**	
		10	...	.134* .20**	.50* .75**	
Input Capacitance	C_{IN}		...	5.0		pF

*FOR HCTR6010.AND HCTR6010A **FOR HCTR6010B ONLY

† Due to low Scan Oscillator Input impedence, the HCTR 6010B is not recommended for driven Scan Oscillator applications.

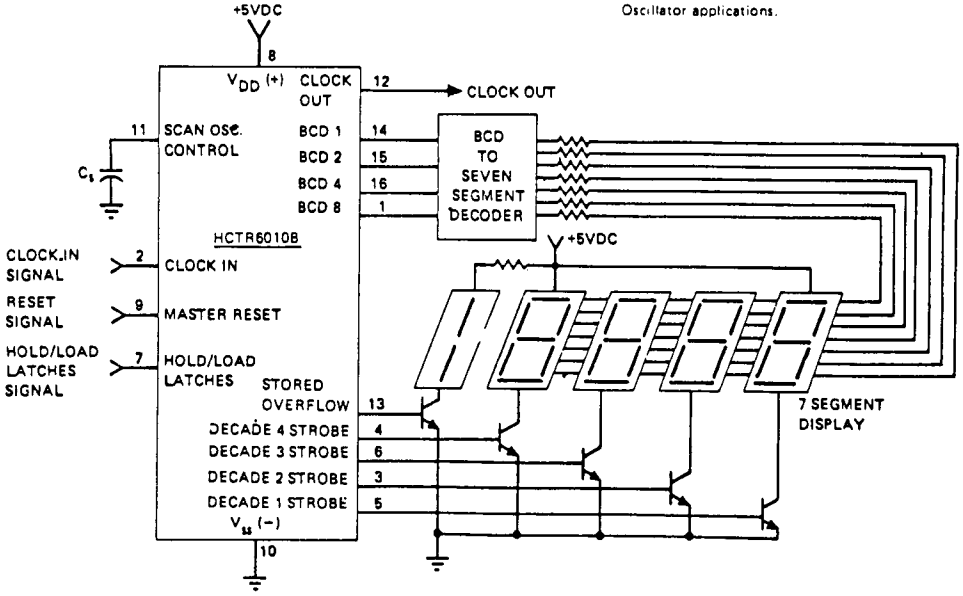


FIGURE 9 - TYPICAL APPLICATION OF THE HCTR6010B FOR A 4-1/2 DIGIT DISPLAY

AC CHARACTERISTICS Unless otherwise specified T_A = 0 - 75°C and V_{DD} Tolerance = ±5%

Characteristic	Figure	Symbol	V_{DD} . (Vdc)	Value			
				Min	Typ	Max	Unit
Output Rise Time (C_L = 15pF)							
BCD Outputs	5(b)	t_r	5	...	440	720	ns
Stored Overflow Output	5(d)		10	...	240	375	
Decade Strobe Output	2(b)						
Clock Out	5(c)		5	...	210	330	ns
			10	...	110	180	
Output Fall Time (C_L = 15pF)							
BCD Outputs	5(b)	t_f	5	...	100	160	ns
Stored Overflow Output	5(d)		10	...	55	110	
Decade Strobe Output	2(b)						
Clock Out	5(c)		5	...	50	85	ns
			10	...	35	60	
Propagation Delay Time, Clock In to BCD Output (C_L = 15pF)	5(a,b)	t_p	5	...	1500	2400	ns
			10	...	680	1070	
Propagation Delay Time, Clock In to Clock Out (C_L = 15pF)	5(a,c)	t_p	5	...	225	360	ns
			10	...	130	200	
Propagation Delay Time, Load Latches to BCD/Stored Overflow Outputs (C_L = 15pF)	4(b,c)	t_p	5	...	810	1470	ns
			10	...	385	685	
Propagation Delay Time Scan Oscillator Input to Decade Strobe Out							
Falling Edge to Falling Edge	2(a,b)	t_{p1}	5	...	560	900	ns
			10	...	240	405	
Rising Edge to Rising Edge		t_{p2}	5	...	540	865	
			10	...	270	430	
Propagation Delay Time, Master Reset to BCD & Stored Overflow Out (C_L = 15pF)	3(a,b)	t_p	5	...	1200	1950	ns
			10	...	520	810	
Master Reset Input Characteristics							
"1" Pulse Width	3(a)	PW_1	5	715	435	...	ns
			10	300	190	...	
Rise Time		t_r	5	...	...	NO LIMIT	
			10	...	...	NO LIMIT	
Fall Time		t_f	5	...	...	NO LIMIT	
			10	...	...	NO LIMIT	
Clock to Hold Latches Set-up Time (HCTR6010A, HCTR6010B only)	4(a,b)	$t_{set\text{-}up}$	5	1600	975	...	ns
			10	675	425	...	
Clock In Characteristics							
Pulse Repetition Rate		PRR	5		2.7	1.0	MHz
			10		6.2	2.0	
"0" Pulse Width	4(a)	PW_0	5	625	230	...	ns
			10	325	105	...	
"1" Pulse Width		PW_1	5	375	135	...	
			10	175	60	...	
Rise Time		t_r	5	...	...	1000	
			10	...	...	1000	
Fall Time		t_f	5	...	...	1000	
			10	...	...	1000	
Hold/Load Latches Input Characteristics							
"0" Pulse Width	4(b)	PW_0	5	360	165	...	ns
			10	125	75	...	
Rise Time		t_r	5	...	...	NO LIMIT	
			10	...	...	NO LIMIT	
Fall Time		t_f	5	...	...	NO LIMIT	
			10	...	...	NO LIMIT	
Scan Oscillator Input Characteristics (with External Source)							
"0" Pulse Width	2(a)	PW_0	5	585	305	...	ns
			10	225	130	...	
"1" Pulse Width		PW_1	5	265	155	...	
			10	110	65	...	
Rise Time		t_r	5	...	...	NO LIMIT	
			10	...	...	NO LIMIT	
Fall Time		t_f	5	...	...	NO LIMIT	
			10	...	...	NO LIMIT	

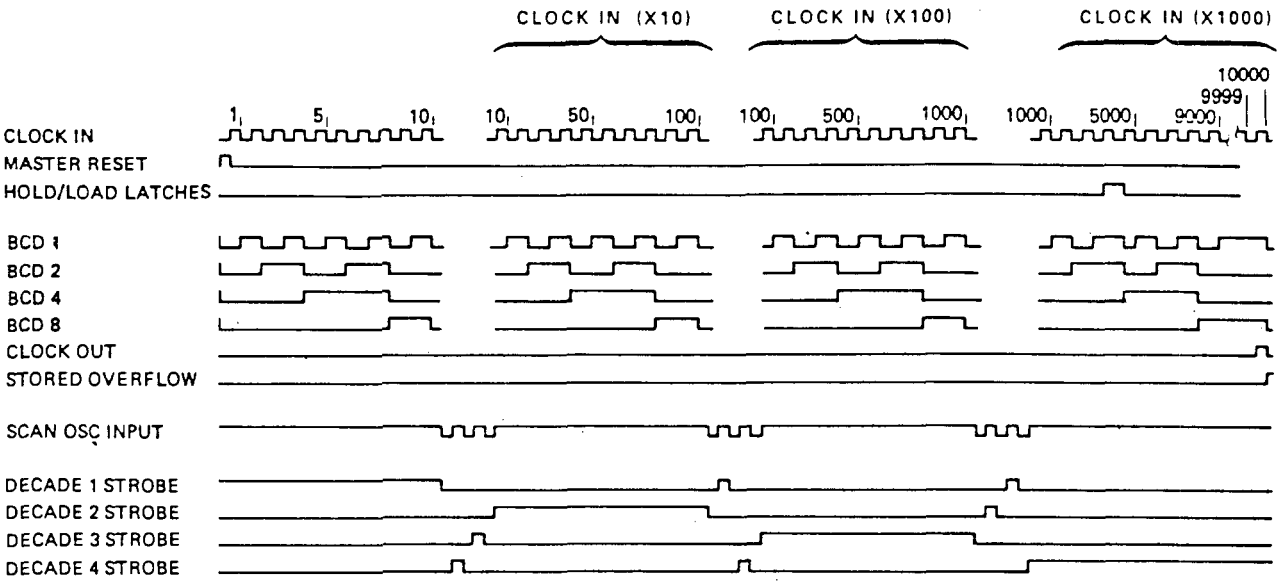
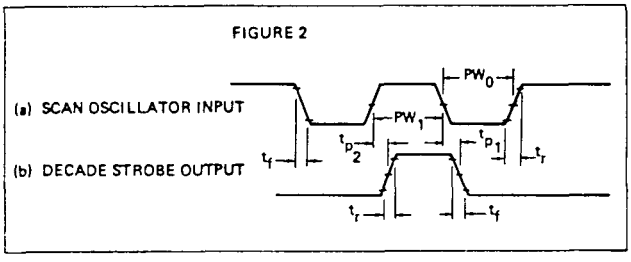
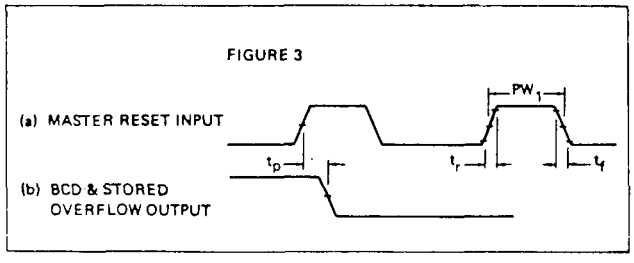
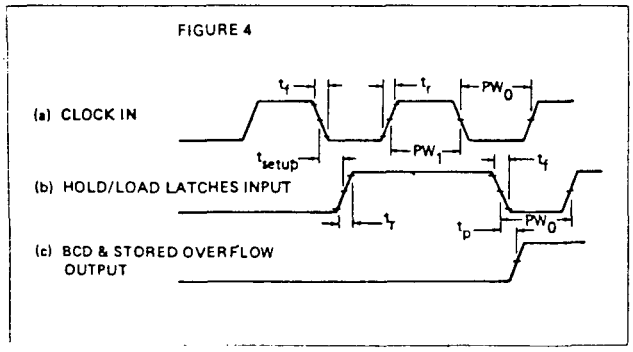
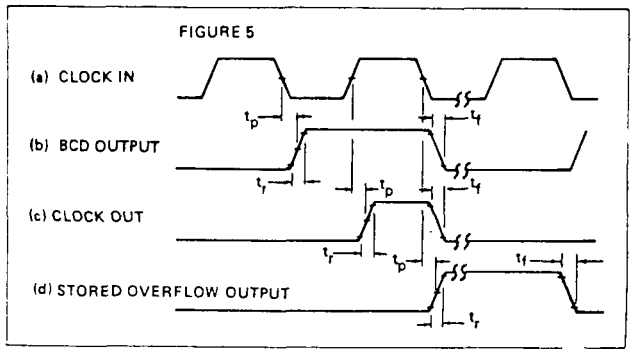


FIGURE 1 – 4½ DECADE COUNTER, TIMING DIAGRAM



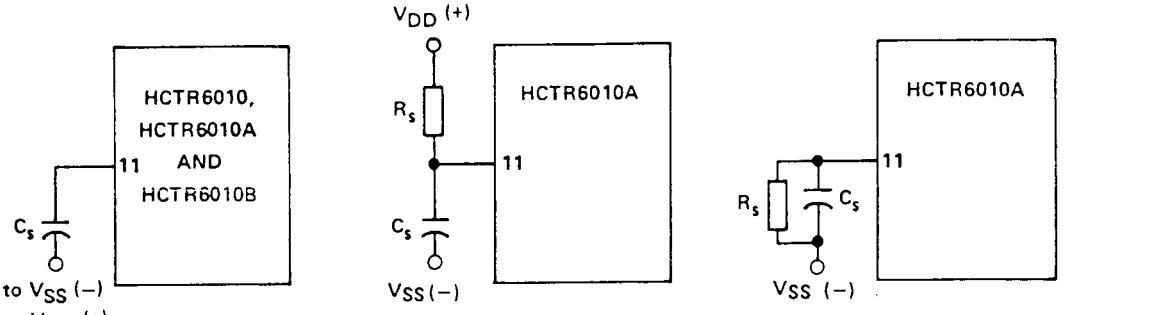






SCAN OSCILLATOR CHARACTERISTICS

All three devices in the 6010 series have on-chip scan oscillators; however, they are different in some characteristics. All devices are designed to permit adjustment of scan oscillator frequency by adjusting the value of a capacitor connected between the scan oscillator input and AC ground (V_{DD} or V_{SS}) as shown in figure 6(a). The nominal duty cycle of each decade strobe output for this configuration is approximately 23% for the HCTR6010 and HCTR6010B and approximately 12% for the HCTR6010A. Typical frequency versus capacitance characteristics are given in figures 7(b) and 7(c). The HCTR6010A is designed to permit adjustment of frequency and duty cycle using an external RC circuit connected to the scan oscillator input as shown in figures 6(b) and 6(c). If only the capacitor is connected the duty cycle is approximately 12%. The duty cycle can be increased or decreased by connecting a resistor to V_{DD} or V_{SS} respectively as shown in Figure 6(b) and 6(c). Typical scan oscillator operating characteristics and waveform definitions are given in Figures 7(a) - 7(d).



(a) SCAN OSCILLATOR FREQUENCY ADJUSTMENT CONFIGURATION

(b) INCREASED DUTY CYCLE CONFIGURATION

(c) DECREASED DUTY CYCLE CONFIGURATION

FIGURE 6

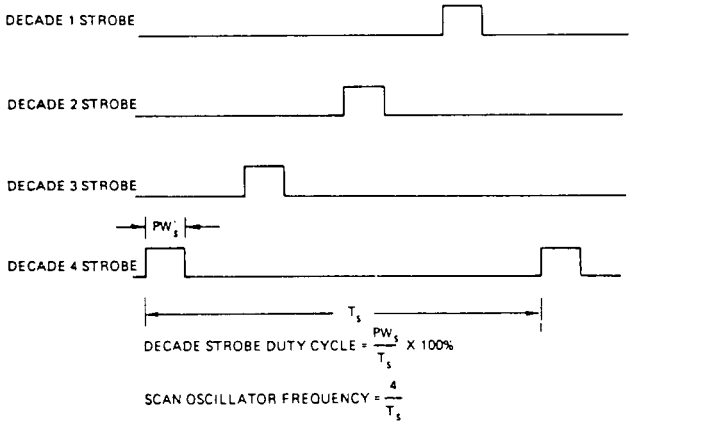
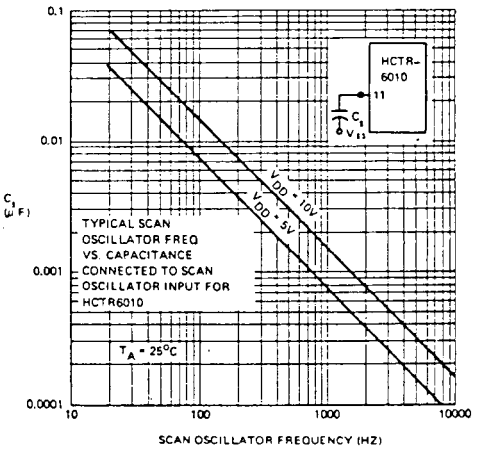
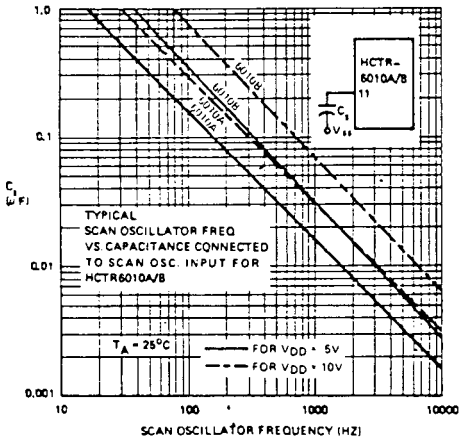


FIGURE 7(a) - DEFINITION OF SCAN OSCILLATOR FREQUENCY AND DECADE STROBE DUTY CYCLE



7(b) - TYPICAL HCTR6010 SCAN OSCILLATOR FREQUENCY CHARACTERISTICS



7(c) - TYPICAL HCTR6010A/B SCAN OSCILLATOR FREQUENCY CHARACTERISTICS

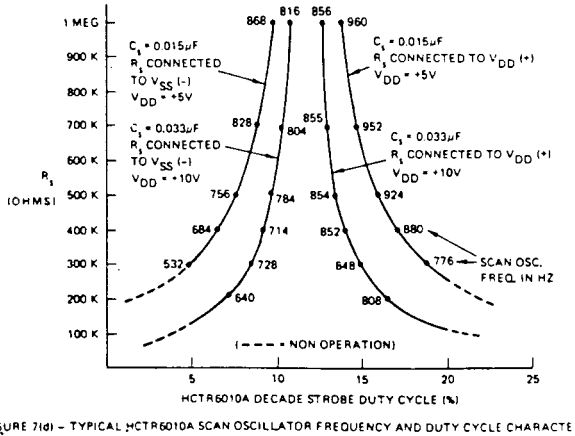


FIGURE 7(d) - TYPICAL HCTR6010A SCAN OSCILLATOR FREQUENCY AND DUTY CYCLE CHARACTERISTICS AT 25°C

GENERAL OPERATING CHARACTERISTICS

As shown in the expanded block diagram of Figure 8, the clock input frequency is counted by a series of four synchronous BCD counters and a divide by two stage. The counter is advanced by the negative going transition of the clock input signal.

The BCD counter data is stored by loading the data into the decade latches and the stored overflow latch. A zero level on the Hold/Load Latches input will transfer data from the counter to the latches. The count is held in the latches when the Hold/Load Latches input is in a high state.

The BCD data from the decade latches is presented sequentially at the BCD outputs by using time division multiplexing. The multiplex sequence is from the most significant decade to the least significant decade. A positive true output signal appears at each of the four Decade Strobe outputs to indicate which decade's BCD data is present at the BCD outputs. The latched overflow information is not multiplexed but connected to the Stored Overflow output through an output buffer stage.

Timing signals for the multiplexer and Decade Strobe signals are generated by an on chip scan oscillator and scan counter/decoder. By connecting a resistor and capacitor to the Scan Oscillator control terminal, it is possible to control the duty cycle and frequency of the decade strobe outputs so that output characteristics can be made suitable for several different types of displays. The Scan Oscillator input may be driven by an external source if desired. The Scan Counter changes on the negative going transition of the Scan Oscillator input.

A delay circuit on the Hold/Load latches input is present in the HCTR6010 but not in the HCTR6010A and HCTR6010B. The delay is long enough to ensure that a count "rippling" through the counter will be stabilized and correctly loaded into the latches even if load latches and clock advance signals are applied simultaneously.

The clock out signal may be used for cascading devices by connecting it to the clock in of the following device. The clock out signal is a positive going pulse with leading edge coincident with the positive going transition of the clock input following count 9999. The trailing edge is coincident with the 1 - 0 transition of the clock input which drives the counter into state 10000.

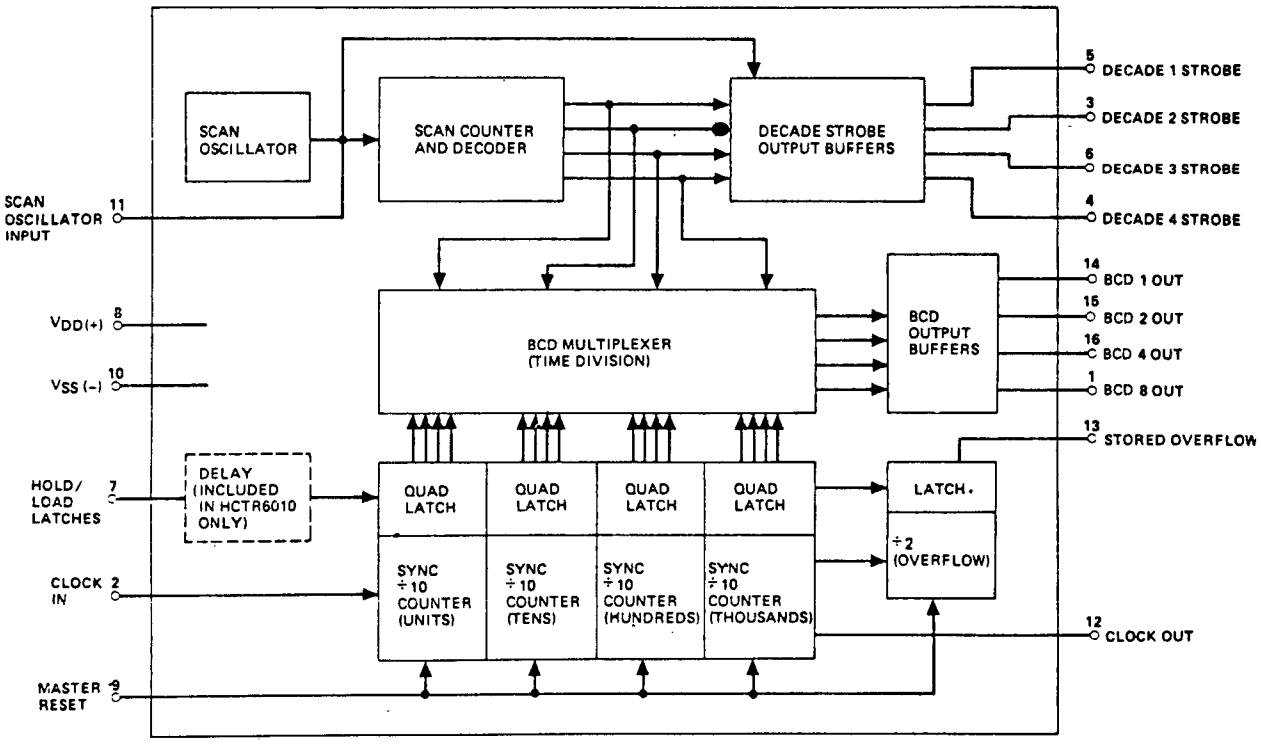


FIGURE 8 – EXPANDED BLOCK DIAGRAM OF HCTR6010/A/B

HUGHES

HUGHES AIRCRAFT COMPANY
MICROELECTRONIC PRODUCTS DIVISION

MOTOROLA

MC14411

BIT RATE GENERATOR

The MC14411 bit rate generator is constructed with complementary MOS enhancement mode devices. It utilizes a frequency divider network to provide a wide range of output frequencies.

A crystal controlled oscillator is the clock source for the network. A two-bit address is provided to select one of four multiple output clock rates.

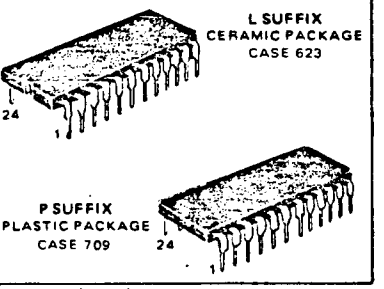
Applications include a selectable frequency source for equipment in the data communications market, such as teleprinters, printers, CRT terminals, and microprocessor systems.

- Single 5.0 Vdc (± 5%) Power Supply
- Internal Oscillator Crystal Controlled for Stability (1.8432 MHz)
- Sixteen Different Output Clock Rates
- 50% Output Duty Cycle
- Programmable Time Bases for One of Four Multiple Output Rates
- Buffered Outputs Compatible with Low Power TTL
- Noise Immunity = 45% of V_{DD} Typical
- Diode Protection on All Inputs
- External Clock May be Applied to Pin 21

CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

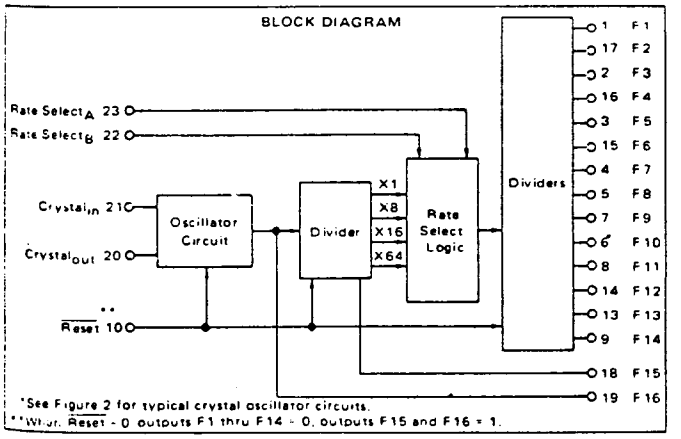
BIT RATE GENERATOR



MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 12.)

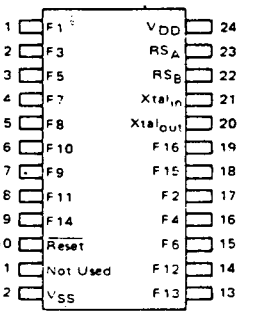
Rating	Symbol	Value	Unit
DC Supply Voltage Range	V_{DD}	5.25 to -0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} + 0.5 to V_{SS} -0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

BLOCK DIAGRAM



*See Figure 2 for typical crystal oscillator circuits.
**When Reset = 0 outputs F1 thru F14 = 0, outputs F15 and F16 = 1.

PIN ASSIGNMENT



V_{DD} = Pin 24
V_{SS} = Pin 12

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	-40°C Min	-40°C Max	25°C Min	25°C Typ	25°C Max	+85°C Min	+85°C Max	Unit
Supply Voltage	V_{DD}	–	4.75	5.25	4.75	5.0	5.25	4.75	5.25	Vdc
Output Voltage "0" Level	V_{out}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
Output Voltage "1" Level		5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
Input Voltage (V_O = 4.5 or 0.5 Vdc)	V_{IL}	5.0	–	1.5	–	2.25	1.5	–	1.5	Vdc
Input Voltage (V_O = 0.5 or 4.5 Vdc)	V_{IH}	5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
Output Drive Current (V_{OH} = 2.5 Vdc) Source	I_{OH}	5.0	-0.23	–	-0.20	-1.7	–	-0.16	–	mAdc
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.23	–	0.20	0.78	–	0.16	–	mAdc
Input Current	I_{in}	–	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation	P_Q	5.0	–	2.5	–	0.015	2.5	–	15	mW
Power Dissipation**† (Dynamic plus Quiescent) (C_L = 15 pF)	P_D	5.0	(P_D = (7.5 mW/MHz) f + P_Q							mW
Output Rise Time** t_{TLH} = (3.0 ns/pF) C_L + 25 ns	t_{TLH}	5.0	–	–	–	70	200	–	–	ns
Output Fall Time** t_{THL} = (1.5 ns/pF) C_L + 47 ns	t_{THL}	5.0	–	–	–	70	200	–	–	ns
Input Clock Frequency	f_{CL}	5.0	–	1.85	–	–	1.85	–	1.85	MHz

† For dissipation at different external load capacitance (C_L) refer to corresponding formula:

$P_T(C_L) = P_D + 2.6 \times 10^{-3} (C_L - 15\ pF) V_{DD}^2 f$

where: P_T, P_D in mW, C_L in pF, V_{DD} in Vdc, and f in MHz.

**The formula given is for the typical characteristics only.

TABLE 1 – OUTPUT CLOCK RATES

Rate Select B	Rate Select A	Rate
0	0	X1
0	1	X8
1	0	X16
1	1	X64

Output Number	Output Rates (Hz) X64	X16	X8	X1
F1	614.4 k	153.6 k	76.8 k	9600
F2	460.8 k	115.2 k	57.6 k	7200
F3	307.2 k	76.8 k	38.4 k	4800
F4	230.4 k	57.6 k	28.8 k	3600
F5	153.6 k	38.4 k	19.2 k	2400
F6	115.2 k	28.8 k	14.4 k	1800
F7	76.8 k	19.2 k	9600	1200
F8	38.4 k	9600	4800	600
F9	19.2 k	4800	2400	300
F10	12.8 k	3200	1600	200
F11	9600	2400	1200	150
F12	8613.2	2153.3	1076.6	134.5
F13	7035.5	1758.8	879.4	109.9
F14	4800	1200	600	75
F15	921.6 k	921.6 k	921.6 k	921.6 k
F16*	1.843M	1.843M	1.843M	1.843M

*F16 is buffered oscillator output.

FIGURE 1 – DYNAMIC SIGNAL WAVEFORMS

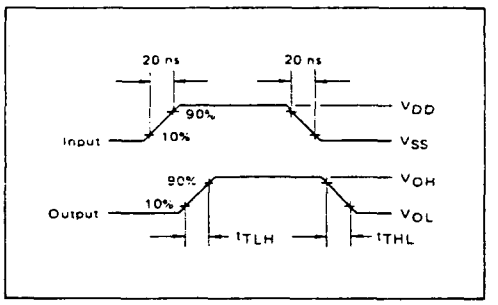
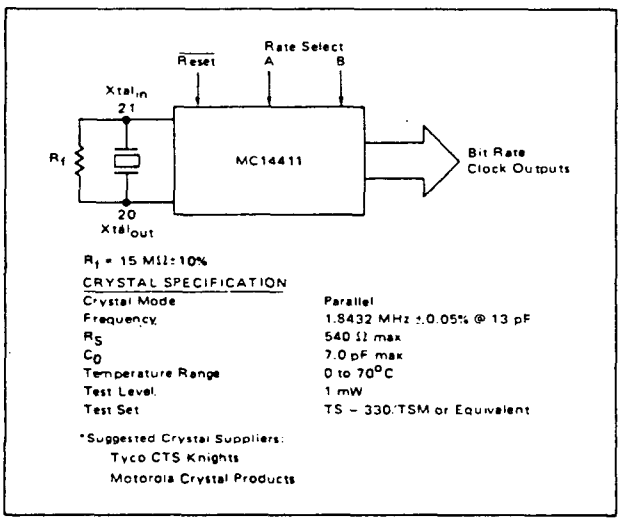


FIGURE 2 – TYPICAL CRYSTAL OSCILLATOR CIRCUIT



R_f = 15 MΩ ±10%

CRYSTAL SPECIFICATION

Crystal Mode	Parallel
Frequency	1.8432 MHz ±0.05% @ 13 pF
R_S	540 Ω max
C_0	7.0 pF max
Temperature Range	0 to 70°C
Test Level	1 mW
Test Set	TS – 330/TSM or Equivalent

*Suggested Crystal Suppliers:
Tyco CTS Knights
Motorola Crystal Products

MOTOROLA

MC14517B

CMOS LSI

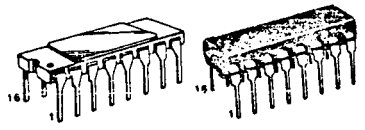
(LOW-POWER COMPLEMENTARY MOS)

DUAL 64-BIT STATIC SHIFT REGISTER

DUAL 64-BIT STATIC SHIFT REGISTER

The MC14517B dual 64-bit static shift register consists of two identical, independent, 64-bit registers. Each register has separate clock and write enable inputs, as well as outputs at bits 16, 32, 48, and 64. Data at the data input is entered by clocking, regardless of the state of the write enable input. An output is disabled (open circuited) when the write enable input is high. During this time, data appearing at the data input as well as the 16-bit, 32-bit, and 48-bit taps may be entered into the device by application of a clock pulse. This feature permits the register to be loaded with 64 bits in 16 clock periods, and also permits bus logic to be used. This device is useful in time delay circuits, temporary memory storage circuits, and other serial shift register applications.

- Quiescent Current = 10 nA/package typical @ 5 Vdc
- *Noise Immunity = 45% of V_{DD} typical*
- Diode Protection on All Inputs
- Fully Static Operation
- Output Transitions Occur on the Rising Edge of the Clock Pulse
- 6.7 MHz Operation @ V_{DD} = 10 Vdc
- Exceedingly Slow Input Transition Rates May Be Applied to the Clock Input
- 3-State Output at 64th-Bit Allows Use in Bus Logic Applications
- Shift Registers of any Length may be Fully Loaded with 16 Clock Pulses
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range



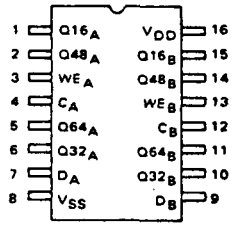
L SUFFIX
CERAMIC PACKAGE
CASE 690

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

PIN ASSIGNMENT



MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

FUNCTIONAL TRUTH TABLE

CLOCK	WRITE ENABLE	DATA	16-BIT TAP	32-BIT TAP	48-BIT TAP	64-BIT TAP
0	0	X	Content of 16-Bit Displayed	Content of 32-Bit Displayed	Content of 48-Bit Displayed	Content of 64-Bit Displayed
0	1	X	High Impedance	High Impedance	High Impedance	High Impedance
1	0	X	Content of 16-Bit Displayed	Content of 32-Bit Displayed	Content of 48-Bit Displayed	Content of 64-Bit Displayed
1	1	X	High Impedance	High Impedance	High Impedance	High Impedance
↗	0	Data entered into 1st Bit	Content of 16-Bit Displayed	Content of 32-Bit Displayed	Content of 48-Bit Displayed	Content of 64-Bit Displayed
↗	1	Data entered into 1st Bit	Data at tap entered into 17-Bit	Data at tap entered into 33-Bit	Data at tap entered into 49-Bit	High Impedance
↘	0	X	Content of 16-Bit Displayed	Content of 32-Bit Displayed	Content of 48-Bit Displayed	Content of 64-Bit Displayed
↘	1	X	High Impedance	High Impedance	High Impedance	High Impedance

X = Don't Care

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in}= 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	–0.5	–0.9	–	–0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	–1.5	–3.5	–	–1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	–0.8	–1.7	–	–0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	–0.16	–0.36	–	–0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	–0.4	–0.9	–	–0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	–1.2	–3.5	–	–1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.010	5.0	–	150	µAdc
(Per Package)		10	–	10	–	0.020	10	–	300	
		15	–	20	–	0.030	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	50	–	0.010	50	–	375	µAdc
(Per Package)		10	–	100	–	0.020	100	–	750	
		15	–	200	–	0.030	200	–	1500	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (4.2 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (8.8 µA/kHz) f + I_{DD}							
		15	I_T = (13.7 µA/kHz) f + I_{DD}							
Three-State Leakage Current (AL Device)	I_{TL}	15	–	±0.1	–	±0.00001	±0.1	–	±3.0	µAdc
Three-State Leakage Current (CL/CP Device)	I_{TL}	15	–	±1.0	–	±0.00001	±1.0	–	±7.5	µAdc

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 4 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	180	360	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	90	180	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	65	130	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH},					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 390 ns	t_{PHL}	5.0	–	475	770	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 177 ns		10	–	210	300	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 115 ns		15	–	140	215	
Clock Pulse Width	t_{WH}	5.0	330	170	–	ns
		10	125	75	–	
		15	100	60	–	
Clock Pulse Frequency	f_{cl}	5.0	–	3.0	1.5	MHz
		10	–	6.7	4.0	
		15	–	8.3	5.3	
Clock Pulse Rise and Fall Time	t_{TLH}, t_{THL}	5.0	**See Note			–
		10				
		15				
Data to Clock Setup Time	t_{su}	5.0	0	-40	–	ns
		10	10	-15	–	
		15	15	0	–	
Data to Clock Hold Time	t_h	5.0	150	75	–	ns
		10	75	25	–	
		15	35	10	–	
Write Enable to Clock Setup Time	t_{su}	5.0	400	170	–	ns
		10	200	65	–	
		15	110	50	–	
Write Enable to Clock Release Time	t_{rel}	5.0	380	160	–	ns
		10	180	55	–	
		15	100	40	–	

*The formula given is for the typical characteristics only.

**When shift register sections are cascaded, the maximum rise and fall time of the clock input should be equal to or less than the rise and fall time of the data outputs, driving data inputs, plus the propagation delay of the output driving stage.

FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

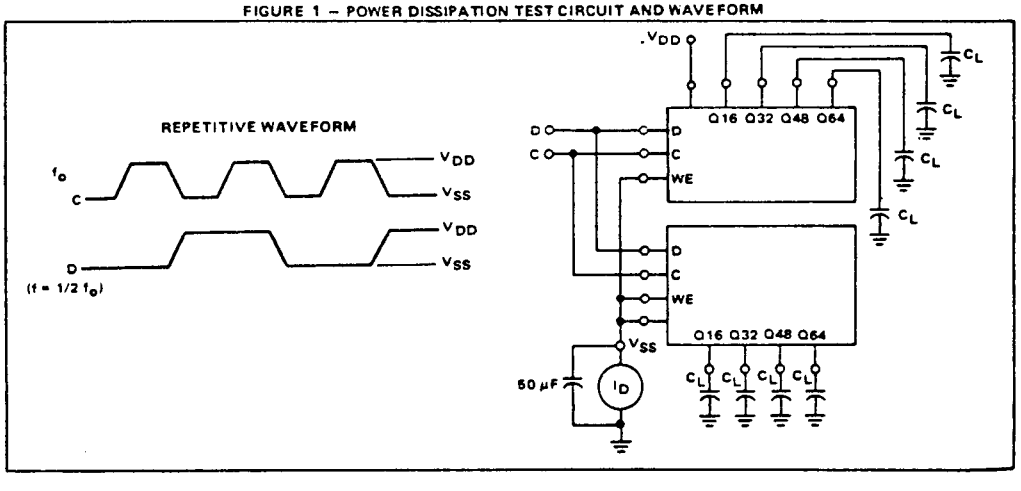
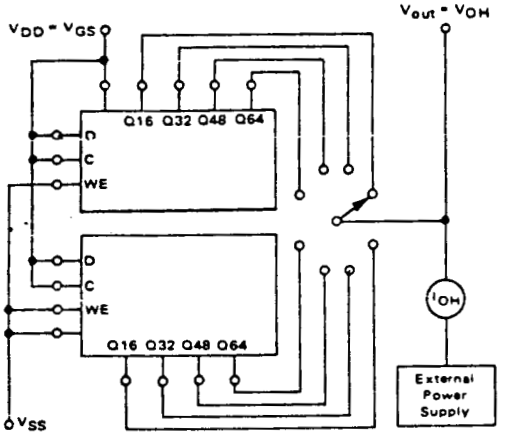
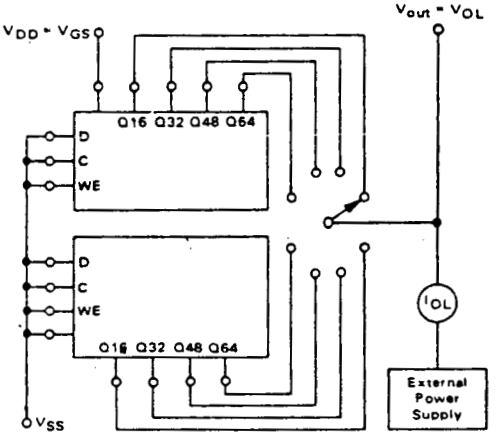


FIGURE 2 – TYPICAL OUTPUT SOURCE CURRENT CHARACTERISTICS TEST CIRCUIT



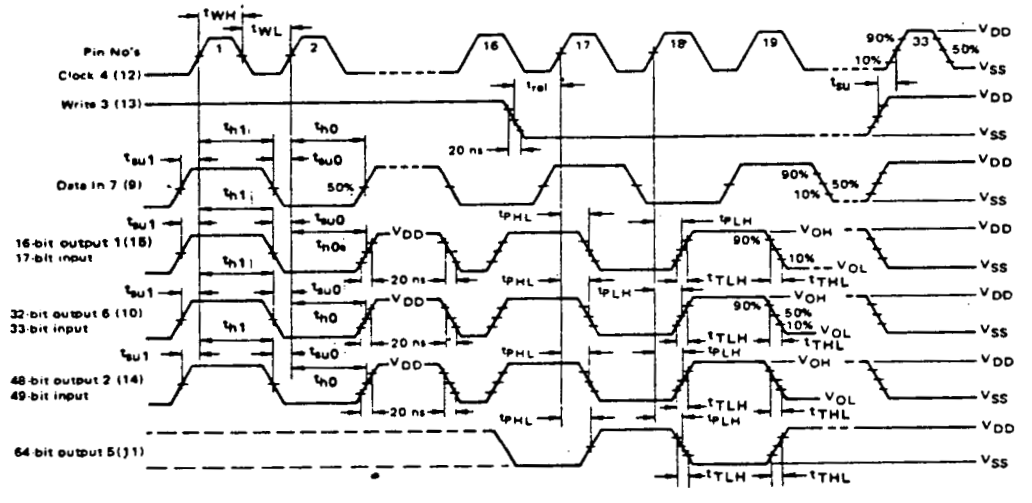
(Output being tested should be in the high-logic state).

FIGURE 3 – TYPICAL OUTPUT SINK CURRENT CHARACTERISTICS TEST CIRCUIT

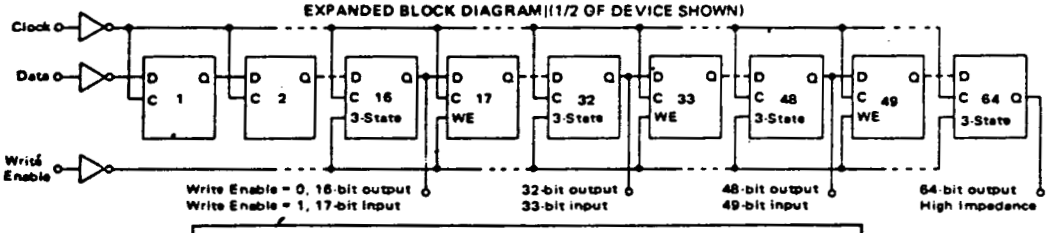


(Output being tested should be in the low-logic state).

FIGURE 4 – AC TEST WAVEFORMS



EXPANDED BLOCK DIAGRAM (1/2 OF DEVICE SHOWN)



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

MOTOROLA

MC14557B

1-TO-64 BIT VARIABLE LENGTH SHIFT REGISTER

The MC14557B is a static clocked serial shift register whose length may be programmed to be any number of bits between 1 and 64. The number of bits selected is equal to the sum of the subscripts of the enabled Length Control inputs (L1, L2, L4, L8, L16, and L32) plus one. Serial data may be selected from the A or B data inputs with the A/B select input. This feature is useful for recirculation purposes. A Clock Enable ($\overline{CE}$) input is provided to allow gating of the clock or negative edge clocking capability.

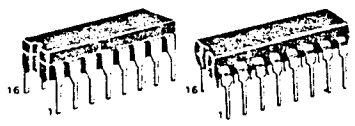
The device can be effectively used for variable digital delay lines or simply to implement odd length shift registers. characteristics can be found on the Family Data Sheet.

- Quiescent Current = 10 nA/package typical @ 5 Vdc
- 1-64 Bit Programmable Length
- Q and $\overline{Q}$ Serial Buffered Outputs
- Asynchronous Master Reset
- All Inputs Buffered
- No Limit On Clock Rise and Fall Times
- 8 MHz Operation @ V_{DD} = 10 Vdc Typical
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

1-TO-64 BIT
VARIABLE LENGTH
SHIFT REGISTER



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

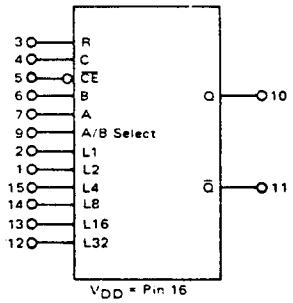
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL, CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

LENGTH SELECT TRUTH TABLE

L32	L16	L8	L4	L2	L1	Register Length
0	0	0	0	0	0	1 Bit
0	0	0	0	0	1	2 Bits
0	0	0	0	1	0	3 Bits
0	0	0	0	1	1	4 Bits
0	0	0	1	0	0	5 Bits
0	0	0	1	0	1	6 Bits
.	.	.	.	.	.	.
.	.	.	.	.	.	.
.	.	.	.	.	.	.
1	0	0	0	0	0	33 Bits
1	0	0	0	0	1	34 Bits
.	.	.	.	.	.	.
.	.	.	.	.	.	.
.	.	.	.	.	.	.
1	1	1	1	0	0	61 Bits
1	1	1	1	0	1	62 Bits
1	1	1	1	1	0	63 Bits
1	1	1	1	1	1	64 Bits

Note: Length equals the sum of the binary length control subscripts plus one.

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

TRUTH TABLE

Inputs				Output
R	A/B	Clock	$\overline{CE}$	Q
0	0	⌐	0	B
0	1	⌐	0	A
0	0	1	¬	B
0	1	1	¬	A
1	X	X	X	0

Q is the output of the first selected shift register stage.
X = Don't Care.

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									Vdc
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-1.2	–	-1.0	-1.7	–	-0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.25	–	-0.2	-0.36	–	-0.14	–	
(V_{OH} = 9.5 Vdc)		10	-0.62	–	-0.5	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)		15	-1.8	–	-1.5	-3.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-1.0	–	-0.8	-1.7	–	-0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.2	–	-0.16	-0.36	–	-0.12	–	
(V_{OH} = 9.5 Vdc)		10	-0.5	–	-0.4	-0.9	–	-0.3	–	
(V_{OH} = 13.5 Vdc)		15	-1.4	–	-1.2	-3.5	–	-1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.010	5.0	–	150	μAdc
(Per Package)		10	–	10	–	0.020	10	–	300	
		15	–	20	–	0.030	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	50	–	0.010	50	–	375	μAdc
(Per Package)		10	–	100	–	0.020	100	–	750	
		15	–	200	–	0.030	200	–	1500	
Total Supply Current** (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.75 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (3.5 μA/kHz) f + I_{DD}							
		15	I_T = (5.25 μA/kHz) f + I_{DD}							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 1 \times 10^{-3}\ (C_L - 50)\ V_{DD} f$
where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.

**The formulas given are for the typical characteristics only at 25°C.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

Minimum No. of Bits Selected	Typical Setup Time B → $\overline{CE}$ ns	Length Select Lines = 1
1	180	None
2	120	L1
3	90	L2
5	60	L4
9	30	L8
17	0	L16
33	-30	L32

SETUP TIME CHART

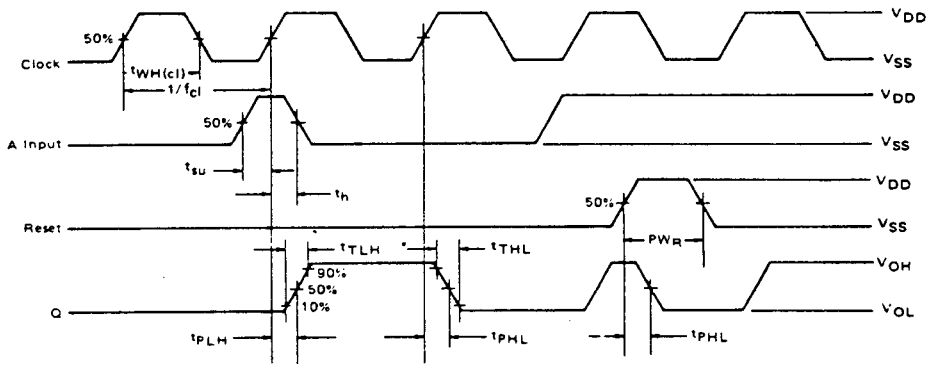
The nature of the length select logic causes the setup time to vary with the number of bits selected. The following table summarizes the typical variation at V_{DD} = 10 V, T_A = 25°C.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise Time	t_{PLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	180	360	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	90	180	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	65	130	
Output Fall Time	t_{PHL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
(C or CE to Q or Q)						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 415 ns		5.0	–	500	1000	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 167 ns		10	–	200	400	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 125 ns		15	–	150	300	
(R to Q or Q)						ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 390 ns		5.0	–	475	550	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 157 ns		10	–	190	380	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 115 ns		15	–	140	280	
Clock Pulse Width	$t_{WH(C)}$	5.0	440	220	–	ns
		10	136	68	–	
		15	100	50	–	
Reset Pulse Width	$t_{WH(R)}$	5.0	600	300	–	ns
		10	180	90	–	
		15	120	60	–	
Clock Pulse Frequency	f_{cl}	5.0	–	2.5	1.7	MHz
		10	–	8.0	5.0	
		15	–	10.5	6.7	
Clock Pulse Rise and Fall Time	t_{TLH}, t_{THL}	5.0	No Limit			–
		10				
		15				
Data to Clock Setup Time (A or B to C or CE) L1, L2, L4, L8, L16, L32 = 0	t_{su}	5.0	900	450	–	ns
		10	360	180	–	
		15	170	135	–	
Data to Clock Hold Time (A or B to C or CE) L1, L2, L4, L8, L16, L32 = 0	t_h	5.0	-225	-450	–	ns
		10	- 90	-180	–	
		15	- 60	-135	–	
Reset Fall Time	t_{TLH}	5.0	–	–	15	μs
		10	–	–	5	
		15	–	–	4	

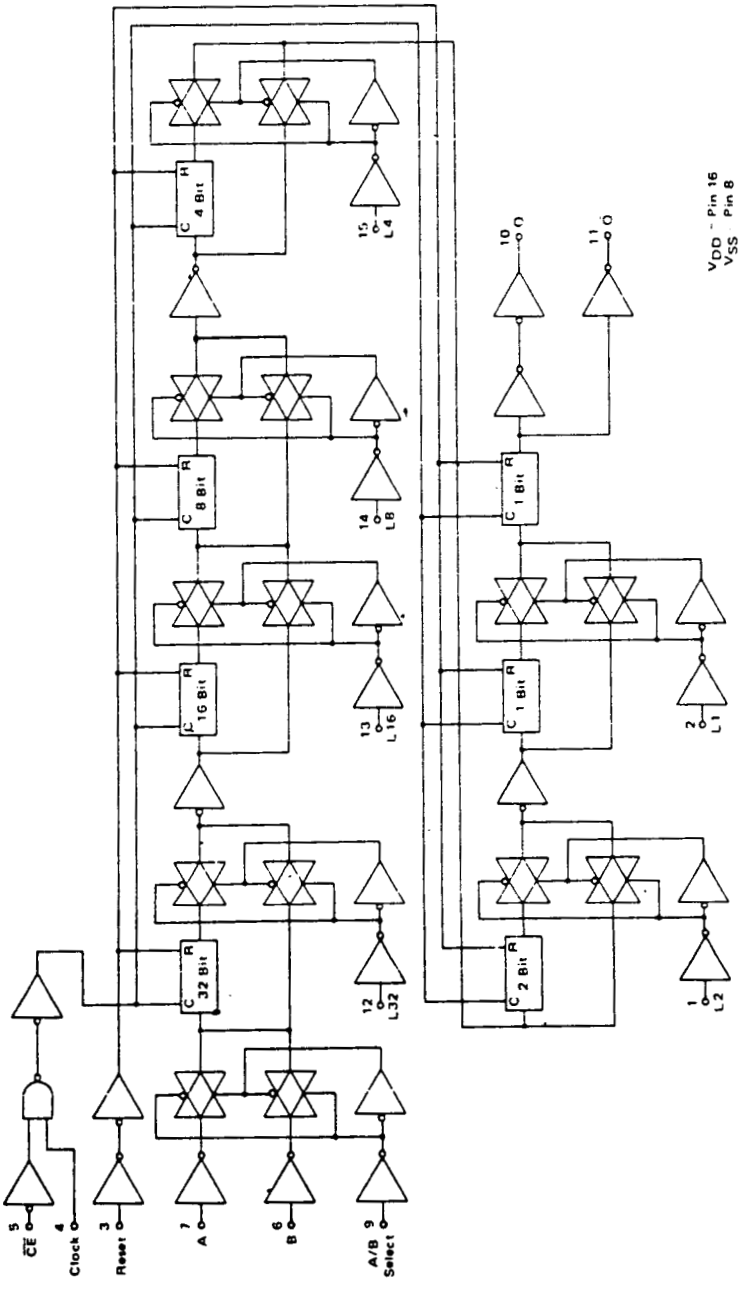
*The formula given is for the typical characteristics only.

TIMING DIAGRAM



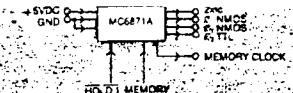
1-bit length:
$\overline{CE}$ = 0
A/B = 1
L1 = L2 = L4 = L8 = L16 = L32 = 0

LOGIC DIAGRAM



MC6871A

full function microprocessor clock
850 kHz to 2.5 MHz



specifications

Rating	Symbol	Value	Unit
Supply Voltage	V_{cc}	5.00±5%	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Power Supply Drain (max.)	I_{pd}	100	mA

ELECTRICAL CHARACTERISTICS (V_{cc} = 5.0 ± 5%, V_{ss} = 0, T_A = 0° to 70°C, unless otherwise noted)

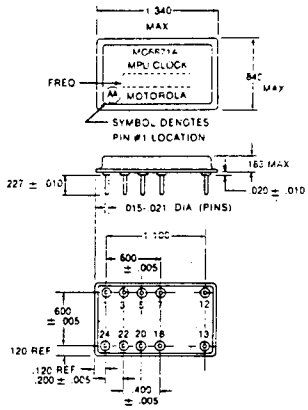
Characteristic	Symbol	Min	Typ	Max	Unit
Frequency					
Operating Frequency	f_c	.850		2.5	MHz
Frequency stability (inclusive of calibration tolerance at +25°C, operating temperature, input voltage change, load change, aging, shock and vibration)			±.01		%
NMOS Outputs at 1.0 MHz Operation* **					
Pulse Width (meas. at V_{cc} = −.3V dc level)	$TØ_1H$ $TØ_2H$	430 450			ns ns
Logic Levels	V_{OLC} V_{OHC}	V_{ss}-.1 V_{cc}-.3	— —	V_{ss}+.3 V_{cc}+.1	Vdc Vdc
Rise and Fall Times	t_r t_f	5 5	12 12	50 50	ns ns
*Overshoot/Undershoot Logic "1" Logic "0"	 V_{OS}	 V_{cc}-.5 V_{ss}-.5		 V_{cc}+.5 V_{ss}+.5	 Vdc Vdc
Pulse duration of any overshoot or undershoot	T_{OS}			40	ns
Period @ 0.3V dc Level	t_{cyc}		1.00		us
Edge Timing @ V_{cc}=0.3V dc	Tx	940			ns
NMOS Relationship @ +0.5V dc Level	t_{d1} t_{d2}	0 0		 8.0	 us
TTL Outputs					
In ref. to $Ø_2$ NMOS @ 0.3V dc					
$Ø_2$ TTL @ 1.4V dc	T_A T_H	15 10	30 25	45 40	ns ns
Memory Clock @ 1.4V dc	T_C T_J	30 20	50 40	70 60	ns ns
2xfc @ 1.4V dc	T_B	40	80	120	ns
Logic Levels	V_{OH} V_{OL}	2.4	3.2 .3	 .4	Vdc Vdc
Rise and Fall Times .4V and 2.4V 2.4V and .4V	 t_r t_f			 15 15	 ns ns
Logic "0" Sink (/Gate)	I_{OL}			−1.6	mA
Logic "1" Source (/Gate)	I_{OH}			+40	uA
Current Output Shorted	I_{SC}	−18		−57	mA
Load					
NMOS—Load Capacity $Ø_1$, $Ø_2$	C_{NMOS}	80	120	160	pf
TTL—No. of Loads				5	ttl
TTL—Load Capacity	C_{TTL}			50	pf
Logic Inputs ("0" Level Applies HOLD or MEMORY READY)**					
Holds $Ø_1$ NMOS 'High', $Ø_2$ NMOS 'Low', $Ø_2$ TTL 'Low'	$\overline{HOLD\ 1}$	−.2		+.4	Vdc
Holds $Ø_1$ NMOS 'Low', $Ø_2$ NMOS 'High', $Ø_2$ TTL 'High', and MEMORY CLOCK 'High'	MEMORY READY	−.2		+.4	Vdc

*Into specified test load

**Must be externally held at "1" level (2.4V min., 5.0V max.) if not used

***Apply the following parameters for frequencies other than 1 MHz:
$TØ_1H$=0.5 (P-140) ns
$TØ_2H$=0.5 (P-100) ns
Tx=(P-60) ns
where P=desired period of operation in nanoseconds

DIMENSIONS

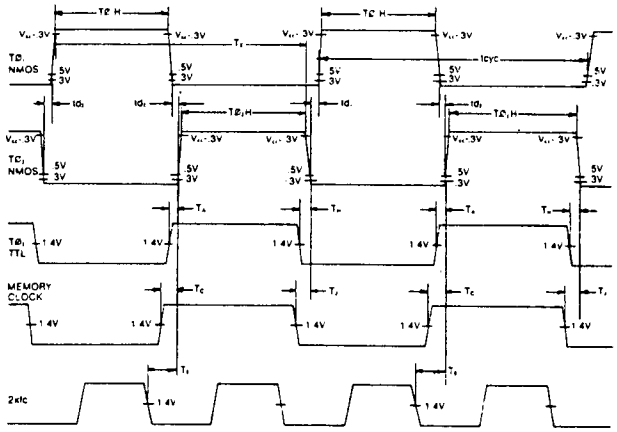


PIN	CONNECTION
1	GND
3	MEMORY CLOCK
5	$Ø_1$ TTL
7	V_{cc} (+5VDC)
12	$Ø_2$ NMOS
13	$Ø_1$ NMOS
18	GND
20	$\overline{HOLD\ 1}$
22	MEMORY READY
24	2xfc

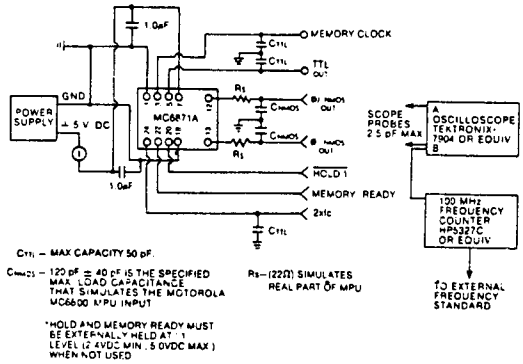
Note: All dimensions are in inches

WAVEFORM TIMING

(ALL TIME IN NANOSECONDS)



TEST CIRCUIT



C_{TTL} – MAX CAPACITY 50 pF.

C_{NMOS} – 120 pF ± 40 pF IS THE SPECIFIED MAX. LOAD CAPACITANCE THAT SIMULATES THE MOTOROLA MC6800 MPU INPUT

R_S – (220Ω) SIMULATES REAL PART OF MPU

*HOLD AND MEMORY READY MUST BE EXTERNALLY HELD AT "1" LEVEL (2.4VDC MIN., 5.0VDC MAX.) WHEN NOT USED

specifications

Rating	Symbol	Value	Unit
Supply Voltage	V_{cc}	5.00±5%	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Power Supply Drain (max.)	I_{pd}	100	mA

ELECTRICAL CHARACTERISTICS (V_{cc} = 5.0 ± 5%, V_{ss} = 0, T_A = 0° to 70°C, unless otherwise noted)

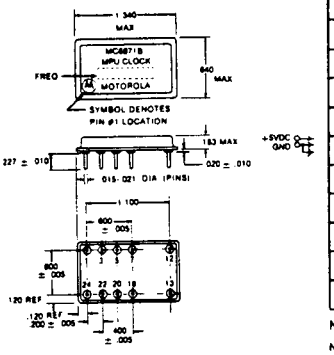
Characteristic	Symbol	Min	Typ	Max	Unit
Frequency					
Operating Frequency Frequency stability (inclusive of calibration tolerance at +25°C, operating temperature, input voltage change, load change, aging, shock and vibration)	f_o	.250	±.01	2.5	MHz %
NMOS Outputs at 1.0 MHz Operation***					
Pulse Width (meas. at V_{cc} = −.3V dc level)	$T\emptyset_1H$ $T\emptyset_2H$	430 450			ns ns
Logic Levels	V_{OLC} V_{OHC}	V_{ss}-.1 V_{cc}-.3	— —	V_{ss}+.3 V_{cc}+.1	Vdc Vdc
Rise and Fall Times	t_r t_f	5 5	12 12	50 50	ns ns
*Overshoot/Undershoot Logic "1" Logic "0"	V_{OS}	V_{cc}-.5 V_{ss}-.5		V_{cc}+.5 V_{ss}+.5	Vdc Vdc
Pulse duration of any overshoot or undershoot	T_{OS}			40	ns
Period @ 0.3V dc Level	t_{cyc}		1.00		us
Edge Timing @ V_{cc}=0.3V dc	Tx	940			ns
NMOS Relationship @ +0.5V dc	t_{d1} t_{d2}	0 0		8.0	us
TTL Outputs					
In ref. to $\emptyset_2$ NMOS @ 0.3V dc					
$\emptyset_2$ TTL @ 1.4V dc	T_A T_H	15 10	30 25	45 40	ns ns
$\emptyset_2$ Ungated @ 1.4V dc	T_C T_J	30 20	50 40	70 60	ns ns
2xfc @ 1.4V dc	T_B	40	80	120	ns
Logic Levels	V_{OH} V_{OL}	2.4	3.2 .3	.4	Vdc Vdc
Rise and Fall Times .4V and 2.4V 2.4V and .4V	t_r t_f			15 15	ns ns
Logic "0" Sink (/Gate)	I_{OL}			−1.6	mA
Logic "1" Source (/Gate)	I_{OH}			+40	uA
Current Output Shorted	I_{SC}	−18		−57	mA
Load					
NMOS—Load Capacity $\emptyset_1$, $\emptyset_2$	C_{NMOS}	80	120	160	pf
TTL—No. of Loads				5	ttl
TTL—Load Capacity	C_{TTL}			50	pf
Logic Inputs ("0" Level applies HOLD)**					
Holds $\emptyset_1$ NMOS 'High', $\emptyset_2$ NMOS 'Low', $\emptyset_2$ TTL 'Low'	$\overline{HOLD\ 1}$	−.2		+.4	Vdc
Holds $\emptyset_1$ NMOS 'Low', $\emptyset_2$ NMOS 'High', $\emptyset_2$ TTL 'High'	$\overline{HOLD\ 2}$	−.2		+.4	Vdc

*Into specified test load

**Must be externally held at "1" level (2.4V min., 5.0V max.) if not used

***Apply the following parameters for frequencies other than 1 MHz:
$T\emptyset_1H$=0.5 (P-140) ns
$T\emptyset_2H$=0.5 (P-100) ns
Tx=(P-60) ns
where P=desired period of operation in nanoseconds

DIMENSIONS



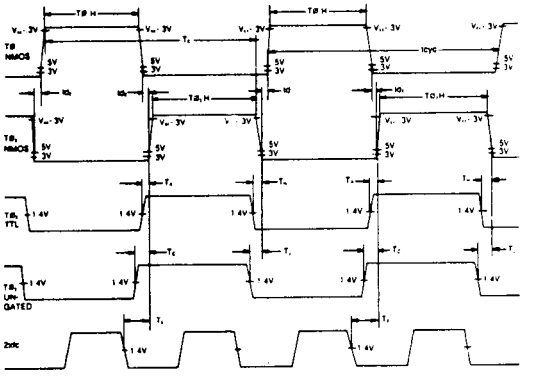
PIN	CONNECTION
1	GND
3	$\emptyset_2$ TTL UNGATED
5	$\emptyset_2$ TTL
7	V_{cc} (+5VDC)
12	$\emptyset_2$ NMOS
13	$\emptyset_1$ NMOS
18	GND
20	$\overline{HOLD\ 1}$
22	$\overline{HOLD\ 2}$
24	2xfc

Note: 4xfc available on request

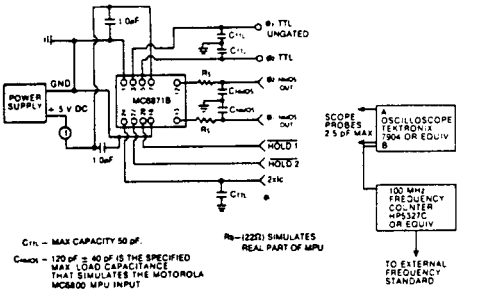
Note. All dimensions are in inches

WAVEFORM TIMING.

ALL TIME IN NANOSECONDS.



TEST DIAGRAM



C_{TTL} – MAX CAPACITY 50 pF.

C_{NMOS} – 120 pF ± 40 pF IS THE SPECIFIED MAX. LOAD CAPACITANCE THAT SIMULATES THE MOTOROLA MC6800 MPU INPUT

"HOLD" 1 AND HOLD 2 MUST BE EXTERNALLY HELD AT "1" LEVEL (2.4VDC MIN., 5.0VDC MAX.) WHEN NOT USED

R_S–(22Ω) SIMULATES REAL PART OF MPU

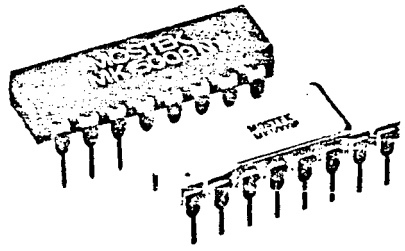
MOTOROLA INC. COMPONENT PRODUCTS DEPT.
2553 N. Edgington Franklin Park, Ill. 60131 312/451-1000

R29-3-5

MOS Counter Time-Base Circuit

MOSTEK

- Ion-implanted for full TTL/DTL compatibility
- Internal clock operates from:
  - External signal
  - External RC network
  - External crystal
- Operates DC to above 1 MHz
- Binary-encoded for frequency selection



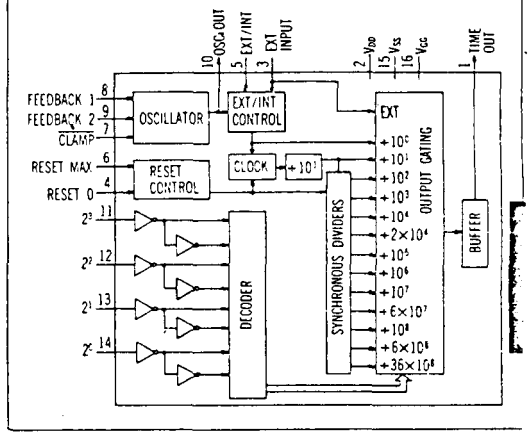
DESCRIPTION

The MK 5009 P is a highly versatile MOS oscillator and divider chain manufactured by Mostek using its depletion-load, ion-implantation process and P.-channel technology. The 16-pin DIP package provides frequency division ranges from 1 to 36×10^8. The circuit will operate from any of three frequency sources: the internal oscillator with an external RC combination; the internal oscillator with an external crystal; or with an externally-applied TTL signal. Control inputs provide additional versatility and allow the circuit to be used in a variety of applications including instruments, timers, and clocks.

With an input frequency of 1 MHz, the MK 5009 P provides the basic time periods necessary for most frequency measuring instruments, i.e., 1 μs through 100 seconds. One-minute, ten-minute, and one-hour periods are also available using a 1 MHz input. Using a 1/1.2 MHz input, the MK 5009 P can also provide a 50/60 Hz output for accurate generation of line frequencies in portable instruments or clocks.

The time-base output (TIME OUT) is a square wave, its frequency determined by the selected counter division, and by the oscillator frequency or external input. The falling edge of the output square wave should be used to control external gating circuitry.

FUNCTIONAL DIAGRAM



TIME OUT

ADDRESS INPUTS				WITHOUT RESET	RESET		BYPASS MODES (see page 3)		
					Reset Max.	Reset Min.	Mode 1	Mode 2	Mode 3
				$R_{MAX}=0$	$R_{MAX}=1$	$R_{MAX}=0$	$R_{MAX}=V_{GG}$	$R_{MAX}=0$	$R_{MAX}=V_{GG}$
2^3	2^2	2^1	2^0	$R_O=0$	$R_O=0$	$R_O=1$	$R_O=0$	$R_O=V_{GG}$	$R_O=V_{GG}$
0	0	0	0	$\div 10^0$	$\div 10^0$	$\div 10^0$	$\div 10^0$	$\div 10^0$	$\div 10^0$
0	0	0	1	$\div 10^1$			$\div 10^1$	$\div 10^1$	$\div 10^1$
0	0	1	0	$\div 10^2$	Resets	Resets	$\div 10^2$	$\div 10^2$	$\div 10^2$
0	0	1	1	$\div 10^3$			$\div 10^3$	$\div 10^3$	$\div 10^3$
0	1	0	0	$\div 10^4$	Counters	Counters	$\div 10^4$	$\div 10^4$	$\div 10^4$
0	1	0	1	$\div 10^5$			$\div 10^2$	$\div 10^5$	$\div 10^2$
0	1	1	0	$\div 10^6$	to their	to their	$\div 10^3$	$\div 10^6$	$\div 10^3$
0	1	1	1	$\div 10^7$			$\div 10^4$	$\div 10^7$	$\div 10^4$
1	0	0	0	$\div 10^8$	Highest	Lowest	$\div 10^5$	$\div 10^5$	$\div 10^2$
1	0	0	1	$\div 6\times10^7$			$\div 6\times10^4$	$\div 6\times10^4$	$\div 6\times10^1$
1	0	1	0	$\div 36\times10^8$	States	States	$\div 36\times10^5$	$\div 36\times10^5$	$\div 36\times10^2$
1	0	1	1	$\div 6\times10^8$			$\div 6\times10^5$	$\div 6\times10^5$	$\div 6\times10^2$
1	1	1	0	$\div 2\times10^4$			$\div 2\times10^1$	$\div 2\times10^1$	$\div 2\times10^1$
1	1	1	1	Ext. In.	Ext. In.	Ext. In.	Ext. Int.	Ext. Int.	Ext. Int.

*Addresses 1100 and 1101 result in Logic 0 at the output regardless of the state of the Reset Max. and Reset 0 inputs.

Logic 1 = High = V_{SS}

Logic 0 = Low = V_{DD}

ABSOLUTE MAXIMUM RATINGS

Voltage on Any Terminal Relative to V_{SS} . . . . . + 0.3V to − 20V
Operating Temperature Range (Ambient) . . . . . 0°C to +70°C
Storage Temperature Range (Ambient) . . . . . − 55 C to + 150°C

RECOMMENDED OPERATING CONDITIONS

($0°C \leq T_A \leq 70°C$)

	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{SS}	Supply Voltage	+ 4.5		+ 5.5	V	
V_{DD}	Supply Voltage	0.0		0.0	V	
V_{GG}	Supply Voltage	− 9.6		− 14.4	V	
f_{XTAL}	Crystal Frequency	0.1		2.0	MHz	
f_{RC}	RC Frequency	DC		200	kHz	
f_{EXT}	External Frequency	DC		2.0	MHz	
t_{PL}	Logic 0 Pulse Width, $\overline{CLAMP}$	—				Note 5
	Ext. Input	200			nsec	
t_{PH}	Logic 1 Pulse Width, Ext. Input	200			nsec	
	Reset Max	10.0			μsec	
	Reset 0	10.0			μsec	
R	Feedback Resistance	.01		2.5	MΩ	Fig. 1
V_{IL}	Input Voltage, Logic 0, Reset Inputs	0.0		0.8	V	
	Reset (Bypass Mode)	V_{GG}		V_{GG} + 1.0	V	Note 2
	All Other Logic Inputs			0.8	V	
V_{IH}	Input Voltage, Logic 1, All Logic Inputs	V_{SS}-1.0	V_{SS}	V_{SS} + 0.3	V	

ELECTRICAL CHARACTERISTICS

(V_{SS} = +5V ±10%; V_{DD} = 0V; V_{GG} = −12.0V ±20%; 0°C $\leq T_A \leq$ 70°C)

	PARAMETER	MIN	TYP†	MAX	UNITS	NOTES
I_{SS}	Supply Current, V_{SS}		6.0	11.0	mA	Note 1
I_{GG}	Supply Current, V_{GG}		6.0	11.0	mA	
I_{IL}	Input Current, Logic 0			− 1.6	mA	Note 2: V_I = 0.4V
V_{OL}	Output Voltage, Logic 0			0.4	V	I_{OL} = 1.6mA*
V_{OH}	Output Voltage, Logic 1	2.4			V	I_{OH} = −40μA*
f_{STA}	Frequency Stability w/ Volt. Change, RC Mode		± 3.0		%/V	Note 3
	/ Temp. Change, RC Mode		− 0.2		%/°C	
	Crystal Mode		—			Note 4
$t_{e\,e}$	Jitter, Edge-to-Edge Variation		<15		nsec	Temp. & Supply Voltage Constant

†Typical values at V_{SS} = +5V, V_{DD} = 0V, V_{GG} = −12V, and T_A = 25°C

1. Logic inputs at V_{SS}, output open circuited. Each logic input (see Note 2) contributes an additional 1.6 mA (max.) to I_{SS} when at logic 0.
2. Logic Inputs are: Reset Max; Reset 0; Address Inputs; Ext. Input; Ext. Int. Select; and $\overline{Clamp}$.
3. Frequency variations due to power supply changes only.
4. Crystal mode stability is dependent upon crystal.
5. Minimum logic 0 time at clamp input is 50% of oscillator period.

*V_{OH}, V_{OL} apply only to Time Out.

DESCRIPTION OF OPERATION

The MK 5009 P consists basically of a series of counters, selectable via an internal multiplexer. The ÷ 10¹ counter output is used to generate an internal clock signal for the 10^2 through 36×10^6 counter stages, which are fully synchronous with each other.

OSCILLATOR CONTROLS

Operation in the RC oscillator mode is achieved as shown in Figure 1. Frequency, f, is approximately 0.8 RC. The clamp circuit can be used in the RC mode to provide one-shot or accurate start-up operations. When Clamp goes to a logic 0, the internal circuitry is held at a reference level so that upon release of the Clamp (return to logic 1), the oscillator's first cycle will be a full cycle.

The crystal oscillator mode is shown in Figure 2. Values for the resistors are chosen to bias the internal circuitry for optimum performance. The two capacitors are chosen to provide the loading capacitance (C_L) specified for the selected crystal. It is recommended that C1 = C2 = 2 C_L.

RESET/BYPASS CONTROLS

The MK 5009 P provides two different reset conditions. A positive-going pulse of 10 µs or longer on Reset 0 will reset counters to their lowest state, while a positive-going pulse at Reset Max will reset counters to their highest state. The Reset Max control enables the user to set up the counters to provide a falling edge at the next oscillator cycle or negative-going external input, regardless of which divider chain is selected.

In addition, taking one or both Reset Inputs to the most negative voltage, V_{GG}, allows bypassing portions of the divider chain for testing or other purposes (see table on page 1).

EXTERNAL/INTERNAL FREQUENCY SOURCE

When using an external signal source to operate the MK 5009 P, that signal should be applied at the External Input (Pin 3), and the External/Internal Select (Pin 5) should be brought to logic 1.

For operation with an internal signal, the External/Internal Select should be at logic 0.

OSCILLATOR OUTPUT

The oscillator output, provided at Pin 10, is not a true logic output, but may be used to drive a high impedance device such as a junction FET or other MOS circuitry.

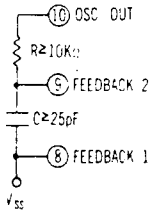


FIG. 1

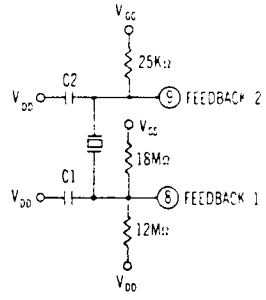
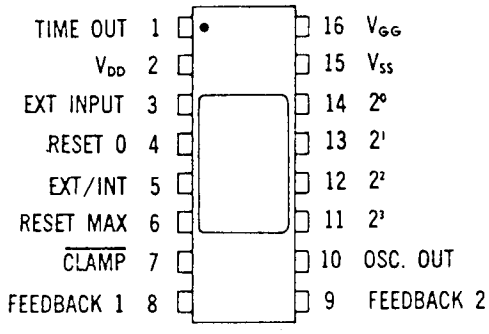
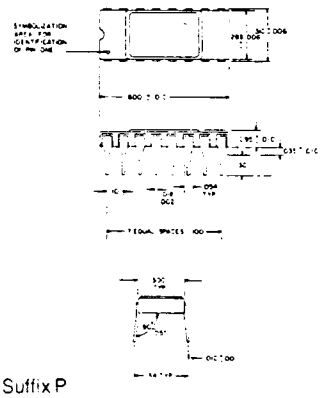


FIG. 2

PIN CONNECTIONS

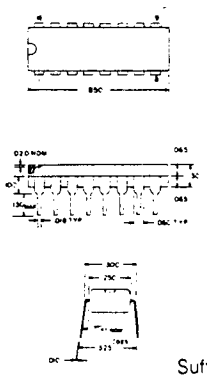


PACKAGE
16-pin ceramic dual-in-line



Suffix P

PACKAGE
16-pin plastic dual-in-line

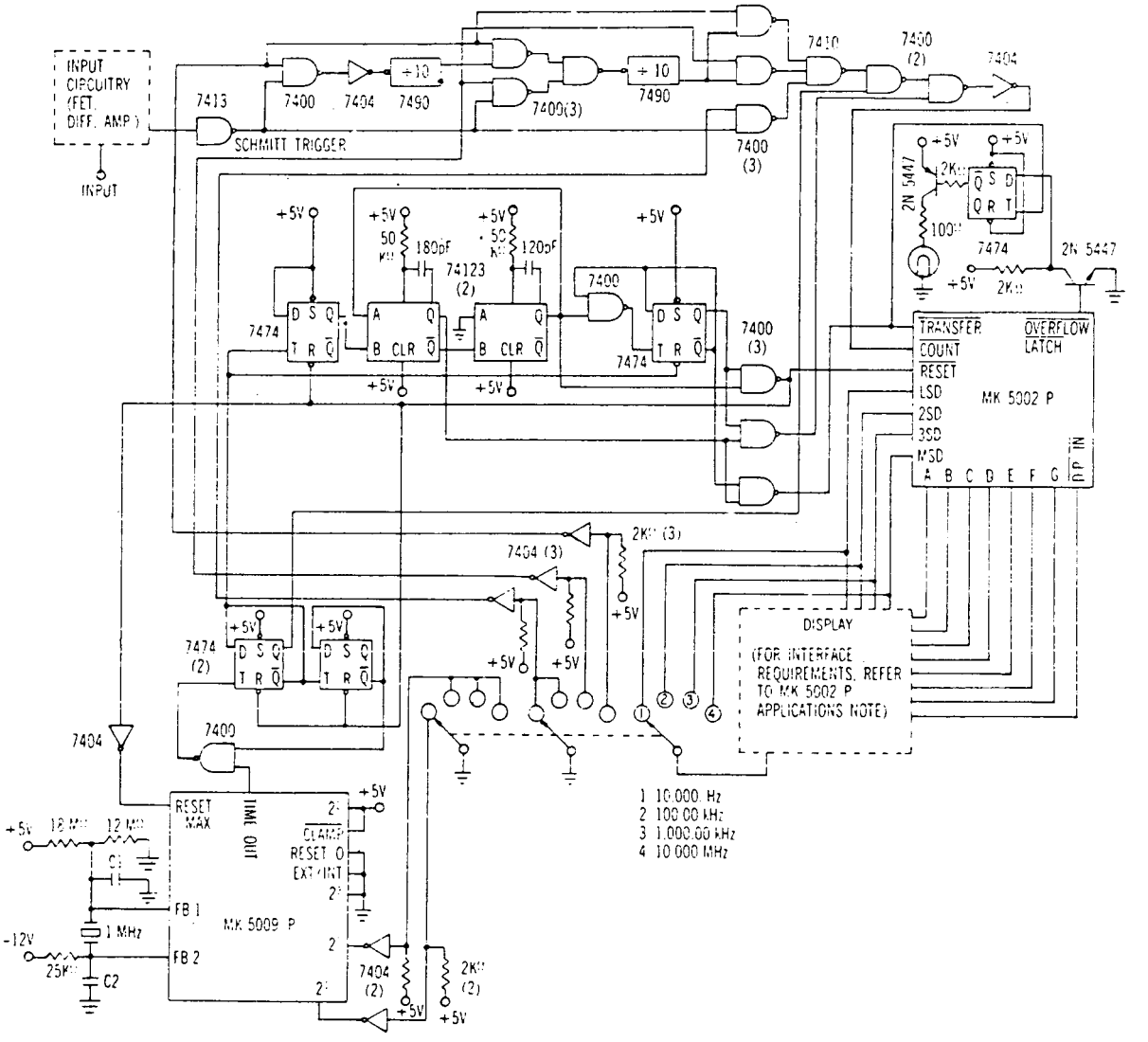


Suffix N

APPLICATION — 10 MHz Frequency Counter

The circuit shown below is a frequency counter capable of counting input rates up to 10 MHz, selected in four ranges. The MK 5009 P provides the time base intervals while the Mostek MK 5002 P counter circuit provides counting, storage, and display functions. Two decades of prescaling using TTL are employed. TTL one-shots provide proper timing for the 5002.

To replace the functions of the MK 5009 P, an active device and Schmitt trigger for the crystal oscillator would be needed, plus six 7490's to achieve the correct time out. Replacing the functions of the MK 5002 would require four 7490's, four 7475's, and four BCD-to-seven-segment decoders.



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HEWLETT hp PACKARD
COMPONENTS

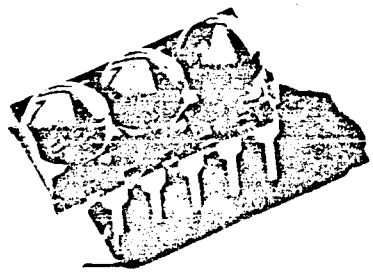
SOLID STATE NUMERIC INDICATOR (7 Segment Monolithic)

5082-7430 SERIES

TENTATIVE DATA OCT. 19

Features

- MOS COMPATIBLE
  - Can be Driven Directly from many MOS Circuits
- LOW POWER
  - Excellent Readability at Only 0.5mW per Segment
- CONSTRUCTED FOR STROBED OPERATION
  - Minimizes Lead Connections
- STANDARD DIP PACKAGE
  - End Stackable
  - Integral Red Contrast Filter
  - Rugged Construction
- CATEGORIZED FOR LUMINOUS INTENSITY
  - Assures Uniformity of Light Output from Unit to Unit within a Single Category

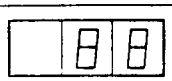


Description

The HP 5082-7430 series displays are .11 inch high, seven segment GaAsP numeric indicators packaged in 2 and 3 digit end-stackable clusters on 200 mil centers. An integral magnification technique increases the luminous intensity, thereby making ultra-low power consumption possible. These clusters have the standard lower right hand decimal points.

Applications include hand-held calculators, portable instruments, digital thermometers, or any other product requiring low power, low cost, minimum space, and long lifetime indicators.

Device Selection Guide

Digits per Cluster	Configuration		Part Number
	Device	Package	
2(right)		(Figure 5)	5082-7432
3		(Figure 5)	5082-7433

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Peak Forward Current per Segment or dp (Duration < 500μs)	I_{PEAK}		50	mA
Average Current per Segment or dp	I_{AVG}		5	mA
Power Dissipation per Digit [1]	P_D		80	mW
Operating Temperature, Ambient	T_A	−40	75	°C
Storage Temperature	T_S	−40	100	°C
Reverse Voltage	V_R		5	V
Solder Temperature 1/16" below seating plane (t ≤ 5 sec.) [2]			230	°C

NOTES: 1. Derate linearly @ 1 mW/°C above 25°C ambient. 2. See Mechanical section for recommended flux removal solvents.

Electrical/Optical Characteristics at T_A=25°C

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Units
Luminous Intensity/Segment or dp [3]	I_v	I_{AVG} = 500μA (I_{PK} = 5mA duty cycle = 10%)	10	40		μcd
Peak Wavelength	λ_{peak}			655		nm
Forward Voltage/Segment or dp	V_F	I_F = 5mA		1.55	2.0	V
Reverse Current/Segment or dp	I_R	V_R = 5V			100	μA
Rise and Fall Time [4]	t_r, t_f			10		ns

NOTES: 3. The digits are categorized for luminous intensity. Intensity categories are designated by a letter located on the back side of the package. 4. Time for a 10%-90% change of light intensity for step change in current.

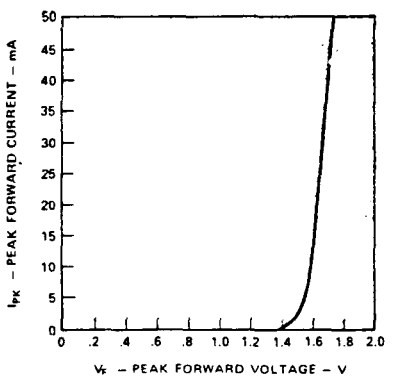


Figure 1. Peak Forward Current vs. Peak Forward Voltage

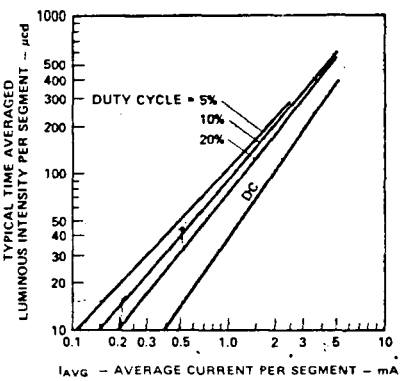


Figure 2. Typical Time Averaged Luminous Intensity per Segment vs. Average Current per Segment

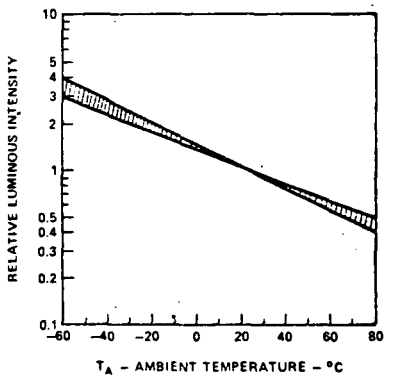


Figure 3. Relative Luminous Intensity vs. Ambient Temperature at Fixed Current Level

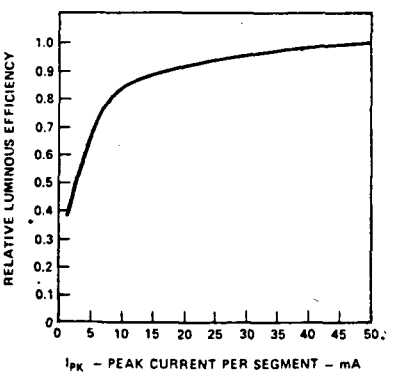


Figure 4. Relative Luminous Efficiency vs. Peak Current per Segment

Package Description

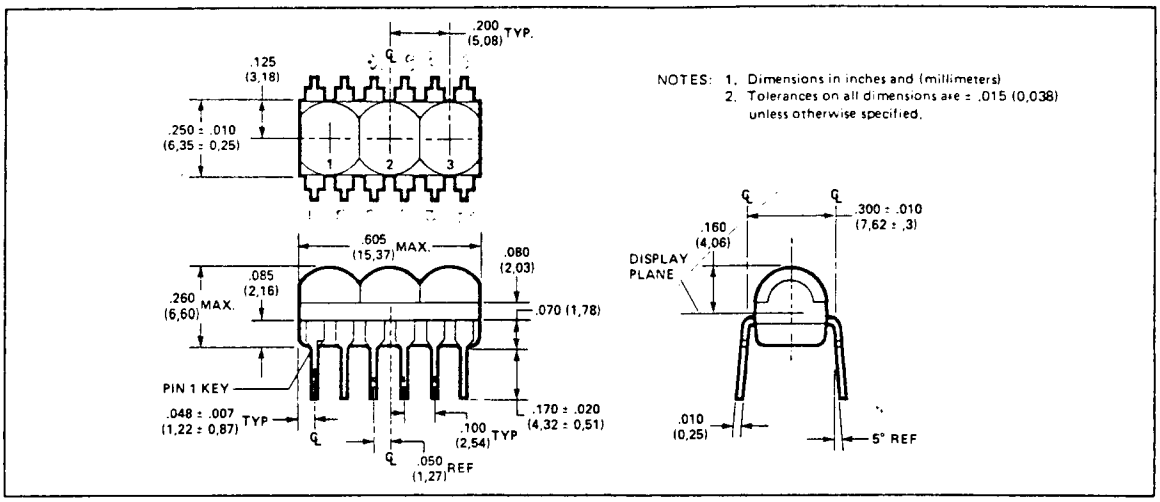


Figure 5.

Magnified Character Font Description

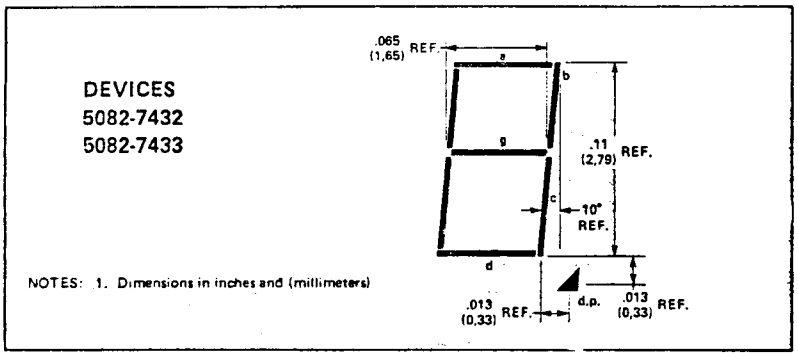


Figure 6.

Device Pin Description

PIN NUMBER	5082-7432 FUNCTION	5082-7433 FUNCTION
1	N/C	CATHODE 1
2	ANODE e	ANODE e
3	ANODE d	ANODE d
4	CATHODE 2	CATHODE 2
5	ANODE c	ANODE c
6	ANODE dp	ANODE dp
7	CATHODE 3	CATHODE 3
8	ANODE b	ANODE b
9	ANODE g	ANODE g
10	ANODE a	ANODE a
11	ANODE f	ANODE f
12	N/C	N/C

Electrical/Optical

The 5082-7430 series devices utilize a monolithic GaAsP chip of 8 common cathode devices for each display digit. The segment anodes of each digit are interconnected, forming an 8 by N line array, where N is the number of characters in the display. Each chip is positioned under an integrally molded lens giving a magnified character height of 0.11 inches. Satisfactory viewing will be realized within an angle of approximately ± 20° from the center-line of the digit.

Character encoding on the 5082-7430 series devices is performed by standard 7 segment decoder/driver circuits. Through the use of strobing techniques only one decoder/driver is required for very long multidigit displays.

A discussion of display circuits and drive techniques appears in Application Note 946.

Mechanical

The 5082-7430 series package is a standard 12 Pin DIP consisting of a plastic encapsulated lead frame with integrally molded lenses. It is designed for plugging into DIP sockets or soldering into PC boards. Alignment problems are simplified due to the clustering of digits in a single package.

To improve display contrast, the plastic encapsulant contains a red dye to reduce the reflected ambient light.

The devices can be soldered for up to 5 seconds at a maximum solder temperature of 230°C (1/16" below the seating plane). The plastic encapsulant used in these displays may be damaged by some solvents commonly used for flux removal. It is recommended that only Freon TE, Freon TE-35, Freon TF, Isopropanol, or soap and water be used for cleaning operations.

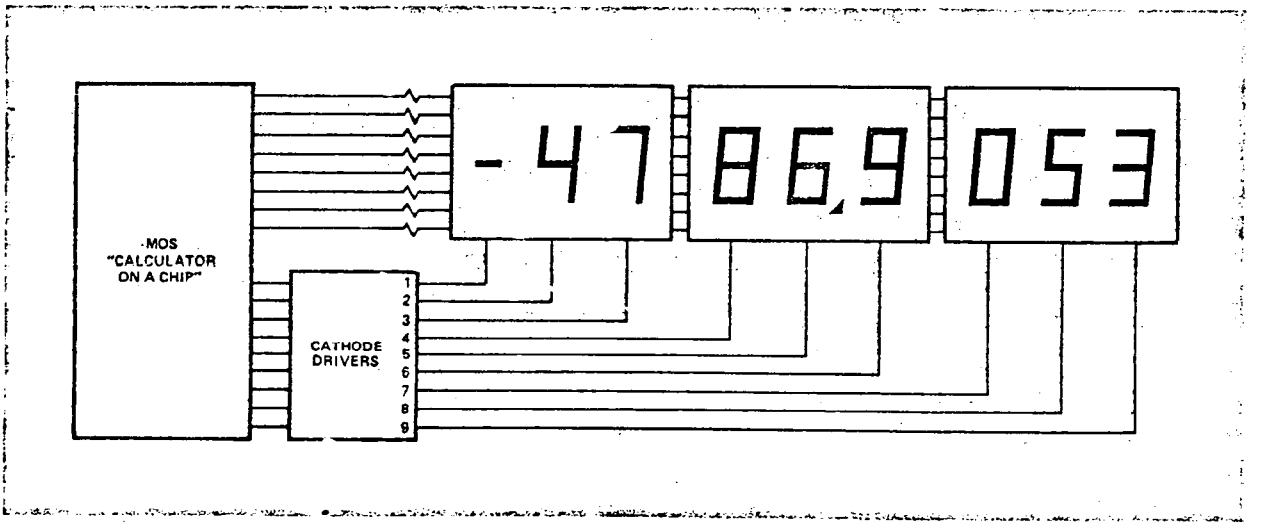


Figure 7. Block Diagram for Calculator Display

SPEED/PACKAGE AVAILABILITY

DESCRIPTION

The 82S83 4-bit binary coded (BCD) adder is a high speed Schottky MSI circuit that has been designed for easy systems usage. This unit produces the BCD sum of two decimal numbers presented in the 8-4-2-1 weighted BCD format. Carry-in and carry-out terms are provided for easy expansion to any number of decades. The 82S83 BCD adder has been designed such that input and output logic levels including the carry are in their true logic form.

Compared to cumbersome hardware implementations previously at the designer's disposal that consist of binary addition followed by decimal correction, the 82S83 BCD adder generates the BCD carry terms internally in the look-ahead mode and does BCD addition directly. For valid BCD numbers (0 through 9) at the A and B inputs the BCD sum is formed at the output. If addition (A+B+CIN) would yield a number greater than 9, a valid BCD number and a carry result.

Input codes above 9 are not defined except for binary to BCD conversion. Binary to BCD conversion is obtained by applying any 4-bit binary number to the AN or BN inputs while the remaining inputs are grounded. For input codes 0 through 9 a BCD number result at the output is usual. If binary inputs 10 through 15 are applied a carry term is generated and the carry output together with the sum out are the BCD equivalent of the binary input. Conversion of binary numbers greater than 16 can be achieved by cascading 82S83's.

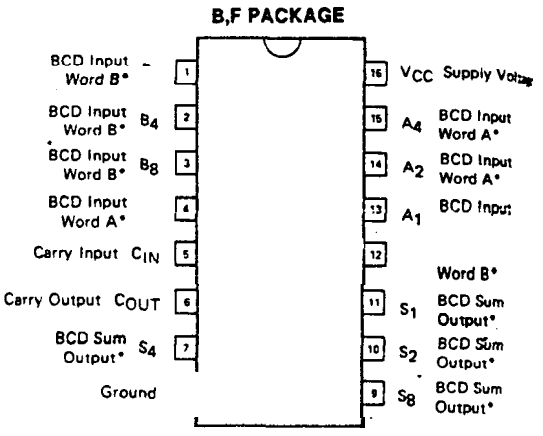
Subtraction can be done with the 82S83 by using 9's complement addition. Rather than implementing a 9's complement circuit with gates or ROM's, the 82S83 BCD arithmetic unit should be used. The 82S83 incorporates the 9's complement feature and performs BCD addition, BCD subtraction, and number comparison.

SWITCHING CHARACTERISTICS

TA = 25°C and VCC = 5.0V

PARAMETER		LIMITS			
		MIN.	TYP.	MAX.	UNITS
Turn-On/Turn-Off Delays					
Any AN, BN, Cin	ton		20	35	ns
to SN	toff		20	35	ns
Any AN, BN, to	ton		33	40	ns
Cout	toff		17	25	ns
Cin to Cout	ton		17	25	ns
	toff		10	15	ns

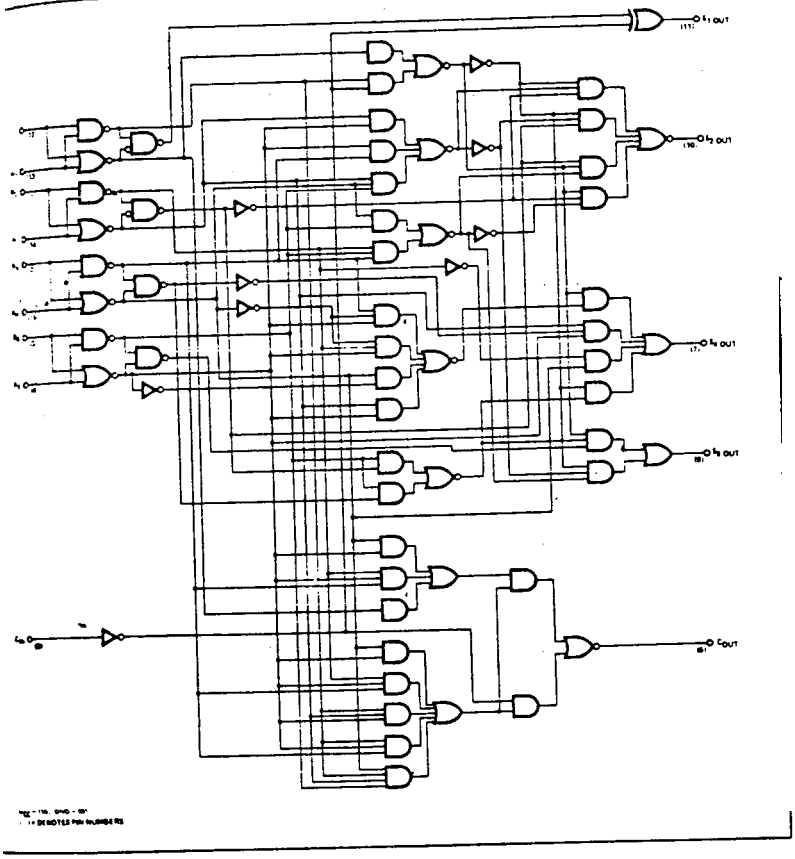
PIN CONFIGURATION



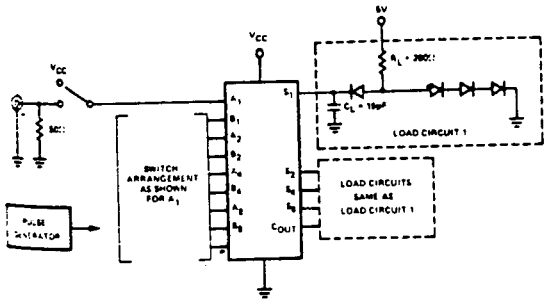
TRUTH TABLE

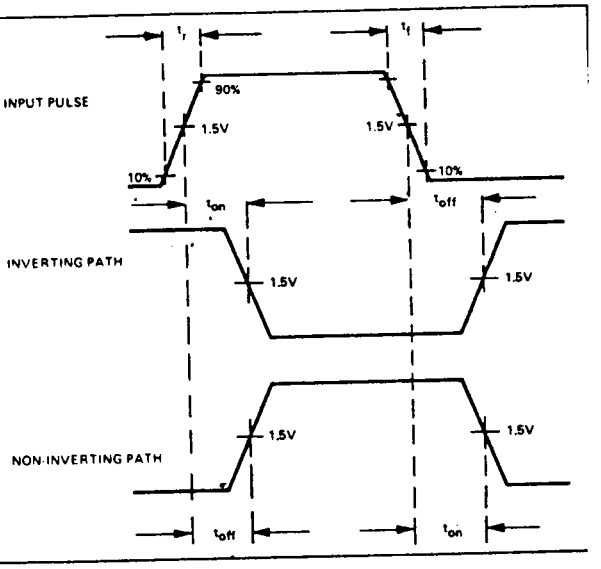
BCD CODE				
Decimal Equivalent	BCD Number 8	4	2	1
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

IC DIAGRAM



C TEST FIGURE AND WAVEFORMS





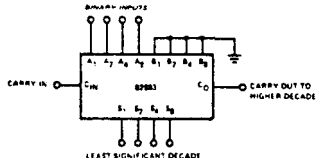
INPUT PULSE:
PRR = 1 MHz
tr = tf = 5 ns
ALL DIODES ARE 1N3064
CL INCLUDES PROBE AND JIG CAPACITANCE

ICAL APPLICATIONS (CONT'D.)

BINARY TO BCD CONVERSION USING A_I INPUTS

PARTIAL TRUTH TABLE FOR AI > 9, BI = 0

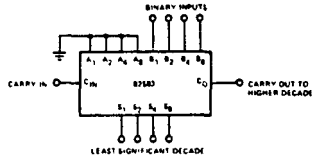
CIN	A1	A2	A4	A8	B1	B2	B4	B3	S1	S2	S4	S8	CO
0	0	1	0	1	0	0	0	0	0	0	0	0	1
0	1	1	0	1	0	0	0	0	1	0	0	0	1
0	0	0	1	1	0	0	0	0	0	1	0	0	1
0	1	0	1	1	0	0	0	0	1	1	0	0	1
0	0	1	1	1	0	0	0	0	0	0	1	0	1
0	1	1	1	1	0	0	0	0	1	0	1	0	1
1	0	1	0	1	0	0	0	0	1	0	0	0	1
1	1	1	0	1	0	0	0	0	0	1	0	0	1
1	0	0	1	1	0	0	0	0	1	1	0	0	1
1	1	0	1	1	0	0	0	0	0	0	1	0	1
1	0	1	1	1	0	0	0	0	1	0	1	0	1
1	1	1	1	1	0	0	0	0	0	1	1	0	1



BINARY TO BCD CONVERSION USING B_I INPUTS

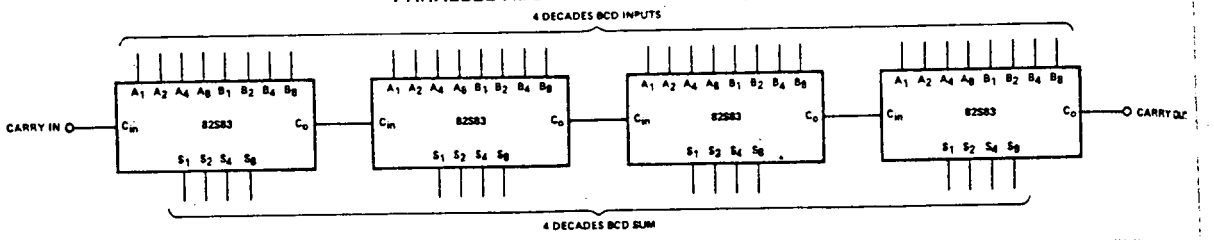
PARTIAL TRUTH TABLE FOR BI > 9, AI = 0

CIN	A1	A2	A4	A8	B1	B2	B4	B8	S1	S2	S4	S8	CO
0	0	0	0	0	0	1	0	1	0	0	0	0	1
0	0	0	0	0	1	1	0	1	1	0	0	0	1
0	0	0	0	0	0	0	1	1	0	1	0	0	1
0	0	0	0	0	1	0	1	1	1	1	0	0	1
0	0	0	0	0	0	1	1	1	1	0	0	1	0
0	0	0	0	0	1	1	1	1	1	0	1	0	1
1	0	0	0	0	0	1	0	1	1	0	0	0	1
1	0	0	0	0	1	1	0	1	0	1	0	0	1
1	0	0	0	0	0	0	1	1	1	1	0	0	1
1	0	0	0	0	1	0	1	1	0	0	1	0	1
1	0	0	0	0	0	1	1	1	1	0	1	0	1
1	0	0	0	0	1	0	0	0	0	1	1	0	1

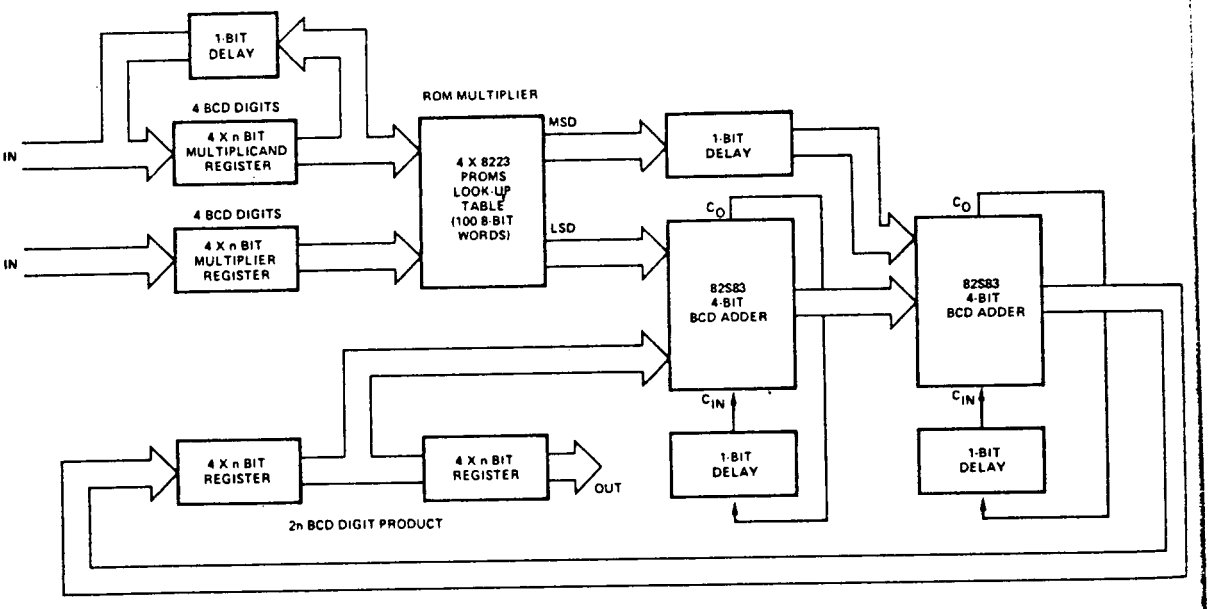


TYPICAL APPLICATIONS

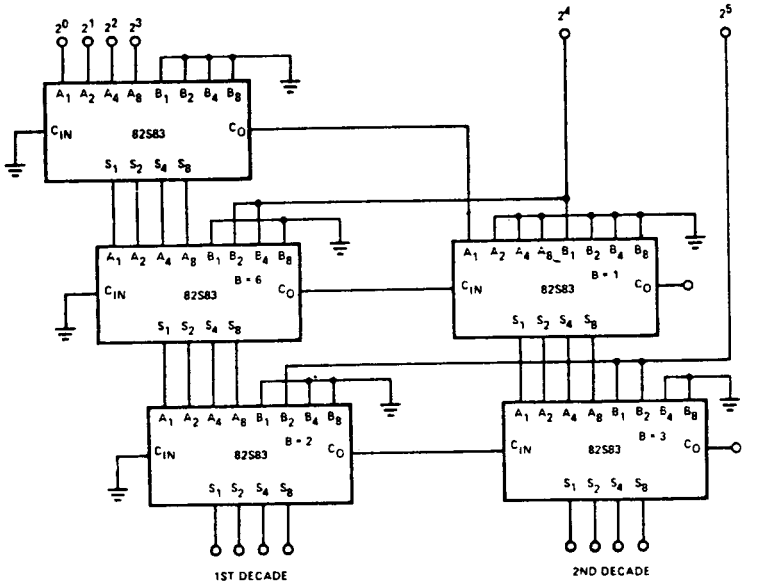
PARALLEL ADDITION OF FOUR DECADES



BIT PARALLEL-WORD SERIAL BCD MULTIPLIER



BINARY TO BCD CONVERSION FOR TWO DECADES



OP-07

ULTRA-LOW OFFSET VOLTAGE OPERATIONAL AMPLIFIER

FEATURES

- Ultra-Low V_{OS} 10μV
- Ultra-Low V_{OS} Drift ..... 0.2μV/°C
- Ultra-Stable vs Time 0.2μV/Month
- Ultra-Low Noise ..... 0.35μV_{p-p}
- No External Components Required
- Replaces Chopper Amps at Lower Cost
- Single-Chip Monolithic Construction
- Large Input Voltage Range ..... ±14.0V
- Wide Supply Voltage Range ..... ±3V to ±18V
- Fits 725, 108A/308A, 741, AD510 Sockets

GENERAL DESCRIPTION

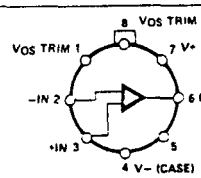
The OP-07 Series represents a breakthrough in monolithic operational amplifier performance — V_{OS} of 10μV, TCV_{OS} of 0.2μV/°C and long-term stability of 0.2μV/month are achieved by a low-noise, chopper-less bipolar input transistor amplifier circuit. Complete elimination of external components for offset nulling, frequency compensation and device protection permits extreme miniaturization and optimization of system Mean-Time-Between-Failure Rates in high-performance aerospace/defense and industrial applications. Excellent device interchangeability provides reduced system assembly time and eliminates field recalibrations.

True differential inputs with wide input voltage range and outstanding common mode rejection provide maximum flexibility and performance in high-noise environments and non-inverting applications. Low bias currents and extremely-high input impedances are maintained over the entire temperature range.

The OP-07 provides unparalleled performance for low noise, high-accuracy amplification of very low-level signals in transducer applications. Devices are available in chip form for use in hybrid circuitry. The OP-07 is a direct replacement for 725, 108A/308A*, and OP-05 amplifiers; 741-types may be directly replaced by removing the 741's nulling potentiometer.

*TO-99 package only. For Matched Dual see OP-207.

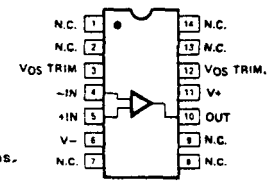
PIN CONNECTIONS & ORDERING INFORMATION

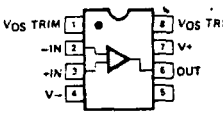


TO-99 (J-Suffix)
ORDER: OP-07AJ OP-07CJ
OP-07J OP-07DJ
OP-07EJ

14-PIN DIP (Y-Suffix)*
ORDER: OP-07AY
OP-07Y
OP-07EY
OP-07CY

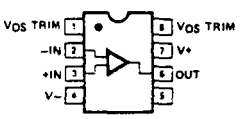
*Not recommended for new designs.





EPOXY B MINI-DIP (P-Suffix)
ORDER: OP-07CP
OP-07EP
OP-07DP

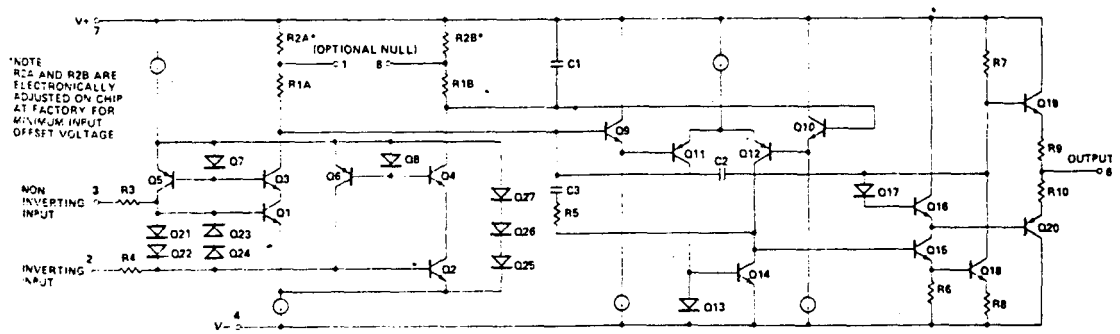
8-PIN DIP (Z-Suffix)
ORDER: OP-07AZ
OP-07Z
OP-07EZ
OP-07CZ



Military Temperature Range Devices with MIL-STD-883 Class B Processing

ORDER: OP07AJ/883 OP07AZ/883 OP07Y/883
OP07AY/883 OP07J/883 OP07Z/883

SIMPLIFIED SCHEMATIC



PINOUTS FOR J, Z AND P PACKAGES.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±22V
Internal Power Dissipation (Note 1) 500mW
Differential Input Voltage ..... ±30V
Input Voltage (Note 2) ..... ±22V
Output Short Circuit Duration ..... Indefinite
Storage Temperature Range ..... −65°C to +150°C
Operating Temperature Range
OP-07A, OP-07 ..... −55 to +125°C
OP-07E, OP-07C, OP-07D ..... 0°C to +70°C
Lead Temperature Range (Soldering, 60 sec.) ..... 300°C

NOTES:
1. Maximum Package Power Dissipation vs. ambient temperature.

Package Type	Maximum Ambient Temperature for Rating	Derate Above Maximum Ambient Temperature
TO-99 (J)	80°C	7.1mW/°C
Dual-in-Line (Y)	100°C	10.0mW/°C
Mini-Dip (P)	36°C	5.6mW/°C
8-Pin Hermetic Dip (Z)	75°C	6.7mW/°C

ELECTRICAL CHARACTERISTICS at V_S = ±15V, T_A = ± 25°C, unless otherwise noted.

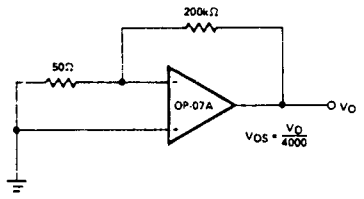
PARAMETER	SYMBOL	CONDITIONS	OP-07A MIN	OP-07A TYP	OP-07A MAX	OP-07 MIN	OP-07 TYP	OP-07 MAX	UNITS
Input Offset Voltage	V_{OS}	(Note 1)	—	10	25	—	30	75	µV
Long Term Input Offset Voltage Stability	$\Delta V_{OS}/Time$	(Note 2)	—	0.2	1.0	—	0.2	1.0	µV/Mo
Input Offset Current	I_{OS}		—	0.3	2.0	—	0.4	2.8	nA
Input Bias Current	I_B		—	±.7	±2.0	—	±1.0	±3.0	nA
Input Noise Voltage	e_{np-p} (Note 3)	0.1Hz to 10Hz	—	0.35	0.6	—	0.35	0.6	μV_{p-p}
Input Noise Voltage Density	e_n (Note 3)	f_o = 10Hz	—	10.3	18.0	—	10.3	18.0	$nV/\sqrt{Hz}$
		f_o = 100Hz	—	10.0	13.0	—	10.0	13.0	
		f_o = 1000Hz	—	9.6	11.0	—	9.6	11.0	
Input Noise Current	i_{np-p} (Note 3)	0.1Hz to 10Hz	—	14	30	—	14	30	pA_{p-p}
Input Noise Current Density	i_n (Note 3)	f_o = 10Hz	—	0.32	0.80	—	0.32	0.80	$pA/\sqrt{Hz}$
		f_o = 100Hz	—	0.14	0.23	—	0.14	0.23	
		f_o = 1000Hz	—	0.12	0.17	—	0.12	0.17	
Input Resistance — Differential Mode	R_{IN}		30	80	—	20	60	—	MΩ
Input Resistance — Common Mode	R_{INCM}		—	200	—	—	200	—	GΩ
Input Voltge Range	IVR		±13.0	±14.0	—	±13.0	±14.0	—	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±13V	110	126	—	110	126	—	dB
Power Supply Rejection Ratio	PSRR	V_S ±3V to ±18V	100	110	—	100	110	—	dB
Large Signal Voltage Gain	A_{VO}	R_L ≥ 2kΩ, V_O = ±10V	300	500	—	200	500	—	V/mV
		R_L ≥ 500Ω, V_O = ±.5V, V_S = ±3V	150	500	—	150	500	—	
Maximum Output Voltage Swing	V_{OM}	R_L ≥ 10kΩ	±12.5	±13.0	—	±12.5	±13.0	—	V
		R_L ≥ 2kΩ	±12.0	±12.8	—	±12.0	±12.8	—	
		R_L ≥ 1kΩ	±10.5	±12.0	—	±10.5	±12.0	—	
Slewing Rate	SR	R_L = ≥2kΩ (Note 3)	0.1	0.2	—	0.1	0.2	—	V/µs
Closed Loop Bandwidth	BW	A_{VCL} = +1.0 (Note 3)	0.4	0.6	—	0.4	0.6	—	MHz
Open Loop Output Resistance	R_O	V_O = 0, I_O = 0	—	60	—	—	60	—	Ω
Power Consumption	P_d	V_S = ±15V	—	75	120	—	75	120	mW
		V_S = ±3V	—	4	6	—	4	6	
Offset Adjustment Range		R_p = 20kΩ	—	±4	—	—	±4	—	mV

NOTES:
1. Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.
2. Long Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5µV — refer to typical performance curve on Page 5. Parameter is not 100% tested: 90% of units meet this specification.
3. Parameter is not 100% tested: 90% of units meet this specification.

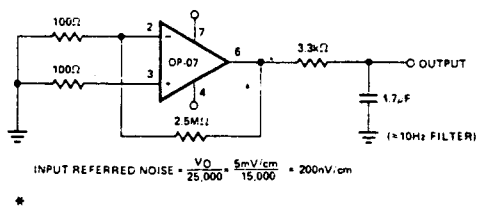
ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-55°C \le T_A \le +125°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-07A MIN	OP-07A TYP	OP-07A MAX	OP-07 MIN	OP-07 TYP	OP-07 MAX	UNITS
Input Offset Voltage	V_{OS}	(Note 1)	—	25	60	—	60	200	μV
Average Input Offset Voltage Drift Without External Trim	TCV_{OS}	(Note 3)	—	0.2	0.6	—	0.3	1.3	μV/°C
With External Trim	TCV_{OSn}	$R_p = 20k\Omega$	—	0.2	0.6	—	0.3	1.3	
Input Offset Current	I_{OS}		—	0.8	4.0	—	1.2	5.6	nA
Average Input Offset Current Drift	TCI_{OS}	(Note 3)	—	5	25	—	8	50	pA/°C
Input Bias Current	I_B		—	±1.0	±4.0	—	±2.0	±6.0	nA
Average Input Bias Current Drift	TCI_B		—	8	25	—	13	50	pA/°C
Input Voltage Range	IVR		±13.0	±13.5	—	±13.0	±13.5	—	V
Common Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	106	123	—	106	123	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	94	106	—	94	106	—	dB
Large Signal Voltage Gain	A_{VO}	$R_L \ge 2k\Omega$, $V_O = \pm 10V$	200	400	—	150	400	—	V/mV
Maximum Output Voltage Swing	V_{OM}	$R_L \ge 2k\Omega$	±12.0	±12.6	—	±12.0	±12.6	—	V

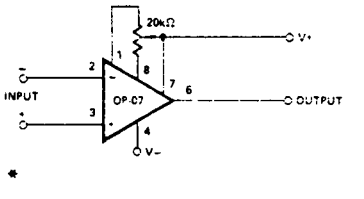
TYPICAL OFFSET VOLTAGE TEST CIRCUIT



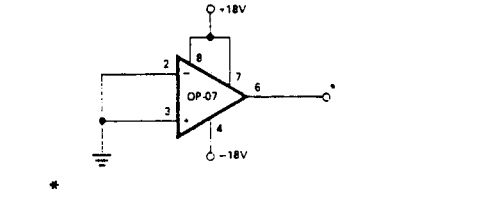
TYPICAL LOW FREQUENCY NOISE TEST CIRCUIT



OPTIONAL OFFSET NULLING CIRCUIT



BURN-IN CIRCUIT



ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

			OP-07E			OP-07C			OP-07D			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	(Note 1)	—	30	75	—	60	150	—	60	150	μV
Long Term V_{OS} Stability	V_{OS}/Time	(Note 2)	—	0.3	1.5	—	0.4	2.0	—	0.5	3.0	μV/Mo
Input Offset Current	I_{OS}		—	0.5	3.8	—	0.8	6.0	—	0.8	6.0	nA
Input Bias Current	I_B		—	±1.2	±4.0	—	±1.8	±7.0	—	±2.0	±12	nA
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz (Note 3)	—	0.35	0.6	—	0.38	0.65	—	0.38	0.65	μV_{p-p}
Input Noise Voltage Density	e_n (Note 3)	$f_o = 10Hz$	—	10.3	18.0	—	10.5	20.0	—	10.5	20.0	$nV/\sqrt{Hz}$
		$f_o = 100Hz$	—	10.0	13.0	—	10.2	13.5	—	10.3	13.5	
		$f_o = 1000Hz$	—	9.6	11.0	—	9.8	11.5	—	9.8	11.5	
Input Noise Current	i_{np-p}	0.1Hz to 10Hz (Note 3)	—	14	30	—	15	35	—	15	35	pA_{p-p}
Input Noise Current Density	i_n (Note 3)	$f_o = 10Hz$	—	0.32	0.80	—	0.35	0.90	—	0.35	0.90	$pA/\sqrt{Hz}$
		$f_o = 100Hz$	—	0.14	0.23	—	0.15	0.27	—	0.15	0.27	
		$f_o = 1000Hz$	—	0.12	0.17	—	0.13	0.18	—	0.13	0.18	
Input Resistance — Differential Mode	R_{IN}		15	50	—	8	33	—	7	31	—	MΩ
Input Resistance — Common Mode	R_{INCM}		—	160	—	—	120	—	—	120	—	GΩ
Input Voltage Range	IVR		±13.0	±14.0	—	±13.0	±14.0	—	±13.0	±14.0	—	V
Common Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	106	123	—	100	120	—	94	110	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	94	107	—	90	104	—	90	104	—	dB
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	200	500	—	120	400	—	120	400	—	V/mV
		$R_L \geq 500\Omega$, $V_O = \pm .5V$	150	500	—	100	400	—	—	—	—	
		$V_S = \pm 3V$	150	500	—	100	400	—	—	—	—	
Maximum Voltage Voltage Swing	V_{OM}	$R_L \geq 10k\Omega$	±12.5	±13.0	—	±12.0	±13.0	—	±12.0	±13.0	—	V
		$R_L \geq 2k\Omega$	±12.0	±12.8	—	±11.5	±12.8	—	±11.5	±12.8	—	V
		$R_L \geq 1k\Omega$	±10.5	±12.0	—	—	±12.0	—	—	—	—	V
Slewing Rate	SR	$R_L \geq 2k\Omega$ (Note 3)	0.1	0.2	—	0.1	0.2	—	0.1	0.2	—	V/μs
Closed Loop Bandwidth	BW	$A_{VCL} = +1.0$ (Note 3)	0.4	0.6	—	0.4	0.6	—	0.4	0.6	—	MHz
Open Loop Output Resistance	R_O	$V_O = 0$, $I_O = 0$	—	60	—	—	60	—	—	60	—	Ω
Power Consumption	P_d	$V_S = \pm 15V$	—	75	120	—	80	150	—	80	150	mW
		$V_S = \pm 3V$	—	4	6	—	4	8	—	4	8	
Offset Adjustment Range		$R_p = 20k\Omega$	—	±4	—	—	±4	—	—	±4	—	mV

NOTES:

1. Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.
2. Long Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5μV — refer to typical performance curve on Page 5. Parameter is not 100% tested; 90% of units meet this specification.
3. Parameter is not 100% tested; 90% of units meet this specification.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $0°C \le T_A \le +70°C$, unless otherwise noted.

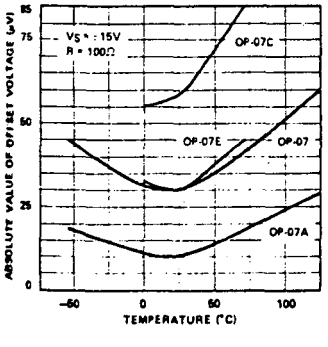
PARAMETER	SYMBOL	CONDITIONS	OP-07E MIN	OP-07E TYP	OP-07E MAX	OP-07C MIN	OP-07C TYP	OP-07C MAX	OP-07D MIN	OP-07D TYP	OP-07D MAX	UNITS
Input Offset Voltage	V_{OS}	(Note 1)	—	45	130	—	85	250	—	85	250	µV
Average Input Offset Voltage Drift Without External Trim	TCV_{OS}		—	0.3	1.3	—	0.5 (Note 3)	1.8	—	0.7 (Note 3)	2.5	µV/°C
With External Trim	TCV_{OSn}	$R_p = 20k\Omega$	—	0.3	1.3	—	0.4 (Note 3)	1.6	—	0.7 (Note 3)	2.5	µV/°C
Input Offset Current	I_{OS}		—	0.9	5.3	—	1.6	8.0	—	1.6	8.0	nA
Average Input Offset Current Drift	TCI_{OS}	(Note 3)	—	8	35	—	12	50	—	12	50	pA/°C
Input Bias Current	I_B		—	±1.5	±5.5	—	±2.2	±9.0	—	±3.0	±14	nA
Average Input Bias Current Drift	TCI_B	(Note 3)	—	13	35	—	18	50	—	18	50	pA/°C
Input Voltage Range	IVR		±13.0	±13.5	—	±13.0	±13.5	—	±13.0	±13.5	—	V
Common Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	103	123	—	97	120	—	94	106	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	90	104	—	86	100	—	86	100	—	dB
Large Signal Voltage Gain	A_{VO}	$R_L \ge 2k\Omega$, $V_O = \pm 10V$	180	450	—	100	400	—	100	400	—	V/mV
Maximum Output Voltage Swing	V_{OM}	$R_L \ge 2k\Omega$	±12.0	±12.6	—	±11.0	±12.6	—	±11.0	±12.6	—	V

NOTES:

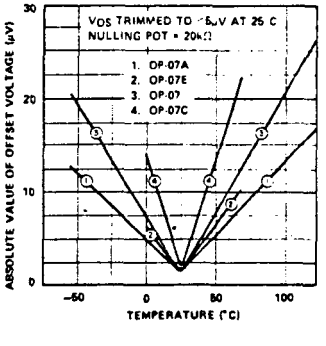
1. Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.
2. *Long Term Input Offset Voltage Stability* refers to the averaged trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5µV — refer to typical performance curve on Page 5. Parameter is not 100% tested; 90% of units meet this specification.
3. Parameter is not 100% tested; 90% of units meet this specification.

TYPICAL PERFORMANCE CURVES

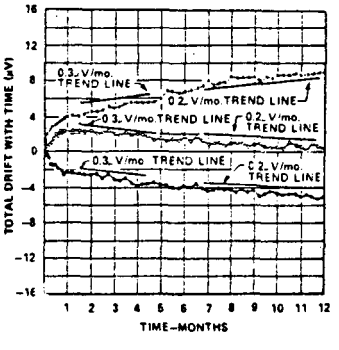
UNTRIMMED OFFSET VOLTAGE vs TEMPERATURE



TRIMMED OFFSET VOLTAGE vs TEMPERATURE

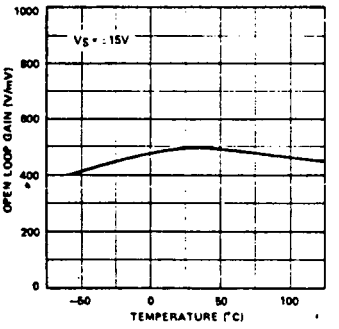


OFFSET VOLTAGE STABILITY vs TIME

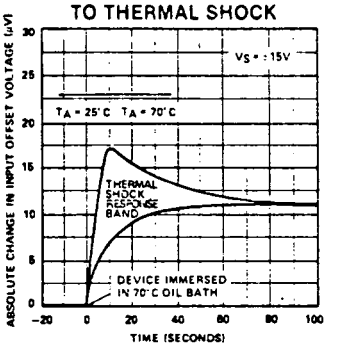


TYPICAL PERFORMANCE CURVES

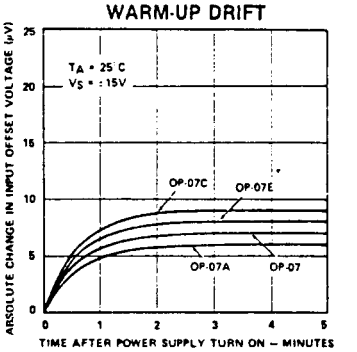
OPEN LOOP GAIN vs TEMPERATURE



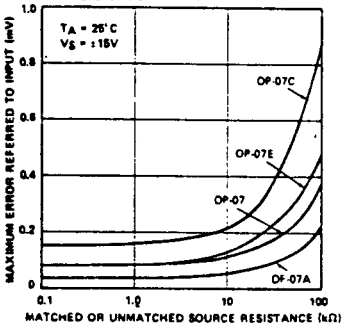
OFFSET VOLTAGE CHANGE DUE TO THERMAL SHOCK



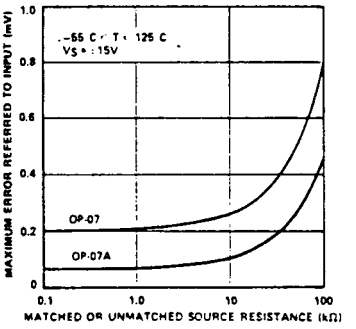
WARM-UP DRIFT



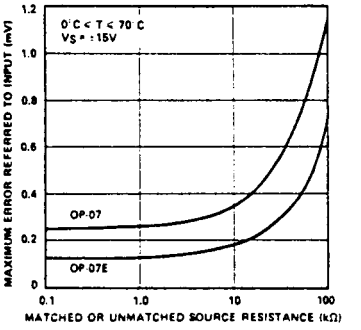
MAXIMUM ERROR vs SOURCE RESISTANCE



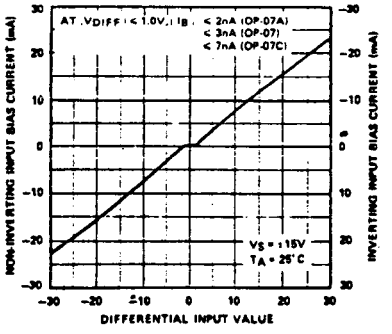
MAXIMUM ERROR vs SOURCE RESISTANCE



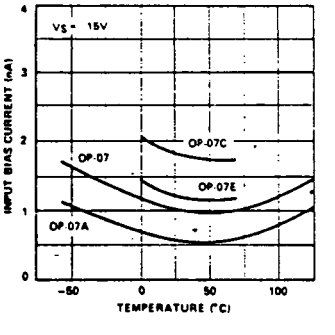
MAXIMUM ERROR vs SOURCE RESISTANCE



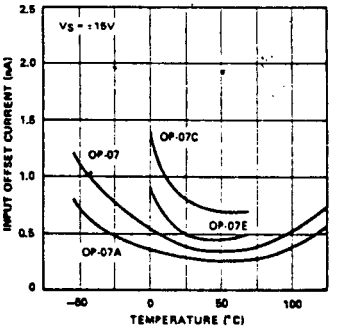
INPUT BIAS CURRENT vs DIFFERENTIAL INPUT VOLTAGE



INPUT BIAS CURRENT vs TEMPERATURE

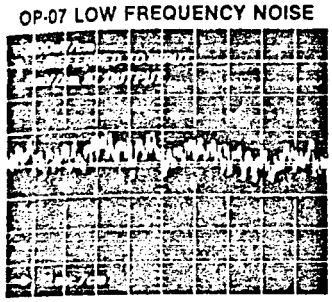


INPUT OFFSET CURRENT vs TEMPERATURE



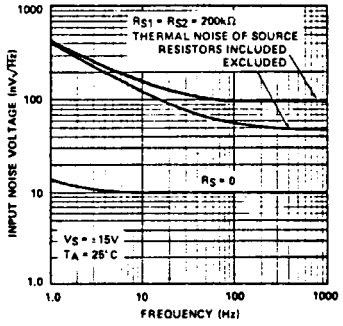
TYPICAL PERFORMANCE CURVES

OP-07 LOW FREQUENCY NOISE

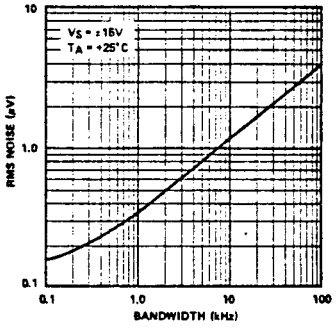


(SEE NOISE TEST CIRCUIT)

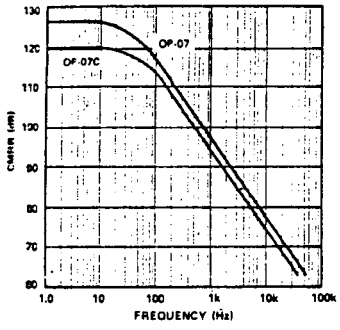
TOTAL INPUT NOISE VOLTAGE vs FREQUENCY



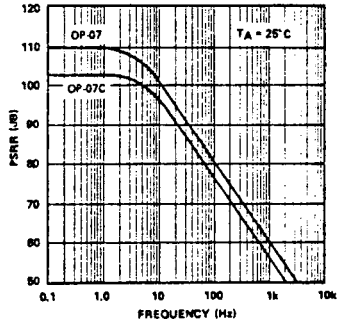
INPUT WIDEBAND NOISE vs BANDWIDTH (0.1Hz TO FREQUENCY INDICATED)



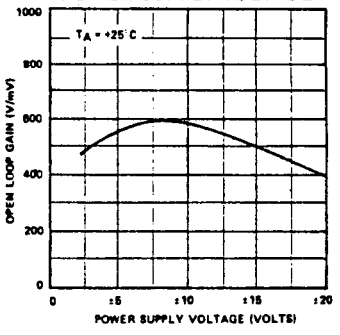
CMRR vs FREQUENCY



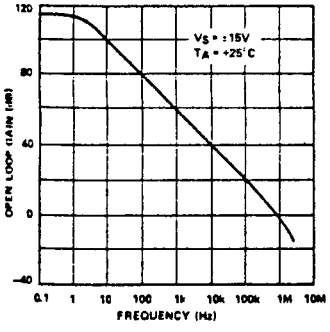
PSRR vs FREQUENCY



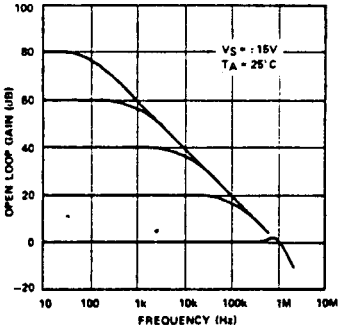
OPEN LOOP GAIN vs POWER SUPPLY VOLTAGE



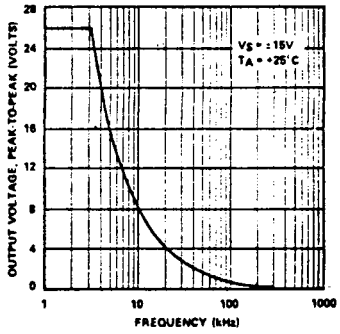
OPEN LOOP FREQUENCY RESPONSE



CLOSED LOOP RESPONSE FOR VARIOUS GAIN CONFIGURATIONS

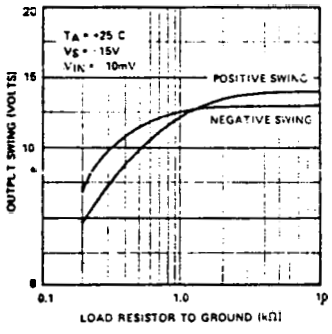


MAXIMUM UNDISTORTED OUTPUT vs FREQUENCY

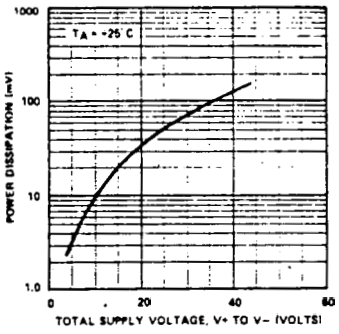


TYPICAL PERFORMANCE CURVES

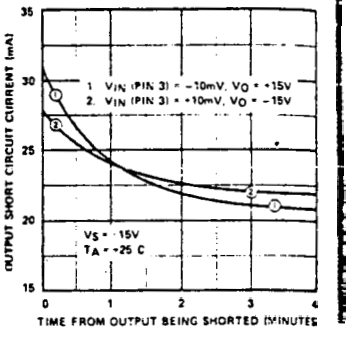
OUTPUT VOLTAGE vs LOAD RESISTANCE



POWER CONSUMPTION vs POWER SUPPLY

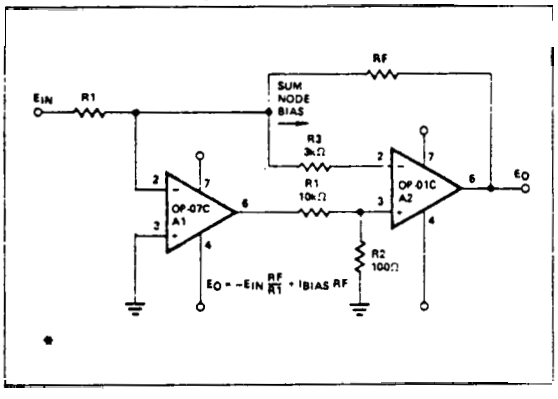


OUTPUT SHORT-CIRCUIT CURRENT vs TIME

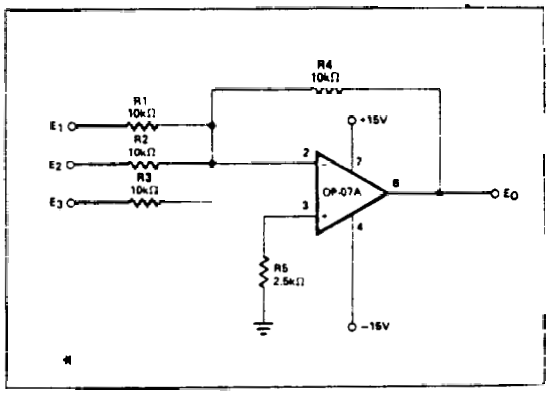


TYPICAL APPLICATIONS

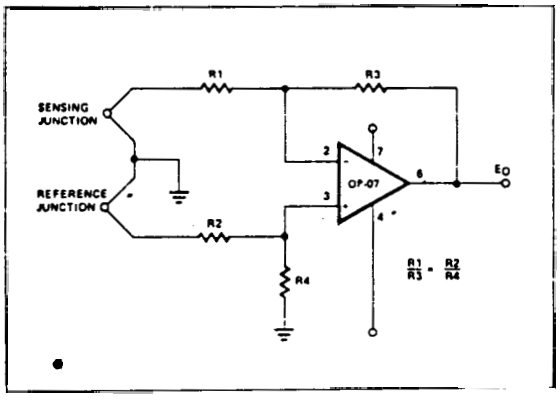
HIGH SPEED, LOW V_{OS} COMPOSITE AMPLIFIER



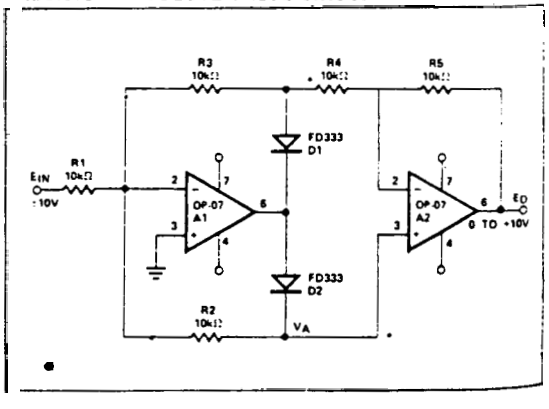
ADJUSTMENT-FREE PRECISION SUMMING AMPLIFIER



HIGH STABILITY THERMOCOUPLE AMPLIFIER



PRECISION ABSOLUTE VALUE CIRCUIT

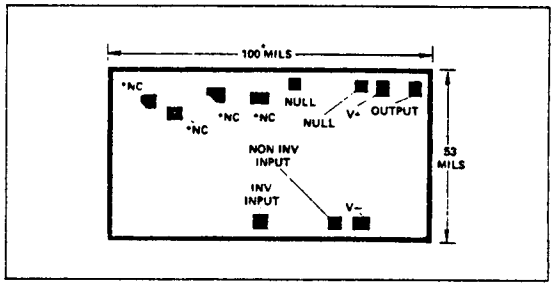


APPLICATIONS INFORMATION

OP-07 Series units may be fitted directly to 725, 108A/308A* and OP-05 sockets with or without removal of external compensation or nulling components. Additionally, OP-07 may be fitted to unnulled 741-type sockets; however if conventional 741 nulling circuitry is in use, it should be modified or removed to enable proper OP-07 operation. OP-07 offset voltage may be nulled to zero (or other desired setting) through use of a potentiometer (see diagram).

The OP-07 provides stable operation with load capacitance up to 500pF and ±10V swings; larger capacitances should be decoupled with 50Ω decoupling resistor. The designer is cautioned that stray thermoelectric voltages generated by dissimilar metals at the contracts to the input terminals can prevent realization of the drift performance indicated. Best operation will be obtained when both input contacts are maintained at the same temperature, preferably close to the temperature of the device's package.

DICE DIMENSIONS



PHOTOMULTIPLIER POWER SUPPLY TYPE PMSB 2-025-1

SPECIFICATION

OUTPUT:

Voltage:	300V DC to 2000V DC variable with input voltage.
Load:	80M ohms Min.
Ripple:	Less than 3V p/p at 1800V output and 180M load
Capacity:	Less than .002 mfd

Momentary Short Circuit Protected
Output isolated 2500V to input ground

INPUT:

Voltage:
(a) Approx. 3V to10V DC for required output voltage.
(b) With fixed output load 180M ohms input voltage shall be less than 8V and input current less than 12 mA for 1800V output.
(c) Reverse polarity protected

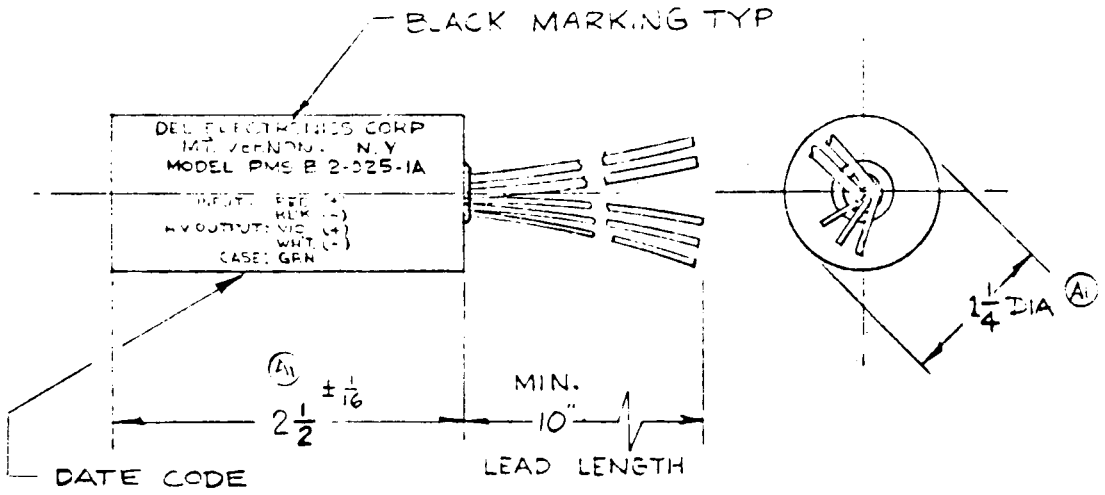
ENVIRONMENTAL:

Operating temperature -10°C to 40°C
Temperature coefficient less than +.02%/°C

CONFIGURATION:

As Drawing A10740 Sheet 1

APPLICATION		REVISIONS			
NEXT ASS'Y	USED ON	SYM	DESCRIPTION	DATE	APPROVAL
		A	1) 2/2 WAS 2/4 ; 1/4 WAS 1" DIA 2) MODEL NO WAS PMSB 2-025-1	ECN 9826 10-15-73	10/15/73
		B	REPLACED S/N MARKING WITH DATE CODE	ECN 9827	12/20/74
		C	REVISED PER E.C.N. 1329	APR 25-75	4/24/75



LEAD DESIGNATIONS

INPUT : RED (+)
: BLACK (−)

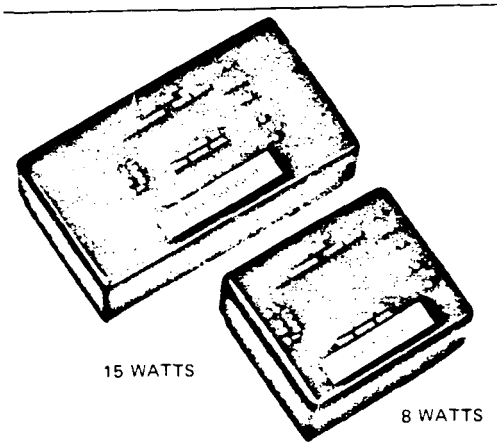
H.V. OUTPUT : VIOLET (+)
WHITE (−)

CASE : GREEN

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES FRACTIONS DECIMALS ANGLES ± 1/32 ONE PL ± .020 ± 1° TWO PL ± .010 THREE PL ± .005 MATERIAL FINISH HOT TIN DIP	DRAWN BY EGC DATE 6-14-72 CHECKED BY DATE 6-14-72 APPROVED BY MFG DATE APPROVED BY ENG DATE 6/22/72	SPECIFICATION CONTROL DRAWING PHOTOMULTIPLIER PMS B 2-025-1A A2	DEL ELECTRONICS CORP. MOUNT VERNON, NEW YORK SCALE UNIT WT DWG SIZE A 10740 C DRAWING NUMBER SYM SHEET 1 OF 2

Reproduced with permission from Del Electronics Corporation, Mt. Vernon, NY 10550.

15 Watts of Regulated Power (6.5V - 40VDC) INPUT
High efficiency ±15V, +5V TRIPLE OUTPUT
From a Single Module DC/DC CONVERTER
That Accepts an Input From 6.5V to 40VDC POWER SUPPLY *Industrial WC Series*



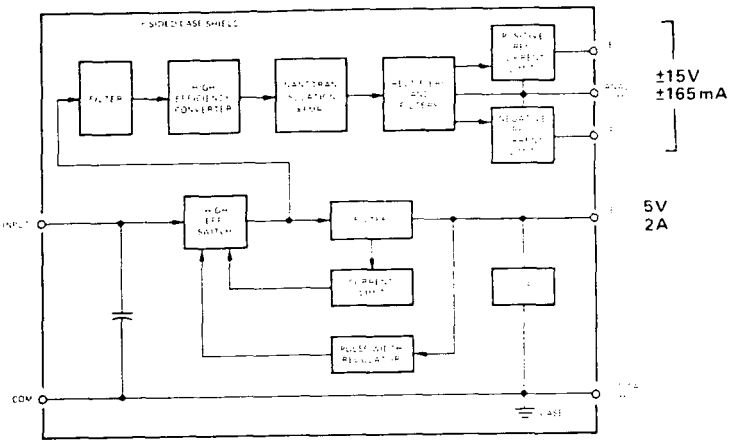


Figure 1. Block Diagram

The Stevens-Arnold Wide Range Input Triple Output DC to DC Converter advances the art by joining two well accepted power processing concepts, packaged in a single module for PCB mounting.

The Input voltage is applied directly to a step-down Switching Regulator. This converts the 6.5V to 40 volt DC Input to a Well Regulated (0.5% line, 0.2% load) Low Noise (40 mV p-p) 5 volts DC Output. This Output is *not* Isolated from the Input voltage since they must share common negative returns.

Within the module the 5 volts is additionally filtered and used to power a Fully Isolated DC to DC Converter of the Low Noise, High Efficiency design employed in our popular Series A Iso-Pak Converters. This delivers an extremely Well Regulated (0.01% typical) ±15 volts DC (or ±12) completely Isolated from the Input and the 5 volt Output.

The result is a Single Module which can operate with virtually constant power Efficiency (68 to 73%) over and anywhere within the entire Input voltage range of 6.5V to 40 volts DC. In addition, the High Efficiency produces a very Low Operating Case Temperature rise of 20 °C thus improving the reliability of the module.

Operating Considerations

(CL) Capacitive Load Limits The 5VDC digital Output (sw. reg.) can be damaged or even destroyed if the Regulator sees a true effective Capacitive load greater than 100 μF.

(R R in) Reflected Input Ripple Noise Current Switching Regulators normally exhibit Input Current Pulses equal in magnitude to the Load Current. We have prepared an Application Note "Filtering Switching Regulators" which discusses a number of filtering techniques. An accessory Input Filter module, to be inserted between the Input source and the power Module, is available.

Fault Mode When the 5VDC Single Output is short circuited the Dual Output will also shut down.

Source Impedance The WC Series should be powered from a Source having a sufficiently Low Impedance to hold the voltage at the Input Terminals below 1 Volt p-p at 10KHz or above.

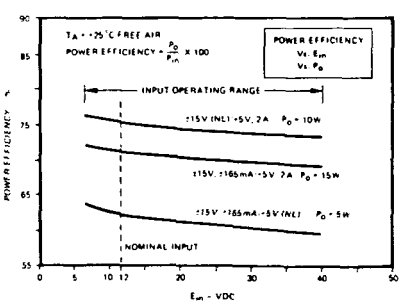


Figure 2. Typical Performance Curves

FEATURES

ONE MODEL for any DC Input Source from from 6.5V to 40VDC

LOW COST
- 15 watt output $114.00 (1-9)
- 8 watt output $99.00 (1-9)

SHORT CIRCUIT PROTECTION AND O.V.P. (5V)

HIGH EFFICIENCY 70%

LOW SURFACE TEMPERATURE RISE
- FL Case Temp. Rise at 12V Nominal Input: +20 °C

ISOLATION
- Input to Dual Output: 1 X 10^9 ohms 500VDC min.
- Input to Single Output: None

EMI/RFI SHIELDING
- Transformer is Double Shielded
- Case is shielded 6 sides (continous)

LOW WIDEBAND NOISE (BW = 20 MHz)
1 mV true RMS – 40 mV p-p

APPLICATIONS

U.P.S. (UNINTERRUPTABLE POWER SUPPLIES)
- Increases "Backup Power" operating time significantly
- High Efficiency: 70%

PORTABLE OR MOBILE SYSTEMS AND INSTRUMENTS
- Extends the voltage-usable range of Low Cost dry cells
- Extends the Voltage-usable range of 12 VDC Rechargeable cells and reduces the Charge Duty Cycle

GENERAL
- Provides 0.1% Regulation from a 6.5V to 40VDC Battery Input
- Provides P.C. Board point-of-load Regulation from an Unregulated main system Supply

SPECIFICATIONS ①

INPUT	
Voltage	12.0 Volts DC
Range	6.5 to 40 Volts DC
Grounding	Minus Input to Case
SINGLE OUTPUT	
Voltage	+5 Volts DC
Setting Accuracy	±1% Max, at FL
Maximum Current (8 Watt Model)	1.0 Amperes
(15 Watt Model)	2.0 Amperes
Ripple and Noise ②	5 mV RMS, 40 mV p-p (5Hz – 20MHz)
Line Regulation (Full Range)	±0.5% Max.
Load Regulation	±0.2% Max.
Temperature Coefficient	±0.02%/°C Max.
Short Circuit Protection ④	Output to Common
Over Voltage Protection	Standard: +6.8 VDC
Voltage Stability	±0.05%/24 Hours
Switching Frequency	14kHz to 40 kHz
Isolation	None: Output Common to minus Input
DUAL OUTPUT (±15 VDC)	
Voltage	±15 Volts DC (Tracking)
Setting Accuracy (+15 V)	±1% Max. @ FL
Balance (-15V)	±1% Max.
Maximum Current (8 Watt Model)	±100 mA
(15 Watt Model)	±165 mA
Ripple and Noise (Either Output) ②	1 mV RMS, 40 mV p-p (5Hz – 20MHz)
Line Regulation (Either Output)	±0.1% Max.
Load Regulation	±0.1% Max.
Temperature Coefficient (Either Output)	±0.01%/°C Max.
Short Circuit Protection	*Either Output to Common*
Voltage Stability	+0.05%/24 Hours
Switching Frequency	>20 kHz
COMMON SPECIFICATIONS	
Cooling	Convection
Derating	None Required
Temperature Rise on Case (8 Watt Model)	+25°C at FL at 12V Input
(15 Watt Model)	+20°C at FL at 12V Input
Operating Temperature Range	0 [redacted]°C to +71°C Ambient
Storage Temperature Range	-55°C to +125°C
Efficiency	See Table
Isolation	$>10^9$ Ohms at 500 VDC Between Input and Dual Output. No Isolation from Input to Single Output
EMI/RFI Shielding	Unit Fully Metallically Enclosed (6 sides), Transformer Double Shielded

NOTE: UNLESS OTHERWISE SPECIFIED

① All specifications are typical @ +25°C and 12 VDC nominal Input
② AN-1 "DC/DC Converter Noise Measurements" Dan Sheehan
③ (RRin) Reflected Input Ripple Current: See AN-5: "Filtering Switching Regulators"
④ 5VDC Output Fault Mode will also shutdown ±15V Output
⑤ All Specifications and Prices are subject to change without notice

	EFFICIENCY		NOMINAL I_{in} (Avg)	
INPUT VOLTAGE	8 WATT MODEL	15 WATT MODEL	8 WATT MODEL	15 WATT MODEL
7.0 VDC	67%	72%	1.7 A	2.98 A
12.0 VDC	65%	71%	1.02 A	1.76 A
24.0 VDC	64%	70%	.52 A	0.89 A
28.0 VDC	63%	69%	0.45 A	0.78 A
40.0 VDC	62%	68%	0.32 A	0.55 A

MODELS

All models have Triple Outputs consisting of 1 Dual Output (either ±15 V or ±12 V) plus 1 Single Output. Other combinations are available on Special Order. The Single Output is always 5 volts, 2 Amp. in the U Package and 1 Amp. in the X Package.

TYPICAL ORDERING SPECIFICATION
WC (7-40) T15/165 U

PRICES

Spec Series	Input Voltage Range	Number of Outputs	Dual Output Voltage	Dual Output Current (mA)	Pkg	Price (1-9)
WC	(7-40)	T	15	165	U	$114.00
WC	(7-40)	T	12	165	U	114.00
WC	(7-40)	T	15	100	X	99.00
WC	(7-40)	T	12	100	X	99.00

INDUSTRIAL ISO-PAK™ X PACKAGE
(X2 WITH TABS)

TOLERANCE .XX ±0.020" .XXX ±0.005"
(Dimensions in parentheses are in millimeters)

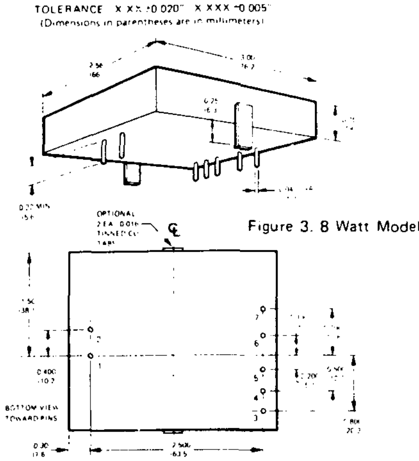


Figure 3. 8 Watt Model

INDUSTRIAL ISO-PAK™ U PACKAGE
(U2 WITH TABS)

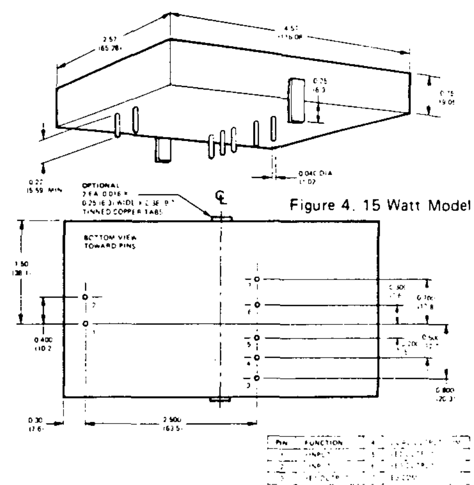


Figure 4. 15 Watt Model

Pins 0.040" diameter gold plated hardened brass
Header Non conducting seating surface Reinforced G10 epoxy laminate
Weight X Package 12 oz max 340 grams max
U Package 24 oz max 680 grams max
Optional Tabs Order X2 case or U2 case $2.00 (1-9)
Mating Socket Order MS X $4.00 net any quantity
Individual 0.040" Socket for 1/16" PC bd Order 1MS 040
Price $0.25 ea. net any quantity

WARRANTY We warrant our products and parts to be free of defects of materials and workmanship for one year from the date of shipment. Our liability under this warranty is limited to exchanging, repairing or issuing credit f.o.b. our factory, at our option, for any products or parts justifiably returned by the customer. We assume no responsibility for consequential damages of any nature. ALL OTHER WARRANTIES, EXPRESSED OR IMPLIED, INCLUDING WARRANTIES FOR FITNESS FOR ANY PARTICULAR PURPOSE AND MERCHANTABILITY, ARE EXCLUDED.

STEVENS INCORPORATED ARNOLD
The Super Isolation People
7 Elkins Street, South Bo· Mass. 02127
TEL: 617-26
Catalog No. SF-613 Cable Address Stearco
Printed in U.S.A.

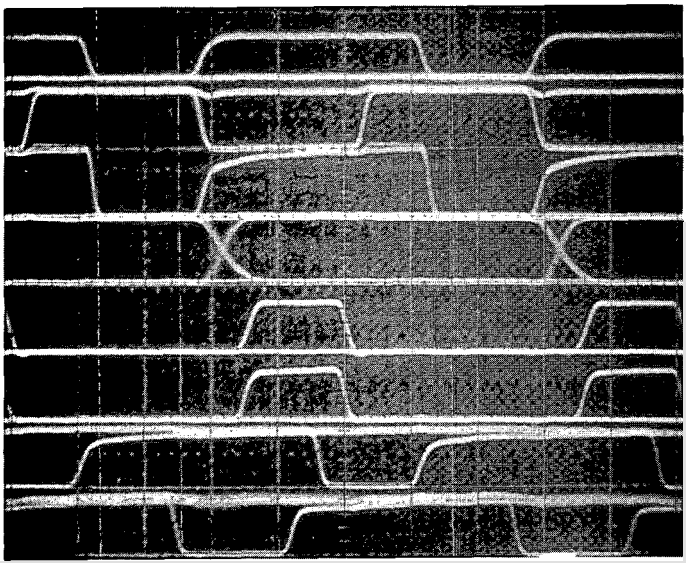
APPENDIX E

SYSTEM-TIMING ILLUSTRATIONS

The illustrations in this appendix show the data and clock-timing relationships in the HEC-100 (HLNCC) in both real-time and idealized form. Figures E-1 and -2 show overall data timing; Fig. E-3 shows coincidence gate timing; Figs. E-4, -5, and -6 illustrate events in the coincidence summation circuitry with varying inputs; and Fig. E-7 illustrates clock-timing relationships. Figures E-1, -2, and -3 are real-time photographs, whereas Figs. E-4 through -7 are idealized figures.

Figures E-1 and -2 are photographs obtained with a Tektronix 475 oscilloscope, with a 20-MHz bandwidth set, and a C-30 oscilloscope camera. Each figure's horizontal scale is 100 ns/div. The top trace in both photos was the synchronization (triggering) signal; the signal is present at test point TA2 whenever there is a signal present at the shift-register input. In this case, the input was driven at a rate greater than 128 kHz by the Los Alamos RP-501 random-pulse generator. The TAx and TBx designators at the immediate right of each photo refer to the test points found at the top of the shift-register board; each designator is followed by a signal label and, parenthetically, the voltage amplitude of the signal. The two photos are multiple exposures, with triggering as above, and vertical offsets from trace to trace, with each trace attenuated, as necessary, to produce a 1-graticule-division (vertical) transition for the logic levels. The test points and associated subcircuits (source and destination components) are schematically represented on Los Alamos Dwgs. D200734-1 and -2.

Figure E-3 is a photograph made with the same equipment as was used for Figs. E-1 and -2, including the signal source. The figure's horizontal scale is 50 ns/div. The vertical scale is 2 V/div. The oscilloscope trigger was the top trace (R+A strobe, TB5). The bottom trace reflects logic transitions in the R+A "1" bit board component location 3C, pin 11 (82S83 BCD adder) resulting from the interaction of the R+A strobe, latch, and the UP/DOWN counter. Horizontal sweep rate was 50 ns/div. The photograph was originally taken to confirm that the circuitry met certain design requirements; namely, that latching, up-count, and down-count could all be done within one clock cycle and still meet component setup times conservatively.



TA2 SYNC (5 V)

TB1 ϕ 1 (12 V)

TB3 DELAY DATA IN (5 V)

TB4 DELAY DATA OUT (5 V)

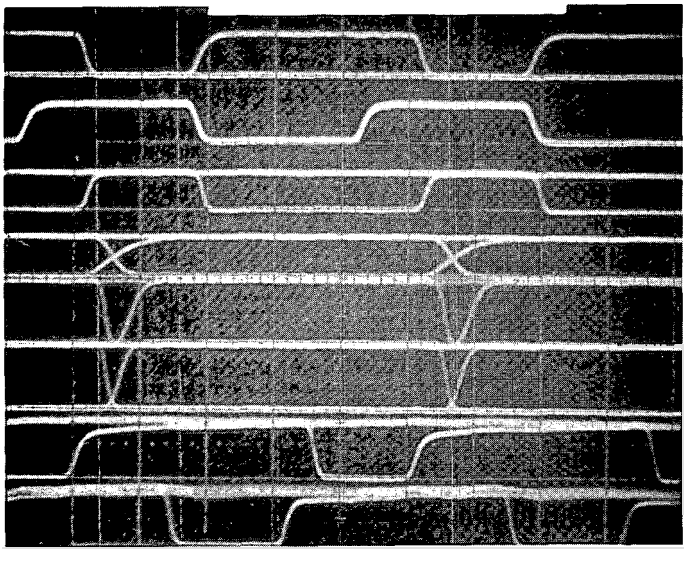
TB5 R+A (5 V)

TB7 A (5 V)

TB2 UP (5 V)

TA7 DOWN (5 V)

Fig. E-1. Data timing No. 1.



TA2 SYNC (5 V)

TA3 SRCK (12 V)

TA4 PREDELAY IN (12 V)

TA1 PREDELAY OUT (12 V)

TA6 PREDELAY OUT (5 V)

TA5 32 μs GATE (5 V)

TB2 UP (5 V)

TA7 DOWN (5 V)

Fig. E-2. Data timing No. 2

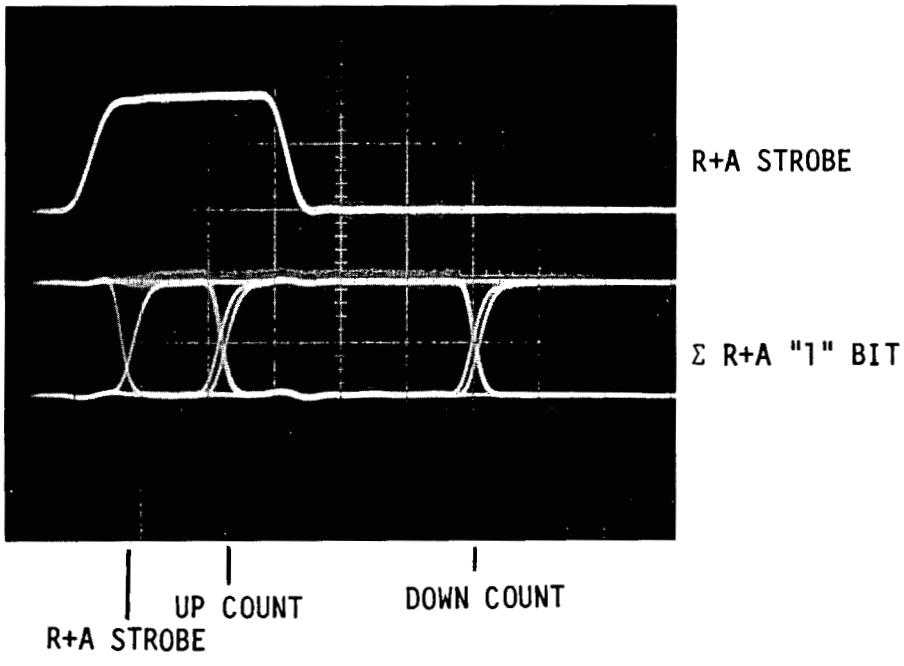


Fig. E-3. Coincidence gate timing.

Figures E-4, -5, and -6 are photographs obtained with a Tektronix 7D01 logic analyzer (plug-in) module installed in a Tektronix 7603 oscilloscope mainframe using a C-50 camera. Each figure's horizontal scale is nominally 250 ns/div. The traces are idealized figures, rather than real time; the signals are available at the test points listed after the signal label with the exception of the (Sigma) R+A 1 signal, which is sourced at component 3C, pin 11 (shift-register board). The timing reference is the top trace, SRCK (Shift-Register Clock) TA3. Triggering was generated by the SYNC OUT (Data Synchronizer Output) TA2. In Fig. E-4, the input to the shift register was a manually triggered single-shot pulse and in Figs. E-5 and -6, a manually triggered pulse and (variable) delay pulse pair. The delay pulse in Fig. E-5 was delayed by less than the predelay setting from the initial pulse, whereas that of Fig. E-6 was delayed by a time greater than that of the predelay setting.

Figure E-7 illustrates the various clock signals in the HEC-100. The photograph was taken with the same equipment as that used in Figs. E-4, -5, and -6; again, these are idealized waveforms rather than real-time representations. The figure's horizontal scale is nominally 200 ns/div. Triggering was on the initial positive-going transition of Phase 2; this signal is available at (shift-register board) component location 8D, pin 11 (Phase 2 level shifter). The other signals aside from Phase 1 and SRCK, which are available at the listed test points, are sourced at the following locations.

CK	component location 10D, pin 2
CK 1/2	component location 9D, pin 6
CK 1/2 + 150 ns	component location 6D, pin 12
CK 1/2 + 250 ns	component location 6D, pin 10
CK 1/2 + 350 ns	component location 6D, pin 8

The clock sources are schematically represented on Los Alamos Drawing D200734-1.

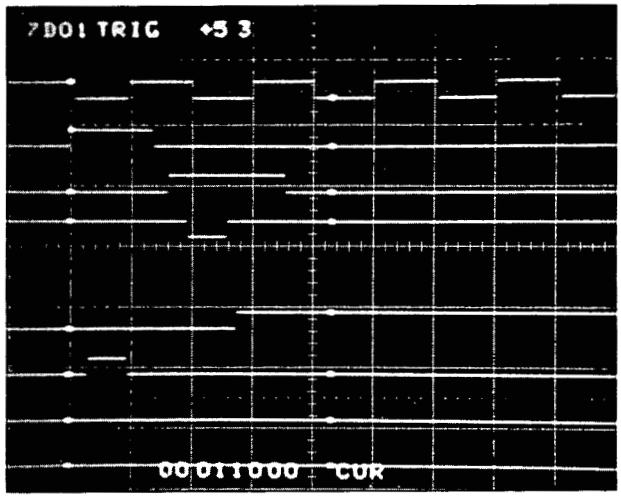


Fig. E-4. Single pulse input.

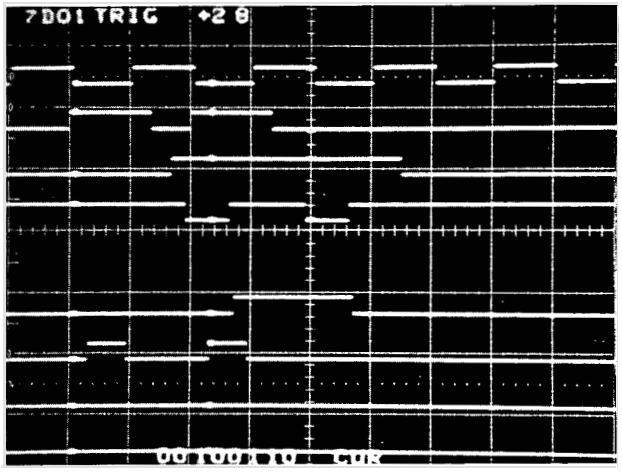


Fig. E-5. Double pulse input. (Delay period less than predelay).

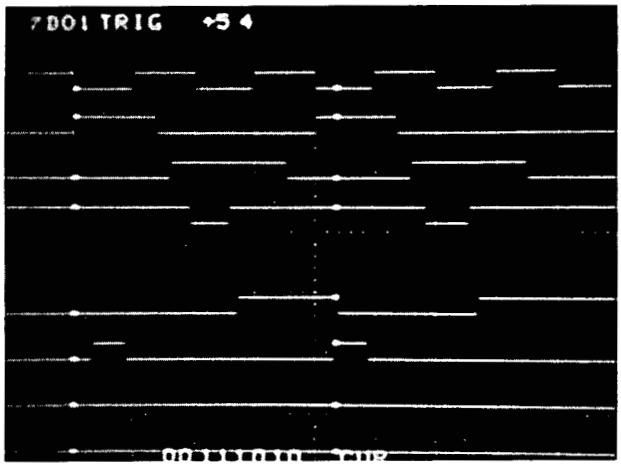
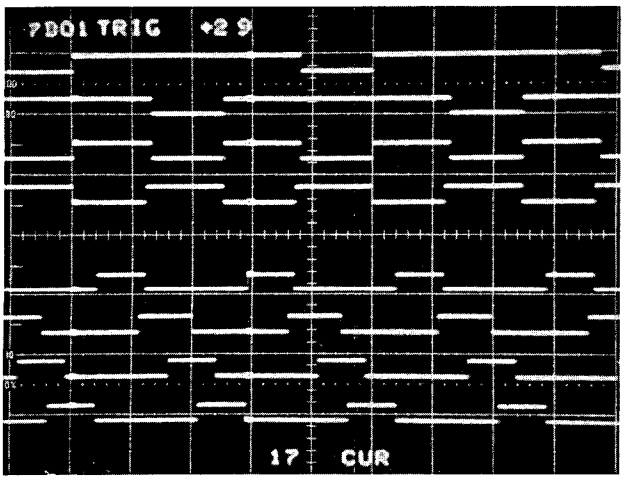


Fig. E-6. Double pulse input. (Delay period greater than predelay).



ϕ 2
ϕ 1 TB1
SRCK TA3
CK

CK 1/2
CK 1/2 plus 150 ns
CK 1/2 plus 250 ns
CK 1/2 plus 350 ns

Fig. E-7. Clock Timing.

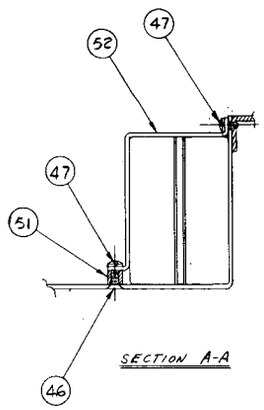
APPENDIX F

HLNCC SCHEMATIC SET

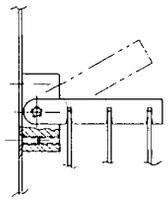
The schematic sets in these manuals derive from the schematic set documenting the original (prototype) instrument. The title for that set is IAEA Thermal Neutron Coincidence Counter, Los Alamos Dwg. 68Y155362, sheets D1 through D11. The schematic set was then redrawn and renumbered for publication[2] by EG&G in conjunction with their manufacture of the production prototype instrument. A listing of the schematic sets is shown below. The EG&G drawing set has subsequently been retitled/renumbered by IRT Corporation for inclusion in their manual[3] (issued with the current production instrument).

E200794 Neutron Counter Assembly
D200726 System Cable Interconnect
D200740 Power Distribution
C200694 Preamplifier Board Assembly
D200739 HV J-Box and Preamplifier Schematic
C200749 Mother Board Assembly
C200728 Amplifier Board Assembly
D200729 Analog/Discriminator Schematic
C200735 Shift-Register Assembly
D200734 Shift-Register Schematic (two sheets)
C200768 Component Platform Assembly
C200742 Microprocessor Assembly
D200741 Microprocessor Schematic (four sheets)
C200755 Driver Board Assembly
D200753 Display and Driver Boards Schematic
C200752 Display Board Assembly
C200757 DC/DC Converter Assembly
D200758 DC/DC Converter Schematic
C200746 High-Voltage Board Assembly
D200747 High-Voltage Board Schematic
C200760 Rectifier Board Assembly
D200733 Neutron Counter Phase II (Two sheets)

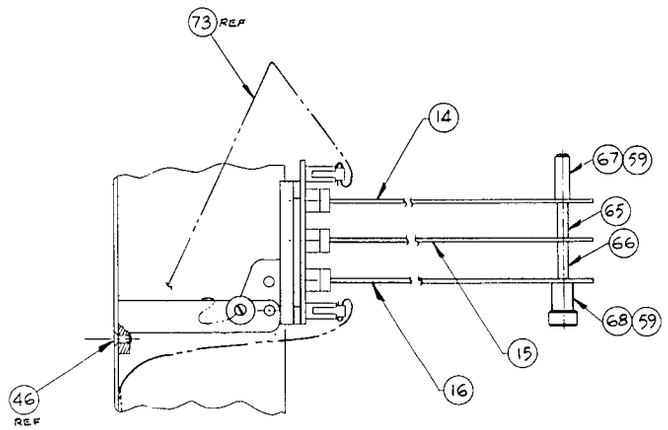
REVISIONS				
LTR	ZONE	DESCRIPTION	DATE	APPR
A		REV WITH EXTENSIVE CHANGES	5-4-78	KJ
B		ITEM NO. 7 P/N WAS: R-6377	9-7-78	KS
C		ADD ITEM 82 ITEM 33 WAS: DBM-25P ITEM 34 WAS: DAM-15P	10/4/78	PR



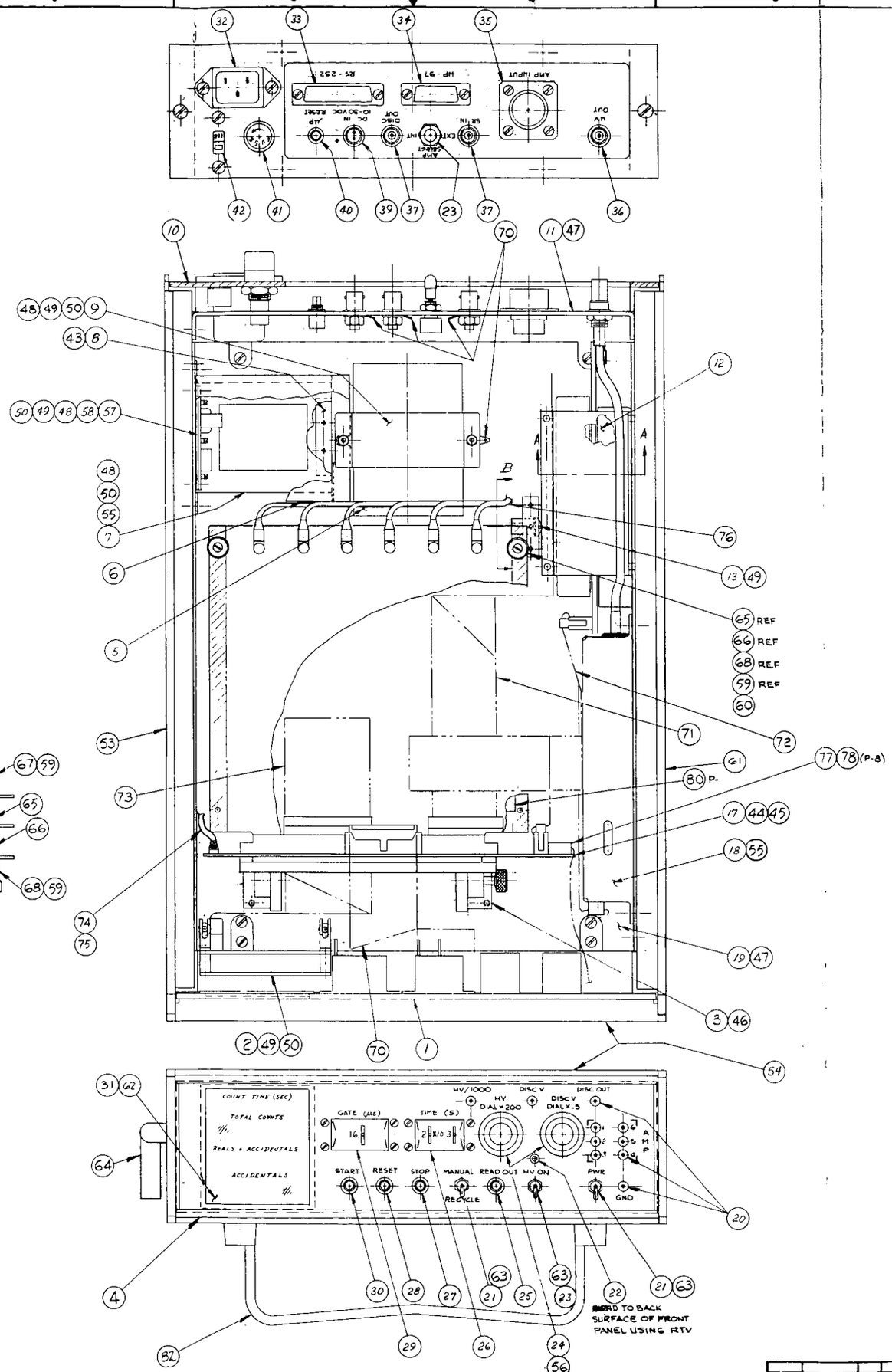
SECTION A-A



SECTION B-B



VIEW SHOWING PC BOARDS ROTATED TO VERTICAL



NOTES:

1. APPLY LOCTITE TO THE FOLLOWING:
   - A. ALL CHASSIS ASSEMBLY SCREWS
   - B. ALL COMPONENT/BRACKET MOUNTING SCREWS, EXCEPT THOSE HOLDING SWITCHES AND CONNECTORS
   - C. ALL MOTHER BOARD MOUNTING SCREWS
2. APPLY HEAT SINK COMPOUND TO THE OUTSIDE SURFACES OF THE DC/DC CONVERTERS.

AR		HEAT SINK COMPOUND DOW	A-A	84
AR		LOCTITE 242	A-A	83
1		BAE, BUCKEYE #MA-40008-8		82
REF	D200726-00	SYSTEM CABLE INTERCONNECT		81
REF	A200756-00	WIRE & PIN ASSIGNMENT		80
1	C200877-00	ASSY, CABLE, 12 COND, TWISTED PR		79
8	75691-015	CONTACT BERG		78
1	69043-033	CONNECTOR, 8 POS. BERG		77
6	C200873-02	ASSY, CABLE, COAX		76
1	C200873-01	ASSY, CABLE, COAX		75
1	C200873-00	ASSY, CABLE, COAX		74
1	C200874-00	ASSY, CABLE, 50 COND. RIBBON		73
1	C200874-00	ASSY, CABLE, 50 COND. RIBBON		72
1	C200875-01	ASSY, CABLE, 26 COND. RIBBON		71
1	C200874-00	ASSY, CABLE, 26 COND. RIBBON		70
4		GROUND LUG		69
2	B200869-00	KNOB		68
1	B200870-02	STANDOFF		67
2	B200870-01	STAND OFF		66
2	B200870-00	STANDOFF		65
1		8" ECONO HANDLE		64
4	N-40	SWITCH, DRESS NUT ALCO		63
AR		ADHESIVE, EASTMAN 910		62
1	D200812-00	CHASSIS SIDE PLATE MODIFICATION		61
1		SCREW, CAP, BIND HD, #4-40UNC-2B × 3/8 LG SST		60
3		SCREW, CAP, BIND HD, #4-40UNC-2B × 1/4 LG SST		59
2	397	SPACER, .196 × .167 DIA. ALUMINUM, KEYSTONE		58
1	B200760-00	BRIDGE RECTIFIER ASSEMBLY		57
2	M-498-3	DIAL, POTENTIOMETER, COUNTING BOURNS		56
5		SCREW, BIND HD, #6-32UNC-2A × 3/16 LG		55
1	35-3-17	BUCKEYE CHASSIS (MOD. PER ITEMS 1,6,10,57,61)		54
1	D200812-01	CHASSIS SIDE PLATE MODIFICATION		53
1	B200811-00	BRACKET, DC/DC CONVERTER		52
1	B200796-00	BRACKET, MOUNT DC/DC CONVERTER		51
4		NUT, HEX HD #6-32UNC-2B		50
6		SCREW, FLT HD, 100° CSK #6-32UNC-2A × 3/8 LG		49
4		WASHER, SPLIT LOCK #6		48
12		SCREW, BIND HD, #6-32UNC-2A × 1/4 LG		47
8		SCREW, FLT HD, 100° CSK #6-32UNC-2A × 1/4 LG		46
6		WASHER, FLAT #4 SST		45
6		SCREW, CAP, BIND HD, #4-40UNC-2B × 9/16 LG SST		44
4		SCREW, FLT HD, 100° CSK #4-40UNC-2A × 3/8 LG		43
1	4G25GLPE	SWITCH - VOLTAGE SELECTOR SWITCHCRAFT		42
1	342004	FUSE HOLDER, PANEL MTG LITTELFUSE		41
1	S85-AL-01	SWITCH, PUSH BUTTON TECLITE		40
1	2014-1-11	BNC, BULKHEAD RECEPTACLE, TWIN CONTACT		39
1	C200888-00	INSTRUMENT CASE, (NOT SHOWN ON ASSY)		38
2		BNC CONN UG-1094/U		37
1	51494-1	H.V. BNC AMP		36
1	MIL-C-23216	CONNECTOR BURNDY		35
1	DDM-15S	CONNECTOR CANNON		34
1	DBM-25S	CONNECTOR CANNON		33
1	GEFE	A.C. RECEPTACLE CORCOM		32
1	C200765-00	WINDOW (RED) L.E.D. DISPLAY		31
1	55BL-C05-AL12	SWITCH, PUSH BUTTON (GREEN LENS) TECLITE		30
1	1801750	SWITCH THUMBWHEEL, E-D-BGI INTERSWITCH		29
1	55BL-B05-AL04	SWITCH, PUSH BUTTON (YELLOW LENS) TECLITE		28
1	55BL-A05-AL02	SWITCH, PUSH BUTTON (RED LENS) TECLITE		27
1	1801751	SWITCH, THUMBWHEEL; E-D-BGI, INTERSWITCH		26
1	55BL-A05-AL07	SWITCH, PUSH BUTTON (CLEAR LENS) TECLITE		25
2	35005-1	POTENTIOMETER BOURNS		24
2	MTL-206N	SWITCH - TOGGLE ALCO		23
1	5082-4468	L.E.D. H.P.		22
2	MTE-206N	SWITCH - TOGGLE ALCO		21
10	43521-0310	JACK CAMBION		20
1	E200808-00	COMPONENT TRAY		19
1	C200820-00	H.V. PWR ASSEMBLY		18
1	C200749-00	MOTHER BOARD ASSEMBLY		17
1	C200728-00	ANALOG BOARD ASSEMBLY		16
1	C200735-00	SHIFT REGISTOR BOARD ASSEMBLY		15
1	C200742-00	MICROPROCESSOR BOARD ASSEMBLY		14
1	C200801-00	P.C.B. SUPPORT ASSEMBLY		13
1	C200757-00	DC TO DC CONVERTER ASSEMBLY		12
1	D200799-00	REAR SUB-PANEL		11
1	C200798-00	REAR PANEL		10
1	B200810-00	CAPACITOR CLAMP		9
1	B200767-00	TRANSFORMER BRACE		8
1	P-6877	PWR TRANSFORMER STANCOR		7
1	B200868-00	SHIELD A.C.		6
1		CAPACITOR (602D123G050CB2D) SPRAGUE		5
1	B200878-00	CROSS BRACE, MOD. (BUCKEYE CHASSIS)		4
1	C200863-00	LIFT & SUPPORT MECHANISM (MOTHER BOARD		3
1	C200795-00	L.E.D. DISPLAY ASSEMBLY		2
1	D200797-00	FRONT PANEL		1
PART NO.		DESCRIPTION	NOTE	ITEM NO.

LIST OF MATERIAL

DRAWN	J.T. SUTTON 2/9/78	EG&G LOS ALAMOS DIVISION
CHECKED		EG&G, INC. P.O. BOX 809, LOS ALAMOS, NEW MEXICO 87544
DESIGNER		NEUTRON COUNTER ASSY
ENGINEER		
PROJ. ENG.		
PROJECT APPROVAL		
FINISH SPECS		CALC. WT. / CODE IDENT NO. / SIZE / DWG. NO. / REV. C / E 200794

QTY REQ'D PER ASS'Y UNLESS OTHERWISE SPECIFIED

DIMENSION TOLERANCE: DECIMALS ± / FRACTIONS ± / ANGULAR ±

A. DRILLED HOLE TOLERANCE PER ANSI B94.11

B. REMOVE BURRS AND SHARP EDGES

C. WELDS REMOVE LOOSE SCALE & SPATTER

D. SURFACE ROUGHNESS PER MIL-STD-10

E. WORKMANSHIP PER EG&G STD 220008

H-DES — CROSS INDEX — NEXT ASSEMBLY — REQ'D

PART NO. E200794

DO NOT SCALE THIS DWG. SCALE ½ SHEET 1 OF 1

REVISIONS				
LTR	ZONE	DESCRIPTION	DATE	APPR

DISPLAY BOARD
SCH D200753
ASSY C200752

DRIVER BOARD
SCH. D200753
ASSY. C200755

J30
P30

50
C200876

P1
J1

TO FRONT PANEL

26
C200875-00

P3
J3

TO REAR PANEL

26
C200875-01

P2
J2

DISC. OUT

S.R. IN

EXT
INT
SW10

COAX
C200873

P9
J9

COAX
C200873

P10
J10

DISC OUT TO FRONT PANEL MONITOR POINT

1

P8
J8

MOTHER BOARD
WIRE LIST A200809

J4
P4

J5
P5

J6
P6

J7
P7

J32 ANALOG BOARD
SCH. D200729
ASSY. C200728
J101 J102 J103 J104 J105 J106

SHIFT REGISTER BOARD
SCH. D200734
ASSY. C200735

MICROPROCESSOR BOARD
SCH. D200741
ASSY. C200742

26

NOTE:
ALL FRONT & REAR PANEL CONNECTIONS REFER TO SYSTEM WIRE LIST A200750

4
10
14
C200874
10
20
40

P12
J12

HIGH VOLTAGE BOARD
SCH. D200747
ASSY. D200746

P11
J11

DC/DC CONV. BOARD
SCH. D200758
ASSY. D200757

6
C200877

6 COAX
C200873

TO FRONT PANEL MONITOR POINTS

TO P15 REAR PANEL (ANALOG INPUT)

TO P15 REAR PANEL (PWR OUT TO J BOX)

TO FRONT PANEL

TO REAR PANEL (HI-V OUT)

TO FRONT PANEL DISC. V.

POWER IN

C1
12,000 μf

PART NO	DESCRIPTION	NOTE	ITEM NO.

LIST OF MATERIAL

DRAWN	LEM	4-78
CHECKED		
DESIGNER		
ENGINEER	R. SLICE	
PROJ. ENG.		
PROJECT APPROVAL		
FINISH SPECS		

QTY REQ'D PER ASSY
UNLESS OTHERWISE SPECIFIED
DIMENSION TOLERANCE
DECIMALS ± FRACTIONS ± ANGULAR ±
A. DRILLED HOLE TOLERANCE PER ANSI 0367
B. REMOVE BURRS AND SHARP EDGES
C. WELDS: REMOVE LOOSE SCALE & SPATTER
D. SURFACE ROUGHNESS PER MIL-STD-10
E. WORKMANSHIP PER EG&G STD A900020

CROSS INDEX	NEXT ASSEMBLY	REQ'D PER N/A
H-DT-3	E200794	REF -00

PART NO. D200726

EG&G LOS ALAMOS DIVISION
EG&G, INC. P.O. BOX 809, LOS ALAMOS, NEW MEXICO 87544

SYSTEM CABLE INTERCONNECT NEUTRON COUNTER PHASE-II

CALC. WT.	CODE IDENT NO.	SIZE	DWG. NO.	REV.
			D200726	

DO NOT SCALE THIS DWG | SCALE: ~ | SHEET 1 OF 1

REVISIONS				
LTR	ZONE	DESCRIPTION	DATE	APPR
A		RENUMBERED JT		

RECTIFIER BOARD
C200760

DC/DC CONVETER BD.
C200757
SCHEM. D200758

HIGH VOLTAGE BD.
C200746
SCHEM. D200747

MOTHER BD.
C200749
RUN LIST A200803

DISPLAY/DRIVER BOARDS
C200752
C200755
SCHEM. D200753

BIFURCATED TERMINAL LUGS

J19 REAR PANEL DC IN

TWISTED WIRE

ON/OFF FRONT PANEL

IN4722

TWISTED SHIELDED

CORCOM A.C. RECEPTACLE AND FILTER

110/220 LINE

REAR PANEL

SHOWN IN 220V POSITION

VARO VH447 BRIDGE RECTIFIER

12,000 µF

82µF 82µF 2.2µF

TO CHASSIS GND LUG

DC/DC CONVERTER
+12V
-12V
+5V

DC/DC CONVERTER
-15V
+15V
+5V N/U

-12V

LM220 -5V

VOLTAGE REGULATOR

TO FRONT PANEL

50

P12 J12

J12

J11 P11

P7 J7

SPARE
SPARE

C6 4.7 35V
C5 2.2µ 35V
C4 2.2µ 35V
C1 2.2µ 35V
C2 2.2µ 35V
C3 2.2µ 35V

J1 P1

P30 J30

F J15 PRE-AMP CONNECTOR REAR PANEL
E -15V
G +15V
H

TWISTED

50 WIRE FLAT RIBBON CABLE (WIRE 1 IS MARKED BROWN AND LOCATED PHYSICALLY NEAR BOTTOM OF THE CHASSIS)

CROSS INDEX	NEXT ASSEMBLY	REQ'D PER N/A
H-DT-3	E200794	REF 00

PART NO. D200740

QTY REQ'D PER ASSY

UNLESS OTHERWISE SPECIFIED

DIMENSION TOLERANCE

DECIMALS ±	FRACTIONS ±	ANGULAR ±

A DRILLED HOLE TOLERANCE PER ANSI B32.1
B REMOVE BURRS AND SHARP EDGES
C WELDS: REMOVE LOOSE SCALE & SPATTER
D SURFACE ROUGHNESS PER MIL-STD-10
E WORKMANSHIP PER EG&G STD 4900020

FINISH SPECS

PART NO	DESCRIPTION	NOTE	ITEM NO.

LIST OF MATERIAL

DRAWN	L&M
CHECKED	
DESIGNER	
ENGINEER	R. SLICE
PROJ. ENG	
PROJECT APPROVAL	

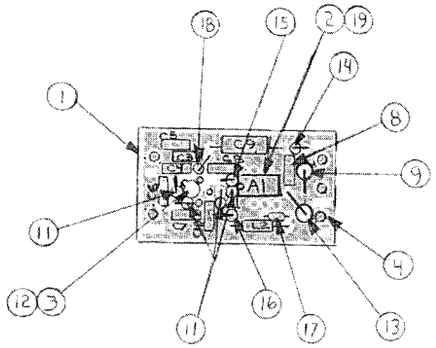
EG&G LOS ALAMOS DIVISION
EG&G, INC. P.O. BOX 809, LOS ALAMOS, NEW MEXICO 87544

SCHEMATIC DIAGRAM POWER DISTRIBUTION DWG

CALC. WT.	CODE IDENT NO.	SIZE	DWG. NO.	REV.
		D	D200740	A

DO NOT SCALE THIS DWG | SCALE: ~ | SHEET 1 OF 1

REVISIONS				
LTR	ZONE	DESCRIPTION	DATE	APPR
A		REDESIGNED/REDRAWN		



NOTES: UNLESS OTHERWISE SPECIFIED:

1. FOR SHEMATIC SEE DWG NO. D200739
2. DIODES MOUNTED WITH CATHODE UP.
3. MOUNT WITH POSITIVE END DOWN.
4. REMOVE AND DISCARD TOP HALF OF PIN.

	PART NO.	SOURCE	DESCRIPTION	DESIG.	NOTE	ITEM NO.
1	1321	TELEDYNE	OP AMP EE-1951/46A-46	A1		19
1	CB 4765	A/B	RESISTOR, 47 M, 1/4W, 5% EE-3827/4T-16P	R3		18
1	BB 6235	A/B	RESISTOR, 62K, 1/8W, 5% EE-3965/4T-6B	R5		17
1	CB 2235	A/B	RESISTOR, 22K, 1/4W, 5% EE-8273/4T-12Q	R6		16
1	CB 1825	A/B	RESISTOR, 1.8K, 1/4W, 5% EE-8247/4T-11N	R4		15
1	CB 1015	A/B	RESISTOR, 100 Ω, 1/4 W, 5% EE-8217/4T-17	R7		14
2	1537-76	DELLVAN	COIL, 100 μh EE-9302/5N-150K	L1, L2		13
1	2N 4860	NSC	TRANSISTOR, FET EE-9403/4GA-9	Q1		12
4	IN4154	ITT	DIODE, SWITCHING EE-7382/4EA-52	CR1-4	2	11
1	150D476X9006B2	SPRAGUE	CAP, ELECT, 47 μF, 6V EE-2155/5H-129	C9		10
1	150D226X9015B2	SPRAGUE	CAP, ELECT, 22 μF, 15V EE-2162/5H-141	C12	3	9
3	8131-100-651-474M	ERIE	CAP, CER. MONO, .47 μF EE-489/5G-35	C7,10,11		8
1	8121-100-W5R0-103K	ERIE	CAP, CER. MONO, .01 μF, EE-484/5G-29	C6		7
1	DM-15-121	ARCO	CAP, SIL. MICA, 120 pF EE-7651/5M-37	C5		6
3	CN15B100J	CENTRALAB	CAP, CER, NPO, 10 pF EE-10008/5AB-185	C3,4,8		5
5			PIN EE-0658/5U-64		4	4
3	3-330808-8	AMP	SOCKET, PIN EE-8011/4F-5			3
1	930802	TI	SOCKET, 8 PIN DIP EE-4654/4DA-68			2
1	B200693-00	EG&G	PWB, PREAMP			1

LIST OF MATERIAL

DRAWN	S. SCARLOTT	8-8-78
CHECKED		
DESIGNER	R RICE	
ENGINEER	R. SLICE	
PROJ. ENG		

PROJECT APPROVAL

FINISH SPECS

H-DT-3		6	-00
CROSS INDEX	NEXT ASSEMBLY	REQ'D PER N/A	

PART NO. C200694

QTY REQ'D PER ASS'Y

UNLESS OTHERWISE SPECIFIED

DIMENSION TOLERANCE

DECIMALS ± FRACTIONS ± ANGULAR ±

A. DRILLED HOLE TOLERANCE PER ANDI0387

B. REMOVE BURRS AND SHARP EDGES

C. WELDS: REMOVE LOOSE SCALE & SPATTER

D. SURFACE ROUGHNESS PER MIL-STD-10

E. WORKMANSHIP PER EG&G STD A900020

EG&G LOS ALAMOS DIVISION

EG&G, INC. · P.O. BOX 809, LOS ALAMOS, NEW MEXICO 87544

ASSY, PREAMP BOARD

NEUTRON COUNTER

CALC. WT.	CODE IDENT NO.	SIZE	DWG. NO.	REV
		C	C200694	A

DO NOT SCALE THIS DWG | SCALE: 1/1 | SHEET 1 OF 1

REVISIONS				
LTR	ZONE	DESCRIPTION	DATE	APPR
'A	C4	ADDED 50Ω RES & .039/3KV CAP		

NEUTRON COUNTER REAR PANEL

P16 J16

HIGH VOLTAGE BOX / PRE-AMP BOARD

PRE-AMP CH. 1 BOARD

FROM DET CH. 1 — P2 J2 E2

TEST INPUT — P3 J3 E3

E1 — R1 100K — R101 100K — C102 .01UF 3KV — R102 47M

.039 uFd 3KV — 50Ω

C101 2.2 PF

C106 .01 — C103 10 PF — C104 70PF — C105 120PF — R103 47M

CR101 IN 4154 — CR102 IN4154 — -15V

+15V — R104 1.8K — R105 62K — R106 22K

Q101 2N4860

CR103 IN-4154 — CR104 IN-4154

3 / 2 / 6 / 8 — 1321 A101 — C108 10PF — C107 .47

C109 47. 6V — R107 100 — E102

+15V — L101 100UH

PRE-AMP DECOUPLING

7 / 1321 / 4

C110 .47 — C112 22 15V — C111 .47

-15V — L102 100UH

C201 2.2 PF — R201 100K — CHANNEL 2

C301 2.2 PF — R301 100K — CHANNEL 3

C401 2.2 PF — R401 100K — CHANNEL 4

C501 2.2 PF — R501 100K — CHANNEL 5

C601 2.2 PF — R601 100K — CHANNEL 6

R207 100 — E202

R307 100 — E302

R407 100 — E402

R507 100 — E502

R607 100 — E602

L1 100UH +15V — E3

C1 100 20V — C2 .47

GND — E4

C3 100 20V -15V — C4 .47 — E5

L2 100UH

TWISTED/SHIELDED PAIR

J4	P4	P15	J15
A	A	A	A
B	B	B	B
P	P	P	P
R	R	R	R
M	M	M	N
N	N	N	N
L	L	L	L
U	U	U	U
V	V	V	V
S	S	S	S
K	K	K	K
J	J	J	J
H	H	H	H
G	G	G	G
E	E	E	E
F	F	F	F
C	C	C	C
D	D	D	D
T	T	T	T

N.C. N.C. N.C.

HIGH VOLTAGE CABLE — E1 — HIGH VOLTAGE SUPPLY SEE H.V. SCHEMATIC D200747

P101 J101 — P201 J201 — P301 J301 — P401 J401 — P501 J501 — P601 J601

ANALOG BD SEE ANALOG BD. SCHEMATIC D200729

P11 J11

P11	J11	
1	1	+15V
2	2	±15V RET
3	3	-15V
4	4	±15V RET

DC/DC CONVERTER BD. SEE DC/DC SCHEMATIC D200758

NOTES: UNLESS OTHERWISE SPECIFIED:
1. RESISTORS ARE IN OHMS, ⅛ W, 1%
2. CAPACITORS ARE IN MICROFARADS
3. FIRST DIGIT OF 3 DIGIT REFERENCE DESIGNATORS REFLECT CHANNEL NO.
4. LAST REFERENCE DESIGNATORS USED:

C4	A601	P601
E5	C612	Q601
J4	CR604	R607
L2	E602	
P4	J601	
R1	L602	

LIST OF MATERIAL

PART NO	DESCRIPTION	NOTE	ITEM NO.

DRAWN	L&M	4-21-78
CHECKED		
DESIGNER	P. RICE	
ENGINEER	R. SLICE	
PROJ ENG		
PROJECT APPROVAL		

QTY REQ'D PER ASSY

UNLESS OTHERWISE SPECIFIED
DIMENSION TOLERANCE
DECIMALS ± FRACTIONS ± ANGULAR ±

A DRILLED HOLE TOLERANCE PER ANDI0387
B REMOVE BURRS AND SHARP EDGES
C WELDS: REMOVE LOOSE SCALE & SPATTER
D SURFACE ROUGHNESS PER MIL-STD-10
E WORKMANSHIP PER E G & G STD A900020

FINISH SPECS

CROSS INDEX	NEXT ASSEMBLY	REQ'D PER N/A
14-DT 3	E200794	REF DO

PART NO D200739

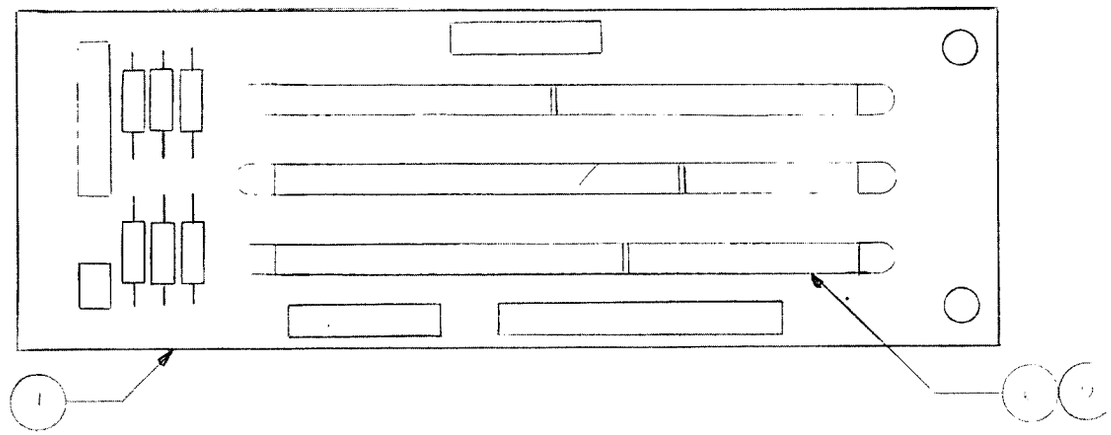
EG&G LOS ALAMOS DIVISION
EG&G, INC. P.O. BOX 809, LOS ALAMOS, NEW MEXICO 87544

SCHEMATIC DIAGRAM HIGH VOLTAGE JUNCTION BOX AND PRE-AMP NEUTRON COUNTER - II

CALC. WT.	CODE IDENT NO.	SIZE	DWG. NO.	REV
			D200739	A

DO NOT SCALE THIS DWG | SCALE: | SHEET 1 OF 1

REVISIONS				
LTR	ZONE	DESCRIPTION	DATE	APPR



ITEM NO	QTY	PART NO.	SOURCE	DESCRIPTION	DESIG.	NOTE
9	3	7192-0584	SYLVANIA	KEY, POLORIZING		
8	2	031E0059-0001	MALCO	CONNECTOR, COAXIAL, P.C.	J9, J10	
7	1	65611-308	BERG	CONNECTOR, MINI-LATCH	J8	
6	3	6AD04-50-1A2-00	SYLVANIA	CONNECTOR, CARD EDGE	J4, J5, J6	3
5	3	3493-2003	3M	CONNECTOR, HEADER	J2, J3, J7	
4	1	3496-2003	3M	CONNECTOR, HEADER	J1	
3	1	150D475X9035B2	SPRAGUE	CAP, TANTALUM, 4.7 μf, 35 WVDC	C6	2
2	5	150D225X9035B2	SPRAGUE	CAP, TANTALUM, 2.2 μf, 35 WVDC	C1-C5	2
1	1	C200748-00	EG&G	PWB, MOTHER		

LIST OF MATERIAL

C200749-00

NOTES: UNLESS OTHERWISE SPECIFIED

1. FOR SCHEMATIC DIA. SEE DWG NO. A200809
2. CAPACITORS C1-C6 ARE OPTIONAL
3. INSERT KEY ON J4 BETWEEN PINS 26-27
   J5 BETWEEN PINS 15-16
   J6 BETWEEN PINS 20-21
4. USE THE FOUR CORNER PINS ON J8 AND THE MATING CONNECTOR FOR MECHANICAL SUPPORT

DRAWN	S. SCARLOTT	5-3-78	
CHECKED			
DESIGNER	W. SHAW		
ENGINEER	R. SLICE		
PROJ ENG			

PROJECT APPROVAL

EG&G LOS ALAMOS DIVISION

EG&G, INC · P O BOX 809, LOS ALAMOS, NEW MEXICO 87544

ASSY, MOTHER BOARD

NEUTRON COUNTER II

CALC. WT.	CODE IDENT NO.	SIZE	DWG. NO.	REV
			C200749	

DO NOT SCALE THIS DWG | SCALE: 1/1 | SHEET 1 OF 1

QTY REQ'D PER ASS'Y

UNLESS OTHERWISE SPECIFIED

DIMENSION TOLERANCE

DECIMALS ± | FRACTIONS ± | ANGULAR ±

A DRILLED HOLE TOLERANCE PER ANDI0387

B REMOVE BURRS AND SHARP EDGES

C WELDS REMOVE LOOSE SCALE & SPATTER

D SURFACE ROUGHNESS PER MIL-STD-10

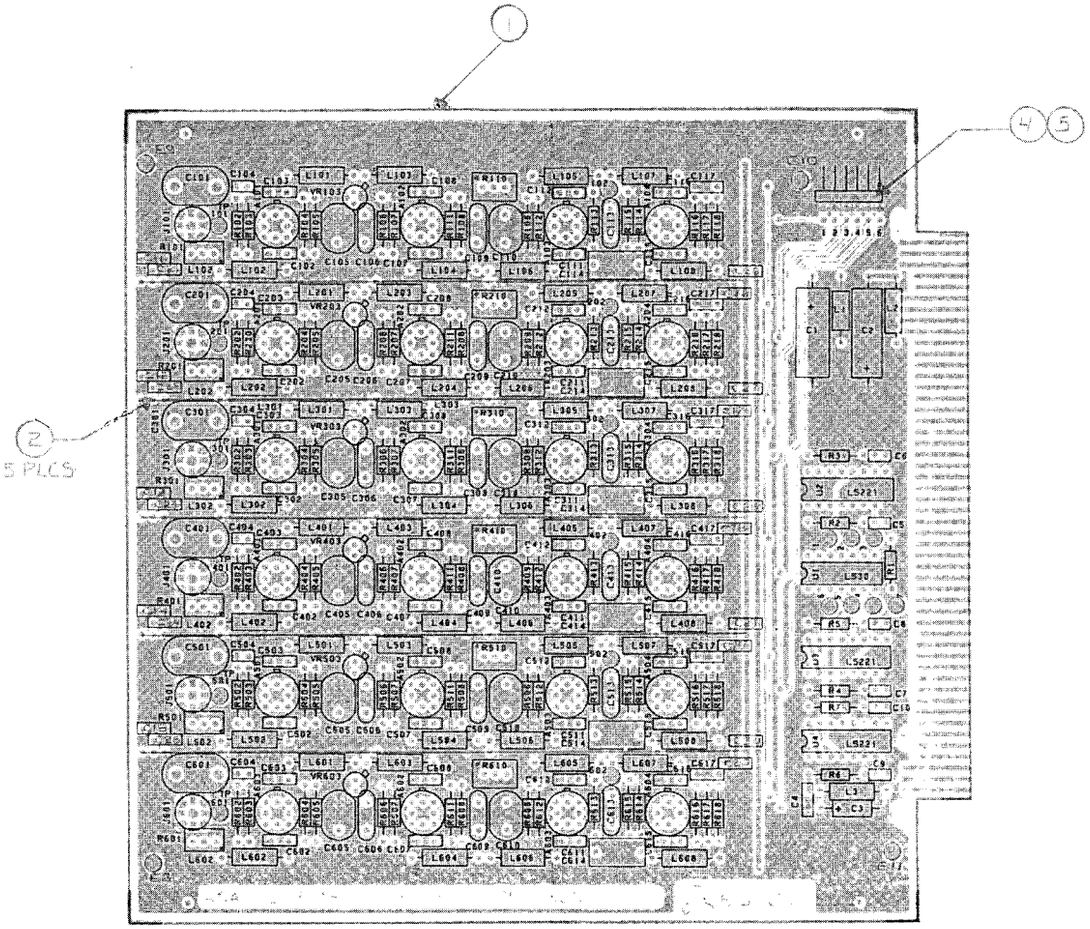
E WORKMANSHIP PER EG&G STD A900020

FINISH SPECS

CROSS INDEX	NEXT ASSEMBLY	REQD PER N/A	
H-DT-3	E200794	1	00

PART NO. C200749

REVISIONS				
LTR	ZONE	DESCRIPTION	DATE	APPR
A		L/M UPDATE.		
B		ITEM 10 WAS: CENTRALAB #CN10B4R7D200V ITEM 11 WAS: 851-C080-220J	5/9/79	SB



NOTES: UNLESS OTHERWISE SPECIFIED:
1. FOR SCHEMATIC DIA. SEE DWG D200729
2. "X" IN REFERENCE DESIGNATOR DENOTES CHANNEL NUMBER 1 THRU 6

12	1321	TELE/PHIL	OP AMP	AX01,X02	2	44
6	1322	TELE/PHIL	OP AMP	AX03	2	43
6	LM311H	NATL	VOLTAGE COMPARITOR	AX04	2	42
6	LM103	NATL	VOLTAGE REGULATOR	VRX01	2	41
3	74LS221	TI	DUAL ONE SHOT	U2-U4		40
1	74L530	TI	8-INPUT NAND	U1		39
6	CEA-TO	TRW/IRC	RESISTOR, MF, 100K, ¼ W, 1%	RX01	2	38
6	63WR10K	BECKMAN	POT, 10K, 22 TURN	RX10	2	37
12	CEA-TO	TRW/IRC	RESISTOR, MF, 12.1K, 1/8W, 1%	RX08, RX13	2	36
6	CEA-TO	TRW/IRC	RESISTOR, MF, 10K, 1/8W, 1%	RX14	2	35
12	CEA-TO	TRW/IRC	RESISTOR, MF, 5.11K, 1/8 W, 1%	RX04, RX05	2	34
6	CEA-TO	TRW/IRC	RESISTOR, MF, 2.74K, 1/8W, 1%	RX11	2	33
12	CEA-TO	TRW/IRC	RESISTOR, MF, 2.05K, 1/8W, 1%	R2-R4 RX03, RX16	2	32
6	CEA-TO	TRW/IRC	RESISTOR, MF, 1.33K, 1/8W, 1%	RX09	2	31
18	CEA-TO	TRW/IRC	RESISTOR, MF, 1.1K, 1/8W, 1%	RX06, RX07 RX18	2	30
6	CEA-TO	TRW/IRC	RESISTOR, MF, 274Ω, 1/8W, 1%	RX02	2	29
6	CEA-TO	TRW/IRC	RESISTOR, MF, 100Ω, 1/8W, 1%	RX15	2	28
6	CB1045	A/B	RESISTOR, 100K, 1/4W, 5%	RX17	2	27
						26
6	CB1025	A/B	RESISTOR, 1K, 1/4W, 5%	RX18	2	25
1	CB1015	A/B	RESISTOR, 100Ω, 1/4W, 5%	R1		24
3	1537-76	DELEVAN	INDUCTOR, 100 μh	L1, L2, L3		23
48	1537-60	DELEVAN	INDUCTOR, 47 μh	LX01, LX08	2	22
2	150D106X9035R2	SPRAGUE	CAP, TANT. ELECT., 10 μF, 35 VDC	C1, C2		21
1	150D685X9006A2	SPRAGUE	CAP, TANT. ELECT., 6.8 μF, 6 VDC	C3		20
6	5CE5U225X0050K5	SPRAGUE	CAP, CER. MONO, 2.2 μF, 50V	CX14	2	19
55	8131-100-651-474M	ERIE	CAP, CER. MONO., .47 μF, 100V	C4, CX02, CX07, CX08, CX11, CX12, CX15, CX16	2	18
20	8131-100-651-104M	ERIE	CAP, CER. MONO., .1 μF, 100V	C11-C30		17
6	DM19-471	ARCO	CAP, SILVER MICA, 470 pf	CX01	2	16
6	DM15-391	ARCO	CAP, SILVER MICA, 390 pf	CX10	2	15
6	DM-15-121	ARCO	CAP, SILVER MICA, 120 pf	CX05	2	14
6	CN20B820J	CENTRALAB	CAP. CER, NPO, 82 pf, 200V	C5-C10		13
12	851-C020-330J	ERIE	CAP CER. S. NPO, 33 pf, 500V	CX06, CX13	2	12
6	851-C020-270J	ERIE	CAP. CER. S. NPO, 27 pf, 500V	CX09	2	11
6	8101-100-C0H0-479D	ERIE	CAP, CER. MONO., 4.7 pf, 100V	CX04	2	10
3	716-AG-2D	AUGAT	SOCKET, 16 PIN DIP			9
1	714-AG-2D	AUGAT	SOCKET, 14 PIN DIP			8
24	7068-362-0	EMIC	SOCKET, 8 PIN			7
23	2043-2	CAMBION	TERMINAL, SOLDER	E1-E47 TPX01, TPX02	2	6
1	65524-106	BERG	HEADER, 6 PIN	P31		5
1	65521-106	BERG	HEADER, 6 PIN	P31		4
6	031-0061-0001	MALCO	CONNECTOR, MIN. COAX, MICRODOT	JX01	2	3
5	B200730-00	EG&G	BUS STRIP			2
1	C200727-00	EG&G	PWB, AMPLIFIER			1
PART NO.		SOURCE	DESCRIPTION	DESIG.	NOTE	ITEM NO.

C200728-00

LIST OF MATERIAL

DRAWN	S. SCARLOTT	4-26-78
CHECKED		
DESIGNER		
ENGINEER	R. SLICE	
PROJ. ENG		
PROJECT APPROVAL		

EG&G LOS ALAMOS DIVISION
EG&G, INC. P.O. BOX 809, LOS ALAMOS, NEW MEXICO 87544

ASSY, AMPLIFIER BOARD

NEUTRON COUNTER II

CALC. WT.	CODE IDENT NO.	SIZE	DWG. NO.	REV
		C	C200728	B

DO NOT SCALE THIS DWG | SCALE 1/1 | SHEET 1 OF 1

FINISH SPECS

H-DT-3	E280794	1	00
CROSS INDEX	NEXT ASSEMBLY	REQD PER N/A	

PART NO. C200728

QTY REQ'D PER ASS'Y

UNLESS OTHERWISE SPECIFIED

DIMENSION TOLERANCE		
DECIMALS ±	FRACTIONS ±	ANGULAR ±

A DRILLED HOLE TOLERANCE PER ANDI0387
B REMOVE BURRS AND SHARP EDGES
C WELDS REMOVE LOOSE SCALE & SPATTER
D SURFACE ROUGHNESS PER MIL-STD-10
E WORKMANSHIP PER EG&G STD A900020

REVISIONS				
LTR	ZONE	DESCRIPTION	DATE	APPR
A	C1	UPDATED	5-7-79	S.S.
B	A,B 1	ADDED A,B-42, A,B-43 TO P4/J4	10/30/79	PRC

ANALOG CHANNEL 1
ANALOG CHANNEL 2
ANALOG CHANNEL 3
ANALOG CHANNEL 4
ANALOG CHANNEL 5
ANALOG CHANNEL 6

P31 TO FRONT PANEL MONITOR POINTS

POLE ZERO
GAIN

TO FRONT PANEL DISC OUT MONITOR POINT

REAR PANEL TO HI-VOLT JCT BOX

DIGITAL SECTION

SHIFT REGISTER BD.

ANALOG BD.
MOTHER BD.

NOTES: UNLESS OTHERWISE SPECIFIED:

1. ALL FRONT AND REAR PANEL CONNECTIONS REFER TO SYSTEM WIRE LIST A200750
2. FIRST DIGIT OF 3 DIGET REFERENCE DESIGNATORS REFLECT CHANNEL NUMBER
3. RESISTORS ARE IN OHMS, 1/8W, 1%
4. CAPACITORS ARE IN MICROFARADS
5. LAST REFERENCE DESIGNATORS USED

C615	TP602	U4	R7
A604	J601	E11	
R618	VR601	L3	
L608		C30	

PART NO	DESCRIPTION	NOTE	ITEM NO.

LIST OF MATERIAL

DRAWN	L&M	4-21-78
CHECKED		
DESIGNER		
ENGINEER	R.SLICE	
PROJ ENG		
PROJECT APPROVAL		
FINISH SPECS		

QTY REQ'D PER ASSY
UNLESS OTHERWISE SPECIFIED
DIMENSION TOLERANCE
DECIMALS ± FRACTIONS ± ANGULAR ±
A. DRILLED HOLE TOLERANCE PER ANDI0387
B. REMOVE BURRS AND SHARP EDGES
C. WELDS: REMOVE LOOSE SCALE & SPATTER
D. SURFACE ROUGHNESS PER MIL-STD-10
E. WORKMANSHIP PER EG&G STD A900020

14-DT-3	C200728	REF	00
CROSS INDEX	NEXT ASSEMBLY	REQ'D PER NHA	

PART NO. D200729

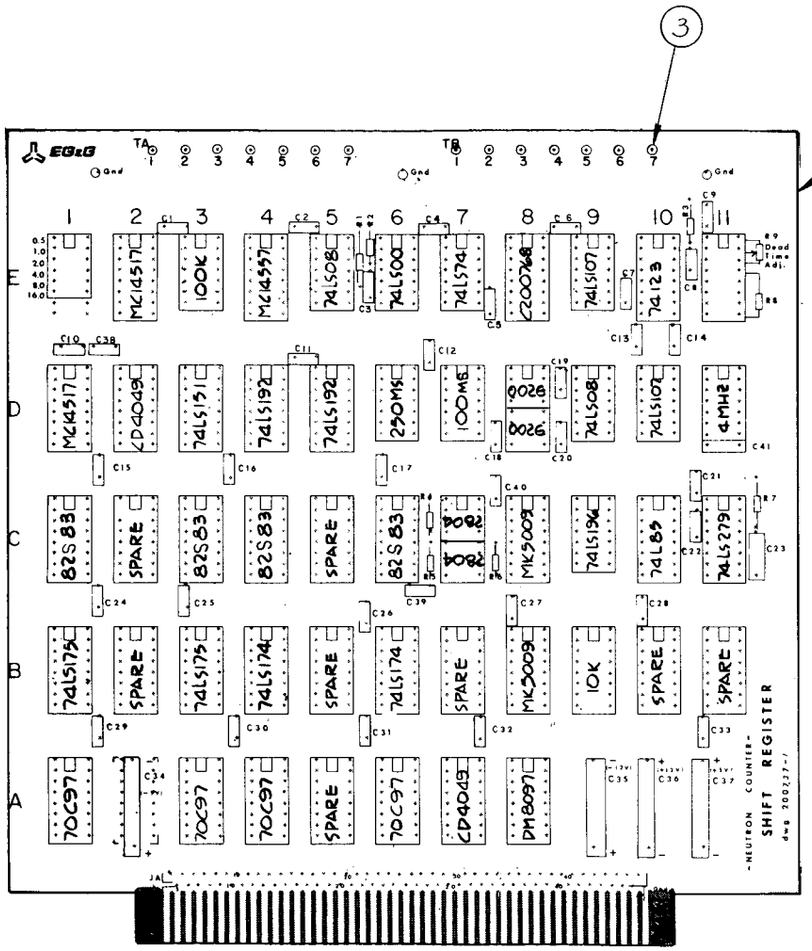
EG&G LOS ALAMOS DIVISION
EG&G, INC. P.O. BOX 809, LOS ALAMOS, NEW MEXICO 87544

SCHEMATIC DIAGRAM ANALOG / DISCRIMINATOR NEUTRON COUNTER PHASE II

CALC. WT.	CODE IDENT NO.	SIZE	DWG. NO.	REV
			D200729	B

DO NOT SCALE THIS DWG | SCALE: ~ | SHEET 1 OF 1

REVISIONS				
LTR	ZONE	DESCRIPTION	DATE	APPR
A	B4 B2	B4 WAS: 74LS175. ITEM 7 WAS: 8121-100-W5R0-152K	5/9/79	ECO
B	B1	ITEM 5 WAS: 100pF	10/16/79	ECO



NOTES : UNLESS OTHERWISE SPECIFIED

1. FOR SCHEMATIC DIA. SEE DWG. D200734
2. MOUT WITHOUT SOCKET
3. REFERENCE DESIGNATORS FOR ITEM 8 ARE C1, C2, C4, C6, C9 - C21, C24 - C33, C38 - C41

QTY	PART NO.	SOURCE	DESCRIPTION	DESIG	NOTE	ITEM NO
1	SN74LS196	TI	COUNTER/DIVIDER	9C		41
2	SN74LS192	TI	BCD COUNTER	4D,5D		40
2	SN74LS175	TI	QUAD 'D' FLIPFLOP	1B,3B		39
2	SN74LS174	TI	HEX 'D' FLIPFLOP	4B,6B		38
1	SN74LS151	TI	DATA SELECTOR, 1 OF 8	3D		37
1	SN74123	TI	DUAL SINGLE SHOT	10E		36
2	SN74LS107	TI	DUAL J-K FLIPFLOP	9E,10D		35
1	SN74L85	TI	4 BIT MAGNITUDE COMPARATOR	10C		34
1	SN74LS74	TI	DUAL 'D' FLIP FLOP	7E		33
2	SN74LS08	TI	QUAD AND	9D,5E		32
1	SN74LS00	TI	QUAD NAND	6E		31
4	N82S83	SIGNETICS	BCD ADDER, 4 BIT	1C, 3C 4C, 6C		30
4	MM70C97	NATL	HEX TRISTATE BUFFER	1A, 3A 4A, 2A		29
2	MK5009P	MOSTEK	COUNTER, TIME BASE	8B,8C		28
2	MMH0026	MOTA	LEVEL SHIFTER	8D		27
1	MC14557BA	MOTA	64 BIT VARIABLE LENGTH REGISTER	4E		26
2	MC14517BA	MOTA	DUAL SHIFT REGISTER	1D, 2E		25
1	DM8097	NATL	HEX TRI STATE BUFFER	8A		24
1	C02388	VECTRON	OSC, 4MHz	11D	2	23
2	CD4049AD	RCA	HEX BUFFER	7A, 2D		22
2	AM2804	AMD	1024 BIT SHIFT REGISTER	7C		21
1	899-1-R100K	BECKMAN	R-PAK, 100K	3E		20
1	898-1-R10K	BECKMAN	R-PAK, 10K	9D		19
1	66X-R10K	BECKMAN	POT, 10K, 22 TURN	R9		18
1	CB1045	A/B	RESISTOR, 100K, 1/4W, 5%	R7		17
1	CB3335	A/B	RESISTOR, 33K, 1/4W, 5%	R3		16
1	CB1025	A/B	RESISTOR, 10K, 1/4W, 5%	R1		15
1	CB4725	A/B	RESISTOR, 4.7K, 1/4W, 5%	R5		14
2	CB3025	A/B	RESISTOR, 3K, 1/4W, 5%	R4, R6		13
1	CEA-TO	TRW/IRC	RESISTOR, 2.05K, 1/8W, 1%	R8		12
1	CEA-TO	TRW/IRC	RESISTOR, 470Ω, 1/8W, 1%	R2		11
4	150D106X9035R2	SPRAGUE	CAP. TANT. ELECT., 10μF, 35V	C34-C37		10
2	5C25U225X0050C5	SPRAGUE	CAP. CER. MONO., 2.2μF, 50V	C8, C23		9
31	8131-100-651-474M	ERIE	CAP. CER. MONO., .47μF, 100V		3	8
1	8101-100-W5R0-680K	ERIE	CAP. CER. MONO., 68PF, 100V	C5		7
1	8111-100-W5R0-681K	ERIE	CAP. CER. MONO., 680PF, 100V	C7		6
1	8121-100C060-201K	ERIE	CAP. CER. MONO., 200PF, 100V	C22		5
1	8121-100C060-470K	ERIE	CAP. CER. MONO., 47 PF, 100V	C3		4
17	2043-3	CAMBION	TERMINAL, TURRET			3
1	C200768	EG&G	ASSY, COMPONENT PLATFORM	8E		2
1	D200737-00	EG&G	CKT. BD. SHIFT REGISTER			1
C200735-00	PART NO.	SOURCE	DESCRIPTION	DESIG.	NOTE	ITEM NO.

LIST OF MATERIAL

30	716-AG-2D	AUGAT	SOCKET, DIP, 16 PIN			47
11	714-AG-2D	AUGAT	SOCKET, DIP, 14 PIN			46
1	76PB-06	GREYHILL	DIP SWITCH	1E		45
1	TTL-DM2350	EC²	TIME DELAY	6D		44
1	TTL-DM100	EC²	TIME DELAY	7D		43
1	SN74LS279	TI	QUAD LATCH	11C		42

PART NO. C200735

CROSS INDEX	NEXT ASSEMBLY	REQ'D PER N/A	
H-DT-3	E200794	1	-00

QTY REQ'D PER ASS'Y

UNLESS OTHERWISE SPECIFIED

DIMENSION TOLERANCE

DECIMALS ±	FRACTIONS ±	ANGULAR ±

A DRILLED HOLE TOLERANCE PER ANDI0367
B REMOVE BURRS AND SHARP EDGES
C WELDS: REMOVE LOOSE SCALE & SPATTER
D SURFACE ROUGHNESS PER MIL-STD-10
E WORKMANSHIP PER EG&G STD A900020

DRAWN	O. FERNANDEZ	
CHECKED		
DESIGNER		
ENGINEER	R. SLICE	
PROJ. ENG		

PROJECT APPROVAL

FINISH SPECS

EG&G LOS ALAMOS DIVISION

EG&G, INC. P.O. BOX 809, LOS ALAMOS, NEW MEXICO 87544

ASSY, SHIFT REGISTER

NEUTRON COUNTER II

CALC. WT.	CODE IDENT NO.	SIZE	DWG. NO.	REV
		C	C200735	B

DO NOT SCALE THIS DWG | SCALE: 1/1 | SHEET 1 OF 1

REVISIONS				
LTR	ZONE	DESCRIPTION	DATE	APPR
A	C1	ADDED J5/P5-B10 & P6/J6-A10		
B	B1	ADDED .01/50 CAPS AT SW1 & SW3	5-9-79	S.B
C	B2	C22 WAS 100 pFd	10/4/79	RBC

REAR PANEL — M.B. — J5 P5 — +5V — R1 10K — S.R. IN — J17 — P10 — J10 — SW10 EXT / INT — DISC OUT — J18 — P9 — J9 — ANALOG BD. P4 J4 — 1/4 5E — 1/4 74LS08 INPUT BUFFER — 470 R2 — 1/4 6E 74LS00 — LO CLR — +5V

INPUT SYNCHRONIZER 1ST STAGE 74LS74 — 1/2 7E — 68 PF C5 — 7A14

INPUT SYNCHRONIZER 2ND STAGE 74LS74 — 1/2 7E — 9D2 CK — +5V — TA2

V4 74LS00 INPUT SYNCH GATE — 1/4 6E — 9D6 CK — 1/2

68PF — 8E 1.1K — 8D 1/6 MH0026 DATA LEVEL SHIFTER — 4E6 — TA4

1/4 74LS08 6D10 E&A CLOCKED GATE — CK 1/2+ 250ns — 1/4 5E — TB5 — 4B9 — 8A2

1/4 74LS08 INTERROGATE START/STOP GATE — TB3

8D9 Ø1 — Ø2 8D11 — TB1

R6 3K — IN 7C 2804PC STAGE 1 "A" S.R. — VCC +5V — VDD -5V — R5 4.7K — IN 7C 2804PC STAGE 2 "A" S.R. — R4 3K

μP M.B. — P6 J6 B10 B10 — J5 P5 A10 A10 — P6 J6 A10 A10 — J5 P5 B10 B10

8A4

TB4 — 5E5 CK 1/2+ 250ns — 1/4 5E — TB7 — 6B9 — 74LS08 "A" CLOCKED GATE

F.P. M.B. — P3 J3 — J5 P5 — N/C — B30 B30 — 9B 10K — 1/2 10E 74123 B2 DEAD TIME — CLR CORRECT. — A2 R2EXT. C2EXT — C7 — R8 680PF — 2K — R9 50K — +5V

TBG — 1/2 9E 74LS107 INHIBITED INHIBIT TIMING FLIP FLOP — J K CLR CLK — 1/2 9E 74LS107 CK ÷2 TIMING FLIP FLOP

8C E/I RST MK5009 DIVIDED BY N — -V +V 2⁰ 2¹ 2² PM VDD 2³ — -12V — +5V

8B E/I RST MK5009 IN DIVIDE BY N — 10E13 HI CLR. — LOAD 9C CLR — CLK1 74LS196 DIVIDE BY N — CLK2 — LO CLR

1/4 11C Q 74LS279 START/STOP INV — R S

11D 4 MHZ CLK VECTRON C02388 — +5V

9B 10K ×4 — +5V

P5 J5 M.B. — J3 P3 F.P. — B26 B26 — A26 A26 — B27 B27 — A27 — 17 17 — 4 4 — 18 18 — 5 5 — FRONT PANEL SW9B — "TIME" (EXPON.)

Ø2 7C6 — Ø1 7C10 — SECK 10D12 — CK 7B3 — CK 1/2 6E10 — CK 1/2 +150 nS 6E13 — CK 1/2 +250 nS 5E5 — CK 1/2 +350 nS 6E1

1/2 10D CLR J K 74LS107 1ST STAGE CLK DIV. — J K CLR 1/2 10D 74LS107 2ND STAGE CLK DIV.

MH0026 Ø2 LEVEL SHIFTER — 1/2 8D — 1/4 9D 74LS08 Ø2 GATE — 100 — 270PF — 8E — MH0026 Ø1 LEVEL SHIFTER — 74LS08 Ø1 GATE — NPO — MH0026 SR.CLK LEVEL SHIFT.

SR.CLK GATE — 1/4 9D — 74LS08 CK 1/2 GATE

7D ECCTTLDM100 IN 100nS CLK 1/2 DELAY OUT — 6D ECCTTLDM250 IN 250nS CLK 1/2 DELAY OUT

ADB(I) AKB(I) 10C 74LS85 COMPARATOR (0) A=B(I) — A0 A1 A2 A3 — AKB — 200 PF C22

9B 10K ×4 — P5 J5 M.B. — J3 P3 F.P. — B28 B28 — A28 A28 — B29 B29 — A29 — 19 19 — 6 6 — 20 20 — 7 7 — FRONT PANEL SW9A — "TIME" (MANTISSA)

μP BD. — P5 J5 J6 P10 — A9 A9 — B9 B9

1/4 11C Q 74LS279 START/STOP F.F. — 9B 10K ×2 — P5 J5 M.B. — J3 P3 F.P. — A37 A37 — B37 B37 — 13 13 — 26 26 — STOP .01/50 SW3 — START .01/50 SW1 — FRONT PANEL

P6 J6 — A36 A36 — B36 B36

μP — M.B.

TRUTH / FUNCTION TABLES, FRONT PANEL THUMBWHEELS.

GATE LENGTH (μS)		SET TIME (MANTISSA)	SET TIME (EXPONENT)
C B A		8 4 2 1 ● = SW. CLOSED	8 4 2 1 ● = SW. CLOSED
4 2 1			
● ○ ○	3 → 2^3 = 8 μS	○ ○ ○ ○ 0	○ ○ ○ ○ 0
○ ● ●	4 → 2^4 = 16 μS	● ○ ○ ○ 1	● ○ ○ ○ 1
○ ● ○	5 → 2^5 = 32 μS	○ ● ○ ○ 2	○ ● ○ ○ 2
○ ○ ●	6 → 2^6 = 64 μS	● ● ○ ○ 3	● ● ○ ○ 3
○ ○ ○	7 = 2^7 = 128 μS	○ ○ ● ○ 4	○ ○ ● ○ 4
"●" = SW. CLOSED		● ○ ● ○ 5	● ○ ● ○ 5
GATE LENGTH = 2^N μS		○ ● ● ○ 6	○ ● ● ○ 6
		● ● ● ○ 7	● ● ● ○ 7
		○ ○ ○ ● 8	○ ○ ○ ● 8
		○ ● ○ ● 9	○ ● ○ ● 9
		SETS N IN COUNT TIME	SETS N IN COUNT TIME
		T = N X 10 SECONDS	T = M X 10^N SECONDS
		INOPERABLE W/MANTISSA = 0	

NOTES: UNLESS OTHERWISE SPECIFIED
1. RESISTORS ARE IN OHMS, 1/4 W, 5 %
2. CAPACITORS ARE IN MICROFARADS
3. LAST REFERENCE DESIGNATORS USED:

	IC's:
C21	8A
J10	9B
P10	11C
R9	11D
	10E

PART NO	DESCRIPTION	NOTE	ITEM NO.

LIST OF MATERIAL

DRAWN	L&M	4-78
CHECKED		
DESIGNER		
ENGINEER	R. SLICE	
PROJ. ENG		
PROJECT APPROVAL		
FINISH SPECS		

EG&G LOS ALAMOS DIVISION
EG&G, INC. P.O. BOX 809, LOS ALAMOS, NEW MEXICO 87544

SCHEMATIC DIAGRAM SHIFT REGISTER BD. NEUTRON COUNTER PHASE II

CALC. WT.	CODE IDENT NO.	SIZE	DWG. NO.	REV.
		D	D200734	C

DO NOT SCALE THIS DWG | SCALE: | SHEET 1 OF 2

H-DT-3	C200735	REF	00
CROSS INDEX	NEXT ASSEMBLY	REQD PER N/A	

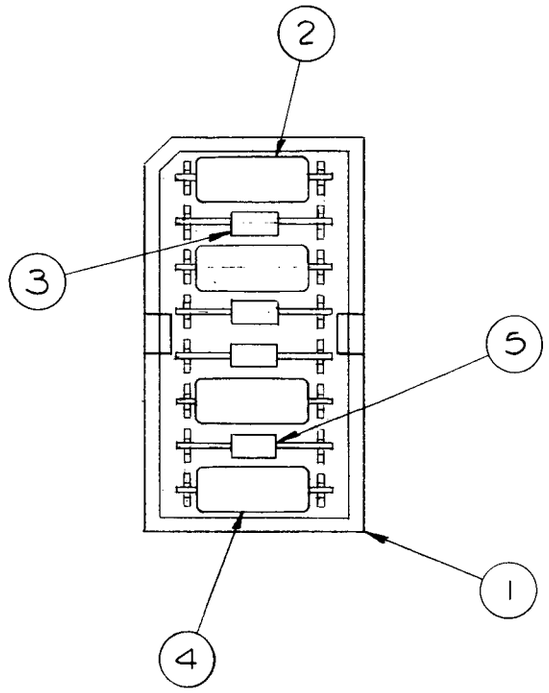
PART NO. D200734

QTY REQ'D PER ASSY

UNLESS OTHERWISE SPECIFIED
DIMENSION TOLERANCE
DECIMALS ± FRACTIONS ± ANGULAR ±

A. DRILLED HOLE TOLERANCE PER ANSI B87
B. REMOVE BURRS AND SHARP EDGES
C. WELDS: REMOVE LOOSE SCALE & SPATTER
D. SURFACE ROUGHNESS PER MIL-STD-10
E. WORKMANSHIP PER EG&G STD A9000020

REVISIONS				
LTR	ZONE	DESCRIPTION	DATE	APPR
A	B1	ITEM 4 WAS: 1W	10/16/79	PRC



QTY	PART NO.	SOURCE	DESCRIPTION	NOTE	ITEM NO.
1	8121-100C060-680K	ERIE	CAP, CER. MONO, 68P, 100V		5
1	CB1125	A/B	RESISTOR, 1.1K, 1/4W, 5%		4
3	8121-100C060-271K	ERIE	CAP, CER. MONO, 270 P, 100V		3
3	CB1015	A/B	RESISTOR, 100 Ω, 1/4 W, 5%		2
1	CA-16P-05	CKT ASSY	COMPONENT PLATFORM		1

LIST OF MATERIAL

H-DT-3	C200735	1	-00
CROSS INDEX	NEXT ASSEMBLY	REQ'D PER N/A	

PART NO. C200768 -4

QTY REQ'D PER ASS'Y -1

UNLESS OTHERWISE SPECIFIED

DIMENSION TOLERANCE

DECIMALS ± FRACTIONS ± ANGULAR ±

A. DRILLED HOLE TOLERANCE PER ANDI0387

B. REMOVE BURRS AND SHARP EDGES

C. WELDS: REMOVE LOOSE SCALE & SPATTER

D. SURFACE ROUGHNESS PER MIL-STD-10

E. WORKMANSHIP PER EG&G STD A900020

DRAWN	O. FERNANDEZ	
CHECKED		
DESIGNER		
ENGINEER	R. SLICE	
PROJ. ENG		

PROJECT APPROVAL

FINISH SPECS

EG&G LOS ALAMOS DIVISION

EG&G, INC. · P.O. BOX 809, LOS ALAMOS, NEW MEXICO 87544

ASSY, COMPONENT PLATFORM

NEUTRON COUNTER II

CALC. WT.	CODE IDENT NO.	SIZE	DWG. NO.	REV
			C200768	A

DO NOT SCALE THIS DWG | SCALE: 2/1 | SHEET 1 OF 1

REVISIONS				
LTR	ZONE	DESCRIPTION	DATE	APPR
A		NOMENCLATURE CHANGES		
B	A4	ADDED .01/50 CAP. AT SW2	5-7-79	S.B.

TA3 · TA1 · TA4 · TA5 · TA6 · TA7 · TB2 · 8E11 · SR CLOCK · 8D13 · 10E13 HI CLR · 11C5 · 8B3 · 8B4 · 7E10 · 11C6 LO CLR · 5E11 · 5E6 · 11C15 · 11C13 · 5D13 · 5D14 HI CLR · 4B1 LO CLR · 6D8 · 6D12 CK 1/2 +150 ns

3E 100K · PRE DELAY SR · 1E PREDELAY · BIT 1 · BIT 2 · BIT 3 · BIT 4 · BIT 5 · BIT 6

4E MC14557A R CE ABSEL CLK · 1/2 2E MC14517A Q64A GATE S.R. · 1/2 2E MC14517A Q64B GATE S.R. · 1/2 1D MC14517A GATE S.R. · 1/2 1D MC14517A GATE S.R.

5D 74LS192 TENS · 4D 74LS192 UNITS · UP/DOWN 4 COUNTERS

UP BD · M.B. · P6 J6 · J5 P5 · TIME MARK R+A > 100 A > 100

7A CD4049 SCALER SERIAL DATA BUFFER INVERTER

FRONT PANEL · F.P. · M.BD · START (SW1) · STOP (SW3) · FAULT (SW2)

8A 8097 LED & OUTPUT DRIVER

4C 82S83 Σ R+A TENS · 3C 82S83 Σ R+A ONES · 6C 82S83 Σ A TENS · 1C 82S83 Σ A ONES

4B 74LS174 R+A TENS LATCH · 3B 74LS175 R+A ONES LATCH · 6B 74LS174 A TENS LATCH · 1B 74LS175 A ONES LATCH

4A 70C97 R+A TENS TRISTATE BUFFER · 3A 70C97 R+A ONES TRISTATE BUFFER · 6A 70C97 A TENS TRISTATE BUFFER · 1A 70C97 A ONES TRISTATE BUFFER

1/4 11C 74LS279 FAULT STATUS · 1/4 11C 74LS279 · CLEAR ONE SHOT TRIGGERING F/F

1/2 10E 74123 CLEAR ONE SHOT · R3 33K · C8 2.2UF · RESET · SW2 .01/50

1/4 6E 74LS00 · UP COUNT STROBE GATE · DOWN COUNT STROBE

2D CD4049 COUNT LEVEL SHIFTER

3D 74LS151 · GATE LENGTH SELECTOR

9B 10 K Ω · FRONT PANEL SW8 "GATE"

J1 · TO DISPLAY BD. · UP BD.

R7 100K · C23 2.2 · C37 10 · C1,C2,C4,C6 C9-C21,C38-C41 .47 · C34 10 · C35 10 · C36 10

+12V · +5V · -5V · -12V · GND

PART NO	DESCRIPTION	NOTE	ITEM NO.

LIST OF MATERIAL

DRAWN	L.F.M.	4-21-78
CHECKED		
DESIGNER		
ENGINEER	R. SLICE	
PROJ. ENG		
PROJECT APPROVAL		

QTY REQ'D PER ASSY

UNLESS OTHERWISE SPECIFIED

DIMENSION TOLERANCE: DECIMALS ± · FRACTIONS ± · ANGULAR ±

A. DRILLED HOLE TOLERANCE PER ANDI0387

B. REMOVE BURRS AND SHARP EDGES

C. WELDS: REMOVE LOOSE SCALE & SPATTER

D. SURFACE ROUGHNESS PER MIL-STD-10

E. WORKMANSHIP PER EG&G STD A900020

FINISH SPECS

4-DT-3	C200735	REF 00
CROSS INDEX	NEXT ASSEMBLY	REQ'D PER N/A

PART NO. D200734

EG&G LOS ALAMOS DIVISION

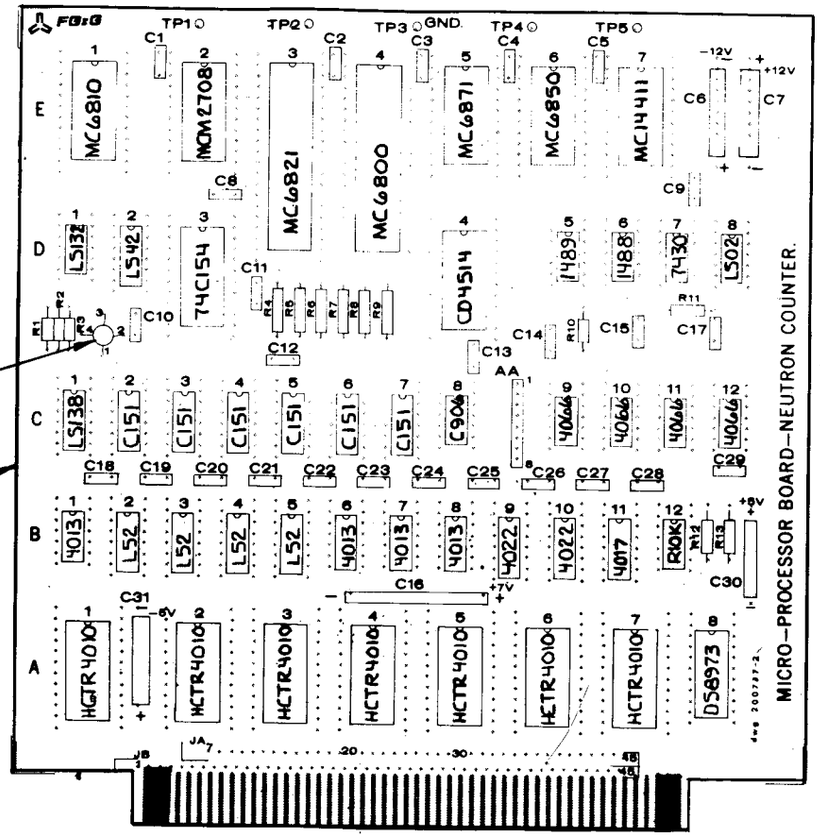
EG&G, INC. P.O. BOX 809, LOS ALAMOS, NEW MEXICO 87544

SCHEMATIC DIAGRAM SHIFT REGISTER BD. NEUTRON COUNTER PHASE-II

CALC. WT.	CODE IDENT NO.	SIZE	DWG. NO.	REV.
			D200734	B

DO NOT SCALE THIS DWG · SCALE: ~ · SHEET 2 OF 2

REVISIONS				
LTR	ZONE	DESCRIPTION	DATE	APPR
A	C3	11B WAS: 4066 12B WAS: 4066	5-9-79	S.S.



NOTES: UNLESS OTHERWISE SPECIFIED:
1. FOR SCHEMATIC DIA. SEE DWG D200741
2. REFERENCE DESIGNATORS FOR ITEM 7 ARE C1,C2,C5,C8,C9,C12-C15,C17-C29

ITEM NO.	DESCRIPTION	SOURCE	PART NO.	DESIG.	NOTE	QTY
41	DECODER 3TO8	TI	SN74LS138	1C		1
40	QUAD NAND	TI	SN74LS132	1D		1
39	DECODER, BCD TO DECIMAL	TI	SN74LS42	2D		1
38	8 INPUT NAND	TI	SN.7430	7D		1
37	QUAD NOR	TI	SN74LS02	8D		1
36	HEX BUFFER	NATL	MM74C906	8C		1
35	DECODER, 4 TO 16	NATL	MM74C154	3D		1
34	DATA SELECTOR, 8 LINE	NATL	MM74C151	2C-7C		6
33	PROM, 1024X8	MOTOROLA	MCM2708	2E		1
32	BAUD RATE GENERATOR	MOTOROLA	MC14411	7E		1
31	2 PHASE CLOCK	MOTOROLA	MC6871	5E		1
30	ACIA	MOTOROLA	MC6850	6E		1
29	PIA	MOTOROLA	MC6821	3E		1
28	RAM, 128 X8	MOTOROLA	MC6810	1E		1
27	MICROPROCESSOR	MOTOROLA	MC6800	4E		1
26	LINE RECEIVER	MOTOROLA	MC1489	5D		1
25	LINE DRIVER	MOTOROLA	MC1488	6D		1
24	DECADE COUNTER	HUGHES	HCTR4010	1A-7A		7
23	9 DIGIT LED DRIVER	NATL	DS8973	8A		1
22	TRISTATE SYNCRONOUS COUNTER	NATL	DM75LS2	2B-5B		4
21	DECODER, 4TO 16	RCA	CD4514BD	4D		1
20	QUAD BILATERAL SWITCH	RCA	CD4066AD	9C-12C		4
19	COUNTER, ÷8	RCA	CD4022AD	9B 10B		2
18	DECADE COUNTER	RCA	CD4017AD	11B		1
17	DUAL 'D' FLIPFLOP	RCA	CD4013AD	18,6B-8B		4
16	RESISTOR, 10M, 1/4W, 5%	A/B	CB1065	R2		1
15	RESISTOR, 100K, 1/4W, 5%	A/B	CB1045	R4,5,12		3
14	RESISTOR, 2.7K, 1/4W, 5%	A/B	CB2735	R10		1
13	RESISTOR, 10K, 1/4W, 5%	A/B	CB1035	R11,R13		2
12	RESISTOR, 5.1K, 1/4W, 5%	A/B	CB5125	R3		1
11	RESISTOR, 3.3K, 1/4W, 5%	A/B	CB3325	R6-R9		4
10	RESISTOR, 200Ω, 1/4 W, 5%	A/B	CB2015	R1		1
9	CAP, TANT ELECT, 10μF, 35V	SPRAGUE	150D106X9035R2	C6,C7		2
8	CAP, TANT ELECT, 10μF, 20V	SPRAGUE	150D106X9020B2	C14,30,31		3
7	CAP, CER MONO, .47μF, 100V	ERIE	8131-100-651-474M		2	22
6	CAP, CER MONO, .047μF, 100V	ERIE	8121-100-651-473M	C10		1
5	CAP, CER MONO, .01μF, 100V	ERIE	8121-100-651-103M	C3,C4		2
4	CAP, CER MONO, 1500PF, 100V	ERIE	8121-100-651-152M	C11		1
3						
2						
1	CKT BD, MULTIWIRE, μP	EG&G	C200737-01			1

LIST OF MATERIAL

50	SOCKET, DIP, 40 PIN		AUGAT	740-AG-4D	2	
49	SOCKET, DIP, 24 PIN		AUGAT	724-AG-4D	14	
48	SOCKET, DIP, 22 PIN		AUGAT	722-AG-2D	1	
47	SOCKET, DIP, 16 PIN		AUGAT	716-AG-2D	15	
46	SOCKET, DIP, 14 PIN		AUGAT	714-AG-2D	15	
45	TERMINAL, TURRET	TP1-5	CAMBION	2043-3	5	
44	FET, SWITCH		MOTOROLA	MFE-3002	1	
43	R-PAK, 10K	12B	BECKMAN	899-1-R10K	1	
42	R-PAK, 100K	AA	BECKMAN	764-1-R100K	1	
ITEM	DESCRIPTION	DESIG	SOURCE	PART NO.	QTY	

H-DT-3 | E200794 | 1 | -00
CROSS INDEX | NEXT ASSEMBLY | REQD PER N/A

PART NO. C200741

QTY REQ'D PER ASS'Y

UNLESS OTHERWISE SPECIFIED
DIMENSION TOLERANCE
DECIMALS ± FRACTIONS ± ANGULAR ±
A DRILLED HOLE TOLERANCE PER ANDI0387
B REMOVE BURRS AND SHARP EDGES
C WELDS REMOVE LOOSE SCALE & SPATTER
D SURFACE ROUGHNESS PER MIL-STD-10
E WORKMANSHIP PER EG&G STD A900020

FINISH SPECS

DRAWN	P. RICE	6-12-78
CHECKED		
DESIGNER		
ENGINEER		
PROJ ENG		
PROJECT APPROVAL		

EG&G LOS ALAMOS DIVISION
EG&G, INC. P.O. BOX 809, LOS ALAMOS, NEW MEXICO 87544

ASSY, MICROPROCESSOR

NEUTRON COUNTER II

CALC. WT.	CODE IDENT NO.	SIZE	DWG. NO.	REV
			C200742	A

DO NOT SCALE THIS DWG | SCALE 1/1 | SHEET 1 OF 1

REVISIONS				
LTR	ZONE	DESCRIPTION	DATE	APPR
A		SOME PINS ON J2 WERE MISLABELED		

SWITCHING, SELECTOR

ELECTRONIC SWITCH

LIP/CALCULATOR LOGIC LEVEL BUFFER

+5V

8C 74C906

3E13 12 → 13(8)

3E12 10 → 11(4)

3E11 6 → 5(2)

3E10 4 → 3(1)

3D9 2 → 1

3D10 8 → 9

7

AA 100K

+7V

4D CD4514 DATA SELECTOR

STO(F) 15
ENT(E) 16
CLX(D) 13
C 14

22 A3(8)
21 A2(4)
3 A1(2)
2 A0(1)
1 E
23 $\overline{E}$

12

+7V

CD4066 10C SWITCH SET #2

B 19
A 20
9 17
8 18

13 EB
12 EA
6 E9
5 EB

2 K16
1 DS12
10 K18
11 DS7
9 K16
8 DS18
3 K16
4 DS1

7

+7V

CD4066 11C SWITCH SET #3

7 4
6 5
5 6
4 7

13 E7
12 E6
6 E5
5 E4

2 K16
1 DS13
10 K17
11 DS18
9 K17
8 DS1
3 K17
4 DS13

7

+7V

CD4066 12C SWITCH SET #4

3 8
2 10
1 9
0 11

13 E3
12 E2
6 E1
5 E0

2 K18
1 DS18
10 K18
11 DS1
9 K18
8 DS13
3 K15
4 DS9

7

+7V

CD4066 SWITCH SET #1

13 EF (STO)
12 EE (ENT)
6 ED (CLX)
5 EC (N/U)

2 K16
1 DS16
10 K18
11 DS14
9 K15
8 DS24
3 N/U
4 N/U

7

MICROPROSSOR BOARD — MOTHER BOARD — REAR PANEL

P6	J6	J2	P2	J14
A37	A37	1	1	8
A38	A38	2	2	15
A39	A39	3	3	7
A40	A40	4	4	14
A41	A41	5	5	6
A42	A42	6	6	13
A43	A43	7	7	5
A44	A44	8	8	12
B44	B44	21	21	4
B43	B43	20	20	11
A49	A49	13	13	3
B41	B41	18	18	10
B40	B40	17	17	2
B39	B39	16	16	9
B38	B38	15	15	1

+7V

C16 10 20V

NOTES: UNLESS OTHERWISE SPECIFIED:
1. RESISTORS ARE IN OHMS, 1/4 W, 5%
2. CAPACITORS ARE IN MICROFARADS
3. LAST REFERENCE DESIGNATORS USED:

C31	IC'S: 8A
J14	12E
P7	12C
R13	8D
SW11	7E
TP5	

CALCULATOR INTERFACE

PART NO	DESCRIPTION	NOTE	ITEM NO.

LIST OF MATERIAL

DRAWN	L&M	4-78
CHECKED		
DESIGNER		
ENGINEER	R. SLICE	
PROJ. ENG.		
PROJECT APPROVAL		
FINISH SPECS		

QTY REQ'D PER ASSY

UNLESS OTHERWISE SPECIFIED
DIMENSION TOLERANCE
DECIMALS ± FRACTIONS ± ANGULAR ±

A. DRILLED HOLE TOLERANCE PER ANDI0387
B. REMOVE BURRS AND SHARP EDGES
C. WELDS: REMOVE LOOSE SCALE & SPATTER
D. SURFACE ROUGHNESS PER MIL-STD-10
E. WORKMANSHIP PER EG&G STD A900020

CROSS INDEX	NEXT ASSEMBLY	REQ'D PER N/A
H-DT-3	C200742	REF 00

PART NO. D200741

EG&G LOS ALAMOS DIVISION
EG&G, INC. P.O. BOX 809, LOS ALAMOS, NEW MEXICO 87544

SCHEMATIC DIAGRAM
MICROPROSSOR BOARD
NEUTRON COUNTER II

CALC. WT.	CODE IDENT NO.	SIZE	DWG. NO.	REV.
			D200741	A

DO NOT SCALE THIS DWG | SCALE: ~ | SHEET 1 OF 4

REVISIONS				
LTR	ZONE	DESCRIPTION	DATE	APPR
A		NOMENCLATURE UPDATES		

A>100

MULIPLEX OSC. INPUT

TOTALS INPUT

TOTALS

TIME

R+A>100

R+A>100 INPUT

TIMER INPUT

PART NO	DESCRIPTION	NOTE	ITEM NO.

LIST OF MATERIAL

DRAWN	L.F.M	4-21-78
CHECKED		
DESIGNER		
ENGINEER	R. SLICE	
PROJ. ENG.		
PROJECT APPROVAL		

QTY REQ'D PER ASSY

UNLESS OTHERWISE SPECIFIED

DIMENSION TOLERANCE

DECIMALS ± FRACTIONS ± ANGULAR ±

A. DRILLED HOLE TOLERANCE PER ANDI0367

B. REMOVE BURRS AND SHARP EDGES

C. WELDS: REMOVE LOOSE SCALE & SPATTER

D. SURFACE ROUGHNESS PER MIL-STD-10

E. WORKMANSHIP PER EG&G STD A900020

FINISH SPECS

CROSS INDEX	NEXT ASSEMBLY	REQ'D PER N/A
H-D1-3	C200742	REF DD

PART NO. D200741

EG&G LOS ALAMOS DIVISION

EG&G, INC. P.O. BOX 809, LOS ALAMOS, NEW MEXICO 87544

SCHEMATIC DIAGRAM
MICROPROCESSOR BD.
NEUTRON COUNTER II

CALC. WT.	CODE IDENT NO.	SIZE	DWG. NO.	REV
			D200741	A

DO NOT SCALE THIS DWG | SCALE: ~ | SHEET 2 OF 4

REVISIONS				
LTR	ZONE	DESCRIPTION	DATE	APPR
A		NOMENCLATURE UPDATES		
B	C4	ADDED .01/50 CAP AT SW5	5-9-79	SB.

SHIFT REGISTER BOARD — MOTHER BD — MICROPROSSOR BD

P5 J5 — J6 P6

P5	J5	J6	P6
B10	B10	A10	A10
B9	B9	A9	A9
A9	A9	B9	B9
A37	A37	A36	A36
B36	B36	A35	A35
B37	B37	B36	B36
		A32	A32
		B32	B32

READ OUT, RECYCLE, START, RESET, STOP, FAULT, TIME OUT, RUN

FRONT PANEL — M.B.

P3 J3

P3	J3	
25	25	SW4 RECYCLE/MANUAL
10	10	SW5 READ OUT
13	13	SW3 STOP
12	12	SW2 RESET
26	26	SW1 START

.01/50

+5V — R4 100K — R5 100K

2C 74C151 SELECTOR G (STATUS)
ST C B A
D7 D6 D5 D4 D3 D2 D1 D0 — 12 13 14 15 1 2 3 4 — 5

1C 74LS138 SELECTOR F (OPERATION)
Y7 Y6 Y5 Y4 Y3 Y2 Y1 Y0 — 7 9 10 11 12 13 14 15
+5V — 6 — G1; 4 — G2A; G2B — 5
C B A — 3 2 1

START, RESET, STOP

C11 1500 PF

3C 74C151 SELECTOR E (STROBE)
ST C B A
D7 D6 D5 D4 D3 D2 D1 D0 — 12 13 14 15 1 2 3 4 — 6 W
A1 A2 A3 A4 A5 — 11B2 11B4 6A8 6A6 6A9

4C 74C151 SELECTOR D (STROBE)
A6 A7 A8 A9 A10 R1 R2 R3 — 12 13 14 15 1 2 3 4 — 6
6A7 7A8 7A6 7A7 7A7 11B7 11B0 6A8

5C 74C151 SELECTOR C (STROBE)
R4 R5 R6 R7 R8 R9 R10 C1 — 12 13 14 15 1 2 3 4 — 6
6A6 6A9 6A7 5A8 5A6 5A9 5A7 11B1

6C 74C151 SELECTOR B (STROBE)
C2 C3 C4 C5 C6 C7 C8 C9 — 12 13 14 15 1 2 3 4 — 6
11B5 6A8 6A6 6A9 2A8 6A6 6A8 2A9

7C 74C151 SELECTOR A (STROBE)
C10 T1 T2 T3 T4 T5 T6 — 12 13 14 15 1 2 3 4 — 6
2A7 11B6 11B9 3A8 3A6 3A9 3A7

9B13

74LS02 BLANKING DRIVER — 8D — 8 9 — 10

M.B. — DISPLAY DRIVER BD

P6 J6 — J1 P1

P6	J6	J1	P1
B15	B15	18	18

8D — 5 6 — 4 → 3E9

74LS02 FLAG MULTIPLEX STROBE GATE

7D 7430 INHIBIT/MULTIPLEX STROBE GATE — 8

R11 10K — +5V

11 10 6 5 4 3 2 1

3E12, 3E11, 3E10

8C2 → 9

8C8 → 10

3D 74C154 INTERFACE CHIP SELECTOR
6 5 4 3 2 1 0 — 8 — 9
D C B A — 20 21 22 23
18 19

3E16, 3E15, 3E14, 3E13

+5V — C30 10 20V — C31 C4 .01 — .47 C1,C2,C5,C8 C9 C12-C15 C17-C29

+12V — C7 10 35V — -12V — C6 10 35V — -5V — C31 10 20V

DR. BD — M.B.

P1 J1 — J6 P6

P1	J1	J6	P6	
36	36	B24	B24	7C14, T2
28	28	B20	B20	7C13, T1
48	48	B30	B30	6C12, C2
38	38	B25	B25	5C9, C1
33	33	A23	A23	4C3, R2
45	45	A29	A29	4C2, R1
13	13	A13	A13	3C1, A2
25	25	A19	A19	3C15, A1

DC/DC — M.B.

P7 J7 — J6 P6

P7	J7	J6	P6	
2	2	A1	A1	→ -5V
3	3	B1	B1	
15	15	A2	A2	
16	16	B2	B2	
		A3	A3	
		B3	B3	
10	10	A4	A4	→ -5V
23	23	B4	B4	
8	8	A46	A46	→ -12V
21	21	B46	B46	
9	9	A47	A47	→ +12V
22	22	B47	B47	
4	4	A48	A48	
5	5	B48	B48	
17	17	A49	A49	
18	18	B49	B49	
		A50	A50	
		B50	B50	

PART NO	DESCRIPTION	NOTE	ITEM NO.

LIST OF MATERIAL

DRAWN	L&M	4-21-78
CHECKED		
DESIGNER	R. SLICE	
ENGINEER		
PROJ. ENG		
PROJECT APPROVAL		

EG&G LOS ALAMOS DIVISION
EG&G, INC. P.O. BOX 809, LOS ALAMOS, NEW MEXICO 87544

SCHEMATIC DIAGRAM MICROPROCESSOR BD. NEUTRON COUNTER II

CALC. WT.	CODE IDENT NO.	SIZE	DWG. NO.	REV.
		D	D200741	B

DO NOT SCALE THIS DWG | SCALE: ~ | SHEET 3 OF 4

QTY REQ'D PER ASSY			
UNLESS OTHERWISE SPECIFIED			
DIMENSION TOLERANCE			
DECIMALS ±	FRACTIONS ±	ANGULAR ±	
A. DRILLED HOLE TOLERANCE PER ANDI0367			
B. REMOVE BURRS AND SHARP EDGES			
C. WELDS: REMOVE LOOSE SCALE & SPATTER			
D. SURFACE ROUGHNESS PER MIL-STD-10			
E. WORKMANSHIP PER EG&G STD A9000220			

H-DT-3	C200742	REF	DO
CROSS INDEX	NEXT ASSEMBLY	REQ'D PER N/A	

PART NO. D200741

FINISH SPECS

REVISIONS				
LTR	ZONE	DESCRIPTION	DATE	APPR
A		NOMENCLATURE UPDATES		
B	B1	ADDED CIRCUIT FROM 3E PIN 19		
C	B1	J3/P3 PIN 23 WAS PIN 24	10/30/79	DRC

5E MC6871A MPU CLK 921.6 KHZ — Ø2 TTL Ø1 Ø2 — 2XFC — R9 3.3K — +5V

7E MC 14411 BAUD RATE GENERATOR — VCC B RST IN GND A — F9

5D MC1489 LINE RECIEVER — R10 27K — -12V

6D MC1488 LINE DRIVER — -12V +12V

6E MC6850 ACIA — CS0 CS1 CS2 E RxCLK RxD TxCLK D0 D1 D2 D3 D4 D5 D6 D7 R/W RS VSS VDD DCD CTS — Tx

P6 J6 J2 P2 — B45 B45 22 22 — A45 A45 9 9

REAR PANEL

J13 P13 — 1:1 2:2 3:3 4:4 5:5 6:6 7:7 8:8 9:9 10:10 11:11 12:12 13:13 14:14 15:15 16:16 17:17 18:18 19:19 20:20 21:21 22:22 23:23 24:24 25:25

TO GND VIA J14-3

TI 700 SERIES TERMINAL (OR OTHER RS-232 COMPATIBLE DEVICE)

4E MC 6800 µP — Ø2 DBE Ø1 VMA R/W RST D0-D7 A0-A15 VCC VSS VSS TSC — R8 3.3K R7 3.3K R6 3.3K

1D 1/4 74LS132

4-2D 74LS42 CHIP SEL. VCC GND

2E 2708 PROM — D0-D7 A0-A9 VCC VDD VBB VSS CS

1E MCG810 RAM — D0-D7 A0-A6 R/W CS1 CS2 CS3 CS4 CS5 GND VCC

3E MC6821 P.I.A. — D0-D7 R/W RST RS0 RS1 CS1 CSØ CS2 VCC VSS CB2 CB1 PB7-PB0 CA2 CA1 PA7-PA0

- 16 (1C40) → 3D20
- 15 (1C20) → 3D21
- 14 (1C10) → 3D22
- 13 (1C8) → 3D23, 8C12
- 12 (1C4) → 7C9, 8C10
- 11 (1C2) → 7C10, 8C6
- 10 (1C1) → 7C11, 8C4
- PA0 "1" → 2B6
- PA1 "2" → 2B5
- PA2 "4" → 2B3
- PA3 "8" → 2B4
- PA4, PA5 → +5V
- PA6, PA7 → 8D4 INTERRUPT LINE

M.B. P6 J6 J3 P3 — 8D 1/4 74LS02 — B42 B42 23 23 — "READOUT" → +5V — FRONT PANEL

µP RESET SW11 — P2 J2 J6 P6 — B37 B37 — REAR PANEL

R3 5K — R1 200Ω — C10 .047µF — R2 10M — 1D 1/4 74LS132 — MFE3002

PART NO	DESCRIPTION	NOTE	ITEM NO.

LIST OF MATERIAL

DRAWN	C.F.M.	4-78
CHECKED		
DESIGNER		
ENGINEER	R. SLICE	
PROJ. ENG		
PROJECT APPROVAL		

EG&G LOS ALAMOS DIVISION
EG&G, INC. P.O. BOX 809, LOS ALAMOS, NEW MEXICO 87544

SCHEMATIC DIAGRAM
MICROPROCESSOR BD
NEUTRON COUNTER II

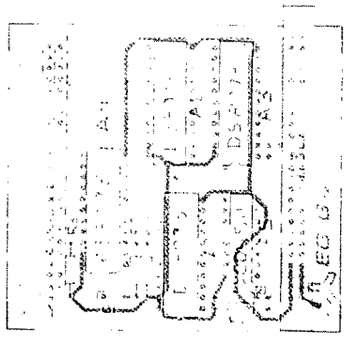
CALC. WT.	CODE IDENT NO.	SIZE	DWG. NO.	REV
			D200741	C

DO NOT SCALE THIS DWG | SCALE: ~ | SHEET 4 OF 4

QTY REQ'D PER ASSY			
UNLESS OTHERWISE SPECIFIED			
DIMENSION TOLERANCE			
DECIMALS ±	FRACTIONS ±	ANGULAR ±	
A. DRILLED HOLE TOLERANCE PER ANDI0367			
B. REMOVE BURRS AND SHARP EDGES			
C. WELDS: REMOVE LOOSE SCALE & SPATTER			
D. SURFACE ROUGHNESS PER MIL-STD-10			
E. WORKMANSHIP PER EG&G STD A900020			
FINISH SPECS			

44-07-3	C200742	REF	00
CROSS INDEX	NEXT ASSEMBLY	REQ'D PER N/A	
PART NO. D200741			

REVISIONS				
LTR	ZONE	DESCRIPTION	DATE	APPR
B		MOVED J30 UP.100 / REDRAWN		



NOTES: UNLESS OTHERWISE SPECIFIED:
1. FOR SCHEMATIC DIA. SEE DWG NO D200753
2. MOUNT FAR SIDE.
3. MOUNT WITH BODY OFFSET TOWARD CENTER OF BOARD

4	722-AG-2D	AUGAT	SOCKET, 22PIN DIP			12
1	716-AG-2D	AUGAT	SOCKET, 16PIN DIP			11
4	DS8973	NATL	9BIT DRIVERS			10
1	CD4511	RCA	BCD TO 7 SEGMENT DECODER	A5		9
1	CB4735	A/B	RESISTOR, 47K, 1/4W, 5%.	R5		8
3	CB1035	A/B	RESISTOR, 10K, 1/4W, 5%.	R1,2,4		7
1	CB1025	A/B	RESISTOR, 1K, 1/4W, 5%	R3		6
1	8121H100-W5R0-222K	ERIE	CAP. CER MONO 2200PF 100V	C1		5
						4
2	SB-25-100	ROB/NUG	HEADER		2,3	3
1	3496-2002	3M	HEADER, 50 PIN			2
1	B200754-00	EG&G	PWB, DRIVER			1
C200755-00	PART NO.	SOURCE	DESCRIPTION	DESIG.	NOTE	ITEM NO.

LIST OF MATERIAL

DRAWN	P. RICE	6-19-78
CHECKED		
DESIGNER	P. RICE	
ENGINEER	R. SLICE	
PROJ. ENG		
PROJECT APPROVAL		

EG&G LOS ALAMOS DIVISION
EG&G, INC. P.O. BOX 809, LOS ALAMOS, NEW MEXICO 87544

ASSY, DRIVER BOARD

NEUTRON COUNTER II

CALC. WT.	CODE IDENT NO.	SIZE	DWG. NO.	REV
			C200755	B

DO NOT SCALE THIS DWG | SCALE: 1/1 | SHEET 1 OF 1

H-DT-3	C200795	1	-00
CROSS INDEX	NEXT ASSEMBLY	REQ'D PER N/A	

PART NO. C200755

QTY REQ'D PER ASS'Y

UNLESS OTHERWISE SPECIFIED

DIMENSION TOLERANCE

DECIMALS	FRACTIONS	ANGULAR
±	±	±

A. DRILLED HOLE TOLERANCE PER ANDI0387
B. REMOVE BURRS AND SHARP EDGES
C. WELDS: REMOVE LOOSE SCALE & SPATTER
D. SURFACE ROUGHNESS PER MIL-STD-10
E. WORKMANSHIP PER EG&G STD A900020

FINISH SPECS

REVISIONS				
LTR	ZONE	DESCRIPTION	DATE	APPR
A		SWITCHED J30 PINS 1,3,5,7 WITH 2,4,6,8		
B		ADDED BUBBLES TO DS8973'S		

TO MOTHER BOARD J1

DRIVER BOARD

DISPLAY BOARD

NOTES: UNLESS OTHERWISE SPECIFIED:
1. RESISTORS ARE IN OHMS, 1/4W, 5%
2. 7-SEGMENT LEDS ARE HP 5082-7433
3. LAST REFERENCE DESIGNATORS USED:
C1
R5
J30
P30
U5

PART NO	DESCRIPTION	NOTE	ITEM NO.

LIST OF MATERIAL

DRAWN	S. SCARLOTT	5-2-78
CHECKED		
DESIGNER		
ENGINEER	R. SLICE	
PROJ. ENG.		
PROJECT APPROVAL		

EG&G LOS ALAMOS DIVISION

EG&G, INC. P.O. BOX 809, LOS ALAMOS, NEW MEXICO 87544

SCHEMATIC, DISPLAY & DRIVER BOARDS

NEUTRON COUNTER II

CALC. WT.	CODE IDENT NO.	SIZE	DWG. NO.	REV.
			D200753	B

DO NOT SCALE THIS DWG | SCALE: NONE | SHEET 1 OF 1

CROSS INDEX	NEXT ASSEMBLY	REQ'D PER N.A.
H-DT-3	C200755	REF 00
H-DT-3	C200752	REF 00

PART NO. D200753

QTY REQ'D PER ASSY

UNLESS OTHERWISE SPECIFIED

DIMENSION TOLERANCE: DECIMALS ± | FRACTIONS ± | ANGULAR ±

A. DRILLED HOLE TOLERANCE PER ANDI0387

B. REMOVE BURRS AND SHARP EDGES

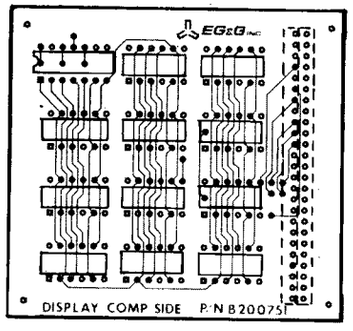
C. WELDS: REMOVE LOOSE SCALE & SPATTER

D. SURFACE ROUGHNESS PER MIL-STD-10

E. WORKMANSHIP PER EG&G STD A800020

FINISH SPECS

REVISIONS				
LTR	ZONE	DESCRIPTION	DATE	APPR
A		ITEM 2 WAS: HEADER 15: SOCKET	5-9-79	S.B.



NOTES: UNLESS OTHERWISE SPECIFIED:
1. FOR SCHEMATIC DIA. SEE DWG D200753
2. MOUNT FAR SIDE
3. DISCARD UNUSED PINS
4. MOUNT WITH BODY OFF SET TOWARDS CENTER OF BOARD

PART NO.	SOURCE	DESCRIPTION	DESIG.	NOTE	ITEM NO.
5082-7433	H.P.	LED DISPLAY			6
899-3-R100	BECKMAN	R-PACK, 100 Ω			5
714-AG-2D	AUGAT	LEAD SOCKET, 14 PIN		3	4
714-AG-2D	AUGAT	LEAD SOCKET, 14 PIN			3
SB-25-100	ROB/NUG	SOCKET		2,4	2
C200751-00	EG&G	PWB, DISPLAY			1

LIST OF MATERIAL

C200752-00

DRAWN	S. SCARLOTT	4-26-79
CHECKED		
DESIGNER		
ENGINEER	R. SLICE	
PROJ ENG		
PROJECT APPROVAL		

FINISH SPECS

QTY REQ'D PER ASS'Y →
UNLESS OTHERWISE SPECIFIED
DIMENSION TOLERANCE
DECIMALS ± FRACTIONS ± ANGULAR ±
A DRILLED HOLE TOLERANCE PER ANDI0387
B REMOVE BURRS AND SHARP EDGES
C WELDS REMOVE LOOSE SCALE & SPATTER
D SURFACE ROUGHNESS PER MIL-STD-10
E WORKMANSHIP PER EG&G STD A900020

CROSS INDEX	NEXT ASSEMBLY	REQ'D PER N/A	
H-DT-3	C200795	1	00

PART NO. C200752 →

EG&G LOS ALAMOS DIVISION

EG&G, INC. · P.O. BOX 809, LOS ALAMOS, NEW MEXICO 87544

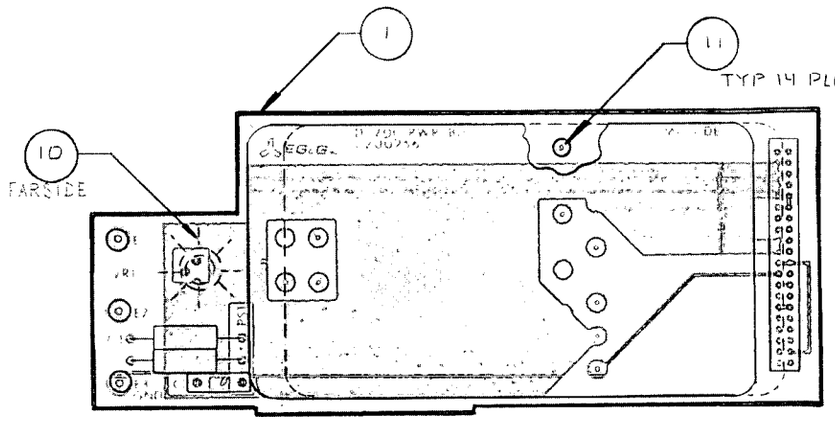
ASSY, DISPLAY BOARD

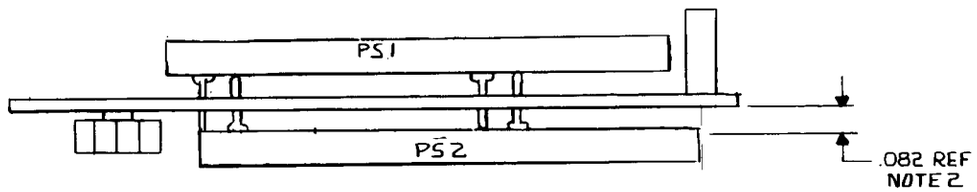
NEUTRON COUNTER II

CALC. WT.	CODE IDENT NO.	SIZE	DWG. NO.	REV
			C200752	A

DO NOT SCALE THIS DWG | SCALE: 1/1 | SHEET 1 OF 1

REVISIONS				
LTR	ZONE	DESCRIPTION	DATE	APPR
A		REDESIGNED/REDRAWN		





NOTES: UNLESS OTHERWISE SPECIFIED:
1. FOR SCHEMATIC DIAGRAM SEE DWG D200758
2. INSTALL ITEM 11 WITH FIXTURE B200763 TO OBTAIN CORRECT SOCKET PROTRUSION OF .082 ON BOTH SIDES OF P.W.B.

REF	PART NO.	SOURCE	DESCRIPTION	DESIG.	NOTE	ITEM NO.
14	380598-1	AMP	SOCKET, PIN		2	11
1	207-CB	WAKEFIELD	HEATSINK			10
1	LM220H-5.0	NATL	REGULATOR, VOLTAGE	VR1		9
1	WC(T-40)T15/165U	STEPHENS ARNOLD	POWER SUPPLY, DC CONVERTER	PS2		8
1	WC(T-40)T12/165U	STEPHENS ARNOLD	POWER SUPPLY, DC CONVERTER	PS1		7
1	3495-2003	3M	CONNECTOR, 40PIN HEADER	J11		6
3	1310C	USECO	TERMINAL, BIFURCATED	E1-E3		5
1	5C25U225X0050C3	SPRAGUE	CAP, CER. MONO, 2.2μ, 50V	C2		4
2	146D826X9050J2	SPRAGUE	CAP, TANT. ELECT., 82μF, 50V	C1, C3		3
REF	B200763	EG&G	FIXTURE, PIN SPACING		2	2
1	C200756-00	EG&G	PWB, DC/DC CONVERTOR			1

LIST OF MATERIAL

C200757-00

DRAWN	S. SCARLOTT	6-878	
CHECKED			
DESIGNER	W SHAW		
ENGINEER	R. SLICE		
PROJ. ENG			

PROJECT APPROVAL

FINISH SPECS

QTY REQ'D PER ASS'Y

UNLESS OTHERWISE SPECIFIED

DIMENSION TOLERANCE

DECIMALS	FRACTIONS	ANGULAR
±	±	±

A. DRILLED HOLE TOLERANCE PER ANDI0387
B. REMOVE BURRS AND SHARP EDGES
C. WELDS: REMOVE LOOSE SCALE & SPATTER
D. SURFACE ROUGHNESS PER MIL-STD-10
E. WORKMANSHIP PER EG&G STD A900020

CROSS INDEX	NEXT ASSEMBLY	REQ'D PER N/A	
H-DT-3	E200794	1	00

PART NO. C200757

EG&G LOS ALAMOS DIVISION

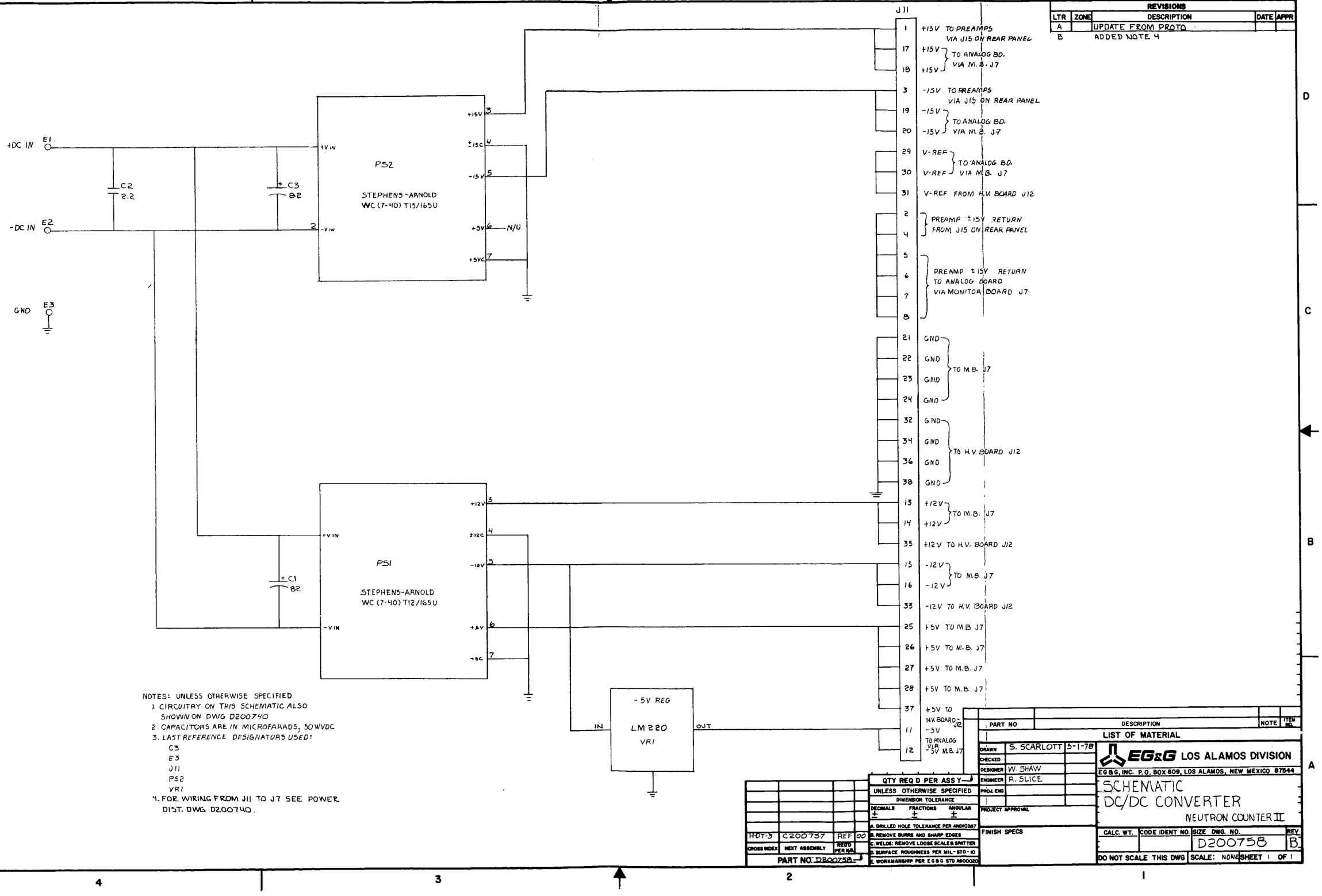
EG&G, INC. · P.O. BOX 809, LOS ALAMOS, NEW MEXICO 87544

ASSY, DC/DC CONVERTER

NEUTRON CNTR II

CALC. WT.	CODE IDENT NO.	SIZE	DWG. NO.	REV
			C200757	A

DO NOT SCALE THIS DWG | SCALE: 1/1 | SHEET 1 OF 1



NOTES: UNLESS OTHERWISE SPECIFIED
1. CIRCUITRY ON THIS SCHEMATIC ALSO SHOWN ON DWG D200740
2. CAPACITORS ARE IN MICROFARADS, 50WVDC
3. LAST REFERENCE DESIGNATORS USED:
   C3
   E3
   J11
   PS2
   VR1
4. FOR WIRING FROM J11 TO J7 SEE POWER DIST. DWG D200740.

REVISIONS				
LTR	ZONE	DESCRIPTION	DATE	APPR
A		UPDATE FROM PROTO		
B		ADDED NOTE 4		

PART NO	DESCRIPTION	NOTE	ITEM NO.

LIST OF MATERIAL

DRAWN	S. SCARLOTT	5-1-78
CHECKED		
DESIGNER	W. SHAW	
ENGINEER	R. SLICE	
PROJ. ENG.		
PROJECT APPROVAL		

EG&G LOS ALAMOS DIVISION
EG&G, INC. P.O. BOX 809, LOS ALAMOS, NEW MEXICO 87544

SCHEMATIC
DC/DC CONVERTER
NEUTRON COUNTER II

CALC. WT.	CODE IDENT NO.	SIZE	DWG. NO.	REV.
		D	D200758	B

DO NOT SCALE THIS DWG | SCALE: NONE | SHEET 1 OF 1

CROSS INDEX	NEXT ASSEMBLY	REQ'D PER N/A
HDT-3	C200737	REF 00

PART NO D200758-

QTY REQ'D PER ASSY

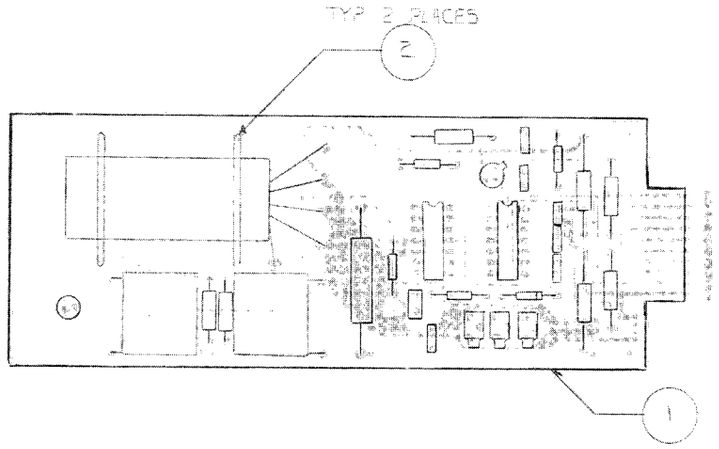
UNLESS OTHERWISE SPECIFIED
DIMENSION TOLERANCE
DECIMALS ± FRACTIONS ± ANGULAR ±

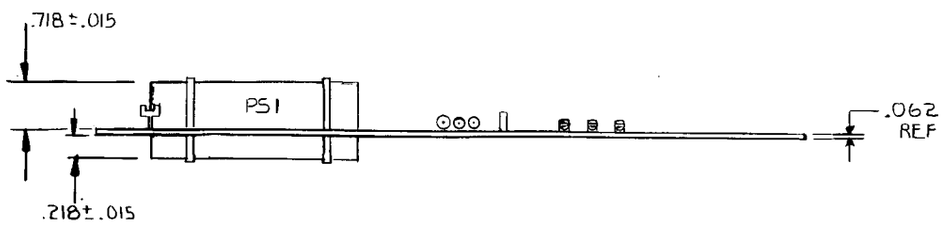
A. DRILLED HOLE TOLERANCE PER ANSI B97
B. REMOVE BURRS AND SHARP EDGES
C. WELDS: REMOVE LOOSE SCALE & SPATTER
D. SURFACE ROUGHNESS PER MIL-STD-10
E. WORKMANSHIP PER EG&G STD A900020

FINISH SPECS

REVISIONS				
LTR	ZONE	DESCRIPTION	DATE	APPR
A		PARTS LIST UPDATED		
B		ITEM 6 WAS: SCMC6560E-77R-393KA3 11 WAS: PMSB2-.025	5-9-79	SB.
C		ITEM 14, R4 WAS 5.1K Ω.	10/30/79	RRC

NOTES
UNLESS OTHERWISE SPECIFIED
1 FOR SCHEMATIC DIAGRAM SEE DWG # D200747
2 MOUNT PS1, ITEM 11 TO DIMENSIONS SHOWN WITH ITEM 2





ITEM NO.	QTY	PART NO.	SOURCE	DESCRIPTION	DESIG.	NOTE
26	1	1N4740A	MOTOROLA	DIODE, ZENER,	VR2	
25	1	LM113H	NATL	REGULATOR, 1.22V,	VR1	
24	1	OP-07EY	P.M.I.	OP AMP	U2	
23	1	LM224J	NATL	QUAD OP AMP	U1	
22	1	CGH-2-TO	TRW/IRC	RESISTOR, H.V., 200M, 2W, 1%	R7	
21	1	CGH-1/4-TO	TRW/IRC	RESISTOR, H.V., .499K, 1/4W, 1%	R6	
20	1	CEC-TO	TRW/IRC	RESISTOR, 4.64K, 1/2W, 1% M.F.	R10	
19	1	S102C	VISHAY	RESISTOR, 1.5K, .15W, .05%	R11	
18	1	S102C	VISHAY	RESISTOR, 5.2623K, .15W, .05%	R12	
17	1	S102C	VISHAY	RESISTOR, 5K, .15W, .05%	R5	
16	2	CB1045	A/B	RESISTOR, 100K, 1/4W, 5%	R8, R9	
15	1	CB1035	A/B	RESISTOR, 10K, 1/4W, 5%	R13	
14	1	CB5125	A/B	RESISTOR, 15K, 1/4W, 5%	R4	
13	1	1240X-5K	VISHAY	POTENTIOMETER, 5K, 21 TURN	R3	
12	2	1240X-2K	VISHAY	POTENTIOMETER, 2K, 21 TURN	R1, R2	
11	1	PMSB2-.025-1	DEL ELECT.	POWER SUPPLY, HIGH VOLTAGE, 2KV	PS1	2
10	2	1537-76	DELEVAN	INDUCTOR, 100 μH	L1, L2	
9	1	1310B	USECO	TERMINAL, BIFURCATED	E1	
8	1	IN3731	IDC	DIODE, IN3731	D1	
7	1	8131-100-651-47MM	ERIE	CAP CER, .47μF, 100 WVDC	CB	
6	2	SCMC6560E-X7R-393KA3	SEMTECH	CAP, CER, .039μF, 3KVDC	C6, C7	
5	1	8101-100-W5R0-682K	ERIE	CAP, CER, 6800 pF, 100 WVDC	C5	
4	2	8121-100-W5R0-103K	ERIE	CAP, CER, .01μF, 100 WVDC	C2, C4	
3	2	1500-106X9035Z2	SPRAGUE	CAP, TANT, 10μF, 35WVDC	C1, C3	
2	2			STRAP, WIRE BUNDLE		2
1	1	C200745-00	EG&G	PWB, HIGH VOLTAGE		

C200746-00

LIST OF MATERIAL

DRAWN	S. SCARLOTT	5-8-78
CHECKED		
DESIGNER	W. SHAW	
ENGINEER	R. SLICE	
PROJ. ENG.		
PROJECT APPROVAL		
FINISH SPECS		

EG&G LOS ALAMOS DIVISION
EG&G, INC. P.O. BOX 809, LOS ALAMOS, NEW MEXICO 87544

ASSY, HIGH VOLTAGE PWB

NEUTRON COUNTER II

CALC. WT.	CODE IDENT NO.	SIZE	DWG. NO.	REV
		C	C200746	C

DO NOT SCALE THIS DWG | SCALE: 1/1 | SHEET 1 OF 1

H-DT-3	C200820	1	00
CROSS INDEX	NEXT ASSEMBLY	REQ'D PER N/A	

PART NO. C200746

QTY REQ'D PER ASS'Y

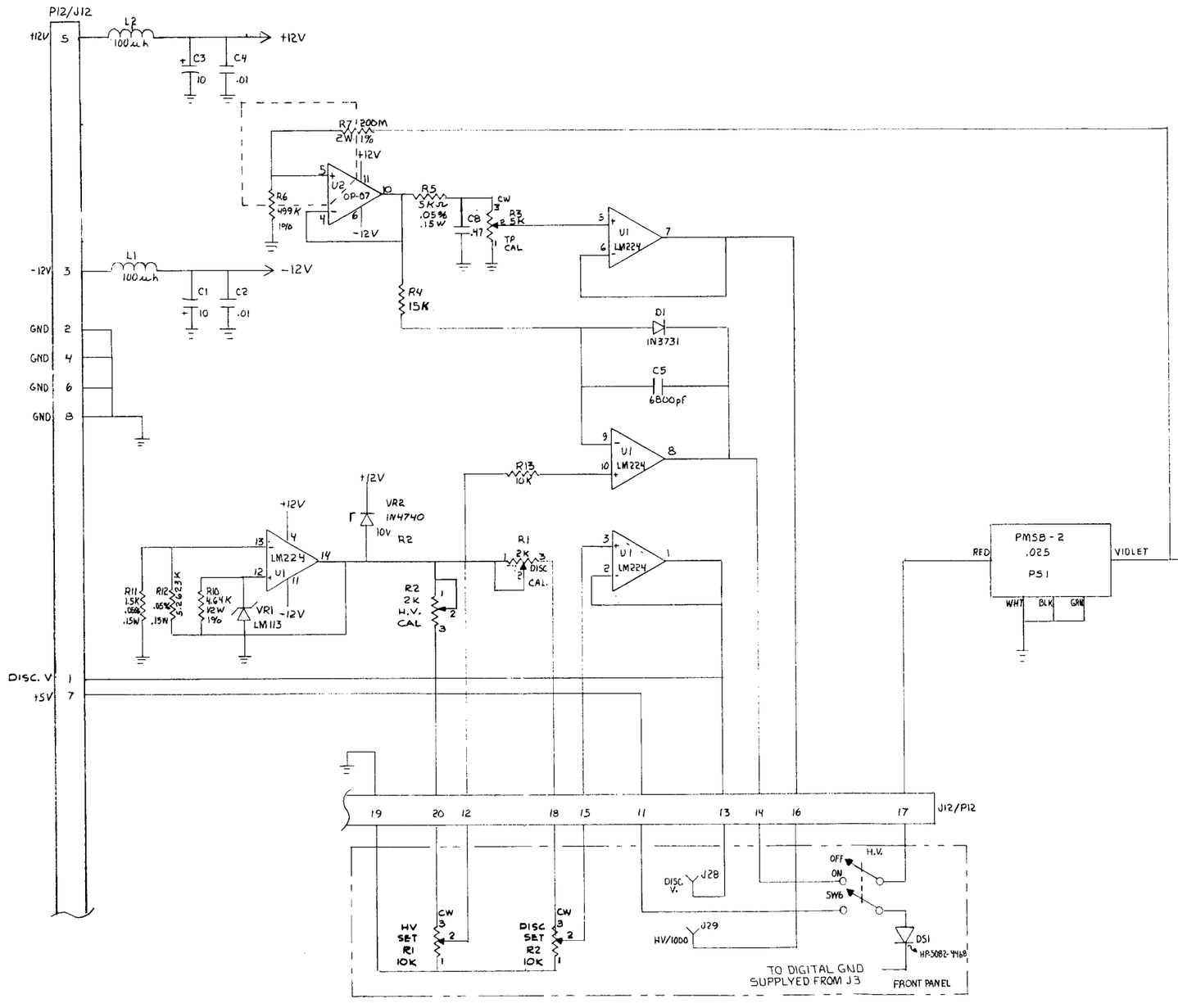
UNLESS OTHERWISE SPECIFIED

DIMENSION TOLERANCE

DECIMALS ± | FRACTIONS ± | ANGULAR ±

A DRILLED HOLE TOLERANCE PER ANDI0387
B REMOVE BURRS AND SHARP EDGES
C WELDS REMOVE LOOSE SCALE & SPATTER
D SURFACE ROUGHNESS PER MIL-STD-10
E WORKMANSHIP PER EG&G STD A900020

REVISIONS				
LTR	ZONE	DESCRIPTION	DATE	APPR
A		R4 WAS 5.1K		



NOTES: UNLESS OTHERWISE SPECIFIED:
1. ALL RESISTORS ARE IN OHMS, 1/4 W, 5%
2. ALL CAPACITORS ARE IN MICROFARADS.
3. LAST REFERENCE DESIGNATORS USED ON BOARD
   - C8
   - D1
   - E1
   - J12
   - L2
   - P12
   - PS1
   - R13
   - U2
   - VR2

PART NO	DESCRIPTION	NOTE	ITEM NO.

LIST OF MATERIAL

DRAWN	S. SCARLOTT	5-3-78
CHECKED		
DESIGNER	W. SHAW	
ENGINEER	R. SLICE	
PROJ. ENG		
PROJECT APPROVAL		

EG&G LOS ALAMOS DIVISION
EG&G, INC. P.O. BOX 809, LOS ALAMOS, NEW MEXICO 87544

SCHEMATIC, HIGH VOLTAGE PWB NEUTRON COUNTER II

CALC. WT.	CODE IDENT NO.	SIZE	DWG. NO.	REV
		D	D200747	A

DO NOT SCALE THIS DWG | SCALE: NONE | SHEET 1 OF 1

FINISH SPECS

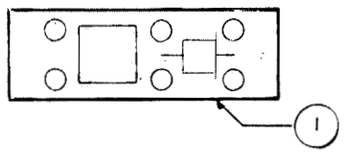
QTY REQ'D PER ASSY	
UNLESS OTHERWISE SPECIFIED	
DIMENSION TOLERANCE	
DECIMALS ±	FRACTIONS ±
ANGULAR ±	
A. DRILLED HOLE TOLERANCE PER ANSI 0387	
B. REMOVE BURRS AND SHARP EDGES	
C. WELDS: REMOVE LOOSE SCALE & SPATTER	
D. SURFACE ROUGHNESS PER MIL-STD-10	
E. WORKMANSHIP PER EG&G STD A900020	

CROSS INDEX	NEXT ASSEMBLY	REQ'D PER N/A
H-DT-3	C200746	REF 00

PART NO. D200747

REVISIONS				
LTR	ZONE	DESCRIPTION	DATE	APPR

NOTES: UNLESS OTHEWISE SPECIFIED:
1. FOR SCHEMATIC DIA. SEE POWER DISTRIBUTION DWG. NO. D200740.



ITEM NO.	QTY	PART NO.	SOURCE	DESCRIPTION	DESIG.	NOTE
4	6	1310B	USECO	TERMIVAL, BIFURCATED	E1-E6	
3	1	IN4722	MOTOROLA	RECTIFIER, DIODE,	CR2	
2	1	VH447	VARO-SEMI	RECTIFIER, BRIDGE, 6A	CR1	
1	1	B200759-00	EG&G	PWB, RECTIFIER		

LIST OF MATERIAL

C200760-00

DRAWN	S. SCARLOTT	5-8-78
CHECKED		
DESIGNER	W. SHAW	
ENGINEER	R. SLICE	
PROJ. ENG		
PROJECT APPROVAL		

EG&G LOS ALAMOS DIVISION
EG&G, INC · P.O. BOX 809, LOS ALAMOS, NEW MEXICO 87544

ASSY, RECTIFIER

NEUTRON COUNTER II

CALC. WT.	CODE IDENT NO.	SIZE	DWG. NO.	REV
		C	C200760	

DO NOT SCALE THIS DWG | SCALE: 1/1 | SHEET 1 OF 1

CROSS INDEX	NEXT ASSEMBLY	REQ'D PER N/A	
H-DT-3	E200794	1	00

PART NO. E200760

QTY REQ'D PER ASS'Y

UNLESS OTHERWISE SPECIFIED

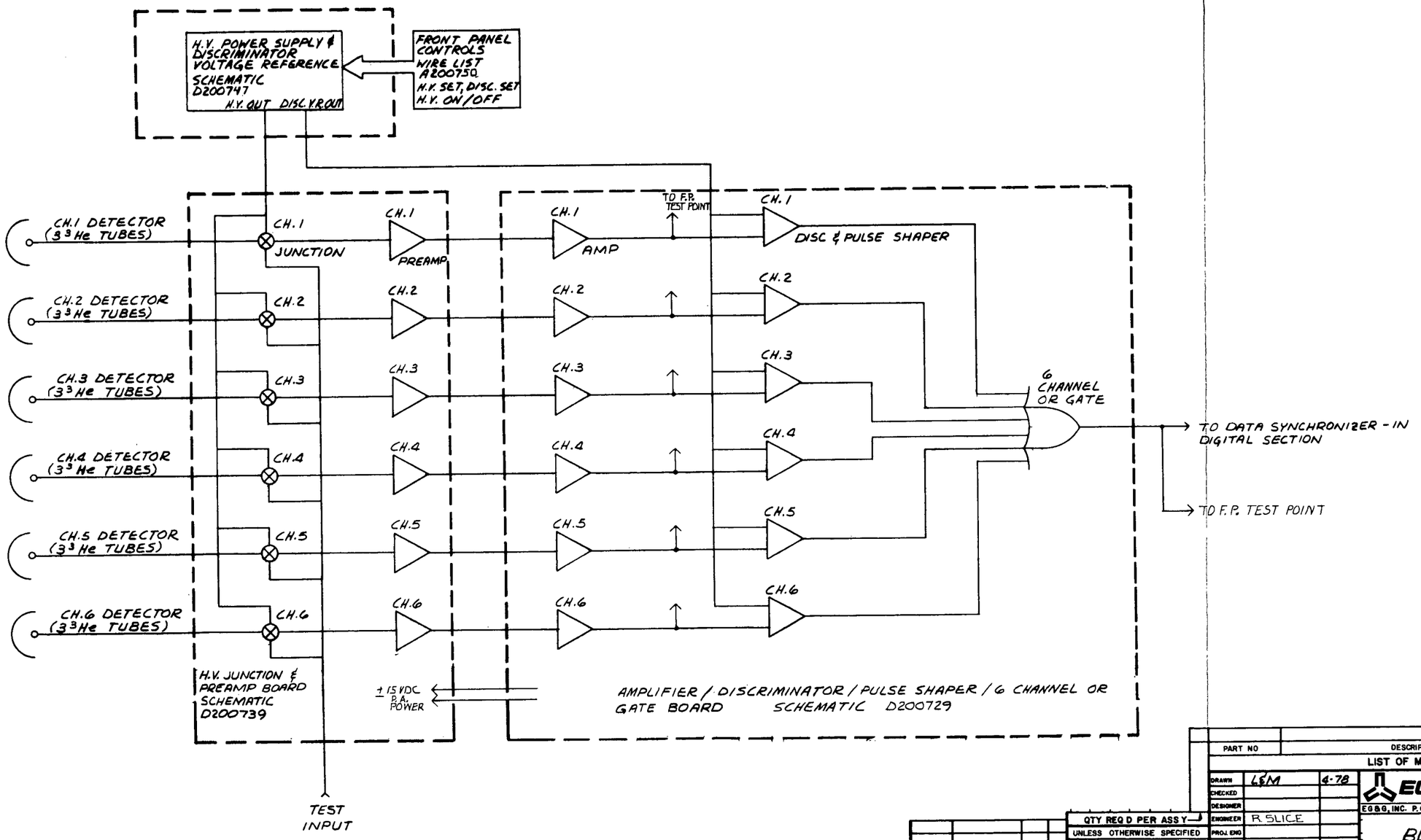
DIMENSION TOLERANCE		
DECIMALS ±	FRACTIONS ±	ANGULAR ±

A DRILLED HOLE TOLERANCE PER ANDI0387
B REMOVE BURRS AND SHARP EDGES
C WELDS REMOVE LOOSE SCALE & SPATTER
D SURFACE ROUGHNESS PER MIL-STD-10
E WORKMANSHIP PER EG&G STD A900020

FINISH SPECS

REVISIONS				
LTR	ZONE	DESCRIPTION	DATE	APPR
A		MINOR NOMENCLATURE UPDATES		

ANALOG SECTION



PART NO	DESCRIPTION	NOTE	ITEM NO.

LIST OF MATERIAL

DRAWN	L&M	4-78
CHECKED		
DESIGNER		
ENGINEER	R. SLICE	
PROJ. ENG		
PROJECT APPROVAL		

FINISH SPECS

QTY REQ'D PER ASSY
UNLESS OTHERWISE SPECIFIED
DIMENSION TOLERANCE
DECIMALS ± FRACTIONS ± ANGULAR ±
A. DRILLED HOLE TOLERANCE PER ANDI0387
B. REMOVE BURRS AND SHARP EDGES
C. WELDS: REMOVE LOOSE SCALE & SPATTER
D. SURFACE ROUGHNESS PER MIL-STD-10
E. WORKMANSHIP PER E G & G STD A900020

CROSS INDEX	NEXT ASSEMBLY	REQ'D PER NA
H-DT-3	E200794	REF 00

PART NO. D200733

EG&G LOS ALAMOS DIVISION
EG&G, INC. P.O. BOX 809, LOS ALAMOS, NEW MEXICO 87544

BLOCK DIAGRAM NEUTRON COUNTER PHASE II

CALC. WT.	CODE IDENT NO.	SIZE	DWG. NO.	REV
			D200733	A

DO NOT SCALE THIS DWG | SCALE: ~ | SHEET 1 OF 2

DIGITAL SECTION

SHIFT REGISTER BOARD
SCHEMATIC D200734

FROM 6 CHAN OR GATE - ANALOG SECTION

IN DATA SYNCHRONIZER
RESET
CLK

RESET LOGIC

RESET TO μP COUNTER, LATCHES, SCALERS, & μP INTERFACE

F.P. RESET SW. OR μP CONTROL RESET

2 MHZ SQ WV. @ 250(nS) SQ PULSE @ 2 MHZ REP. RATE

S.R. CLOCK 4 MHZ

CLOCK DIVIDERS GATE & LEVEL SHIFTERS

2 MHZ
2 MHZ
2Ø CLK
S.R. CLK
1 MHZ

PRESET TIMER

F.P. RUN TIME SEL. SW. 1 SEC → 9×10⁹ SEC

1 P.P.S.

TIMED OUT STATUS TO μP INTERFACE

START/STOP LOGIC

F.P. S/S SW. OR μP CONTROL S/S

START / STOP / RUN STATUS TO μP INTERFACE

Σ LATCH INTERROGATE START/STOP GATE

S.R. CLOCK

PRE DELAY SHIFT REGISTER

INTERNAL SW SELECTABLE PRE DELAY 1 μS → 32.5 μS IN .5 μS INCREMENT

2Ø CLOCK 1

FIXED PERIOD ACCIDENTAL DELAY SHIFT REGISTER ≃ 1 mS

S.R. CLOCK

DELAY GATE SHIFT REGISTER

F.P. SWITCH SEL. GATE PERIOD 8, 16, 32 & 128 μS

RESET INPUT

UP/DOWN COUNTER

2 DIGIT BCD BUS

Σ (R & A) $N_1 + M_1$ M_1

N_2 M_2 Σ A $N_2 + M_2$

2 DIGIT BCD & CY

A INTERROGATE

R & A INTERROGATE

RESET INPUT

R & A LATCH

A LATCH

2 DIGIT BCD

2 DIG BCD & CY

μ PROCESSOR ASYNCHRONOUS COMM. INTERFACE ADAPTER (ACIA)

RX

TX

RS232 DATA COMM.

BIDIRECTIONAL BUS (ADDRESS & DATA)

μ PROCESSOR (6800 SYSTEM)

BIDIRECTIONAL BUS (ADDRESS & DATA)

μ PROCESSOR PERIPHERAL INTERFACE ADAPTER (PIA)

MUX STROBE & STATUS TO μP SOFTWARE SWITCH DATA CONTROL & INHIBIT TO S.R. & MUX'R

HP-97 INTERFACE

DATA TO HP-97

μ PROCESSOR INTERFACE

MULTIPLEX STROBE & STATUS INPUT

CONTROL & INHIBIT OUTPUT TO S.R. & MUX'R

MICROPROCESSOR BOARD
SCHEMATIC D200741

RESET INPUT
MUX* IN

RUNNING TIME SCALER (1 SEC RES)

T MUX DIGIT STROBE TO μP INTERFACE & DISPLAY

TOTAL EVENTS SCALER

C MUX DIGIT STROBE TO μP INTERFACE & DISPLAY

R & A SCALER

R & A MUX DIGIT STROBE TO μP INTERFACE & DISPLAY

A SCALER

A MUX DIGIT STROBE TO μP INTERFACE & DISPLAY

MULTIPLEX BCD DATA BUS

DISPLAY TIME

DISPLAY TOTALS

DISPLAY R & A

DISPLAY A

TO SCALERS & μP*

MULTIPLEX STROBE LINES

MULTIPLEXER (OSC.: ≃ 2 KHZ & 3 STROBE SELECTORS)

MULTIPLEX INHIBIT FROM μP INTERFACE

* LEAST SIGNIFICANT DIGIT STROBES (1'S DIGIT & 10'S DIGIT) GO DIRECTLY TO SCALERS, μP, AND DISPLY.
100'S DIGIT AND GREATER DIGIT STROBES ARE GENERATED IN THE HCTR4010 SCARLERS FOR USE IN DISPLAY AND μP. (SEE INSTRUCTION & MAINT. MANUAL).

DISPLAY / DRIVER BOARD
SCHEMATIC D200753

REVISIONS

LTR	ZONE	DESCRIPTION	DATE	APPR

PART NO	DESCRIPTION	NOTE	ITEM NO.

LIST OF MATERIAL

DRAWN	L&M	4-78
CHECKED		
DESIGNER		
ENGINEER	R. SLICE	
PROJ. ENG		
PROJECT APPROVAL		

EG&G LOS ALAMOS DIVISION
EG&G, INC. P.O. BOX 809, LOS ALAMOS, NEW MEXICO 87544

BLOCK DIAGRAM
NEUTRON COUNTER PHASE II

CALC. WT.	CODE IDENT NO.	SIZE	DWG. NO.	REV
			D200733	A

DO NOT SCALE THIS DWG | SCALE: | SHEET 2 OF 2

QTY REQ'D PER ASSY			
UNLESS OTHERWISE SPECIFIED			
DIMENSION TOLERANCE			
DECIMALS ±	FRACTIONS ±	ANGULAR ±	
A. DRILLED HOLE TOLERANCE PER ANSI B97			
B. REMOVE BURRS AND SHARP EDGES			
C. WELDS: REMOVE LOOSE SCALE & SPATTER			
D. SURFACE ROUGHNESS PER MIL-STD-10			
E. WORKMANSHIP PER EG&G STD A80000			
FINISH SPECS			

H-DI-3	E200794	REF	00
CROSS INDEX	NEXT ASSEMBLY	REQ'D PER NA	

PART NO. C200733

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