A Radiation-Hardened Bulk Si-Gate CMOS Microprocessor Family*

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RCA and Sandia Laboratories have jointly developed a radiation-hardened bulk Si-gate CMOS technology which is used to fabricate the CDP-1800 series microprocessor family. Total dose hardness of 1×10^6 rads (Si) and transient upset hardness of 5×10^8 rads (Si)/sec with no latch up at any transient level has been achieved. Radiation-hardened parts manufactured to date include the CDP-1802 microprocessor, the CDP-1834 ROM, the CDP-1852 8-bit I/O port, the CDP-1856 N-bit 1 of 8 decoder, and the TCC-244 256 x 4 Static RAM. The paper is divided into three parts. In the first section, the basic fundamentals of the non-hardened C^2L technology used for the CDP-1800 series microprocessor parts is discussed along with the primary reasons for hardening this technology.[1,2] The second section discusses the major changes in the fabrication sequence that are required to produce radiation-hardened devices. The final section details the electrical performance characteristics of the hardened devices as well as the effects of radiation on device performance. Also included in this section is a discussion of the TCC-244 256 x 4 Static RAM designed jointly by RCA and Sandia Laboratories for this application.

Selection of C^2L Technology

CMOS, in general, has found wide use in many systems because of its moderate speed and very low-power dissipation. The CDP-1800

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series microprocessor family of devices was chosen for radiation hardening because it is commercially available and designed in the C^2L technology. The basic topology of C^2L has certain advantages in a radiation environment. The C^2L technology is a self-aligned silicon-gate technology in which the chip surface is heavily doped with either p+ or n+ such that potential problems associated with field inversion due to irradiation are eliminated.[3]

The elemental C^2L structure is illustrated in Figure 1. The drain of each device is totally enclosed by the polysilicon gate. The fully enclosed geometry totally eliminates the need to guardband since no uncontrolled current can flow to any drain which is gated on all sides. The transistor source is the surrounding substrate or source plane (a p+ doped source plane for PMOS FETs and an n+ doped source plane for NMOS FETs). Hence, individual source connections are not required for each transistor.

Radiation-Hardened C^2L Process

Several special processing constraints are necessary in order to harden C^2L devices. Radiation hardening of the thin (approximately 500A to 700A) channel oxide is accomplished in either a 1000°C dry oxidation or a 900°C pyrogenic steam/dry oxidation. Subsequent wafer processing occurs at limited temperatures usually below the channel oxide growth temperature. Polysilicon is deposited as an intrinsic film and then doped n+ during a low-temperature diffusion step, or the poly is deposited and doped N+ in situ. The source/drain regions are created by ion implantation of n+ and p+ utilizing either photoresist or aluminum as an implant mask. An undoped CVD oxide serves as the intermediate dielectric, and the final metallization is approximately 2 percent SiAl. The final metal is deposited by either an In-source or S-gun evaporation. Neutron irradiation is used to reduce the minority carrier lifetime to prevent latch-up and to improve the transient upset level of the circuits.[4]

Electrical Performance Characteristics

When radiation hardening an existing technology, there are certain trade-offs in electrical performance which must be considered. The radiation-hardened processing causes the devices to be slower in speed by as much as 30 percent because low-temperature processing precludes drive-in of the sources and drains resulting in longer channel lengths, and because the thin-gate oxide gives increased capacitances and therefore

larger RC time constants. Also increased substrate doping required to increase the n-channel threshold reduces the carrier mobility in the channel.

The radiation-induced threshold shifts require that the circuit design be able to tolerate wide variation and imbalance of the n-channel and p-channel thresholds. Specifically, the primary cause of degradation in the circuit performance of the C^2L devices is the loss of p-channel drive due to the p-channel threshold becoming more negative with radiation.

We have found that the primary cause of failure of the CDP-1802 microprocessor is reduction in speed and p-channel output drive due to the radiation-induced p-channel threshold shifts. The internal circuit design is quite tolerant of parametric variations resulting from processing and ionizing radiation. The CDP-1834 has also been found to be quite tolerant of the processing and radiation-induced circuit parameter variations.

This was not the case with the TC-1190 256 x 4 bit Random Access Memory. Certain portions of the address decoding circuitry were sensitive to internal RC time constants, threshold voltages, and n-channel and p-channel drive. The condition became worse with radiation. This required redesigning those portions of the circuitry which were particularly pattern sensitive. The resulting circuit, renamed the TCC-244, has proven to be a reliable radiation-tolerant memory. During the redesign of the memory, the fact that the p-channel thresholds become more negative with radiation was taken into account. As a result, the primary failure mode of the TCC-244 in a radiation environment is "imprinting" of the the memory, i.e., the pattern which is in the memory during the irradiation becomes the preferred state for the memory cells due to the different threshold shifts in the n-channel and p-channel devices when irradiated under the opposite bias configurations which always occur in a static 6-transistor CMOS memory cell.

Characterization of the electrical parameters of the radiation-hardened devices is being performed for both pre-irradiation and post-irradiation conditions. Table I summarizes the data which has been obtained to date. A complete characterization of both the AC and DC parameters as a function of ionizing radiation dose will be available shortly. A 1000-hour reliability evaluation is being performed on circuits processed using the radiation-hardened process. In addition, over 400 devices have been burned-in for 168 hours at 150°C with a failure rate of less than 5 percent.

Conclusions

We have demonstrated a reliable, radiation-hardened silicon gate/bulk silicon technology which is applied to a commercial microprocessor family. Total dose hardness of 1×10^5 to 1×10^6 rads (Si) and transient upset hardness of 5×10^8 to 1×10^9 rads (Si)/sec with no latch up at any transient dose level has been achieved. At the present time, radiation-hardened circuits in the CDP-1800 microprocessor family are being produced for several spacecraft applications.

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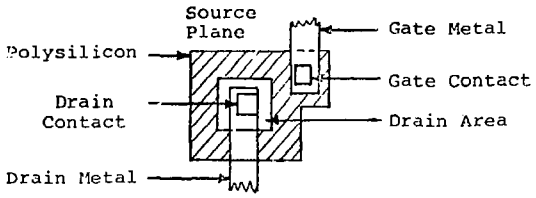

Figure 1. C^2L MOS Transistor

TABLE I
Ionizing Radiation Effects on Radiation Hardened
Silicon Gate/Bulk CMOS LSI

Circuit Type: Performance Characteristic	CDP-1802 Microprocessor	TCC-244 Random Access Memory
Transient Latch-up (Rads Si/sec)	$>10^{10}$ (no latch-up observed)	$>10^{10}$ (no latch-up observed)
Minimum Observed Upset Level (Rads Si/sec)	5×10^{8} (5V) 1×10^{9} (10V)	5×10^{8} (5V) 5×10^{8} (10V)
Total Dose Worst Case Failure Level	3.3×10^{5} (5V) 1.4×10^{6} (10V)	1.5×10^{5} (5V) 5.5×10^{5} (10V)

Typical Performance Characteristics
of the TCC-244 RAM

	Pre-Irradiation	Post Irradiation (2×10^5 rads/Si,
N-Channel Output Drive (10V)	5 ma	4 ma
P-Channel Output Drive (10V)	3 ma	2.5 ma
Power Supply Leakage (12V)	0.5 µa-50 µa	1 µa-100 µa
Access Time from Address Change (10V)	170 ns	240 ns
Min. Write Pulse Width (10V)	50 ns	100 ns