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# TOTAL-DOSE HARDNESS ASSURANCE FOR SPACE APPLICATIONS OF COMMERCIAL CMOS DEVICES*

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35-Word Abstract

Lot acceptance tests are evaluated for nonhardened CMOS devices for low total-dose space applications. Examples are presented for cases in which gate- or field-oxide leakage dominates device response.



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There is growing evidence that lot acceptance tests of hardened CMOS electronics intended for use in low-dose-rate space environments must include measurements of device response after postirradiation annealing, i.e. "rebound testing" [1-6]. This is based on observations that Co-60 irradiation at typical laboratory dose rates (100-300 rad(Si)/s) does not adequately screen out devices for which interface-trap buildup causes eventual failure in a low-dose-rate environment [4-6]. Recently, several hardness assurance strategies have been proposed to account for this behavior [6-9]. Perhaps the simplest of these to implement is that described by Fleetwood et al. in Ref. 6. There it is recommended that hardened CMOS circuits intended for use in a space environment be irradiated with Co-60 $\gamma$-rays to a total dose that is 1.5-times the anticipated exposure during the lifetime of the system, and that device functional and parametric testing be performed after a subsequent 1-week biased anneal at 100°C [6].

While this kind of test may be suitable for screening hardened devices whose primary cause of failure in space is speed or drive reduction caused by interface-trap buildup, it has not been established that a similar test can be used to qualify devices whose primary cause of failure in space is excess leakage currents caused by oxide-trapped charge buildup. For example, commercial (nonhardened) CMOS devices may fail Co-60 testing and still be suitable for use in space systems if sufficient annealing of oxide-trapped charge occurs over the long times over which the dose is accumulated [10,11].

In this paper we compare the response of nonhardened CMOS devices following Co-60 exposure and elevated temperature annealing to that of devices irradiated at low dose rates. We show that, for devices whose primary cause of failure is gate- or field-oxide induced leakage, lot acceptance methods similar to those defined for hardened devices [6] can be defined as well. However, preliminary results suggest that the overstress required in testing may have to be increased to as much as a factor of 2-3 times the system level specification.

In this summary we limit our discussion to one device type: SGS 4007 inverters (oxide thickness of $\simeq$ 100 nm) whose primary failure mechanism in a low-dose-rate environment is leakage due to n-channel transistors going into depletion mode. This is illustrated in Fig. 1, where Idd (leakage at 0 V) and Vth (extrapolated threshold voltage) are plotted as a function of total dose for Cs-137 irradiations of n-channel transistors at a dose rate of 0.16 rad(Si)/s. The large increase in leakage at $\simeq$ 7 krad(Si) in this case is caused by oxide-trapped charge buildup in the transistor, which is approaching depletion mode. This behavior is also characteristic of SGS 4013s that we have investigated, as discussed in the full paper.

In Fig. 2 we plot Idd as a function of irradiation and annealing time for SGS 4007s, irradiated in a Co-60 source at a dose rate of $\simeq$ 240 rad(Si)/s to total doses of 7, 11, and 21 krad(Si), corresponding to 1-times, 1.5-times,

and 3-times the failure dose of ≃ 7 krad observed in Fig. 1. Note in Fig. 2 that the leakage is well above 1 μA in all cases immediately after exposure, with significant recovery during annealing. The initial reduction in Idd at 100°C appears to be thermally activated (and caused by a faster-than-logarithmic change in threshold voltage with time [12]), as demonstrated by the large decrease in Idd between 3600 and 7200 seconds in Fig. 2 [12]. After this initial period of thermally-activated recovery, the leakage decreases more slowly with time, which is more suggestive of oxide trapped-charge removal and/or electron injection via a tunneling process [12]. Note that the devices irradiated to 1.5- and 3-times the failure level still show appreciable leakage after this period of elevated temperature anneal, showing that many uncompensated holes remain in the gate oxide after the annealing period. This result suggests that, with the appropriate choice of overstress in dose, the leakage of nonhardened devices following anneal could be matched to that in a low-dose-rate environment.

We illustrate such a process in Fig. 3. Here we plot Idd as a function of irradiation and annealing time for Co-60 and low-dose-rate exposures of SGS 4007s. (Lower dose-rate exposures to comparable doses will be completed for the final paper, and comparable data on SGS 4013s will also be shown.) These Co-60 and Cs-137 results are extrapolated to project possible leakage levels in, for example, a seven-year mission with a 7-krad total dose requirement. The solid line is a best fit to the data points. Uncertainties in the extrapolation, due to the scatter in the Co-60 data, are shown by the dashed lines. (Whether a straight-line extrapolation of this data is justified, given the shapes of the annealing curves in Fig. 2 is not clear. We will explore this in detail in the full paper with longer annealing-time measurements and lower-dose rate irradiations for both gate-oxide and field-oxide leakage.) The projected leakage at low-dose-rate may now be compared with the leakage levels observed after Co-60 irradiation plus elevated-temperature anneal, as shown in Fig. 3 at $2 \times 10^8$ sec. Note that Co-60 irradiation to 7-krad plus anneal significantly underpredicts the projected leakage, while Co-60 irradiation to 21-krad plus anneal significantly overpredicts the leakage anticipated at the end of a seven-year exposure to 7-krad. The best match to the projected low-dose-rate response, based on these data, appears to be Co-60 irradiation to 1.5-2.0 times the total radiation dose anticipated in the low-dose-rate environment, under these irradiation and anneal conditions.

In the full paper we will show similar low-dose-rate and rebound-testing for commercial devices in which field-oxide leakage dominates the device response, and data for other nonhardened devices (with thinner gate oxides) in which the gate oxide leakage dominates the device response. Mechanisms for the annealing of the leakage current will be compared for these cases, with a focus on possible differences between recovery rates for gate and field oxides. Detailed implications for lot acceptance testing will also be discussed. In all cases that we have investigated, Co-60 irradiation to a level that is 3-times that expected in a low-dose-rate environment, followed by a 1-week 100°C anneal, appears to overpredict the leakage exhibited by devices at low dose rates. Such a test may well provide a reasonable, conservative estimate for the response of nonhardened CMOS circuits in a space environment. Therefore, it may be possible to define a single (conservative) test to screen hardened and commercial CMOS devices for use in a space.

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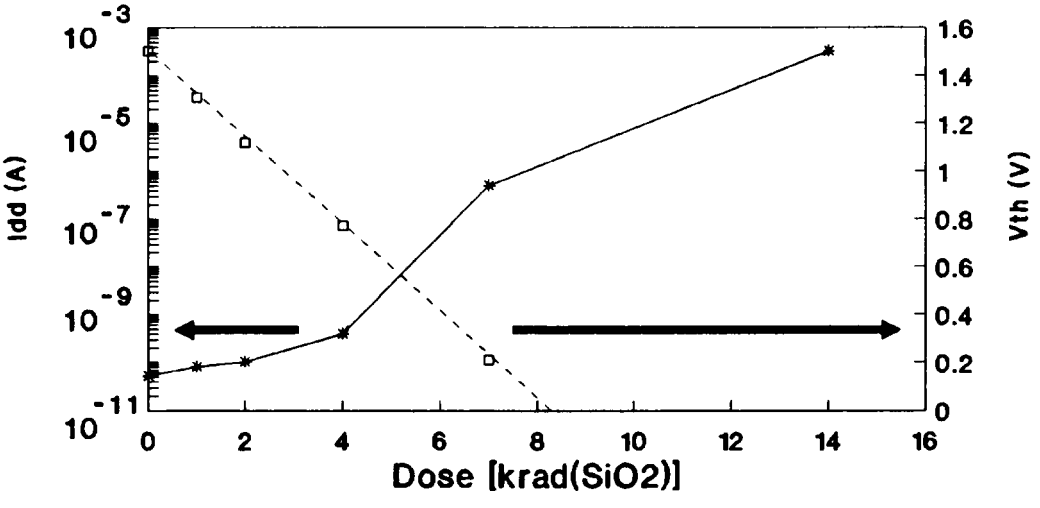


Fig. 1. Idd (left-hand scale) and Vth (right-hand scale) as a function of Cs-137 dose for n-channel transistors on SGS-4007 inverters. The dose rate was 0.16 rad(Si)/s, and the bias was 15 V.

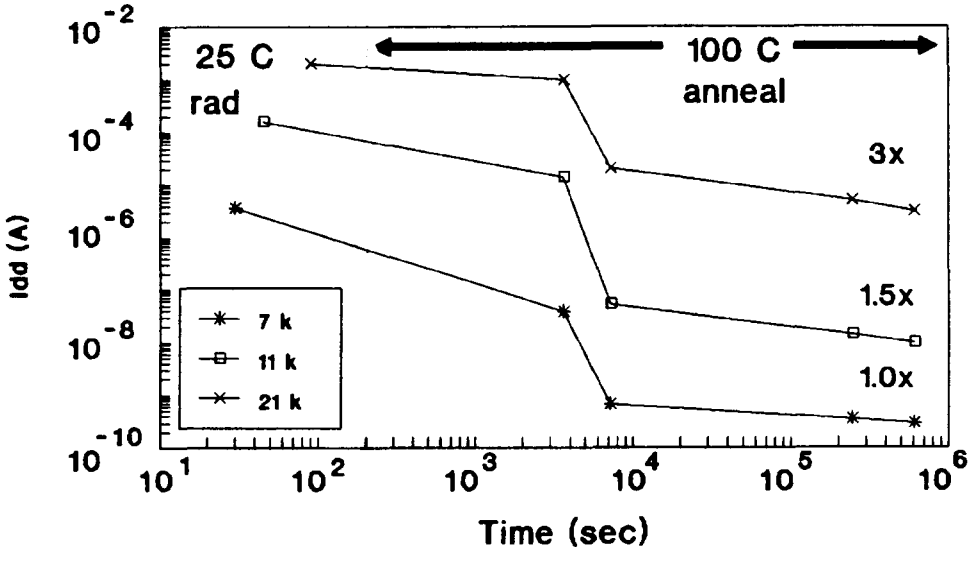


Fig. 2. Idd as a function of irradiation and annealing time for n-channel transistors on SGS-4007 inverters. The transistors were irradiated with Co-60 at 240 rad(Si)/s to doses of 7, 11, and 21 krad(Si), and annealed at 100°C. The irradiation and anneal bias was 15 V.

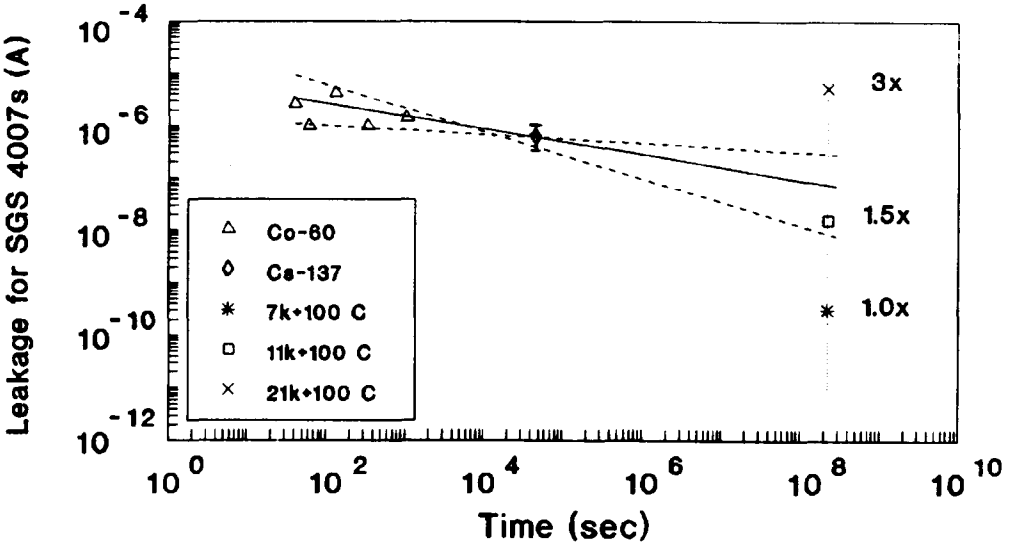


Fig. 3. Idd as a function of irradiation and annealing time for n-channel transistors on SGS-4007 inverters. The triangles denote 5 separate transistors irradiated with Co-60 at 240 rad(Si)/s to 7.0 krad(Si), and annealed for varying times at 25°C. The diamond denotes devices irradiated with Cs-137 at 0.16 rad(Si)/s to 7.0 krad(Si). The "X", "□", and "*" denote devices irradiated with Co-60 to the doses in the inset, and annealed at 100°C. These data are plotted at a time of seven years, for comparison with the extrapolated leakage of the Co-60 and Cs-137 irradiated devices, as discussed in the text.