Fermi National Accelerator Laboratory

A Working, VME-based, 106MHz FADC Data Acquisition System for the Tracking Detectors at D0

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Disclaimer

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Abstract

A data acquisition system for the tracking detectors of the D0 Colliding Detector has been built and is operational, taking cosmic ray data. It is composed of 8200 channels of 106MHz 8-bit Flash Analog to Digital Converters(FADC). These are configured as sixteen channels per FADC Module, up to sixteen FADC Modules per crate, and a total of thirty-six 9U VME crates. A crate controller module, the control system interface, and a high speed data buffer/driver complete the FADC crate. Design and operation details are described.

I. OVERVIEW OF THE D0 CENTRAL TRACKING FRONT END ELECTRONICS SYSTEM

Four separate drift chambers and a transition radiation detector make up the Central Tracking System for the D0 colliding beam detector. The transition radiation detector and two of the drift chambers are positioned around the collision point as three concentric cylinders coaxial with the beamline. The two remaining drift chambers are disk like in structure, positioned orthogonal to the beam axis at both ends of the central structure. There is a total of 8200 wire and delay line sensors in the Central Tracking detectors, each requiring a separate channel of electronics to condition and digitize signals resulting from proton-antiproton collisions (presently every 3.5µs for a duration of 2.5µs).

A block diagram of the electronics for a single channel is shown in **Figure 1**. Signals generated in the chambers are first amplified by common base, charge-to-voltage pre-amplifiers that are mounted at the ends of the chambers. The signals are carried on forty-seven feet of micro-coaxial cables, formed into a sixteen channel ribbon, from the pre-amplifier outputs to pulse shaping electronics located on the detector platform. There are thirty-two channels of pulse shaping electronics in one Shaper Module, and up to sixteen modules can be installed into one Shaper Crate. The polarity, gain, shaping response and cable compensation for each Shaper Channel is programmed independently via removable passive component networks. Since each channel can be configured independently, one Shaper Module mother board design is used for all five Central Tracking detectors. The gaussian shaped analog outputs of

the Shaper Modules are driven into 155 foot, 75Ω micro-coaxial ribbon cables in groups of sixteen channels to the inputs of two FADC Modules. The FADC channels digitize the signals at 106.208MHz and store compressed pulse information in double-buffered memories, accessible to the VME bus. The FADC Module design is described in more detail in following sections.
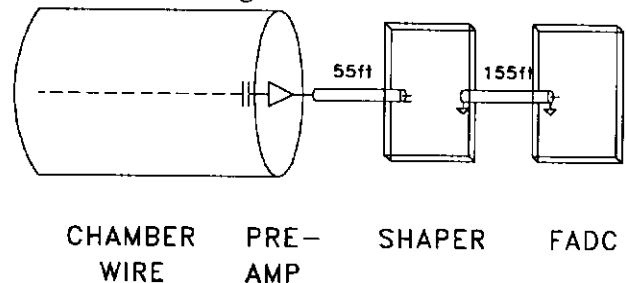

CHAMBER   PRE-   SHAPER   FADC
WIRE   AMP
Figure 1 D0 Central Tracking Electronics

II. OVERVIEW OF THE FADC DATA ACQUISITION SYSTEM

The FADC Data Acquisition System consists of up to sixteen FADC Modules installed in one 9U by 400mm Eurocard VME Crate under the control of one FADC Controller Card. A module providing a communication link to the control system via a Token Ring network and a module designed to read and transfer data from the FADC Modules to the event processing equipment round out the population of the VME crate. A fully loaded water cooled FADC crate dissipates approximately 1.7kW.

A trigger signal, corresponding to proton/antiproton bunch crossings, is received by the Controller Card and distributed to all FADC Modules. In response to this trigger signal, all FADC channels in the crate begin storing the digitized version of the signals received from the Shaper Modules. After data is stored, a second type of trigger signal may or may not be received by the Controller Card. This second signal is the overall D0 trigger and indicates an event of interest. If it is not received, the original data is overwritten with the data from the next bunch crossing indication. The Controller Card responds to this second trigger by instructing the FADC Modules to process the stored data, removing baseline information, and make the resulting data available to the data readout module on the VME backplane. After data has been processed, the Controller Card instructs the buffer/driver module to read the data in all of the FADC channels. Each

channel on the FADC Module contains a double-buffered memory for storing processed data. Under the control of the Controller Card, a second event can be processed by the FADC Module before the data readout module has finished reading the data from the previous event.

III. SYSTEM COMMUNICATION

Three VME MASTERs can exist in a FADC crate to provide communication with the rest of the D0 world. The two most important are the Vertical Interconnect and the VME Buffer/Driver. The third, the TRD Trigger Card[1], is installed in the FADC crates associated with the transition radiation detector and participates in the trigger decision process.

A. Vertical Interconnect

The Vertical Interconnect (VI) Card performs the duties of the VME system controller in the FADC crate. In addition, the VI exists as the slave unit in a bidirectional, serial 60Mb/s serial communication link. The master VI operates in a VME crate with a VME/Token ring interface module, and provides the path for control system communication with the FADC crate. Typically used to download operating parameters to the FADC system, the VI link can also be used to read data for diagnostic purposes.

B. VME Buffer/Driver

Operating as a VME MASTER, the VME Buffer/Driver (VBD) responds to handshaking signals from the FADC Controller Card to read stored data from all channels in the FADC crate utilizing VME LONGWORD Block Transfer read cycles. Event data is stored in a double buffer memory while awaiting transfer to event processing equipment. Data transfer out of the crate is accomplished on a thirty-two bit wide data cable.

IV. FADC MODULE

The FADC Module is an 8 layer, 9U by 400mm VME module. Each FADC Module contains sixteen channels of digitizing electronics. Up to 256 channels in one crate

digitize the analog outputs of the Shaper Modules, simultaneously, in response to a trigger signal supplied by the FADC Controller Card. This parallel design, repeated in all thirty-six FADC Crates, permits up to 8200 channels to be digitized synchronously. With typical event storage cycles lasting approximately 2.5µs, in excess of 2Mbytes of data is generated for each system-wide trigger signal. System-wide trigger signals are expected to occur at an approximately 280kHz rate, yielding data storage at rates exceeding 600×10^9 bytes/second. It is unrealistic to attempt to transfer this quantity of data to event processing equipment in a timely manner. A semi-custom gate array was designed to remove baseline data at the channel level. This gate array is expected to reduce the quantity of data which needs to be transferred out of a given VME crate by 90%.

A single channel with support systems is depicted as a block diagram in **Figure 2**. Analog outputs of the Shaper Modules are received on 75Ω micro-coaxial ribbon cables in groups of sixteen. 75Ω micro-strip lines on the FADC Module deliver the signals to impedance matched analog buffers. Each buffer provides anti-aliasing filtering and programmable gain and pedestal control. Two versions of the analog buffer are available; one has a linear transfer characteristic, while the second provides a bilinear transfer function. The buffer output signal is driven onto 75Ω micro-strip lines to a Sony CX20116 Flash Analog to Digital Converter operating at 106.208MHz. The ECL level output of the FADC chip is converted to TTL levels for storage in the Front End Memory. The analog input to the FADC chip is constantly being digitized. In response to a proton/anti-proton bunch crossing indication, the Front End Memory sections for all channels are enabled to receive data. Data is stored for a programmable amount of time from 0.601 to 38.866µs in 0.301µs increments. If not instructed to save the data from the previous bunch crossing, all FADC channels will overwrite the data in the Front End Memories with subsequent bunch crossing data.

The Zero Suppression Chip (ZSP)[2] is a semi-custom gate array that reads the Front End Memories and stores only pulse data and time stamp information in the Back End Memories. The Back End Memory for each channel is configured as four 500 byte memory sections, each
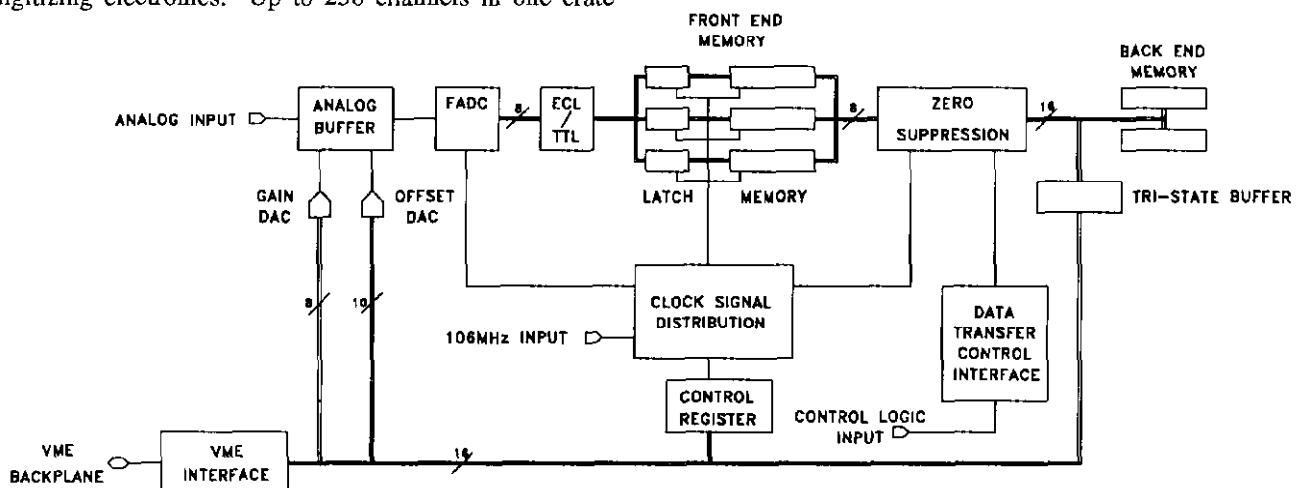

Figure 2 FADC channel block diagram

capable of storing event data and being read by the VBD over the VME backplane.

The FADC Module has been designed to operate as a SLAVE module on the standard VME backplane. As a SLAVE, the FADC Module exhibits the following VME characteristics: Responds only to VME Standard (24 bit) Addressing. Capable of participating in both WORD (16 bit data bus) and LONGWORD (32 bit data bus) VME data transfers for both READ and WRITE cycles. Finally, the FADC Module is capable of participating in VME BLOCK data transfer cycles, but this participation is limited to WRITE and READ cycles involving the Back End Memory in any FADC channel.

Differential ECL signals for the 106.208MHz clock and bunch crossing indication pulse are individually delivered to each FADC Module, driven onto the custom J3 backplane by the Controller Card. All ECL level signals on the FADC Module are carried on 75Ω strip or micro-strip transmission lines.

Copper planes for power distribution are utilized on the printed circuit board of the FADC Module. This provides ground planes for the strip and micro strip lines and results in lower I²R losses. To minimize the effects of digital noise on analog signals, separate analog and digital power and ground planes were implemented.

A. Analog Buffer

The analog buffer circuit was designed to drive the 8-bit Flash Analog to Digital Converter (FADC), provide dc offset (pedestal) control of the FADC, and have adjustable gain over a range of a factor of 2[3]. The buffer was fabricated using hybrid thick-film technology on a one by two inch ceramic substrate populated with surface mount components.

Two varieties of the analog buffer were designed - one having a linear gain and the other having a bilinear gain characteristic. **Figure 3.** compares the gain characteristics of the two buffer types. The bilinear function compresses large signals and effectively expands the system dynamic range from 8 to 9.5 bits. The function closely approximates two straight lines with a break point occurring at 1/4 of the buffer input range and 3/4 of the FADC input range. Gain below the break point ranges from nine to eighteen, above from one to two, while the break point remains fixed.

Instrumentation was designed to interface with the hybrid manufacturer's equipment during the active laser trimming process to enable the gain and break point values to be matched in all the buffer amplifiers within 1.5%. This proves accurate enough to enable compressed data to be "unfolded" using a single look-up table for all the channels in the central tracking detector.
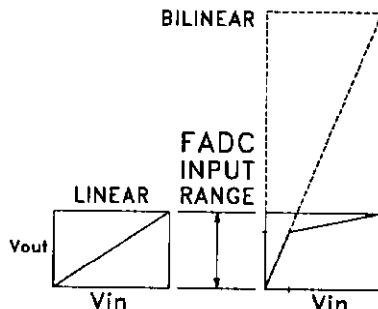
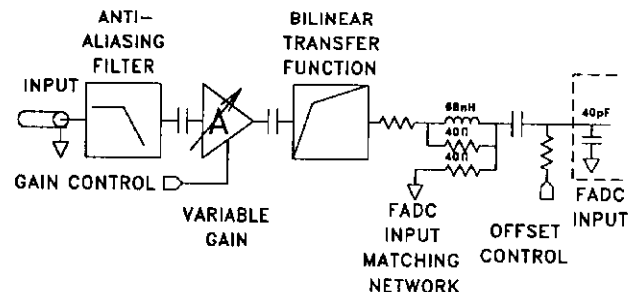**Figure 3** Analog buffer transfer functions

Figure 4 Bilinear buffer functional diagram.

The anti-aliasing filter is a low pass, 38MHz, five pole Bessel and matched to the 75Ω input cable. The linear group delay of the Bessel preserves pulse waveform shape.

Both the variable gain stage and the bilinear stage are designed with wide-band cascode amplifiers. In the linear buffer the bilinear function is defeated by eliminating a Schottky diode and a thermistor, and setting the gain of that stage to 2. The only circuit differences between the two buffers are the diode and thermistor, and one emitter resistor value.

To eliminate overshoot in driving the 40pF input capacitance of the FADC, a matching network was placed in series with the output as shown in **Figure 4**. All together, the bandwidth of the buffer is wide enough to allow the Bessel filter to define the hybrid's frequency characteristics.

Out of necessity, the various stages of the buffer are capacitively coupled. The resulting low end frequency response is about 250Hz. Capacitive coupling in the analog chain of the central tracking electronics will cause baseline shift in response to very large and/or very frequent signals from the detector.

B. Front End Memory Section

Each Front End Memory is divided into three sections of latch and digital delay line. The digital delay line is configured to operate as a First In First Out (FIFO) memory device. Data is written into the Front End Memory in three phase fashion, each section receiving every third 8 bit word. Each section of the Front End Memory requires control signals for operation. The design of the FADC Module takes advantage of the repetitive layout of the channels to deliver control and clock signals to groups of two channels, reducing the number of components required.

C. Clock Signal Distribution

There are four major operating clock frequencies found on the FADC Module, 106.208, 35.403, 26.552, and 16MHz. The 106.208 and 35.403MHz clocks, used to digitize and store data, are distributed as single ended ECL levels on 75Ω micro-strip lines. The 26.552MHz clock, used by the Zero Suppression Chips, are distributed on two, terminated, TTL level traces. The 16MHz VME system clock signal is used by the VME interface circuit. In an attempt to reduce the RF noise in the 106MHz spectrum, signal routing on the FADC Module is arranged so

that ECL clock signals on half of the module are 180° out of phase with similar signals on the other half.

D. Zero Suppression Chip

The Zero Suppression Chip (ZSP) found in each channel on the FADC Module is manufactured by the ASIC Components Division of the Intel Corp. for Fermilab. Implemented in 1.5 micron technology, the ZSP operates at a clock rate of 26.55MHz and dissipates approximately 1W from the +5V supply.

8 bit data words are read from the Front End Memory at a rate of 26.5MHz in response to an indication that interesting collision data has been stored. This indication is generated by the D0 Trigger Framework[4] system based on energy and momentum information, and is distributed to all FADC Modules by the Controller Card. The ZSP controls the Back End Memory, enabling data storage when pulses are found, disabling storage when they are not. The ZSP also stores the trailer information required by event processing equipment for pulse reconstruction and identification.

The ZSP implements a data reduction algorithm based on finding leading and trailing edges of pulses embedded in the input data stream. The ZSP analyzes the data read from the Front End Memory using 7 user programmable comparators, and recognizes leading and trailing edges by using a combination of slopes and/or thresholds. Once the leading edge of a pulse is detected, the ZSP enables the Back End Memory and stores output data there. This storage continues until the ZSP detects a trailing edge. As multiple pulses are possible in the digitized data, this enabling and disabling of the Back End Memory continues until a predetermined amount of data has been read from the Front End Memory. To facilitate pulse reconstruction, the ZSP adds trailer data to each pulse found. This data consists of the width of the stored pulse (in number of data bins) and the time slice (numerical position of bin in data stream) of the last bin of the stored pulse. The channel number and the total number of bytes (data and trailer) are also stored in the Back End Memory at the conclusion of this data processing cycle.

The algorithm implemented in the ZSP to find and store pulses can be described by the following boolean equations[5]:

$$LE = C_1 \cdot C_5 + C_2$$
$$TE = C_3 \cdot C_6 + C_4$$

Where LE is the indication that a Leading Edge condition has been met, and TE is the indication that a Trailing Edge condition has been met. The logicals C_1, C_2, C_3, C_4, C_5, and C_6 are internal condition flags defined as:

$$C_1 = (B_{i-2} > T1) \cdot (B_{i-1} > T1) \cdot (B_i > T1)$$
$$C_2 = (B_{i-2} \geq T2) \cdot (B_{i-1} \geq T2) \cdot (B_i \geq T2)$$
$$C_3 = (B_{i-2} < T3) \cdot (B_{i-1} < T3) \cdot (B_i < T3)$$
$$C_4 = (B_{i-2} < T4) \cdot (B_{i-1} < T4) \cdot (B_i < T4)$$
$$C_5 = (D_{i-1} > S1) \cdot (D_i > S1)$$
$$C_6 = (S2 > D_{i-1} > S3) \cdot (S2 > D_i > S3)$$

Where B_i is the value of the digitized waveform at time slice i and D_i is the difference of consecutive data values

B_i - B_{i-1}. The registers T1, T2, T3, and T4 contain voltage threshold values. The S1, S2, and S3 registers contain slope (difference) thresholds. Examples of a digitized waveform and computed difference as a function of time slice value are shown in **Figure 5**.
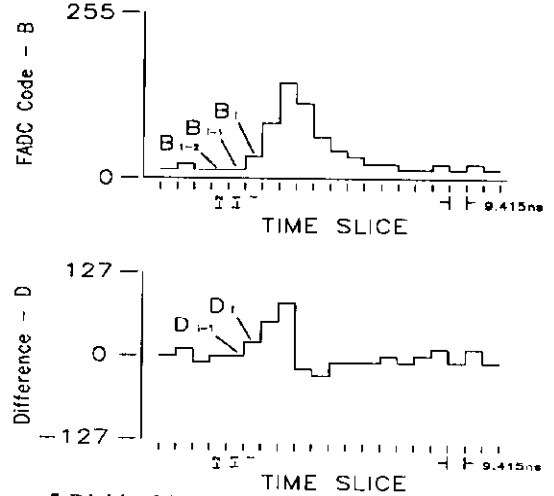

Figure 5 Digitized Waveform Definitions

The ZSP has a second mode of operation designed to be utilized by the TRD Trigger system[7]. In the SUM mode, the ZSP compares the accumulated sum of data passed though the device at the end of the process, to a user loaded register. This register value defines a threshold for energy deposited on the chamber wire (integrated voltage). If the accumulated sum of data exceeds this threshold, then a flag is set in an external VME readable register, and data stored in the Back End Memory is available for reading. If the threshold is not exceeded, the flag is not set and the ZSP only stores trailer data (channel number and channel length) in the back end memory. Cleverly chosen threshold values can be use to speed up the trigger decision process by reducing the number of FADC channels to read.

V. FADC CONTROLLER CARD

As the brains of the FADC Data Acquisition System the functions of the FADC Controller Card in the FADC VME crate are many. Differential ECL level 106.208MHz clock signals and bunch crossing indications are received from the D0 Clock System[6], delivered to a fan out network, and then driven as differential ECL level copies of the two signals to each FADC Module in the crate. Event identification numbers generated by the D0 Trigger Framework System are received and stored. The FADC Controller Card initiates the cycle in which digitized data, stored in the Front End Memory sections of all channel in the crate, is processed by the ZSP and stored in the Back End Memory for readout. The crate-wide pointer for selecting which of the two buffers in the Back End Memory, found on each channel, will be used for data storage and data retrieval, is controlled. The retrieval of FADC data for transfer to event analysis equipment is coordinated by handshaking with the VBD. In addition, the FADC

Controller Card provides facilities for diagnostic and test modes of operation.

The FADC Controller Card drives differential ECL level copies of the 106.208MHz clock and bunch crossing indications onto a custom backplane to each FADC Module in the crate. Considered in the design of the card are the different lengths of signal travel on the backplane. To reduce the effects of differing propagation delays on the backplane, signals which are to be driven to the nearest FADC Modules are driven onto the longest traces from driver to backplane connection. To provide a clock signal with optimal duty cycle for the FADC chips the FADC Controller Card reshapes the 106.208MHz clock duty cycle prior to fan out. Both signals can be controlled for diagnostic and/or test modes of operation.

As a group, the Central Tracking detectors are divided into twelve Geographic Sectors or sections. The design of the data acquisition system is such that each of the Geographic Sectors is capable of being triggered and running independently. To facilitate this operation, event identification numbers are assigned by Geographic Sector. The FADC Controller Card reads and stores this event identification number with each trigger. The VBD reads this number, along with other information, from the FADC Controller Card and forms an event header which is sent to the event processing equipment prior to FADC data.

In response to hardware processed energy and momentum sums from the Calorimeter and Muon detector systems, the D0 Trigger Framework System broadcasts a signal to FADC Controller Cards indicating that interesting information may be stored in the Front End Memory sections. Handshaking between the FADC Controller Card and the FADC Modules in the crate insure that stored data is not corrupted. The FADC Controller Card informs the FADC Modules that a cycle to process the stored data is imminent. The FADC Modules wait until the current data storage cycle is completed and any current VME data transfer cycles are finished before signaling the FADC Controller Card that they are ready to begin. Upon this notification, the FADC Controller Card issues the signal which starts the data processing cycle. When all channels in the crate indicate that they are finished processing stored data, the FADC Card instructs the VBD to begin it's readout process.

It is possible that the VBD might not complete it's readout process before another indication to process stored data from the D0 Trigger Framework arrives. In this case, the FADC Controller Card will repeat the handshaking with the FADC Module, but will change the crate-wide pointer for the Back End Memory sections. The FADC Module will pause current VME data transfer cycles with the VBD to permit the storing of the new processed data in Back End Memory sections. Once the storage of new data is complete, the FADC Controller Card restores the crate-wide pointer and VME data transfer cycles with the VBD, continuing the reading of the original stored data, resume. After the VBD completes the current process, the FADC Controller Card will change the pointer to the new data and instruct the VBD to again start its data transfer process to read the new stored data.

Two synchronous finite state machines, implemented in Erasable/Programmable Logic Devices are use to control the handshaking with the Trigger Framework System, all of the FADC Modules, and the VBD. State changes are synchronous with the 16MHz VME System Clock. Clock registered inputs and Gray code, used to define sequential states, are used to avoid glitches in the operation of the state machine. The FADC Controller Card has worked flawlessly at trigger rates several orders of magnitude greater than those expected during normal operation.

VI. OBSERVATIONS

All required FADC Modules and FADC Controller Cards have been installed and have been operational for a period of nearly one year. One cosmic ray data taking run has been completed with thousands of events passed to event analysis equipment. Numerous calibration and data-taking-software debugging runs have been taken. Noise studies of the FADC System find that an FADC Module with no input signals displays noise distributions of less than 1/2 LSB. Noise distributions of 1 1/2 LSB have been observed when Shaper Modules and detector pre-amplifiers are powered and connected. The D0 colliding beam detector is scheduled to come on-line in early 1992. With one year of nearly continuous operation under it's belt, the FADC Data Acquisition System is ready to do it's part.

VII. REFERENCES

[1],[7] M. Utes, et. al., "A TRD Trigger for the Tevatron Collider Experiment at D0," these proceedings, November 1991

[2] M. Martin, et al., "100 Mbs, 8 Bit Data Acquisition and Zero Suppression System for the D0 Detector," *IEEE Transactions on Nuclear Science*, Vol. 34, No. 1, pp. 258-260, February 1987.

[3] M. Martin, G Saewert, internal documentation, 1987.

[4] M. Abolins, et. al., "A High Luminosity Trigger Design for the Tevatron Collider Experiment in D0," *IEEE Transactions on Nuclear Science*, Vol. 36, No. 1, pp. 384-389, February 1989.

[5] M. Martin, "Zero Suppression Algorithm," internal communication, May 1986.

[6] C. Rotolo, et. al., " The Fermilab D0 Clock System," these proceedings, November 1991.