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PROCESS RESEARCH ON POLYCRYSTALLINE SILICON MATERIAL (PROPSM)

Quarterly Report No. 8 for the Period October 1—December 31, 1982

By
Jerry Culik
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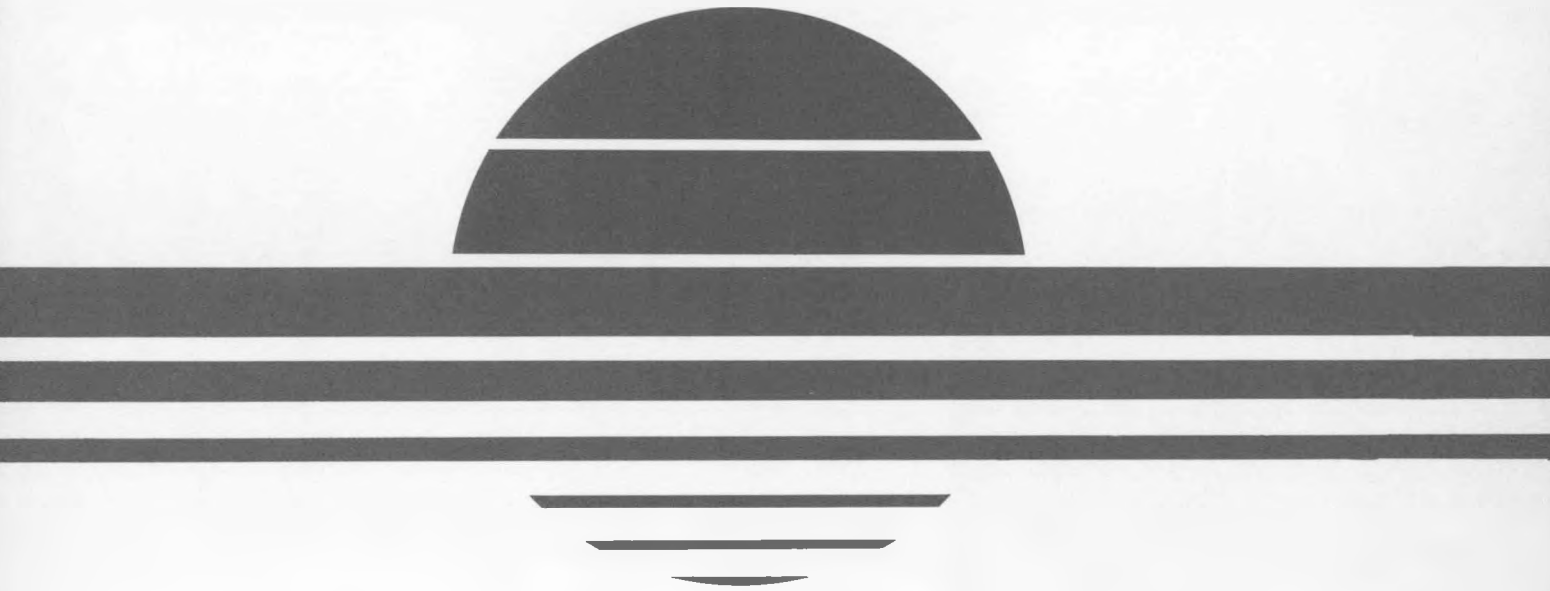

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The JPL Flat-Plate Solar Array Project is sponsored by the U.S. Department of Energy and forms part of the Solar Photovoltaic Conversion Program to initiate a major effort toward the development of low-cost solar arrays. This work was performed for the Jet Propulsion Laboratory, California Institute of Technology by agreement between NASA and DOE.

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ABSTRACT

Performance-limiting mechanisms in polycrystalline silicon were investigated by fabricating a matrix of 4cm^2 solar cells of various thicknesses from 10cm x 10cm polycrystalline silicon wafers of several bulk resistivities. During this quarter, the matrix was completed with the fabrication and measurement of Lots 5 and 7.

The analysis of the results for the entire matrix indicates that bulk recombination is the dominant factor limiting the short-circuit current in large-grain (greater than 1 to 2 mm diameter) polycrystalline silicon, the same mechanism that limits the short-circuit current in single-crystal silicon. The average open-circuit voltage of the polycrystalline cells is 30 to 70 mV lower than that of the single-crystal (control) cells; the fill-factor is comparable. Both open-circuit voltage and fill-factor have substantial scatter which is not related to thickness or resistivity. This implies that these parameters are sensitive to an additional mechanism which is probably spatial in nature since the cell position on the wafer was not controlled.

An experiment to investigate the limiting mechanisms of open-circuit voltage and fill-factor for large-grain polycrystalline silicon was designed. An array of small photodiodes (mini-cells), each approximately 0.20cm^2 in area,

will be fabricated across several 10cm x 10cm polycrystalline wafers. Current-voltage characteristics of each cell will be measured and used to locate areas of significantly lower open-circuit voltage, fill-factor, and short-circuit current. These areas will then be analyzed in depth using dark I-V analysis, light spot scanning, and dislocation content analysis to determine the cause of the degradation.

Two process sequences to fabricate these small cells were investigated during this quarter. For the first process sequence, cell-to-cell isolation was obtained by masking the wafer during diffusion (with SiO_2) so that a P-type silicon surface remains between neighboring cells. In the alternate process, cell isolation was realized by etching away silicon to form a mesa structure. This process sequence was ultimately chosen to fabricate the mini-cells because of its comparative insensitivity to process variables.

DESCRIPTION OF PROJECT

The purpose of this program is to determine the mechanisms affecting the conversion efficiency of polycrystalline silicon solar cells and, once knowing these mechanisms, to develop solar cell fabrication processes that take full advantage of its potential as a photovoltaic material. The primary emphasis of this work is on large-grain polycrystalline silicon as supplied by Semix, Inc. However, the results of this work are generic and will be applicable to all polycrystalline silicon materials.

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I. Introduction

This report summarizes the progress achieved during the third quarter of a program to determine the mechanisms affecting the conversion efficiency of polycrystalline silicon solar cells and, once knowing these mechanisms, to develop solar cell fabrication processes that take full advantage of its potential as a photovoltaic material.

Section II of this report summarizes the solar cell performance results that were obtained by fabricating a matrix of $4cm^2$ solar cells of various thicknesses from 10cm x 10cm polycrystalline silicon wafers of several bulk resistivities. This section also describes preliminary work on an experiment to fabricate an array of small ($< 0.2cm^2$) photodiodes across several 10cm x 10cm polycrystalline wafers. Section III presents the conclusions to date of this investigation of the fundamental mechanisms limiting the performance of polycrystalline solar cells.

II. Mechanisms Limiting the Performance of Polycrystalline Silicon Solar Cells

A. Thickness-Resistivity Matrix

The investigation of the performance-limiting mechanisms in polycrystalline silicon was begun by fabricating a matrix of $4cm^2$ solar cells of various thicknesses from polycrystalline P-type silicon wafers of several resistivities as supplied by Semix, Inc.

A high-efficiency process was used to fabricate the cells; the process sequence is shown in Figure 1 [1]. The wafers were thinned to the nominal thickness - 50, 100, 150, 200, 250 and 300 microns - using a CP-type etch; then diffused with phosphorus to a nominal 70 ohms/□ to form a thin N^+ layer and junction on both sides. The rear junction was compensated by the aluminum alloy to form a thick P^+ back surface field (BSF). Front and rear contacts were Ti/Pd/Ag; the front pattern was defined photolithographically. Finally, the wafers were sawn into 2cm x 2cm cells, and a Ta_2O_5 anti-reflection coating was applied. For each group of wafers, single-crystal control wafers were included to monitor the process.

Figure 1. Thickness-Resistivity Matrix Test Cell Process Sequence

1.	Thinning Etch:	CP-type; final thicknesses: 50, 100, 150, 200, 250, 300 microns.
2.	Diffusion:	Phosphine, tube diffusion; 70-80 ohms/□.
3.	BSF:	Englehard A-3484 aluminum paste, tube alloy, 30 seconds at 850°C; HCl post-alloy etch.
4.	Front Metallization:	Evaporated Ti/Pd contacts, photolithographically defined.
5.	Rear Metallization:	Evaporated Ti/Pd contacts.
6.	Electroplate Silver Conductor	
7.	AR Coating:	Evaporated Ta_2O_5

Due to the fragility of the 50 micron thick polycrystalline wafers, none survived the processing intact, and therefore no results are reported for 50 micron thick cells. Overall the yield increased with thickness, and some results for 100 micron thick wafers were obtained. Preliminary analyses of the data from lots 1, 2, 3, 4, and 6 were previously reported [2, 3]. Tables 1 through 7 summarize the results for the entire matrix, including lots 5 and 7 which were fabricated and measured during this quarter.

Table 1 shows the number of $4cm^2$ polycrystalline solar cells for each thickness and resistivity category by lot number. The resistivity of the polycrystalline silicon wafers fell into three ranges: "low resistivity", 0.5 to 0.6 ohm-cm; "medium resistivity", 1.0 to 1.9 ohm-cm; and "high resistivity", 4.2 to 6.5 ohm-cm.

The variation of short-circuit current with thickness and resistivity is shown in Table 2. The short-circuit current of the polycrystalline cells decreases as the resistivity decreases, just as it does with single-crystal (control) cells, as shown in Table 3. The dependence of the short-circuit current of the single-crystal cells on resistivity is attributed to the dependence of the minority carrier diffusion length on the dopant concentration. This

Table 1. Sample size; number of 4 cm^2 AR-coated cells in each thickness-resistivity category, by lot.

		THICKNESS (μm)					
	LOT NO.	100	150	200	250	300	ρ(ohm-cm)
LOW RESISTIVITY	6		20	26	20		0.4 - 0.6
MEDIUM RESISTIVITY	1		6	20	19		1.3 - 1.7
	2	7	5	12	13	19	1.0 - 1.9
	7	9	14	11	8		1.2 - 1.8
HIGH RESISTIVITY	3	5	9	19			5.5 - 6.5
	5		10	18	22	10	4.2 - 6.2

Table 2. Short-circuit current of 4 cm^2 AR-coated polycrystalline cells in each thickness-resistivity category, by lot. Measured at AMO, 135 mW/cm^2, 25°C.

		THICKNESS (μm)				
	LOT NO.	100	150	200	250	300
LOW RESISTIVITY	6		126(4)	127(4)	127(4)	
MEDIUM RESISTIVITY	1		132(6)	128(6)	126(15)	
	2	104(33)	132(2)	127(3)	135(7)	131(5)
	7	143(2)	146(2)	140(3)	142(2)	
HIGH RESISTIVITY	3	141(3)	141(2)	143(2)		
	5		145(4)	147(5)	146(6)	145(7)

Mean (standard deviation about mean), in mA.

Table 3. Short-circuit current of 4 cm^2 AR-coated single-crystal control cells in each thickness-resistivity category, by process group. Measured at AMO, 135 mW/cm^2, 25°C.

	Thickness (μm)						
	50	100	150	200	250	300	ρ(ohm-cm)
LOW RESISTIVITY		145(2)	149(2)	148(2)			0.7
		145(1)	146(2)	147(3)	148(2)		0.7
MEDIUM RESISTIVITY	145(3)	154(2)	159(1)	155(2)	159(1)	159(2)	1.7
			155(2)	155(4)	155(1)		1.7
HIGH RESISTIVITY		153(3)	159(3)	162(3)	164(1)	163(1)	7-22
	146(3)	151(4)	151(2)	150(3)			13-18
			156(3)	164(5)	161(2)	159(3)	10-16

Mean (standard deviation about mean), in mA.

behavior, though not well understood, is at least well known for Czochralski single-crystal silicon [4, 5, 6]. The variation of the short-circuit current of the single-crystal cells with base thickness is also related to minority carrier diffusion length. If the base width is less than the minority carrier diffusion length, then nearly all of the carriers that are photogenerated will be collected; as the base width increases, the amount of light absorbed and the short-circuit current also increase. The short-circuit current will continue to increase with cell thickness until the base width is approximately equal to the minority carrier diffusion length. When the base width is greater than the minority carrier diffusion length, even though additional carriers may be generated deeper in the bulk they will not be collected. Therefore, at some base thickness approximately equal to the minority carrier diffusion length, the short-circuit current will saturate. This current saturation is clearly seen for the single-crystal (control) cells. For each lot of wafers, the short-circuit current increases with cell thickness until it saturates. As the resistivity increases, and therefore the minority-carrier diffusion length increases, the cell thickness at which the short-circuit current saturates also increases. This behavior, though less clearly seen, is nevertheless also present for the polycrystalline cells. However, the short-circuit current

of all polycrystalline cells appears to have saturated for cell thicknesses greater than 150 microns. This fact, together with the short-circuit currents for the polycrystalline cells being five to ten percent lower than those of single crystal cells of similar resistivity, indicates that the minority carrier diffusion length of the polycrystalline material is less than that of the single crystal silicon wafers.

It does not appear that the reduced short-circuit currents are the result of recombination at the grain boundaries. If this were the case, then there should be even more scatter in the data since no attempt was made to control the grain size, which varied from about 1 to 10 mm in diameter. With the exception of the cells from Lot 1 and the 100 micron thick cells of Lot 2, the scatter in the short-circuit current of the polycrystalline cells is equivalent to that of the single-crystal control cells, that is, three to four percent. This result is consistent with the previous work - both theoretical and experimental - which shows that the light-generated current is not substantially affected by recombination at the grain boundaries when the grain diameter is several times larger than the minority carrier diffusion length [7, 8]. For a diffusion length of 100 to 150 microns, as indicated by the behavior of the short-circuit current with thickness and resistivity, this dimension would be on the order of 1 to 2 mm. In most present examples of cast polycrystalline

silicon (Semix, Wacker, HEM) the grain size is consistently equal to or greater than this dimension. Hence, the short-circuit current of these materials should be dominated by bulk properties, rather than grain boundary recombination. This also implies that forming polycrystalline silicon with grain diameters larger than several diffusion lengths, or even passivating the grain boundaries of smaller-grain (grain diameter equal to minority carrier diffusion length) polycrystalline silicon, will not result in any substantial increase in short-circuit current. Improvements in the short-circuit current of large-grain polycrystalline silicon, at most five to ten percent, will be mainly due to elimination of the sources of recombination in the bulk.

The results for the open-circuit voltage of the polycrystalline cells in the thickness-resistivity matrix are shown in Table 4. Although there is some indication that the open-circuit voltage increases as the resisitivy decreases, it is very difficult to conclude that dopant concentration is the dominant factor because the scatter in the data ranges from less than one percent to more than fifty percent. Likewise, it is difficult to establish any clear dependence of open-circuit voltage on thickness, though in some lots the thinner cells did have slightly higher values of open-circuit voltage.

Table 4. Open-circuit voltage of 4 cm^2 AR-coated polycrystalline cells in each thickness-resistivity category, by lot. Measured at AMO, 135 mW/cm^2, 25°C.

		THICKNESS (μm)				
	LOT NO.	100	150	200	250	300
LOW RESISTIVITY	6		577(24)	583(8)	580(8)	
MEDIUM RESISTIVITY	1		559(5)	559(19)	559(14)	
	2	333(158)	539(36)	538(67)	555(16)	553(11)
	7	587(4)	586(3)	573(10)	582(4)	
HIGH RESISTIVITY	3	573(8)	570(4)	570(5)		
	5		570(13)	552(30)	566(16)	559(19)

Mean (standard deviation about mean), in mV.

For comparison, Table 5 gives the results of the open-circuit voltage of the single-crystal (control) cells. As expected, the open-circuit voltage increases as the resistivity decreases and, because of the back surface field, is not very sensitive to thickness. The average open-circuit voltage of the single-crystal cells is 30 to 70 mV greater than that of the polycrystalline cells in the same thickness-resistivity category. For most single-crystal control groups the scatter is within 10 mV of the mean, that is, less than two percent. In the worst case the scatter is about five percent of the mean. Hence, the scatter in the open-circuit voltage of the polycrystalline cells is significantly greater than that of the single-crystal (control) cells.

Most of the thickness-resistivity groups of polycrystalline cells which showed very large amounts of open-circuit voltage scatter also had a very high average shunt conductance, as shown by the shunt conductance data in Table 6. In these groups the low open-circuit voltage, and also the scatter, were most likely the direct result of excessive shunt conductance. However, one group, the 150 micron thick cells of Lot 2, had shunt conductances which could in no way account for the low average or the scatter in the open-circuit voltage. In addition, polycrystalline cells with moderate amounts of open-circuit voltage scatter

Table 5. Open-circuit voltage of 4 cm^2 AR-coated single-crystal (control) cells in each thickness-resistivity category, by process group. Measured at AMO, 135 mW/cm^2, 25°C.

	THICKNESS (μm)					
	100	150	200	250	300	(ohm-cm)
LOW RESISTIVITY	601(4)	607(4)	602(5)			0.7
	607(4)	612(3)	612(6)	609(2)		0.7
MEDIUM RESISTIVITY	601(8)	608(2)	606(3)	604(3)	606(1)	1.7
	606(2)	599(10)	600(9)	603(3)		1.7
HIGH RESISTIVITY	580(15)	590(5)	598(3)	596(4)	600(3)	10-20
	598(3)	599(2)	593(26)			13-18
		602(2)	607(3)	601(5)	590(15)	10-15

Mean (standard deviation about mean), in mV.

Table 6. Shunt conductance of 4 cm^2 AR-coated polycrystalline cells in each thickness-resistivity category, by lot.

		THICKNESS (μm)				
	LOT NO.	100	150	200	250	300
LOW RESISTIVITY	6		19.70(41.5)	2.49 (4.59)	3.31 (3.74)	
MEDIUM RESISTIVITY	1		1.12 (1.72)	7.59 (4.58)	2.25 (3.33)	
	2	110. (63.)	2.47 (2.11)	33.2 (88.7)	26.5 (51.6)	3.89(3.67)
	7	0.35 (0.28)	0.56 (0.58)	1.69 (1.78)	0.99 (1.00)	
HIGH RESISTIVITY	3	21.9 (27.7)	5.58 (5.16)	7.50 (9.81)		
	5		4.31 (6.63)	63.7 (86.1)	0.56 (1.23)	1.73(1.66)

Mean (standard deviation about mean), in mmho.

($\pm$5 to $\pm$20 mV) invariably had shunt conductances that were so low as to have no significant effect on the open-circuit voltage.

The lower average open-circuit voltage (20 to 50 mV lower than single-crystal control cells) and the scatter in the open-circuit voltages of the non-shunted polycrystalline cells appears to indicate that there is a voltage-controlling mechanism, not present in the single-crystal (control) cells, which is limiting the open-circuit voltage.

A comparison of the fill-factor of the polycrystalline cells to that of the single-crystal (control) cells is shown in Table 7. As with the open-circuit voltage, most of the groups with large amounts of scatter were also badly shunted; the shunts were very likely the cause of the low fill-factors as well as the low open-circuit voltages. The average fill-factor of most of the groups of non-shunted polycrystalline cells was not significantly different from that of the single-crystal (control) cells. However, the fill-factor of four polycrystalline groups (Lot 6 - 250 microns; Lot 2 - 150 microns; and Lot 3 - 150 and 200 microns) was much lower than that of their single-crystal controls, and not because of shunting. This indicates that, while there does not appear to be any fundamental

Table 7. Comparison of fill-factor (in %) of polycrystalline and single-crystal (control) cells in each thickness-resistivity category, by lot.

		THICKNESS (μm)				
	LOT NO.	100	150	200	250	300
LOW RESISTIVITY	6		68(11) 80 (1)	73 (3) 77 (6)	71 (5) 79 (1)	
	1		76 (2) 75 (1)	75 (2) 76 (1)	75 (4) 76 (1)	
MEDIUM RESISTIVITY	2	32(8) 74(7)	70(10) 80 (1)	70(14) 80 (1)	68(13) 78 (2)	74 (3) 78 (1)
	7	76(1) 76(1)	76 (1) 77 (2)	75 (1) 78 (2)	76 (2) 79 (1)	
	3	70(7) 75(5)	64 (4) 78 (1)	64 (4) 77 (1)		
HIGH RESISTIVITY	5		75 (2) 77 (1)	64(15) 77 (3)	75 (1) 77 (3)	75 (1) 71(11)

limit to fill-factor in large-grain polycrystalline silicon, there is a mechanism, not present in single crystal silicon, which can reduce the fill-factor in some polycrystalline samples.

B. Mini-Cell Wafer Evaluation

The scatter in both the open-circuit voltage and the fill-factor of the polycrystalline cells in the thickness-resistivity matrix indicates that there is an additional performance-limiting mechanism not associated with bulk properties - specifically base thickness or resistivity. The degradation of both the open-circuit voltage and the fill-factor seems to have a spatial nature because each group contains individual cells with very good I-V characteristics (as shown by the sum of the mean plus one standard deviation) even though the average open-circuit voltage or fill-factor might be low. Since the location of any particular cell on a wafer was not controlled, this position-dependent scatter is implicit. Therefore, an experiment was designed to determine, first, the location of cells with degraded I-V characteristics, and, second, the fundamental cause of the degradation. To achieve these objectives an array of up to 400 small (approximately 0.20cm^2 in size) cells will be fabricated on a selection of cast polycrystalline silicon wafers

(10cm x 10cm), and the I-V characteristics of each test cell ("mini-cell") will be measured to create a map of each I-V parameter - open-circuit voltage, short-circuit current, and fill-factor. This map will be used to locate areas on the wafers where the mini-cells have degraded open-circuit voltages and fill-factors. The mini-cells will be characterized using dark I-V analysis to determine the dark quasi-neutral and space-charge recombination current components and diode-quality (N) factor. Light spot scanning [6] will be used to characterize the grain boundaries, and the dislocation density will be determined and correlated to the grain boundary structure and dark current qualities in order to determine the cause of the degradation. The work this quarter consisted of evaluating two potential process sequences for fabricating the mini-cells.

One important processing requirement in the mini-cell experiment is isolation between neighboring test cells. One process, designated Process I, obtains this isolation by masking the wafer during diffusion (with SiO_2) so that a P-type silicon surface remains between the test cells, as shown in Figure 2A. Test cell isolation in the alternative process, Process II, is realized by etching away silicon, as shown in Figure 2B.

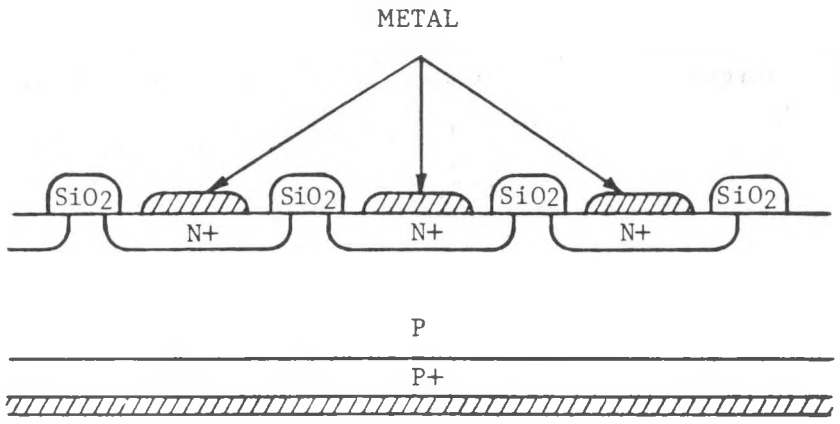

Figure 2A. Oxide diffusion mask isolation test structure (Process I).

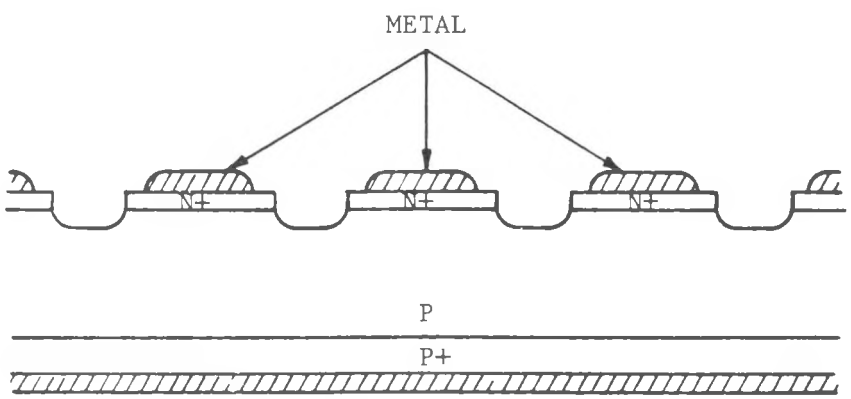

Figure 2B. Mesa etch isolation test structure (Process II).

Figure 2. Mini-cell test structures.

The advantage of the Process I sequence is that contact pad alignment is not critical; a misaligned pad will be isolated from the base by the oxide. The disadvantages are that a high temperature step is necessary to grow the oxide (or densify a deposited oxide), that there may be pinholes in the oxide which would act to reduce the isolation, and that there could be an electrostatically-induced inversion layer which would negate the attempted isolation.

The advantages of the Process II sequence are the elimination of the high temperature oxide-growing step that is not characteristic of normal solar cell processing, and the virtual guarantee of junction isolation. The disadvantage is that contact pad alignment becomes important - any metal not on the diffused region could shunt the junction.

A small group of $1cm^2$ (1cm x 1cm) cells was fabricated to evaluate these two isolation techniques (this cell size is larger than the mini-cell, but was chosen to keep the amount of data to a manageable level). The actual process sequences used are shown in Figures 3 and 4. Note that only single-crystal silicon was used in this group in order to eliminate variations due to material; this trial was to concentrate solely on processes.

Figure 3. Process Sequence for Oxide Diffusion Mask Isolation (Process I).

1. Etch 1-3 ohm-cm silicon wafer to 250±10 μm thickness.

2. Diffusion Mask:
   - Grow Oxide
   - Spin Photoresist
   - Open Windows in Resist
   - HF Etch to Open Windows in Oxide
   - Strip Resist

3. Diffusion: 80 ohm/□

4. BSF:
   - Aluminum Paste
   - Bake
   - Alloy
   - HCl Etch

5. Front Metallization:
   - Spin Photoresist
   - Open Windows for Pads
   - Evaporate Ti/Pd
   - Liftoff

6. Rear Metallization: Ti/Pd

7. Electroplate Ag

8. Sinter

Figure 4. Process Sequence for Mesa Etch Isolation (Process II).

1. Etch 1-3 ohm-cm silicon wafer to 250±10 μm thickness.

2. Diffusion: 80 ohm/□

3. Mesa Etch Mask: Spin Photoresist
   Open Window Frame in Resist

4. Mesa Etch (CP-Type, 10 μm Removed)

5. Strip Resist

6. BSF: Aluminum Paste
   Bake
   Alloy
   HCl Etch

7. Front Metallization: Spin Photoresist
   Open Windows for Pads
   Evaporate Ti/Pd
   Liftoff

8. Rear Metallization: Ti/Pd

9. Electroplate Ag

10. Sinter

A comparison of the two process sequences as far as cell I-V characteristics is summarized in Tables 8 and 9 which show the mean and standard deviation about the mean of the open-circuit votage, fill-factor and shunt conductance for the two process sequences. A number of test cells fabricated with the Process II sequence had misaligned contact pads, were shunted, and had characteristically lower open-circuit voltages. These cells were excluded from the wafer averages. The fill-factor of all of these cells is low due to high series resistance since the sheet resistance of the diffused layer was higher than expected (120 ohms/□) and the top contact is just a stripe pad without gridlines. Comparison of the two process sequences shows that the average open-circuit voltage of the Process II cells (mesa etch isolation) is higher than that of the Process I cells (oxide diffusion mask isolation), although the absolute values for both are somewhat low. These low open-circuit voltages appear to be related to processing, particularly since the shunt conductance is inconsistent, at best.

TABLE 8. Oxide Diffusion Mask Isolation (Process I) I-V Characteristics.

Wafer No	Number of Cells	V_{oc} (mV)	FF	G (mmho)
2A	15	555 (37)	.39 (.02)	.62 (.40)
4A	25	556 (26)	.36 (.04)	.30 (.25)
5A	20	547 (47)	.40 (.01)	.44 (1.15)

TABLE 9. Mesa Etch Isolation (Process II) I-V Characteristics: (Without Cells With Misaligned Pads).

Wafer No.	Number of Cells	V_{oc} (mV)	FF	G (mmho)
1B	20	572 (27)	.41 (.02)	.78 (1.23)
2B	20	577 (9)	.40 (.03)	.36 (.28)
3B	15	565 (25)	.35 (.03)	2.07 (2.30)

Mean (Standard deviation about mean)

The cell-to-cell isolation was evaluated by applying a voltage of 100 mV between two adjacent cells and measuring the leakage current (in μA). A scatter plot showing the results of this measurement is given in Figure 5. For nearly every case, whether for isolation due to the oxide diffusion mask or due to the mesa etch, the leakage current was less than 100 μA, which corresponds to an effective cell-to-cell isolation resistance greater than 1,000 Ohms. An isolation resistance closer to 10 KOhms was more common.

The choice between the two mini-cell process sequences is based not only on test cell performance and isolation, but also on ease of fabrication since a more complicated process sequence will inevitably result in a decreased yield of usable samples. The process II sequence, the mesa etch isolation, contains one less high temperature step and is less sensitive to processing variables. The only critical step is the alignment of the contact pad mask, and problems with this step are obvious: one can visually verify the pad photoresist registration before metallization. If the pattern is misaligned, the photoresist can be stripped and the patterning repeated correctly. Because of this insensitivity to process variables, the mesa etch isolation process sequence was chosen for use in fabricating the mini-cell wafers.

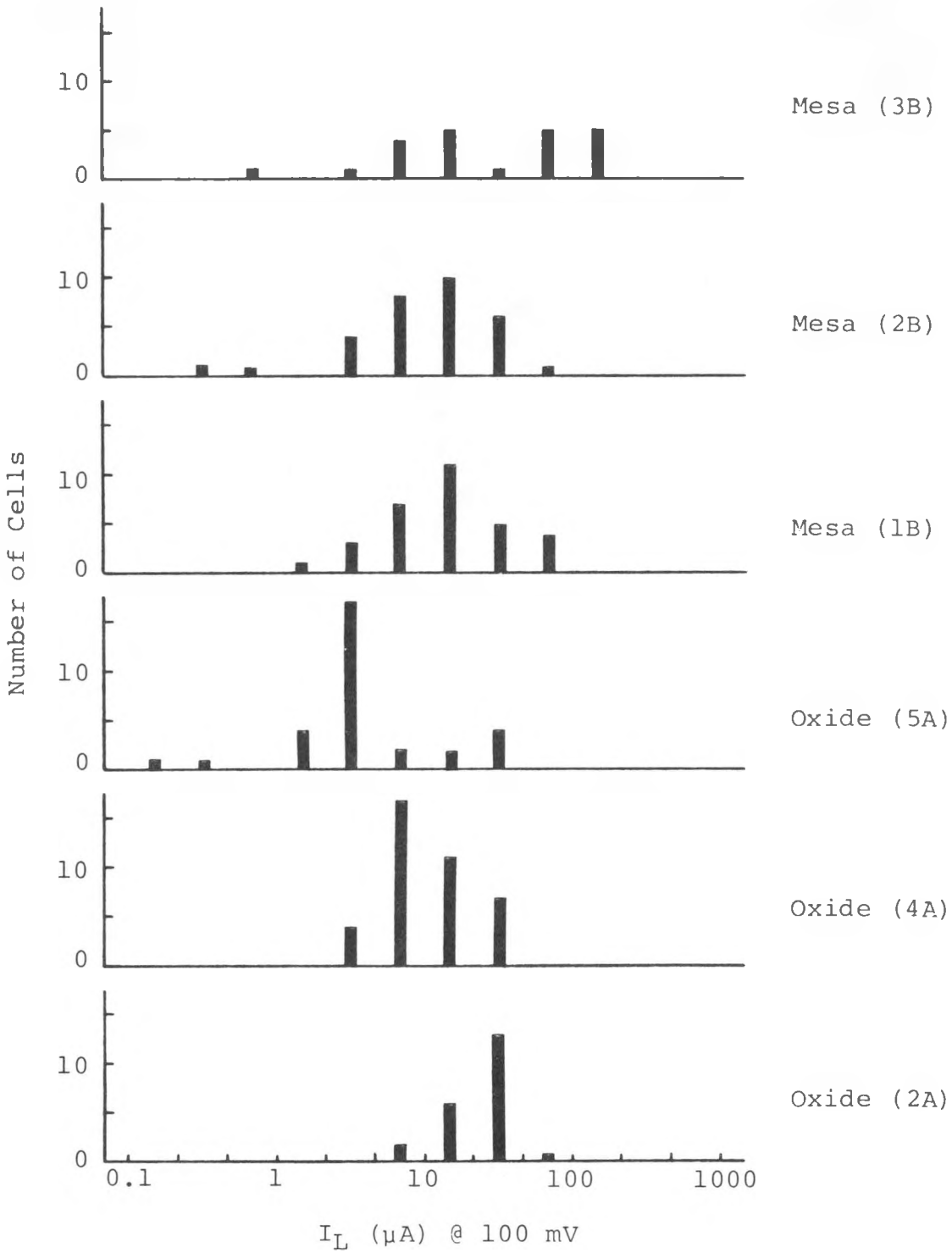

Figure 5. Scatter plot of leakage current (at 100 mV cell-to-cell bias voltage) for the two mini-cell process sequences.

III. CONCLUSIONS

Investigation of the performance-limiting mechanisms in polycrystalline silicon was initiated by fabricating a matrix of $4cm^2$ solar cells of various thicknesses fom 10cm x 10cm polycrystalline wafers of several bulk resistivities. During this quarter, the matrix was completed.

Analysis of the results of the thickness-resistivity matrix indicates that the short-circuit current of large-grain (greater than 1-2 mm diameter) polycrystalline silicon is dominated by recombination of photogenerated minority carriers in the bulk, as opposed to recombination at the grain boundaries. This result is in agreement with previous theoretical and experimental results which indicate that the light-generated current is not substantially affected by recombination at the grain boundaries when the grain diameter is several times larger than the minority carrier diffusion length. However, it also implies that improvements in the short-circuit current of large-grain polycrystalline silicon will be mainly due to elimination of sources of recombination in the bulk.

Both the open-circuit voltage and fill-factor of the cells in the thickness-resistivity matrix had substantial amounts of scatter which were not related to the main experimental variables - thickness and bulk resistivity. The scatter in the

values of open-circuit voltage and fill-factor implies that there is an additional performance-limiting mechanism which may not be strongly associated with bulk properties. The degradation of these parameters appears to have a spatial nature and to be related to the grain structure since the grain boundary content of any particular cell on a wafer was not controlled. Therefore, an additional experiment is necessary to establish, if possible, the relationship between grain structure and degradation of the open-circuit voltage and fill-factor.

This experiment, to measure an array of small photodiodes across a 10cm x 10cm wafer, was designed to determine, first, the location of cells with degraded I-V parameters, and, second, the fundamental cause of the degradation. The work this quarter consisted of developing and evaluating two alternate methods of fabricating the mini-cell wafers. A process sequence which resulted in cells which had junction isolation due to a mesa structure was chosen for use in fabricating the actual mini-cell wafers. This sequence was relatively insensitive to process variables, had the least probability of modifying the bulk properties (for a diffused junction), and resulted in test cells which had consistently high isolation resistance.

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