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A RADIATION-HARDENED BULK CMOS TECHNOLOGY*

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Introduction

This paper will review the evolutionary development of a radiation-hardened bulk CMOS technology. The metal gate hardened CMOS status will be summarized, including both radiation and reliability data. This paper will also discuss the development of a radiation-hardened bulk silicon gate process which was successfully implemented to a commercial microprocessor family and applied to a new, radiation-hardened, LSI standard cell family. The cell family will be reviewed and preliminary characterization data will be presented. Finally, a brief comparison of the various radiation-hardened technologies with regard to performance, reliability, and availability will be made.

The metal gate CMOS technology was originally chosen for radiation-hardening because many systems required low standby power dissipation, and the inherently superior CMOS noise margins allowed greater radiation-induced threshold voltage shifts without significant performance degradation.

The thrust of the metal gate hardening effort was directed toward hardening the gate oxide and relying upon diffused guardrings to prevent radiation-induced inversion of the p-well field oxide. Briefly, the experimental results showed that the gate oxidizing ambient and temperature, as well as the gate anneal, had a major effect on the gate oxide hardness. The gate metallization process was another critical operation, as e-beam metallization deposition introduced unannealable damage that resulted in large p-channel threshold voltage shifts after irradiation.

Other process parameters, such as the silicon orientation and surface quality, preoxidation clean, and metallization sinter ambient, were not as deleterious to the gate hardness. One significant result of the hardness study was the discovery that the radiation-induced threshold voltage shift was proportional to the cube of the oxide thickness; thus, significant improvements in hardness would be achieved by reducing the gate thickness. The Sandia metal gate hardened process now utilizes a 700 Å, 1000°C-100 percent O_2 gate oxidation without an anneal with an in-source aluminum metallization.[1-3] The threshold voltage shift, as a function of total dose for this process, is illustrated in Figure 1.

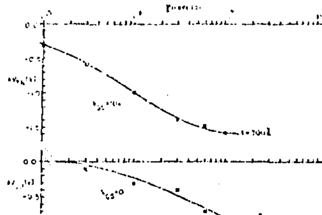

FIGURE-1
THRESHOLD VOLTAGE SHIFTS VS TOTAL DOSE FOR METAL GATE CMOS

To summarize the present radiation-hardened metal gate CMOS status, over 40 custom chips have been designed and evaluated for systems use, and 4000-series hardened parts are available from several sources. Megarad capability has been well established, and the process has demonstrated an MTBF capability in excess of 1000 hours for a 200°C biased life test. The disadvantages of this technology, however, are its limited performance (≤5 MHz) and packing density (~1500 transistors in a standard cell random logic chip configuration). These limitations of the metal gate technology for the military systems use have forced, as they did in the commercial world, the development of a hardened silicon gate technology.

Hardened Silicon Gate Technology

The bulk CMOS silicon gate radiation hardening technology development was built upon the hardened metal gate process. In particular, a 1000°C-100 percent O_2 gate oxidation with a nominal 600 Å thickness is used, and all post-gate thermal cycles are minimized. The polysilicon deposition is done at 700°C and is followed by an 850°C phosphorous diffusion to obtain a polysilicon sheet resistance of 50 Ω/□. After the polysilicon delineation, the n^+ and p^+ junctions are formed by a masked ion implantation. The implantation activation occurs during the high temperature (850-950°C) interlevel oxide deposition. The high-temperature oxide, which achieves good step coverage, is used for this layer since the radiation hardness constraints preclude the conventional reflow cycle used to achieve good interlevel step coverage. The metallization is an induction-source Si-Al alloy, and after metal delineation the sinter and passivation complete the process cycle.

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This process sequence permits fabrication of bulk silicon gate circuits that may operate after a 1×10^{6} rad (Si) exposure. The n- and p-channel threshold voltage, as a function of radiation, is illustrated in Figure 2. As with the metal gate technology, the dip in the n-channel threshold voltage as a function of irradiation requires that the pre-radiation value must be above the typical nonhardened value to prevent depletion-mode operation. The increase in p-channel threshold voltage as a function of dose also infers that hardened circuits will typically operate at a lower frequency than their nonhardened counterparts. As a result of the asymmetric threshold shifts, extensive circuit analysis must be performed to insure that race conditions will not arise as the p-channel threshold voltage increases while the n-channel threshold voltage decreases.

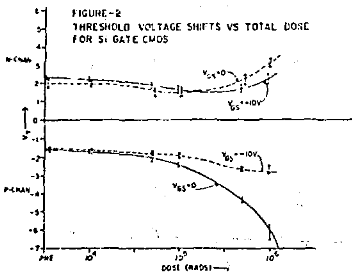

FIGURE-2
THRESHOLD VOLTAGE SHIFTS VS TOTAL DOSE FOR Si GATE CMOS

The other aspect of total dose hardening is the field region, which with megarad exposures, can exhibit negative threshold voltage shifts in excess of 100 volts. For typical p-well surface concentrations, field inversion will occur between $5\text{-}10\times10^{3}$ rads, causing dramatic increases in I_{DD}. For the metal gate technology, where the n^{+} and p^{+} diffusions are formed prior to the gate metallization, guardrings can be implemented at no processing expense. For the silicon gate technology however, the conventional guardring formation, which of necessity is accomplished prior to the polysilicon deposition, requires an additional photodelineation and diffusion. The guardbanding can also be achieved by using the $C^{2}L$ layout technique, which has no field oxide underneath polysilicon and diffused source planes underneath the metallization.[4] There is, however, a significant packing density penalty for multiple input gates when $C^{2}L$ layout techiques are utilized.

The bulk CMOS technology also requires hardening for transient ionizing radiation since parasitic SCRs, which exist in all bulk CMOS circuits, can latch-up in a transient environment. Analyses of the bulk latch-up phenomenon have, however, suggested several generic solutions to the latch-up problem.[5] Minority carrier lifetime control, such as gold doping or neutron irradiation, reduces the parasitic bipolar gain such that SCR action is physically impossible.[5,6] An attractive feature with this approach is that the parasitic gains can be measured at wafer probe to confirm transient latch-up hardness. Both the gold doping technique[7] and neutron irradiation have been successfully implemented on commercial parts and offer a well controlled technique for latch-up prevention.[8] Neutron irradiation is particularly attractive since it is a low-temperature, noncritical, post-processing step that requires no modification of normal processing steps. The annealing characteristics of the neutron damage have been modeled and fit to experimental data, which confirms the long-term reliability of this process. To date, over 13,000 packaged metal-gate parts and over 6,000 die have been neutron irradiated and sampled for latch-up. Parametric and life tests indicate no deleterious effects from the neutron irradiation.[8]

The use of an epitaxial substrate will also prevent latch-up by shunting the parasitic SCR and forcing the holding current to exceed a value that the chip will support.[5,9] This technique may be more attractive to commercial vendors than either the gold doping or neutron irradiation since it is easier to implement and, moreover, epitaxial circuits do not exhibit the slightly increased leakage current, especially at high temperature, associated with reduced lifetime.

The first application of the hardened bulk CMOS silicon gate technology was to implement a hardened version of an existing microprocessor family for use in a satellite system with a severe radiation environment. Power constraints required CMOS, and the existing RCA 1800 family, using the $C^{2}L$ technology, appeared the most amenable to hardening. A joint Sandia-RCA program was established to develop and implement the hardened technology on the 1800 family using the 1802 microprocessor, TCC-244 256x4 RAM, and 1834 1024x8 ROM.[10] As discussed earlier, the first step in the hardening effort included extensive circuit simulation to insure that the circuits would function through the range of radiation-induced threshold voltage shifts. The simulations, confirmed by a comprehensive test program, indicated race conditions only in the 256x4 RAM circuit, which subsequently was redesigned to eliminate the problems.

The radiation testing utilized a Co^{60} source at an exposure rate of 1×10^{6} rads/hour. The microprocessor was irradiated with a 10 kHz clock

applied; the RAM and ROM were both exposed with a static bias, which is a worst-case exposure. These bias conditions are representative of typical system operation which requires continuous 2 MHz clocking of the microprocessor with most of the RAM and ROM circuits on standby. The circuits were irradiated at room temperature and then tested within 1 hour of the exposure to minimize annealing.

The primary radiation failure mode of the 1802 microprocessor and 1834 ROM was due to the large p-channel threshold voltage shift which causes unacceptable degradation in p-channel output drive and circuit operational frequency. For custom radiation-hardened circuits, the p-channel devices are usually enlarged to minimize the effects of the threshold voltage degradation.

The primary RAM radiation failure mode is related to the bias-dependent, radiation-induced threshold voltage shift, which produces a preferred state for the memory cells. The irradiation of a biased flip-flop memory cell tends to increase the drive of the "off" inverter relative to the "on" inverter. This leads to the generation of a preferred state which increases the write time, and radiation failure typically occurs when the device fails this specification. However, for a high-dose but long-term exposure environment where the memory cells would normally be cycled many times, this imprintation will not occur, and the hardness level is greater than that attainable in the static bias condition.

Table I summarizes the pre- and post-irradiation electrical parameters for the radiation-hardened devices. Presently, over 600 high rel devices have been burned-in under bias for 168 hours at 150°C with a failure rate of less than 5 percent.

TABLE I

TCC-244 ELECTRICAL-RADIATION CHARACTERISTICS

	Pre-Rad	$1x10^5$	$5x10^5$	$1x10^6$
I_{DN} (mA)	4.0-5.0	4.0-5.0	3.0-4.0	2.0-3.0
I_{DP} (mA)	2.5-3.0	2.4-2.9	2.0-2.5	1.0-1.5
T_{AA} (ns)	150-240	150-240	250-350	500-750
T_{WW} (ns)	40-60	45-65	70-110	140-220
I_{DD} (A)	.5-50	.5-50	1.0-110	1.0-100

Data represents range of 5 lots

This program has successfully demonstrated the implementation of a radiation-hardened bulk CMOS process to a commercial microprocessor family. Total dose hardness under worst-case bias at $5x10^5$ rads and transient upset hardness of $5x10^8$ rads/sec, with no latch-up at any level, has been achieved. To date, over 600 high reliability, radiation-hardened 1802s, TCC-244s, and 1834s have been delivered for use in satellite systems.

ELA Cell Family

In parallel with the radiation-tolerant Si-Gate bulk CMOS process development, a complete new standard cell family utilizing all the advantages afforded by a self-aligned polysilicon gate structure has been developed. Designated the Expanded Linear Array (ELA), the principal objectives of the technology are higher density, increased speed of operation, greater topological design flexibility and radiation hardness. Packing densities of 1,000 gates/die, 3-8 ns gate delays and 20 MHz counter operation are the goals of this ELA technology.

In designing the Si-Gate standard cell family, prime consideration was given to topological flexibility. Past experience with a metal gate CMOS standard cell family dictated cell layout techniques and design rules that would allow new cells to be designed easily and quickly with a minimum amount of design experience. Additionally, existing cells can be modified to take advantage of design rule shrinking without a large investment in manpower.

To accomplish these goals, cells are arranged in a linear array where all n and p transistors have equal channel length-to-width ratios. This is illustrated in Figure 3, which depicts an ELA structure for a two-input gate. The vertical polysilicon gate lines are on a fixed horizontal pitch of 20 microns, and metal interconnects tie the appropriate regions to one another. The standard cell height (150 microns) was determined by performing extensive simulations to arrive at a reasonable compromise between cell performance (drive and speed) and density. This compromise results in a cell height that is 30 percent larger than the minimum possible height dictated only by layout design rules. Briefly, the cell height was adjusted so that the inherent layout capacitance of a two-input gate equalled the input capacitance resulting from a fan-out of two for similar gates. The n and p devices have channel widths of 38 μm and 77 μm, respectively, to account for the difference in mobility for the two types of silicon. It should be noted that increasing the device sizes to attain higher drive capability simply requires a straightforward vertical stretch of all cells.

FIGURE-3
2 INPUT OR/NOR GATE

Another very important advantage of the linear array layout approach apparent from Figure 3 is that cell inputs and outputs are accessible from both the top and bottom of each cell; this dual-port approach yields tremendous advantages in standard cell chip layouts and makes the cell family particularly attractive for use with computer design aids such as automated layout programs.[11] Layouts can be generated with a negligible amount of end-around wiring channels characteristic of layouts accomplished with single port cells. Additionally, the end cap of most cells can be utilized as an intercell row feedthrough to further minimize end-around wiring channels. An automated layout program named SICLOPS,[12,13] capable of taking full advantage of the two-ported cell structure to produce optimized random logic layouts, is presently under development at Sandia.

In addition to utilizing radiation-hard processing techniques which minimize charge buildup in oxides, the ELA cell family layout technique completely isolates all devices. This is accomplished, as illustrated in Figure 3, by:

1. providing a continuous p^+ guardband along the p-well perimeter of the cell array, and

2. a vertical, polysilicon field shield whose gate is tied either to V_{SS} or V for the required lateral isolation.

The n-channel field shield extends from the bottom p^+ quardband to the top guardband. This field shield lateral isolation is much more efficient in area than a diffused guardband; thus, the linear array layout technique provides complete device isolation with a minimum effect on cell dimensions. The diffused guardband causes less than a 10 percent penalty in cell height.

An ELA test chip was designed, fabricated, and evaluated to provide an experimental verification test vehicle for the cell family. The test chip contains a range of test devices to provide the necessary experimental process and cell design verification. In addition to basic physics-type devices (Van der Paw patterns, n^+, p^+ and poly resistors, etc.), there are:

1. typical n and p transistors on both gate and field oxides,

2. representative cells,

3. pair delay strings of inverters, two input NAND gates and two input AND gates,

4. Johnson counters with different flip-flop elements,

5. binary counter, and

6. arrays of devices (4050 ea.) of n and p devices with varying gate lengths.

From a designer's point of view, the test chip provides structures from which a complete matrix of modeling parameters can be obtained as well as circuits utilizing the basic cell gates which can be analyzed and tested to verify the validity and accuracy of model parameters. All cell and circuit responses were simulated using the SPICE circuit analysis program.

A representative sample of experimentally derived electrical parameters for the cell family are shown in Table II. Included are:

1. typical cell delay times for various combinational logic gates,

2. maximum clocking frequency of counter circuits, and

3. n- and p-drive current data tabulated for 5 and 10 volts at room temperature. The cell family can be generally characterized as having 5-10 ns gate delays at 10 volts and 10-20 ns gate delays at 5 volts. Counter operation in the 10 to 20 MHz range is possible at 10 volts.

TABLE II

TYPICAL ELA CELL FAMILY
ELECTRICAL CHARACTERISTICS

Frequency of Ring Counters
3-5 MHz @ 5 V
8->10 MHz @10 V

Gate Propagation Delays

	5 V	10 V
Inverter	7-11 ns	3-5 ns
2-input NOR	13-19 ns	6-8 ns
2-input NAND	14-20 ns	6-8 ns

Output Drives (mA) 2 V Off Rail

	n	p	n	p
Output Buffer	7	5	14	9
Standard Cells	1	0.8	1.7	1.0

The test chip has also been used to characterize the radiation tolerance of the ELA technology. Figure 4 shows typical gate delay degradation with radiation. In Figure 5, the drive currents obtained from the output buffers are shown as function of dose.

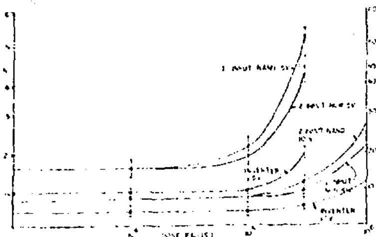

FIGURE-4
GATE DELAY VS DOSE

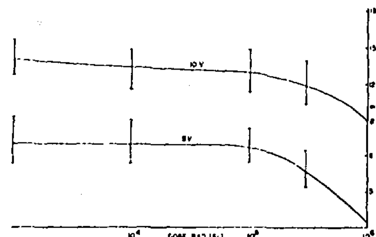

FIGURE-5a
N-CHANNEL OUTPUT DRIVE VS DOSE

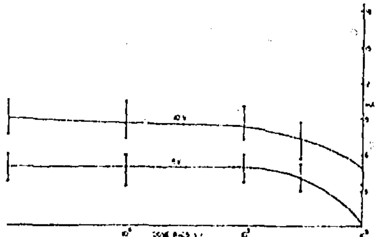

FIGURE-5b
P-CHANNEL OUTPUT DRIVE VS DOSE

Although work is continuing in optimizing the ELA Si-Gate process for electrical properties and in extending the radiation tolerance, the data presented demonstrate that the ELA cell family and technology is a high-performance bulk silicon technology capable of operating after high radiation doses.

To further demonstrate the capability of the ELA cell family, an 8-bit Arithmetic Logic Unit (ALU) was designed with the appropriate standard cells. This ALU was the test circuit chosen as a technology and design evaluation vehicle for the Air Force Fault Tolerant Computer Program. The chip contains 172 standard cells (12 types) ranging from inverters to 4 input gates and a specially designed multiplex gate. Chip statistics of interest can be summarized as follows:

1346 n and p devices,

6.69 K mils^2 actual cell area,

21.7 K mils^2 total chip area (175 X 124 mils), and

40 I/O pads.

Of particular interest in the evaluation of ALU performance is one critical delay path containing 14 gates which is used as a figure-of-merit for the technology-layout comparison. Finally, Figure 6 depicts the critical path delay as a function of ionization dose.

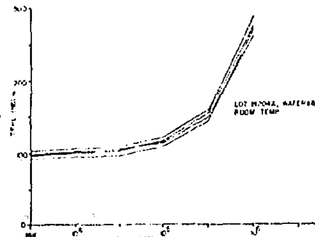

FIGURE-6
CRITICAL PATH DELAY VS DOSE, VDD=10V

CMOS-Hardened Technology Comparison

While CMOS has been established as a major technology to meet the power, performance, and radiation requirements for many space-borne applications, the choice whether to use bulk or SOS has not been resolved. Historically, the SOS technology appeared to offer the only guaranteed solution to the CMOS latch-up phenomenon. Also, because of its reduced junction and interconnect capacitance, it promised higher performance, although the performance aspect is somewhat open since the SOS technology has a significantly lower mobility than the bulk technology. The trade-offs for these assets were the *required material understanding of the* silicon-sapphire structure and the disadvantage of not utilizing a mainstream process. Since both technologies have been in development for several years, it is now appropriate to evaluate their relative merits.

In terms of latch-up, both the bulk and CMOS/SOS technologies have generic solutions to the latch-up problem. For the bulk case, however, either epitaxial substrates or lifetime control must be implemented. These techniques have demonstrated that they have no deleterious effects upon circuit costs, performance, yield or reliability. For transient hardness, however, the SOS circuit will have an upset level about 10x above its bulk counterpart. Present bulk CMOS circuits utilizing latch-up prevention, but without layout transient-hardening features, typically have transient upset levels of $5-10 \times 10^8$ rads/sec (20 ns pulse width).

A performance-packing density comparison between SOS and bulk radiation-hardened CMOS is available as a result of the standard cell ALU design for the fault-tolerant, space-borne computer program previously mentioned. Sandia and another commercial supplier designed the part with bulk CMOS technology; two other commercial suppliers used the CMOS/SOS technology. Table III summarizes the performance and density characteristics for the four designs.

TABLE III*

FT ALU CMOS COMPARISON

	Cells	Total Area of Cells	Chip Area
		($mils^2$)	(K mil^2)
Bulk CMOS			
Supplier A	227	14,365	36.1
Sandia	172	6,691	21.7
CMOS/SOS			
Supplier B	169	5,628	22.8
Supplier C	107	6,151	19.9

Performance-Critical Path

Bulk	
Supplier A	95-132 ns
Sandia	75-110 ns
CMOS/SOS	
Supplier B	140-200 ns
Supplier C	60-130 ns

*Data from M. Seavey, Raytheon

It should be pointed out that with the exception of supplier A, the parts were designed to operate at 10 volts. Supplier A did a 5-volt design which adversely compromised the packing density. The Sandia bulk CMOS design is quite competitive in both packing density and performance.

The SOS technology still continues to have material problems, such as the radiation-induced back-channel leakage. For example, a major advantage of the CMOS technology is its low static power dissipation. While hardened bulk CMOS circuits exhibit no I_{DD} increase as a function of total dose, CMOS/SOS circuits typically exhibit mA-level I_{DD} increases. In addition, the radiation-hardened SOS technology generally has step coverage problems due to its severe topology and lack of a high temperature, interlevel reflow sequence. This has a major impact upon yield and reliability. Although it is probably possible to solve these problems, the cost-effectiveness of doing so, in light of the well established hardened bulk CMOS technology, is open to serious question.

Future evolutionary trends in the bulk CMOS technology, which will build upon the mainstream commercial bulk technology, will further improve its packing density and performance. For example, the use of a hardened field oxide[14] will eliminate the need for guardbands, and self-aligning the n-well to source-drains will make the bulk CMOS topology virtually identical to the CMOS/SOS. Reduced polysilicon resistance will minimize the RC interconnect load, making the carrier mobility a more significant factor in circuit performance. Based on present data concerning yield, reliability, deliverability, performance, and future trends, the radiation-hardened bulk CMOS technology is clearly the best technology for systems with radiation environments.

Conclusions

The radiation-hardened bulk metal gate CMOS technology has a proven track record for megarad hardness, high reliability, availability, and no latch-up. This process has been extended to a hardened silicon gate process that was applied to a commercial microprocessor family, which led to the successful fabrication and delivery of high-reliability, radiation-hardened microprocessors, 256x4 RAMS and 1024x8 ROMS. A hardened cell family was developed that offers significantly improved performance and packing density over its metal gate predecessor and maintains low static power dissipation in a radiation environment. This topologically simple, high-performance, dual-ported cell family was used in a bulk-SOS design comparison and exhibited competitive performance and packing density while offering demonstrated yield and reliability advantages. Presently, a radiation-hardened, 1024x1 RAM and 1024x8 ROM are being designed in the hardened bulk CMOS technology. Future ongoing evolutionary developments will provide even greater performance for this versatile technology.

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