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Low-Pressure Chemical Vapor Deposition of Amorphous Silicon Photovoltaic Devices

Annual Technical Progress Report 1 May 1984 - 30 April 1985 A Subcontract Report

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University of Delaware
Newark, Delaware

Prepared under Subcontract No. XB-4-04061-1

SERI

Solar Energy Research Institute
A Division of Midwest Research Institute
1617 Cole Boulevard
Golden, Colorado 80401-3393

Operated for the
U.S. Department of Energy
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SUMMARY

Objectives:

In May 1984, a two year research program was initiated at the Institute of Energy Conversion with an interim goal of 6% efficiency small area a-Si:H cells by CVD of higher order silanes at growth rates exceeding 5 A/s by the end of the first year. The three integrated research tasks are: material preparation and analysis; chemical reactor analysis of CVD kinetics; and device fabrication and analysis. The technical approach is based on optimization of material properties and devices through feedback of device results, with material preparation being guided by quantitative analysis of reactor behavior.

Discussion:

Chemical vapor deposition of a-Si:H from higher order silanes has been used to produce hybrid p-i-n devices (p layer deposited by glow discharge deposition) with short circuit currents exceeding 9 mA/cm^2 and efficiencies of 4 percent, measured under ELH illumination at 87.5 mW/cm^2. Critical material properties -photoconductivity, activation energy, density of states and sub-band gap absorption- are susceptible to comparison with glow discharge material. Investigations of factors influencing film deposition rate has resulted in deposition of specular a-Si:H films at rates of 10 A/s. Experimental and theoretical investigations of reactor behavior has shown that long chain silanes are the principal film formation precursors. Glow discharge films have been shown to grow from short chain neutral radical precursors and are subject to electron and ion bombardment. These fundamental differences in growth mechanisms suggested that CVD had the potential to produce a-Si:H at high deposition rates having improved intrinsic stability. However, it was recognized that further improvements in intrinsic and doped film quality leading to higher efficiency were needed in order to assess any of the potential benefits of CVD for the long range objectives of a low cost solar electric technology based on a-Si:H thin films.

Intrinsic and doped a-Si:H films have been deposited by low pressure chemical vapor deposition from disilane. Conditions for depositing intrinsic material at growth rates up to 50 A/s have been established.

Reactor kinetics of CVD are governed by gas phase and surface reactions of higher order silanes. A chemical reaction engineering model which quantitatively describes reactor behavior was developed and verified.

The optical, electronic and transport properties of CVD a-Si:H intrinsic materials were characterized and correlated with device behavior. Diffusion length, measured by SPV was 0.1 micrometer. Mid-gap density of states, determined from measurements of sub-band gap optical absorption and from space charge limited current measurements were in the range 0.5-2 x 10^{17} $cm^{-3}eV^{-1}$. Space charge densities from measurements of capacitance and from SPV were of the order of 10^{17} cm^{-3}.

P-i-n cells having 3.6% efficiency were fabricated with intrinsic layers deposited by CVD at growth rates of 9 A/s. The maximum open circuit voltage achieved was 0.74 V. The open circuit voltage was limited by the flat band voltage, which did not depend on intrinsic layer or doped layer properties. Short circuit current of 11 mA/cm^2 (87.5 mW/cm^2, ELH) were obtained with boron compensated intrinsic layers. Boron compensation was found to enhance collection width and red response. The maximum fill factor obtained was 49%. Fill factor was found to be limited by high series resistance, which consisted of a light dependent component and a light independent contact resistance.

Conclusions:

The highest efficiency achieved was 4% with CVD intrinsic layers deposited at 1 A/s. An efficiency of 3.6% was attained with CVD intrinsic layers that were deposited at 9 A/s.

PARAMETER	TARGET	ACHIEVED
V(oc)	0.7-0.8	0.74V
J(sc)	11-13	10.9 mA/cm^2
FF	55-65	49%

Open circuit voltage (best value = 0.74 V) is not a limiting factor for achieving 6% efficiency. Short circuit current with boron compensated intrinsic layers (best value = 11 mA/cm^2) should be adequate. Moreover, optimization of the ITO with respect to anti-reflection properties would provide some improvements in current. Fill factor, however, is a major limitation for obtaining 6% efficiency. The fill factor in CVD cells is limited by high series resistance. Elimination of the light independent, or contact resistance, component of the series resistance would yield FF > 55%. Improved contact materials and optimization of the transition between doped and intrinsic layer deposition are reasonable approaches to reducing contact resistance. Thus, 6% efficiency may be attainable without major improvements in the quality of CVD intrinsic materials, if contact resistance losses are reduced. Higher efficiency will require major improvements in the properties of CVD intrinsic material.

CONTRIBUTORS

The following personnel at the Institute of Energy Conversion have contributed to the work described in this report:

Program Manager	Bill N. Baron
Principal Investigator	Richard E. Rocheleau
Device Analysis	Steven S. Hegedus
a-Si Deposition/Elec. Measurements	Wayne A. Buchanan Peter J. Lutz
Optical Measurements	James M. Cebulka
Laser Scan	Patrick G. Lasswell
Reactor Model Development	Ricardo J. Bogaert
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Cell Testing	Sally Buchanan Kristine K. Palmer
Report Preparation	Elaine A. Koronik

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SECTION 1.0

INTRODUCTION

Chemical vapor deposition of a-Si:H from higher order silanes had been used to produce hybrid p-i-n devices (p-layer deposited by glow discharge deposition) with short circuit currents exceeding 9 mA/cm^2 and efficiencies of 4 percent, measured under ELH illumination at 87.5 mW/cm^2. Critical material properties -photoconductivity, activation energy, density of states and sub-band gap absorption- were suitable for comparison with glow discharge material. Investigations of factors influencing film deposition rate had resulted in deposition of specular a-Si:H films at rates of 10 A/s. Experimental and theoretical investigations of reactor behavior had shown that long chain silanes are the principal film formation precursors. Glow discharge films have been shown to grow from short chain neutral radical precursors and are subject to electron and ion bombardment. These fundamental differences in growth mechanisms suggested that CVD had the potential to produce a-Si:H at high deposition rates having improved intrinsic stability. However, it was recognized that further improvements in intrinsic and doped film quality leading to higher efficiency were needed in order to assess any of the potential benefits of CVD for the long range objectives of a low cost solar electric technology based on a-Si:H thin films.

In May, 1984, a two year research program was initiated at the Institute of Energy Conversion with an interim goal of 6% efficiency small area a-Si:H cells by CVD of higher order silanes at growth rates exceeding 5 A/s by the end of the first year. Three integrated research tasks were contemplated: material preparation and analysis; chemical reactor analysis of CVD kinetics; and device fabrication and analysis. The technical approach was based on optimization of material properties and devices through feedback of device results, with material preparation being guided by quantitative analysis of reactor behavior.

During the first six months of the program, conditions for depositing CVD i-layers at rates exceeding 10 A/s were identified. Boron compensation of CVD i-layers was found to improve fill factor and short circuit current. Short circuit current of 11 mA/cm^2 was obtained. Series resistance was found to limit fill factor to 50%. These findings are described in detail in the Semi-Annual Report for the period May 1, 1984 through October 30, 1984 (1).

In this report we describe additional results obtained during the period November 1, 1984 through April 30, 1985 and summarize the status of CVD a-Si cell development during Phase I of the program.

SECTION 2.0

TASK 1 - MATERIAL PREPARATION AND ANALYSIS

The objective of this task was the improvement of intrinsic and doped a-Si:H material made by CVD from disilane for fabricating high efficiency cells. The work under this task during Phase 1 included: evaluation of disilane source material; identification of impurities; characterization of intrinsic layer properties by optical absorption, photoconductivity, activation energy, sub-band gap absorption, density of states and minority carrier diffusion length; identification of conditions for depositing device quality films at rates exceeding 5 A/s; deposition and characterization of intrinsic materials deposited at rates greater than 10 A/s; deposition and characterization of CVD p layers; deposition and characterization of wide band gap p-type window layers; and optimization of CVD n-layer conductivity.

2.1 REVIEW OF PREVIOUS WORK

The Semi-Annual Report(1) describes in detail results obtained in connection with studies of: disilane feed gas purity; p-layer; i-layer deposition temperature and growth rate; and boron doping of intrinsic layers. A brief summary follows.

Disilane from three commercial vendors -AIRCO, Matheson and Synathatron- were evaluated with respect to silane composition and trace impurities. AIRCO SED grade disilane, which is produced by Chronar Corporation, was found to have very low impurity levels. SIMS analysis of CVD i-layers formed at 400°C showed [O] = 2-5 x $10^{18}cm^{-3}$, [C] = 1-3 x $10^{18}cm^{-3}$ and no detectable Cl or N. AIRCO disilane was found to contain significant amounts of mono-, tri- and tetrasilane. The silane composition of AIRCO gas changed with use because of preferential vaporization of the higher order silanes.

SIMS analysis of intrinsic films made using Matheson disilane revealed high levels of Cl and another cylinder was found to contain >1% butane. Synthatron disilane was found to contain 5% of an organo-silicon impurity. The impurity was identified as ethylsilane. Analysis of the CVD reactor effluent showed that the organosilicon impurity underwent significant reaction during depositions at 440°C.

Boron doped a-Si:H p-layers were deposited by CVD at temperatures ranging from 200 to 250°C. Band gap and conductivity were found to depend strongly on diborane fraction in the feed gas, independent of substrate temperature. For subsequent device research deposition conditions yielding a band gap of 1.45 eV and dark conductivity of 2 x 10^{-5} $(ohm\text{-}cm)^{-1}$ were selected. Measurements of total transmission and reflection of CVD p-type a-Si:H, sputtered ITO and ITO/p layers were made to assess the optical

losses affecting device performance. Optical losses due to ITO/CVD p-layers amounted to nearly 40% at 450 nm and contributed to the poor blue response CVD p-i-n devices. In order to overcome these losses, development of glow discharge p-type a-SiC:H for use in hybrid devices was initiated. Band gaps as high as 2 eV were achieved.

The effects of intrinsic layer deposition temperature and growth rate on material properties and device performance were studied at 420 and 440°C, and growth rates from 2 to 40 A/s. Optical band gaps ranged from 1.53 to 1.57 eV. Photo- and dark conductivities were 1-3 x 10^{-6} (ELH, 87.5 ,mW/cm^2) and less than 10^{-10} S/cm, respectively and were not sensitive to deposition conditions. Characteristic energies of tail states were determined from space charge limited current (SCLC) measurements on n-i-n devices grown at 440°C. Values of 43, 56 and 64 meV corresponded to i-layers grown at 10, 29 and 37 A/s, respectively. Density of states obtained from SCLC measurements showed a peak at about 0.77 from the conduction band. The maximum in the density of states (DOS) was 7-8 x 10^{17} for i-layers grown at 37 A/s and 2 x 10^{17} $cm^{-3}eV^{-1}$ at 10 A/s. Neglecting the peaks, DOS of CVD i-layers was 2-4 times greater than device quality glow discharge material.

The effect of diborane additions to the feed gas during intrinsic layer deposition were studies. No significant effect on photoconductivity, activation energy and band gap was observed for diborane fractions up to 13 vppm.

2.2 RECENT RESULTS

2.2.1 DIFFUSION LENGTH

Diffusion length and space charge density of undoped and boron doped CVD i-layers were measured using the constant surface voltage technique (SPV). In Figure 2-1 are a representative plot of SPV data and a tabular listing of results from samples made over a range of deposition conditions. Diffusion lengths were about 0.1 micrometer and dark space charge densities were greater than $10^{16}cm^{-3}$. These results are in good agreement with previously reported values obtained from device measurements.

2.2.2 DENSITY OF STATES AND SPACE CHARGE DENSITY

Mid-gap density of states and space charge density were determined in order to characterize intrinsic CVD a-Si:H material. Table 2-2 summarizes mid-gap DOS and space charge density in CVD material obtained from a variety of experimental techniques. Data from both space charge limited current measurements and the optical absorption shoulder at 1.3 eV yielded mid-gap DOS values, g(E) = 0.5-2 x 10^{17} ($cm^{-3}eV^{-1}$). Space charge density

from photo-capacitance at room temperature, dark capacitance at 100°C and SPV was in the range 0.2-3 x 10^{17} cm^{-3}.

2.2.3 SPUTTERED SiC

Sputtering was briefly explored as an alternative technique for depositing wide band gap p-layers. SiC films were RF sputter deposited on unheated 7059 glass substrates using argon as the sputtering gas. Deposition rates were about 10 A/s using 2 W/cm RF power and a boron doped SiC target. X-ray diffraction of a 2000 A sample showed no evidence of crystallinity. A single broad peak, characteristic of amorphous material, was obtained. SEM revealed no structure up to a magnification of 20,000 X. Optical data for a 2000 A thick film is shown in Figure 2-2. The extrapolated band gap was 2.5eV. The room temperature dark conductivity was 1-2 x 10^{-4} S/cm. These high conductivity-band gap values suggest that sputtered SiC may be of interest for amorphous silicon devices in general.

2.2.4 HIGH CONDUCTIVITY CVD n-LAYERS

Previously reported analysis of efficiency limiting mechanisms indicated high resistance at the n+/Mo contact in CVD p-i-n cells. In order to achieve higher doping efficiency, the effect of substrate temperature during n-layer deposition was studied. Figure 2-3 shows the deposition temperature effect on dark conductivity at room temperature for 5000 A thick CVD n-layers deposited with a phosphine/disilane ratio of 10% at the inlet. The observed decrease in conductivity with increasing deposition temperature between 400 and 450°C and subsequent increase above 475°C was attributed to the different activation energies for phosphine cracking and film deposition. Between 400 and 450°C the rate of film deposition increases more rapidly with temperature than the rate of phosphine cracking, so that the relative rate of dopant incorporation decreased. Above 475°C, the cracking rate becomes appreciable and gas phase depletion effects further reduce the relative rate of film growth, so that doping efficiency increased markedly. Room temperature dark conductivity of 0.1 S/cm was obtained by depositing CVD n-layers at temperatures >550° C.

CVD Sample	i-Layer Conditions Temp. (°C)	Boron (vppm)	Gr. Rate (Å/S)	L_D (μm)
545.72	400	12	2.0	.12
546.72	440	12	4.1	.11
551.61	440	0	11.6	.10
553.51	440	0	27.0	.07

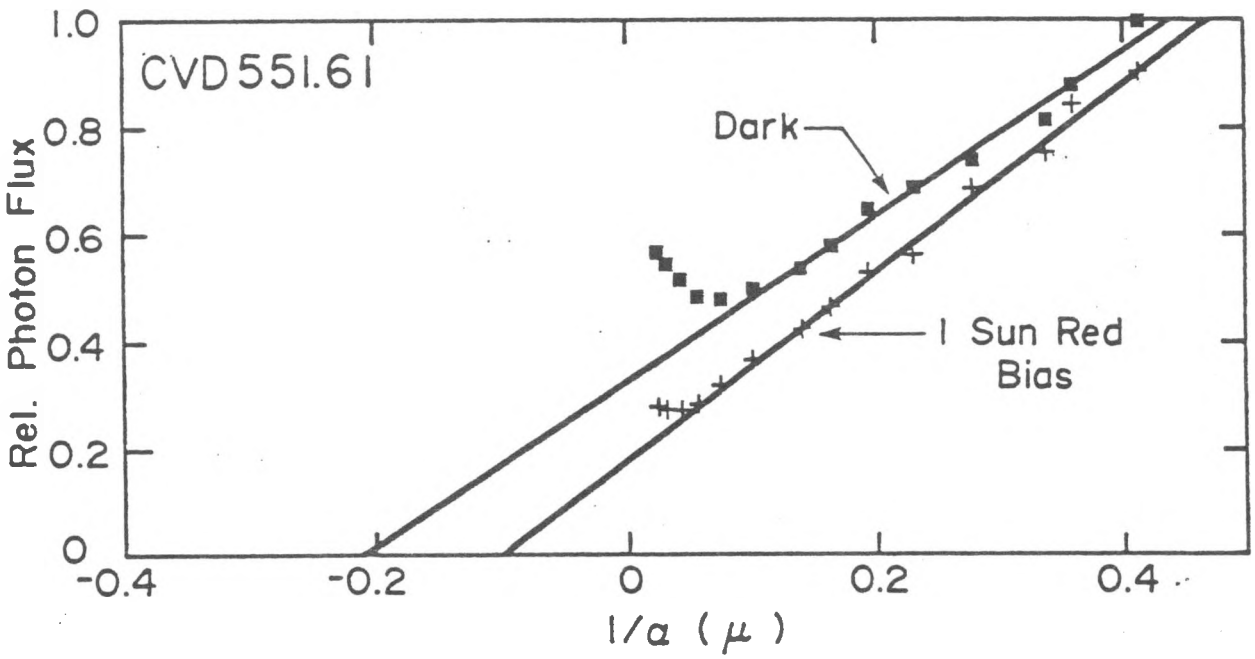

Figure 2-1. SPV Diffusion Length

Table 2-1. Mid-Gap DOS and Space Charge Density

MID-GAP DOS	
SCLC	$g(E) \sim 0.5\text{-}2.0 \times 10^{17} cm^{-3} eV^{-1}$
PDS	$g(E) \sim 0.7\text{-}2.0 \times 10^{17} cm^{-3} eV^{-1}$
SPACE CHARGE DENSITY	
Photo-capacitance @ 25°C	$N \sim 0.2\text{-}1.0 \times 10^{17} cm^{-3}$
Dark capacitance @ 100°C	$N \sim 0.2\text{-}1.0 \times 10^{17} cm^{-3}$
SPV (dark)	$N \sim 0.3\text{-}3.0 \times 10^{17} cm^{-3}$

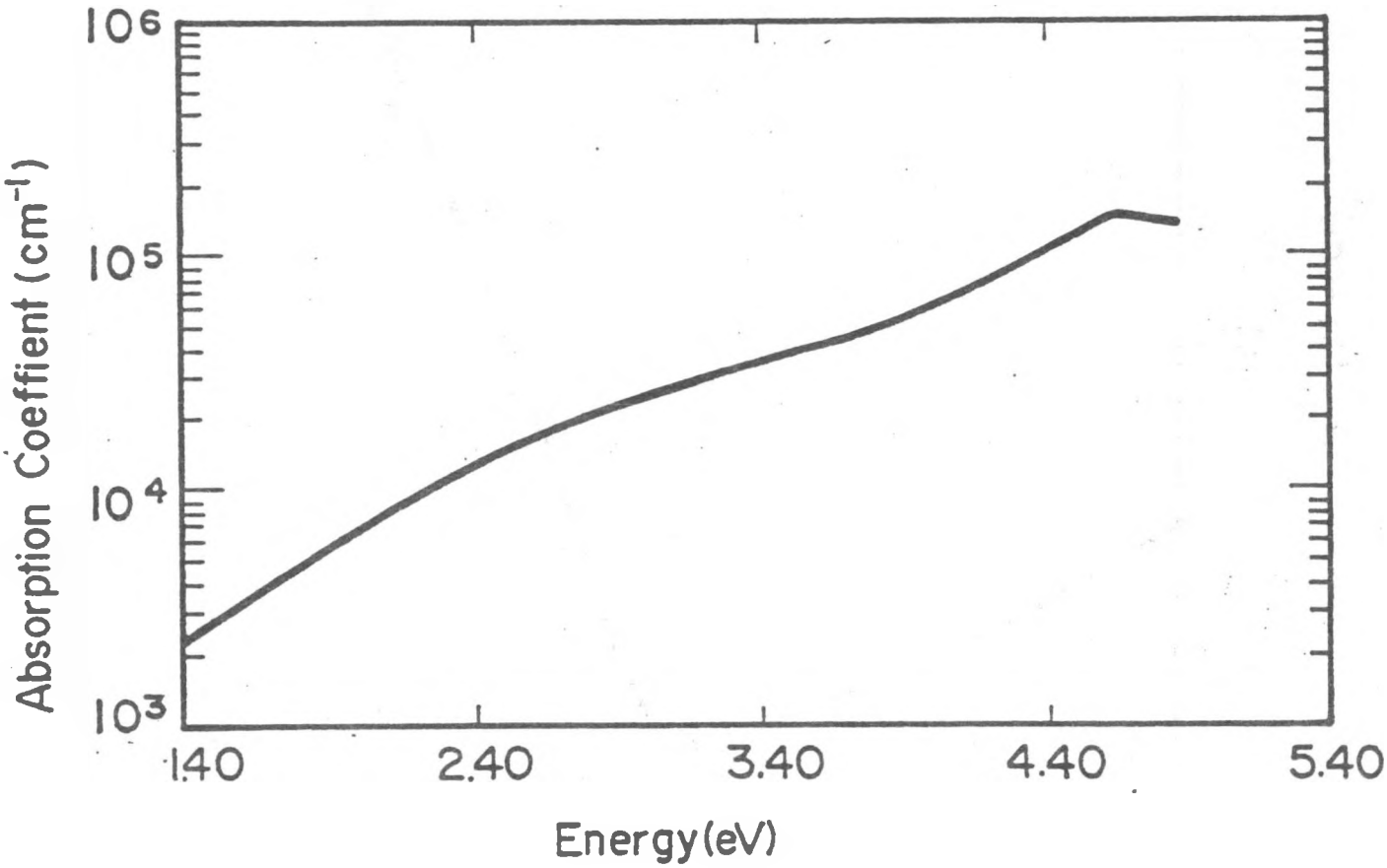

Figure 2-2. Optical Absorption of Sputtered SiC

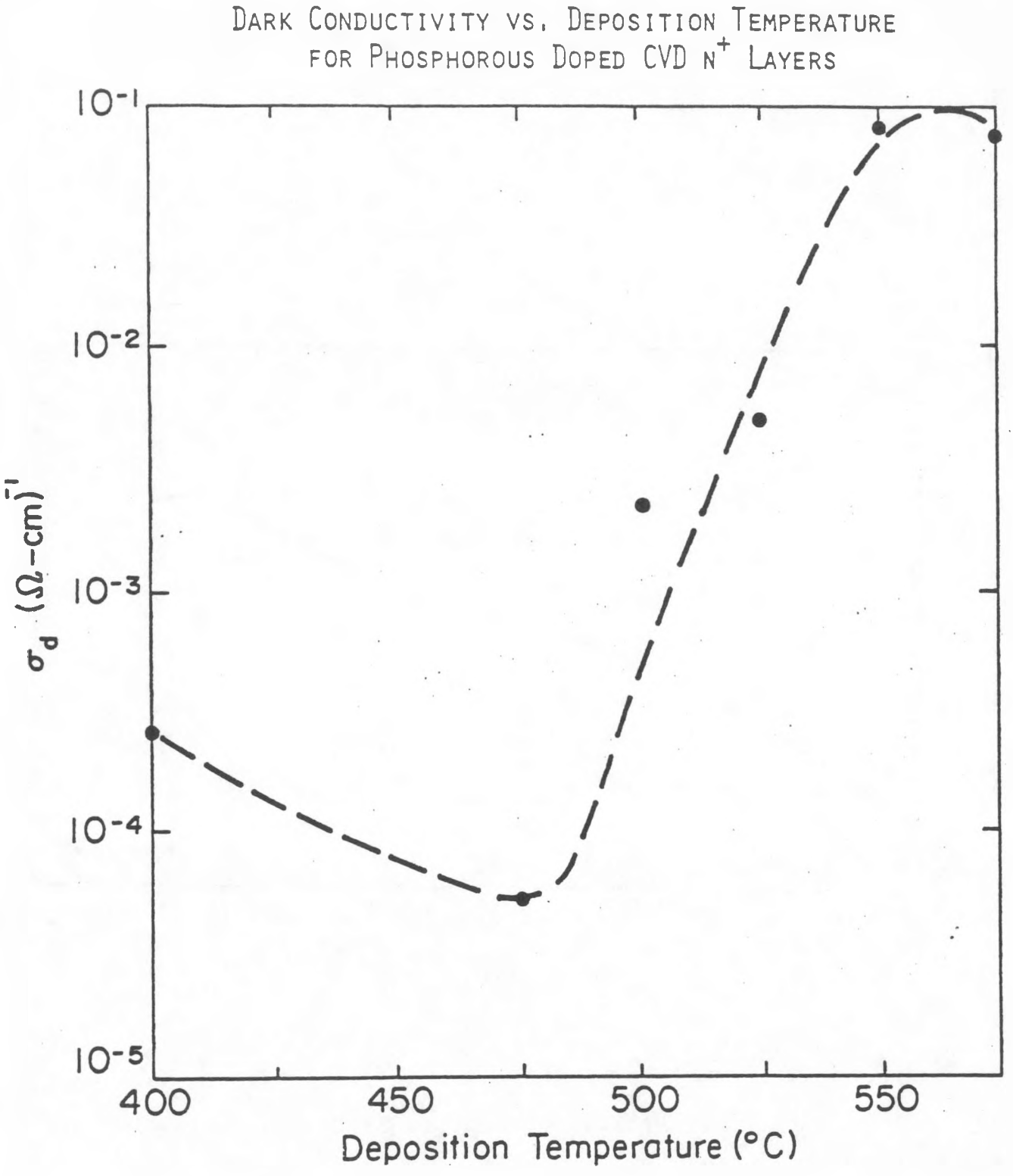

Figure 2-3. N Layer Conductivity v. Deposition Temperature

SECTION 3.0

TASK 2 - REACTOR ANALYSIS

A chemical reaction engineering model of the tubular flow reactor used in Task 1 was developed to quantitatively describe film growth and gas phase composition with respect to pressure, temperature, flow rate and axial position. On-line gas chromatography was used to measure inlet and outlet gas composition.

3.1 Review of Previous Work

The Semi-Annual Report(1) contains a detailed description of the chemical reaction engineering analysis. The kinetics of higher order silanes CVD were modelled for a tubular reactor with static substrates. A gas phase reaction network based on published silylene insertion and decomposition pathways was adopted. Mass balances for hydrogen and all saturated silanes through octasilane were derived. A quantitative description of the gas phase reactions was obtained by uncoupling the gas and solid phase mass balances and numerically optimizing the chemical rate constants for the gas phase reactions. The uncoupling was achieved by using experimentally determined growth rate data and testing several hypotheses for the stoichiometry of the film formation reaction. The numerical optimization was carried out using a multifactor objective function and experimentally measured gas phase composition data. The best over-all fit was based on film growth via decomposition of pentasilane and the generation of silane and hydrogen.

3.2 Recent Results

Alternate film growth mechanisms involving surface reaction of higher silanes and generation of lower silanes were studied, Table 3-1. The best fit to data from runs at 400 and 420°C was obtained when film growth was assumed to occur via surface reaction of trisilane, tetrasilane and pentasilane to form film and silane and hydrogen according to Mechanism X. The predicted and observed dependence of gas phase composition on holding time at 400°C were in good agreement, as shown in Figures 3-1 and 3-2. Similar good agreement was obtained at 420°C. However, agreement between the model and experiment was not acceptable at 430°C for long holding times.

Table 3-1. Film Formation Reaction Mechanisms

MECHANISM X

Si_3H_8 ------> Si_s + 2 SiH_4

Si_4H_{10} -----> 2 Si_s + 2 SiH_4 + H_2

Si_5H_{12} -----> 3 Si_s + 2 SiH_4 + H_2

MECHANISM Y

Si_3H_8 ------> Si_s + Si_2H_6 + H_2

Si_4H_{10} -----> Si_s + Si_3H_8 + H_2

Si_5H_{12} -----> Si_s + Si_4H_{10} + H_2

MECHANISM Z

Si_3H_8 ------> 2Si_s + SiH_4 + 2H_2

Si_4H_{10} -----> 2Si_s + Si_2H_6 + 2H_2

Si_5H_{12} -----> 2Si_s + Si_3H_8 + 2H_2

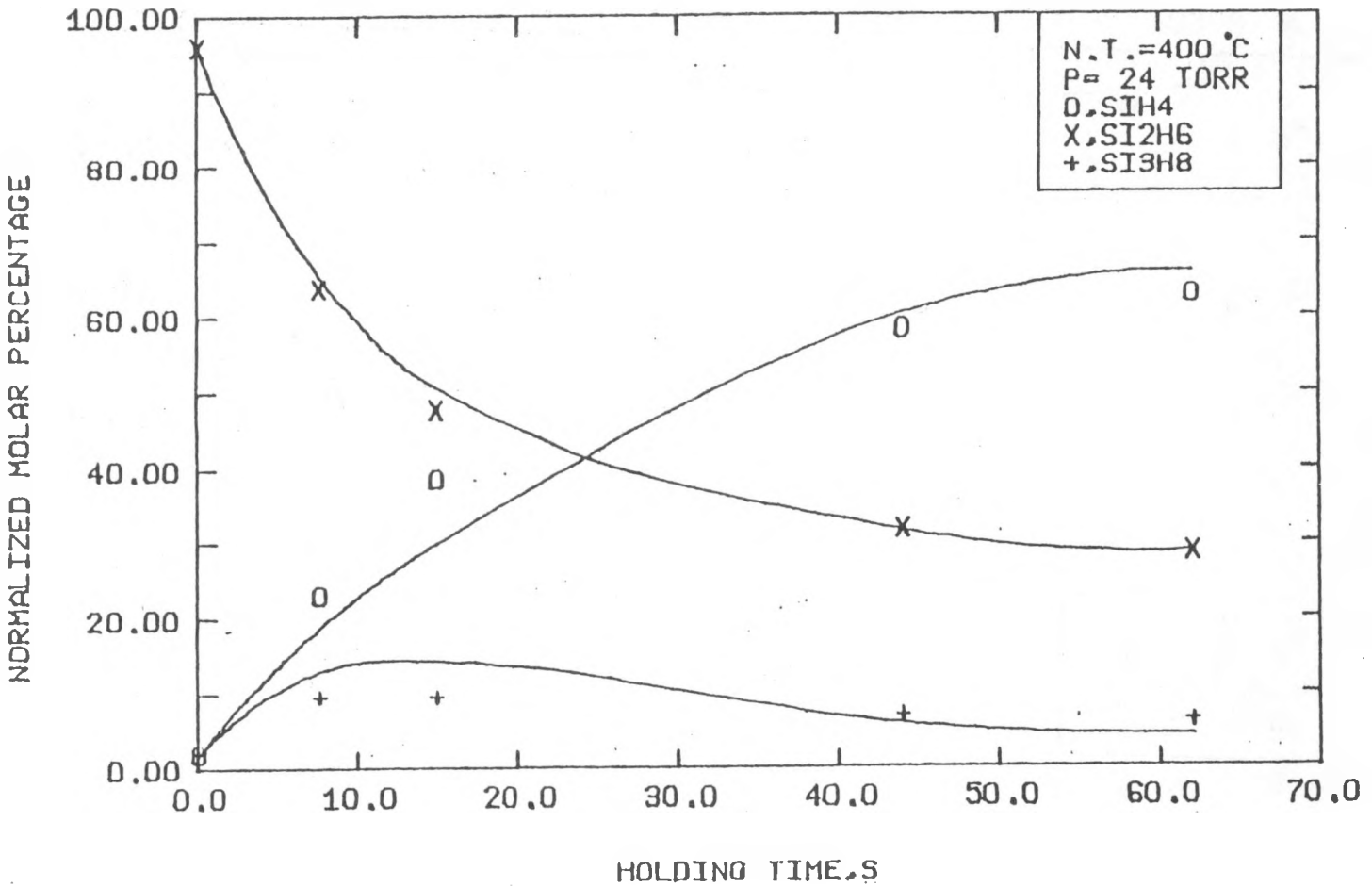

Figure 3-1. Major Silanes Mole Percent Versus Holding Time

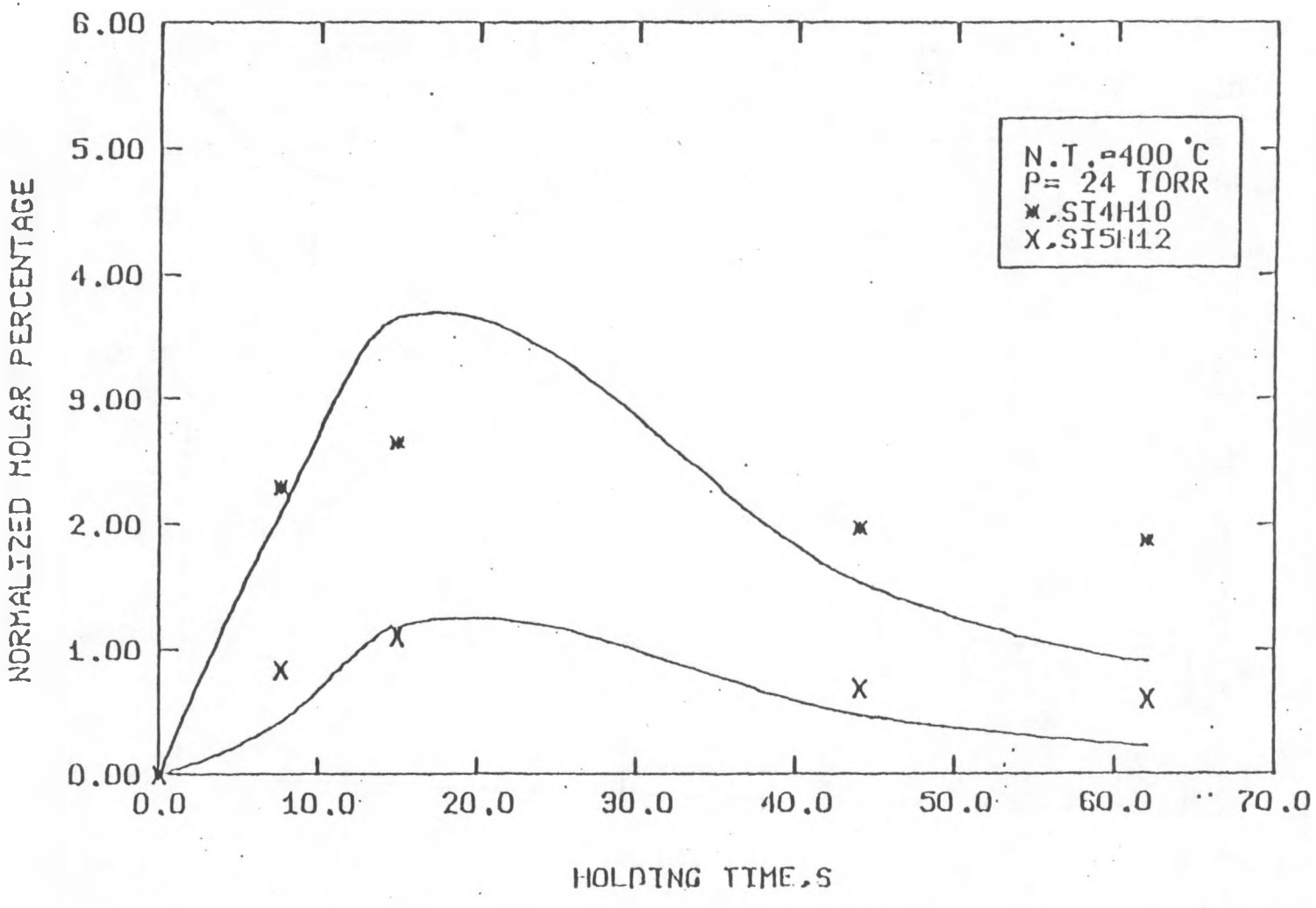

Figure 3-2. Minor Silanes Mole Percent Versus Holding Time

SECTION 4.0

TASK 3 - DEVICE FABRICATION AND ANALYSIS

The primary objective of device studies was achievement of 6% efficiency p-i-n cells fabricated using CVD from disilane. Quantitative analysis of efficiency limiting mechanisms and measurement of fundamental device parameters were carried out. Device analysis was used to study fabrication process variables and optimize material properties.

4.1 Review of Previous Work

The Semi-Annual Report(1) describes the data and conclusions reached in connection with device studies during the first half of Phase I. A brief summary follows.

Cell parameters of p-i-n cells were correlated with deposition temperature and growth rate of uncompensated i-layers. Fill factor (max. value = 49%) and short circuit current (max. value = 9 mA/cm^2) were found to depend on deposition conditions, while open circuit voltage (0.65-0.72V) did not. Deposition conditions of 440°C and growth rates less than 5 A/s were selected for future device development efforts.

The effect of diborane additions to the feed gas during i-layer deposition were studied. While no significant effect on i-layer photoconductivity, activation energy and band gap was observed for diborane fractions to 13 ppm, diborane addition improved the performance of CVD p-i-n cells. Short circuit currents of 11 ma/cm^2 at 87.5 mW/cm^2 ELH were obtained with a boron compensated i-layer thickness of 5500 A. Enhanced red response (2X at 700 nm) was observed with boron doped i-layers. Boron compensation also had a significant effect on series resistance and fill factor. Series resistance values of 20-30 $ohm-cm^2$ were obtained with boron doped i-layers up to 5500 A, compared to 40-50 $ohm-cm^2$ without boron doping. Furthermore, series resistance was nearly independent of i-layer thickness for boron compensated material up to 4500 A. Measurements of current-voltage behavior as a function of light intensity yielded diode factor, A = 1.4.

Analyses of efficiency limiting mechanisms showed that fill factor was limited by a series resistance of about 20 $ohm-cm^2$ which could not be readily attributed to bulk i-layer resistivity. Experimental evidence and calculations indicated high resistance at the n+/Mo back contact possibly due to insufficient conductivity in the CVD n-layer. Priority experiments aimed at increasing the doping levels in CVD n-layers were planned.

The spectral response of CVD p-i-n cells was best described by a double junction model(2). A 0.3μm field-free region separating the front and back junctions was found for uncompensated i-layers

having hole $\mu\tau = 2\text{-}4 \times 10^{-9}$ cm^2/V and hole diffusion length less than 0.1 μm. Capacitance vs. voltage data yielded space charge densities, $N = 4\text{-}6 \times 10^{16}$ cm^{-3}.

4.2 CVD p-i-n Solar Cell Development

The status of CVD p-i-n cells with respect to the Phase I goal of 6% efficiency is summarized in Table 4-1. The basic device configuration was ITO/p-i-n/metal/glass. Table 4-2 lists the device fabrication variables that were studied in connection with improving the efficiency of CVD cells. A systematic analysis of the open circuit voltage, fill factor and short circuit current follows.

Table 4-1. CVD Solar Cell Device Parameters

CVD SUMMARY

GOAL: 6% Efficiency with LPCVD i-layer at 5 Å/S

STATUS:

Parameter	Typical Range	Best to Date
V_{OC}(V)	.62 - .72	.74
J_{SC} (mA/cm^2 @ 87.5 mW/cm^2)	8 - 10.5	10.9
FF	40 - 45	49
Growth Rate (Å/S)	2 - 10	50
η	2.5 - 3.5	4% at 1 Å/S 3.6% at 9 Å/S

Table 4-2. Device Fabrication Parameter Space

CELL FABRICATION
ITO/pin/metal/glass

Variable	Range Studied	Values Yielding 3.5% Cells
Metal contact	Mo-sputter and e-beam NiCr Cr Ti	Sputter Mo
Disilane	MgSi (Chronar) SED (AIRCO) Matheson Synthatron	All
n^+	CVD 400 - 575°C 10^{-4} to 10^{-1} $(\Omega\text{-cm})^{-1}$	CVD 400 - 420°C
CVD i	1000 - 7000 A 380 - 460°C 0.1 - 50 A/S Boron compensated	3200 - 5700 A 400 - 440°C 0.5 - 9.0 A/S 0 - 12 ppm
p^+	CVD Si:H GD Si:H GD SiC:H Sputter SiC:H	CVD Si:H GD Si:H (GD SiC:H 3.2%)
ITO	Sputter E-beam	both

4.2.1 Open Circuit Voltage

The highest open circuit voltage obtained with a CVD p-i-n cell was 0.74 V. The typical range for devices fabricated during Phase I was 0.62 to 0.72 V.

Open circuit voltage was virtually independent of i-layer thickness as shown in Figure 4-1 for intrinsic layers with and without boron compensation. Diode quality factors from measurements of log J vs. V at different light intensities were A = 1.4, with and without boron compensation. The thickness independence of V_{oc} and A factor data indicated that open circuit voltage of CVD cells may not be limited by i-layer bulk recombination, but by lower built-in voltage.

Flat band potential, V(fb), was determined from measurements of monochromatic light generated current vs. bias voltage using 1-5 mW/cm^2, 670 nm excitation chopped at 70 Hz and white light bias. Flat band voltages were typically in the range 0.70 to 0.75 V. For comparison, V(fb) in the range 0.8 to 0.9 V are typical of glow discharge cells. As seen in Figure 4-2, V(fb) did not depend on n-layer doping, p-layer band gap or boron compensation. However, V(fb) was found to depend on both excitation and bias light intensities. These data suggest that open circuit voltage in current CVD cells is most likely limited by the intrinsic layer. As noted in Section 2, CVD material was found to have higher space charge density and lower band gap than device quality glow discharge material.

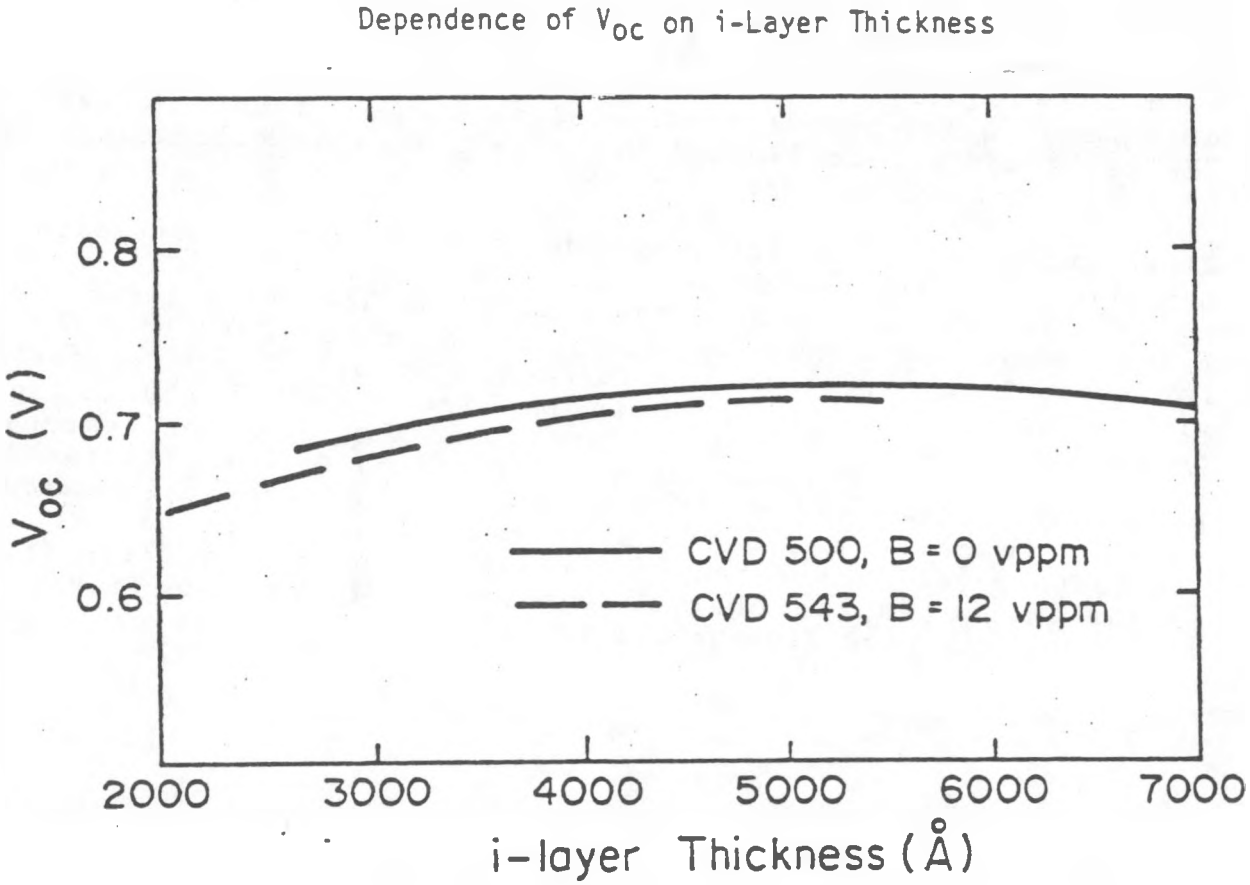

Figure 4-1. Dependence of Open Circuit Voltage on i-layer thickness

Bias Dependence of Chopped Photocurrent

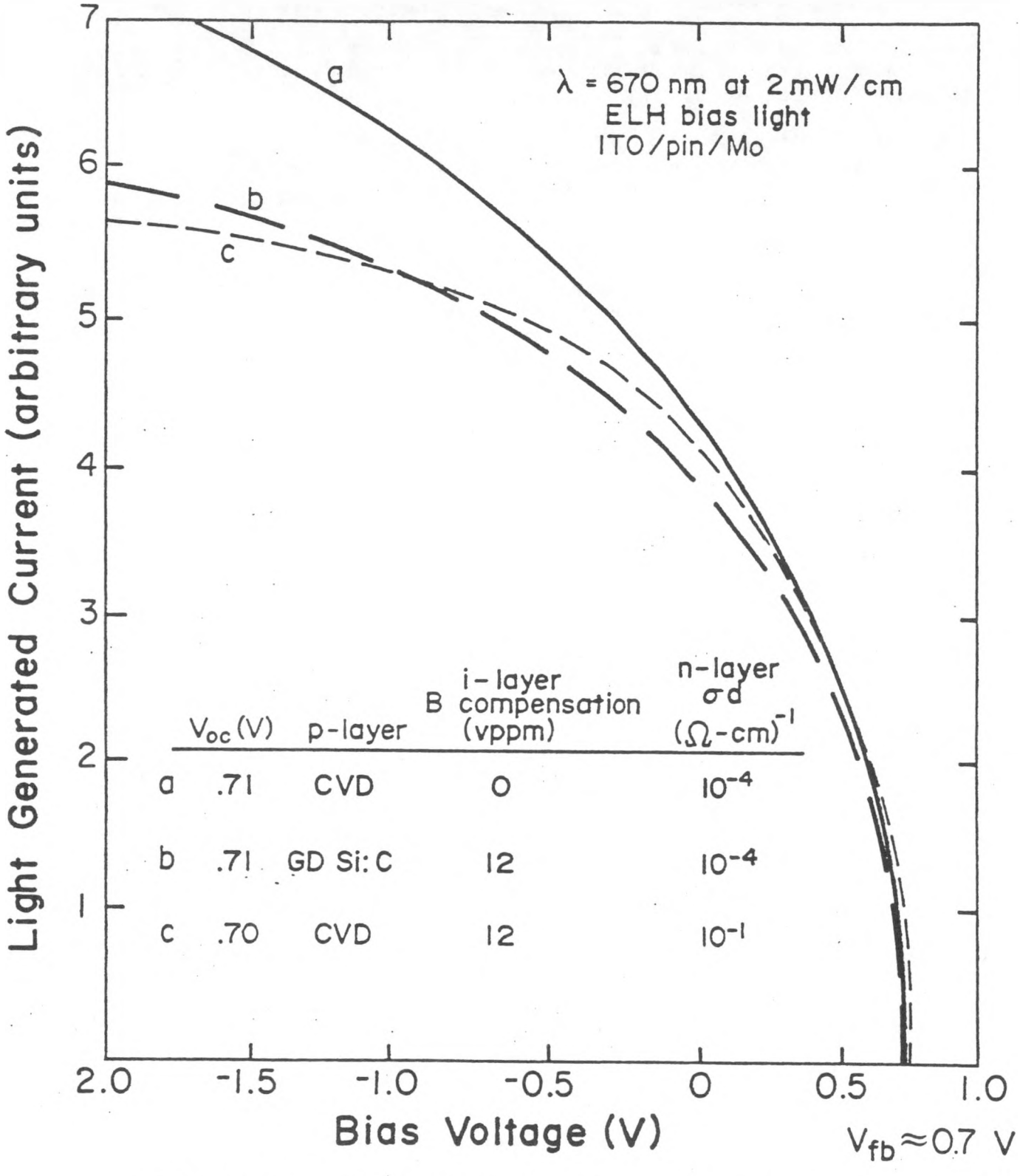

Figure 4-2. Light Generated Current v. Bias Voltage

4.2.2 Fill Factor

The highest fill factor obtained with CVD p-i-n cells with i-layers thicker than 3000A was 0.49. The typical range for devices fabricated during Phase I was 0.40 to 0.45.

The major limitation to fill factor in CVD cells was series resistance. Series resistance was determined from the measurement of dV/dI at I=0 during cell testing. Figure 4-3 shows the correlation between fill factor and series resistance for 190 cells, with and without boron compensated intrinsic layers, that were fabricated from six depositions. Figure 4-4 shows the dependence of series resistance on i-layer thickness for uncompensated and boron compensated material, respectively. Series resistance of uncompensated material increased with i-layer thickness from 20-30 ohm-cm^2 at 3000 A to 60-70 ohm-cm^2 above 6000 A. With boron compensation, series resistance was 20-30 ohm-cm^2 and did not vary with i-layer thickness between 2000 and 5500 A. Above 5500 A, the series resistance of boron compensated i-layer increased with thickness.

In order to separate the components of series resistance, dI/dV(I=0) was measured at different intensities. The light dependent and light independent components were determined(3) from the slope and intercept of plots of series resistance versus reciprocal short circuit current, Figure 4-6.

The light independent component of series resistance ranged from 4 to 12 ohm-cm^2. Experiments, which were described in the Semi-Annual Report(1), had suggested high resistance or blocking behavior at the n-layer/Mo interface were the most likely cause of the light independent resistance. The effect of n-layer conductivity on series resistance was studied by fabricating cells having n-layers prepared at various deposition temperatures (cf. Section 2.2.4) which corresponded to n-layer conductivities ranging from 0.0001 to 0.1 S/cm. No reduction in the dark component of series resistance was obtained. While the transition between the n-layer and i-layer deposition proved to be a critical step, especially when the n-layers were deposited at higher temperatures to increase conductivity, no improvements in fill factor were realized.

Alternate contact metals, NiCr and Ti, as well as sputtered versus e-beam Mo were tested. No improvements in fill factor were obtained and, in general, these alternatives yielded poor cells. The J-V behavior of p-i-n devices fabricated on NiCr compared to Mo is illustrated in Figure 4-6.

The behavior of the light dependent component of series resistance with i-layer thickness is shown in Figure 4-7 for uncompensated and boron compensated i-layers. In uncompensated material, the light dependent component varied linearly with i-layer thickness, from 10 ohm-cm^2 at 2000 A to 30 ohm-cm^2 at

7000 A, with a slope of 4×10^5 ohm-cm. This corresponds to a photoconductivity of 2.5×10^{-6} S/cm, which is in good agreement with values obtained from gap-cell measurements on CVD intrinsic material. However, with boron compensated i-layers, the light dependent component was a constant 10 ohm-cm^2 for thickness up to 5000 A; and between 5000 and 7000 A, the light dependent component increased to about 30 ohm-cm^2. No simple explanation for the complex behavior of boron compensated material was found.

Another limiting element related to the fill factor is the voltage dependence of the photocurrent. In general, the ratio of short circuit current to light generated current in CVD cells was 0.8 to 0.9. A ratio of 0.95 will be needed in order to achieve fill factor >0.65 needed for high efficiency cells.

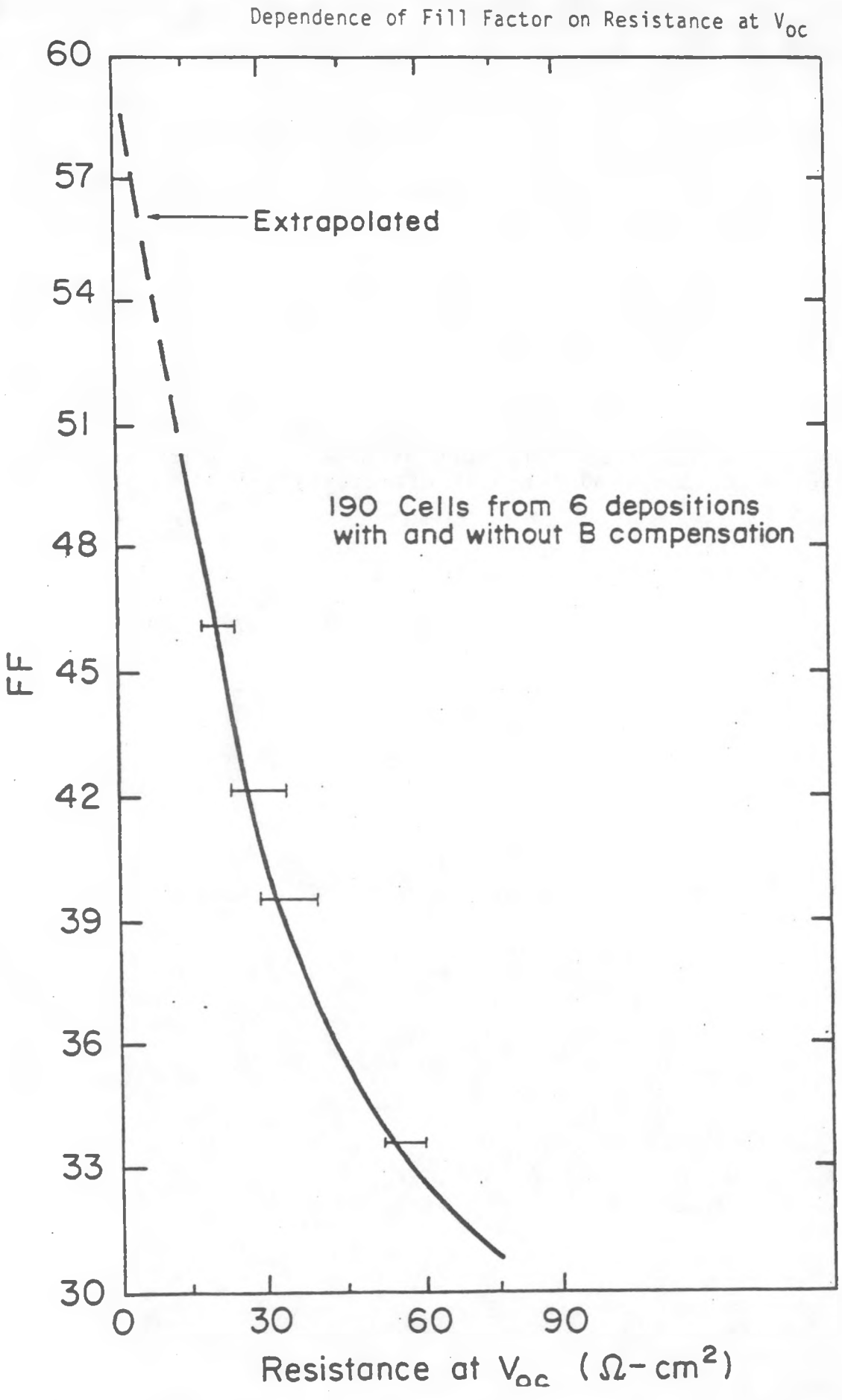

Figure 4-3. Fill Factor Versus Series Resistance

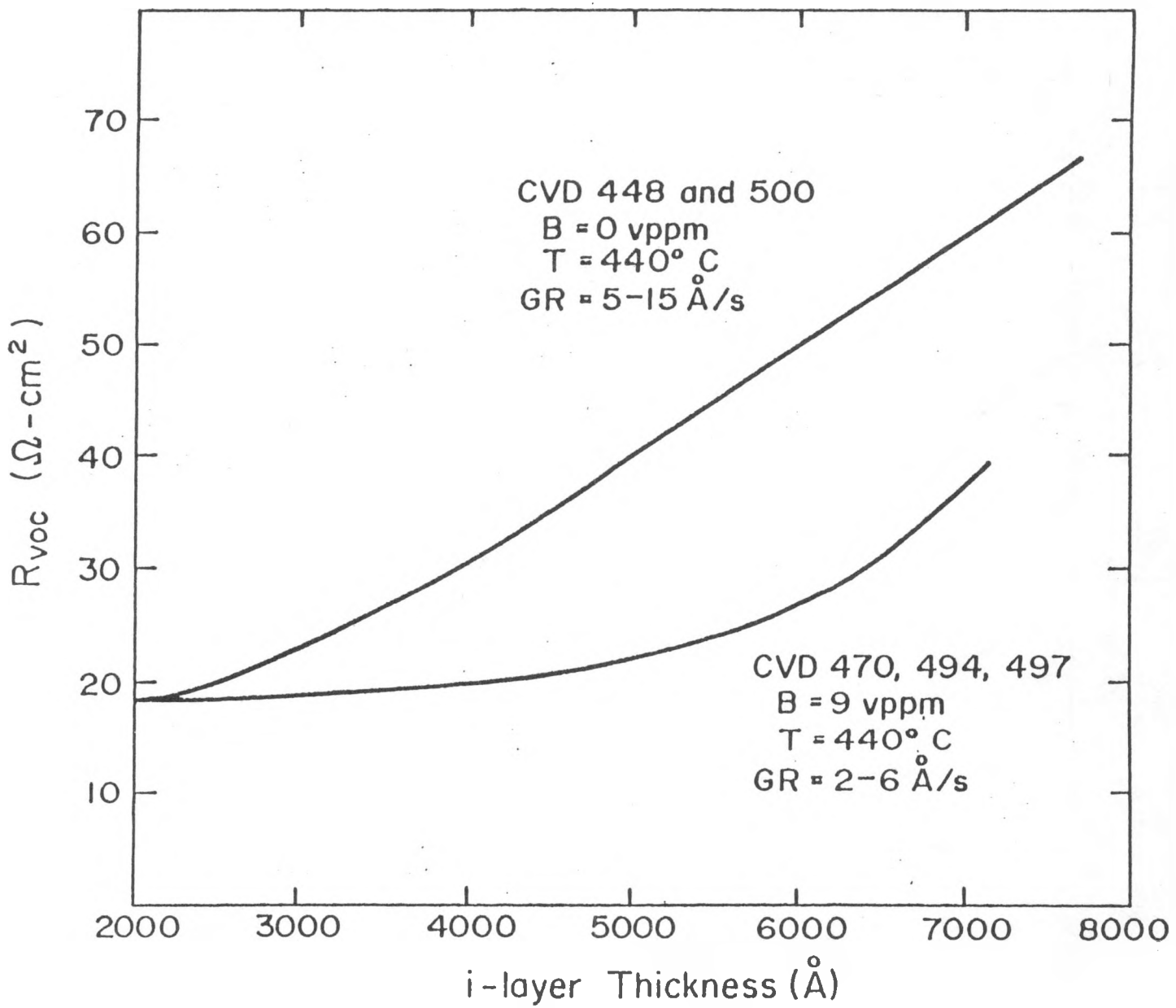

Figure 4-4. Series Resistance Versus Intrinsic Layer Thickness

Analysis of Series Resistance

		W_i (Å)	B_2H_6/Si_2H_6	R_C (Ω-cm^2)	R_L (Ω-cm^2)
a)	CVD500.61.4	7000	0	12	31
b)	CVD500.42.2	3100	0	8	11
c)	CVD543.71.2	5000	12 ppm	6	11
d)	CVD543.41.4	2000	12 ppm	4	10

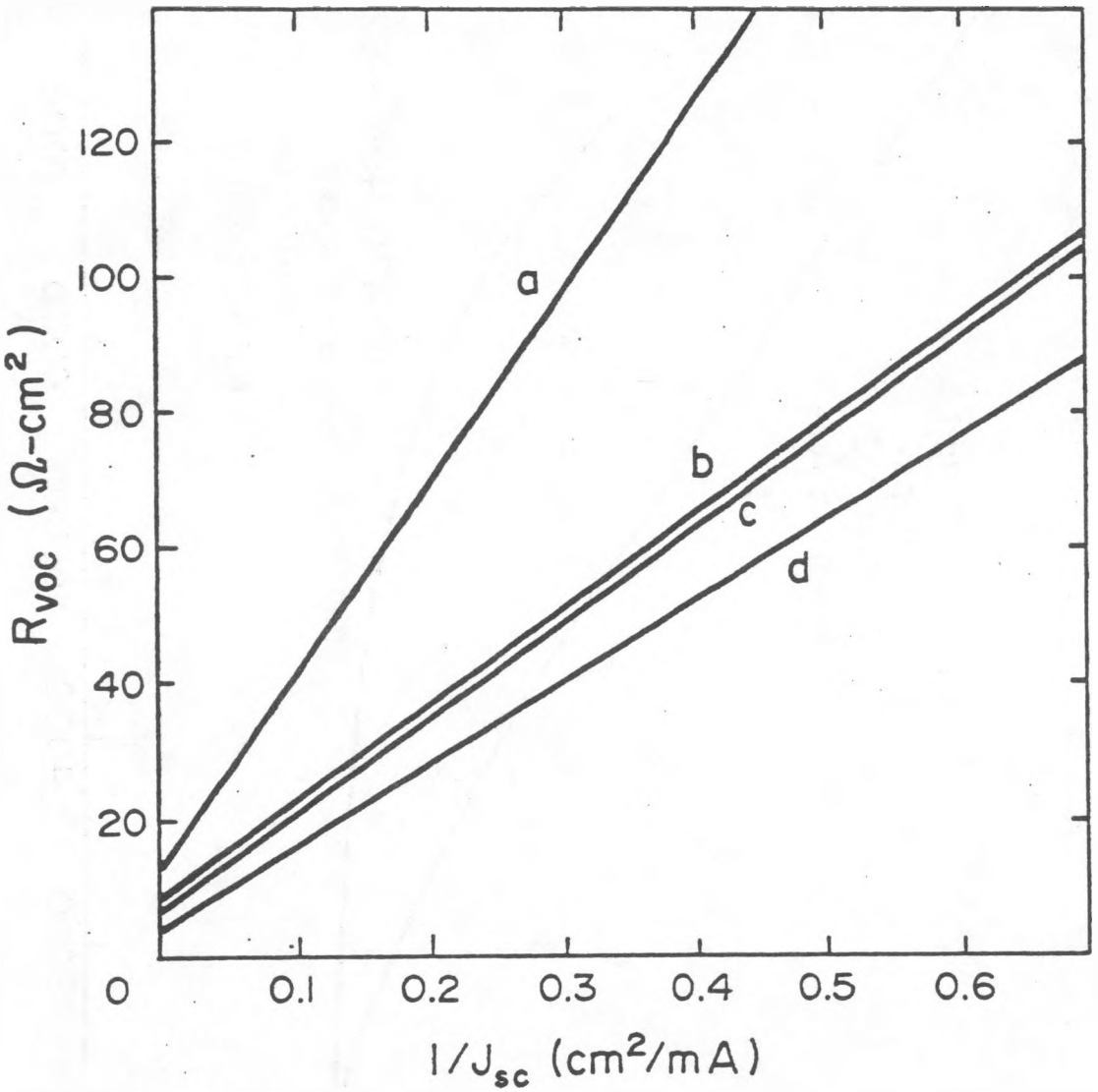

Figure 4-5. Analysis of Series Resistance

J-V Characteristics for CVD564 with Mo and NiCr Substrates

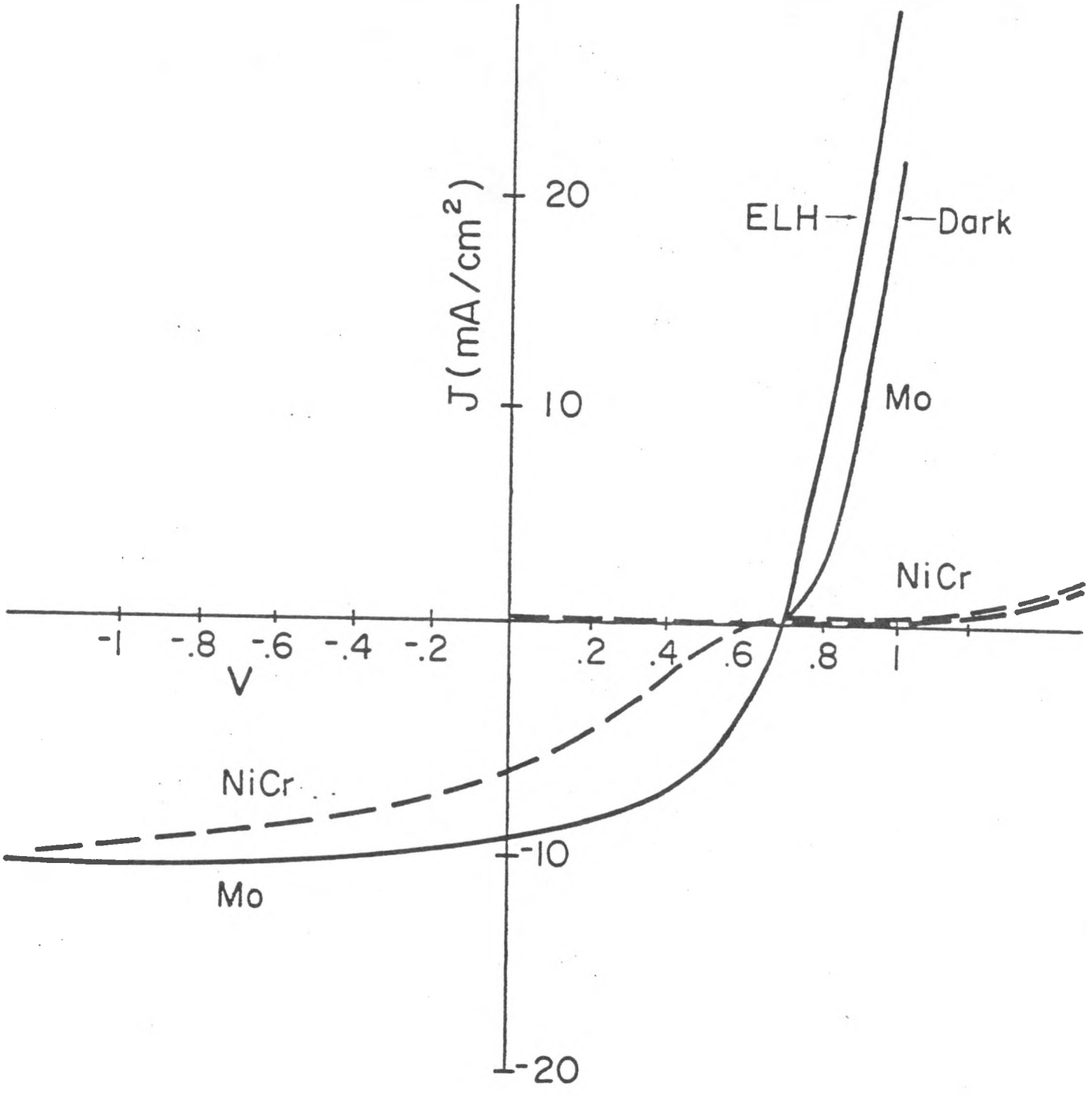

Figure 4-6. Behavior of Mo and NiCr Back Contact Metals

Effect of Boron Compensation and i-Layer Thickness on Light-Dependent Resistance from R_{VOC}-1/J_{SC} Analysis

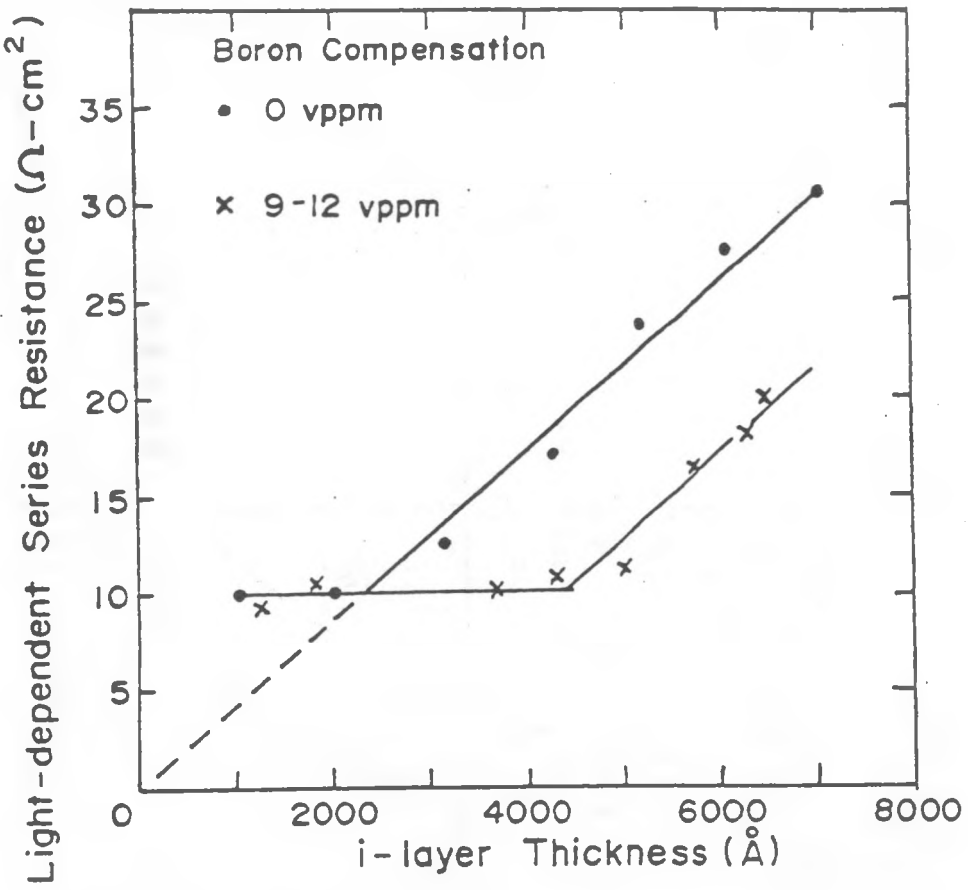

Figure 4-7. Light Dependent Series Resistance Component Versus Intrinsic Layer Thickness

4.2.3 Short Circuit Current

The highest short circuit current obtained with CVD p-i-n cells was 10.9 mA/cm^2 at 87.5 mW/cm^2 ELH. The typical range for devices fabricated during Phase I was 8.0 to 10.5 mA/cm^2. The short circuit current of CVD cells was examined with respect to generation and collection.

The influence of the p-type window layer on current generation was studied by fabricating p-i-n cells with p-layer band gaps ranging from 1.45 to 1.9 eV. Cells with high band gap p-layers were hybrid, i.e., p-type a-Si:H or a-SiC:H were formed by glow discharge deposition from silane or silane plus methane, respectively. Short circuit current did not change with p-layer band gap. This result is consistent with the analysis of Schade, et al.(4). Following Schade et al., calculations of losses in light generated current due to optical properties of the ITO and p-layers were performed. Figure 4-8 summarizes the calculation of light generated current (under 87.5 mW/cm^2, ELH) as a function of p-layer band gap between 1.4 and 2.0 eV would, at best, increase short circuit current by 1 mA/cm^2. These results are also consistent with measurements of ITO/p-layer transmission and reflection described in the Semi-Annual Report(1).

Collection of light generated carriers was the most important feature characterizing short circuit current in CVD cells. Figure 4-9 shows the spectral response at short circuit under ELH white light bias of p-i-n cells with and without boron compensated intrinsic layers. The short circuit currents, measured at 87.5 mW/cm^2 ELH, and intrinsic layer thicknesses are also indicated in the figure. The collection width in boron compensated material was 0.30 to 0.35 micrometer, and 0.20 to 0.25 micrometer in uncompensated material, see Figure 4-10. The effect of boron compensation, already noted in the Semi-Annual Report, was to increase red response and effective collection width. However, poor field profile due to high space charge density, i.e., 10^{16}-10^{17}cm^{-3} as noted in Section 2.2.2, is a fundamental limitation on collection width.

Current collection in CVD cells was most accurately described by a double junction model(2). Analysis of collection efficiency data according to this model yielded hole mobility-lifetime products in the range 2-4 x 10^{-9} cm^2/V. These values were consistent with the diffusion length and space charge density values described above.

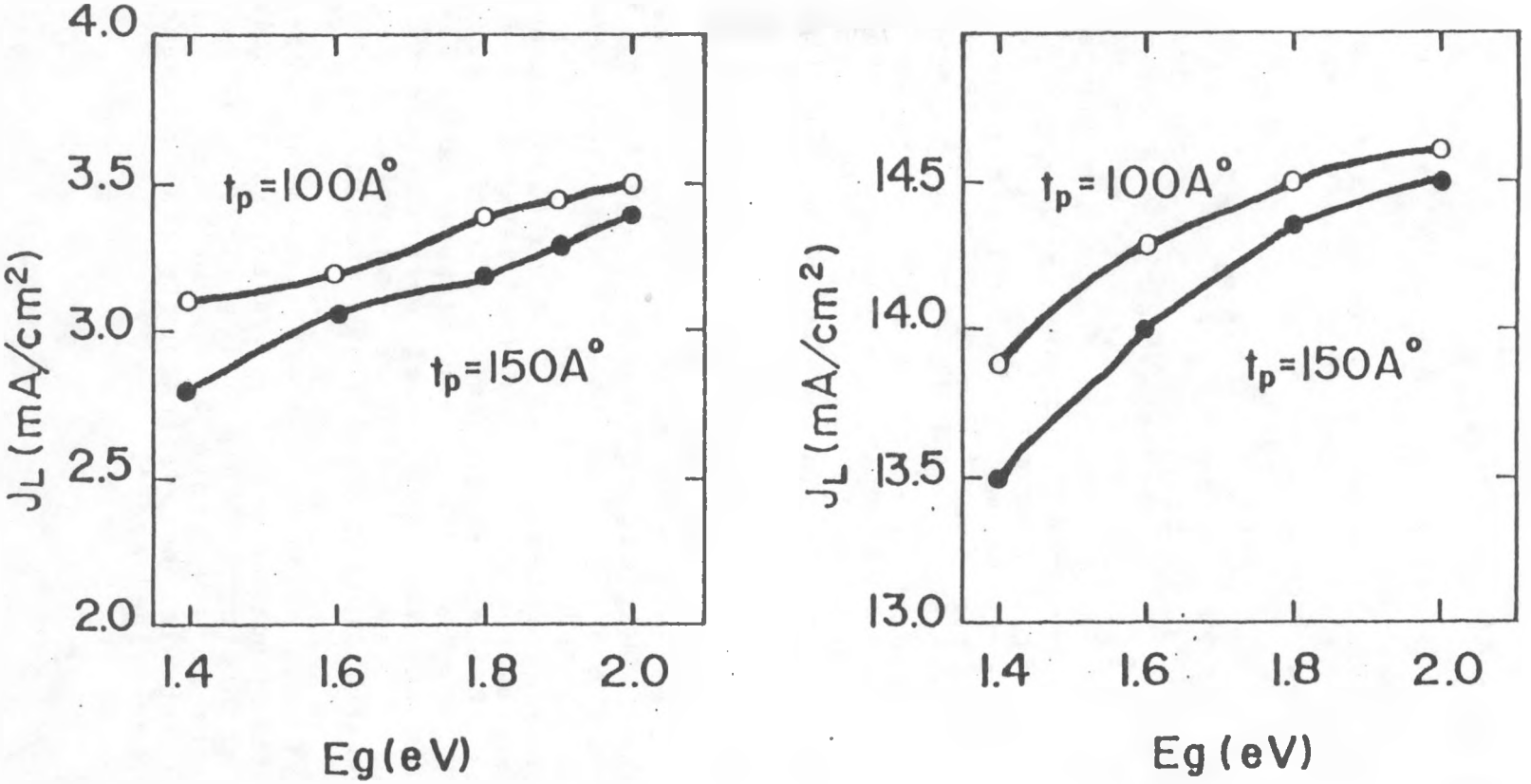

Figure 4-8. Calculated Light Generated Current Versus P Layer Band Gap

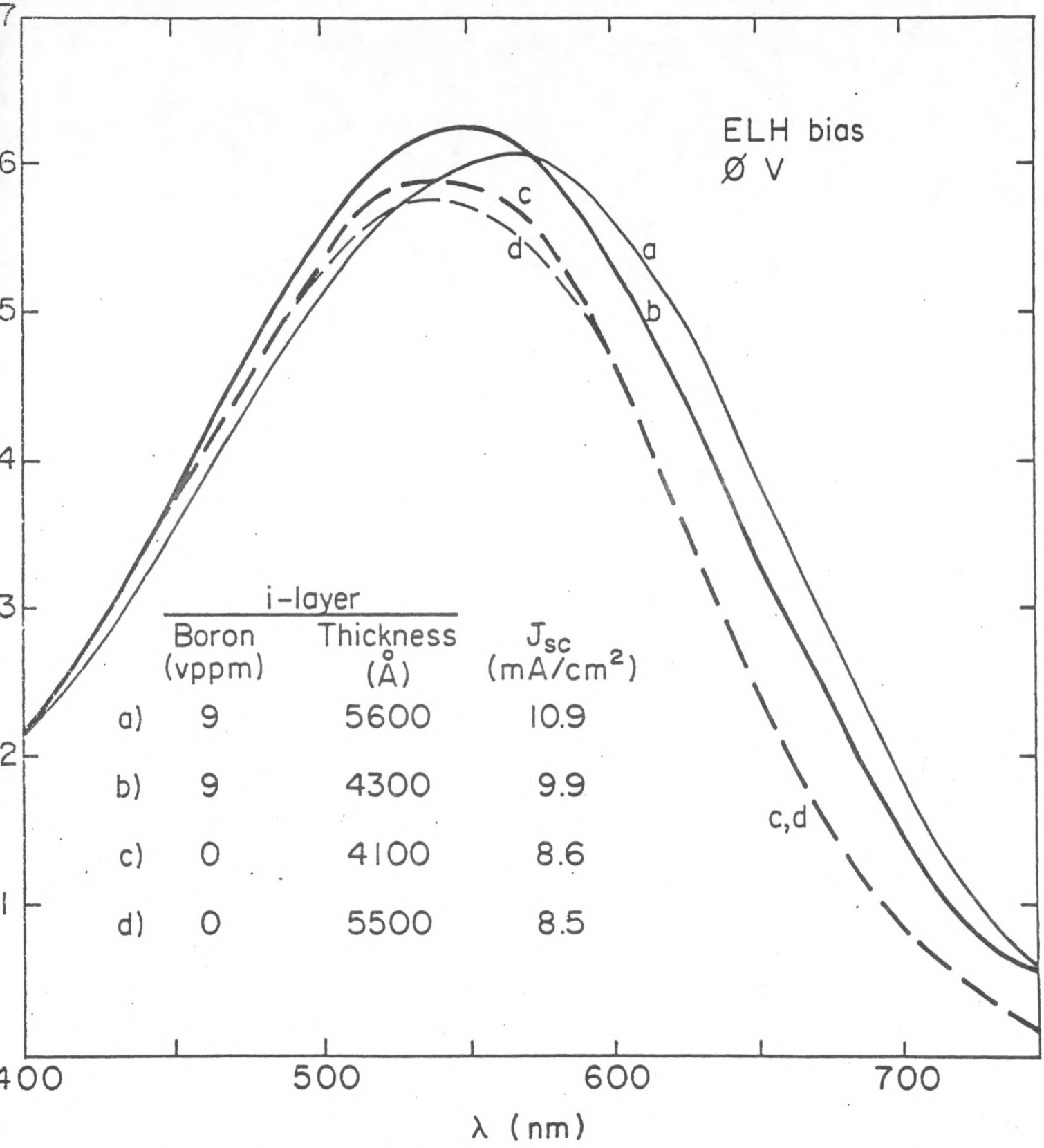

Figure 4-9. Spectral Response of CVD p-i-n Cells: Effect of Intrinsic Layer Boron Compensation

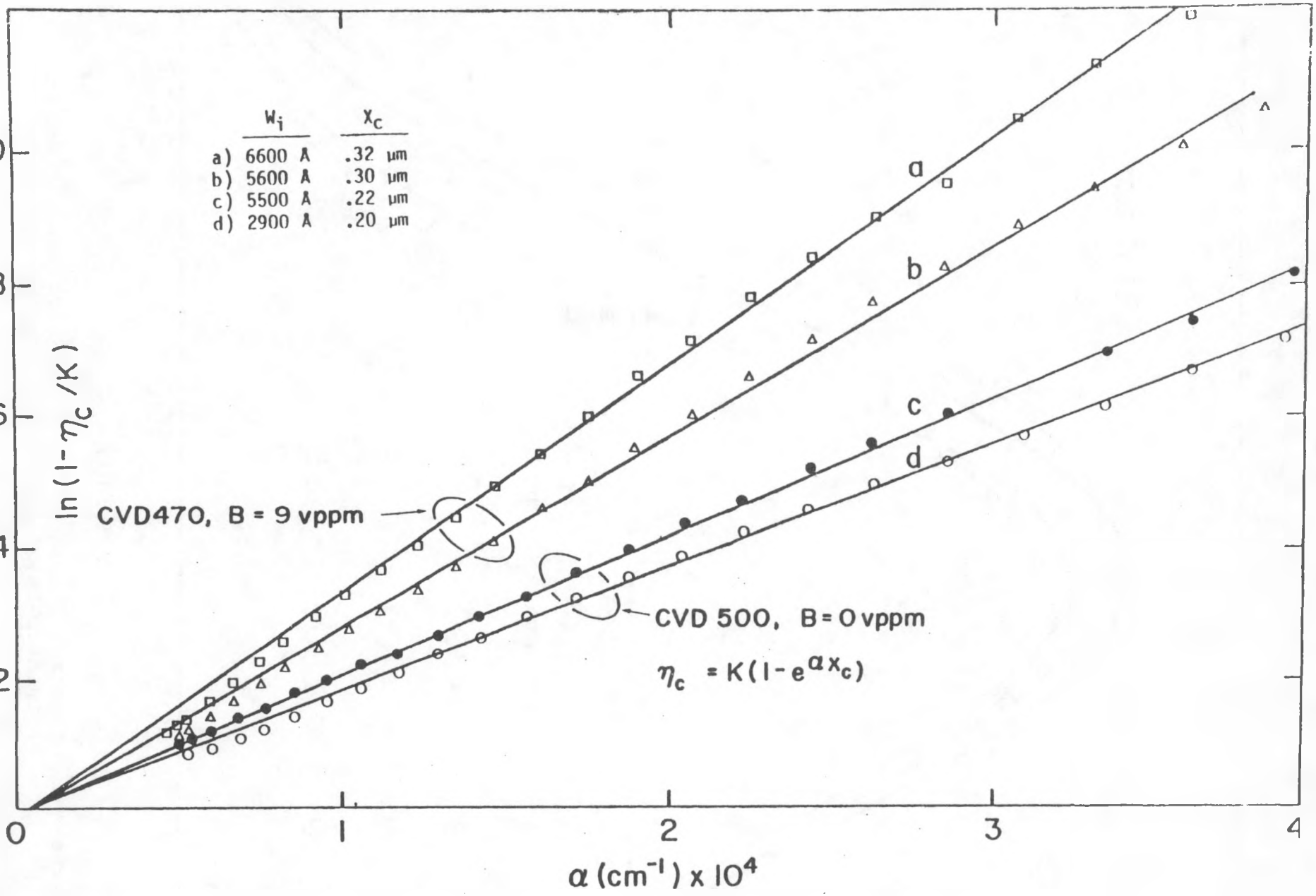

Figure 4-10. Determination of Collection Width

4.3 Sumary of Phase I Device Development

PARAMETER	TARGET	ACHIEVED
V_{oc}	0.7-0.8	0.74 V
J_{sc}	11-13	10.9 mA/cm^2
FF	55-65	49%

The highest efficiency achieved was 4% with CVD intrinsic layers deposited at 1 A/s. An efficiency of 3.6% was attained with CVD intrinsic layers that were deposited at 9 A/s.

Open circuit voltage (best value = 0.74 V) is not a limiting factor for achieving 6% efficiency. Short circuit current with boron compensated intrinsic layers (best value = 11 mA/cm^2) should be adequate. Moreover, optimization of the ITO with respect to anti-reflection properties would provide some improvements in current. Fill factor, however, is a major limitation for obtaining 6% efficiency. The fill factor in CVD cells is limited by high series resistance. Elimination of the light independent, or contact resistance, component of the series resistance would yield FF > 55%. Improved contact materials and optimization of the transition between doped and intrinsic layer depositions are reasonable approaches to reducing contact resistance. Thus, 6% efficiency may be attainable without major improvements in the quality of CVD intrinsic materials.

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2. Hegedus, S.S., J. Non-Cryst. Solids, 66 (1, 21), pp. 369-374 (1984).

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4. Schade, H. et al., J. Appl. Phys. 57 (2), pp. 568-574 (1985).