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PHASE 2, AUTOMATED ARRAY ASSEMBLY, TASK IV LOW-COST SOLAR ARRAY PROJECT

Final Report

October 1978

Work Performed Under Contract No. NAS-7-100-954898

Lockheed Missiles & Space Company, Inc.
Sunnyvale, California

U.S. Department of Energy

Solar Energy

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PHASE 2, AUTOMATED ARRAY ASSEMBLY, TASK IV
LOW-COST SOLAR ARRAY PROJECT

FINAL REPORT

OCTOBER 1978

Prepared By

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The JPL Low-Cost Silicon Solar Array Project is sponsored by the U.S. Department of Energy and forms part of the Solar Photovoltaic Conversion Program to initiate a major effort toward the development of low-cost solar arrays. This work was performed for the Jet Propulsion Laboratory California Institue of Technology by agreement between NASA and DoE.

FOREWORD

The results described herein represent the work performed from November 1, 1977 to October 28, 1978 by the Manufacturing Research Organization of Lockheed Missiles & Space Company, Inc. in Sunnyvale, California. The project team, headed by Mike Lopez, was staffed with the following key personnel:

Dean Housholder, Semiconductor and Device Technology

Jerry Katzeff, Laser Technology (Annealing)

Bob Casey, Automation Processes

Harold Weinstein, R&D Staff, Photovoltaic Devices, International Rectifier Corporation

Other principal contributors included John Knudson, Ion Implantation; and Cheryl Bostwick, Screen Printing of Contacts.

The JPL Contract Technical Manager was B. D. Gallagher.

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Section 1

SUMMARY

This contract was to verify the technological readiness of a select process sequence with respect to satisfying the Low Cost Solar Array Project objectives of meeting the designated goals of $.50 per peak watt in 1986 (1975 dollars). The sequence examined consisted of: 3" diameter "as-sawn" Czochralski grown 1:0:0 silicon, texture etching, ion implanting, laser annealing, screen printing of ohmic contacts and sprayed anti-reflective coatings. The contract was a one (1) year effort.

The texture-etching process as furnished by JPL was exercised using the sodium hydroxide (NaOH) solution on representative "as-sawn" wafers. The initial "flash-etch" step consisting of a solution of nitric, hydrofluoric and acetic acids to remove saw damage from the silicon surfaces prior to the texture-etch step was eliminated, thereby simplifying the process. A 1%-2% solution of NaOH followed by a neutralizing step of hydrogen peroxide-sulfuric acid solution resulted in acceptably etched wafers. Texture-etched wafers processed into functional cells were comparable in electrical output (η = 10% AM1) to those flash etched. Both types were electroless nickel plated, solder dipped and AR coated by vacuum evaporation.

Ion implantation evaluations for junction formation with phosphorus was performed with a Lockheed Acceleration, Inc. Model MP400 unit and an International Rectifier Extrion Model 20-200 unit. The Extrion 20-200 implanter proved best suited for the solar cell junction formation due principally to the lower acceleration voltage levels necessary for shallow junction devices. For our work, wafers were implanted at the lowest practical level of 25 KeV, with a beam current of 150 μA, and at a 7° tilt angle to minimize channeling. Best cell results were attained at the 2.5 to 3 x 10^{15} ions/cm^2 fluence levels. Acceleration voltage levels of 5 to 10 KeV are more desirable for shallow junction solar cells and will also minimize the bucking drift field created near the immediate silicon surface during implantation due to the Gaussian

ion distribution. It is felt that this bucking field can be eliminated through the use of a programmed implant cycle, where the acceleration voltage can be automatically varied with time, holding the beam current constant.

Cells implanted and thermally annealed compared favorably in electrical output with diffused junction cells, and were used as controls for the evaluation of the subsequent laser annealing step.

Laser annealing work consisted of experimentation with various available lasers using implanted wafers. With the absorption coefficient of silicon as the guiding criteria, it was decided that the most suitable lasers for silicon annealing are ruby, Nd:YAG or Frequency Doubled Nd:YAG with wavelengths of 694 nm, 1064 nm, and 532 nm, respectively. Extent of annealing was determined by measurements made with a 4-point probe. Impurity profiling, as implanted and after annealing, was performed by Secondary Ion Mass Spectrometry (SIMS). Energy densities on the order of 1.5 joules/cm^2 were found necessary to achieve annealing using a ruby laser; whereas, with the Nd:YAG lasers used for this work, energy densities of >2 joules/cm^2 were required.

Approximately forty (40) cells, 1 x 2 cm, 2 x 4 cm and 3 inches diameter, were fabricated at the conclusion of this program, which were ion implanted, Nd:YAG laser annealed, vacuum evaporated Ti/Pd/Ag contacts and evaporated SiO_2 AR coating. These cells yielded AM1 conversion efficiencies ranging from 10.1 to 13.3% with an average of 12.3%. This represents a significant step towards reduction-to-practice of a potentially high volume, low cost process, and warrants continuation for scale-up.

Screen printing of ohmic contacts did not prove entirely successful during the course of this contract. Using some generally accepted silver and silver-aluminum pastes, namely, DuPont 7095 and 7095+ Alcoa aluminum powder 7123, and a 325 mesh stainless steel screen, difficulty was experienced in the firing schedule which were manifested in poor cell curve functions. Also highlighted in our work, was the high cost of conductive paste materials,

which appears questionable towards meeting the LSA cost goals. This screen printing work was not pursued further due to the extensive investigations by other participants in this PROJECT.

Sprayed-on AR coating evaluations were conducted with a vapor carrier auto-coater system. Best thickness uniformity of 1100Å to 1240Å was attained on a 3/4" width pattern with a single spray pass. Multiple passes and work indexing was required for a 3-inch diameter cell. Improved nozzle and vapor spreader design and precision fabrication are required for optimized performance of this equipment. A tantalum solution sprayed on 3-inch texture-etched cells yielded a 7% electrical output increase which appears consistent with published literature on AR-coated textured surfaces.

High volume production projections were made on the selected process sequence. Automated processing and movement of hardware at high rates were conceptualized to satisfy the PROJECT's 500 MW/yr capability. A production plan was formulated with flow diagrams integrating the various processes in our cell fabrication sequence.

Section 2

INTRODUCTION

This contract was a process development effort to verify the technological readiness of a selected process sequence from the "as-sawn" Czochralski grown silicon wafers to the module assembly.

The process investigated consisted of the following sequence:

- Starting material: 3-inch "as-sawn" CZ silicon wafers
- Texture etching of silicon wafers using sodium hydroxide
- Junction formation by ion implantation of phosphorus
- Laser annealing of ion implanted wafers
- Screen printing of Ag, Ag-Al for ohmic contact
- Spraying of Tantalum oxide AR coating
- Assembly of modules using the LMSC module design, developed under the JPL Contract 954653, as baseline

This selected process sequence was evaluated for its technical potential of achieving the economic goals of the Low Cost Solar Array Project of $.50/watt for 500 megawatt/year production by 1986.

Specific areas of investigation under this contract consisted of the following:

- Performance of detailed technical and economic evaluations of the selected process sequence
- Preparation of process step descriptions detailing input-output requirements and characteristics, and identifying materials, supplies and equipment utilized

- o Performance of critical reviews to identify processing areas which require significant development, or proof of operation to reach the PROJECT goals
- o Performance of process verifications of the selected sequence
- o Demonstration of the technological readiness of the selected process by fabrication of cells

Solar cells were fabricated and evaluated for their respective efficiencies and throughput. The SAMICS format was utilized for inputs in the determination of economic considerations.

International Rectifier, El Segundo, California worked jointly with us to satisfy the various facets of the contract.

Two process steps of the specified sequence received greater emphasis in this contract. These were: laser annealing and sprayed AR coating. Laser annealing offers the potential of reduced energy consumption and improved efficiency at no loss in throughput over conventionally practiced techniques. Automated spray coating of anti-reflective film has the potential of improved thickness control and uniformity over large surface areas. The balance of the steps in the cell processing sequence were performed only to provide a supply of wafers with which to exercise the laser anneal and spray coating work. These were considered routine and were studied in greater detail by other contractors.

At the outset, fabricated cells using our process sequence were to be assembled into the Lockheed-designed module configuration. The effort was later redirected resulting in deletion of the module work so that resources could be more effectively applied to the main stream of cell processing.

Section 3

TECHNICAL DISCUSSION

3.1 TECHNICAL AND ECONOMIC EVALUATION

A detailed evaluation of our selected process sequence was conducted and reported in the quarterly reports. The sequence consisted of: texture etching, ion implanting, laser annealing, screen printing ohmic contacts and spray-on AR coating. Our analyses of the individual process steps are summarized in the following paragraphs.

3.1.1 Texture Etch

There is general agreement among the LSA contractors that texture etching is a viable process for use on <1:0:0> single crystal silicon. The low cost potential compared with the standard polished surfaces, makes texture etching highly attractive for attaining low reflectance surfaces. The need for decreased surface reflectance is well documented in the literature and through work performed by other JPL/DOE contractors on this LSA PROJECT.

High volume, high throughput potential to satisfy the 500 MW capability is attainable. A high volume production processing concept was identified which utilizes cassettes containing 50 cells, moving via conveyors through the various solutions at a rate of 2 feet/minute. Estimated output rates from such a system are on the order of 200 wafers/minute, which are of sufficient magnitude for the high volume PROJECT goal. The flash etch step using nitric (HNO_3)/hydrofluoric (HF)/acetic (CH_3OOH) acid solutions for saw damage removal was eliminated without any apparent deleterious effects on the performance of the cells. Likewise, it is believed the post texturizing hydrogen peroxide step can be replaced by a fully integrated in-line force flush water spray system. This would eliminate the use of environmentally undesirable chemicals, simplifying the process and lowering costs.

There is some question on the compatibility of textured surfaces with laser annealing, one of our selected process steps. Work performed to date with laser annealing points to the necessity for surface melting in order to obtain proper electrical activation. Thus, the topography of the surface is changed from sharp pyramidal structures to "rolling hill" contours. The effects of melting on the cell junction are discussed in the process verification section under laser annealing.

There is further concern that texture etching increases handling damage, complicating the processing and can lead to lower cell yields. This is caused by the fragile nature of the pyramidal points formed and their susceptibility to breaking, which can then expose the junction.

An alternate to the "wet" chemical texture etching process is plasma etching, where substantial savings can be realized through the elimination of expensive chemicals, and subsequent chemical disposal cost. Also, only one side etching may be performed, thereby saving silicon material losses. Throughput rates, however, need to be improved in order to make this process viable. It is our opinion that plasma etching should be scrutinized more closely as a potential replacement for the wet chemical texturizing process for solar cells.

3.1.2 Ion Implantation

General acceptance of ion implantation for junction formation is primarily based on the high throughput potential. Other significant attributes consist of better control of the doping quality and quantity, and doping profile. These are characteristics essential to insure cell uniformity, quality and repeatability.

The primary disadvantage currently encountered during implantation is the formation of an essentially amorphous surface layer due to impurity ion collisions with the single crystal silicon lattice. Present means for restoring

crystallinity in the surface layer and activating the impurity ions is by thermal annealing in a furnace at 900° to 1000°C for 15 to 45 minutes. Although this technique restores the crystal structure to an acceptable level, it also causes excessive impurity diffusion and introduces bulk dislocation loops in the subsurface silicon due to the high temperature thermal cycling. This causes trapping centers which reduces cell efficiency. This is true to a certain degree for any doping technique requiring a thermal diffusion or redistribution of the desired impurity. Laser annealing obviates this thermal cycle of the bulk silicon by heating only the surface layer, thus, leaving the bulk silicon essentially free of thermally induced dislocation loops.

The automation potential of ion implanting is very high, being limited by mechanical cell handling and the ability to cool cells during implant. New implanters are available from Extrion and Lintott with 2×10^{-3}A and 4×10^{-3}A beam currents, respectively, lowering implant time per cell to seconds. As an example, calculations based on a present Extrion 20-200 system with a 50 μa beam current result in an implant time of 209 seconds. This compares with soon to be available dedicated 10 ma beam current systems which can reduce the time to 1 second. With the short implant time, the major obstacle to achieve high throughput lies in the cell handling.

In view of the potentially short implant time, a high volume, high throughput process was conceptualized during the course of this contract (reported in Quarterly Report No. 3) which reflects the 1 wafer/second rate of a 10 ma beam current system. This concept addresses the movement and handling of cells at a rapid rate, and is summarized in Section 3.4, High Volume Production Plan. A production rate of 3000 wafers/hour is projected per implanter.

3.1.3 Laser Anneal

Based on the published literature[1-4], laser annealing offers several technical advantages over the presently utilized furnace annealing technique. The advantages are:

1. Reduction by one to two orders of magnitude of the bulk silicon dislocations introduced by present furnace anneal techniques
2. Increase in the minority carrier lifetime in the implanted layer and in the underlying substrate material
3. Change of the implanted concentration profile from an undesired Gaussian distribution to a broader, nearly flat top distribution - This improves solar cell performance by eliminating the undesired bucking drift field produced by the Gaussian distribution, hence increasing the collection efficiency of the cell.
4. More complete regrowth of the implanted surface resulting in fewer dislocation loops and stacking faults due to the higher temperature achieved with pulsed laser annealing in comparison to what is a practical temperature with furnace annealing
5. Precision control of annealing depth by choice of laser type can be accomplished since most of the energy expended will be dissipated near the silicon surface and will depend on the wavelength of the particular laser chosen and its absorption coefficient in silicon

The guiding criteria in selecting a laser system for solar cell annealing falls into three categories which are as follows:

1. The laser must be capable of providing sufficient power and energy to allow the required annealing process to take place.
2. The laser must be of a suitable wavelength to minimize the depth of beam penetration into the silicon.
3. The laser must be capable of annealing the cells at energies and speeds which would make the system cost compatible with the PROJECT objectives.

Since the light absorption coefficient, Figure 1, of silicon and consequently the mean absorption length increase considerably with increase in the wave-

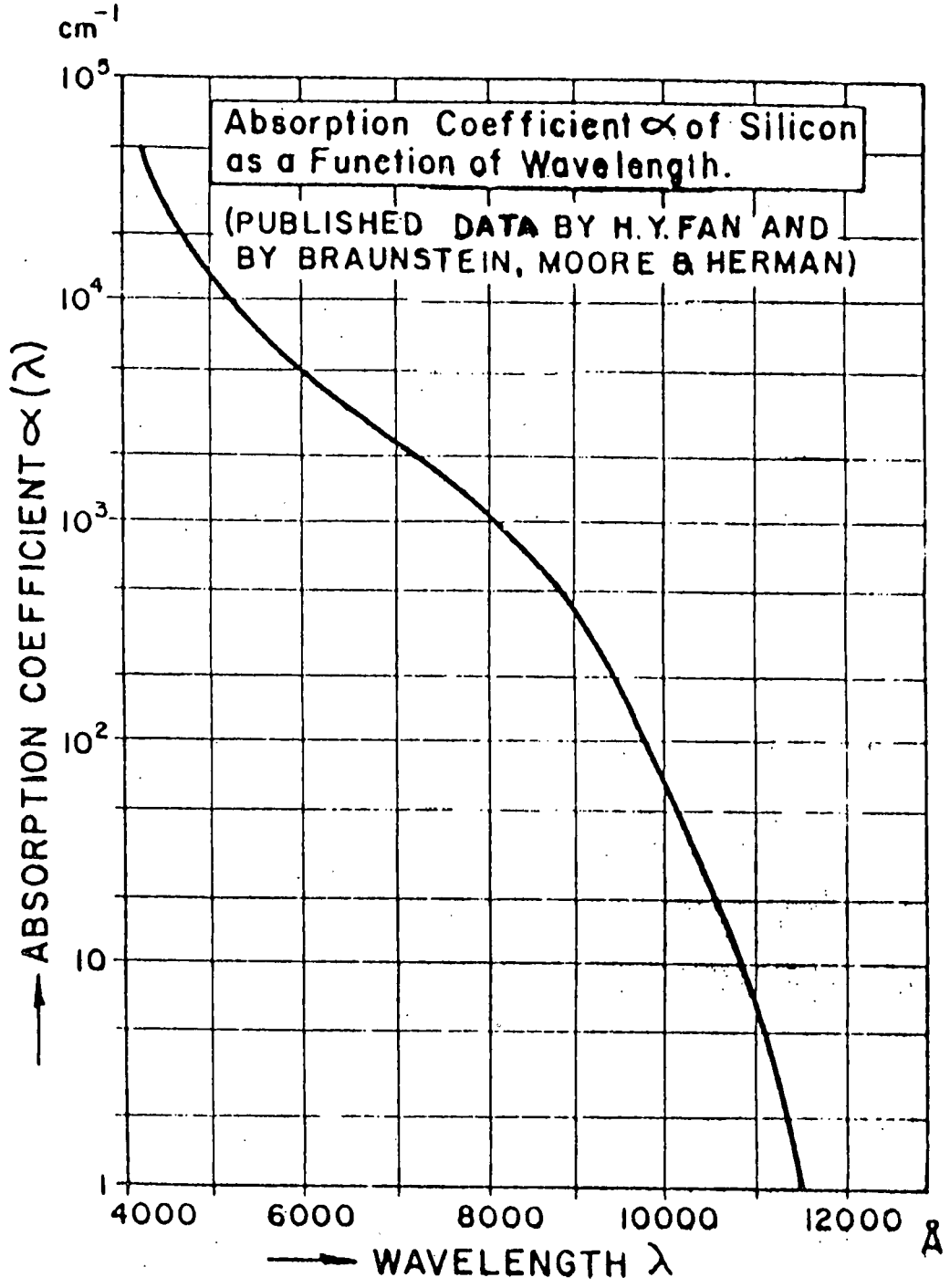


Figure 1. Absorption Coefficient ∝ of Silicon as a Function of Wavelength

length of the incident beam, it was concluded that no laser exceeding the wavelength of a YAG laser need be considered. The three lasers which appeared to be the best candidates for this evaluation were ruby, Nd:YAG, and Nd:YAG/SHG (a Nd:YAG laser coupled to a second harmonic generator, or as it is also called, a frequency doubler). These lasers have wavelengths of 694 nm, 1064 nm, and 532 nm, respectively. Based on the high throughput projection requirements for the LSA PROJECT, only pulsed laser systems were considered.

Transitions from amorphous to single crystal layers with pulse annealing are due to the formation of a liquid-solid system during laser irradiation.

It has been reported by other researchers[1,5] that annealing of the implant damage and electrical activation of the implanted ions can be achieved with a continuous wave (CW) argon laser (λ = 488 nm) through a solid-solid reaction. To obtain a solid-solid reaction, the surface to be annealed is maintained below its melting point. The duration that a surface point requires for annealing is in the order of several milliseconds. This time span in relation to incident energy is apparently long enough to anneal the implant damage and electrically activate the implanted ions but is too short for profile changes to occur.

On the first glance, it may appear that for a wavelength dependent process, CW annealing offers the advantages of creating shallow junctions by annealing and activating the surface while maintaining the relative immobility of the junction. It is our feeling, however, that extremely shallow junctions for solar cell applications can be attained through low level implants $\sim$ 5 KeV followed by annealing with a frequency doubled Nd:YAG or Nd:Glass laser at λ = 532 nm. Annealing with the frequency doubled laser should not only yield shallow junctions but will also change the implanted concentration profile from an undesired Gaussian distribution (unaltered after CW annealing) to a broader, nearly flat top distribution. This improves solar cell performance by eliminating the undesired bucking drift field produced by the Gaussian distribution, hence increasing the collection efficiency of the cell.

By utilizing pulse annealing, it appears that throughputs on the order of one 3-inch diameter wafer per second can be attained. Argon lasers on the other hand are of fairly low power requiring time spans on the order of minutes for annealing a 3-inch diameter wafer. The input power requirements of such a system would be prohibitive as well as the impracticality of the process in view of the high throughput requirements of the PROJECT, namely 500 MW/year fabrication capability.

Theoretical and experimental work carried out on the pulsed lasers revealed that for ruby and Nd:YAG/SHG lasers with pulse duration in the 10-30 nsec range, an energy density of approximately 1.5 joules/cm^2 is needed to attain the required annealing. This translates to approximately 68 joules for single pulse annealing of a 3-inch diameter wafer. Energy densities necessary vary with the pulse duration and wavelength. For example, investigations have shown that a Nd:YAG (1064 nm) laser with a 100 nsec pulse requires an energy density output of approximately 4.8 joules/cm^2 to effect proper annealing. A Nd:YAG laser with a longer wavelength and pulse duration is not as efficient as a ruby (694 nm) or frequency doubled YAG (532 nm) laser due to deep penetration into the silicon. Deeper penetration means greater energy losses in the bulk material rather than at the immediate surface ($\approx .2\ \mu m$), where it is required for proper annealing.

Laser annealing is conducive to high throughput manufacturing. Performed in an air atmosphere, a 3-inch diameter single pulse system is projected for the LSA PROJECT high volume capability. With a pulse duration of less than 50 nanoseconds, laser repetition rate, and wafer positioning and handling become the most important elements for achieving high throughputs. High energy demands and high repetition rates (1 pulse per second) can be satisfied with a laser that utilizes phosphate glass for its laser rod material. Rapid positioning and handling of wafers are addressed in a concept detailed in Quarterly Report No. 3, and summarized in Section 3.4, High Volume Production Plan, where quantities of 3600 wafers/hour/laser can be processed.

An economic evaluation was made showing the potential savings of laser vs. furnace annealing. This analysis was also reported in Quarterly Report No. 3,

but is again included in its entirety because of the significant cost advantages.

Cost savings realized by application of laser annealing fall into the following categories:

1. Increased cell efficiency with subsequent decrease in the number of cells, support structures, and associated hardware for a 500 megawatt production rate
2. Decrease in energy consumption realized by using laser annealing techniques as opposed to furnace annealing

Savings realized from item 1 above are as follows:

- Area of 3-inch diameter cell = 45.6 cm^2
- Illumination Intensity = 100 mW/cm^2
- Total Incident Irradiation = (45.6 cm^2) x (100 mW/cm^2) = 4.56 watts
- A 12% conversion efficiency cell yields an output of ~.55 watts
- Assuming that laser annealing can yield a 2% conversion efficiency increase or a 14% cell, the yield will be ~.64 watts
- Projected into 1986, 500 MW/yr production capability at $.50/watt, the savings represent

$$\left[\left(\frac{500\ MW}{.55\ W/cell}\right) - \left(\frac{500\ MW}{.64\ W/cell}\right)\right] \times .55\ \frac{W}{cell} \times \$.5/W = \underline{\underline{\$35,156,250}}$$

Savings realized from item 2 above are as follows:

Preliminary theoretical and experimental data indicates that for a ruby or frequency doubled glass laser, an energy density of approximately 1.5 joules/cm^2 is required to attain annealing of ion implanted silicon wafers. This translates to an energy of approximately 68 joules for

single pulse annealing of a 3-inch diameter wafer. A Q-switched glass laser capable of operating at this energy level with a pulse repetition rate of 1 pps has a conversion efficiency of approximately .5%. This system offers the following savings:

- Resistance Furnace Power Requirements*
  1.88 KW to maintain 900°C annealing temperature
  125 3-inch diameter wafers per run @ 30 min/run
  1.88 KW x .5 hr = .94 KW hr to anneal 125 cells or
  7.52 W hr/cell

- Laser Power Requirements
  68 joules required to anneal a 3-inch diameter wafer
  At .5% conversion efficiency, the laser requires 68/.005 = 13,600 joules = 3.78 watt x hr to supply the 68 joules

- 7.52/3.78 ≈ 2 or half as much energy is required for laser annealing as compared to furnace annealing

- For 500 MW/yr production capability

$$\left(\frac{500\ MW}{.55W} \times 7.52\ W\ hr\right) - \left(\frac{500\ MW}{.64W} \times 3.78\ W\ hr\right) \approx 3{,}900\ MW\ hr/yr \text{ savings}$$

3.1.4 Screen Printed Contacts

In our technical and economic evaluations of screen printing conductive pastes for ohmic contacting on solar cells, it was agreed that this technique offers the excellent prospects for low cost manufacturing to achieve the 1986 goals. High throughput screen printing equipment is available with rates up to 5000 parts/hour. Screens with 325 mesh can routinely produce patterns with excellent line definition. Screened line widths of 5 mils have been reported by participants in this LSA PROJECT.

*Thermo-Brute American Furnace, 4-1/2 inch O.D. Tube Size

Cost of materials, particularly with the silver filled pastes, is still a concern. Our estimates on large volume buys of the Ag paste approximate a cost of $.05 to $.15/watt, when applied 100% on the back, and 5-7% area coverage for the patterned front side.

Our experience in working with an "approved" Ag-filled paste using documented processes has shown that the process is not yet entirely foolproof. Working with DuPont 7095 material, firing schedules were used which ranged in temperatures from 550°C to 690°C and times of 20 seconds to 2 minutes with only limited success.

It is recognized that this area, including the copper and aluminum paste materials, is being investigated extensively by other participating firms, and through these efforts, it is believed that this could soon become a viable process.

Our high volume production concept, reported in Quarterly Report No. 3, reflects a screen printing and firing rate of 9000 cells/hour/unit equipment.

3.1.5 Spray-On AR Coatings

General concensus is that spray-on AR coatings offers the best chances for high throughput and good coating thickness uniformity over large surface areas. Also, spraying is not as sensitive to irregular surface finishes, such as for texture-etched cells, as compared with spin coating.

A high throughput capability was conceptualized (detailed in Quarterly Report No. 3) where a production rate of 9000 cells/hour/machine was projected.

3.2 CRITICAL REVIEWS

3.2.1 Texture Etching

It has been fairly well established that the wet chemical process for

anisotropically texture etching using 1-2% solution of hot sodium hydroxide can satisfy the 1986 Project goals.

It is felt that further process verification should be conducted to determine the merits of replacing the post etching hydrogen peroxide/sulfuric acid neutralizing step with force flush DI water rinses.

Significant development still required to meet the 1986 cost goals consist of:

- o In-process monitoring of etch solution, textured wafer reflectivity, rinse solution pH, etc.
- o Automatic inspection for process uniformity and product quality
- o Etch and rinse solution disposal and reclamation
- o Equipment automation design and integration of monitor feedback loops

3.2.2 Ion Implant

As previously stated, ion implantation is considered a viable approach from both a technical and economic standpoint. At present, off-the-shelf equipment for optimum implantation of solar cells, i.e., <10 KeV @ >10 ma beam current is not readily available, although the technology base exists for fabricating a "dedicated" implanter. Implantation of the presently available higher acceleration voltages (>20 KeV) result in a front surface bucking drift field which reduces cell output unless annealed in a furnace utilizing background doping. Laser annealing, and it is expected E-beam annealing, minimizes this problem. Another technique for minimizing the bucking current drift field is to tailor the impurity profile during implantation. This can be accomplished with a programmed implant cycle that varies beam energy and time, holding the beam current constant. Because of equipment limits (minimum of 25 KeV acceleration voltage), this technique was not verified.

Major areas for investigation in ion implantation recommended for the 1986 objectives are:

- o Ion implantation junction profiling by beam energy programming
- o Development and fabrication of a high beam current, high throughput, dedicated ion implanter

3.2.3 Laser Anneal

Reduction of the annealing process time and energy consumption with the use of pulsed laser energy beams offers excellent prospects for achieving the high volume, high throughput goals of the PROJECT.

Equipment limitations were experienced during our work on laser annealing. Most of the lasers available for our work were of low energy, delivering small beam spot sizes at the energy densities needed for annealing. Equipment is available* from established cataloged product lines which is capable of delivering energies required for single pulse annealing of 3-inch diameter wafers. This equipment, however, was not available for evaluation. Ruby lasers with a wavelength of 694 nm are well suited for laser annealing, however, suffer in the scale up to accommodate wafers beyond approximately 1.4 inches in diameter. The maximum size of the available ruby rod is 7/8 inch in diameter delivering only 15 joules of energy, and therefore, necessitating step and repeat mode of processing for annealing 3-inch diameter wafers. Glass rod lasers on the other hand do not suffer from this limitation and are, therefore, ideally suited for annealing of large size wafers.

Laser pulse annealing in the energy densities required for suitable ion activation causes surface melting. This has no deleterious effects on the cell junction for polished or flash-etched cells. With texture-etched cells, the prominent pyramidal structures are significantly changed, a condition which appears to cause junction non-uniformity hence adversely affecting the cell function.

*Quantel International, 928 Benecia Avenue, Sunnyvale, Ca. 94086 (408) 735-7313

Even though texture-etched surface cells have received general acceptance for the reason of improved solar absorption over other surface types, a case could be made for utilizing flash-etched cells with laser annealing followed by the projected low cost spraying of AR coating. We have found that electrical output of flash-etched/AR-coated cells are comparable to the texture-etched/AR-coated cells. Substitution of flash etching for texture etching could contribute to reduced costs without compromising performance, since a coating of some type will be required in either case.

It is difficult to declare any major technical shortcomings of the laser annealing process at this time. Perhaps, the fact that the single 3-inch diameter pulse has not been demonstrated could be cause for some concern. It follows that additional experimentation should be done with lasers capable of annealing at least a 1-inch diameter area. From this we can ascertain beam energy uniformity across the wafer surface together with recognition of the need for better optics.

Major areas of investigation required in order to meet the 1986 goals are:

- o Process interdependence data of the relationship of wafer surface melting vs. junction movement vs. reflectivity vs. AR coating
- o Laser beam control using optics to improve beam energy homogeneity on wafer surfaces
- o Acquire a capability for scale-up performance of laser annealing

3.2.4 Screen Printing

Screen printing of ohmic contacts is feasible insofar as line definition and conductor thickness are concerned. Considerable difficulty can still be expected in firing the pastes after screening. In addition, the quality of pastes from lot to lot is highly suspect. In performing our process verification tests several points of critique were uncovered, namely:

- o Closer control (specification) of conductor paste must be made.
- o Presently available belt furnaces are not adequate to accommodate short firing duration pastes (e.g., in the 10 to 30 second range).
- o Use of silver and silver-aluminum pastes are too expensive to meet PROJECT cost goals.
- o Glass-lined belt furnaces should be evaluated to facilitate periodic cleaning.
- o Use of diffusion tube firing is both expensive (energy) and slow (difficult to automate).

3.2.5 Spray-On AR Coatings

Spray coating of an AR film has shown good promise as a cost effective, high throughput process. Equipment is presently available which exhibits controllable parameters necessary to deposit these coatings. However, the most precise spray nozzles and vapor spreaders presently available from the equipment manufacturer limited our uniformity of coated film width to 3/4 inches. Increasing the nozzle height normally widens the deposited film on the cell, but in this case, film thickness uniformity was compromised. It appears that additional effort is required to optimize nozzle and vapor spreader configuration and design.

3.3 PROCESS VERIFICATION

3.3.1 Texture Etching

The texture etching process was performed as part of this contract to verify its adequacy to meet the LSA objectives, and to fabricate cells for use in evaluating the rest of our process sequence.

The procedure, as supplied for use in processing as-sawn wafers, called for a flash etch step consisting of a nitric (HNO_3) - hydrofluoric (HF) - acetic

acid (CH_3OOH) solution, followed by sodium hydroxide (NaOH) texturizing and a neutralizing step of hydrogen peroxide (H_2O_2) - sulfuric acid (H_2SO_4) rinse.

The flash etch step was deemed too costly to meet the overall PROJECT cost objectives, and was subsequently eliminated without any apparent deleterious effects on the performance of the cells. The procedure used calls for a 1% solution of NaOH followed by the H_2O_2/H_2SO_4 neutralizing step and DI water rinses. Wafers processed by this modified texture etch process are typified in the photomicrograph shown in Figure 2.

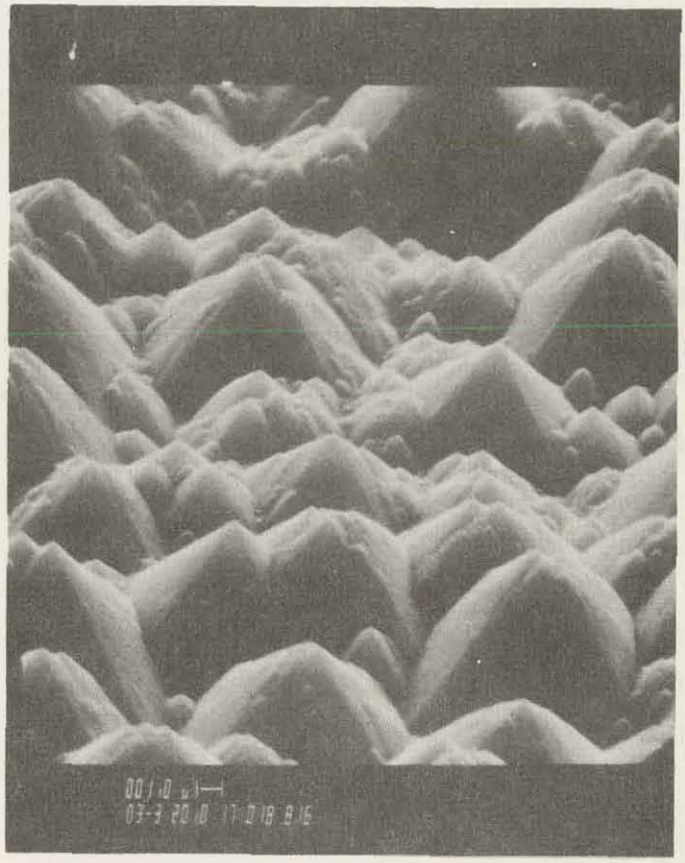


Figure 2. SEM Photomicrograph of Typical Texture-Etched <100> Silicon Wafer Using 1% Solution of NaOH

The hydrogen peroxide/sulfuric acid neutralizing rinse has been eliminated in our projected high volume, high throughput process, as we believe that the simpler dilute H_2SO_4 acid rinse will suffice if followed by multiple DI water sprays. The projected process is detailed in Quarterly Report No. 2.

Due to the time and cost involved in repeated process checks by SEM analysis, required for control of this process, an in-line tester was constructed and used. This instrument was constructed as a quick reference to check the reflectance of the texturized surfaces being produced and was useful regardless of the texturizing process used. It consists of directing light from a light tower through a hole in a black box at normal incidence to the surface of the silicon wafer being measured. Light from the irradiated surface is reflected to silicon photocells mounted on the under surface of the "black box" top, adjacent to the light entrance hole. Short circuit current measurements of these photodetectors give relative reflectance values. For example, semi-polished chemically etched wafer surface exhibited approximately 4 times the reflectance of the NaOH etched groups. This kind of in-process testing (reflectance) could be a regular feature for Q.A. control of texture-etched surfaces and to serve as an adjunct to other generally employed criteria such as SEM analysis. In addition, this type reflectance measurement may later be utilized as a means for screening/categorizing cells for laser anneal, where the reflectance may influence power settings on the laser.

Cells were fabricated in identical fashion except for the wafer surface finishes to verify the adequacy of our texture-etched process. One run was flash etched (#117) and the other texture etched (#118). The POCL diffusion process was used for junction formation with electroless nickel-plated solder-coated contacts and evaporated SiO coatings. Both types of cells exhibited 10% conversion efficiencies with fill factors of 75% and 67%, respectively. Figures 3 and 4 show representative I-V curves from these runs.

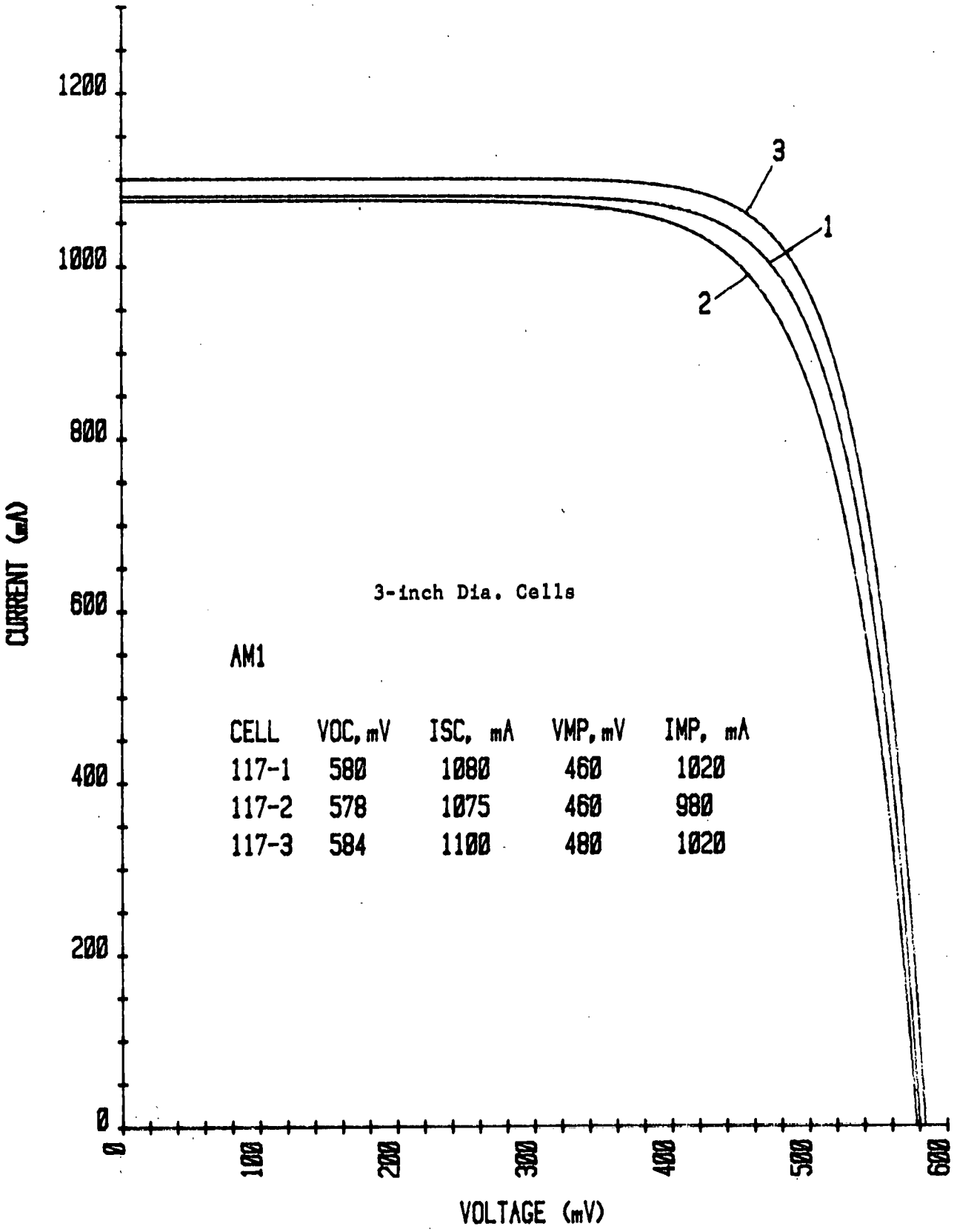


Figure 3. I-V Output for Run No. 117, Cells 1, 2, and 3

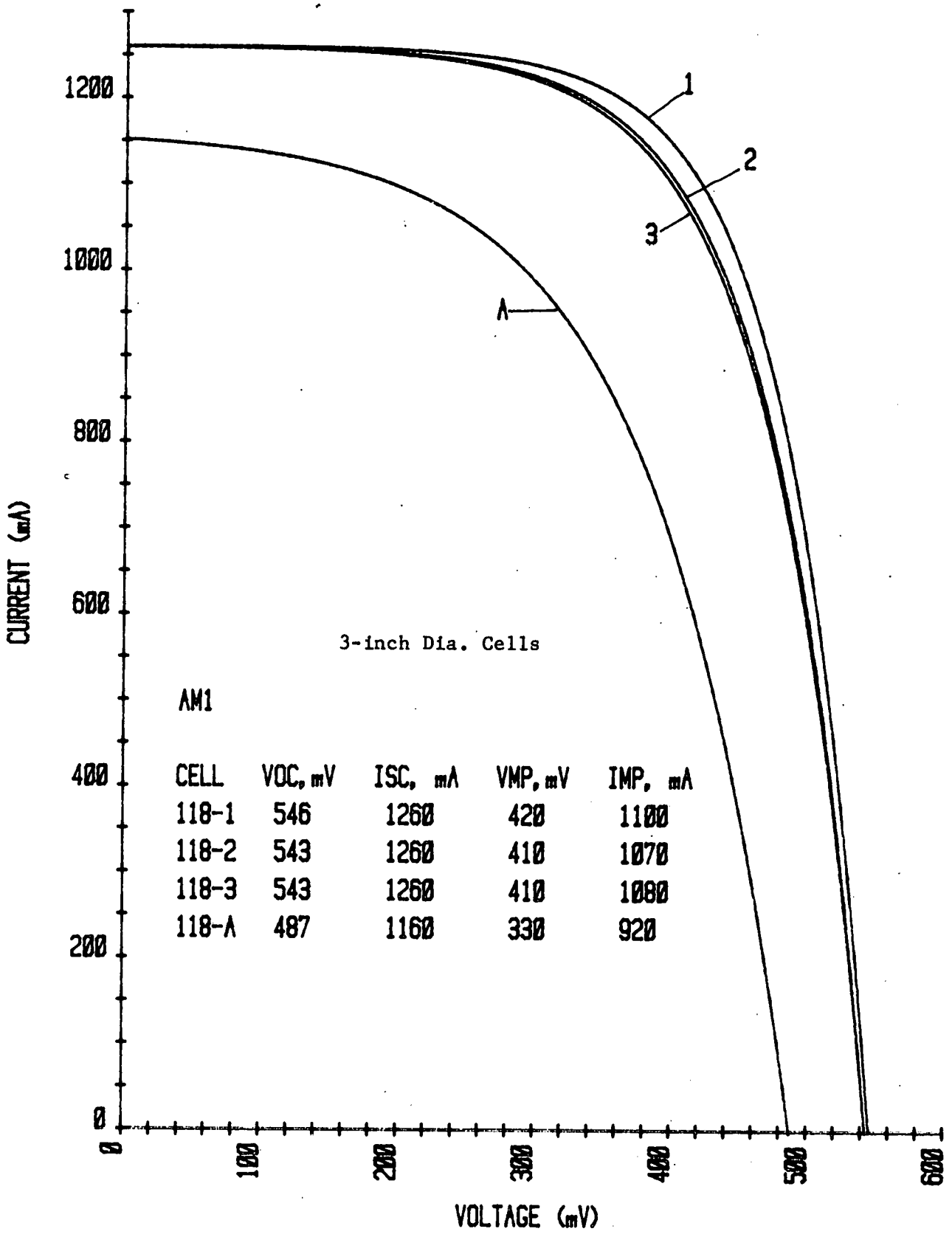


Figure 4. I-V Output for Run No. 118, Cells 1, 2, 3 and 4

3.3.2 Ion Implantation

Verification of ion implantation as a viable process for doping solar cells was accomplished using an Extrion 20-200 (International Rectifier) and an Acceleration, Inc. MP-400 (Lockheed) implanter. Several runs were initially made using implant energy variations ranging from 25 KeV to 140 KeV to determine equipment parameter and effect on cell performance. The higher energy level tests were implanted through SiO_2 to limit ion penetration and reduce the effect of the bucking drift field effect resulting at the front surface due to the Gaussian ion distribution. Fluence dosage levels were varied from 1×10^{15} to 3×10^{15} ions/cm^2 for the ^{31}P dopant. Table 1 shows some of the parameters investigated during the initial test phase.

Some of the initial ion-implanted cells completed for "first look" used the following sequence:

- o 3-inch diameter wafer, texture-etched
- o Ion implanted, 50 KeV, 1×10^{15}/cm ^{31}P
- o Thermal anneal, 900°C/15 minutes
- o Screened-on grid resist
- o Electroless nickel plate front and back
- o Resist removal
- o Edge-etch
- o Solder dip

Electrical outputs of two cells processed using the above sequence as measured with a Spectrolab X-25 Solar Simulator are shown in Figure 5. The cell outputs as measured at AMO represent 7% efficiency at Pmax. This converts to approximately 9% at AM1.

TABLE 1

WAFER IMPLANTATION PARAMETERS

Surface Condition	Beam Energy/Dosage	Implanter	
		Extrion (IR)	Acceleration (LMSC)
TE, No Oxide	50 KeV/1 x 10^{15} ^{31}P	X	
TE, Oxide	125 KeV/1 x 10^{15} ^{31}P		X
TE, Oxide	125 KeV/1 x 10^{15} ^{31}P 150 KeV/5 x 10^{14} ^{11}B		X
Pol. Oxide	125 KeV/1 x 10^{15} ^{31}P		X
TE, Oxide	125 KeV/1 x 10^{15} ^{31}P		X
TE, Oxide	125 KeV/1 x 10^{15} ^{31}P 200 KeV/1 x 10^{15} ^{11}B		X
TE, Oxide	140 KeV/2 x 10^{15} ^{31}P Evap. Alum. BSF		X
TE, Oxide	25 KeV/1 x 10^{15} ^{31}P	X	
TE, No Oxide	25 KeV/3 x 10^{15} ^{31}P 150 KeV/5 x 10^{15} ^{11}B		X
FE, Oxide	65 KeV/3 x 10^{15} ^{31}P	X	
FE, Oxide	25 KeV/1 x 10^{15} ^{31}P Evap. Alum. BSF	X	

NOTE: All Wafers 3" diameter, 1:0:0 Orientation, 7° Angle Implants

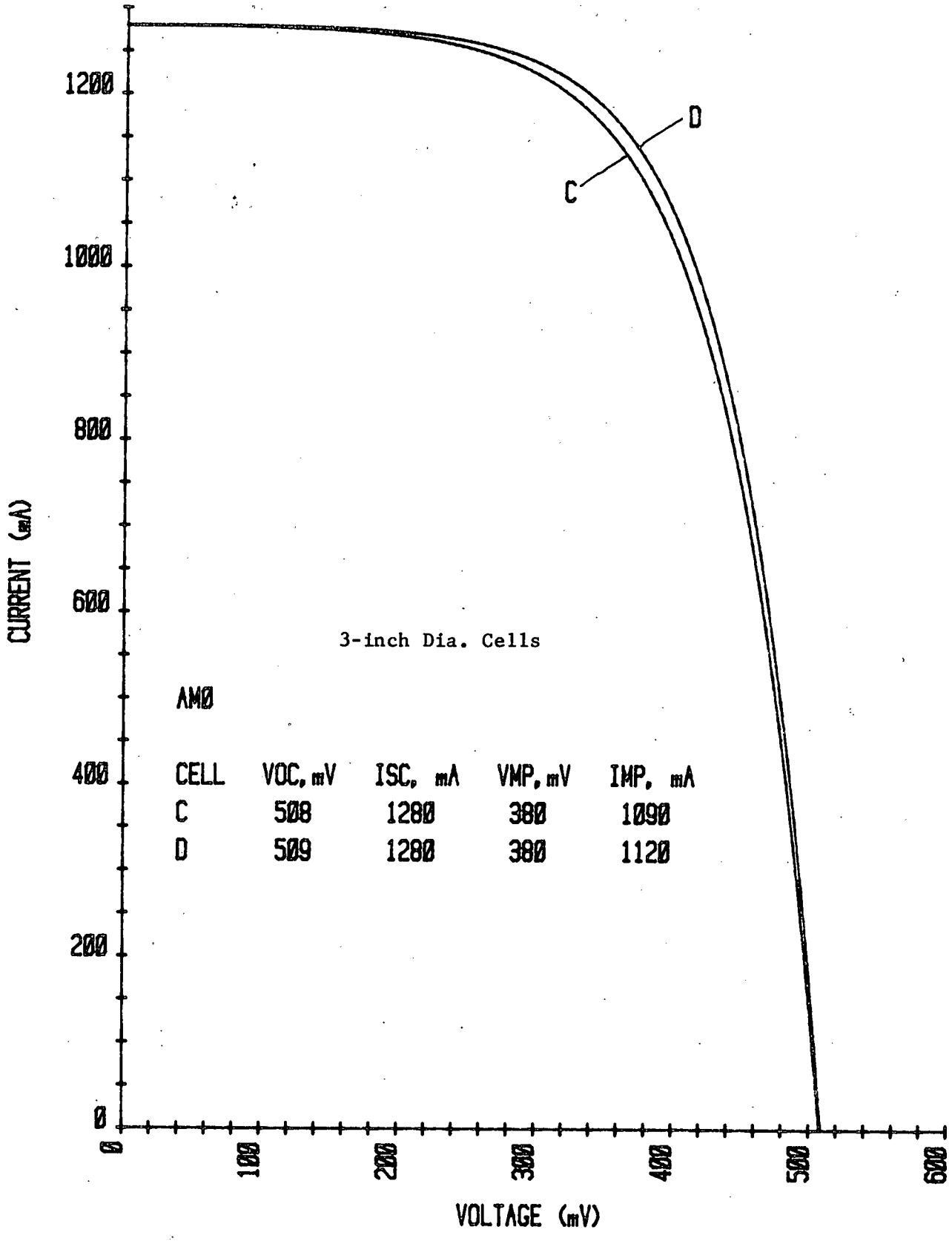


Figure 5. Output Curves for Two Baseline Cells

It became apparent that implanting through oxide was not cost effective and due to the lower practical acceleration level of the MP-400 (≈50 KeV) further use of this system was discontinued. It was in fact evident that the lower practical energy level of the Extrion 20-200 (≈25 KeV), while adequate for process verification studies, was also too high for any practical production of solar cells. To meet the goals of this program, a dedicated system of high beam current (≥10 ma) at low acceleration voltage (<10 KeV) is required. Even at the 10 KeV level there is some concern regarding the bucking drift field previously mentioned. One method considered to minimize this effect was discussed in Section 3.2.2.

As a result of the initial tests, all runs made for subsequent processing, i.e., laser anneal, screen printing, and spray-on AR coating, were made at 25 KeV (our practical minimum) and at fluence levels of 1×10^{15} to 3×10^{15}. Results of these are discussed in their respective sections.

3.3.3 Laser Annealing

In the course of this investigation, annealing work was carried out with lasers made by a variety of manufacturers. The ruby lasers evaluated were made by Korad and Apollo. Nd:YAG lasers, with and without a second harmonic generator, were made by Quanta-Ray, Quantel, Quantronix, ESI/Holobeam, and Raytheon. With the exception of the Raytheon laser, all other lasers were Q-switched with pulse duration in the 10-250 ns range. The Raytheon laser was a conventionally pulsed system with pulse durations between .6-5 msec.

In evaluating the Raytheon laser, it became apparent that this laser, with its long pulse duration and a 1064 nm wavelength, was inadequate for the required annealing work. The combination of the stated output parameters led to heating of the bulk material, with subsequent cracking of the silicon substrate from the thermally induced stresses. Similar investigations with Q-switched lasers revealed satisfactory performance, with annealing attained without substrate damage.

The Q-switched lasers evaluated can be divided into two categories.

1. Repetitively pulsed, Q-switched lasers, or those whose continuous wave emission is converted into pulses by a Q-switch. The Quantronix and ESI/Holobeam laser scribers/trimmers fall into this category.

2. Pulsed lasers, or lasers that emit light in pulses rather than continuously and where the Q-switch increases pulse power by shortening pulse duration while keeping the energy constant. Korad, Apollo, Quantel, and Quanta-Ray are manufacturers of pulsed lasers.

Category 1 lasers are of low energy and high pulse repetition rate (less than a millijoule in the KHz range); whereas, category 2 lasers evaluated were generally of high energy and low repetition rate (.1-5 joules of 2-5 pulses/minute).

When annealing with laser scribers/trimmers, the beam was defocused to provide a spot 1-5 mils in diameter. To ensure complete area coverage, a computer controlled step and repeat process was utilized with approximately a 50% to 80% overlap from spot to spot. For the high energy lasers, a computerized X-Y positioning table was not available; however, the larger diameter annealed spots created by high laser energy allowed manual repositioning of the wafer through utilization of appropriate micrometer positioning devices.

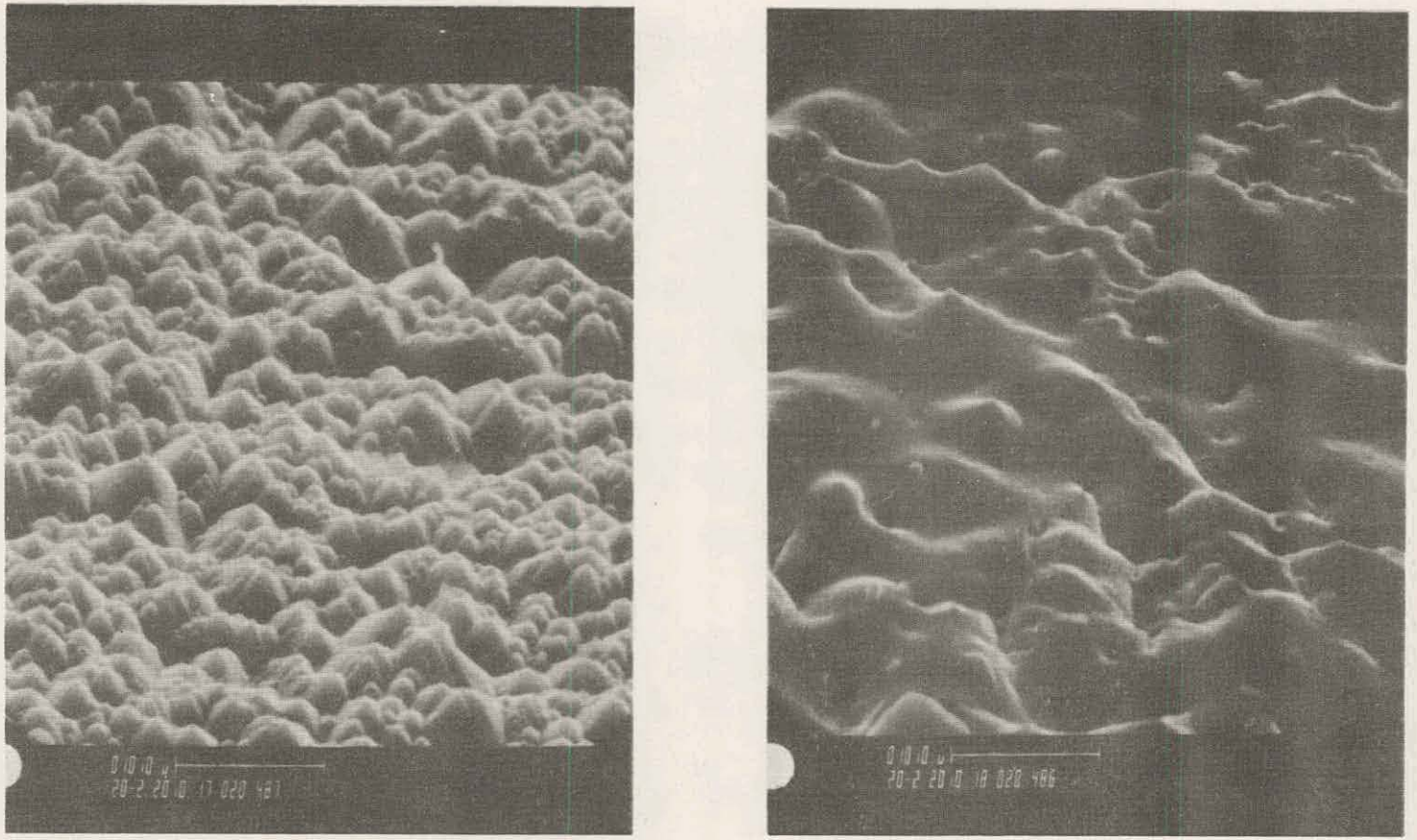
Throughout this investigation, laser annealing was performed on silicon wafers consisting of texture-etched, flash-etched, and polished specimens which were implanted at various energies (25 KeV - 125 KeV) and fluence levels (1×10^{15} ions/cm^2 - 3×10^{15} ions/cm^2). After annealing, the wafers were subjected to four point probe measurements to determine proper electrical activation. This was followed by electrical output testing at AM1 for data on cell electrical characteristics for those annealed specimens fabricated into small cells.

Consistently, I-V outputs for laser annealed texture-etched cells were extremely low. SEM analysis of cell surfaces revealed some melting of the pyramidal structure during the laser annealing operation, Figure 6. It was concluded that melting caused junction non-uniformity with subsequent cell output degradation. Attempts at resolving this problem by reducing laser pulse energy, and for some samples preheating the substrate, were unsuccessful. At settings where melting was minimized, sufficient surface activation was not attained as indicated by high sheet resistivity readings when tested with a four point probe system.

Low I-V outputs were also experienced with laser-annealed flash-etched wafers. These low outputs were expected by virtue of high sheet resistivity readings (70 Ω/sq) yielded by the tested specimens. High resistivity was attributed to low ion implantation fluence level of 1×10^{15} ions/cm^2 as compared to optimized level of 2.5×10^{15} - 3×10^{15} ions/cm^2 utilized on polished and texture-etched wafers and yielding sheet resistivities of ≤ 45 Ω/sq.

The first phase of laser annealing work on polished wafers was performed on wafers implanted at 25 KeV - 2.5×10^{15} ions/cm^2. Sample cells fabricated from the annealed wafer areas yielded an output representing 7.3% AM1 conversion efficiency, Figure 7. The cells were neither sintered nor AR coated, consequently higher conversion efficiencies would have been obtained with incorporation of these two techniques into cell processing. In terms of I_{sc} per unit area, the laser-annealed polished cells demonstrated a fairly good response. The 5ma I_{sc} for the .5 x .5 cm size cell converts to a value of 27 ma/cm^2 based on active area only, discounting the ohmic contacting and probe masking during test. This compares to a diffused junction 11% efficient cell, Figure 8, with an I_{sc} output of 32 ma/cm^2, discounting a 7% ohmic contacting masking area.

This work was followed by additional laser annealing of polished wafers implanted at 25 KeV, 3×10^{15} ions/cm^2. Annealing was carried out with a Quantronix Nd:YAG laser scriber, Korad ruby laser, and ESI/Holobeam Nd:YAG



(A) (B)

Figure 6. SEM photos (2000X/60° Tilt) of the Surface of a Texture-Etched/Ion Implanted Silicon Wafer before (A) and after Laser Annealing (B)

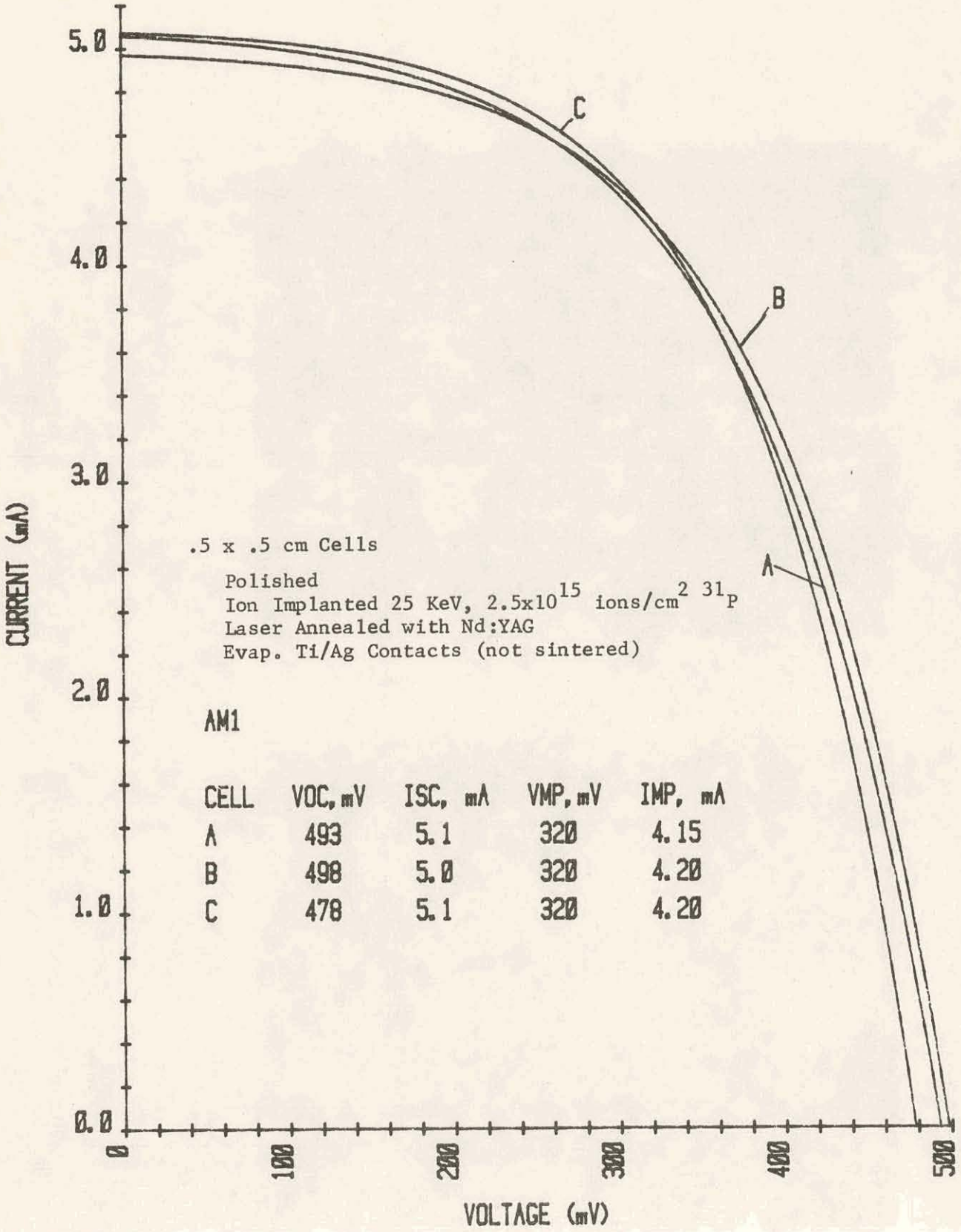


Figure 7. I-V Output for Laser Annealed Solar Cells

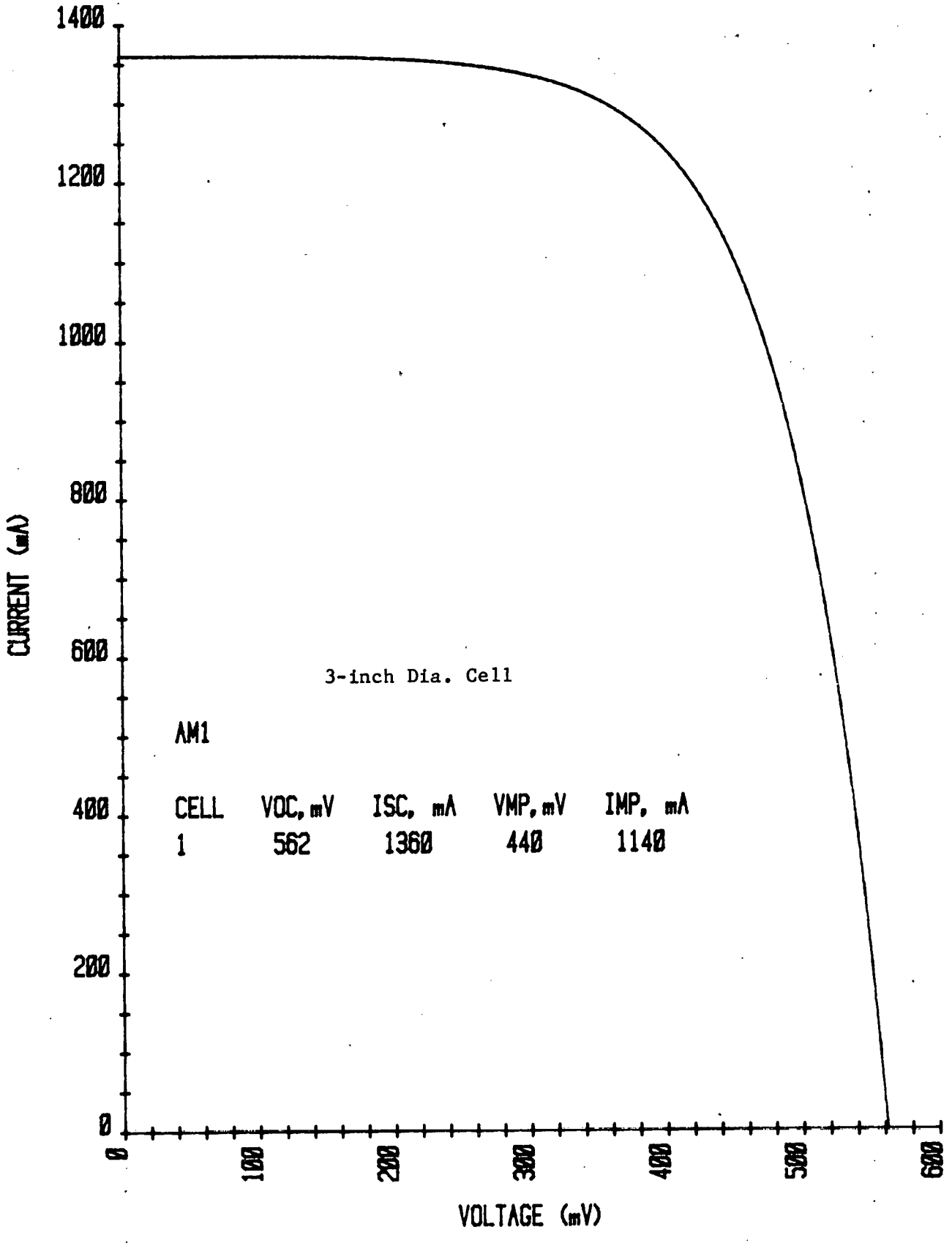


Figure 8. STD Terrestrial Cell

laser scriber and laser trimmer. The annealed regions on the wafers exhibited good sheet resistivity values - approximately 31 Ω/sq. The regions also exhibited a color change associated with good annealing.

At the onset of the second phase annealing work, the ruby laser was damaged before a large enough area on a wafer could be annealed to allow test cell fabrication. Consequently, the only cells made were annealed with Nd:YAG lasers. At this time, the cells were sintered and AR coated, subsequently yielding a conversion efficiency of up to 13.25% or 14.73% in terms of active area only for a 2 x 4 cm cell. With optimization of laser annealing parameters, this efficiency could be pushed above 16%.

Somewhat lower conversion efficiencies were obtained with the two 3-inch diameter cells - 10.4% and 10.7%. It was felt that the lower output was partially due to our I-V test set up where the required test fixtures for these 3-inch diameter cells were inadequate.

In addition, the cells suffered from a fairly large ohmic contact area which substantially reduced the active area of the cell with subsequent reduction in cell output. In terms of the active area, the efficiency of the two cells converts to approximately 12%. Obviously, higher output is anticipated with utilization of proper fixtures for cell electrical testing. Table 2 and Figures 9 through 13 summarize the results of this effort.

To study impurity redistribution following laser and furnace annealing, a number of specimes were subjected to SIMS (Secondary Ion Mass Spectrometry) analysis. SIMS analysis was performed utilizing an ARL (Applied Research Laboratories) ion microprobe mass analyzer (IMMA) interfaced to a PDP-11 computer. Figures 14 through 16 show the depth profiles obtained from this evaluation.

The sharp peak in Figure 14 is typical for an ion implanted sample (25 KeV, 3.0×10^{15} ions/cm^2). The broader profiles indicate phosphorus redistribu-

TABLE 2

SUMMARY OF LASER ANNEALING WORK

Cell Size (cm)	Wafer Surface	Implantation Parameters	Laser Anneal Energy Density (J/cm^2)	Pulse Duration/ Pulse Rep Rate	Annealed Spot Diam (mils)	Center-Center Spacing (mils)	Sheet Resistivity (Ω/sq)	Laser Type	Cell Conversion Efficiency (%)	Typical Fill Factor (%)	Cell Conversion Efficiency In Terms of Active Area (%)
1x1	Flash Etched	25 KeV $1x10^{15}/cm^2$	4.9	140 nsec 4 KHz	2.9	1.0	70	Quantronix Nd:YAG Scriber	Low	-	-
1x1	Texture Etched	25 KeV $3x10^{15}/cm^2$	2.9	140 nsec 4 KHz	4.3	2.0	41	Quantronix Nd:YAG Scriber	Low	-	-
.5x.5	Polished	25 KeV $2.5x10^{15}/cm^2$	3.4	140 nsec 4 KHz	4.0	1.5	38	Quantronix Nd:YAG Scriber	7.3	-	-
1x2	Polished	25 KeV $3x10^{15}/cm^2$	4.7	95 nsec 4 KHz	5.0	1.5	31-35	Quantronix Nd:YAG Scriber	10.88-12.91	76	12.1-14.35
2x4									11.71-13.25	74	13.0-14.73
3" diam									10.4/10.7	66	11.85-12.13
1x2	Polished	25 KeV $3x10^{15}/cm^2$	3.7	100 nsec 5 KHz	5.0	0.9	45	Quantronix Nd:YAG Scriber	11.88-12.58	75	13.2-14.0
1x1.7	Polished	25 KeV 3x10 /cm	8.6	115 nsec 1 KHz	1.0	.5	31	ESI/ Holobeam Nd:YAG Scriber	10.1	76	11.2
1x1.9									11.2		12.43

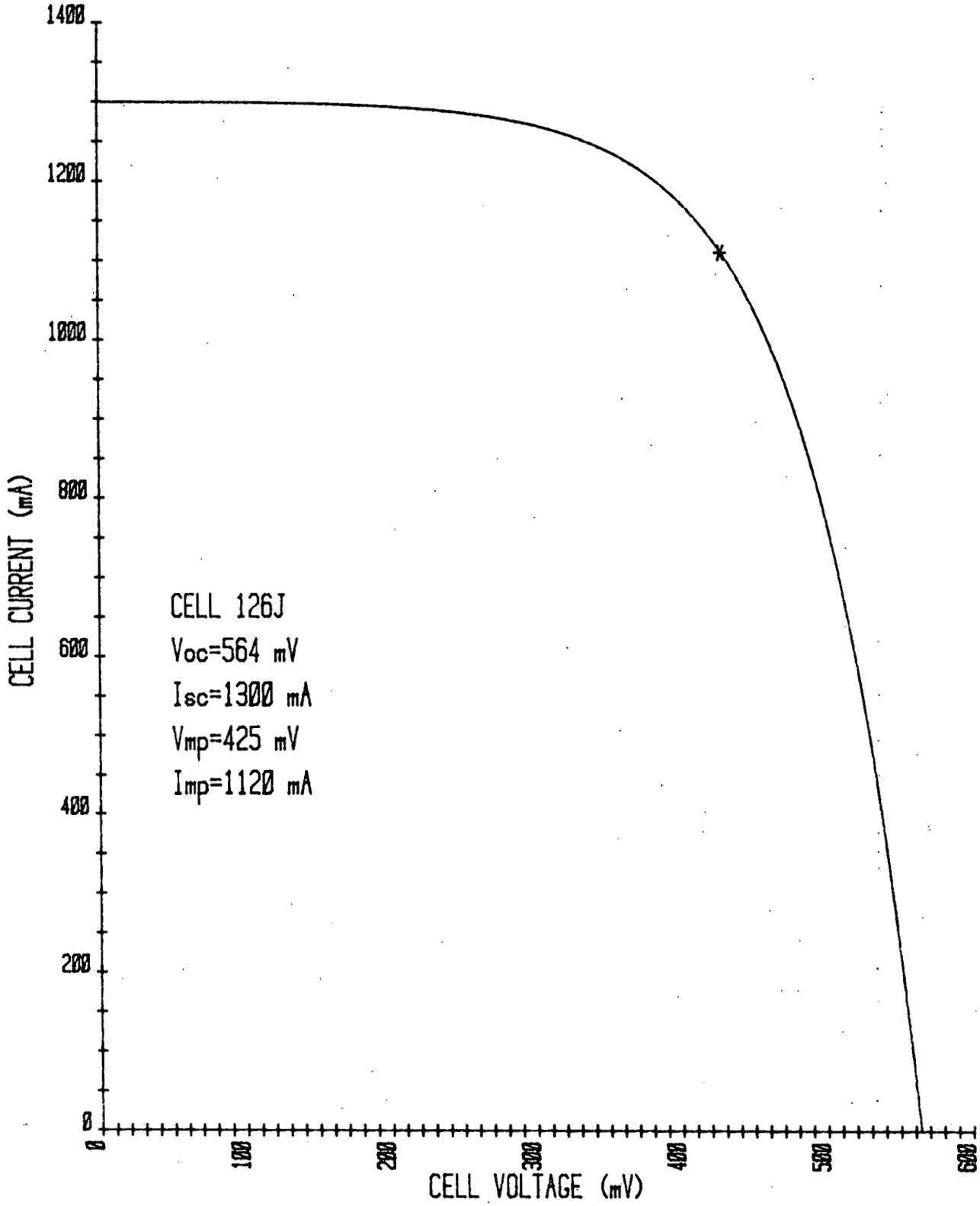


Figure 9. I-V Curve for a 3-inch Diameter Solar Cell Annealed with a Quantronix Nd:YAG Laser Scriber

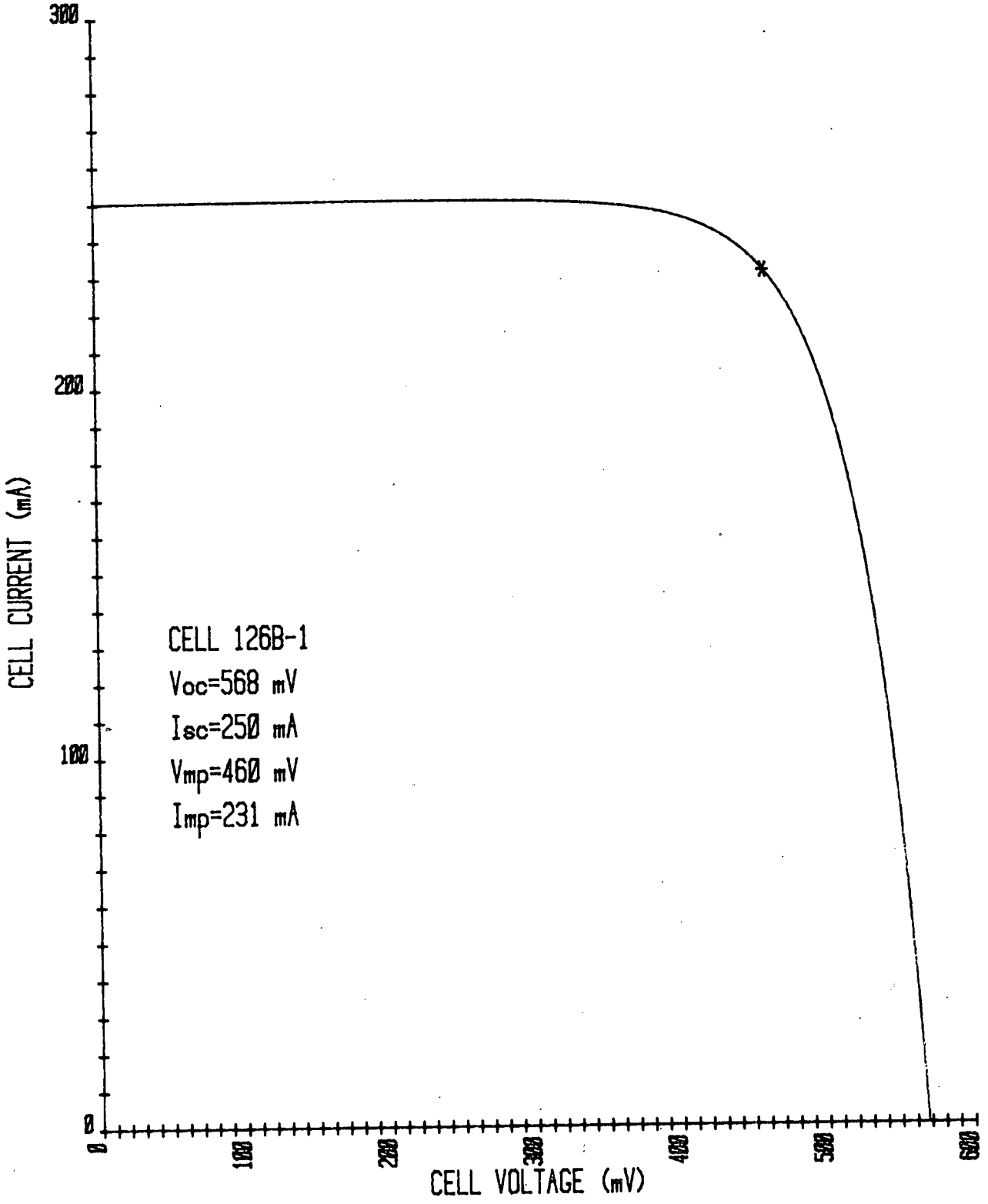


Figure 10. I-V Curve for a 2 x 4 cm Cell Annealed with a Quantronix Nd:YAG Laser Scriber

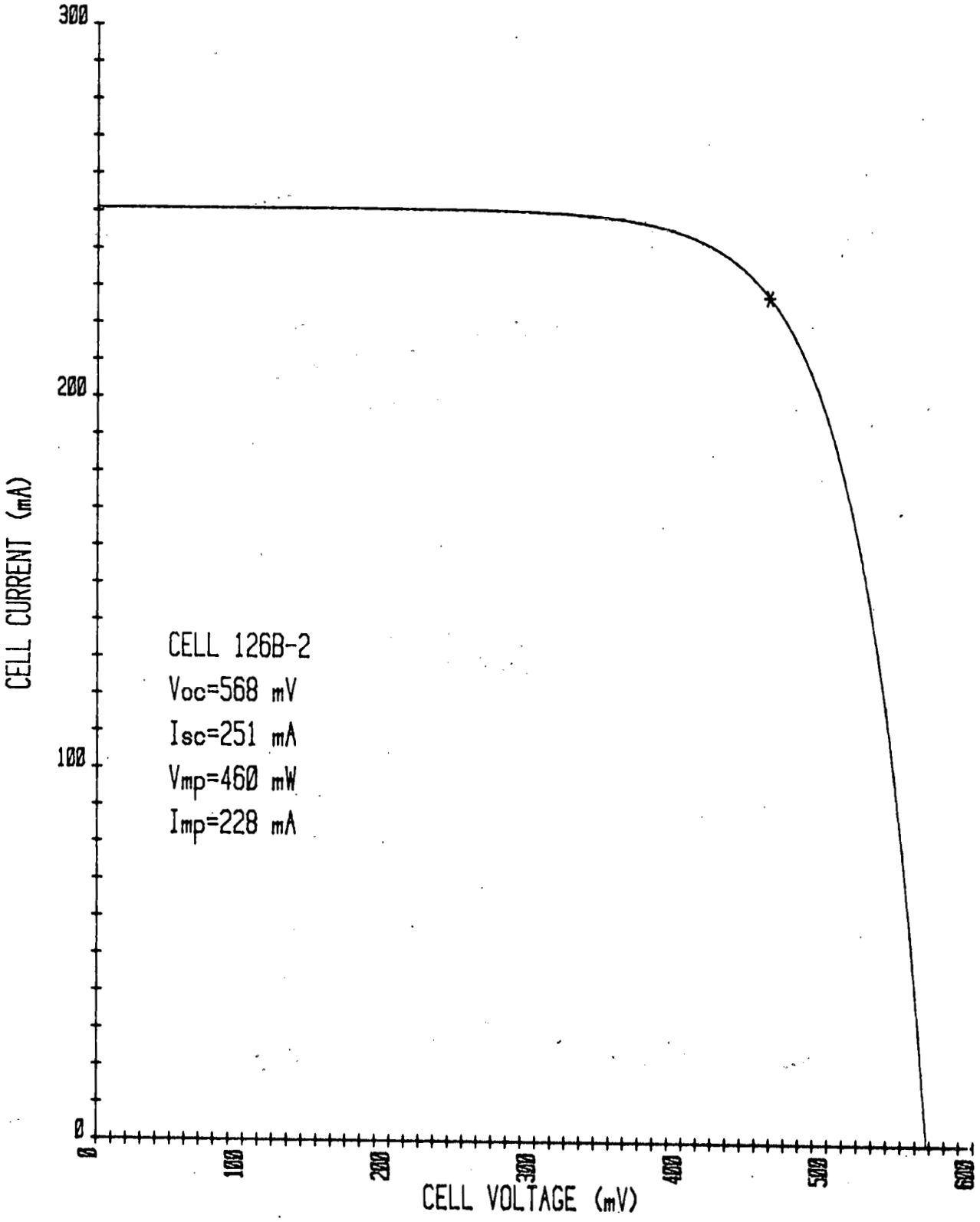


Figure 11. I-V Curve for a 2 x 4 cm Cell Annealed with a Quantronix Nd:YAG Laser Scriber

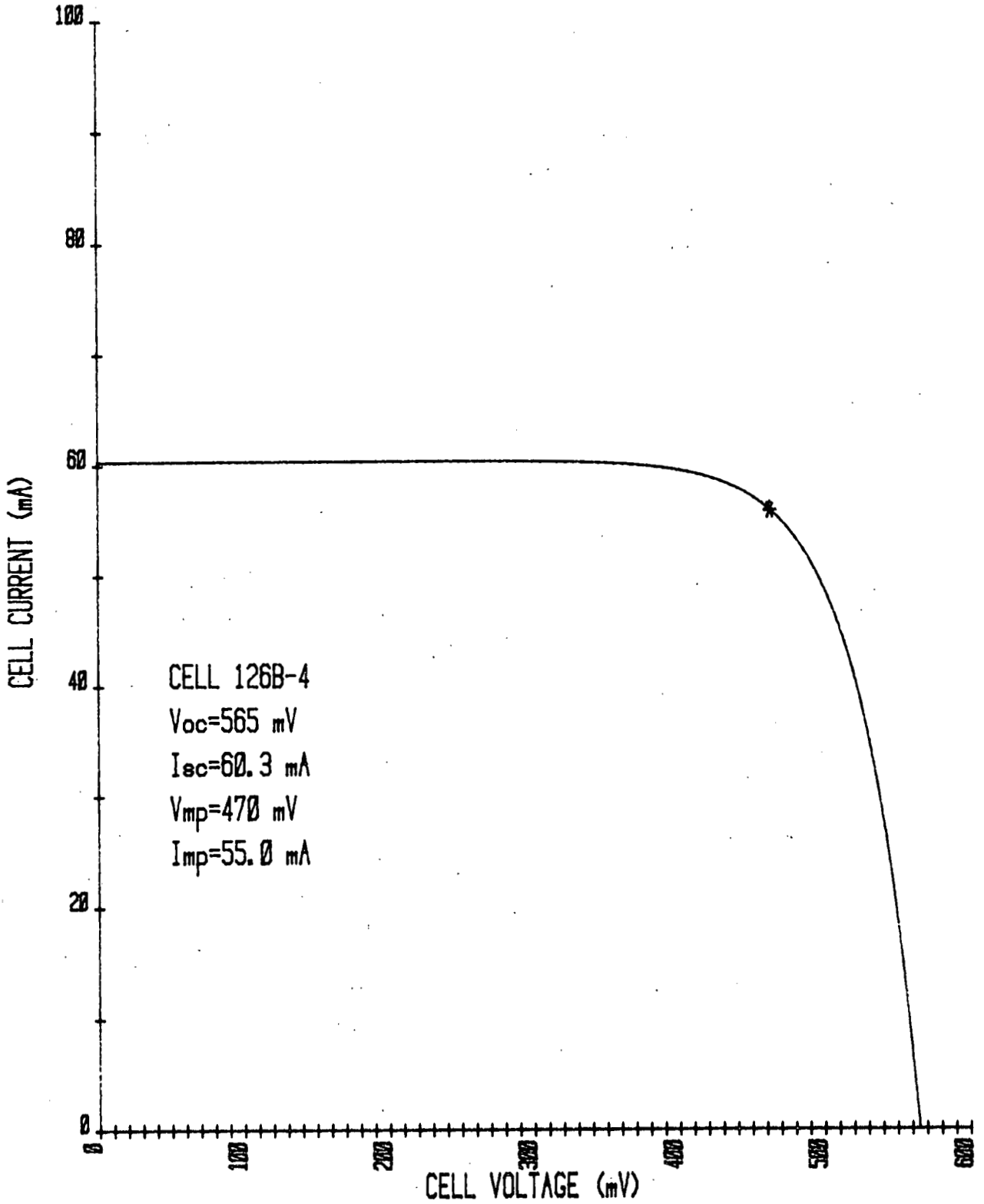


Figure 12. I-V Curve for a 1 x 2 cm Cell Annealed with a Quantronix Nd:YAG Laser Scriber

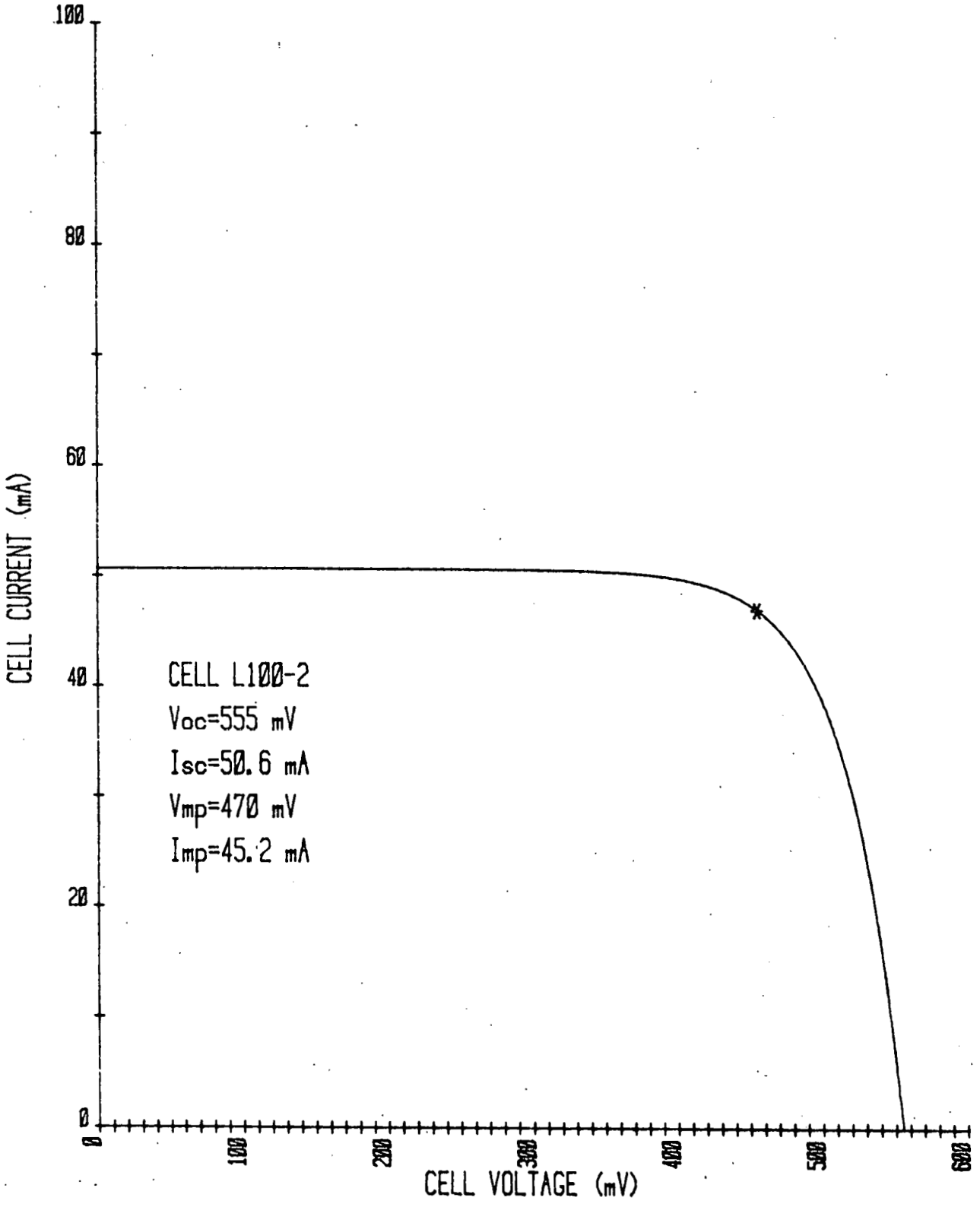


Figure 13. I-V Curve for a 1 x 1.9 cm Cell Annealed with an ESI/Holobeam Nd:YAG Laser Scriber

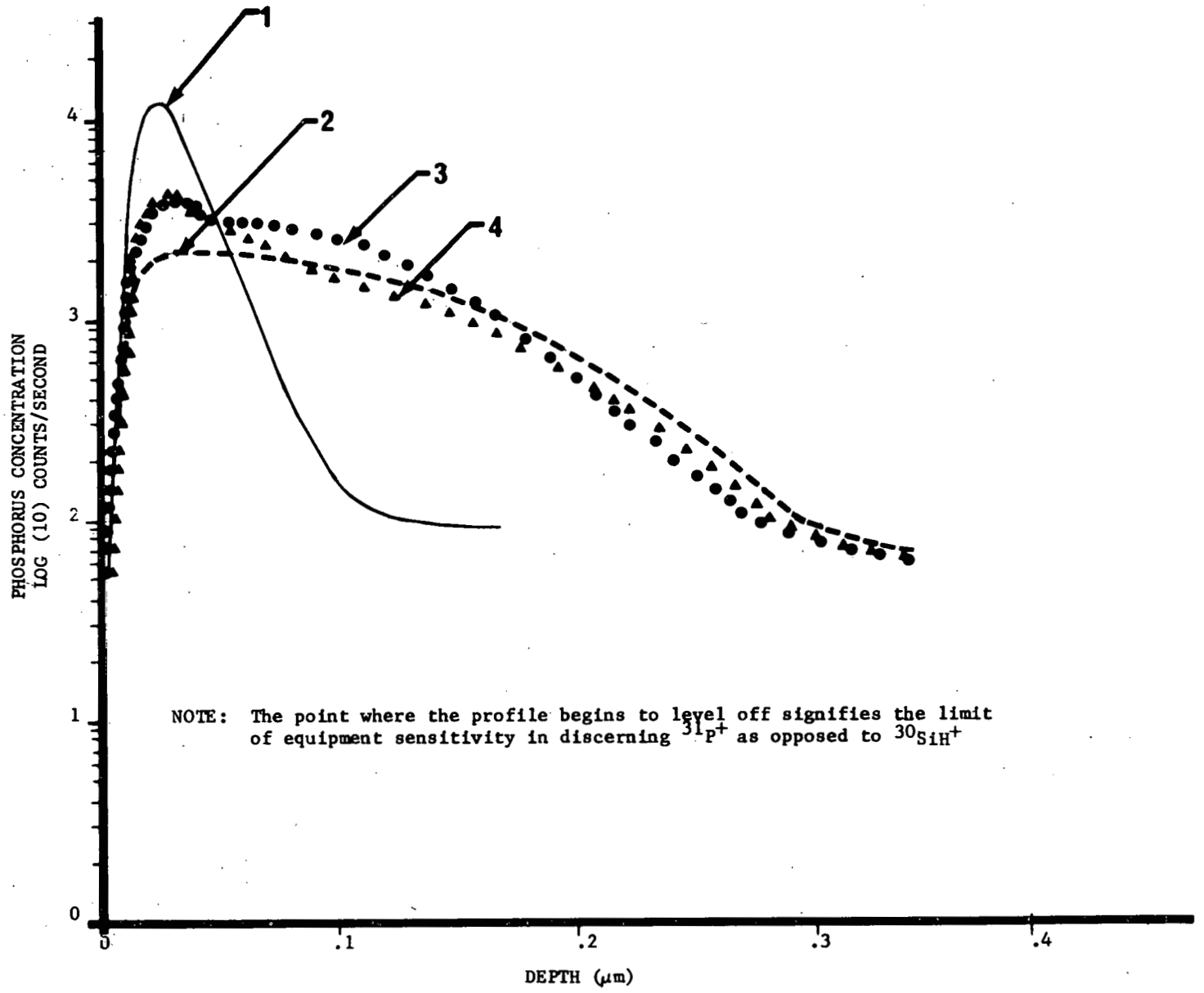


Figure 14. Profiles of the Distribution of Phosphorus Atoms in a Polished Silicon Wafer

(1) —— As Implanted 3 x 10^{15} ions/cm^2, 25 KeV
(2) ▬▬ Ruby Laser Annealed - Korad
(3) ●● Nd:YAG Laser Annealed - Quantronix
(4) ▲▲ Nd:YAG Laser Annealed - Holobeam

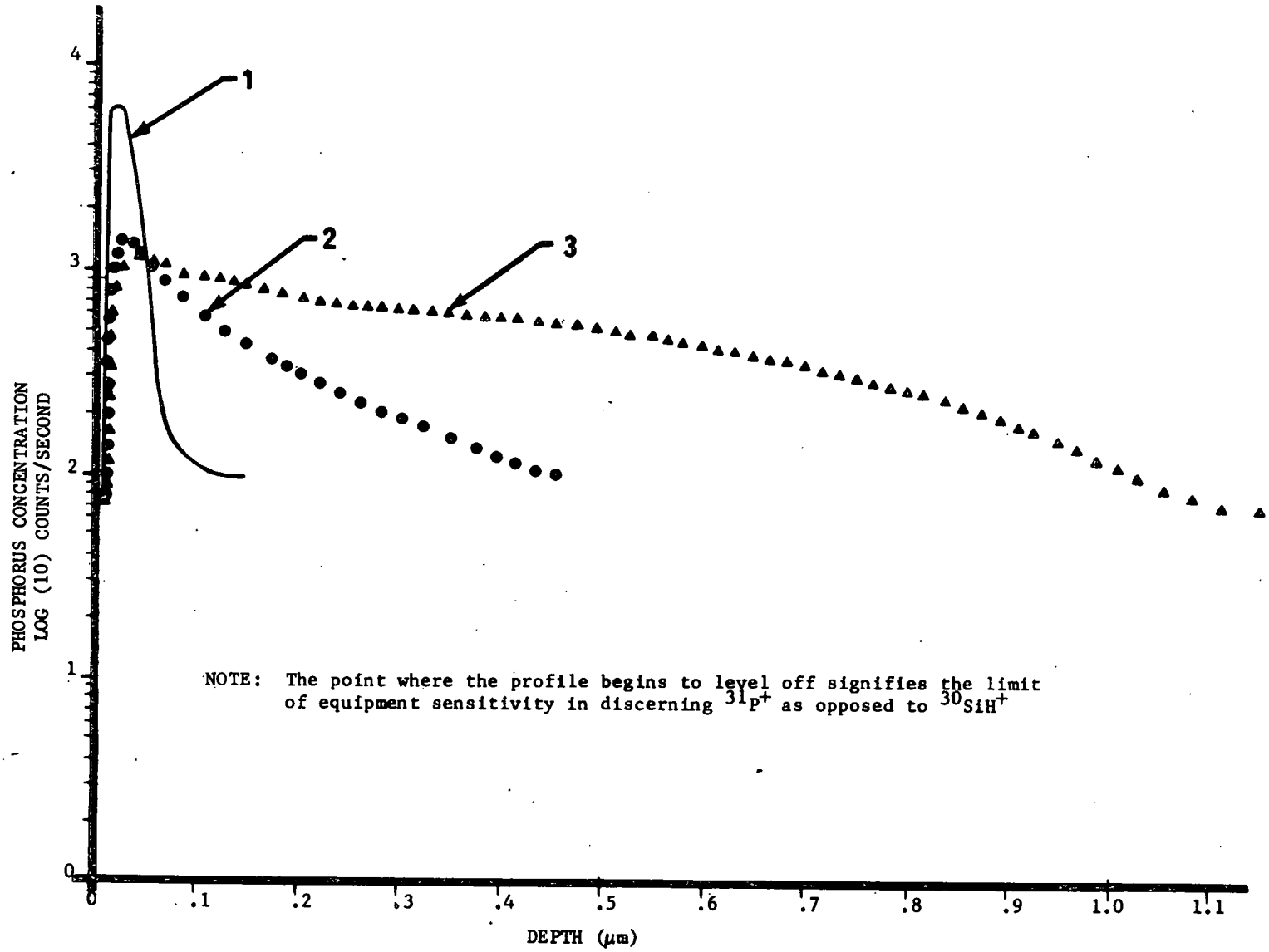


Figure 15. Profiles of the Distribution of Phosphorus Atoms in a Flash-Etched Silicon Wafer

(1) — As Implanted, 2.5 x 10^{15} ions/cm^2, 10 KeV
(2) ●● Furnace Annealed - 900°C/50 minutes
(3) ▲▲ Laser Annealed - Holobeam Nd:YAG

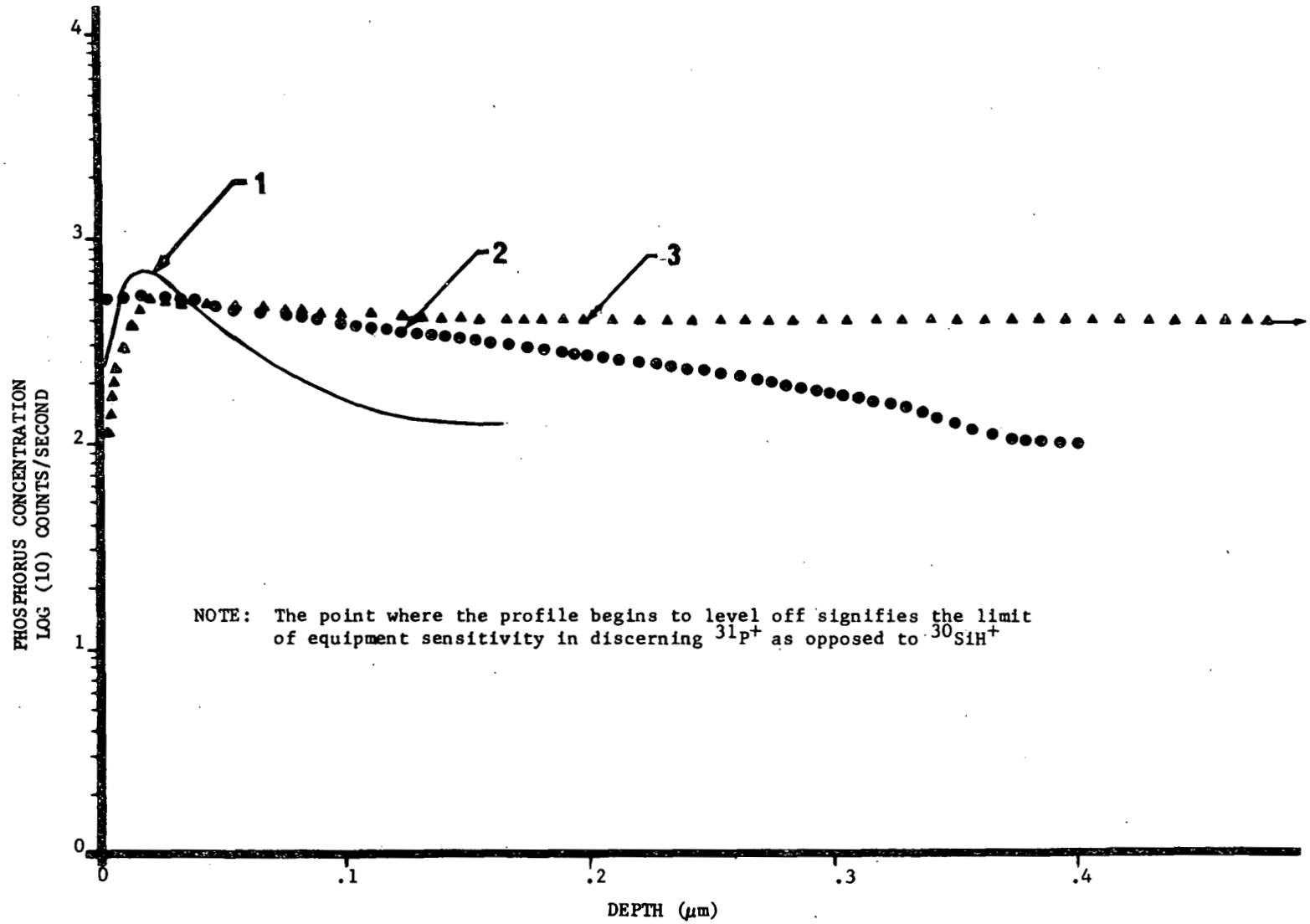


Figure 16. Profiles of the Distribution of Phosphorus Atoms in a Texture-Etched Silicon Wafer

(1) — As Implanted, 3.0 x 10^{15} ions/cm^2, 10 KeV
(2) ●● Furnace Annealed - 900°C/50 minutes
(3) ▲▲ Laser Annealed - Holobeam Nd:YAG

tion brought about by laser annealing. All four profiles were for phosphorus implants into a polished silicon wafer.

The three laser annealed profiles reflect impurity redistribution associated with annealing with various lasers. Profile 2 appears to be ideal, being the closest to a flat top distribution. This profile was attained through annealing with a Korad ruby laser with pulse duration of approximately 20 nsec. Profiles 3 and 4 were obtained through annealing with Quantronix and ESI/ Holobeam Nd:YAG laser systems, respectively. A number of mechanisms were responsible for the fact that impurity redistribution profile with the Nd:YAG lasers was not as flat as with the ruby laser. The 1064 nm wavelength of the YAG lasers exhibits deeper penetration into the silicon with subsequent lower temperatures in implanted surface layers. This condition leads to a slower and shallower progression of the melt front and consequently of the impurity atoms as indicated by the higher impurity peaks near the surface of the Nd:YAG-annealed samples as compared to ruby-annealed samples.

For all three samples, the impurities diffuse to a depth of about .3 μm. For the Nd:YAG lasers, this is accomplished by higher energy densities and utilizing long pulse durations (4.8 joules/cm^2, 95 nsec for Quantronix and 8.6 joules/cm^2, 115 nsec for Holobeam). Also, since step and repeat process with an overlap is utilized, some regions on the wafer are exposed to the laser pulse several times resulting in additional movement of the impurities.

It was previously reported[2,4] that following laser annealing, the impurity concentration in the near surface region, as revealed by SIMS analysis, was substantially increased. This phenomenon was not consistently observed in our tested samples. It is important to note that some instability in the sputtering action of the primary beam of the IMMA for up to the first 200Å on some samples was observed, i.e., instability occurred until

a crater of sufficient depth was created to stabilize the primary beam. This renders the profile depth distribution data near the surface as somewhat questionable. The instability can be eliminated with adequate preparation of the samples, such as deposition of a thin layer of gold on the surface. Beam instability would then be restricted to the gold layer consequently yielding an improved phosphorus profile. It is recommended that additional evaluations be carried out in this area.

Figure 15 shows the impurity profiles for flash-etched wafers. The implanted wafers were supplied by JPL to LMSC. The wafers were implanted at 10 KeV, 2.5×10^{15} ions/cm^2, 10° tilt. Profile 1 is as implanted, whereas Profiles 2 and 3 are furnace and laser annealed, respectively. Furnace annealing was carried out at 900°C for 50 minutes. Considerable impurity movement is evident on the furnace annealed sample. However, the distribution is such that a fairly sharp peak is still maintained with a rapid impurity concentration drop through a depth of approximately .4 μm. The laser annealed samples were again annealed with an ESI/Holobeam laser system. In annealing the samples, the prime requirement was providing JPL with 12 laser-annealed 3-inch diameter wafers. To expedite this job within the time that the subject lasers were available, anneal laser settings had to be modified from what was considered optimum in order to attain wafer annealing within a reasonable time period. To do this, pulse repetition rate was increased from 1 KHz to 12 KHz, and power output of the laser was increased correspondingly until annealing was achieved. Increase in the above mentioned parameters also caused an increase in pulse duration to 250 nsec. This is not an optional selection but rather one that automatically occurs with changes in power and frequency for laser scribers/trimmers. Pulse duration increase also required an increase in energy density from approximately 8.6 joules/cm^2 to 17 joules/cm^2. It was not anticipated at the time the changes were made that these changes would have a profound effect on the impurity profile. In fact, as later realized, the high energy density/high duration pulses coupled to multiple activation of the same area caused creation of a very deep junction - approximately 1.1 μm, as indicated by Profile 3. This condition is obviously not desirable and

consequently an appreciable decrease in efficiency can be expected out of the cells made from these wafers.

The backside of the JPL supplied wafers were boron implanted at 25 KeV, 5×10^{15} ions/cm^2. This was followed by furnace annealing at:

550°C - 2 hours N_2 atmosphere
850°C - 15 minutes
550°C - 2 hours

It is our opinion that the performance of cells made from the subject wafers may be compromised in view of bulk silicon dislocations introduced by the above furnace annealing temperatures. Dislocations will be removed in the implanted layer through laser annealing; however, in the bulk material, the dislocations will remain. As previously discussed, this leads to decrease in the minority carrier lifetime with subsequent decrease in cell efficiency. The laser annealed wafers have been delivered to JPL for subsequent fabrication into solar cells followed by required electrical testing.

Figure 16 shows impurity profiles for texture-etched cells implanted at 25 KeV, 3×10^{15} ions/cm^2. The as-implanted peak is lower than what has been observed for polished and flash-etched wafers. This is understandable in view of considerable increase in active surface area in a textured cell brought about by the pyramidal surface structure. This considerably lowers the effective impurity concentration density which is reflected in Profile 1. Profiles 2 and 3 are furnace annealed and laser annealed with parameters identical to those utilized for flash-etched wafers. Again, an extremely broad distribution was obtained for Profile 3, the laser-annealed sample. The profile was obtained to a depth of approximately .5 μm since time did not allow pursuing this to its full depth which is probably similar to the flash-etched sample. The furnace-annealed sample is also similar to the one obtained for flash-etched wafers, except it lacks the high peak due to lower impurity concentration density in the texture-etched surface.

The margin of error in all of the profiles becomes greater as the distance from the peak center point increases. The level where the $^{31}P+$ profile appears to reach a stable minimum is probably brought about by contributions from $^{30}SiH^{+}$. The presence of this constitutes a limiting factor in the equipment detection sensitivity. Nevertheless, generated profiles are indicative of effects that annealing has on implanted wafers.

3.3.4 Screen Printed Contacts

A Precision Systems Company, Model 150, semi-automatic screen printer was used in conjunction with 325 mesh stainless steel screens to deposit silver and silver/Al or silver/B conductive pastes. Two front grid and three back contact pastes were evaluated for screen printing and firing. They were DuPont 7095 silver for front and 7095 + 2% aluminum and 4021 (Ag+B) for the back and Owens-Illinois 6105 (silver and phosphorus) for front and 6109 (silver and aluminum) for the back.

All pastes screened adequately and no problems were encountered in screening the .005-inch conductors in the grid design using our standard screening processes. Further verification of this process technique for depositing conductors is not considered necessary, since adequate equipment is now available to meet the program goals. Such reservations as exist, concern only the composition of the pastes, their cost and the proper firing schedule for such pastes as are eventually selected. These reservations are delineated in the following firing discussion.

Some time has been expended in an effort to compare firing techniques of screened-on contacts. Belt furnace firing using presently available equipment was considered to be a cost effective technique easily automated, if practical. This technique was compared to diffusion tube firing. Titanium silver (Ti-Ag) evaporated contacts were used as a control.

1. Control cells - For control purposes, cells similarly processed as those for the screen printed ohmic contact evaluation were used except that the contacts were formed by vacuum evaporation of Ti-Ag. Wafer surfaces were flash-etched with junctions formed by $POCL_3$ diffusion. Ti-Ag contacts were deposited using standard positive photoresist and evaporation techniques. The Ti was evaporated to a thickness of 200-400Å and the Ag then deposited to a thickness of 1000Å without breaking vacuum and sintered. The Ag was then electroplated to a thickness of ≈ 10,000Å to assure adequate current carrying capacity.

2. Belt furnace firing - A BTU Engineering, Model VIQ-41-4-36 CRD-41, four-zone, digital control belt furnace was used for this test. Test cells were screened the same for both belt and diffusion tube firing. Fronts and backs were fired both separately and together. A typical profile is shown in Figure 17. Due to the limited nature of this investigation, no final conclusions will be drawn, although it is apparent that within the scope of this investigation, belt furnace firing is not adequate for the pastes evaluated. It is recommended that if further investigation is contemplated, equipment modification (or new equipment) including a high speed belt ≈ 20 inches/minute and a quartz furnace liner be considered.

3. Diffusion tube firing - A Thermco Brute, four-inch, digital controlled furnace was used for this test. Initial results using data published in other reports (45 seconds @ 950°C) resulted in generally poor results due to firing schedule or paste problems or perhaps both. Through consultation and cooperation with Spectro-Lab, who had reported good results with diffusion tube firing, the time and temperature was modified to 20 seconds @ 690°C with improved results. Again, due to the limited scope of this investigation, these improved results have not been further pursued nor optimized since they were deemed adequate for producing cells for subsequent AR-coating tests. It should be pointed out that a new lot of silver paste of the same type (7095) first used was utilized in the latter tests.

None of the pastes performed satisfactorily, although the 6105/6109 combination when fired according to the manufacturer's schedule gave consistently better results than the 7095 (7095+Al) or 7095/4021 combination.

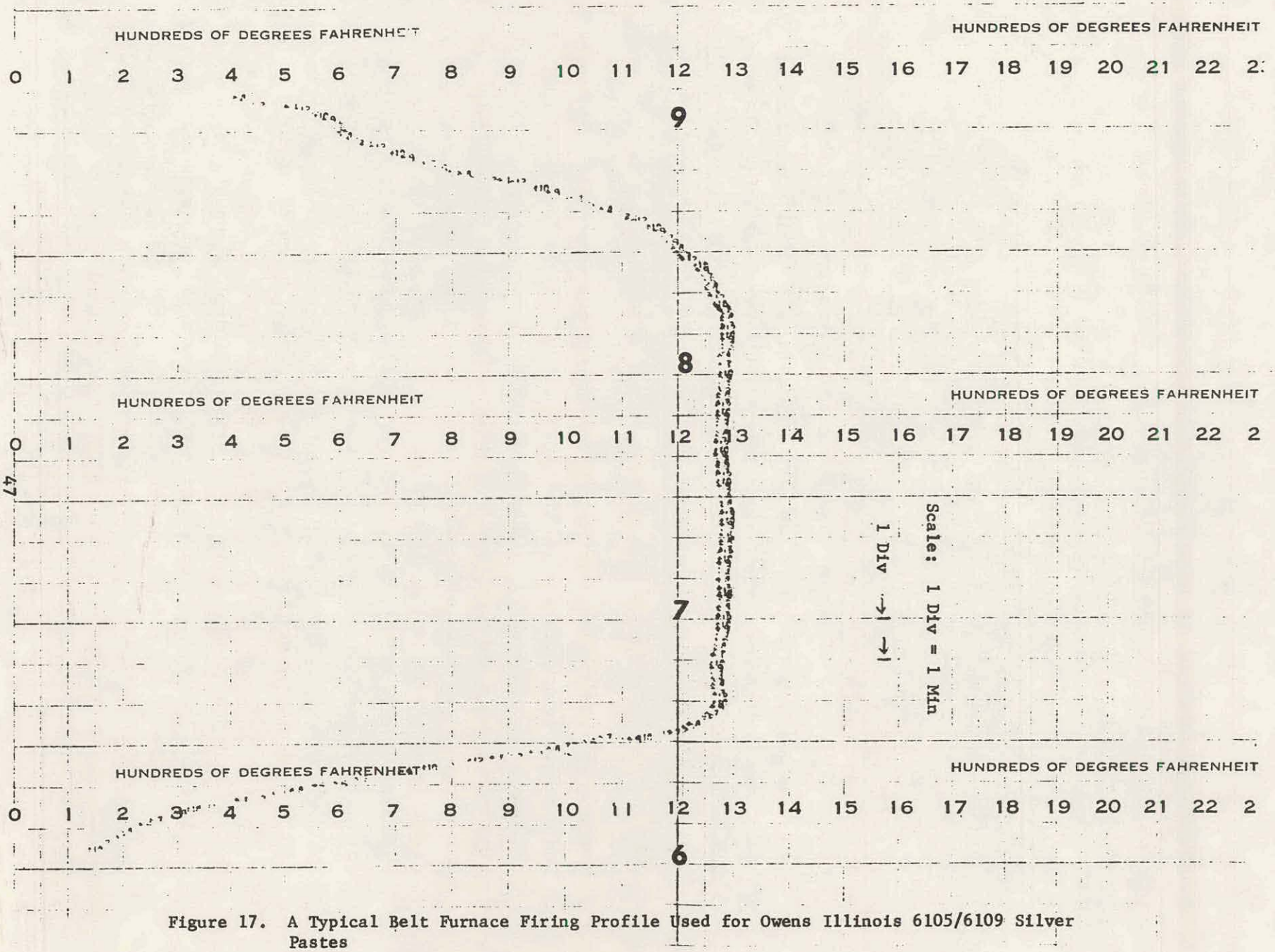


Figure 17. A Typical Belt Furnace Firing Profile Used for Owens Illinois 6105/6109 Silver Pastes

Fill factors for the 6105/6109 combination averaged 52.6, while for the 7095/7095+Al, the average was only 26.8. This compares to 65.7 for the control standard.

It is obvious from these results that considerable work must be done on both pastes and firing schedules before this process is satisfactory. Since the process is highly automatable and thus, has a high appeal (and probability) for meeting the goals of this PROJECT, it is recommended that this development work continue.

3.3.5 Spray-On AR Coating

Spray coating experimentation was performed using a Zicon Autocoater, Model 10000, manufactured by Zicon Corporation, Mount Vernon, New York. The spray gun is mounted overhead within the spray chamber, with the spray directed downward. The spray gun is automatically traversed, front to back, over a distance of 17" with a traverse speed variable up to approximately 20 inches/second, continuously adjustable. A work table with automatic incremental indexing moves the work relative to the spray gun a distance of 22 inches. The standard spray nozzles and vapor spreaders on this equipment as supplied by Zicon are configured to deliver a fan-shaped stream of spray on the part. Figure 18 shows a photo of the Zicon equipment used for this evaluation. There are two companion modules which are normally positioned on each side of the spray modules for in-line processing; however, since the primary objective of this effort was to check sprayability of AR coatings relative to thickness and uniformity characteristics, only the spray module was installed and utilized. From this, extrapolation into a fully automated, high volume process was made and reported in Quarterly Report No. 3.

The tantalum pentoxide coating was of primary interest for our spray process evaluation. Accordingly, two tantalum solutions were formulated and supplied by Allied Chemicals, identified as Nos. 201 and 482. The solutions are low viscosity and low solids systems. The 201 was formulated for spray-on and

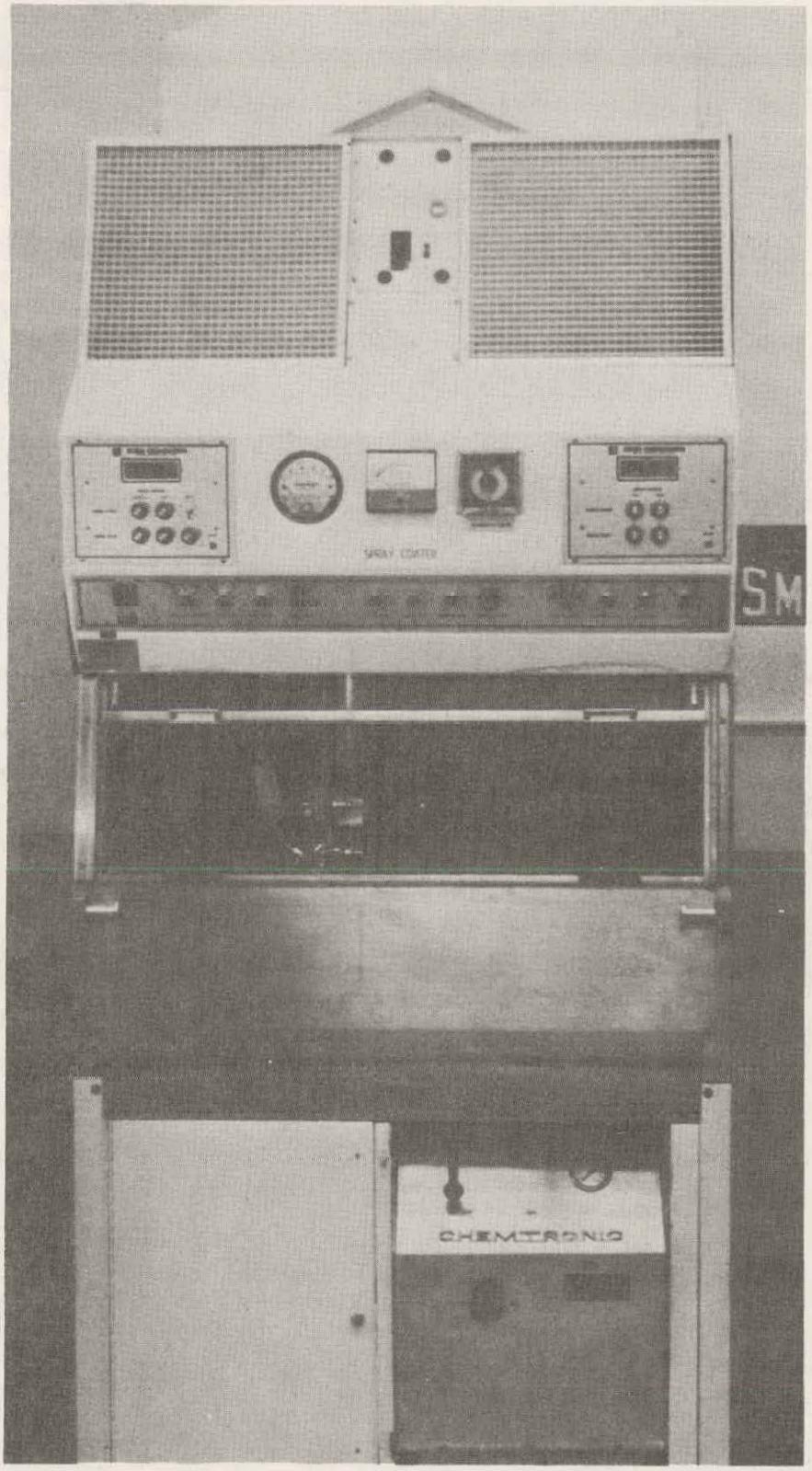


Figure 18. Zicon 10,000 Autocoater - Spray Module

and the 482 for spin-on. Measured viscosities of the solutions were 2.20 cs for the 201 and 1.96 cs for the 482, both at 24°C.

After spraying, the Ta solution is dried at 175°C for 2 to 5 minutes to drive off the solvents. Firing in an air conveyor furnace at approximately 500°C for 2 minutes at temperature converts the film to Ta_2O_5. Extent of drying/firing temperatures would be governed by trade-offs between cell performance and cost impact.

Initial spraying of the Allied Chemical Ta solutions was performed on polished wafer surfaces using the autocoater. Thickness measurements made using a Gaertner Scientific L117 Ellipsometer resulted in coatings on the 3-inch diameter wafers ranging from 500Å to 1200Å. Later work resulted in improved uniformity on a 3/4" width band of 1100Å to 1240Å on chemically-polished cells. Machine settings for these polished cells were as follows:

- o Number passes 1
- o Travel rate 22 inches/second
- o Nozzle height 4.25 inches
- o Orifice size 9 mils diameter
- o Cup pressure 2 psi, N_2
- o Nozzle pressure 40 psi, N_2

To assess the transmittance qualities of the Ta solutions, they were sprayed on micro slides using the machine settings noted above. Representative transmittance (T) and reflectance (R) curves of glass-coated specimens are shown in Figures 19 through 21. The Ta solutions were applied in the same manner as for those polished silicon wafers used for thickness measurements. A Cary 14 Spectrophotometer was used for these plots. Transmittance and reflectance values (from graphs) at a .6μ wavelength are shown as follows:

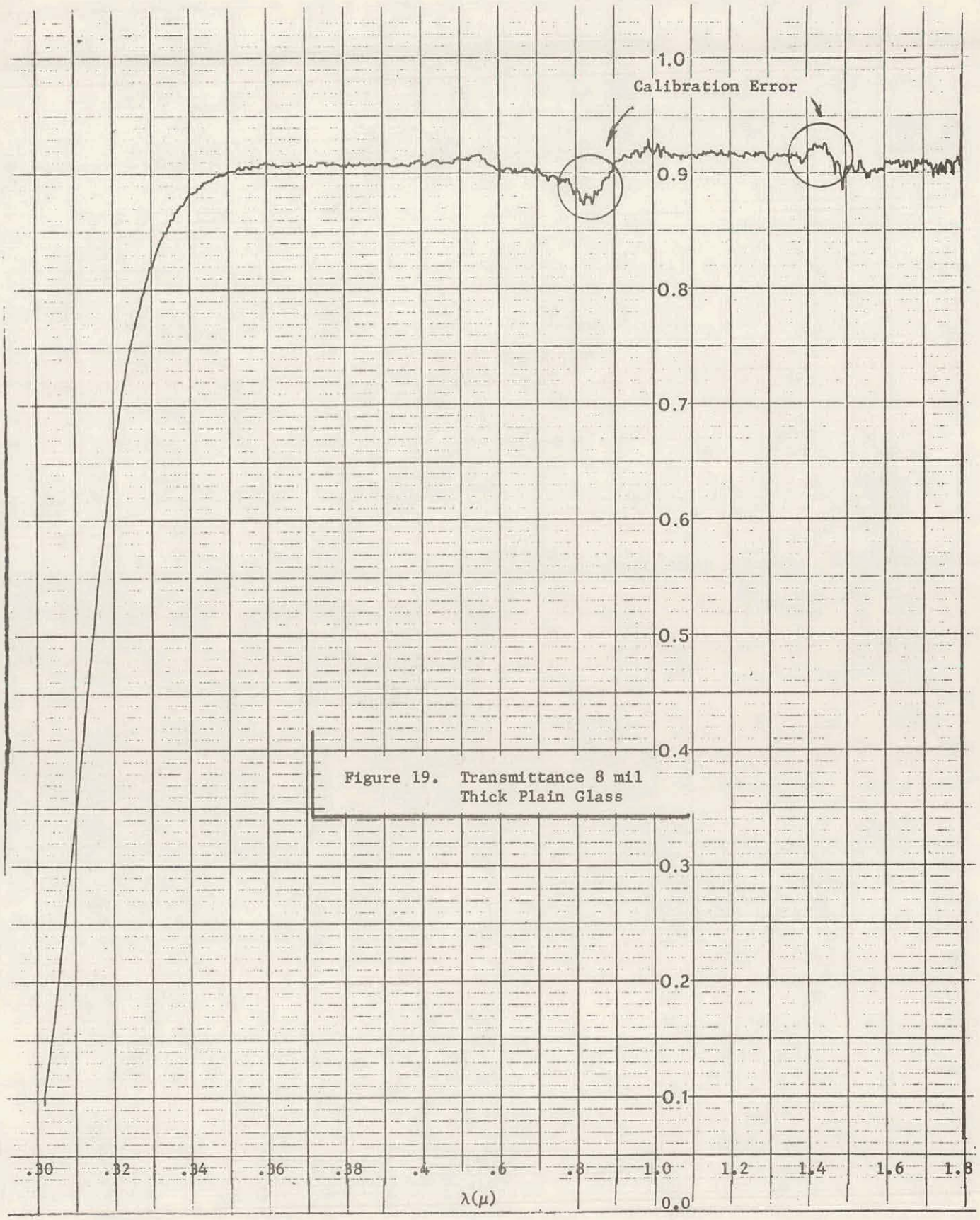


Figure 19. Transmittance 8 mil Thick Plain Glass

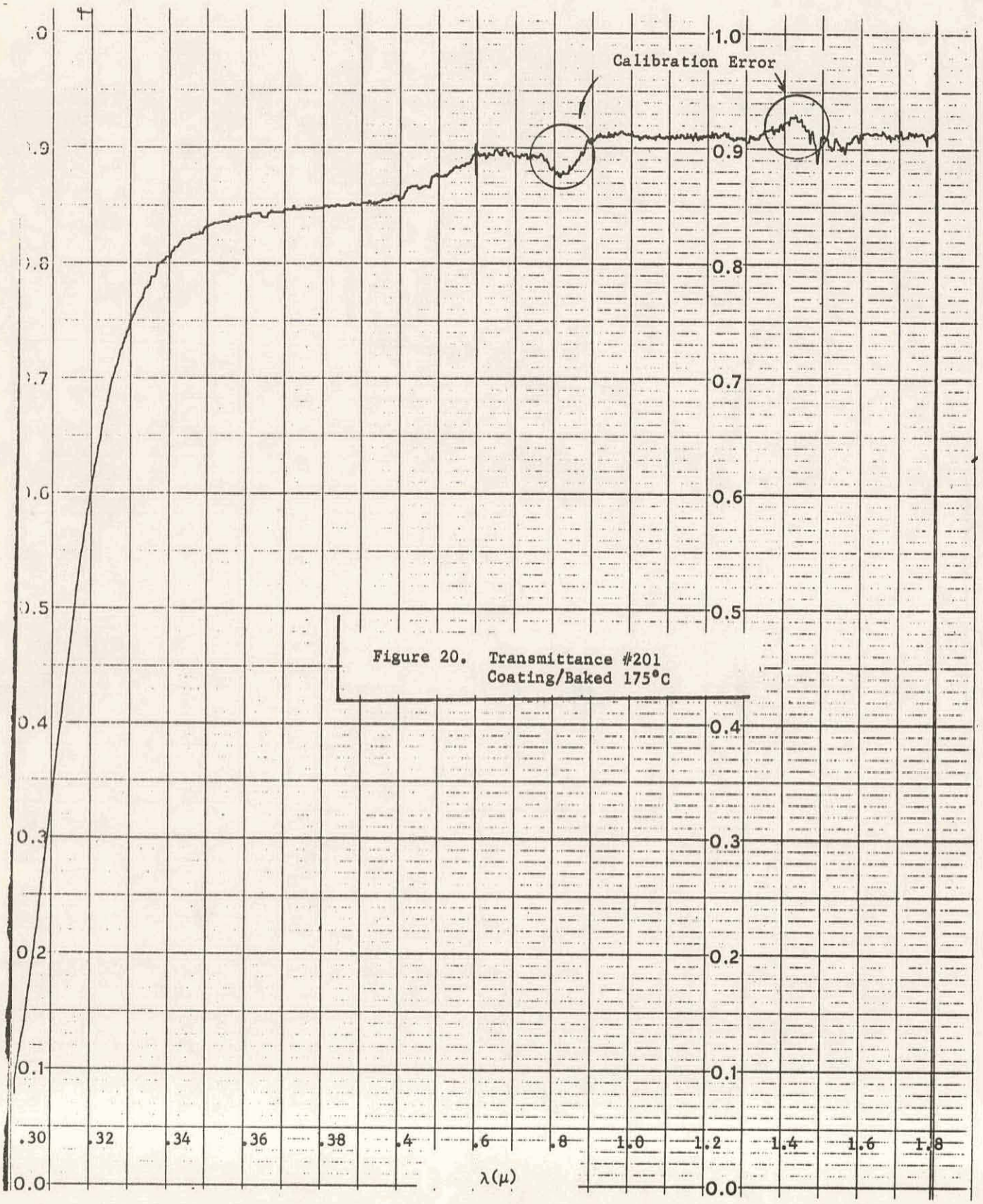


Figure 20. Transmittance #201 Coating/Baked 175°C

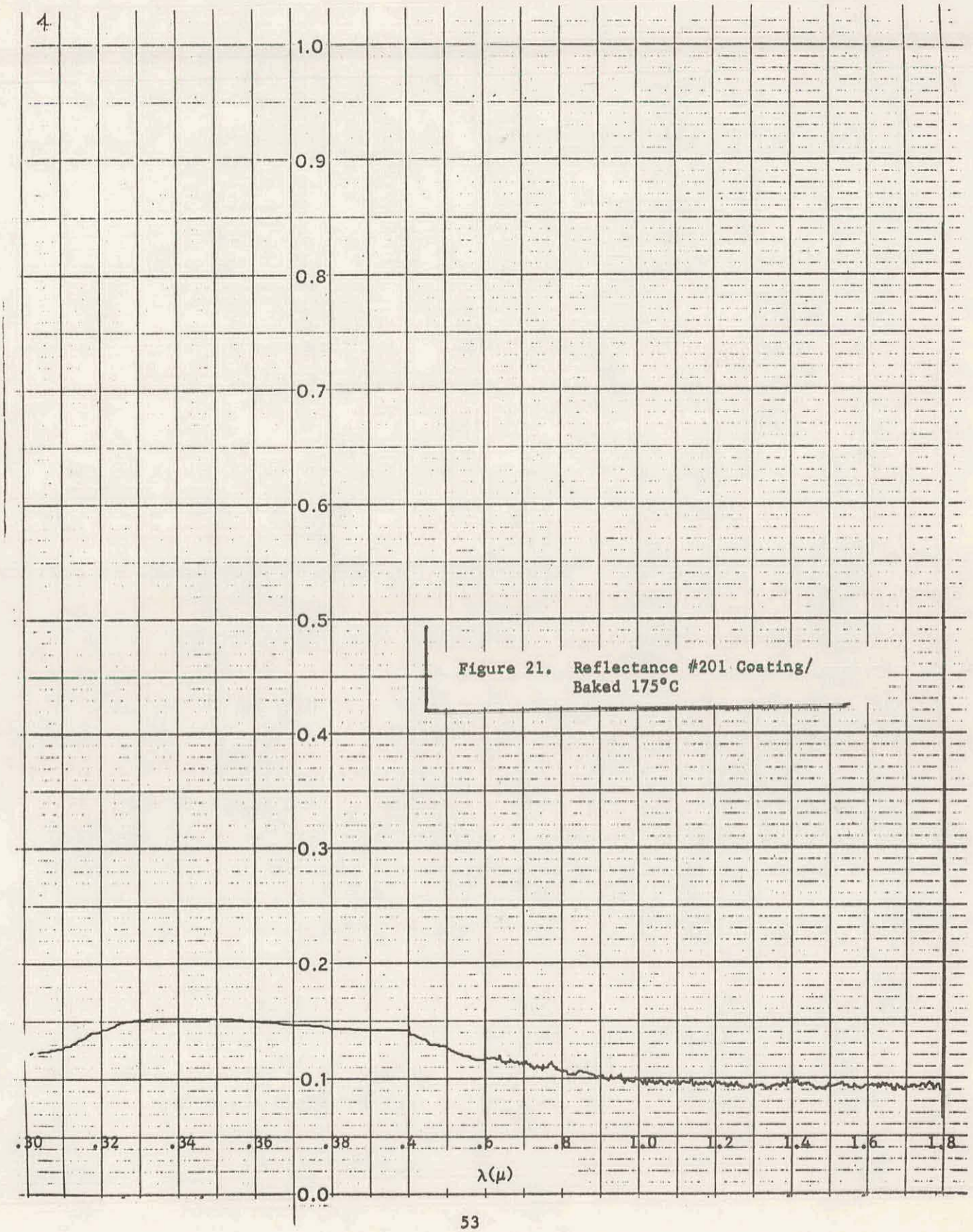


Figure 21. Reflectance #201 Coating/ Baked 175°C

Specimen	λ = .6μ	
	Transmittance	Reflectance
8 mil thick glass (ref)	90%	10%
#201, Baked 175°C	89%	11.5%
#201, Fired 500°C	84%	18%
#482, Baked 175°C	87%	19%
#482, Fired 500°C	85%	16.5%

The significance of these T and R values is that they show acceptable values with the low transmission losses after subtracting the plain glass T value.

Reflectance measurements were also made on a 2 x 4 cm chem-polished silicon cell, before and after spray coated with the 201 material. Figure 22 shows these curves. As can be seen, the reflectance at .6μ wavelength, uncoated is 32%, coated is 7%, representing a significant improvement.

Some initial experimentation was performed to determine electrical output effects of these tantalum solutions. Space cells 2 x 4 cm in size with chem-polished surfaces were used. The cells as-received have an SiO coating. Output measurements were made in the as-received condition, followed by stripping of the SiO with buffered HF, retested, coated with the tantalum solutions, and again retested. Coating with the tantalum solution was performed by both spinning and spraying. Spinning is a proven process and over this small area, good thickness uniformity was assured for comparison with the spray-on technique. Tables 3 and 4 show the results of this experimentation for spin-on and spray-on, respectively.

Reasonably good uniformity was attained on the sprayed specimens as evidenced by the light blue coloring across the cell area. The as-sprayed values as shown in Table 4 ranged from 1% to 6% lower than the as-received SiO. This could be attributable to the index of refraction differences between SiO and TaO.

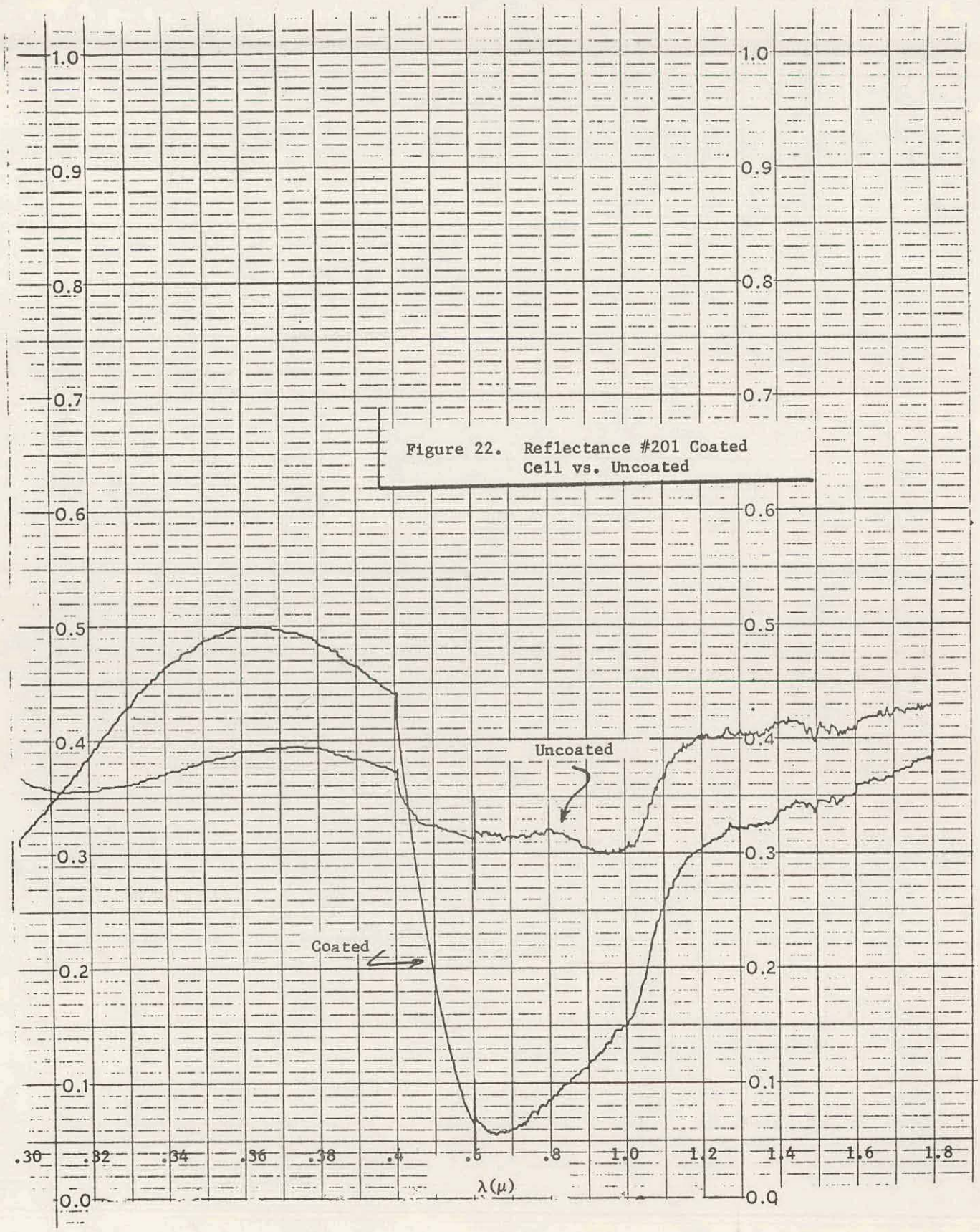


Figure 22. Reflectance #201 Coated Cell vs. Uncoated

TABLE 3

SPUN-ON Ta SOLUTIONS

Specimen: 2 x 4 cm Space Cells with SiO Coat, Chem Polished

Process Parameters: 2000 rpm/10 sec

Specimen No.	Ta Solution	Output I_{sc} (ma)		
		As Received	After SiO Strip	After Coated
AR 1	201	273	212	245
AR 2	201	267	207	265
AR 10	482	270	213	265
AR 13	482	269	199	236

TABLE 4

SPRAY-ON Ta SOLUTIONS

Specimen: 2 x 4 cm Space Cells with SiO Coat, Chem Polished

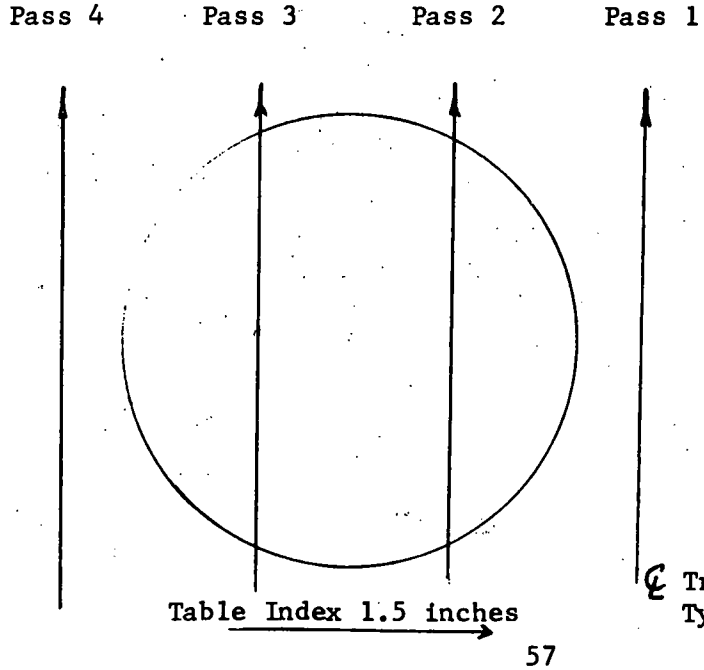
Process Parameters: Zicon Autocoater, 1 pass, 22 inches/second travel, 4.25 inches nozzle Ht, 9 mil orifice, 2 psi source, 40 psi nozzle (both N_2), baked 175°C/2 minutes

Specimen No.	Ta Solution	Output I_{sc} (ma)			% Increase From Bare Cell
		As-Received	After SiO Strip	After Coated	
SPR 1	482	286	215	274	27
SPR 2	482	273	223	257	15
SPR 3	482	275	214	258	21
SPR 4	482	272	221	259	17
SPR 5	482	280	224	262	17
SPR 6	201	283	216	266	23
SPR 7	201	283	219	274	25
SPR 8	201	277	207	268	29
SPR 9	201	290	220	287	30
SPR 10	201	295	222	292	31
SPR 11	201	278	219	271	24

Attempts to increase the effective spray pattern to a uniform, one pass, 3-inch width proved unsuccessful. Width of spray pattern is generally governed by the distance of the nozzle from the part. Early experimentation in varying the equipment parameters such as nozzle height and pressure, showed best results (most uniform in the 1000Å range thickness) to be limited to a 3/4" width band. This, then, necessitated multiple passes to coat the 3-inch diameter cells. Final settings for the 3-inch cells consisted of:

o No. work indexing	4
o Table index distance	1.5 inches
o No. spray pass/index	1
o Travel rate	16 inches/second
o Nozzle height	4.25 inches
o Orifice size	9 mils diameter
o Cup pressure	2 psi, N_2
o Nozzle pressure	40 psi, N_2

Spray pattern used on these 3-inch cells is illustrated in the following diagram.



OPERATION SEQUENCE:
Start
Pass 1
Index 1.5 inches
Pass 2
Index 1.5 inches
Pass 3
Index 1.5 inches
Pass 4
Stop

Results of spray coated 3-inch diameter cells are shown in Table 5.

TABLE 5

SPRAY-ON Ta SOLUTION ELECTRICAL OUTPUT EFFECTS - BEFORE AND AFTER

Cell Size: 3 diameter

Process Parameters:

Zicon Autocoater	
No. Indexing	4
Single Spray Pass/Index	
Orifice Size	9 mils
Nozzle Height	4.25 inches
Rate	16 inches/second
Spray Material	Allied Chem #201

Cell No.	Surface Finish	Contacts	I_{sc} (A) Before Spray Coat	I_{sc} (A) After Spray Coat	Δ%
130 C-21	Flash Etched	Sc-Pr	.935	1.108	+19
-22	" "	"	.958	1.051	+11
-23	" "	"	.924	.978	+ 6
117 -3	" "	Electroless Ni	.869	1.028	+18
-4	" "	" "	.862	1.030	+19
-5	" "	" "	.851	1.024	+20
118 -1	Texture Etch	Electroless Ni	1.121	1.192	+ 6
-2	" "	" "	1.123	1.204	+ 7
-3	" "	" "	1.121	1.200	+ 7

Published data[1] indicates a reflectance % of ~10% for texture-etched silicon cell surfaces. After AR coated, this reflectance value is reduced to ~3%, an absorption improvement of >7%. Relating this 7% value to increased cell output, it compares favorably with before and after results of texture-etched cells shown in the above table.

[1] P.A. Iles, Journal of Vacuum Sciences Technology, Volume 14, No. 5, Sept./Oct. 1977

It is felt that with optimized nozzle and vapor spreader design and dimensional tolerancing, improved performance can be attained with this equipment. Better concentricity of nozzle and vapor spreader parts can improve repeatability. However, the fact that reasonable uniformity was attained with the "as is" equipment lends credence to the merits of this spray technique.

3.4 HIGH VOLUME PRODUCTION PLAN

The specific sequence of solar cell manufacturing processes which was the subject of laboratory study in this contract period have been individually extrapolated to the level of high production process and equipment concept definitions. That work has been previously reported in the quarterlies. This sequence of high production processes has now been integrated into a preliminary plan for a solar cell manufacturing line and is presented in this final report.

The LMSC approach to high production planning favors multiple parallel production lines rather than a single very high throughput system. The rationale for this choice includes several factors: the system can be proven in the first installation which serves as a pilot line; additional lines can reflect incremental process improvements; shutdown of a process step in any one line does not impact the other production lines; shutdown of different process steps on adjacent lines can be accommodated by cross-transfer of parts in process so that the net result is that of one line stopped; a greater degree of flexibility is attained in the establishment of factory production capability; and finally, this arrangement facilitates a hierarchal computer control system for automating the production, with computers at the process, production line, and factory control levels.

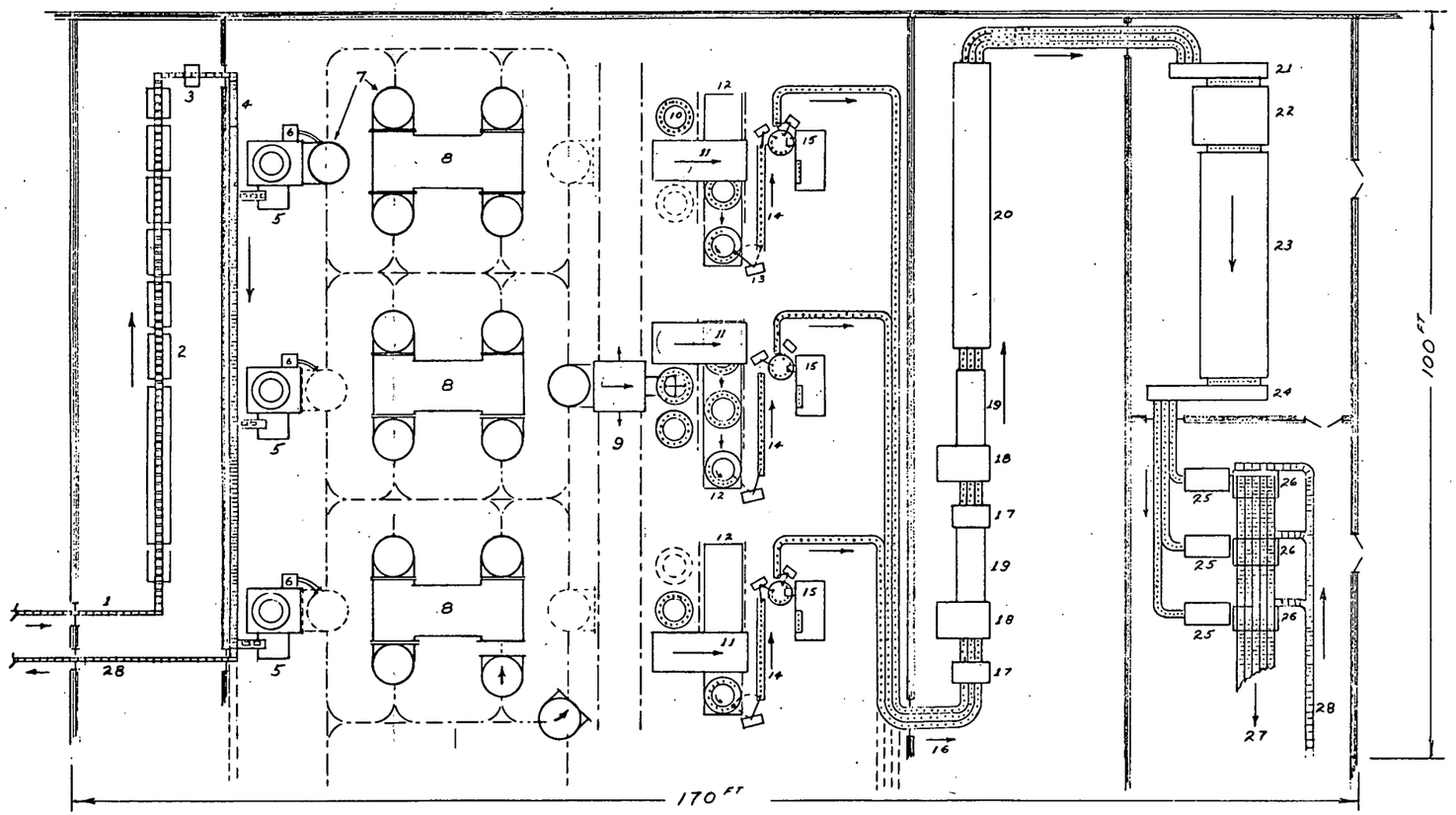
The several process steps in cell manufacturing are listed below, together with the production rates anticipated for each.

	Wafers/Minute/Machine	Line Rate/Minute
Texture Etch	200	200
Ion Implant	50 x 3 machines	150
Laser Anneal	60 x 3 machines	180
Screen Print	150	150
AR Coat	150	150

The pacing element in this sequence is the ion implant operation, with the laser annealing operation capable of a slightly higher rate. Both of these steps are limited in throughput rate by the nature of the process. The rate for the texture etch process was established before the limitations of the ion implant step were determined, but this process could easily be adjusted to suit. Screen printing and AR coating are probably capable of higher throughput rates but were established to match the ion implant step. The resultant overall production rate for this cell manufacturing line is 150 cells per minute or 9000 per hour. On this basis, 5 such lines would produce 45,000 cells per hour. At an assumed yield of 95%, the net production is 42,750 cells per hour which is very close to that estimated for a facility producing 40% of the total 1986 cell requirements.

The proposed layout for the cell processing line is shown in Figure 23. The elements of the line are identified. As noted, the details of the individual production processes have previously been discussed in the quarterlies. This layout introduces the integration of these processes with the special wafer handling and conveyor devices which are capable of being developed into a totally automated production system. The flow of wafers through this line is generally self explanatory, but certain features of the layout should be discussed.

It is assumed that the wafers will be loaded into cassettes by the wafer supplier. These are specially configured with an open frame to facilitate their use as a carrier through the texture etch process. They are also used for in line storage of wafers to supply the ion implant process. The empty cas-



LEGEND:

1. LOADED CASSETTES FROM WAFERCO ON CONVEYOR
2. TEXTIIRE ETCH PROCESS
3. INSPECTION STATION
4. MULTILEVEL CASSETTE STORAGE - STOCK FLOAT FOR ION IMPLANT
5. TRANSFER WAFERS FROM CASSETTES TO TRAYS - CASSETTES RETURN TO EXIT CONVEYOR - EMPTY TRAYS RECEIVED BY OVERHEAD ELEVATOR - FILLED TRAYS ARE LOADED IN VACUUM CHAMBER
6. VACUUM SOURCE FOR PUMP DOWN OF CHAMBER AFTER LOADING
7. MOBILE VACUUM CHAMBERS - FIVE PROVIDED FOR EACH ION IMPLANT STATION
8. ION IMPLANT STATION
9. UNLOAD TRAYS FROM CHAMBERS AND STACK - TRACK GUIDED TRAVEL TO THREE POSITIONS FOR EACH ION IMPLANT STATION
10. TRAY STACK ON ELEVATOR PLATFORM RECESSED IN FLOOR - STOCK FLOAT FOR LASER ANNEAL
11. TRANSFER TRAYS FROM STACK TO TRAY UNLOADER - TRACK GUIDED TRAVEL TO THREE STACK POSITIONS
12. TRAY INDEX TABLE AT END OF TRAY UNLOADER - TRAYS RETURNED TO 5 BY ELEVATOR AND OVERHEAD CONVEYOR
13. "PICK & PLACE" ARM - TRANSFER WAFERS FROM TRAYS TO CONVEYOR
14. STORAGE CONVEYOR WITH "PICK & PLACE" ARM TO UNLOAD
15. LASER WITH INDEXING TURNTABLE - STATIONS FOR WAFER POSITIONING LASER ANNEALING, TESTING AND UNLOADING
16. PARALLEL WAFER CONVEYORS
17. WAFER TURNOVER STATIONS
18. SCREEN PRINT STATIONS
19. BAKE OVEN CONVEYOR
20. FURNACE CONVEYOR
21. REPOSITION WAFERS IN ROWS OF 12
22. SPRAY AR COAT
23. BAKE AR COAT
24. REPOSITION CELLS IN ROWS OF THREE
25. CELL TEST STATIONS
26. SORT CELLS AND LOAD IN CASSETTES - TRANSFER CASSETTES TO OVERHEAD CONVEYOR
27. OVERHEAD CASSETTE CONVEYOR TO FINISHED STORES
28. EMPTY CASSETTE CONVEYORS
    - o PRODUCTION RATE - 9000 CELLS PER HOUR
    - o FIVE LINES REQUIRED FOR PLANT PRODUCING 40% OF 1986 PRODUCTION REQUIREMENTS

SOLAR CELL MANUFACTURING LINE

Figure 23

settes are carried by conveyor to the receiving area for return to the wafer source. The texture etch process requires storage tanks for preheating, filtration, solution makeup, etc. These are intended for installation at the basement level directly below the processing tanks so that this portion of the system maintenance operations are separated from the production area. The high voltage ion beam source is also located in the basement for maintenance and safety as well as satisfaction of the proposed equipment configuration. Certain portions of both the cassette and wafer conveyor lines are expected to be elevated to provide clearance for pedestrian walkways. These locations should be at the cassette entrance and exit conveyors in the texture etch room, at the wafer conveyors leaving the laser anneal stations and entering the screen print room, and for the empty cassette conveyor(s) which supply the final test and sort operations.

The flow of wafers through the several operations is arranged to facilitate extensions of the cassette and wafer conveyors and of the vacuum chamber guide tracks associated with the ion implant process. This will permit cross-transfer of work pieces to an adjacent production line to assist in minimizing the impact of down time for individual processes. It should also be noted that the separate rooms, provided to control cross-contamination between processes, can be extended in length to accommodate additional parallel production lines.

3.5 PROCESS PROCEDURES

Detailed process procedures were prepared and submitted to JPL. They reflect the step-by-step process used in the fabrication of hardware for our process verification evaluations. Processing procedures included: texture-etching, ion implantation, laser annealing, screen printed ohmic contacts, and sprayed AR coatings.

3.6 SAMICS

Solar Array Manufacturing Industry Costing Standards, Format A's for our solar cell process sequence were prepared and are included in Appendix A as follows:

Process Description	Page
Texturize Etch	A-1
Ion Implant	A-13
Laser Anneal	A-18
Screen Printing	A-24
AR Spray Coat	A-30

Section 4

CONCLUSIONS

4.1 Texture etching of 1:0:0 Cz silicon wafers without an initial flash etch step yields acceptably prepared surfaces for standard processing, such as with furnace annealing of ion-implanted cells.

4.2 A dedicated 10 mA beam current ion implanter with an acceleration voltage 5 to 10 KeV will satisfy the high throughput requirements of the 1986 PROJECT goals.

4.3 Laser annealing has been demonstrated to yield high efficiency output ion-implanted cells.

4.4 Laser annealing offers excellent prospects to achieve the low cost objectives through its high throughput and reduced energy consumption potentials. High powered glass lasers are available with the capability of yielding pulsed spot sizes on the order of 3-inch diameters.

4.5 Lasers best suited for annealing of silicon wafers for this LSA PROJECT are pulsed Q-switched, Nd:Glass and Nd:Glass with a frequency doubler. The wavelenghts of these lasers are: 1064 nm and 532 nm, respectively. Comparable lasers in the high frequency, low power categories are not compatible with the high throughput requirements of the PROJECT. This includes ruby and argon CW or pulsed lasers.

4.6 Laser annealing yields a substrate from which higher efficiency cells can be fabricated than those furnace annealed at a conventional 30 minute, single step cycle.

4.7 Laser annealing with Q-switched lasers result in surface melting and therefore, does not appear to be compatible with texture-etched silicon

wafers. However, used with flash-etched and AR spray-coated techniques, additional processing costs could be saved with no loss in cell efficiencies.

4.8 Silver paste material costs to form screen-printed ohmic contacts will not meet the PROJECT cost objectives unless techniques are developed which reduce the amounts utilized. Alternate materials and processes could contribute significantly.

4.9 Semi-automated spray coating of AR film has been demonstrated to show excellent potential for high throughput, low cost manufacturing. However, nozzle and vapor spreader optimization is required for improved performance.

4.10 Low cost, high throughputs of the various process steps of texture etching, ion implanting, laser annealing, screen printing and sprayed AR coatings can be attained to meet the 1986 LSA PROJECT goals based on our automated high volume production plan.

Section 5

RECOMMENDATIONS

5.1 Scale-up the laser annealing verification work using a Q-switched glass laser system capable of single pulse annealing of at least 1-inch diameter spot size. From this work, more concrete determinations can be made for scale-up to high powered lasers with 3-inch diameter spot sizes and rep rates of 1 pps.

5.2 Verification work on alternate high throughput, low cost, ohmic contacting systems should be continued.

5.3 Spray coating of AR film should be optimized by developing more precision nozzles and vapor spreader mechanisms to accommodate larger width, uniform patterns (3 inches).

REFERENCES

1. Physical and Electrical Properties of Laser Annealed Ion-Implanted Silicon/ A. Gat, J. F. Gibbons - Stanford Electronics Laboratories, Stanford, Ca., Appl. Phys. Lett. Vol. 32, p. 142 (1978)

2. Laser Annealed Boron Implanted Silicon Solar Cells/R. T. Young, C. W. White, G. J. Clark, J. Narayan, R. D. Westbrook, W. H. Christie - Oak Ridge National Laboratories, Oak Ridge, Tenn., Proceedings of the Photovoltaic Solar Energy Conference, Luxembourg (Sept 27-30, 1977)

3. Laser Annealing of Implanted Silicon/O. G. Kutukova, L. N. Streltsov - I. V. Kurchatov Institute of Atomic Energy, Moscow, U.S.S.R., Sov. Phys. Semicond. Vol. 10, No. 3 (Mar 1976)

4. Distribution of an Implanted Impurity in Silicon After Laser Annealing/ A. Kh. Antonenko, N. N. Gerasimenko, A. V. Dvurechenskii, L. S. Smirnov, G. M. Tseitlin - Institute of Semiconductor Physics, Academy of Sciences of the U.S.S.R., Novosibirsk, Sov. Phys. Semicond., Vol. 10, No. 1 (Jan 1976)

5. Annealing of Implanted Layers by a Scanning Laser Beam/G. A. Kachurin, G. V. Nidaev, A. V. Khodyachikh, L. A. Koraleva - Institute of Semiconductor Physics, Siberian Branch, Academy of Sciences of the U.S.S.R., Novosibirsk, Sov. Phys. Semicond., Vol. 10 (Oct 1976)

APPENDIX A

SOLAR ARRAY MANUFACTURING INDUSTRY COSTING STANDARDS (SAMICS) FORMAT A'S

SOLAR ARRAY MANUFACTURING INDUSTRY COSTING STANDARDS

FORMAT A

JET PROPULSION LABORATORY
California Institute of Technology
4800 Oak Grove Dr. / Pasadena, Calif. 91103

PROCESS DESCRIPTION

A1 Process Referent: Tex Etch Revision A 6/29/78

A2 Description (Optional): Texturize Etch, Rinse and Dry

PART 1 – PRODUCT DESCRIPTION

A3 Product Referent: TE Wafer

A4 Name or Description: Texture Etched Wafers

A5 Units Of Measure: Wafers

PART 2 – PROCESS CHARACTERISTICS

A6	Output Rate	200	Units (given on line A5) Per Operating Minute
A7	Average Time at Station	40	Calendar Minutes
A8	Process Usage Time Fraction	.976	Average Number of Operating Minutes Per Minute

PART 3 – EQUIPMENT COST FACTORS

A9	Component Referent				
A10	Base Price Year For Purchase Price		1977		
A11	Purchase Price ($ Per Component)	*	$634,000		
A12	Anticipated Useful Life (Years)		7		
A13	Salvage Value ($ Per Component)		$30,000		
A14	Cost of Removal & Installation ($/Component)	**	$83,000		

*A-11 includes on-site assembly and installation costs of $83,000 due to the configuration of this wet process equipment.

**A-14 Removal and installation taken at same level as original installation. Cost of removal assumed to be offset by reuse of some portion of installation, e.g., roof penetrations, safety sumps, electrical plumbing, etc.

JPL 3037-S 11/77

(A) Note: See also Appendix to Format A - Texture Etch for additional information.

Format A: Process Description (Continued)

A14 Process Referent (From Page 1) Tex Etch

PART 4 – DIRECT REQUIREMENTS PER MACHINE

A16 Catalog Number	A17 Requirement Description	A18 Amount Required Per Machine	A19 Units
A2064D	Manufacturing Space (Type A)	1000	Sq. Ft.
B3672D	Chemical Operator II 558885	2.0	Person Years

PART 5 – DIRECT REQUIREMENTS PER BATCH (A continuous process has a "batch" of one unit)

A20 Catalog Number	A21 Requirement Description	A22 Amount Required Per Batch	A23 Units
	Alcohol	.069526	Gal/Minute
	NaOH	.00925	Lbs/Minute
C 1016B	Tap Water	.090454	Gal/Minute
	H_2S_{04} Acid	.779605 (A)	Lbs/Minute
C 1144D	DI Water	.090454	Cu Ft/Minute
	Freon	.01667	Gal/Minute
C 1032B	Electricity	.376888	KW hr/Minute

PART 6 – INTRA-INDUSTRY PRODUCT(S) REQUIRED

A24 Product Reference	A25 Product Name	A26 Yield Factor (Usable Output/Input)	A27 Units
* A.S. Wafer	Texture Etched Wafers	** 99.2%	TE Wafers/A.S. Wafer

Prepared by R. Casey Date 6/29/78

*As Sawn Wafer

**No inspection is planned at completion of this operation - Figure represents average yield for each of seven process stops with final inspection yield of 95%.

APPENDIX TO FORMAT A - TEXTURE ETCH

Prepared by R. J. Casey, LMSC
6/29/78

This material is provided as back-up to SAMICS input as part of JPL contract 954898 and includes the following:

- o A description of the texture etch process (excerpted from Monthly Report No. 6)
- o Explanation of the Format A inputs by part and item
- o Equipment cost estimating sheets (by LMSC Plant Engineering)

3.0 HIGH VOLUME PRODUCTION

3.1 Texture Etch Process

The basic process specification for texture etching of silicon wafers was provided to LMSC (IR) by JPL. Some adjustments to procedural details were made to improve our results in processing of wafers during the early portion of this contract. This modified process has been extrapolated to a large scale automatic etching system as would be required for 1986 production quantities.

The hydrogen peroxide neutralizing rinse has been eliminated in our projected process, as we believe that the simpler acid rinse will suffice if followed by multiple DI water sprays. The system defined here is configured for pilot evaluation. In this regard, it provides for excess capability in terms of sodium hydroxide concentration, immersion time and/or processing temperature. Optimum process parameters for an automated system must necessarily be established during a period of trial operation of the actual system. It will

be simpler at that time to reduce the value of one or more of the variables than to effect an increase. Impact of this approach on overall cost estimates is minimal. Provisions necessary to minimize downtime and maintain real time process control have been considered.

The large number of wafers to be run through a wet system argues convincingly for processing of the work pieces while they are held in cassettes. Accordingly, we have defined a special open frame cassette configuration for wet processing. The 3/16-inch wafer spacing is retained but the length is increased to approximately twelve inches to hold a quantity of 50 wafers. The cassettes are assumed to be loaded by Waferco and entered directly into the Cellco production sequence at this texture etch station. They are automatically clamped to holding devices attached on 6-inch centers to dual conveyor chains which carry the cassettes through the etching steps. Conveyor speed is assumed at 2 feet per minute. Masking of the wafers by the cassette retaining slots is avoided by a technique proven by the Siltec Corporation, Cassette Etch Station, Model 2001, where the cassette is slowly rotated on an eccentric longitudinal centerline. This causes the wafers to move back and forth in their retaining slots, exposing the entire surface to the processing liquids. In this application, the rotation is achieved by spur gears on the end(s) of the cassette holders. The gears engage stationary gear racks as the conveyor chain moves. The conveyor path and the several process steps are shown schematically in Figure 2.

The first step in the etching process is an alcohol rinse, agitated by submerged jets to direct the flow between the wafers. Vapors are recondensed and returned to a reservoir which provides makeup alcohol. Cassettes are then carried directly into the etchant tank and through the hot, two percent sodium hydroxide solution. Agitation is similarly provided. Level, pH, temperature and specific gravity sensors control the makeup system. The solution is circulated in reverse flow direction and filtration is accomplished by De-Laval centrifuges which do not require consumable filters or labor intensive servicing. Vapors may be allowed to vent to the atmosphere carry-

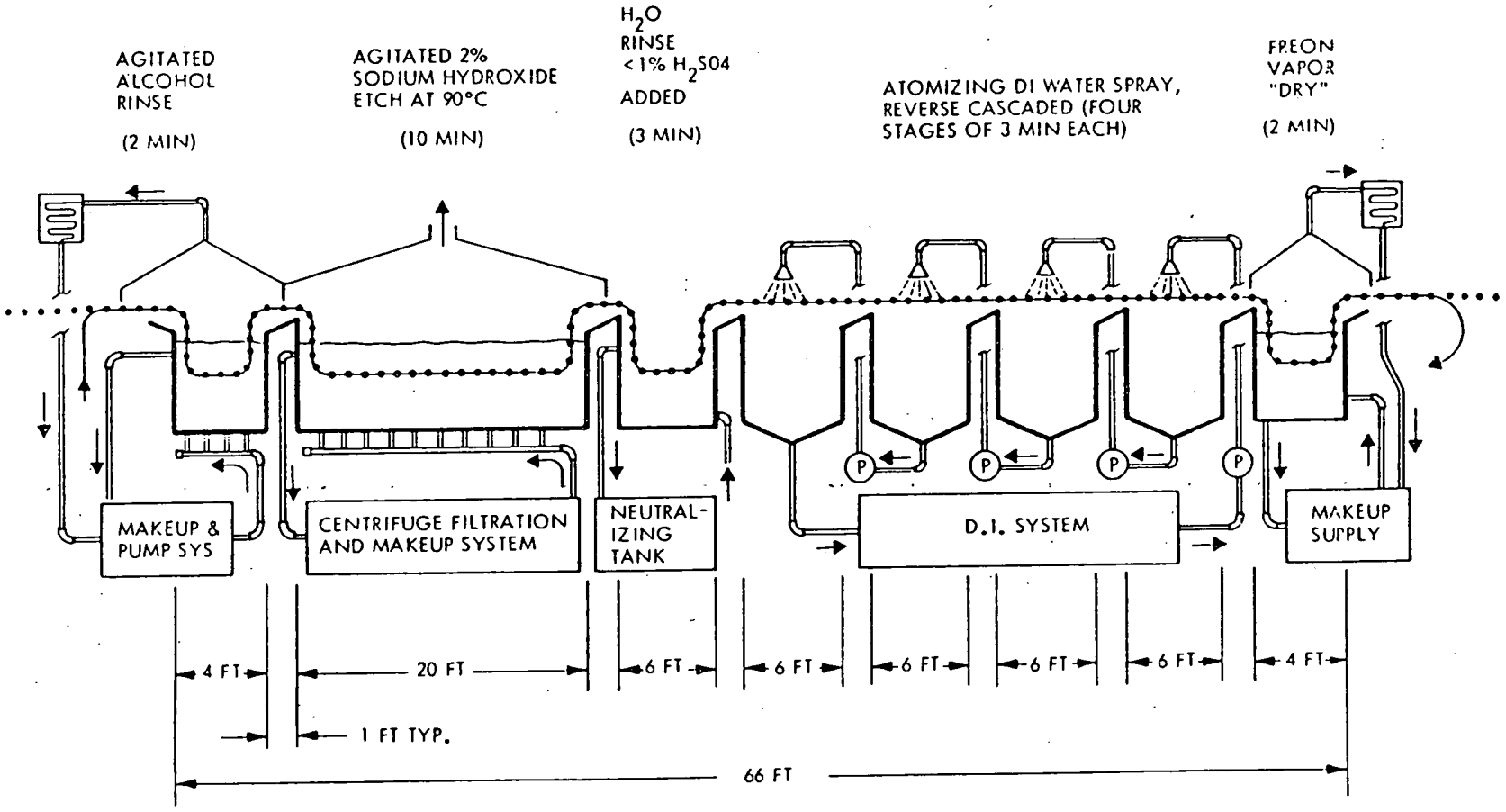


Figure 2. Schematic - Texture Etch Process

ing sodium carbonate salts, which are slightly basic. The next step is a tap water rinse with sufficient acid added to neutralize the drag-out from etching tank. Ten percent of the outflow is brought to neutral pH and discarded to control the salt concentration. Makeup acid and water are added to the remainder which is recirculated. The wafers are then carried through a series of four atomizing spray chambers where they are washed with reverse cascaded DI water. Waste water from the rinse may be used to heat the first spray station through a heat exchanger. This wash water is also reprocessed through filtration and deionizing steps. Finally, the wafers are dried by passing through Freon vapor where surface water on the wafers is displaced. As the wafers emerge, the Freon evaporates. Vapors rising into the hood are recondensed and returned to the system. Displaced water is removed from the Freon to maintain system balance. The cassettes are then fixed in an upright position and disengaged from their holders for transfer to the next operation.

The system will require computer control to maintain the several variables within pre-established limits. Quality of the etch will be sensed by test of the reflectivity of wafers leaving the station with automatic corrective action programmed. It has been suggested by IR that laser induced fluorescent spectroscopy may also be employed to check for contamination levels with automatic correction or shutdown procedures incorporated in the control system.

This texture etch station will process 4 cassettes or 200 wafers per minute. Four parallel stations will be required. Recycling subsystems will be cross-manifolded between stations to minimize downtime. All tanks will be castored and configured for quick-disconnect to allow rapid replacement and offline cleaning and/or refurbishment.

The SAMICS Form A on this process is in preparation and will be submitted under separate cover.

A-6 Output Rate - 200 wafers per minute

Determined by assumed conveyor speed of texture etch equipment at 2 ft/min and spacing of 50 wafer cassettes at 6" apart.

A-7 Average Time at Station = 38 minutes

Determined by assumed conveyor speed of texture etch equipment at 2 ft/min x length of conveyor chain in the processing area.
79 ft ÷ 2 ft/min = 39-1/2 ≅ 40 minutes

A-8 Process Usage Time Fraction = .976

Determined on basis of assumed downtime under the following conditions:

- All tanks fitted with castors and quick disconnect plumbing to allow rapid replacement and off-line cleaning
- Centrifuge filters and other stationary subsystems cross-manifolded to permit rapid changeover, making individual units available for cleaning or service during idle time
- Continuous computer control with feedback loops to eliminate batch operations and allow continuous operation. Downtown assumed to be 4 hrs/wk for mechanical maintenance. 24 hrs/day x 7 days = 168 hrs
  168 hrs - 4 hrs downtime = 164 hrs
  164 operating hours ÷ 168 hrs = .976

A-9 Component Referent - N/A

A-10 Base Price Year for Purchase Price = 1977

Selected for availability of recent cost experience

A-11 Purchase Price per Component = $634,000

Direct estimate from schematic diagram and written description in LMSC Monthly Report No. 6, supplemented by verbal descriptions and process notes. Estimate made by LMSC Plant Engineering organization (attached).

A-12 Anticipated Useful Life (Years) = 7

From 5101-33 Interim Price Estimation Guidelines p. 2-1

A-13 Salvage Value $/Component = $30,000

Arbitrary assumption

A-14 Cost of Removal and Installation = $83,000

Taken at same level as original installation, which is included in A-11 purchase price. Cost of removal is assumed to be offset by reuse of some portion of original installation, e.g., roof penetrations, safety sumps, electrical plumbing, etc.

DIRECT REQUIREMENTS PER MACHINE

A-16 Catalog Number	A-17 Requirement Description	A-18 Amt. Req'd. per Machine	A-19 Units
A-2064-D	Manufacturing Space	1000 66' length of tank line plus 34' of service area = 100' length total 2' width of tanks + 2' for plumbing, etc. = 4' plus clearance for tank removal at 6' = 10 ft total 100' x 10' = 1000 sq ft	Sq Ft
B-3672-D	Chemical Operator II	2.0 Assumes 2 operators tending 4 etchant systems = .5 operator x 4 crews = 2.0	Person/Yrs

DIRECT REQUIREMENTS PER BATCH

A-20 Catalog Number	A-21 Requirement Description	A-22 Amt. Req'd. per Batch	A-23 Units
C1032B	Electricity		KW hr/min
	a. Make up heating of NaOH sol'n to compensate for cooling effect of wafers	@ 90°C process temp - temp rise of wafer is 73°C Specific heat of Si is .15 cal/g - Wafer weight is 4.8g .15 x 4.8 = .72 cal/deg C x 73°C = 52.56 cal/wafer 4.1868 J/cal x 52.56 = 220.0582 J req'd. to reach 90°C or .00006112 KW hr/ wafer x 200 wafers/min = .012224	.012224
	b. Conveyor chain drive @ 10 HP	7.457 KW hr/60 min = .124283	.124283
	c. Pumps & Centrifuges total 8 HP for pumps, 10 HP for centrifuges = 18 HP	13.423 KW hr/60 min = .223716	.223716
	d. Heating & Refrig. units in Freon tank	10 KW/60 min =	.016667
		Total Electricity	.37689 KW hr/min
	Alcohol		
	a. Wafer drag out	Drag out @ .83g/wafer (based on lab tests w/water & alcohol @ 3,141.17 g/gal) = 0002643 gal/wafer x 200 wafers/min	Gals/min .05286
	b. Filtration & Misc. Losses	Estimated @ 1 gal/hr	.016667
		Total Alcohol	.069526 Gal/Min

A-20 Catalog Number	A-21 Requirement Description	A-22 Amt. Req'd. per Batch	A-23 Units
F1080B	Water	Note: All water used is assumed to be tap water since a DI water recycle system is included as part of the texture etch installation	Cu Ft/min
	a. Drag out from NaOH tank	@ 1 cc/wafer (based on lab tests) = .00000215 Cu Ft/wafer x 200 wafers/min = .00043	.00043
	b. Drag out from acid	Same as (a)	.00043
	c. Drag out from DI water rinse	Same as (a)	.00043
	d. 10% of acid rinse tank sol'n neutralized & discarded @ 5 gal per minute flow	= .5 gal/min @ .1337 Cu Ft/gal = .1337/.5 = .06685	.06685
	e. Misc. losses to vapor, processing, etc.	@ 10 gal/hr = .16667 gal/min	.022284
		Total Water	.090454 Cu Ft/Min
	NaOH		Lb/Min
	a. Drag out loss	@ 2% by weight = .02 g/wafer x 200 = 4 g/min ÷ 454 g/lb = .0088105 lb/min	.0088105
	b. Losses to vapor & misc.	.05% by weight = .001 g/wafer x 200 wafers/min = .2 g/min ÷ 454 g/lb = .0004405 lb/min	.0004405
		Total	.00925 Lbs/Min

A-20 Catalog Number	A-21 Requirement Description	A-22 Amt. Req'd. per Batch	A-23 Units
	H_2SO_4		Lb/Min
	a. Drag out loss	@ 1% by weight = .019/ wafer x 200 wafer/min = 2 g/min ÷ 454 g/lb = .004405 lb/min	.004405
	b. Losses to 10% sol'n discard	@ 5 gal sol'n/min = .5 gal discard @ 10% strength = .05 gal acid/min (@ spec gravity of 1.86 = 15.504 lbs/gal) .05 x 15.504 = .7752 lbs/min	.7752
		Total	.779605 Lb/Min
	Freon		Gal/Min
	Misc. Losses	@ 1 gal/hr = .016667 gal/min	.016667

FORMAT A

JET PROPULSION LABORATORY
California Institute of Technology
4800 Oak Grove Dr. / Pasadena, Calif. 91103

PROCESS DESCRIPTION

A1 Process Referent: Ion Plant Revision A, 11-16-78

A2 Description (Optional): Ion implant phosphorus on face side of wafer

PART 1 – PRODUCT DESCRIPTION

A3 Product Referent: P.I. Wafer

A4 Name or Description: Phosphorus ion implanted wafer

A5 Units Of Measure: Wafers

PART 2 – PROCESS CHARACTERISTICS

A6	Output Rate	50	Units (given on line A5) Per Operating Minute
A7	Average Time at Station	1200	Calendar Minutes
A8	Process Usage Time Fraction	.95	Average Number of Operating Minutes Per Minute

PART 3 – EQUIPMENT COST FACTORS

A9	Component Referent	N/A		
A10	Base Price Year For Purchase Price	1978		
A11	Purchase Price ($ Per Component)	$500,000		
A12	Anticipated Useful Life (Years)	7		
A13	Salvage Value ($ Per Component)	$80,000		
A14	Cost of Removal & Installation ($/Component)	$40,000		

Format A: Process Description (Continued)

A14 Process Referent (From Page 1) _____

PART 4 – DIRECT REQUIREMENTS PER MACHINE

A16 Catalog Number	A17 Requirement Description	A18 Amount Required Per Machine	A19 Units
A-2064-D	Manufacturing Space	1500	sq. ft.
B-3704-D	Electronics Technician Automated Processes	4.0	person/years

PART 5 – DIRECT REQUIREMENTS PER BATCH (A continuous process has a "batch" of one unit)

	A20 Catalog Number	A21 Requirement Description	A22 Amount Required Per Batch	A23 Units
		Phosphorus Pentafluoride Gas PF_5	.00555	cc/min
A	C1032B	Electrical Power	7	KW hr/hr
	C1128D	Cooling Water	10	gal/min
	C2032D	Compressed Air - 50 psi	.104	cu ft/min
	C1080D	Liquid Nitrogen	.0625	liters/min
	E1112D	Argon	.5	cu ft/min

PART 6 – INTRA-INDUSTRY PRODUCT(S) REQUIRED

A24 Product Reference	A25 Product Name	A26 Yield Factor (Usable Output/Input)	A27 Units
TE Wafer	Phosphorus Ion Implanted Wafer	99.2%*	PI Wafers/TE Wafer

Prepared by R. Casey Date _____

*No inspection is planned at completion of this operation. Figure represents average yield for each of seven process steps with final inspection yield of 95%.

REVERSE SIDE JPL 3037-S 11/77

A-6 Output Rate 50 Wafers per Minute

Based on calculated scan time for 10 ma beam current with allowance for spacing between cells on a flat tray

A-7 Average Time at Station 1200 Minutes

Based on 16 hours process cycle time per chamber plus two hours load and two hours unload time per chamber = 20 hrs.

A-8 Process Usage Time Fraction .95

Dependent on filament life which is assumed to be 80 ma hrs. and will require 20 minutes to change. Filament and chamber replacement to be concurrent. Represents 3.2 x improvement by 1986 in filament life over present Lintott Series III system.

A-9 Component Referent N/A

A-10 Base Price Year for Purchase Price 1978

Based on current estimate

A-11 Purchase Price per Component $500,000

(1) Ion Implantation System	300K
(5) Cylindrical Chambers @ $20K ea.	100K
(1) Central Implantation Chamber	40K
(2000) Trays @ $30 ea.	60K
Total	500K

A-12 Anticipated Useful Life 7 Years

From 5101-33 Interim Price Estimation Guidelines p. 2-1

A-13 Salvage Value 80K

Assumes refurbishment possible for vacuum chamber and wafer handling systems

A-14 Cost of Removal and Installation 40K

Direct Requirements per Machine

A-16 Catalog No.	A-17 Requirement Description	A-18 Amt. Req'd. per Machine	A-19 Units
A-2064-D	Manufacturing Space Type-A	Estimated as per sketch w/allowance for load/unload station and chamber transfer tracks	sq ft
A-3704-D	Electronics Technician Automated Processes	4.0 Assumes one operator/system x 4 crews	person/ years

Direct Requirements per Batch

Assumed to be a Continuous Process

	A-20 Catalog No.	A-21 Requirement Description	A-22 Amt. Req'd. per Batch	A-23 Units
		Phosphorus Pentafluoride Gas PF_5	.00555 Based on current usage - no scale-up for size	cc/min
A	C1032B	Electrical Power	7 Based on data from Acceleration, Inc. (Lintott Rep.). Diffusion pump requirements are controlling factor. Ion implant energy is minor contribution.	KW hr/ hr
	C2032D	Compressed Air - 50 psi (Operation of gate valves and air cushion bearings)	.104 (5 cu ft per min for 10 min each 8 hr shift = 50 cu ft ÷ 480 min per shift)	cu ft/ min
	C1080D	Liquid Nitrogen	.0625	liters/ min
	E1112D	Argon	.5	cu ft/ min

FORMAT A

JET PROPULSION LABORATORY
California Institute of Technology
4800 Oak Grove Dr. / Pasadena, Calif. 91103

PROCESS DESCRIPTION

A1 Process Referent: LASANNEAL

A2 Description (Optional): Laser Anneal Face of Wafer

PART 1 – PRODUCT DESCRIPTION

A3 Product Referent: L.A. Wafer

A4 Name or Description: Laser Annealed Wafer

A5 Units Of Measure: Wafers

PART 2 – PROCESS CHARACTERISTICS

A6	Output Rate	60	Units (given on line A5) Per Operating Minute
A7	Average Time at Station	1.0	Calendar Minutes
A8	Process Usage Time Fraction	.976	Average Number of Operating Minutes Per Minute

PART 3 – EQUIPMENT COST FACTORS

A9	Component Referent			
A10	Base Price Year For Purchase Price	1978		
A11	Purchase Price ($ Per Component)	$450,000		
A12	Anticipated Useful Life (Years)	7		
A13	Salvage Value ($ Per Component)	$225,000		
A14	Cost of Removal & Installation ($/Component)	$10,000		

Note: See Appendix to Format A - Laser Anneal for details.

Format A: Process Description (Continued)

A14 Process Referent (From Page 1) _____

PART 4 – DIRECT REQUIREMENTS PER MACHINE

A16 Catalog Number	A17 Requirement Description	A18 Amount Required Per Machine	A19 Units
A-2064D	Mfg. Space	200	Sq Ft
B-3704D	Electronics Technician Automated Processes	2.0	Person Years

PART 5 – DIRECT REQUIREMENTS PER BATCH (A continuous process has a "batch" of one unit)

A20 Catalog Number	A21 Requirement Description	A22 Amount Required Per Batch	A23 Units
C 1016B	Tap Water	10	Gal/Min
C 1032B	Electricity	.2268	KW hr/min

PART 6 – INTRA-INDUSTRY PRODUCT(S) REQUIRED

A24 Product Reference	A25 Product Name	A26 Yield Factor (Usable Output/Input)	A27 Units
I.I. Wafer	Ion Implanted Wafer	*99.2%	L.A. Wafer/I. Wafer

Prepared by _____ Date _____

*No inspection is planned at completion of this operation. Figure represents average yield for each of seven process steps with final inspection yield of 95%.

REVERSE SIDE JPL 3037-S 11/77

APPENDIX TO FORMAT A - LASER ANNEAL

Prepared by R. J. Casey
LMSC
June 29, 1978

EQUIPMENT DESCRIPTION

Quantel Glass Laser

This will be a special design unit dedicated to this operation.

Laser energy density of approximately 1.5 joules per cm^2 is required to attain annealing of ion implanted silicon wafers. This translates to an energy of approximately 68 joules for a single pulse annealing of a 3-inch diameter wafer. A Q-switched glass laser capable of operating at this energy level with a pulse repetition rate of 1 pulse per second has a conversion efficiency of approximately .5%.

Power Requirements:

68 joules are required to anneal a 3" diameter wafer. At .5% conversion efficiency the laser requires 68/.005 = 13,6000 joules = 3.78 watt hr

Wafer Transport

The previous operation in the cell manufacturing sequence is ion implanting from which the wafers are unloaded individually. These will be automatically transferred to a conveyor system which moves the wafers under the laser beam at a constant rate of one wafer per second. At a center to center distance of 4-inches, this represents a conveyor speed of 20 feet per minute. Laser pulse duration is 20 nanoseconds. The laser pulse will be triggered by the wafer passing under the work area. Pulse duration is so short that the wafer need not be stopped for the annealing operation. The conveyor belt will carry the annealed wafers directly to the next operation.

A-6 Output Rate 60 wafers/minute

Determined by pulse rate of Quantel laser at 1 pulse per second

A-7 Average Time at Station = 1.0 minute

Determined by time on conveyor moving through 20 foot length of station area at rate of 20 feet per minute = 1 minute

A-8 Process Usage Time Fraction = .976

Arbitrary assumption of 4 hours per week for maintenance.
Plant operation taken as 24 hours/day x 7 days per week = 168 hours
168 hrs - 4 hrs downtime = 164 hours
164 operating hours ÷ 168 hrs = .976

A-9	Component Referent	N/A
A-10	Base Price Year for Purchase Price	1978
	Based on vendor estimate of June 1978	
A-11	Purchase Price	$450,000
	Based on vendor estimate of June 1978	
A-12	Anticipated Useful Life (Years)	7
	From 5101-33 Interim Price Estimation Guidelines p. 21	
A-13	Salvage Value	$225,000
	Arbitrary value based on high capability for refurbishment and update of equipment.	
A-14	Cost of Removal and Installation	$ 10,000
	Arbitrary cost estimate. Requires only electrical and cooling water hookups.	

DIRECT REQUIREMENTS PER MACHINE

A-16 Catalog Number	A-17 Requirement Description	A-18 Amt. Req'd. per Machine	A-19 Units
A-2064-D	Mfg. Space	200 (10' x 20')	Sq Ft
B-3704-D	Electronics Technician Automated Processes	2.0 Assumes one operator tending two machines .5 operator x 4 crews = 2.0 operators	Person/ Years

DIRECT REQUIREMENTS PER BATCH

A-20 Catalog Number	A-21 Requirement Description	A-22 Amt. Req'd. per Batch	A-23 Units
C 1016 B	Tap Water	10 per Equip. Mfr'r (Quantel)	Gal/Min
C 1032 B	Electricity	.2268 3.78 W hr/Wafer @ 60 wafers/min = 226.8 W hr/min or .2268 KW hr/min	KW hr/ min

FORMAT A

JET PROPULSION LABORATORY
California Institute of Technology
4800 Oak Grove Dr. / Pasadena, Calif. 91103

PROCESS DESCRIPTION

A1 Process Referent: Screen

A2 Description (Optional): Screen printing, drying and firing of conductive pastes on back and front sides of wafers

PART 1 – PRODUCT DESCRIPTION

A3 Product Referent: SP Wafer

A4 Name or Description: Screen Printed Wafers - Both Faces

A5 Units Of Measure: Wafer

PART 2 – PROCESS CHARACTERISTICS

A6	Output Rate	150	Units (given on line A5) Per Operating Minute
A7	Average Time at Station	2.77	Calendar Minutes
A8	Process Usage Time Fraction	.98	Average Number of Operating Minutes Per Minute

PART 3 – EQUIPMENT COST FACTORS

		Bk Screen	Ft Screen	Fuse Oven
A9	Component Referent	Bk Screen	Ft Screen	Fuse Oven
A10	Base Price Year For Purchase Price	1978	1978	1978
A11	Purchase Price ($ Per Component)	80,000	80,000	30,000
A12	Anticipated Useful Life (Years)	7	7	7
A13	Salvage Value ($ Per Component)	20,000	20,000	10,000
A14	Cost of Removal & Installation ($/Component)	5,000	5,000	5,000

Format A: Process Description (Continued)

A14 Process Referent (From Page 1) Screen

PART 4 – DIRECT REQUIREMENTS PER MACHINE

A16 Catalog Number	A17 Requirement Description	A18 Amount Required Per Machine	A19 Units
A-2064-D	Manufacturing Space	500	Sq. Ft.
B-3752-D	Production Machine Operator	2	Person Years

PART 5 – DIRECT REQUIREMENTS PER BATCH (A continuous process has a "batch" of one unit)

A20 Catalog Number	A21 Requirement Description	A22 Amount Required Per Batch	A23 Units
C 1032 B	Electricity	.29797	KW hr/min
	DuPont #4021 Silver/Alum Paste	115.652	Grams/min
	Silver Paste DuPont #7095	8.096	Grams/min

PART 6 – INTRA-INDUSTRY PRODUCT(S) REQUIRED

	A24 Product Reference	A25 Product Name	A26 Yield Factor (Usable Output/Input)	A27 Units
*	LA Wafer	Laser Annealed Wafer	** 99.2	Sp Wafer/La Wafer

Prepared by R. Casey, LMSC Date 7/26/78

*Laser Annealed Wafer

**No inspection is planned at completion of this operation. Figure represents average yield for each of 7 process steps with final inspection yield of 95%.

REVERSE SIDE JPL 3037-S 11/77

A-6 Output Rate 150 Wafers/Minute

1500 machine cycles per hour at 6 wafers per cycle processes 9000 wafers per hour ÷ 60 minutes = 150 wafers per minute. Conveyor speeds for drying ovens and firing oven are paced accordingly.

A-7 Average Time at Station Minutes

Screen printer cycles 25 times per minute producing two rows of 3 wafers each to be transferred to the conveyor. Two rows of wafers at 3.1" each row = 6.2" of conveyor length x 25 cycles = conveyor speed of 13 ft/min.

Length of Line:

Turnover and Print Back Face	6 feet
Oven Dry Back Face (30 sec at 150°C)	7 feet
Turnover and Print Front Face	6 feet
Oven Dry Front Face (30 sec. at 150°C)	7 feet
Fuse Conductive Paste (45 sec. at 650°C)	10 feet
Total Length	36 feet

36 ft. ÷ 13 ft/min = 2.77 min at station

A-8 Process Usage Time Fraction .976

Estimated on basis of 4 hours downtime per 168 hour work week.

A-11 Purchase Price per Component

Bk Screen $80,000

Manufacturers estimate of $80,000 for standard unit without cartridge unload and cartridge reload capability.

Ft Screen $80,000

Same as Bk Screen

Fuse Oven $30,000

Direct LMSC Estimate

A-12 Useful Life 7 Years

From 5101-33 Interim Price Estimation Guidelines p. 2-1

A-13 Salvage Valve per Component

Direct LMSC Estimate

A-14 Cost of Removal and Installation

Direct LMSC Estimate

SCREEN PRINT FORMAT A PART 4

A-16 Catalog No.	A-17 Requirement Description	A-18 Amt Req'd per Machine	A-19 Units
A-2064-D	Manufacturing Space	500 ft^2 36' Length of Line x 10 width = 360 ft^2 + 140 ft^2 service area = 500 ft^2	Sq. Ft.
B-3752-D	Production Machine Operator	2 Assumes one Operator tending two screen print systems = .5 operator x 4 crews = 2.0	Person/Years

SCREEN PRINT FORMAT A PART 5

A-20 Catalog No.	A-21 Requirement Description	A-22 Amt Req'd per Batch	A-23 Units
C 1032 B	Electricity (a) combined mechanical drives @ 5 HP	7.457 KW hr ÷ 60 min = .124283	KW hr/min .124283
	(b) drying ovens	@ 150°C drying temp - temp rise of wafer is 131°C Specific heat of silicon is .15 cal/gm Wafer weight is 4.8g - .15x4.8=.72 cal/°Cx 131°C = 94.32 cal/wafer - 4.1868 J/calx94.32= 394.9 Joules req'd to reach 165°C or .0000972 KW hr/wafer x 150 wafers/min = .014578 KW hr/min x 2 ovens = .02915 KWH/min x loss factor of 2.0 = .0583 KW hr/min	.0583
	(c) Paste - Firing Oven	@ 650°C firing temp - temp rise of wafer (from 150°C) is 500°C.	

PART 5 - Continued

A-20 Catalog No.	A-21 Requirement Description	A-22 Amt Req'd per Batch	A-23 Units
		Specific heat of silicon is .15 cal/gm Wafer weight is 4.8 g - .15 x 4.8 = .72 cal/°C x 500°C = 360 cal/wafer - 4.1868 J/cal x 360 = 1507.25 joules req'd. to reach 650°C or .000419 KW hr/wafer x 150 wafers/ min = .0628 KW hr/min x loss factor of 2.0 = .1256	.1256
		Total KW hr/min	.308187
	Silver/Alum Paste DuPont #4021 - 2.9" dia. coverage on back side of cell - Dry thickness of paste is .5 mil - Wet to dry ratio is assumed to be 2:1	Area of 2.9" dia. circular pad is 6.605 in^2 x .001 thickness of paste = .006605 in^3 = .1083 cc per wafer x 150 wafers per min = 16.24 cc/ min @ 65% solids by weight ag = 10.556 cc/min x density of 10.49 g/cc = 110.73 g/min @ 35% solvent by weight solvent = 5.684 cc/min x density of .866 g/cc = 4.922 g/min 110.73 g/min solids + 4.922 g/min solvent 115.652 g/min	115.65 g/min
	Silver Paste (DuPont 7095) Assume 7% coverage x .5 mil dry thickness and wet to dry ratio of 2:1	115.652 g/min x .07 = 8.096 g/min	8.096 g/min

FORMAT A

JET PROPULSION LABORATORY
California Institute of Technology
4800 Oak Grove Dr. / Pasadena, Calif. 91103

PROCESS DESCRIPTION

A1 Process Referent: AR Coat

A2 Description (Optional): Spray Anti-Reflective Coating on Wafers

PART 1 – PRODUCT DESCRIPTION

A3 Product Referent: AR Wafer

A4 Name or Description: Anti-Reflective Coated Wafer

A5 Units Of Measure: Wafers

PART 2 – PROCESS CHARACTERISTICS

A6	Output Rate	150	Units (given on line A5) Per Operating Minute
A7	Average Time at Station	9.5	Calendar Minutes
A8	Process Usage Time Fraction	.98	Average Number of Operating Minutes Per Minute

PART 3 – EQUIPMENT COST FACTORS

A9	Component Referent	Transfer	Spray	Bake
A10	Base Price Year For Purchase Price	1978	1978	1978
A11	Purchase Price ($ Per Component)	$30,000	$65,000	$40,000
A12	Anticipated Useful Life (Years)	7	7	7
A13	Salvage Value ($ Per Component)	0	5,000	5,000
A14	Cost of Removal & Installation ($/Component)	3,000	8,000	8,000

Format A: Process Description (Continued)

A14 Process Referent (From Page 1) AR Coat

PART 4 – DIRECT REQUIREMENTS PER MACHINE

A16 Catalog Number	A17 Requirement Description	A18 Amount Required Per Machine	A19 Units
A-2064-D	Manufacturing Space	600	Sq. Ft.
B 3752 D	Production Machine Operator	2	Person Years

PART 5 – DIRECT REQUIREMENTS PER BATCH (A continuous process has a "batch" of one unit)

A20 Catalog Number	A21 Requirement Description	A22 Amount Required Per Batch	A23 Units
C 1032 B	Electricity	.08165	KW hr/min
C 2032 D	Compressed Air	5.0	Cu Ft/min
	A.R. Coating Mat'l	18.75	cc/min

PART 6 – INTRA-INDUSTRY PRODUCT(S) REQUIRED

A24 Product Reference	A25 Product Name	A26 Yield Factor (Usable Output/Input)	A27 Units
*SP Wafer	Screen Printed Wafer	** 99.2	AR Wafer/SP Wafer

Prepared by R. J. Casey, LMSC Date August 4, 1978

*Screen Printed Wafer

**No inspection is planned at completion of this operation. Figure represents average yield for each of seven process steps with final inspection yield of 95%.

REVERSE SIDE JPL 3037-S 11/77

ANTI-REFLECTIVE COATING FORMAT A PART 2

A-6 Output Rate 150 Wafers/min

Production rate matched to prior operation

A-7 Average Time at Station 9.5 min

Based on conveyor length and speed:

Transfer Device and Spray Booth Conveyor	8 Ft
Baking Oven Conveyor	30 Ft

38 Ft @ 4 Ft/min = 9.5 min

A-8 Process Usage Time Fraction .98

Controlled by preceding screen print operation on basis of 4 hrs. downtime per 168 hr. week

ANTI-REFLECTIVE COATING FORMAT A PART 3

A-11 thru A-14 All items are direct estimates

ANTI-REFLECTIVE COATING FORMAT A PART 4

A-16 Catalog No.	A-17 Requirement Description	A-18 Amt Req'd per Machine	A-19 Units
A-2064-D	Manufacturing Space Type A	38 ft. total conveyor length plus 12 ft clearance = 50 ft x 12 ft width including clearance = 600 sq.ft.	Sq. Ft.
B-3752-D	Production Machine Operator	2 Assumes one operator tending two coating systems = .5 operator x 4 crews = 2.0	Person Years

A-20 Catalog No.	A-21 Requirement Description	A-22 Amt Req'd per Batch	A-23 Units
C-1032 B	Electricity		KW hr/min
	(a) Combined Mechanical drives for: - Vacuum Pump - 2 Conveyors - Spray Head Traverse @ 7 HP	3.729 KW ÷ 60 minutes = .06215 KW hr/min	.06215
	(b) Baking Oven	155°C Temperature rise of Wafers Specific heat of silicon is .15 cal/gm Wafer weight is 4.8 gm .15 x 4.8 = .72 cal/°C x 155°C = 111.6 cal/ wafer 4.1868 J/Cal x 111.6 = 467.25 Joules req'd to reach 175°C oven temperature or 0001298 KW hr/wafer x 150 wafer per min = .0195 KW hr/min	.0195
		Total	.08165 KW/hr/min
C 2032 D	Compressed Air Articulation of Transfer Device and Spray Nozzle Supply	5.0 Direct Estimate	Cu Ft/min
	AR Coating Material	Area sprayed per minute = 1500 angstroms (wet thickness) x 40" x 50" = 18.75 cc/min	18.75 cc/min

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