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SILICON-ON-CERAMIC PROCESS

Silicon Sheet Growth and Device Development for the Large-Area Silicon Sheet and Cell Development Tasks of the Low-Cost Solar Array Project

Quarterly Report No. 11, January 1—March 30, 1979

By
P. W. Chapman
J. D. Zook
J. D. Heaps
B. L. Grung
B. Koepke
S. B. Schuldt

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Honeywell Corporate Material Sciences Center
10701 Lyndale Ave. South
Bloomington, Minnesota 55420

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SUMMARY

The objective of this research program is to investigate the technical and economic feasibility of producing solar-cell-quality sheet silicon. We plan to do this by coating one surface of carbonized ceramic substrates with a thin layer of large-grain polycrystalline silicon from the melt.

Beginning the middle of February 1978, we expanded our program to include activities funded by the Task VI Cell Development Group of the Low-Cost Solar Array (LSA) program at the Jet Propulsion Laboratory. This work is directed toward the solution of unique cell-processing/design problems encountered within the silicon-on-ceramic (SOC) material as a result of its intimate contact with the ceramic substrate.

The Task VI work is contained within this report and is labeled appropriately.

During the quarter, we demonstrated significant progress in several areas:

- We succeeded in fabricating a 4-cm^2 cell having a 10.1 percent conversion efficiency (AM1, AR).
- We succeeded in fabricating a 10-cm^2 cell having a 9.2 percent conversion efficiency (AM1, AR).
- The continuous (SCIM) coater has succeeded in producing a 16-cm^2 coating exhibiting unidirectional solidification and large grain size.

Other results and accomplishments during the quarter can be summarized as follows:

- A layer was grown at 0.2 cm/sec in the experimental coater which was partially dendritic but also contained a large smooth area ~100 μm thick.
- Modifications to the cooling shoes of the experimental dipper were completed, allowing x-y motion and gas cooling.
- Temperature gradients along the trough still present a problem in obtaining uniform continuous coatings using the SCIM coater.
- A top-coating/doctor-blade-type experiment in the SCIM coater yielded a region of smoothly coated large-grain silicon.

- During this quarter, 51 SOC solar cells were fabricated, 39 of which were AR coated.
- Recent analysis shows that the short-circuit current (J_{sc}) deteriorates at roughly -0.11 mA/cm^2 for each consecutive sample dipped.
- The dark characteristic measurements of a typical SOC solar cell yield shunt resistance values of 10K ohms and series resistance values of 0.4 ohm.
- The best 2x cell with concentration has a conversion efficiency of 6.2 percent (AM1, AR) for a total area of 7 cm^2.
- L_D within grains has been determined using an LBIC technique and electrolyte contacts.
- The LBIC technique has been successfully used to determine the difference in performance between our solar cells and those processed by the Solid State Electronics Center.
- A laser scanning system has been set up to determine grain size distribution in SOC material.
- The production dip-coater is operating at over 50 percent yield in terms of good cell quality material. The most recent run yielded 13 "good" substrates out of 15.
- SiC particles are appearing in the production dip-coater after successive dips. The cause for this has not been determined to date.

INTRODUCTION

This research program began on 21 October 1975. Its purpose is to investigate the technical and economic feasibility of producing solar-cell-quality sheet silicon by coating inexpensive ceramic substrates with a thin layer of polycrystalline silicon. The coating methods to be developed are directed toward a minimum-cost process for producing solar cells with a terrestrial conversion efficiency of 12 percent or greater.

By applying a graphite coating to one face of a ceramic substrate, molten silicon can be caused to wet only that graphite-coated face and produce uniform thin layers of large-grain polycrystalline silicon; thus, only a minimal quantity of silicon is consumed. A dip-coating method for putting silicon on ceramic (SOC) has been shown to produce solar-cell-quality sheet silicon. This method and a continuous coating process also being investigated have excellent scale-up potential which offers an outstanding, cost-effective way to manufacture large-area solar cells. The dip-coating investigation has shown that, as the substrate is pulled from the molten silicon, crystallization continues to occur from previously grown silicon. Therefore, as the substrate length is increased (as would be the case in a scaled-up process), the expectancy for larger crystallites increases.

A variety of ceramic materials have been dip-coated with silicon. The investigation has shown that mullite substrates containing an excess of SiO_2 best match the thermal expansion coefficient of silicon and hence produce the best SOC layers. With such substrates, smooth and uniform silicon layers 25 cm^2 in area have been achieved with single-crystal grains as large as 4 mm in width and several cm in length. Crystal length is limited by the length of the substrate. The thickness of the coating and the size of the crystalline grains are controlled by the temperature of the melt and the rate at which the substrate is withdrawn from the melt.

The solar-cell potential of this SOC sheet silicon is promising. To date, solar cells with areas from 1 to 10 cm^2 have been fabricated from material with an as-grown surface. Conversion efficiencies of about 10.0 percent with antireflection (AR) coating have been achieved without optimizing cell processing techniques. Such cells typically have open-circuit voltages and short-circuit current densities of 0.55V and 23 mA/cm^2, respectively.

The SOC solar cell is unique in that its total area is limited only by device design considerations. Because it is on an insulating substrate, special consideration must be given to electrical contact to the base region. One method which offers considerable

promise is to place small slots in the substrate perpendicular to the crystalline growth direction and contact the base region by metallizing the silicon that is exposed through the slots on the back side of the substrate. Smooth, continuous coatings have been obtained on substrates which were slotted in the green state prior to high-temperature firing. The best slotted-cell results indicate a 10.1 percent conversion efficiency (AR-coated) on a 4-cm^2 (total area) cell. This cell was not optimized for device performance.

Development efforts are continuing in such areas as improvement in growth rate, reduction of progressive melt contamination, and optimization of electrical contacts to the base layer of the cell. The investigation has shown that mullite substrates, to a limited extent, dissolve in molten silicon. The impurities from the substrate are believed to adversely affect solar-cell conversion efficiency. A method for reducing substrate dissolution is to reduce the contact area the substrate makes with the silicon melt. Therefore, a silicon coating facility, referred to as SCIM or Silicon Coating by an Inverted Meniscus, has been constructed which is designed to coat large (10-cm x 100-cm) substrates in a continuous manner. It is expected that this facility will not only improve the growth rate, but also minimize the silicon melt contact with the substrate. This should reduce the rate at which the melt becomes contaminated. The facility will also permit a study of possible continued grain growth by accommodating the use of longer substrates. It should also reveal problems that are likely to be encountered in a scale-up process. This machine has succeeded in demonstrating coatings exhibiting unidirectional solidification (desirable and occurring in dip coating) but has yet to achieve continuous coating of a 100-cm-long substrate.

TECHNICAL DISCUSSION

SHEET SILICON GROWTH (J.D. Zook, J.D. Heaps, B. Koepke, L.D. Nelson, D.J. Sauve, O. Harris, and H. Burke)

Dip-Coating Production

The production of SOC substrates during the past few months has been aimed at the delivery of high-quality substrates to JPL for solar cell fabrication by OCLI and Spectrolab. The experimental dip-coating station was also dedicated to production during part of this time. Out of the past 220 substrates dipped, 40 have been shipped to JPL, 30 have been shipped to the Honeywell Solid State Electronics Center, and 40 are ready for shipping. Thus, the overall yield has been about 50 percent. On a most recent run of 15 substrates, 13 were suitable for shipping. The two that did not meet specifications were inadvertently pulled at the wrong pull rate. A number of operational problems plagued the production effort, initially. All of these problems have been resolved except one, as described below:

1) Carbon coating -- The new batch of "K" slotted substrates from Coors apparently have smoother surfaces than the previous batches so that we had considerable difficulty obtaining a good rubbed carbon layer. The surface roughness, as measured by profilometers at Coors and at Honeywell, are quite similar for the different batches, so that the precise nature of the coating difficulty is not understood. We find that by rubbing the surface twice, and blowing off the loose carbon after each coating, consistent wetting can be obtained. The "soak" time in the melt was also reduced to 10 seconds to minimize loss of carbon to the melt. Dag coatings are also being investigated, and a roller method of applying the Dag seems to be quite fast and does not get any Dag in to the slots.

   Ten "type O" substrates from Coors were also dip-coated. The expansion coefficient and other properties seem identical to the type K, except that they are much harder to coat with carbon. The surfaces feel rougher, but the rubbed carbon is readily blown off, and some of the substrates had bare spots that were not wetted by the molten silicon. It would be useful to understand the differences in the surface properties of the ceramic that cause these adverse effects.

2) Dendrites -- There have been a number of problems leading to the appearance of dendrites in the center region of the samples. In large part, the dendrites were apparently caused by insufficient baking of the substrates prior to dipping. At present, the samples are baked at 135°C for 1 hour.

An increase in the number of dendrites also occurred when the new picket-fence-type heater was installed in the production dip-coating system. It was found that these could be eliminated by raising the crucible within the holder and operating at a slightly higher temperature.

3) SiC Particles -- During the course of a run in the production dip-coater, there is a buildup of particles in the melt at the edge of the crucible. After about a dozen substrates have been dip-coated, the particle buildup is such that the particles may adhere to the surface of the layer. This problem arose at the beginning of January and has appeared consistently on every run since then. The results of scanning Auger microscopy (SAM) show very clearly that the particles consist of SiC, with no other detectable impurities. A metallographic examination also showed the SiC crystallites.

A number of experiments have been conducted in an effort to identify and eliminate the source of these particles. They do not appear in the experimental dip-coating system, even when the dipping operation is conducted in the same way by the same operator. They develop in the production dip-coating system only during the actual dipping process. They develop even if uncarbonized substrates are dipped. They do not develop if the system sits without dipping, or if the upper chamber and gate valve are cycled as if substrates were being introduced to the main chamber. Argon from the same source and tubing is used in both systems, and both systems are similar in their ability to hold a vacuum. Undoubtedly there is a logical solution to the problem, but so far it has eluded us.

Experimental Dip Coater

During the past quarter, our efforts to improve the throughput of the dip-coating process were renewed. The basic technique involves the use of cooling shoes placed near the liquid-solid interface during growth to enhance the removal of latent heat. Initial attempts to grow 100-μm-thick silicon layers at pull rates exceeding 0.2 cm/sec involved water-cooled shoes. The cooling was not adequate and one of the shoes was modified to allow a stream of cooled argon gas to be directed at the silicon-coated side of the substrate. With this shoe in place, we grew a dendritic layer at 0.2 cm/sec. However, a large

portion of the coating was smooth and had a thickness of 100 μm. Since the gas jets pointed down, we speculate that the gas cooled the surface of the melt below the liquid-solid interface as well as the silicon coating. As a result, the other shoe was drilled with gas jets that impinge on the coating normal to the coating surface.

The original shoes could only be moved along one axis (the x-axis). Most of the efforts during the past quarter involved modifying the shoes to allow x-y motion without having to open the system during a run. These modifications are now finished and high pull rate dipping experiments will start immediately. A batch of 150 unslotted K-mod substrates was obtained from Coors to be used in the tests. A photograph of the two redesigned cooling shoes in place in the dip coating system is shown in Figure 1. The shoes can be moved up and down by moving the vertical support tube. The shoes can be moved in a direction perpendicular to the support rod by sliding in the track attached to the top of the vertical support. The shoes are moved toward and away from the substrate by rotating rods that protrude from the bottom of the support tubes. A lever attached to the top of each rod affects the motion. A flexible stainless-steel bellows is attached to the vertical support for carrying water and the cooling gas.

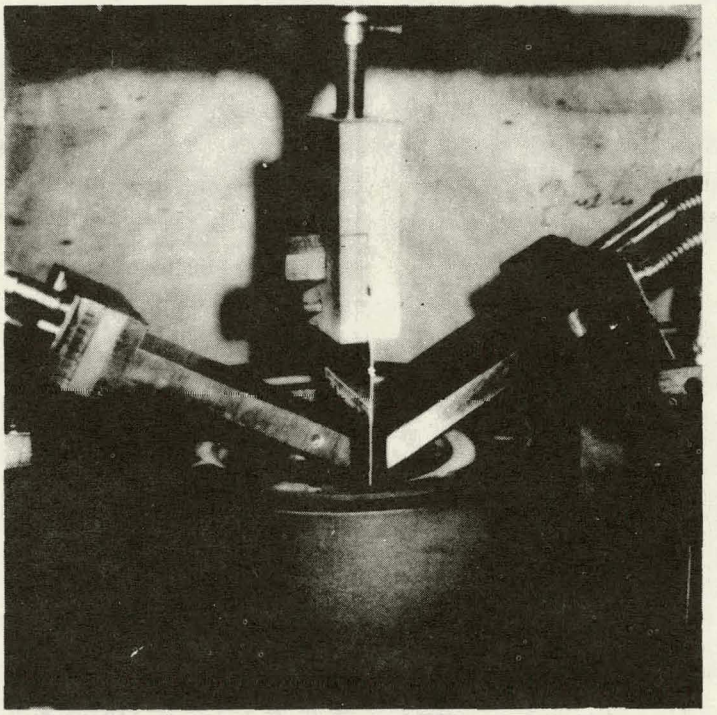


Figure 1. Photograph of Interior of Dip-Coating Apparatus Showing Pull Rod, Substrate, and Cooling Shoes

Continuous Coating Process

Since the SCIM coater became operational in May 1978, numerous coating runs have been made. These runs introduced us to a variety of problems, most of which have since been corrected. One problem that we found to be particularly troublesome from the outset was spillover of molten silicon as the substrate passed over the trough. This problem is illustrated in Figure 2. Initially, as shown in this illustration, solidification of the molten silicon did not occur until the layer was a substantial distance downstream of the trough. We reasoned that if we could create a steeper temperature profile in the solidification zone similar to that in dip-coating, and could produce more uniform temperatures along the trough, the spillover problem would vanish. Over the next few months we did bit-by-bit shift the solidification front upstream until we had the option of causing solidification to occur, if desired, at the downstream edge of the trough. Exercising this option, several runs were made using a variety of solidification conditions, but the spillover problem persisted.

To broaden our perspective of this problem, we consulted with Prof. L. E. Scriven (University of Minnesota) and Profs. J. Verhoeven and R. Trivedi of Ames Laboratories, Iowa State University. They basically agreed with the following proposed explanation of the basic problem with the present SCIM coater system. The problem is believed to arise from the combined effects of gravity and of surface tension gradients. The surface tension of any liquid decreases with increasing temperature, so that temperature gradients always produce surface tension gradients. These variations cause an unstable liquid meniscus in the SCIM geometry because gravity will cause the liquid to be thicker where the surface tension is weakest. Specifically, if the liquid becomes hotter in the center of the substrate, it will get thicker because the surface tension supporting the central region is the weakest. This thicker liquid at the center, therefore, must proceed further downstream in order to solidify (see Figure 3). The liquid-solid interface therefore becomes curved. As the growth front develops curvature, the transverse temperature gradients become more pronounced, producing a positive feedback on the tendency to thicken at the center, resulting in an unstable situation.

Since the meniscus is inherently unstable with respect to transverse temperature gradients, this problem would develop even if there were no initial transverse temperature gradients. The tendency to be cooled at the edges results from the increased radiation from the edges of the substrate. If the edges were purposely made hotter than the center, for example, the instability would presumably cause two thickened regions near the edges instead of one region near the center.

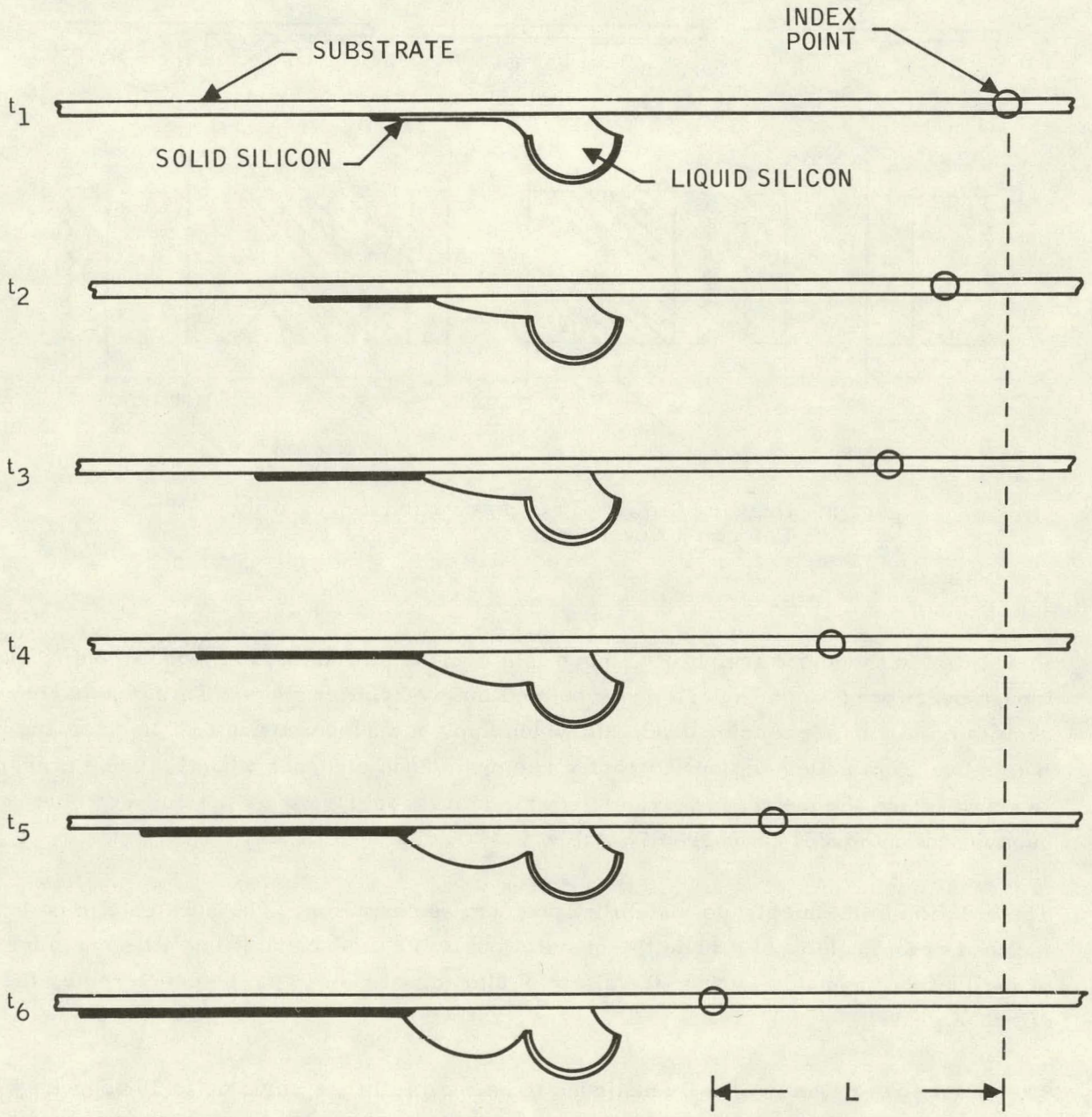


Figure 2. Illustration of Molten Silicon Spillover Problem in Relation to Coating Length, L

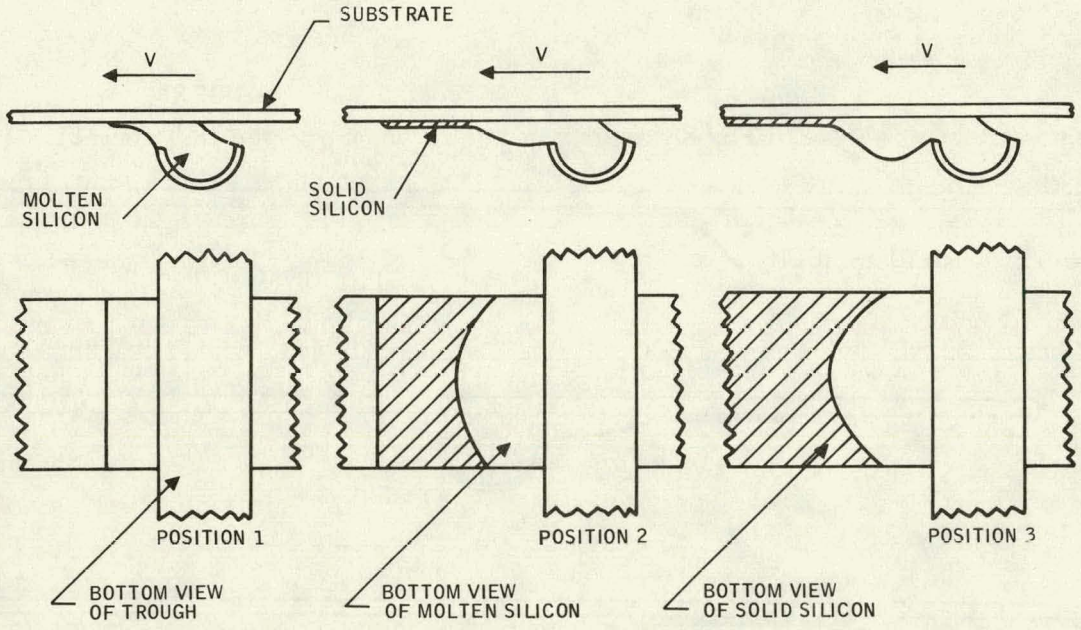


Figure 3. Drawing Showing Progressive Buildup of Molten Silicon Before Spillover Occurs

In addition to the above instability, there is a tendency for liquid to be drawn out of the trough because of Marangoni flow, as pointed out by Prof. Scriven. This type of flow results from surface tension gradients which apply a surface stress to a liquid, causing it to move from hotter regions to cooler regions. Such stresses will always be present in growth from the melt. In vertical growth, Marangoni flow does not cause problems because the meniscus is inherently stable.

The solution to the meniscus instability problem seems clear. The substrate must be inclined at an angle to eliminate the gravitationally induced instability. At some angle of inclination (probably slight), the effect of Marangoni flow would be countered by the effect of gravity.

The SCIM coater was originally designed to be inclined at an angle up to 30 degrees with minimal modification. This modification is presently being implemented. The SCIM coater, however, has been subjected to a number of minor modifications over the past several months and many of these modifications have reduced the efficiency of the insulation which originally surrounded each heating element. While the tilt modification is

being made, we are also updating, as needed, outmoded heaters and their surrounding insulation. While the modified parts are being machined, the coater will continue to operate, and we expect a minimal down-time while the new parts are installed.

Recent Coating Results -- In Quarterly Report No. 10, it was reported that control of the solidification position with respect to the trough had been achieved by using a new type integrated trough/substrate heating element. As shown again in Figure 4, the graphite trough holder was an electrically active leg of the heating element. Heating is very localized, permitting a sharp decrease in temperature downstream of the trough. The solidification location could then be controlled by the temperature setting of the upper substrate heater. Unfortunately, one end of the trough holder was attached to a water-cooled electrode. This introduced a substantial transverse temperature gradient along its length. To overcome this gradient, the heater assembly was modified so that the end of the trough was no longer attached to this cooled electrode. This was done, as shown in Figure 5, by locating one of the rectangular legs of the heater assembly below the trough holder and attaching this leg instead to the cooled electrode. The electrical resistance in this leg was tapered to produce a uniform temperature along its length in support of the trough holder.

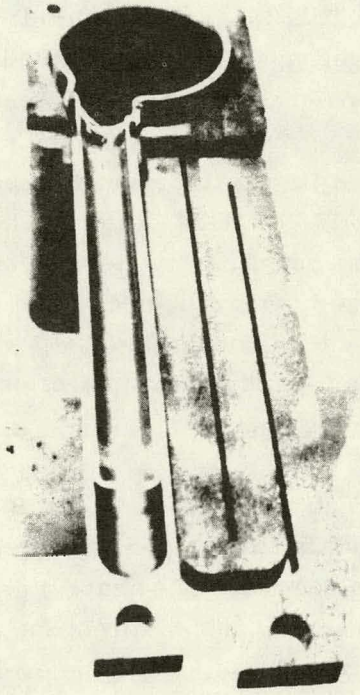


Figure 4. Photograph of New Trough/Substrate Heater (Also Showing Quartz Crucible/Trough Piece)

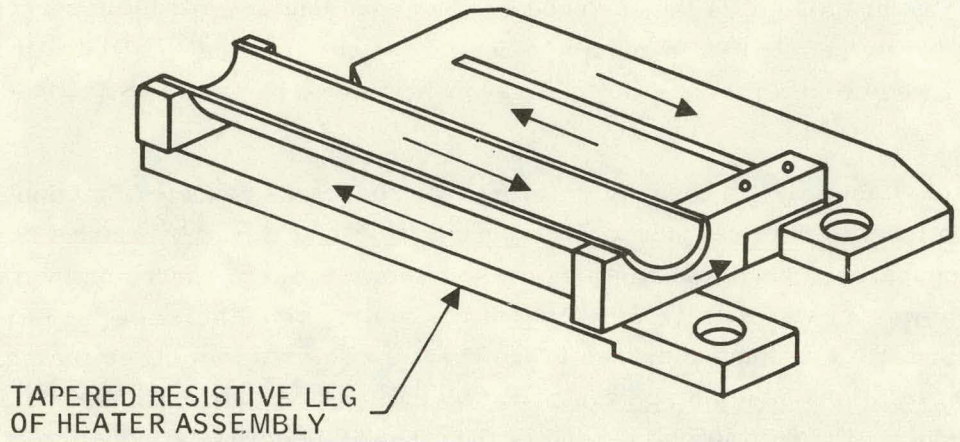


Figure 5. Drawing of Most Recent Trough/Substrate Heater Assembly for SCIM Coating Purposes

Using this latest heater configuration, four coating runs were made. The spill-over problem remained troublesome, but one run produced a coating with impressive large-grain crystalline structure. Figure 6 is a photograph of this coating. The grain structure cannot be seen in the photo, but it is very similar to that of dip-coated layers grown at similar velocities. There appears, in the photo, to be a discontinuity in the layer about midway in its growth. This is a slightly dimpled growth striation which is exaggerated by the photographic lighting. The photo also illustrates the previous description of how the growth front develops curvature before catastrophic spillover occurs.

While parts related to the 30-degree tilt modification are being constructed, top-coating experiments are being performed with the SCIM coater. The coater was temporarily adapted to allow molten silicon to be poured on the top surface of a carbon-coated substrate. The objective was to then pass this silicon covered substrate under a hot (≥1420°C) doctor blade for the purpose of controlling the thickness of the layer. Further downstream, the molten coating would then unidirectionally solidify to produce the columar grains common in dip-coating.

The design of the trough heater and doctor blade is shown in Figure 7. The doctor blade is a quartz-covered graphite rod and is heated by being a resistive element of the heater assembly. Figure 8 shows a cross section of the adapted growth chamber. As shown, a pouring spout was added to the quartz trough to direct the molten silicon onto the substrate. A quartz tray is provided to catch silicon in the event of spillage.

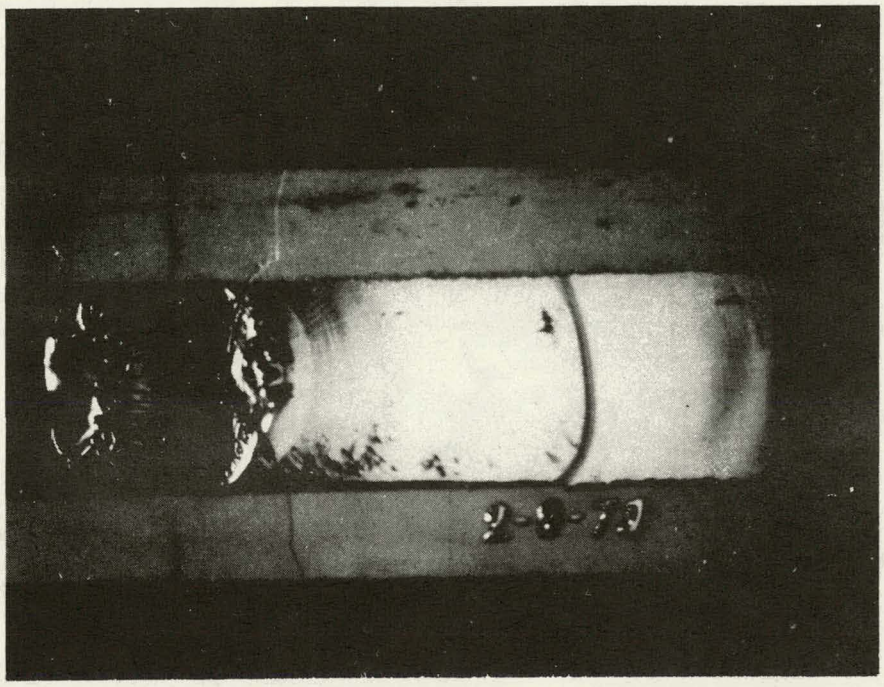


Figure 6. Photograph of Most Recent SCIM-Coated Silicon Layer

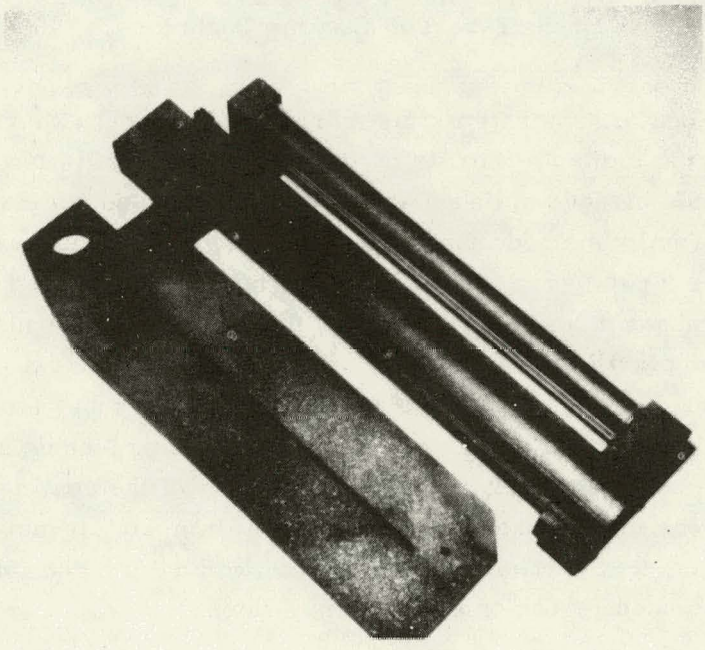


Figure 7. Trough/Substrate Heater Assembly Used for Doctor-Blade-Type Top-Coating Experiment

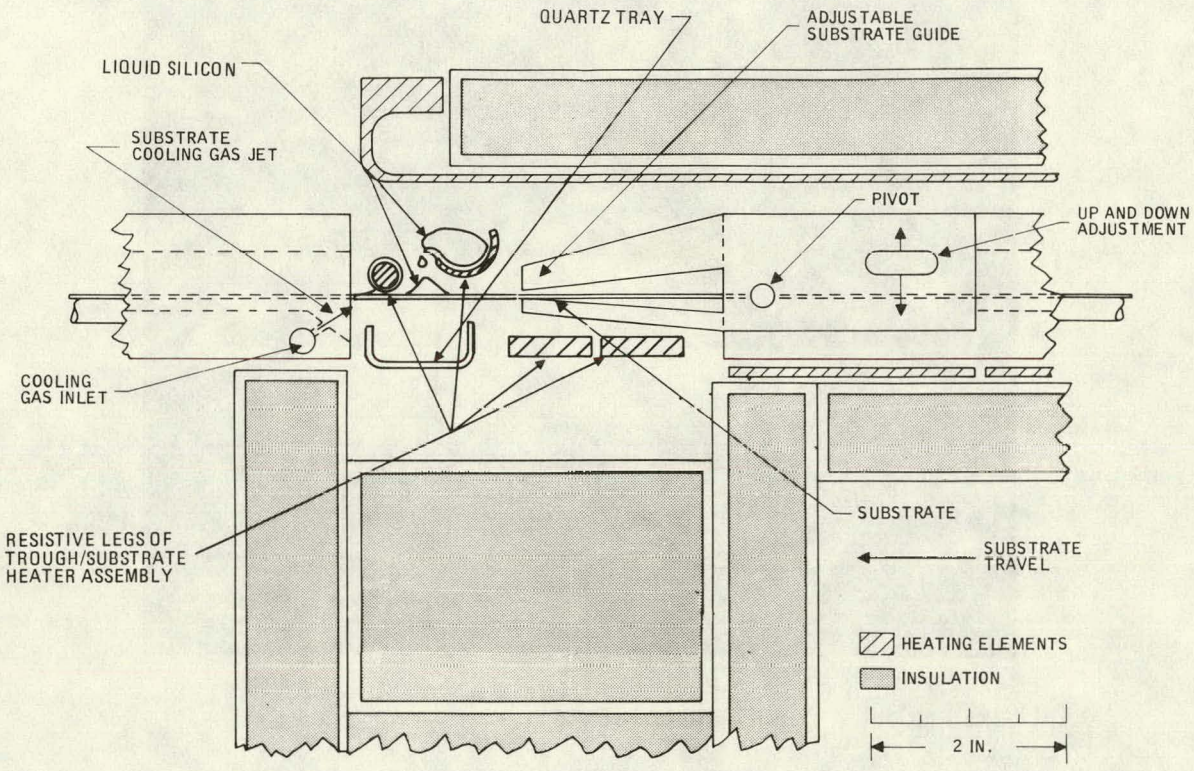


Figure 8. Growth Chamber Cross Section Showing Doctor-Blade-Type Top-Coating Technique

An attempt to top-coat a substrate in this manner was made, with encouraging results. As expected, pouring molten silicon is not trivial because of its large surface tension. Before pouring could be accomplished, a very high meniscus developed along the trough. When the pouring finally started, the quantity of silicon delivered was larger than desired. Figure 9 is a photograph of the coating attained in this attempt. This first attempt did reveal two significant positive factors: 1) the fact that even with an excessive amount of molten silicon applied to substrate, the excess of silicon did not flow outside the boundaries of the carbon coating. (The outermost edges of the substrate were not coated with carbon.) This implies that if we were to adopt this coating technique, uniform application of molten silicon is not likely to be a "fussy" part of the coating procedure. 2) While no attempt was made to keep the substrate in intimate contact with the doctor blade, nevertheless, that portion of the substrate which did make intimate contact produced a smoothly coated region of large-grain silicon.

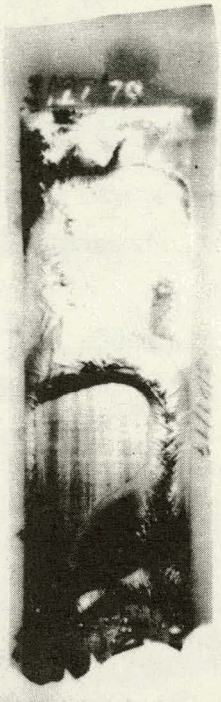


Figure 9. Photograph of First Doctor-Blade-Type Top-Coated Substrate

Future Continuous Coating Plans -- Alterations necessary to incline the SCIM coater are near completion. A number of improvements have been made within the coating chamber to facilitate rapid part substitutions for experimental purposes. These improvements will allow us to intermix experimental top-coating runs with inclined SCIM-coating runs.

During the next quarter, we will investigate the anticipated gravitational advantage of SCIM coating at angles up to 30 degrees above horizontal. In the near future, we also intend to investigate the top-coating potentialities of the method shown in Figure 10. This method proposes to coat the top surface of the substrate via a long, narrow slot in the bottom of the quartz trough. Calculations show that a slotted trough will contain molten silicon, providing a particular liquid level is not exceeded. In top-coating, this level can be temporarily exceeded until silicon contacts the carbon-coated substrate. Once contact has been made, we anticipate that the linear motion of the substrate will continue to draw silicon from the trough. Previous concerns about silicon creeping over the edges of the substrate have diminished now that we have observed that molten silicon does not overflow the carbon-coated areas.

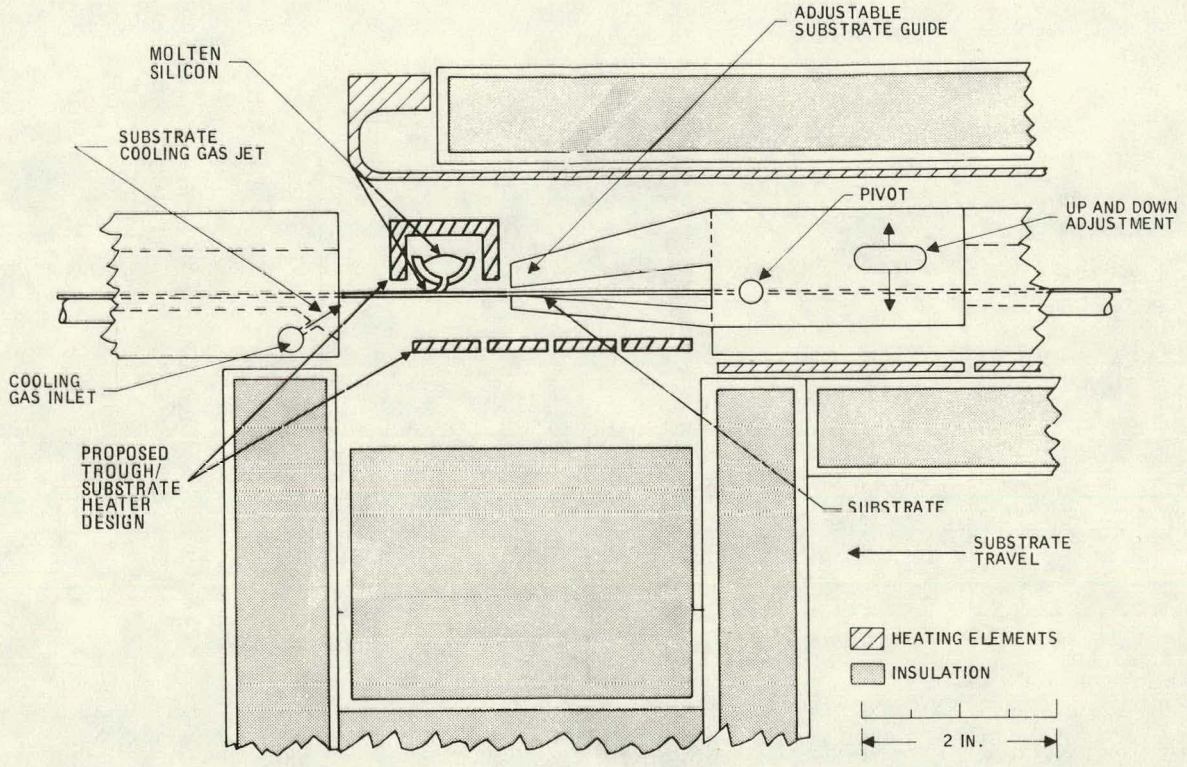


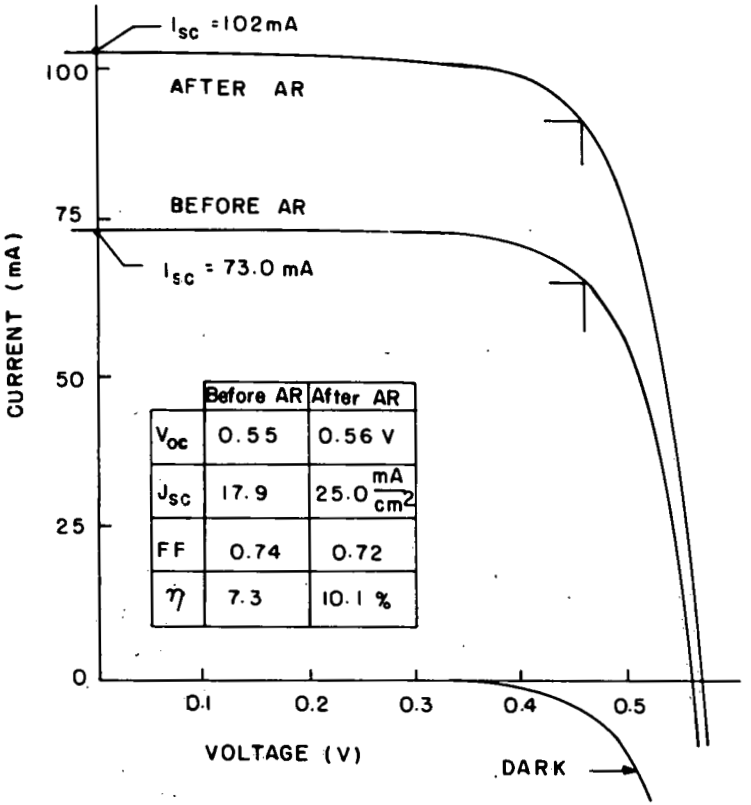
Figure 10. Growth Chamber Cross-Sectional Drawing of Proposed Top-Coating Technique

CELL FABRICATION AND DEVELOPMENT (B. Grung, T. Heisler, and S. Znameroski - Task II and Task VI)

Performance of SOC Cells

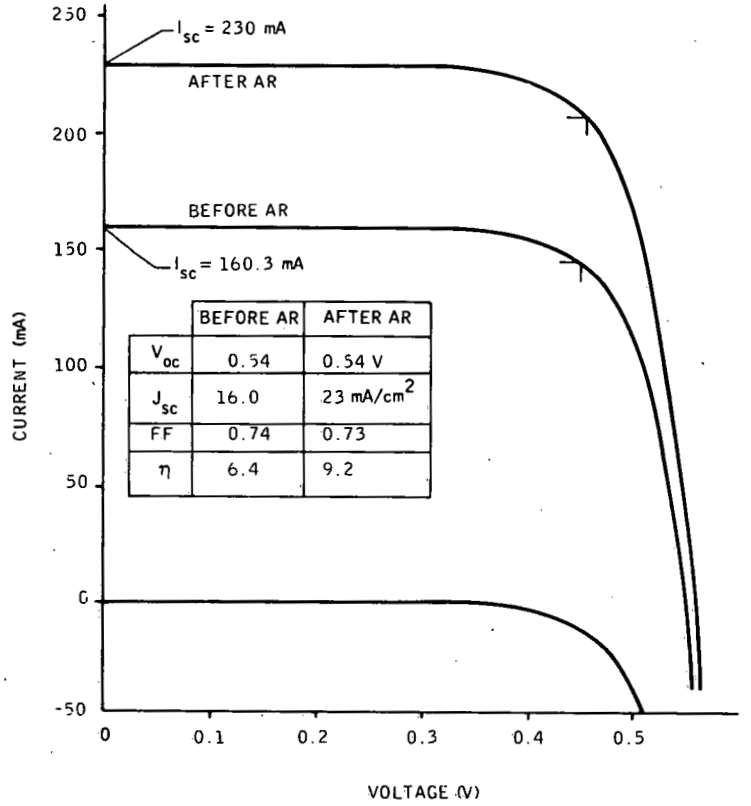
So far, the best SOC cell conversion efficiency is 10.1 percent (AM1, AR), for an area of 4.08 cm^2 Moreover, the best 10-cm^2 SOC cell conversion efficiency is 9.2 percent. The current-voltage characteristics of these two cells are given in Figures 11 and 12. An ELH lamp was used for all measurements and the reference cell was recently calibrated by JPL.

The 10.1 percent cell has an open-circuit voltage, V_{oc}, of 0.56 V, a fill factor of 0.72, a short-circuit current density, J_{sc}, of 25 mA/cm^2, and a metallization coverage of 10 percent. The latter two values give an active-area J_{sc} of 27.5 mA/cm^2, which is one of the highest values measured so far. In addition, the 10.1 percent cell has one of the highest values of V_{oc}, reflecting the high quality of the starting SOC material.



	Before AR	After AR
V_{oc}	0.55	0.56 V
J_{sc}	17.9	25.0 $\frac{mA}{cm^2}$
FF	0.74	0.72
η	7.3	10.1 %

Figure 11. Current-Voltage Characteristics of Slotted SOC Cell No. 160-2-102-1. Total area = 4.08 cm^2, metal coverage = 10 percent.



	BEFORE AR	AFTER AR
V_{oc}	0.54	0.54 V
J_{sc}	16.0	23 mA/cm^2
FF	0.74	0.73
η	6.4	9.2

Figure 12. Current-Voltage Characteristics of Slotted SOC Cell No. 156-11-103. Total area = 10 cm^2, metal coverage = 8 percent.

The 9.2 percent cell shown in Figure 12 has an area of 10 cm^2, a V_{oc} of 0.54 V, a fill factor of 0.73, a J_{sc} of 23 mA/cm^2, and a metallization coverage of 8 percent. The metal fingers are 0.02 cm wide and are spaced 0.25 cm apart. The cell has a length of 4 cm and a width of 2.5 cm. The SiO AR coating has a dark blue appearance, indicating low reflection of incident light. For the 9.2 percent cell, the AR coating increased J_{sc} by approximately 44 percent.

During the past quarter, a total of 51 SOC cells were completed and 39 of these were AR coated. In the future, this group of cells will be called the 1978 baseline cells, for two reasons: First, the characteristics of these cells are remarkably similar and can be used for future comparisons. Second, the cells were fabricated by nearly identical procedures and, as a result, statistically meaningful results can be derived. It should be noted here that most of the baseline cells were fabricated to evaluate the quality of the SOC material that is being delivered to JPL, for cell fabrication by OCLI. Thus, we intentionally completed a large number of cells without significantly changing our fabrication procedures.

For some cells the emitter-contact metallization process was slightly modified, as follows. Just prior to the Ni deposition, a thin (~500-Å-thick) layer of Ti was sputter deposited. This modification appears to improve the adhesion of the emitter metallization, as was expected. More important, the modification appears to increase the fill factor from about 0.72 to about 0.74. Theoretically, Ti should have the lowest contact resistance to n-type silicon. It also should reduce series resistance due to any possible oxide on the silicon surface. As a result of the improved performance, the Ti process step will be incorporated in our standard cell process.

The major characteristics of the 1978 baseline cells are given in Tables 1 and 2. Table 1 gives efficiency values and shows that the average efficiency for AR-coated cells is 8.6 percent, with a standard deviation of 0.7 percent. Except for five 10-cm^2 cells, each cell has an area of 4.08 cm^2. Table 2 gives more complete information on the 1978 baseline cells. Table 3 gives the corresponding information for recent single-crystal cells.

Statistical Analysis

Distribution diagrams for the 1978 baseline cells are given in Figures 13, 14, and 15. Figure 13 shows four diagrams for the baseline cells before AR coating. The upper left diagram is for the open-circuit voltage (V_{oc}) and the others are for the fill-factor (FF), the short-circuit current density (J_{sc}), and the conversion efficiency (η). Without AR

Table 1. Conversion Efficiencies of the 1978 Baseline Cells

Item	Cell No.	Area (cm^2)	Total-Area Conversion Efficiency, %	
			Before AR Coating	After AR Coating
1	143 12-102	4.08	5.0	6.1
2	143-12-201	4.08	5.8	7.7
3	143-13-102	4.08	6.0	9.2
4	143-13-201	4.08	6.5	9.0
5	144-04-102	4.08	6.1	8.3
6	146-06-102	4.08	5.6	9.6
7	146-06-201	4.08	5.2	7.8
8	147-07-102	4.08	4.5	x
9	148-07-101	4.08	6.2	x
10	148-07-202	4.08	6.9	x
11	148-08-101	4.08	5.9	7.9
12	148-08-202	4.08	5.7	7.8
13	148-15-102	4.08	4.4	x
14	148-16-102	4.08	5.4	8.1
15	148-16-201	4.08	6.4	7.7
16	150-14-102	4.08	6.9	9.0
17	151-10-101	4.08	6.3	8.3
18	151-10-202	4.08	6.6	8.4
19	151-13-102	4.08	7.3	8.7
20	151-13-201	4.08	6.6	9.0
21	151-14-102	4.08	6.0	8.2
22	151-14-201	4.08	6.3	8.6
23	151-15-101	4.08	6.5	8.5
24	151-15-202	4.08	5.9	8.2
25	156-02-101	4.08	6.5	8.7
26	156-06-103	10.00	6.6	9.2
27	156-11-103	10.00	6.4	9.2
28	156-12-102	4.08	5.6	7.9
29	156-12-201	4.08	5.7	7.9
30	160-02-102	4.08	7.3	10.1
31	160-02-201	4.08	6.5	9.4
32	160-05-102	4.08	6.7	9.2
33	160-05-201	4.08	6.5	9.1
34	160-09-103	10.00	6.3	8.9
35	164-01-103	10.00	6.6	9.1
36	165-01-101	4.08	5.4	x
37	165-01-202	4.08	5.5	x
38	165-14-103	10.00	5.4	x
39	168-08-101	4.08	6.5	x
40	168-08-202	4.08	5.2	x
41	416-01-101	4.08	6.6	8.8
42	416-01-202	4.08	6.8	8.9
43	416-01-302	4.08	7.1	9.4
44	416-06-101	4.08	6.8	8.9
45	416-06-202	4.08	6.6	8.7
46	416-07-101	4.08	6.5	8.7
47	416-07-202	4.08	6.8	9.5
48	416-08-102	4.08	6.2	8.1
49	416-08-201	4.08	2.1	x
50	416-09-101	4.08	4.7	x
51	416-09-202	4.08	5.8	x
		Average	6.0	8.6
		σ	0.9	0.7
		Number	51	39

Table 2. Characteristics of the 1978 Baseline Cells

Item	Cell No.	I_{sc} (mA)	V_{oc} (V)	Fill Factor	Total-Area Conversion Efficiency	
					J_{sc} (mA/cm^2)	η (%)
1	143-12-102-0	71.40	0.54	0.53	17.5	5.0
	143-12-102-1	92.00	0.55	0.50	22.6	6.1 (AR)
2	143-12-201-0	70.58	0.54	0.62	17.3	5.8
	143-12-201-1	92.30	0.55	0.62	22.6	7.7 (AR)
3	143-13-102-0	64.87	0.54	0.70	15.9	6.0
	143-13-102-1	93.00	0.55	0.74	22.8	9.2 (AR)
4	143-13-201-0	69.60	0.54	0.71	17.1	6.5
	143-13-201-1	95.00	0.54	0.71	23.3	9.0 (AR)
5	144-04-102-1	67.73	0.54	0.68	16.6	6.1
	144-04-102-1	96.70	0.55	0.63	23.7	8.3 (AR)
6	146-06-102-0	73.03	0.55	0.57	17.9	5.6
	146-06-102-1	96.10	0.55	0.74	23.6	9.6 (AR)
7	146-06-201-0	65.69	0.53	0.61	16.1	5.2
	146-06-201-1	91.60	0.54	0.65	22.5	7.8 (AR)
8	147-07-102-0	69.80	0.51	0.51	17.1	4.5
9	148-07-101-0	71.50	0.54	0.65	17.5	6.2
10	148-07-202-0	71.50	0.54	0.73	17.5	6.9
11	148-08-101-0	65.32	0.53	0.69	16.0	5.9
	148-08-101-1	88.10	0.54	0.68	21.6	7.9 (AR)
12	148-08-202-0	67.32	0.54	0.64	16.5	5.7
	148-08-202-1	93.00	0.54	0.63	22.8	7.8 (AR)
13	148-15-102-0	64.00	0.52	0.55	15.7	4.4
14	148-16-102-0	64.60	0.53	0.65	15.8	5.4
	148-16-102-1	88.50	0.54	0.69	21.7	8.1 (AR)
15	148-16-201-0	66.50	0.54	0.72	16.3	6.4
	148-16-201-1	89.60	0.54	0.65	22.0	7.7 (AR)
16	150-14-102-0	70.60	0.54	0.74	17.3	6.9
	150-14-102-1	88.80	0.55	0.75	21.8	9.0 (AR)
17	151-10-101-0	67.10	0.53	0.72	16.5	6.3
	151-10-101-1	88.20	0.54	0.70	21.6	8.3 (AR)
18	151-10-202-0	67.90	0.54	0.74	16.6	6.6
	151-10-202-1	87.50	0.54	0.72	21.5	8.4 (AR)
19	151-13-102-0	76.30	0.53	0.73	18.7	7.3
	151-13-102-1	93.90	0.54	0.69	23.0	8.7 (AR)
20	151-13-201-0	69.80	0.54	0.72	17.1	6.6
	151-13-201-1	93.00	0.55	0.71	22.8	9.0 (AR)
21	151-14-102-0	68.40	0.53	0.67	16.8	6.0
	151-14-102-1	93.00	0.54	0.67	22.8	8.2 (AR)
22	151-14-201-0	68.70	0.54	0.70	16.8	6.3
	151-14-201-1	94.50	0.54	0.69	23.2	8.6 (AR)
23	151-15-101-0	71.00	0.54	0.70	17.4	6.5
	151-15-101-1	95.60	0.54	0.67	23.4	8.5 (AR)
24	151-15-202-0	67.60	0.54	0.66	16.6	5.9
	151-15-202-1	95.20	0.55	0.64	23.3	8.2 (AR)
25	156-02-101-0	69.00	0.54	0.72	16.9	6.5
	156-02-101-1	91.20	0.55	0.71	22.4	8.7 (AR)

Table 2. Characteristics of the 1978 Baseline Cells (Concluded)

Item	Cell No.	I_{sc} (mA)	V_{oc} (V)	Fill Factor	Total-Area Conversion Efficiency	
					J_{sc} (mA/cm^2)	η (%)
26	156-06-103-0 }	163.00	0.54	0.74	16.3	6.6
	156-06-103-1 } 10 cm^2	236.00	0.54	0.72	23.6	9.2 (AR)
27	156-11-103-0 }	160.30	0.54	0.74	16.0	6.4
	156-11-103-1 }	230.00	0.54	0.73	23.0	9.2 (AR)
28	156-12-102-0	62.30	0.53	0.69	15.3	5.6
	156-12-102-1	89.50	0.54	0.66	21.9	7.9 (AR)
29	156-12-201-0	65.00	0.53	0.67	15.9	5.7
	156-12-201-1	91.00	0.54	0.66	22.3	7.9 (AR)
30	160-02-102-0	73.00	0.55	0.74	17.9	7.3
	160-02-102-1	102.20	0.56	0.72	25.1	10.1 (AR)
31	160-02-201-0	68.00	0.54	0.72	16.7	6.5
	160-02-201-1	98.00	0.55	0.71	24.0	9.4 (AR)
32	160-05-102-0	68.20	0.54	0.74	16.7	6.7
	160-05-102-1	95.70	0.55	0.71	23.5	9.2 (AR)
33	160-05-201-0	68.00	0.54	0.72	16.7	6.5
	160-05-201-1	96.70	0.55	0.70	23.7	9.1 (AR)
34	160-09-103-0 }	164.90	0.54	0.70	16.9	6.3
	160-09-103-1 } 10 cm^2	224.00	0.55	0.71	23.0	8.9 (AR)
35	164-01-103-0 }	174.30	0.55	0.69	17.4	6.6
	164-01-103-1 }	244.00	0.55	0.68	24.4	9.1 (AR)
36	165-01-101-0	69.00	0.52	0.62	16.9	5.4
37	165-01-202-0	69.70	0.53	0.61	17.1	5.5
38	165-14-103-0 } 10 cm^2	162.10	0.53	0.63	16.2	5.4
39	168-08-101-0	71.10	0.54	0.69	17.4	6.5
40	168-08-202-0	67.00	0.52	0.61	16.4	5.2
41	416-01-101-0	68.90	0.54	0.72	16.9	6.6
	416-01-101-1	97.50	0.56	0.67	23.9	8.8 (AR)
42	416-01-202-0	71.40	0.54	0.73	17.5	6.8
	416-01-202-1	100.00	0.55	0.66	24.5	8.9 (AR)
43	416-01-302-0	71.60	0.54	0.75	17.6	7.1
	416-01-302-1	98.80	0.55	0.70	24.2	9.4 (AR)
44	416-06-101-0	69.00	0.54	0.75	16.9	6.8
	416-06-101-1	90.90	0.54	0.74	22.3	8.9 (AR)
45	416-06-202-0	68.80	0.53	0.73	16.9	6.6
	416-06-202-1	90.80	0.54	0.72	22.3	8.7 (AR)
46	416-07-101-0	66.50	0.53	0.75	16.3	6.5
	416-07-101-1	93.30	0.54	0.71	22.9	8.7 (AR)
47	416-07-202-0	68.60	0.53	0.76	16.8	6.8
	416-07-202-1	97.70	0.55	0.72	24.0	9.5 (AR)
48	416-08-102-0	69.90	0.53	0.69	17.1	6.2
	416-08-102-1	94.80	0.54	0.65	23.2	8.1 (AR)
49	416-08-201-0	61.90	0.46	0.30	15.2	2.1
50	416-09-101-0	67.00	0.50	0.58	16.4	4.7
51	416-00-202-0	66.30	0.53	0.67	16.3	5.8

Table 3. Characteristics of Recent Single-Crystal Cells

Item	Cell No.	I_{sc} (mA)	V_{oc} (V)	Fill Factor	Total-Area Conversion Efficiency	
					J_{sc} (mA/cm^2)	η (%)
1	Q48A-00-102-0	86.09	0.57	0.79	21.1	9.4
2	Q48A-00-201-0	83.64	0.57	0.78	20.5	9.1
	Q48A-00-201-1	127.90	0.57	0.74	31.4	13.4 (AR)
3	Q48B-00-101-0	91.39	0.56	0.74	22.4	9.2
	Q48B-00-101-1	125.50	0.55	0.71	30.8	12.1 (AR)
4	Q48B-00-202-0	86.50	0.57	0.77	21.2	9.2
	Q48B-00-202-1	127.50	0.57	0.74	31.3	13.3 (AR)
5	Q51A-00-101-0	83.64	0.56	0.78	20.5	8.9
	Q51A-00-101-1	122.80	0.56	0.75	30.1	12.6 (AR)
6	Q51A-00-202-0	85.27	0.56	0.79	20.9	9.3
	Q51A-00-202-1	125.00	0.57	0.75	30.6	13.1 (AR)
7	Q51B-00-101-0	88.94	0.56	0.78	21.8	9.5
	Q51B-00-101-1	124.30	0.57	0.76	30.5	13.2 (AR)
8	Q51B-00-202-0	89.35	0.56	0.79	21.9	9.8
	Q51B-00-202-1	125.20	0.58	0.77	30.7	13.7 (AR)
9	Q52-00-102-0	89.80	0.56	0.79	22.0	9.7
	Q52-00-102-1	128.70	0.56	0.75	31.5	13.3 (AR)
10	Q52-00-201-0	86.40	0.55	0.76	21.2	8.9
	Q52-00-201-1	128.60	0.56	0.71	31.5	12.6 (AR)
11	Q56A-00-102-0	88.00	0.55	0.77	21.6	9.0
12	Q56A-00-201-0	88.70	0.54	0.77	21.7	9.0
13	Q58A-00-101-0	85.70	0.49	0.72	20.9	7.3
14	Q58A-00-202-0	88.60	0.51	0.70	21.7	7.6
15	Q58B-00-102-0	89.00	0.48	0.71	21.8	7.3
16	Q58B-00-301-0	90.60	0.48	0.70	22.2	7.5
17	Q60A-00-103-0 (10 cm^2)	233.00	0.56	0.78	23.3	10.1
	Q60A-00-103-1 (10 cm^2)	296.00	0.57	0.72	29.6	12.2 (AR)
18	Q60B-00-103-0 (10 cm^2)	227.00	0.56	0.75	22.7	9.5
	Q60B-00-103-1 (10 cm^2)	298.00	0.58	0.77	29.8	13.1 (AR)
19	Q62A-00-102-0	85.60	0.55	0.75	21.0	8.7
	Q62A-00-102-1	123.70	0.54	0.70	30.3	11.6 (AR)
20	Q62A-00-201-0	87.20	0.55	0.76	21.4	9.0
	Q62A-00-201-1	123.60	0.56	0.70	30.3	11.9 (AR)
21	Q62B-00-102-0	89.30	0.55	0.76	21.9	9.2
	Q62B-00-102-1	123.80	0.55	0.73	30.3	12.3 (AR)
22	Q64A-00-102-0	89.60	0.57	0.68	22.0	8.5
23	Q64B-00-103-0 (10 cm^2)	214.00	0.57	0.63	21.4	7.7
24	Q69A-00-101-0	88.70	0.56	0.76	21.7	9.2
25	Q69A-00-202-0	87.80	0.56	0.75	21.5	9.0

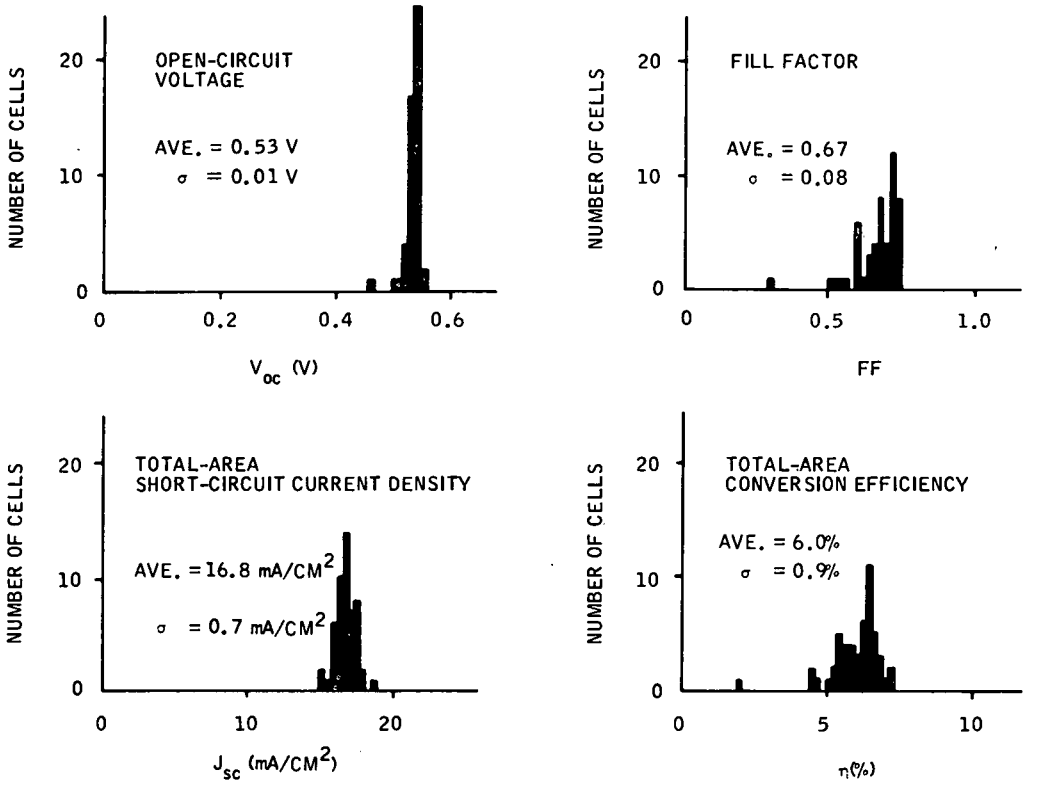


Figure 13. Distribution Diagrams for 1978 Baseline Cells Without AR Coating

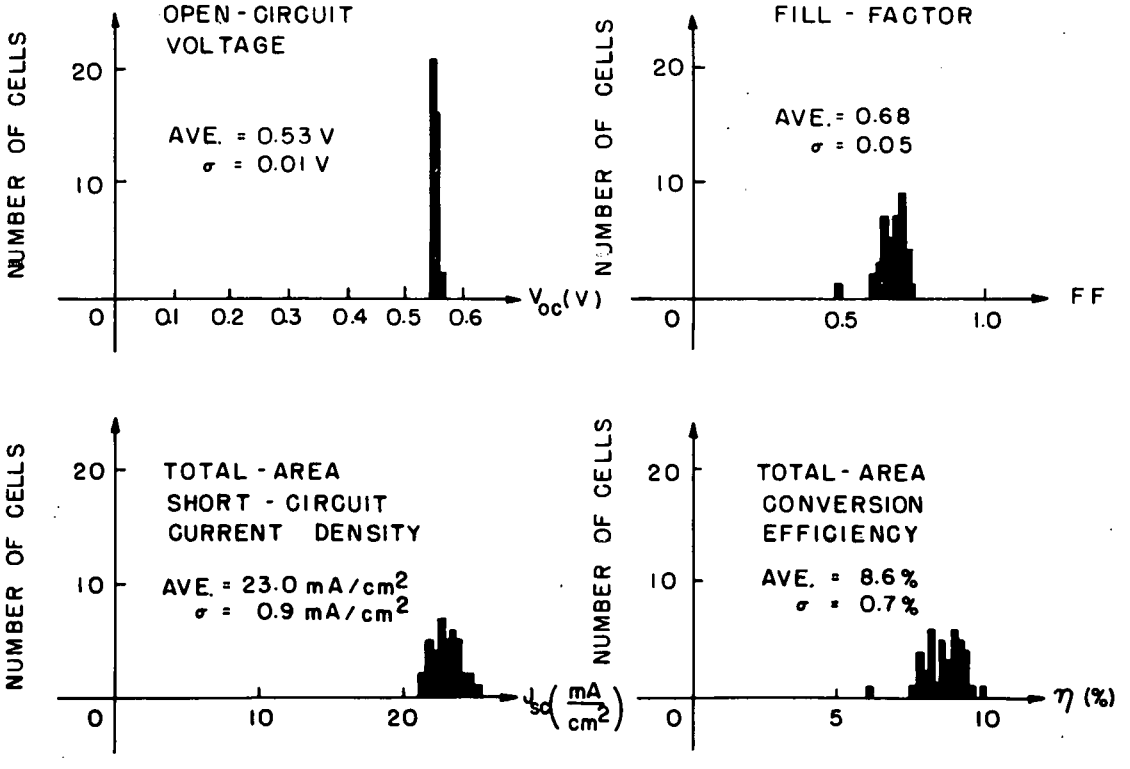


Figure 14. Distribution Diagrams for 1978 Baseline Cells After AR Coating

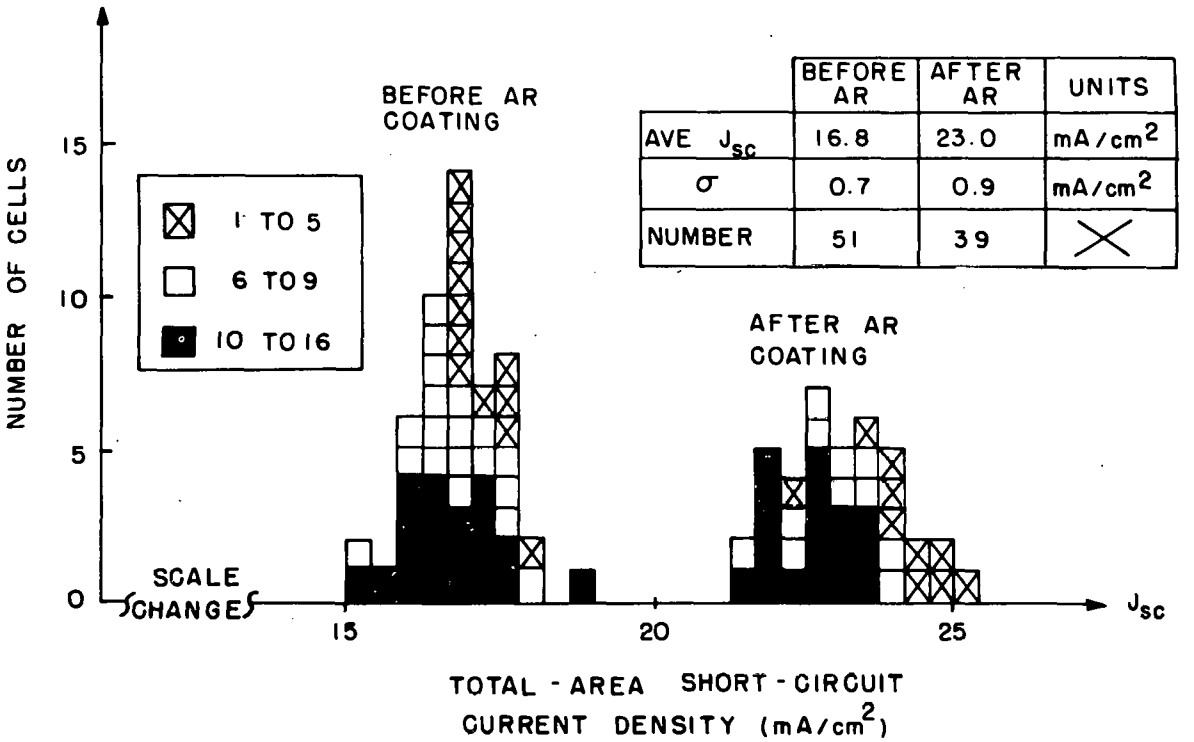


Figure 15. Distribution Diagram for the Short-Circuit Current Density Before and After AR Coating

coating, the baseline cells have: (1) an average V_{oc} of 0.53 V, with a standard deviation (σ) of 0.01 V; (2) an average FF of 0.67, with a σ of 0.08; (3) an average J_{sc} of 16.8 mA/cm^2, with a σ of 0.7 mA/cm^2; and (4) an average η of 6.02 with a σ of 0.9 percent. The efficiency values were in the range from 5.0 percent to 7.32 percent, after omitting the three lowest values.

Figure 14 shows four distribution diagrams for the AR-coated baseline cells. Average and standard deviation values are given in Table 4.

Table 4. Average, Standard Deviation, and Percent Variability Values for Baseline Cells with AR Coatings

Parameter	Average	Standard Deviation	Percent Variability
V_{oc}	0.53 V	0.01 V	4
FF	0.68	0.05	15
J_{sc}	23.0 $\frac{mA}{cm^2}$	0.9 $\frac{mA}{cm^2}$	8
η	8.6%	0.7%	16

The efficiency values are in the range from 7.7 percent to 10.0 percent, after omitting the lowest value of 6.1 percent. The last column in Table 4 gives the percent variability, which is given by dividing the variability by the average value and then multiplying the result by 100. The variability is defined as 2σ, where σ is the standard deviation. For the conversion efficiency, the percent variability if 16 percent, which demonstrates that we can obtain very repeatable results with our present fabrication methods. For the AR-coated baseline cells, about 95 percent of all efficiency values are within 16 percent of the average value of 8.6 percent.

For the short-circuit current density, the information given in Figures 13 and 14 is reproduced in Figure 15, which shows two peaks (one for cells without AR coating and the other for cells with). Each square corresponds to one of the cells given in Tables 1 and 2. As the figure indicates, the cells with dip numbers in the range from 1 to 5 are marked with a cross; those in the range from 6 to 9 are not marked; and those in the range from 10 to 16 are shaded. The figure clearly shows that the short-circuit current density decreases as the dip number increases. This decrease indicates that there is a correlation between cell performance and dip number.

The information shown in Figure 15 can be analyzed more quantitively by using linear regression. The result is an approximate relationship of the form

$$J_{sc} = A + BN \qquad (1)$$

where A and B are constants and N is the dip number. For the 1978 baseline cells, A = 23.9 mA/cm^2 and B = -0.11 mA/cm^2/dip. Thus, the average J_{sc} of cells with N = 1 is 23.9 mA/cm^2. As the dip number N increases, J_{sc} decreases at a rate of 0.11 mA/cm^2 per dip number. The constants A and B for J_{sc} are given in Table 5, along with the corresponding constants for V_{oc}, FF, and η.

Table 5. Linear Regression Constants for Baseline Cells With AR Coating

Parameter	A	B	r^2
J_{sc}	23.9 mA/cm^2	-0.11 (mA/cm^2/dip)	0.34
V_{oc}	0.55 V	-0.0006 (V/dip)	0.24
FF	0.700	-0.001/dip	0.02
η	9.10%	-0.07%/dip	0.20

The last column of Table 5 gives a number, r^2, which indicates the quality of fit achieved by the regression. Values of r^2 close to unity indicate a better fit than those close to zero. The quality of fit is best for J_{sc} and least for fill factor. In fact, the value of 0.02 indicates that there is no correlation between fill-factor and dip number, which is to be expected, since the fill factor is strongly dependent on the fabrication process and only weakly dependent on the material quality. The negative values given in column 3 for the B parameters indicate that the material quality decreases as the dip number increases.

Dark Characteristic Measurements

The dark characteristics of a number of recent SOC cells were measured during the reporting period to determine more accurately the series resistance. Curve fitting methods were employed to evaluate the experimental results. One example is given in Figure 16, which is for cell no. 143-13-102-1. This cell has a V_{oc} of 0.55 V, a J_{sc} of 23.5 mA/cm^2, a fill factor of 0.72, and an η of 9.3 percent, for a total area of 4.08 cm^2.

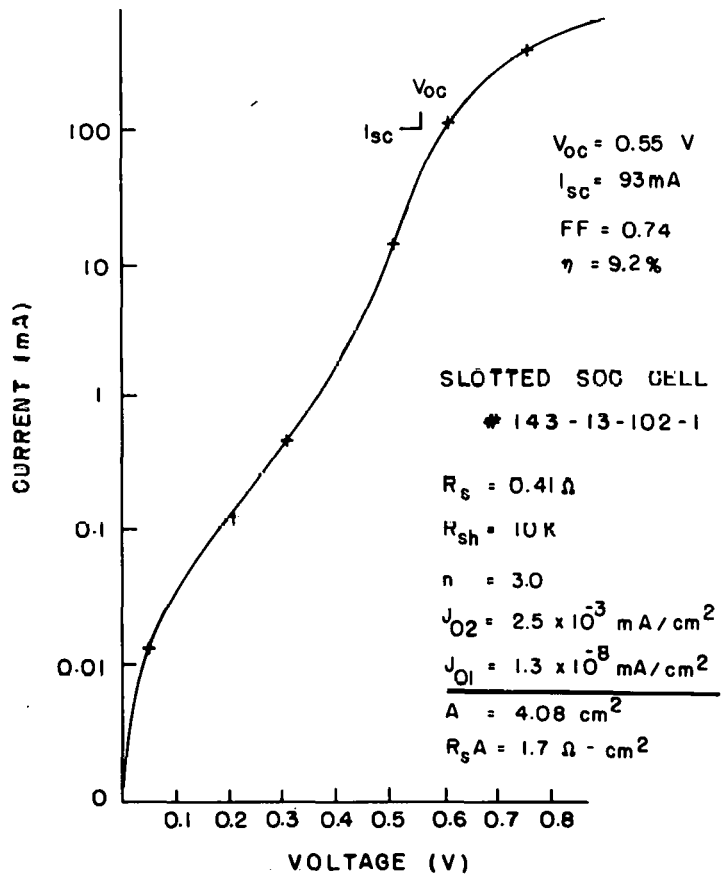


Figure 16. Dark Current-Voltage Characteristics of SOC Cell No. 143-13-102-1

The curve-fitting procedure is as follows. First, it is assumed that the well-known single-crystal solar cell equation is valid for the SOC cells; thus:

$$I = I_{01}\left\{\exp\left[\frac{q(V - IR_s)}{kT}\right] - 1\right\} + I_{02}\left\{\exp\left[\frac{q(V - IR_s)}{n\,kT}\right] - 1\right\} + \frac{V - IR_s}{R_{sh}} \qquad (2)$$

where I_{01} and I_{02} are saturation currents, R_s is the series resistance, R_{sh} is the shunt resistance, and n is a number in the range from 1 to about 4. For voltage values less than about 0.3 V, this equation becomes

$$I = I_{02}\left\{\exp\left[\frac{qV}{n\,kT}\right] - 1\right\} + \frac{V}{R_{sh}} \qquad (3)$$

Second, three voltage values are selected in the range for 0.05 V to 0.3 V and the corresponding current values are found from the dark curve. Each pair of current-voltage values is then substituted into Equation (3), giving three equations in three unknowns. Third, the three equations are solved for I_{02}, n, and R_{sh}, and the resulting values are substituted into Equation (2). Fourth, two voltage values are selected in the range from 0.5 V to 0.8 V and the corresponding current values are found from the dark curve. These two current-voltage pairs are then used with Equation (2) to give two equations in two unknowns. Finally, the two equations are solved for R_s and I_{01}. For the dark curve given in Figure 16, the resulting values are given in Table 6.

Table 6. Dark Curve Values for SOC Cell

Parameter	Value
I_{02}	10^{-2} mA ($J_{02} = 2.5 \times 10^{-3}$ mA/cm^2)
n	3.0
R_{sh}	10K ohms
I_{01}	5.2×10^{-8} mA ($J_{01} = 1.3 \times 10^{-8}$ mA/cm^2)
R_s	0.41 ohm ($R_sA = 1.7$ ohms cm^2)

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The best 2x-cell with concentration has a total-area conversion efficiency of 6.2 percent (AM1, AR), for a total area of 7.06 cm^2. The characteristics of this cell are given in Table 7, along with those of two other 2x-cells, one using SOC material and the second using single-crystal material.

Table 7. Characteristics of Recent 2x-Cells With Concentration

Cell	Section	I_{sc} (mA)	V_{oc} (V)	Fill Factor	J_{sc} (mA/cm^2)	η (%)
SOC cell no. 163-7	1	26.9	0.53	0.66	19.5	6.8
	2	28.9	0.54	0.64	20.9	7.2
	3	27.7	0.53	0.57	20.1	6.1
	4	27.3	0.53	0.61	19.8	6.4
	5	27.4	0.53	0.65	19.9	6.9
	All	137.7	0.53	0.60	19.5	6.2
SOC cell no. 136-13	1	22.4	0.48	0.60	16.2	4.7
	2	25.0	0.52	0.64	18.1	6.0
	3	23.0	0.52	0.66	16.7	5.7
	4	23.3	0.51	0.62	16.9	5.4
	5	23.6	0.47	0.56	17.1	4.5
	All	121.8	0.50	0.59	17.3	5.1
Single-crystal cell	All	206.0	0.55	0.55	29.2	9.1

Note: Each 2x-cell has a total area of 7.06 cm^2 and an active area of 3.70 cm^2.

MATERIAL EVALUATION (D. Zook and R. Hegel)

During the past quarter, evaluation of SOC material using the LBIC (light-beam-induced current) technique continued. This report describes our efforts to extend the technique to evaluate electrolyte cells, cells that have been AR coated, and cells that show appreciable shunting resistance. We have also found that the LBIC technique can be a valuable tool for identifying the causes of differences in short-circuit current due to cell processing. Results are summarized in Table 8.

Table 8. Diffusion Length Measurements by the LBIC Technique

Item	Cell or Substrate No.	AR Coating?	1 - R	L_n (μm)	$\pm\Delta L_n$ (μm)	Measurement Method	Comments
1	130-14-01	No	0.70	21.5	1.5	D-C current	
2	130-14-02	No	0.84	23.0	0.5	D-C current	
3	130-14-06	No	0.75	27.3	0.7	D-C current	
4	130-14-07	No	0.91	32.2	2.8	D-C current	
5	130-14-09	No	0.76	27.2	3.1	D-C current	
6	135-8CJH	No	0.73	20.3	2.3	D-C current	
7	95-4A-05	No	0.85	20.3	1.5		
8	141-6CKH	No	0.69	33.0	4.5	A-C electrolyte	Over slot
9	141-6CKH	No	0.50	50.2	9.7	A-C electrolyte	Over ceramic
10	142-3CKH	No	0.68	43.8	5.7	A-C electrolyte	Over slot
11	142-3CKH	No	0.80	29.6	5.3	A-C electrolyte	Over ceramic
12	143-13-A	Yes	0.99	32.3	0.9	D-C voltage	
13	143-13-D	Yes	0.94	19.9	1.8	D-C voltage	
14	143-5-A	Yes	0.78	38.9	3.5	D-C voltage	SSEC processed
15	143-5-B	Yes	0.89	25.5	1.5	D-C voltage	SSEC processed
16	416-1T-C	No	0.76	73.4	8.3	D-C voltage	Highest L_n measured on SOC material
17	416-7-A	No	0.72	27.6	2.0	D-C voltage	
18	151-13-D	Yes	0.92	28.9	1.8	D-C voltage	
19	TSS-038	Yes	0.93	138.1	14.0	D-C voltage	JPL standard cell with glass slide overcoat

Electrolyte Techniques

The electrolyte technique has only been partially developed to date. The signal-to-noise ratio has not been adequate for good cell scans. However, L_D measurements within grains have been made using a large spot size (~ 100 μm dia.). The cell fabrication procedure is very simple as shown schematically in Figure 17. The cathode material is in the form of a thin platinum foil with a hole a few millimeters in diameter to admit the incident light. The cathode is cemented to a glass cover and an O-ring is used to contain a few drops of electrolyte. The semiconducting photoanode is then clamped in place on the O-ring.

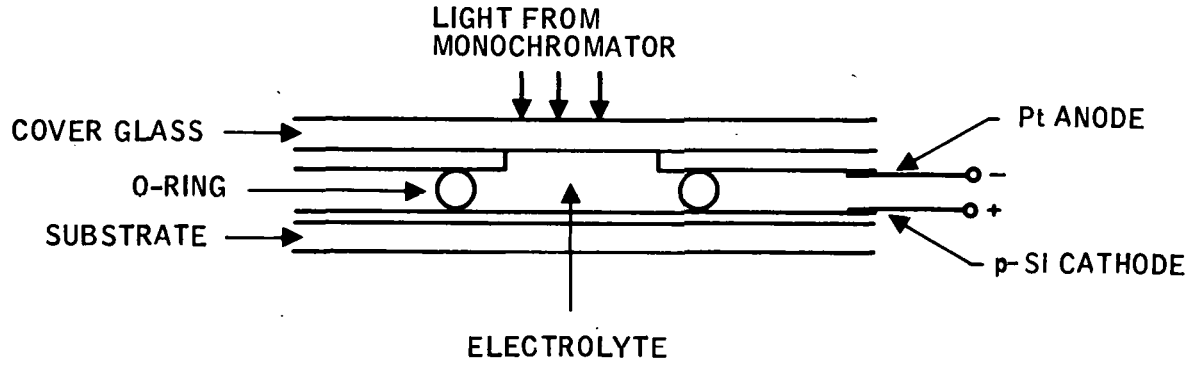

Figure 17. Photovoltaic Electrolyte Test Cell Configuration

We found that p-type silicon generally does not form a good Schottky barrier with any electrolyte. We have therefore used these cells in a photoconductive mode with an applied bias. The bias makes it necessary to use chopped light to separate the signal from the d-c bias current. The best electrolyte found to date has been a 0.1M solution of $EuCl_2$. The d-c bias on the cell is varied to produce the largest signal (as seen on an oscilloscope) across a 100K ohm lead resistor. The signal was compared to that produced by the calibrated photodiode to obtain a spectral quantum efficiency.

Methodology

We have noticed that in the electrolyte method, as well as in the p-n junction photodiode method, there appears to be systematic errors. The possible sources of errors are:

- Values of α_λ (absorption coefficient) obtained from the literature
- Values of R_λ (reflectivity) also from the literature
- Calibration errors of the comparison photodiode
- Wavelength calibration errors of the monochromator

The systematic errors appear as inconsistencies in the usual way of interpreting the data. Examination of the sources of error showed that the most likely problem was the value of R_λ. Certainly with the electrolyte method the literature value of R_λ is not correct because of the presence of the quartz and of the electrolyte. With AR-coated cells, there is also uncertainty in the value of R_λ. We have found an improved method of deducing a

diffusion length from the data that gives more consistent values of L_D. Briefly, the reflectivity, R_λ, is regarded as an unknown constant, R, for each sample, and the value of R is chosen to give the best fit to the data.

All the techniques for deducing L_n from spectral response data depend on the well-known formula for the spectral quantum efficiency:

$$S_\lambda = \frac{(1 - R)\,\alpha_\lambda L_n}{1 + \alpha_\lambda L_n} \tag{4}$$

where R is the reflectivity and α_λ is the absorption coefficient taken from the literature. The formula is valid in the long-wavelength limit. The usual method relies on a plot of S_λ^{-1} versus α_λ^{-1} and on a published value of R. The systematic error appears as an inconsistency in the value deduced from the slope and the value deduced from the intercept.

The new approach we have used for deducing the value of L_n is as follows. An initial guess is made for the value of 1 - R. Each data point (value of S_λ) is then used to calculate a value of L_n by solving the above equation for L_n:

$$L_n = \frac{\alpha_\lambda^{-1}}{1 - R/S_\lambda^{-1}} \tag{5}$$

The values of L_n are then averaged to obtain a value $\bar{L}_n$ and a standard deviation δL_n. The value of R is then varied to give the least relative error, $\delta L_n/\bar{L}_n$. It is interesting that this procedure gives very reasonable values of 1 - R for AR-coated cells as well as non-AR-coated cells, as shown in Table 8.

A second type of systematic error can also be checked with this technique. If there were no systematic errors in the values of α_λ used, the deviations of the individual values of L_n from the average $\bar{L}_n$ would be random. We have looked for a pattern in the deviation by calculating the value of α_λ^{-1} that would have given a perfect fit to the data and listing the relative differences between these values and the literature values used in the calculation. The values from the literature that are most controversial (because they depend on sample preparation, etc.) are the longest wavelength values. We used the values of Runyan,[1] and find that for most of the samples, larger values of α_λ^{-1} would have fit the data better.

[1] "Minority Carrier Diffusion Length in Silicon . . .," ASTM Standard F391-73T (1973).

Generally, we find that AR-coated photodiodes and solar cells have lower shunt resistances than uncoated cells. With our normal procedure, a low value of R_{sh} would make the measurement impossible because of the current offset in the electrometer. One method to overcome the shunting problem would have been to use chopped light and the a-c technique. But, because of phase noise in the lock-in amplifier, this technique has not been as sensitive as the d-c technique.

We have found that the d-c technique can easily be used with "leaky" cells by using a Keithley digital multimeter instead of an electrometer across the cell. The resistance mode of the multimeter is used to measure the actual shunt resistance, R_{sh}. The multimeter is then used in the microvolt mode with the analog output connected to the chart recorder to record LBIC scans. The output is then reduced to current by dividing the voltage value by R_{sh}. For example, suppose R_{sh} = 10K ohms. With the electrometer in the current mode, the offset current is greater than 10^{-9} A when R_{sh} = 10K and the offset current tends to be noisy. In the voltage mode, a signal of 1 nA would give a voltage of 10 μV. We find that the measurement limit is about 1 V, corresponding to 10^{-10} A. This is adequate for diffusion length measurements at 1 sun (30 mA/cm^2), since a 3-μm-diameter high spot gives a current of $3.\ 10^{-9}$ A, or 30 μV. Since many large cells have R_{sh} values in the 10K ohm range, it is possible to make LBIC scans and measure L_n with high spatial resolution in 10-cm^2 cells.

During the past quarter, a number of SOC solar cells were fabricated at Honeywell's SSEC. These cells showed a significantly lower short-circuit current than cells made at Honeywell's CMSC with our standard process. It was of interest to see if the LBIC technique could be used to determine the reason for the lower current values. The cells being compared were AR-coated and had a significantly lower shunt resistance than the cells we had selected for evaluation previously, so that the voltage mode was used.

The spectral response of an SSEC cell and a CMSC cell are compared in Figure 18. The spectral response, as well as the values of L_p, show that the differences in I_{sc} are not due to differences in L_p. It should be noted that values of 1 - R deduced from the six data points used for the L_D determination are consistent with the peak response observed in the visible. The conclusion is that the SSEC processing has resulted in a loss of light at the surface of the cell, since it affects all wavelengths equally. Visually, the cells appear identical, so the differences are not due to light scattering or to thickness of the AR coating.

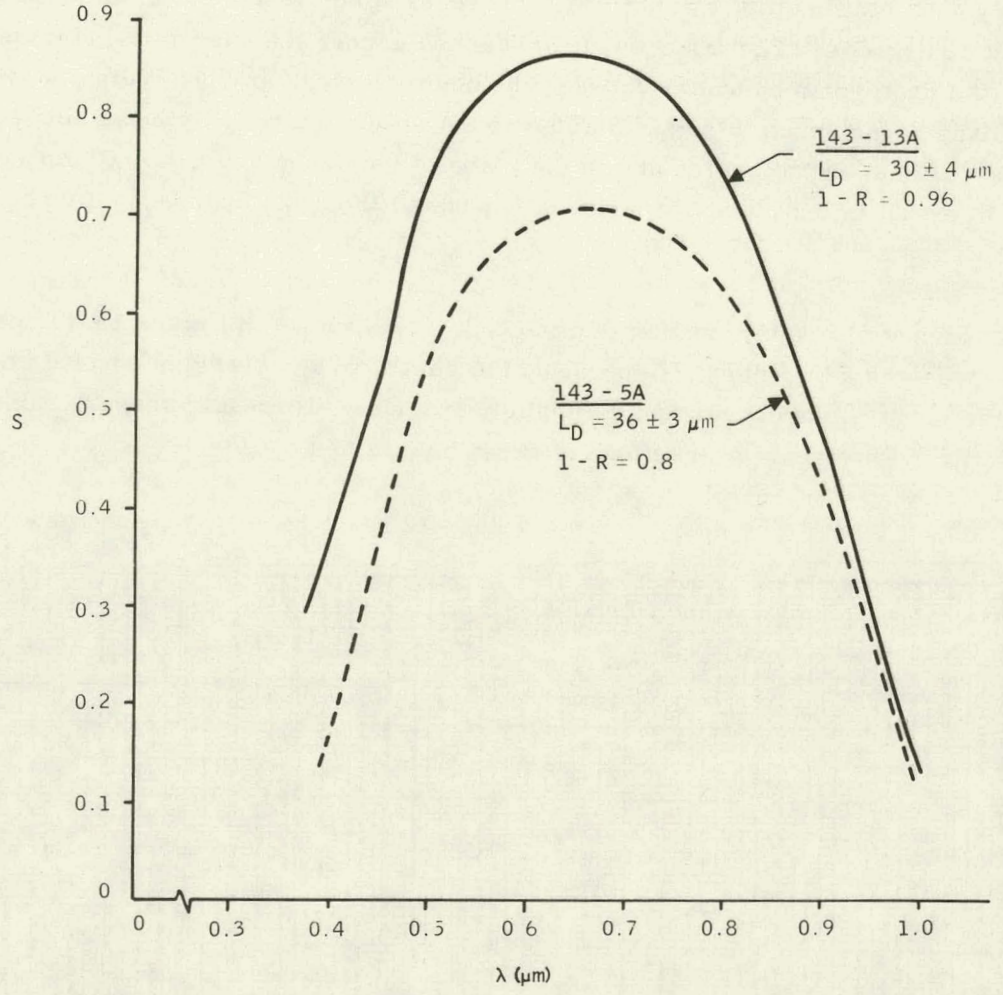

Figure 18. Spectral Response of an SSEC Cell (No. 143-5A) and a CMSC Cell (No. 143-13A). Both cells were AR coated.

The main difference in processing was the application of the top metallization. At SSEC, the metallization was applied using conventional integrated-circuit technology. The metal was evaporated onto the entire surface, and the excess was then removed. At CMSC, the photoresist was applied first, so that metal only contacted the surface at the electrode areas. It is not entirely clear why the differences in processing produced the observed differences in efficiency, but at least the LBIC technique identified the specific mode of degradation.

Grain Size Distribution Measurements

One of the goals of our materials evaluation efforts this year is to develop a simple but viable method of evaluating grain size distributions and correlating these with the growth conditions. During the reporting period, we set up a very simple system which seems quite promising.

In the experimental setup, a He-Ne laser is focused on the sample at an angle of incidence of about 45 degrees. The laser beam is scanned across the sample using a mechanical stage. As each grain boundary crosses the beam, a large amount of light is diffracted. If the plane of incidence is perpendicular to the predominant grain boundaries, the diffraction patterns of the grains are in the plane of incidence and a large amount of light can be detected in the plane of incidence separated from the undiffracted (specularly reflected) light.

A typical trace of a 7-mm region of an SOC layer is shown in Figure 19. Each sharp peak represents a boundary. Generally, the small peaks correspond to twin boundaries, while the large peaks correspond to grain boundaries. However, there is not a complete correlation with visual observations of grain boundaries.

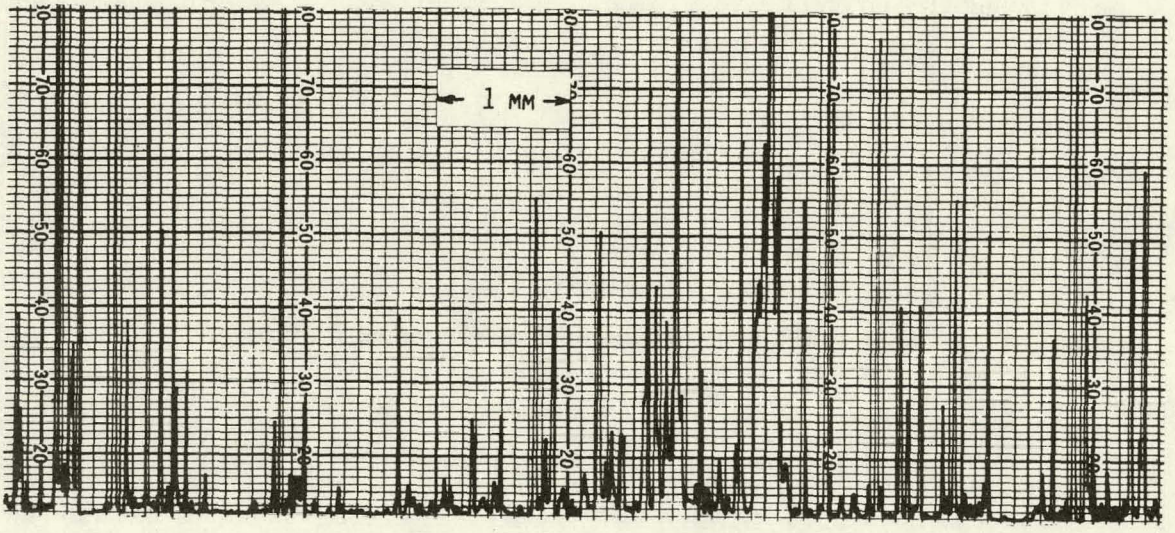

Figure 19. Scattered Laser Light from As-Grown SOC Surface. Conditions: 10-μm spot size, 45-deg angle of incidence, 0-deg scattering angle.

The procedure looks quite promising and work will be continued. A scan can be performed in a minute or two, so that it would be quite feasible to do several scans on every substrate as soon as it is cleaned. If the peak data can be automatically processed to yield a grain size distribution, we would have a valuable tool to evaluate crystalline quality.

CONCLUSIONS AND RECOMMENDATIONS

CONCLUSIONS

From work performed during the quarter, we conclude that:

- The production dip-coating facility is capable of high yield coating of solar cell quality substrates.
- Slotted substrates can be carbon coated easily and successfully using a roller method.
- Water cooling of the cooling shoes in the experimental dip coater is not adequate for fast growth. Gas cooling must also be employed.
- Temperature gradients along the trough of the SCIM coater contribute to a meniscus instability inhibiting our ability to coat continuously.
- Top-coating of the substrate using a doctor-blade technique is able to produce a smooth area of large-grain silicon.
- By using our "standard" slotted-cell processing techniques we can produce cells having a narrow range of performance parameters.
- Successive dip-coated samples show a deterioration of J_{sc} equal to $-0.11\ mA/cm^2$ per dip.
- The shunt resistance of a typical SOC cell is 10K ohms.
- The series resistance in slotted SOC cells is 0.4 to 0.5 ohm, indicating the slotted pattern is not unduly penalizing our cell performance.
- The LBIC technique is useful in measuring L_D within grains on SOC material using electrolyte contacts.
- The LBIC technique can be used for identifying the causes of differences in short-circuit current due to cell processing.

RECOMMENDATIONS

To date, we have been attempting to fabricate 2x concentrator cells to investigate the feasibility of a nonslotted approach to high SOC cell performance. Our experimental activity has lead to cells with high series resistance. We therefore recommend de-emphasizing the experimental aspects of nonslotted cell approaches in favor of a more rigorous analytical investigation of this topic.

PROJECTION OF FUTURE ACTIVITIES

Future activities are projected as follows:

- Work will continue in the production dip-coater with emphasis on providing optimum base doping and thinner layers for cell fabrication.
- The experimental dip-coater will run a series experiments with the new cooling shoes in place, leading to useful layers pulled at from 0.2 to 0.3 cm/sec.
- The SCIM coater will be used to coat substrates at an angle up to 30 degrees with the horizontal. Top-coating of substrates will also be carried out using various trough/crucible schemes.
- Slotted-cell fabrication steps will be modified to provide improved overall performance.
- Analytical studies of nonslotted geometries will be initiated in an attempt to identify the most cost-effective structures.
- "Thin" SOC slotted cells will be fabricated to learn what impact thickness has on cell performance.
- The electrolyte LBIC technique will be refined to provide predevice screening of our SOC material.
- LBIC work will also continue in an attempt to correlate L_D with different growth rates (i.e., grain size) and impurity content.

NEW TECHNOLOGY

There were no reportable "New Technology" items uncovered during this reporting period.

PROGRAM STATUS UPDATE

Updated versions of the Program Plan, Program Labor Summary, and Program Cost Summary are presented in Figures 20, 21, and 22, respectively.

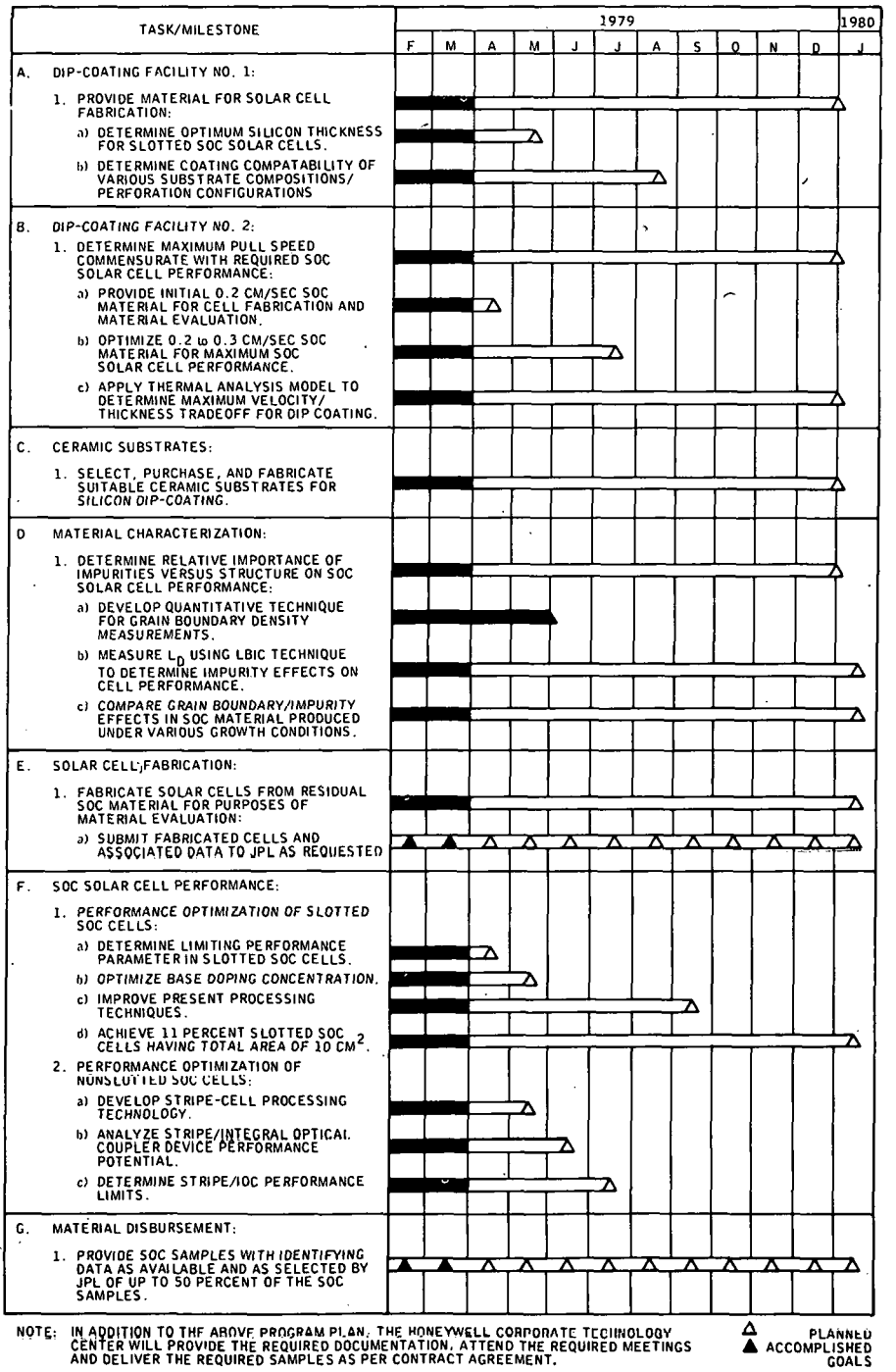

Figure 20. Updated Program Plan

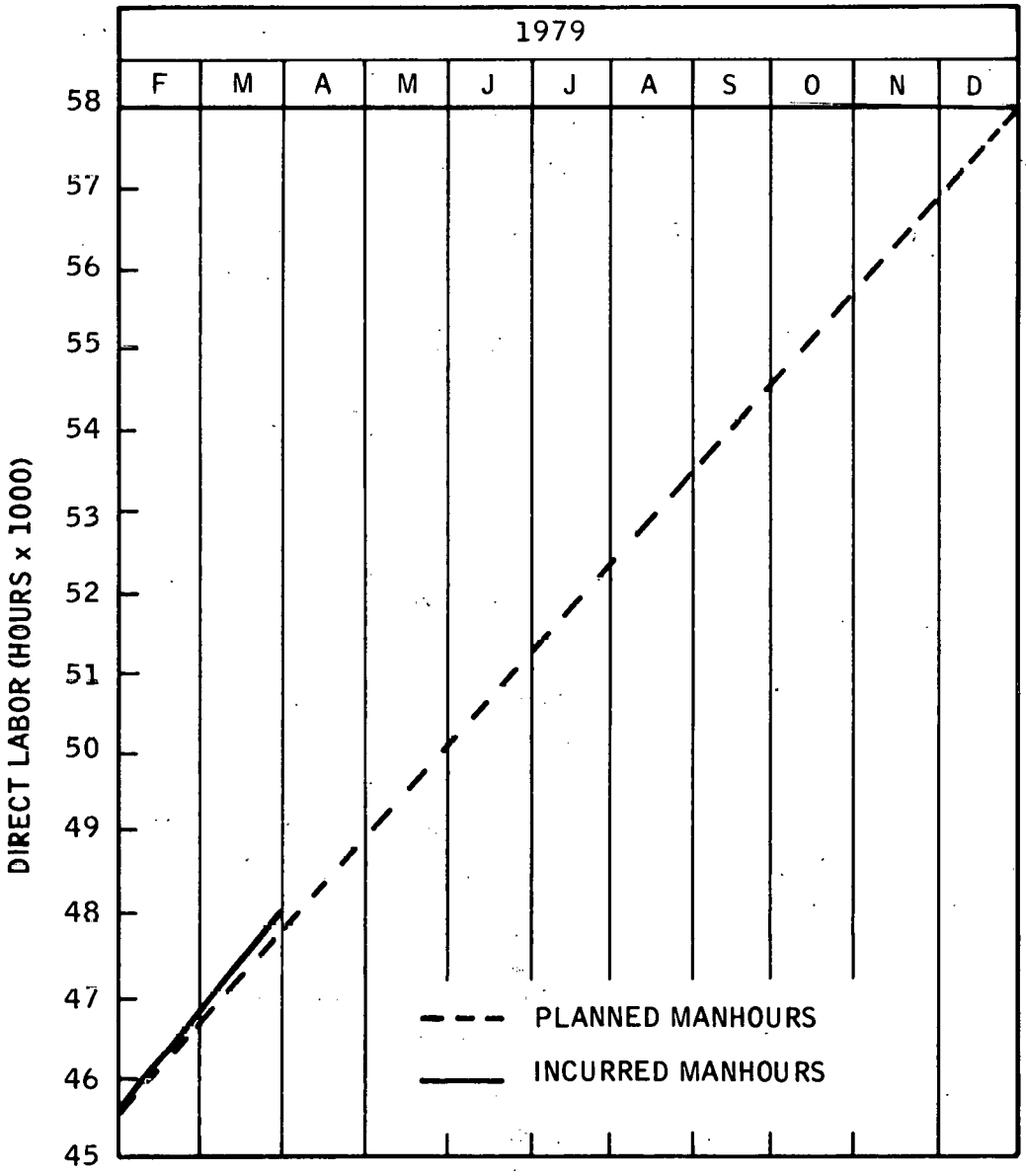

Figure 21. Updated Program Labor Summary

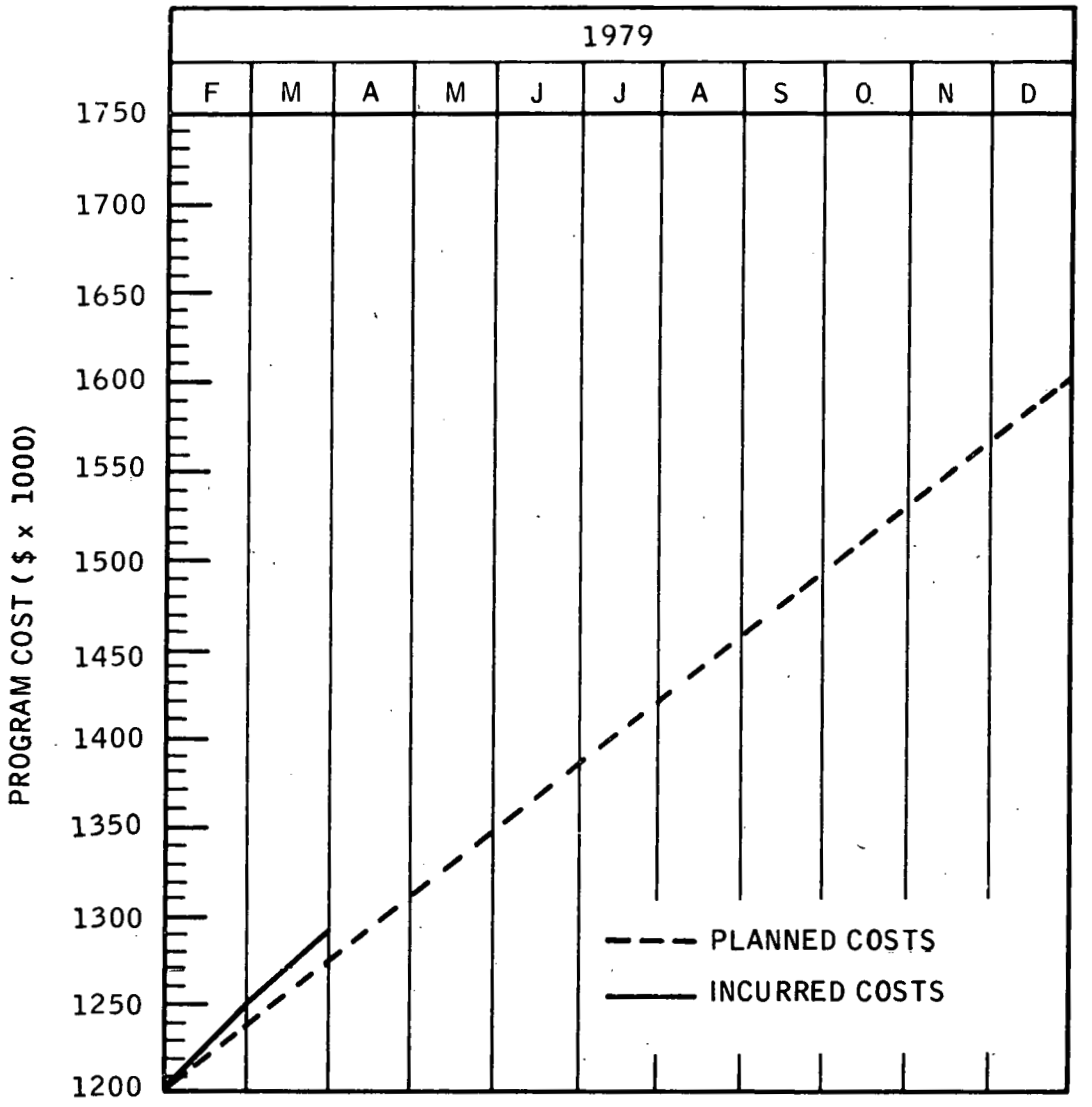

Figure 22. Updated Program Cost Summary

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