CONF-890846--1

SAND--88-3442C

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7-OCT-88 13:13:00

Electrical Measurements for CMOS IC Stuck-Open Faults

Jerry M. Soden, R. Keith Treece,
Michael R. Taylor and Charles F. Hawkins

Abstract - Two incidences of IC failure due to the CMOS stuck-open fault are reported here. The voltage levels, quiescent power supply current(I_{DDQ}), transient response, and tester properties associated with these defects are reported. The transient response of the defective node voltage and power supply current to the high impedance state caused by these defects was measured to determine if the I_{DDQ} measurement technique could detect stuck-open faults. The results show that the I_{DDQ} technique does detect stuck-open faults in some designs, but detection is not guaranteed for all circuits. Modifications to the circuit layout to reduce the probability of the stuck-open fault occurrence are presented.

I. INTRODUCTION

The CMOS stuck-open fault is a failure mechanism associated with loss of charge transfer capability in one of the transistors in a CMOS combinational logic circuit. This fault causes a high impedance or floating node at the output terminal for one of the logic states. For example, the 2-NOR shown in Figure 1 exhibits the stuck-open fault response if the marked location represents a defective open circuit. Activation of transistor MN_1 and inactivation of MN_2 removes active pull down to the output node. If AB=10, then the output drain node is put into a high impedance state with the drain voltage remaining that of the previous logic state.

Detection of this failure mechanism requires a sequence of two test vectors; the first test vector called an initializing input (T_1) pattern charges the output node to a voltage opposite to that expected when the defective transistor is turned-on. The second vector is called the test input (T_2) pattern whose purpose is to evaluate the presence of a stuck-open fault. The defect in Figure 1 is only detected if the test vector pair AB=00 is followed by AB=10. A full binary up count test vector sequence will not detect this defect. A stuck-open fault can also occur if the open circuit appears in the path of the series transistors. If this occurred in

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one of the p-channel transistors in Figure 1, then the node would never be pulled high. A memory fault is possible in this case if the node initially powered up in a high logic state.

Figure 1. 2-NOR logic gate showing an open drain defect location.

The CMOS stuck-open fault was first reported by Case and described in more detail by Wadsack[1,2]. A major emphasis since then has been on development of automatic test generation for the CMOS stuck-open fault in combinational logic circuits[2-11]. Detection of the stuck-open fault is made more difficult because certain CMOS circuits configurations introduce hazards due to differential timing delays that can upset the correct initializing pattern[4-11]. The properties of stuck-open faults in sequential circuits have been reported[3,12]. It was concluded that many faults in sequential circuits may not be detectable without special clocking and parametric tests such as rise and fall time measurements, or without redesigned circuits.

In contrast to this activity, the actual existence of the stuck-open fault was not reported until 1987 when Woodhall, et. al., tested 4552 ICs that had 616 potential and distinct stuck-open sites per die[13]. Stuck-at and stuck-open test sets having 100% coverage were used to differentiate the presence of stuck-open faults. Forty-four die had one or more stuck-open faults and of these, 40 die were detected by a stuck-at test set. The stuck-open escape rate using a stuck-at test set with 100% coverage was then 0.121% or 1210 parts per million(ppm). The die in this study were reported to have higher defect density than normal due to a contact misalignment problem so that the data may have given pessimistic results. Another study by Turner, et. al., reported no stuck-open defects among a sample of SSI and MSI gates, however, the sample size was not given[14].

This paper reports the results of electrical measurements taken from two 1K ROM CMOS ICs that had the stuck-open failure mechanism. Both defective ICs had open metal in the drain line of an n-MOS transistor located in one of the 2-NOR gates in the decoder section. The geometry of the open metal in the drains of the two ICs was different; one IC (IC_A) had a relatively large section of missing metal and the other IC (IC_B) had narrow metal cracks in the steps of three of the 2-NOR decoder gates. The voltage levels, quiescent power supply current(I_{DDQ}), transient response, and tester properties associated with these defects are reported. The timing relation between the floating node voltage and I_{DDQ} was of particular interest to determine if the stuck-open fault could be detected by a measurement of quiescent power supply current in a production environment[15].

II. METHODS AND RESULTS

Measurements on IC_A The stuck-open fault in IC_A was caused by the absence of a 10 um section of metal in the decoder circuitry for memory row address 18. Figure 2(a,b) show the normal metal pattern and the defective metal patterning that caused the stuck-open failure mode. The features of this defect indicate that it was created during wafer fabrication. The metal is completely missing in a 10 um long section on top of polysilicon (and intermediate oxide) that ends abruptly at the edges of the polysilicon. Other die from the same wafer lot did not show this defect and no defects were found in the mask. It is believed that the photoresist failed to adhere in this region, resulting in removal of this section of metal during reactive ion etching (RIE) patterning. Figure 3(a) shows the row decoder subcircuit schematic that includes the defective 2-NOR gate. Figure 3(b) shows the location of the open metal break in the drain interconnect of one of the n-MOS pulldown transistors.

Figure 2. Voltage contrast SEM picture of a ROM decoder 2-NOR circuit showing (a) A normal drain connection and (b) a missing drain drain section.

Figure 3. (a) ROM row decoder and memory array subcircuit showing the location of the defective 2-NOR gate. (b) 2-NOR gate showing the break in the drain metal interconnect of transistor MN_B.

IC_A passed a functional address sequence test, but failed a ping-pong test in which data was read from every memory address just before and just after data was read from every other memory address. Elevated quiescent power supply current (I_{DDQ}) was associated with these failed logic states. The logic operation of the memory array and decoders was then observed using a Cambridge DVCS-1500 voltage contrast electron beam tester. The passivation glass on the IC was removed using a standard wet etchant process. Electrical stimulus for this static CMOS IC was provided by a power supply and a manual switch box. Particular address sequences showed that the defective 2-NOR gate allowed the 25th word line to stay on when it should have been driven off by the control logic. The word line eventually turned-off after about six seconds.

The defect properties were consistent with the observed failing test vectors and with elevated I_{DDQ} in these states. A logic one driven to node B on the defective 2-NOR gate shown in Figure 3 should have pulled the NOR gate output (node C) and the ROM array transistor to 0

V. However, the metal break in the n-MOS pulldown transistor allowed node C to be put in a high impedance state. For those logic states in which failure was observed, the previous state on node C was a logic one. This meant that all array transistors connected to that memory address line were activated for several seconds when they should have been off. These erroneously activated array transistors were put in contention with the p-channel bit-line precharge transistors causing elevated I_{DDQ} for this state. I_{DDQ} was indirectly elevated by the stuck-open fault due to the nature of the design.

The transient and steady state voltages of the output node C of the defective 2-NOR gate were indirectly measured for the high impedance state by placing a 1 um metal probe on node F (Figure 3 of the 2-NAND gate). The voltage response at node F and the power supply current waveform $i_{DD}(t)$ were measured by an HP4145A Semiconductor Parameter analyzer.

Figure 4 shows the timing response when node C was precharged to 0 V (AB = 11) prior to putting it in the high impedance state (AB = 10). The voltage at node F, $v_F(t)$ decayed to about 0.4 V over a time period of about 60 s. I_{DDQ} was 147 pA at AB = 11 just prior to setting the high impedance state. When AB was then set to the high impedance state (AB = 10), $i_{DDQ}(t)$ increased to about 22 mA within an 8 s period and then decreased to about 2 mA over the next approximate 50 s. The timing response of v_F and $i_{DD}(t)$ appear similar over the last approximate 90 s of Figure 4. The shape of $v_F(t)$ in Figure 4 implies that the floating node voltage at node C increased from the precharge value of 0 V to a value high enough to cause the 2-NAND output voltage to drop to 0.4 V. The steady state voltage at node C during the high impedance state was obtained by placing a second metal probe down at node C and measuring a voltage transfer curve for the 2-NAND gate. The steady state voltage of the floating node was then estimated from the transfer curse at 5.5 V.

Figure 4. Timing response of $i_{DD}(t)$ and the voltage at node F $v_F(t)$when node C when node C was precharged to 0 V prior to setting node C in a high impedance state.

The curves shown in Figure 4 are interpreted as due primarily to a drift in the floating node voltage to an equilibrium value that was above the logic threshold of the 2-NAND gate, but not high enough to cut off the p-MOSFET. Consequently, $i_{DD}(t)$ increased as the floating node voltage drifted from a low of about 1 mV to the final equilibrium value of 5.5 V. The peak in $i_{DD}(t)$ occurred as the load inverter was first turned on then off during the transition.

Figure 5 shows the timing response when node C was precharged to a logic high of 11 V (AB = 00) prior to putting it in the high impedance state (AB = 01). The voltage at node F, $v_F(t)$ increased slightly from 0 V to about 0.4 V while $i_{DDQ}(t)$ increased from 147 pA to about 2 mA. The steady state values are the same as measured for the low state precharge of node C as shown in Figure 4.

Figure 5. Timing response of $i_{DD}(t)$ and the voltage at node F $v_F(t)$ when node C when node C was precharged to 11 V prior to setting node C in a high impedance state.

Measurements on IC_B The stuck-open faults in IC_B were caused by failure of step metal coverage in three locations involving the 2-NOR gates of the decoder section of the ROM. Figure 6 shows a SEM photograph of one of these metal breaks that are believed to have occurred during wafer fabrication. These open circuits occurred where the metal for the 2-NOR gate n-channel drain connection made a step over polysilicon and field oxide. These steps were coincident creating a very steep topography that is usually not covered well by evaporated metallization. This has been referred to as a "double step".

Figure 6. Voltage contrast SEM picture of a ROM decoder 2-NOR circuit showing an open crack in the step of the drain line to one of the n-channel transistors.

Analysis of IC_B was conducted in a similar manner as that for IC_A described above. IC_B passed a functional test in which the address decoders were sequenced, but failed a ping-pong test. The functional failures occurred when the defective transistors were driven such that a high impedance node occurred on the 2-NOR output. These logic failures were verified by observations on the Cambridge DVCS-1500 voltage contrast SEM. Elevation of I_{DDQ} was observed and was consistent with the observations on IC_A. The elevated I_{DDQ} occurred as a consequence of both the memory fault allowing contention with the precharge pullup transistor during the precharge clock period and also due to the floating node voltage under steady state conditions.

The timing response of the 2-NAND gate (Figure 3) is shown in Figure 7(a) when the high impedance node was precharged to 0 V. $i_{DD}(t)$ was not obtained for IC_B due the occurrence of a leaky input protection diode that was electrically damaged during one of the test setups. Figure 7(b) shows the voltage response of the 2-NAND gate when node C was precharged high to 11 V. The voltage response of the 2-NAND gate to a floating node input is nearly identical to that obtained for IC_A.

Figure 7. Timing responses of the voltage at node F (Figure 3) when node C was precharged to (a) 0 V prior to setting node C in a high impedance state and (b) when node C was precharged to 11 V prior to setting node C in a high impedance state.

III. DISCUSSION

Measurement of the floating node voltage transient response in the stuck-open fault is important in establishing the nature of the memory defect. The time constants measured in the two stuck-open faults reported here were on the order of several seconds. This establishes that the stuck-open fault acts as a memory fault at normal clock frequencies. The steady state property of the stuck-open faults depends upon the local circuit topography and how that influences the steady state voltage of the floating node[16]. The floating node measured here attained a value of 5.5 V which was one-half of V_{DD}. Due to the low value of logic threshold voltage, the output of the effected gate for both IC_A and IC_B was a weak zero value of about 0.4 V.

The measurement of I_{DDQ} is a very sensitive technique for detection of defects in CMOS ICs[17-19,14,15]. The time constant of the floating node is therefore important for establishing the validity of the I_{DDQ} measurement technique for the stuck-open defect. Floating nodes cause elevated I_{DDQ} when the final steady state is such that both p- and n-channel transistors are turned on. If the time constant for this action is rapid with respect to tester clock frequencies, then the I_{DDQ} technique could be used to detect stuck-open faults. However, the measurement of $i_{DD}(t)$ shown in Figures 4, 5 and 7 shows that the steady state voltage was not reached for several seconds. Figure 4 shows that $i_{DD}(t)$ reached a value of 470 uA in the first 200 ms which is a response that is too slow for tester rates. This data then imply that the I_{DDQ} measurement technique can not be used in a practical sense to guarantee detection of the stuck-open fault. However, it is important to note that this particular failure was initially detected by elevated I_{DDQ} measured on a Sentry S20 tester and not by functional testing of the decoder circuit. The elevated I_{DDQ} was peculiar to the design since the stuck-open defect caused a transistor contention on the bit-line during the precharge cycle. The I_{DDQ} technique can then be interpreted as enhancing the probability of stuck-open fault detection, but not guaranteeing it.

CMOS stuck-open faults are highly significant in that they can escape normal functional or stuck-at fault test sets. In the two cases of stuck-open faults described here, a functional sequencing of the ROM

decoders did not detect the defect. Two possible strategies for detection of stuck-open defects are: (1) use of a stuck-open test set that preconditions each node prior to evaluation by a second test vector and (2) use of a stuck-at test set with 100% node coverage. The first approach guarantees detection of the stuck-open fault, but certain CMOS circuit configurations can cause timing glitches in the presence of stuck-open faults. These types of circuits must first be identified and then corrected in the design since this can lead to erroneous node voltages during the intializing test pattern and subsequent masking of the stuck-open fault[4-11]. It was also reported that computer time to generate a stuck-at test set on an 8000 gate circuit was ten times longer than that required for a stuck-at test generation[9]. That particular stuck-open test generator was successful in obtaing 100% fault coverage for ICs with 2000 gates or less, but could only attain 70% coverage with a circuit having 8000 gates[9].

The second strategy for detecting stuck-open faults relies on a high probability of detection of stuck-open faults by stuck-at test sets. One experiment reported that approximately 90% of the stuck-open faults in a sample of 4552 ICs were detected by a 100% stuck-at test set[13]. It was noted in these experiemnts that the probability of stuck-open fault detection fell rapidly as the stuck-at fault coverage fell below 95%. For high reliability ICs, the simultaneous measurement of I_{DDQ} with a 100% stuck-at fault test set can enhance the probability of stuck-open fault detection as shown by the data reported in this paper.

A third factor in reducing stuck-open fault failure rates is to consider alternate manufacturing and design techniques. The metal process must be stabilized to reduce the probability of metal breaks due to step coverage, thermally induced metallization voids, electromigration or mask particle defects[20,21]. Another important factor is to consider alternate layout styles that replace the drain metal interconnect material with either diffusion or polysilicon material[22,14]. The intent is to use a conducting material that has a lower probability of an open circuit. Koeppe demonstrated a CMOS circuit layout using a ring geometry for the drain interconnect diffusion material that had a typical 2% degradation in timing signal[22]. The area overhead in this alternate design was zero. Studies remain to be done for larger circuits that use such layout techniques to reduce stuck-open failure rates. In addition, it should be noted that although metal cracks due to steps, thermally induced voids and electromigration failures are eliminated, random particle defects on the mask still exist for any conducting material.

(ADD A DESCRIPTION OF THE LAYOUT MOD'S THAT SANDIA DID TO REDUCE SOP FAULT OCCURRENCE - see Keith and Jerry)

The frequency of failure for the stuck-open defect is an important issue. If failure rates are 100 ppm or less for stuck-open faults then the defect is not worth the cost of testing for it in most applications. Woodhall, et. al., reported an escape rate of 1210 ppm in their sample of ICs that were evaluated with a 100% stuck-at test set[13]. If the contact misalignment problem in that sample led to some of the stuck-open faults reported, then typical failure rates may be lower. However, the quality of wafer lots vary and each quality measure is not known until until after the lot is tested. The limited data available suggest that the stuck-open fault is significant and worth testing for until there is hard evidence to the contrary.

IV. CONCLUSION

The electrical properties associated with the stuck-open fault were measured on two ICs. The time constant of the high impedance node caused by the stuck-open fault logic state was found at room temperature to be on the order of seconds confirming that this fault acts as a memory fault for typical tester clock rates. The elevation of I_{DDQ} associated with the floating node voltage was large enough to indicate the presence of a defect, but the time response was too slow for this method to be used as a practical technique that guarantees the detection of stuck-open faults. However, the two cases reported here illustrate that stuck-open faults can in some instances be detected by the I_{DDQ} technique.

This work was performed at Sandia National Laboratories supported by the U.S. Department of Energy under contract DE-AC-04-76DP00789.

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DISCLAIMER

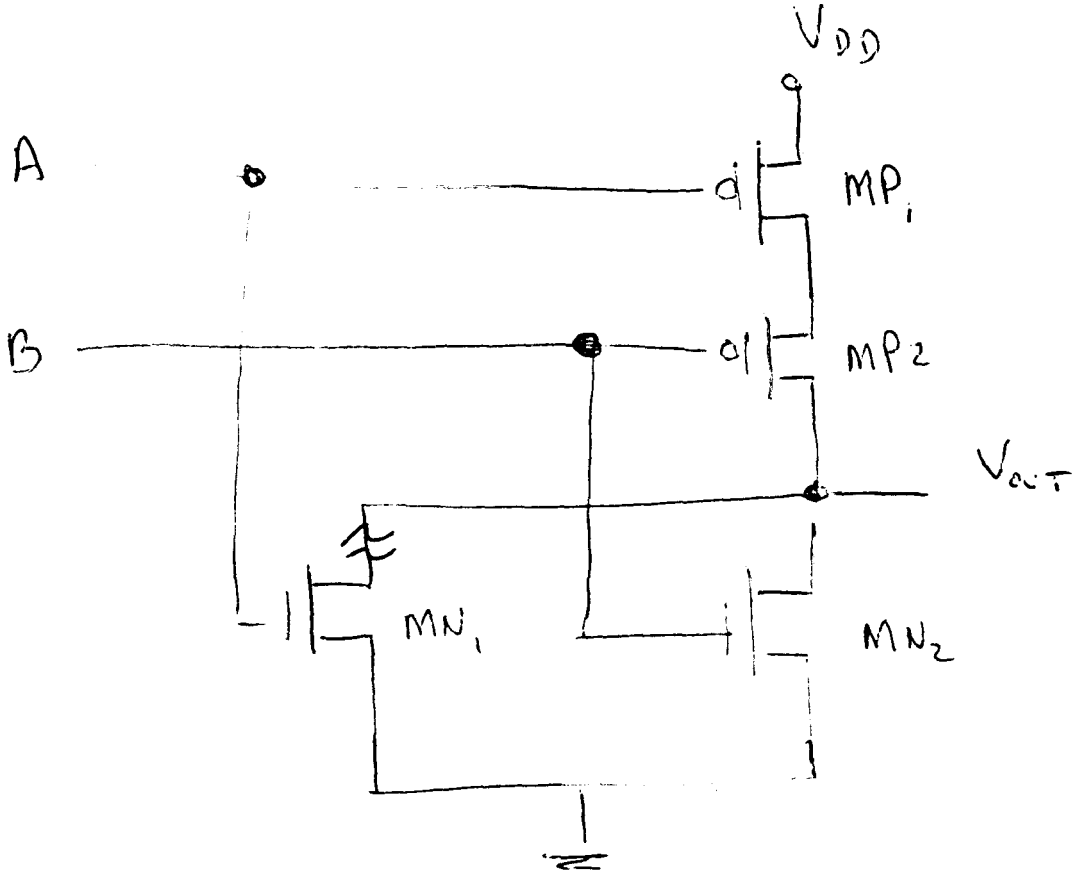
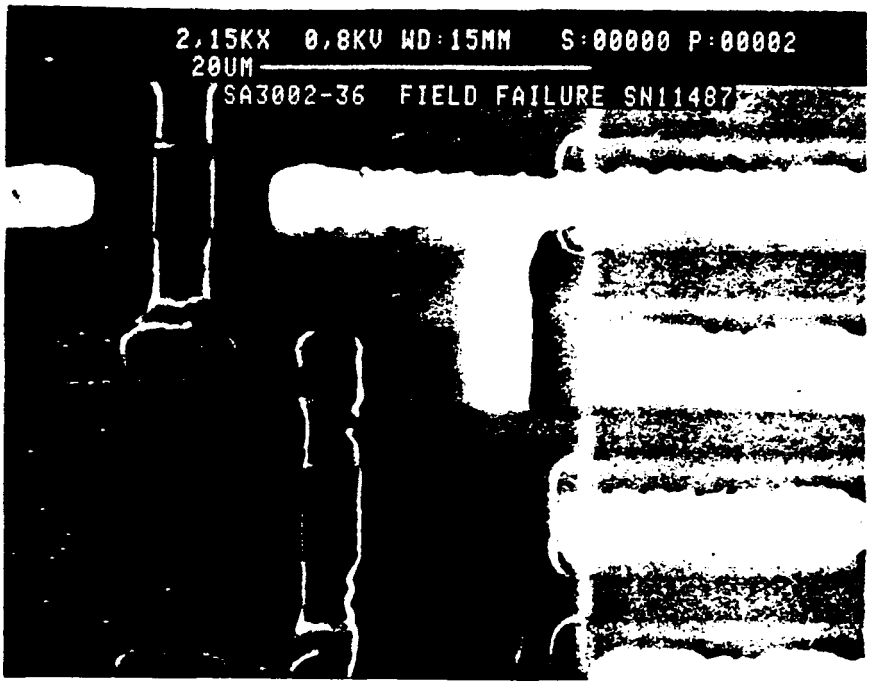
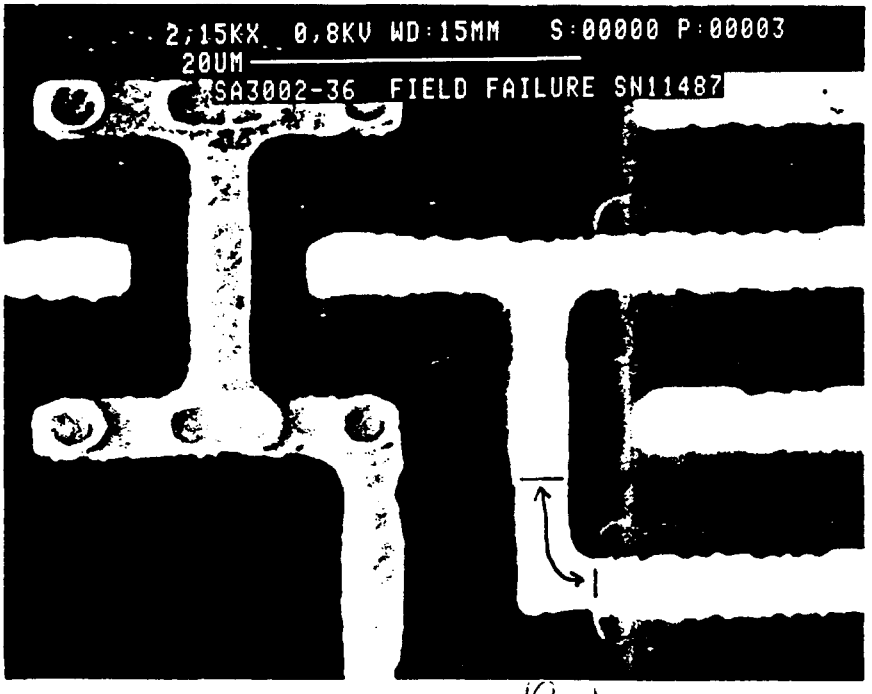


FIGURE 1



SA3002 SN 11487
Failure site with missing metal.
(missing section is indicated in the photo below)

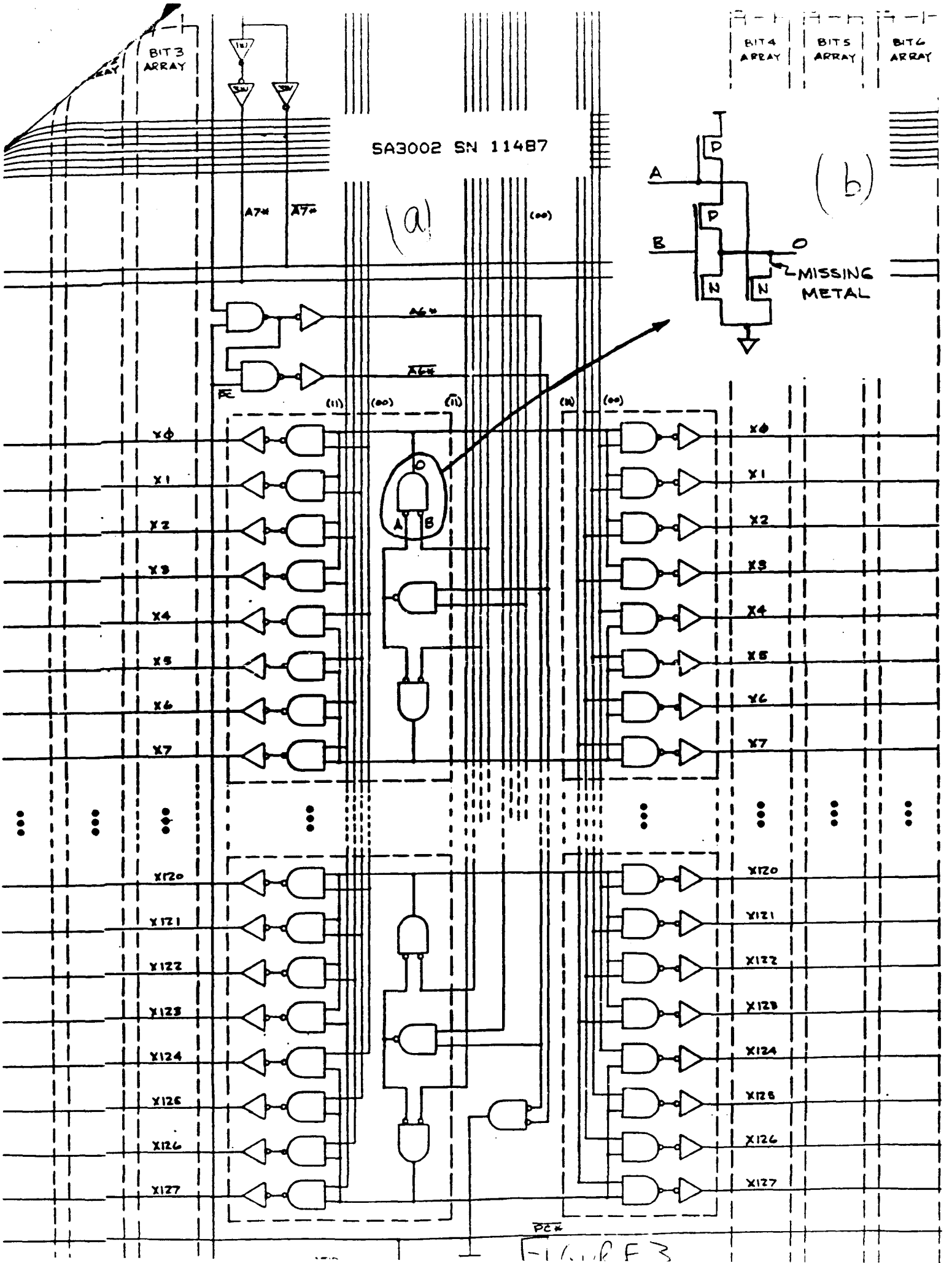
(b)



(a)

SA3002 SN 11487
Adjacent site with correct patterning.

FIGURE 2


SA3002 SN 11487
BIT3 ARRAY
BIT4 ARRAY
BIT5 ARRAY
BIT6 ARRAY
A7*
A7*
A6*
A6*
PE
(11)
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(11)
(11)
(00)
X0
X1
X2
X3
X4
X5
X6
X7
X120
X121
X122
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B
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(a)
(b)
P
P
N
N
MISSING METAL
PC*

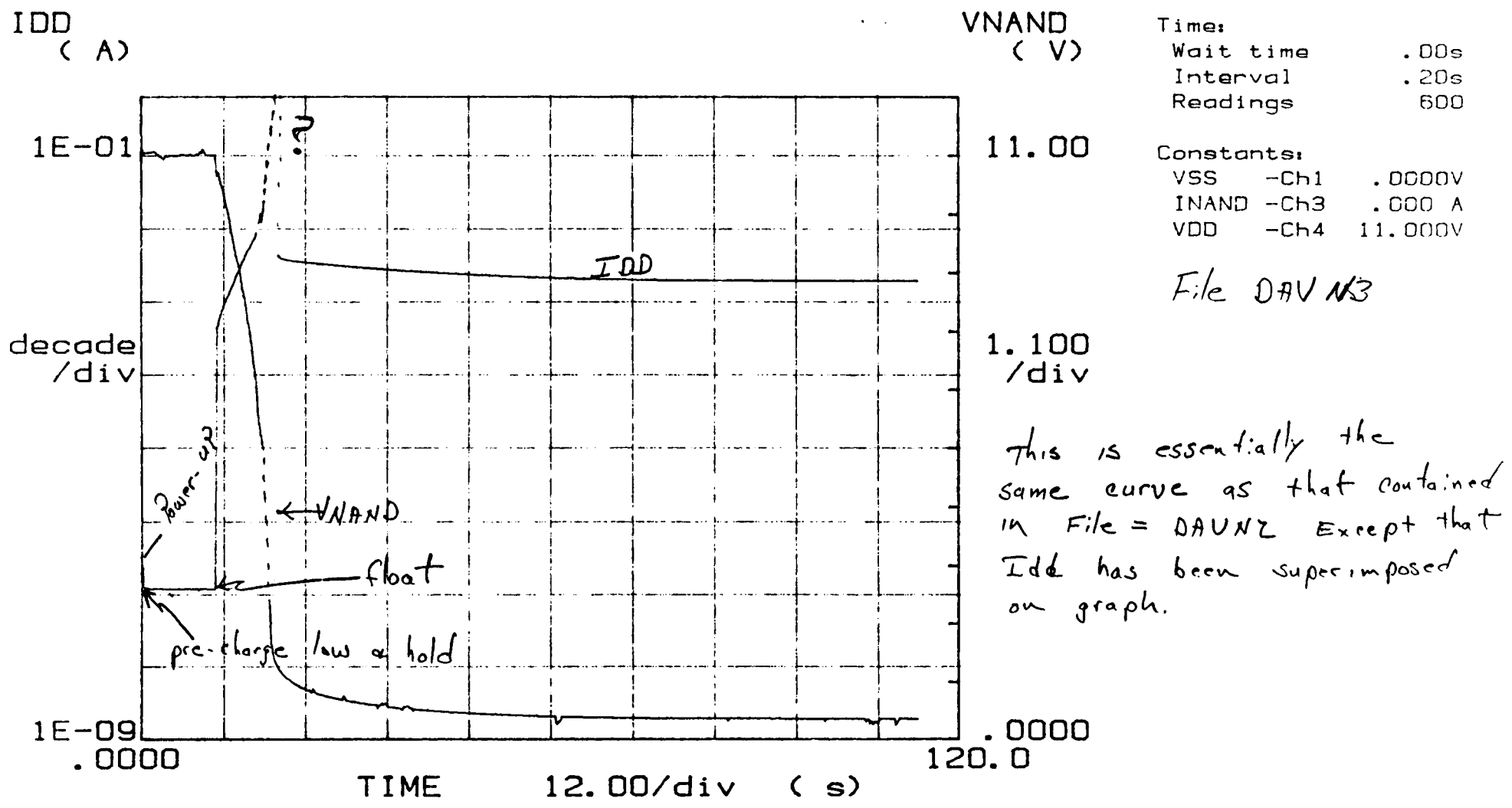
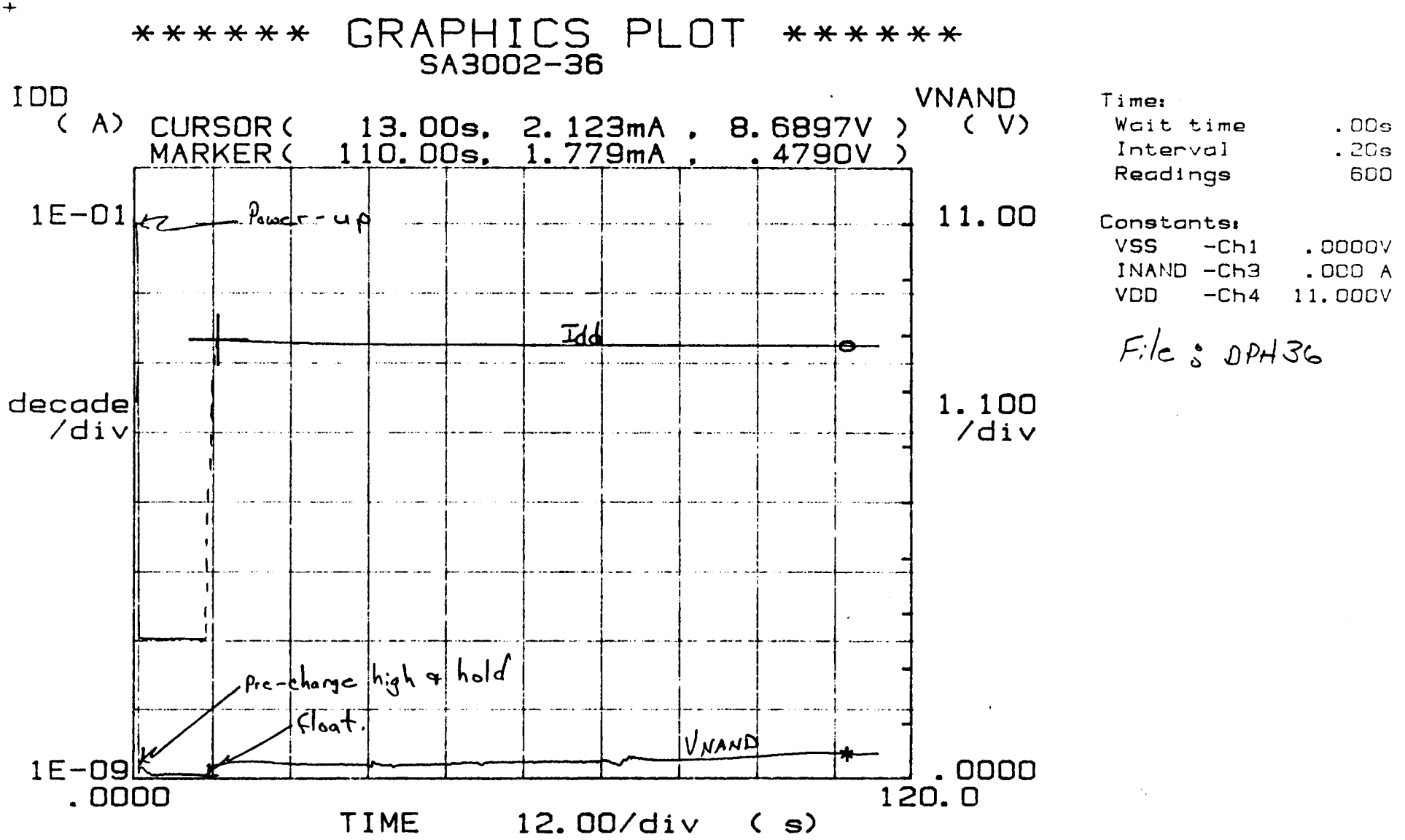

****** GRAPHICS PLOT ******
SA3002-36
IDD
(A)
VNAND
(V)
1E-01
decade
/div
1E-09
.0000
11.00
1.100
/div
.0000
120.0
TIME 12.00/div (s)
IDD
?
Power up
VNAND
float
pre-charge low & hold
Time:
Wait time .00s
Interval .20s
Readings 600
Constants:
VSS -Ch1 .0000V
INAND -Ch3 .000 A
VDD -Ch4 11.000V
File DAVN3
This is essentially the same curve as that contained in File = DAVN2 Except that Idd has been superimposed on graph.

FIGURE 4


****** GRAPHICS PLOT ******
SA3002-36
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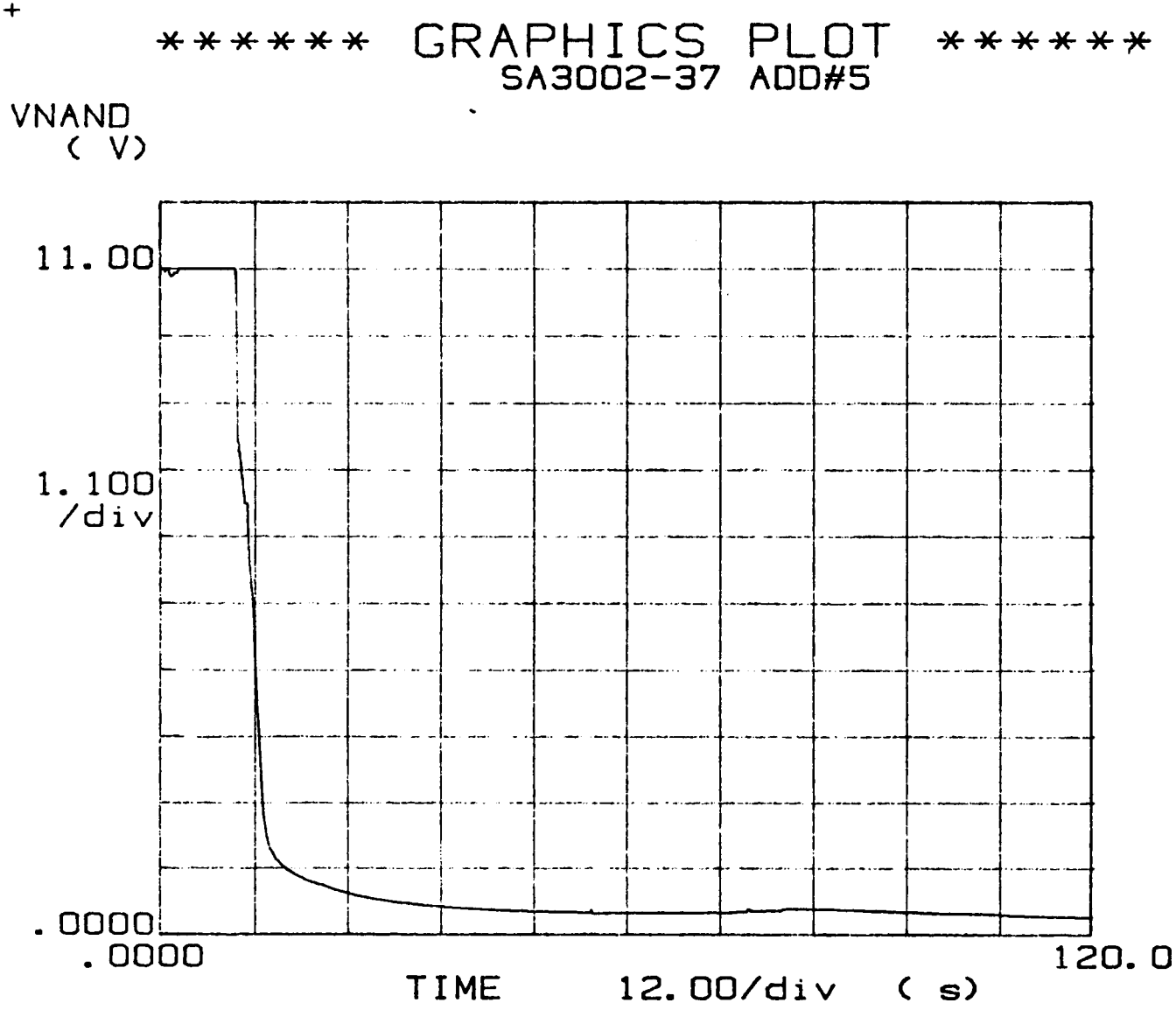
(A)
VNAND
(V)
CURSOR(13.00s, 2.123mA , 8.6897V)
MARKER(110.00s, 1.779mA , .4790V)
1E-01
11.00
Power-up
Idd
decade
/div
1.100
/div
Pre-charge high & hold
float.
VNAND
1E-09
.0000
.0000
120.0
TIME
12.00/div
(s)
Time:
Wait time .00s
Interval .20s
Readings 600
Constants:
VSS -Ch1 .0000V
INAND -Ch3 .000 A
VDD -Ch4 11.000V
File: DPH36

FIGURE 5

SA3002 SN 12213
One of the other NOR gate design rule violation locations which did not fail but is nearly open.

FIGURE 6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(V)
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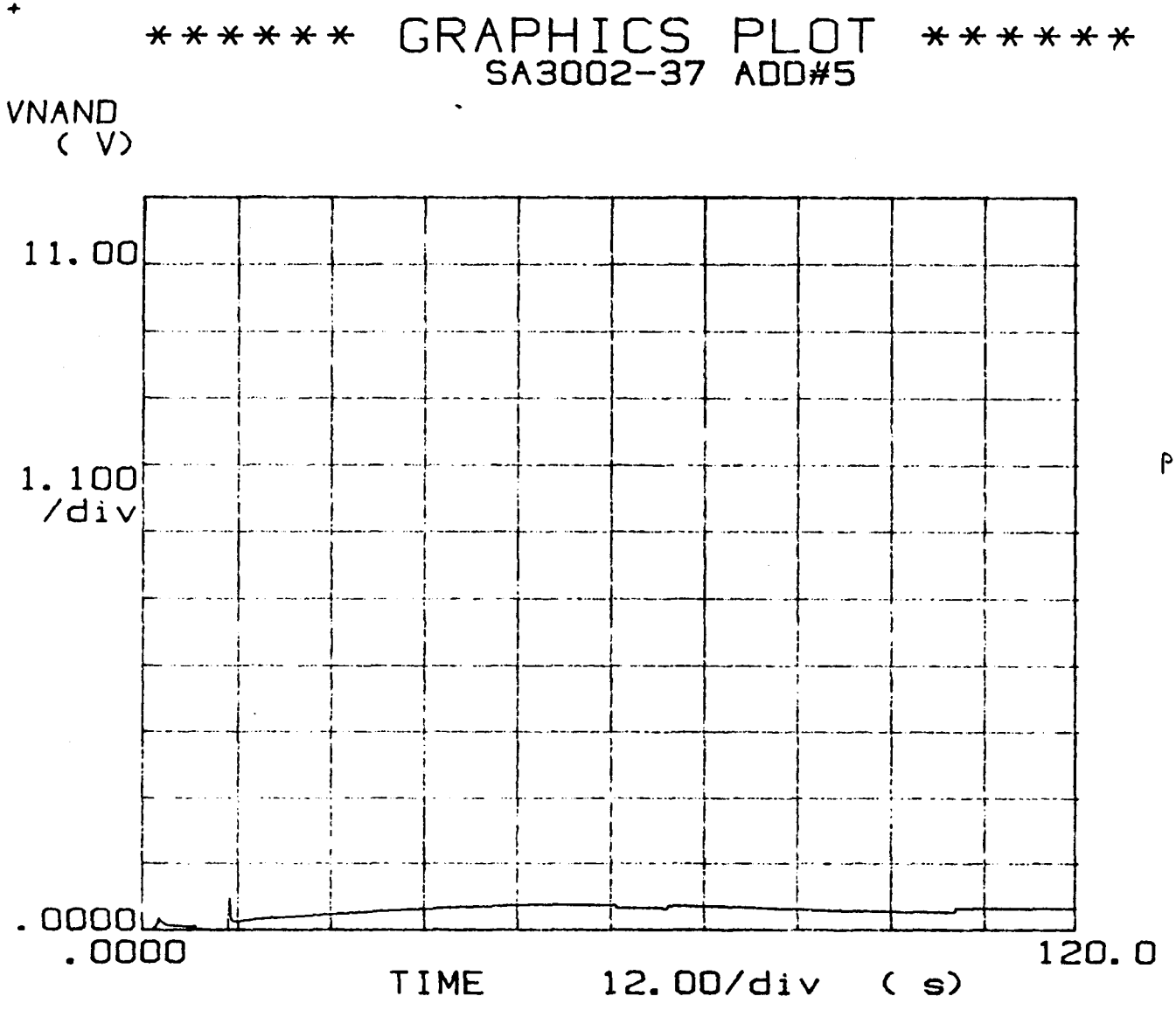
1.100
/div
.0000
.0000
120.0
TIME
12.00/div
(s)
Time:
Wait time .00s
Interval .20s
Readings 600
Constants:
VSS -Ch1 .0000V
INAND -Ch3 .000 A
VDD -Ch4 11.000V
File : DL375
Pre-charge low then float

FIGURE 7(a)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(V)
11.00
1.100
/div
.0000
.0000
120.0
TIME 12.00/div (s)
Time:
Wait time .00s
Interval .20s
Readings 600
Constants:
VSS -Ch1 .0000V
INAND -Ch3 .000 A
VDD -Ch4 11.000V
File: DH375
pre-charge high then float

FIGURE 7(b)