LINEAR IC SPICE MACROMODEL DEVELOPED FROM MEASURED TRANSISTOR PARAMETERS

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Abstract-A transistor level model in a subcircuit definition is presented for the L161 micropower comparator. This macromodel is suitable for use with present-day circuit simulators such as PSPICE and SPICE-2G6. Wherever possible, measured transistor parameter values are used to replace default values in the models. Limitations of the macromodel and a comparison of model performance with data sheet values will be discussed.

INTRODUCTION

The L161 micropower comparator offers control of both AC and DC parameters with a single power supply current setting resistor. This feature allows users to optimize speed-power trade-offs for specific applications. Variation of the setting resistor (RSET) simultaneously alters parameters such as supply current, input bias current, slew rate, output drive capability, and gain.

Currently no commercial model is available for the Siliconix L161 Micropower Quad Comparator. Circuit simulators representative of present-day, general-purpose, circuit-analysis programs include SPICE-2G6 and PSPICE. Various options exist to generate a model compatible with these simulators. For example, a comparator macromodel could be generated with the PARTS option of PSPICE by MicroSim Corporation [1].

The PARTS option of PSPICE is a program internal to PSPICE. This program derives seven specific transistor parameters from data sheet values which are then used in it's comparator macromodel subcircuit. This particular macromodel has been designed as a generic model for comparators. As a result, it does not offer features that are unique to some comparators. The L161 comparator has a feature which allows slew rate, output drive capability, input bias current, and gain to be programmed as a function of supply current (ISET pin). These features are not included in the PSPICE comparator macromodel generated with the PARTS program option. Therefore, important performance characteristics of the linear integrated circuit (IC) would be omitted if the PARTS program were used to generate the macromodel.

Another option is to generate a transistor level model defined by a subcircuit representation. This approach is

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generally not used. A macromodel is usually the most desirable type of model to generate for an IC because it reduces computation time and required computer memory size [2],[3]. This is accomplished through a reduction in the number of transistors in the model resulting in the solution of fewer non-linear equations.

One comparator and the biasing network common to all four comparators in the L161 linear IC involves only eleven transistors. A device level model using eleven transistors in a subcircuit representation does not significantly increase CPU time and permits incorporating the features afforded by the power supply current setting resistor. For this reason a transistor level model defined by a subcircuit representation was developed.

This paper describes the development of the subcircuit definition of the L161 linear IC macromodel and discusses a comparison of data sheet values and simulated values of key parameters to determine the model's limitations. Several DC, AC, and transient responses were tested. The circuit simulator used to obtain simulated values was PSPICE (version 4.04, MicroSim Corp.).

MACROMODEL DEVELOPMENT

The circuit schematic in Fig. 1, obtained from a Siliconix Incorporated data sheet [4], is used for the transistor level representation. The validity of the circuit was confirmed via construction analysis.

The circuit contains three multiple collector PNP transistors. A multiple collector transistor can be modeled as several transistors connected in parallel. The number of transistors is equal to the number of collectors. The base and emitter nodes are shared in common.

A scaling factor (area) representative of the area value for the emitter or collector is included as the last entry in the transistor statement line of the model [1]. The scaling factor is necessary for determining parasitic resistances, base current, collector current, substrate current, and junction capacitances within the bipolar transistor model in SPICE. The following information was obtained from Siliconix [5] and used to determine scaling factors: (collector area of Q3B) = 7 x (collector area of Q3A), (emitter area of Q7) = 2 x (emitter area of Q5), (collector area of Q6C) = 2 x (collector area of Q6A), (collector area of Q6B) = 2 x (collector area of Q6A), and (collector area of Q4B) = 7 x (collector area of Q4A).

The transistor model parameter sets are derived from eighteen critical measured internal parameters that were obtained from the manufacturer [5]. Table I compares measured parameters with their PSPICE and SPICE-2G6 default values. The subcircuit SPICE-2G6/PSPICE netlist of the L161 comparator model is listed in the Appendix. The measured transistor parameters are included in the

.MODEL statements in the subcircuit definition. The PSPICE/SPICE-2G6 default parameters are used where measured parameters are unavailable. If this model is used with a simulator other than PSPICE or SPICE-2G6, the user must verify that the default values listed in Table I match those of their simulator. Where there is disagreement, include the default value from Table I in the .MODEL statement line parameter list.

MACROMODEL PERFORMANCE

The key parameters for evaluating comparator performance are:

CMRR = COMMON MODE REJECTION RATIO
AVOL = DC OPEN LOOP VOLTAGE GAIN
IS = DC POWER SUPPLY CURRENT
IBT = INPUT BIAS CURRENT, TOTAL
IOS = INPUT OFFSET CURRENT
VOS = INPUT OFFSET VOLTAGE
VOL = LOW OUTPUT VOLTAGE
VOH = HIGH OUTPUT VOLTAGE
SR = SLEW RATE
TR = OVERDRIVE RESPONSE TIME

Table II lists the data sheet and simulated values for AVOL, CMRR, IS, IBT, IOS, VOS, VOL, and VOH. These parameters were simulated according to low power and high power conditions defined in the L161 Siliconix data sheet [4]. The choice was made to compare the simulated values with the data sheet limits, instead of the typical values, because the typical values are not guaranteed nor subject to production testing [4], whereas the limits are. A designer should design according to guaranteed parameter values. If the model's simulated values agree with the guaranteed values, then the model can be trusted for design use. The simulated and data sheet values are in good agreement except for input offset voltage. The model presented here does not exhibit an input offset voltage because the input transistors are matched. Input offset voltage is created by mismatches in emitter-base voltages [6]. The programmable supply current feature is exhibited in the results of Table II. Input bias current, input offset current, and DC open loop gain vary when the supply current is increased via use of the ISET pin.

The scales for the plots of slew rate and overdrive recovery, displayed in the L161 Siliconix data sheet [4], are difficult to read with much accuracy (2 significant digits maximum). They are not designed to be used to obtain exact values, but to yield approximations and parameter trends of typical values. As a consequence, there is an error introduced in the interpretation of the parameter values displayed in these plots.

Table III lists the data sheet and simulated values for slew rate with varying power supply current. The data sheet values for slew rate are extracted from plots given in the Siliconix data sheet [4] for the L161 comparator which are listed as typical values. RSET is adjusted to give the supply current indicated in the data sheet. The negative slew rate is approximately 28% smaller than the data sheet typical values. The positive slew rate is approximately 170% larger than the data sheet typical values. This will affect the overdrive recovery times. The relative error is calculated from the following expression: [(simulated - typical value) / typical value]. Even though there is an inaccuracy in the simulation of this parameter, the model exhibits the ability to program slew rate as a function of supply current. The model displays the linear characteristic of positive slew rate and the non-linear characteristic of negative slew rate as indicated in the Siliconix data sheet [4].

Table IV lists the data sheet and simulated values for overdrive recovery and exhibits the model's slew rate inaccuracy. The data sheet values for overdrive recovery times are extracted from plots given in the Siliconix data sheet [4] for the L161 comparator which are listed as typical values. With a -100 mV (low to high response) overdrive and a supply current of 1 mA the model responds twice as fast as the data sheet typical values. This is a consequence of the simulated positive slew rate being nearly three times the data sheet typical value with the same test conditions. The 100 mV (high to low response) overdrive has an inaccuracy similar to the negative transition slew rate. It is 21% slower than the data sheet indicates.

No convergence problems were encountered during the simulations. The typical run time for the simulations was one minute. Slew rate and CMRR [6] simulations took from three to five minutes.

CONCLUSIONS

A transistor level macromodel of the L161 comparator, defined as a subcircuit definition, has been developed for use with the SPICE-2G6 and PSPICE circuit simulators. This model accurately simulates IBT, IOS, VOL, VOH, IS, AVOL, and CMRR. There are several limitations to the model. Negative slew rate is approximately 28% smaller and positive slew rate is approximately 2.5 times larger than the data sheet values. These inaccuracies contribute to similar errors in overdrive response time. These errors may not be as large as indicated due to difficulties in interpretation of the values in the plots displayed in the data sheet and inaccuracies in the plots themselves. The model does exhibit the control of both AC and DC parameters via the power supply current setting resistor. Input bias current, input offset

current, DC open loop gain, and slew rate can all be programmed to change with variation in supply current. A macromodel generated using the PARTS option of PSPICE [1] would not predict this behavior. The use of measured transistor parameters coupled with the programmable supply current features of the model make it more accurate than one generated using the PARTS option of PSPICE.

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APPENDIX

NETLIST OF L161 MODEL FOR SPICE-2G6 OR PSPICE CIRCUIT SIMULATORS

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* CONNECTIONS: NON-INVERTING INPUT
*               |  INVERTING INPUT
*               |  |  POSITIVE POWER SUPPLY
*               |  |  | NEGATIVE POWER SUPPLY
*               |  |  |  |  OUTPUT
*               |  |  |  |  |  ISET
*               |  |  |  |  |  |
.SUBCKT L161    9  7  1  8  10 14
*
Q1   8   7   3   PNPNOM
QD1   4   4   8   NPNNOM
Q2   8   9   6   PNPNOM
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Q3A   3   3   2   PNPNOM
Q3B   4   3   2   PNPNOM   7
Q4A   6   6   2   PNPNOM
Q4B   5   6   2   PNPNOM   7
Q5   5   4   8   NPNNOM
Q6A   11   11   1   PNPNOM
Q6B   10   11   1   PNPNOM   2
Q6C   2   11   1   PNPNOM   2
Q7   10   5   8   NPNNOM   2
Q8   11   12   8   NPNNOM
Q9   1   13   12   NPNNOM
Q10   13   12   8   NPNNOM
J11   14   8   13   JNOM
.MODEL NPNNOM   NPN
+ ( BF=100 BR=1.1 IS=1.66E-16   RB=150 RC=800
+    RE=3   VAF=200    CJE=1.35E-12    VJE=0.964
+    MJE=0.5 CJC=1.35E-12   MJC=0.5   VJC=0.663
+    XTB=1E-12   IKF=7E-3    TF=1E-9   TR=100E-9
+    VAR=26 )
.MODEL PNPNOM   PNP
+ ( BF=40 BR=4   IS=2.83E-17   RB=400   RC=1400
+    RE=20   VAF=80    CJE=0.85E-12    VJE=0.663
+    MJE=0.5 CJC=1.18E-12   MJC=0.5   VJC=0.663
+    XTB=1E-12 IKF=0.1E-3 TF=100E-9 TR=100E-9
+    VAR=40 )
.MODEL JNOM NJF(VTO=-18 BETA=1E-5 )
.ENDS L161
```

DISCLAIMER

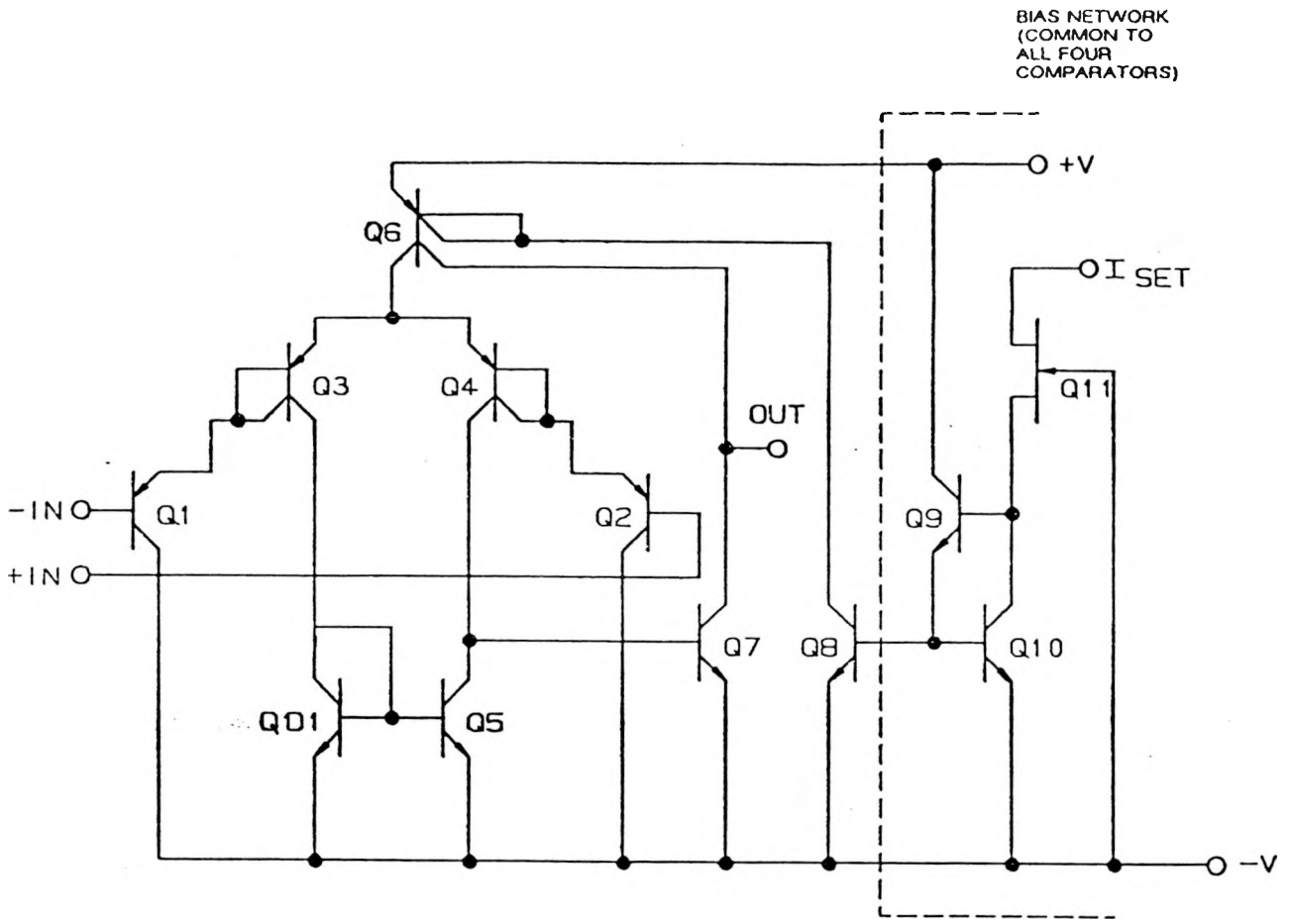
BIAS NETWORK
(COMMON TO
ALL FOUR
COMPARATORS)
+V
I SET
Q6
Q3
Q4
Q11
OUT
-IN
Q1
Q2
Q9
+IN
Q7
Q8
Q10
QD1
Q5
-V

Figure 1

TABLE I

MEASURED AND DEFAULT PSPICE/SPICE-2G6 TRANSISTOR PARAMETERS

PARAMETER	UNITS	DEFAULT	NPN MEASURED	PNP MEASURED
IS	amp	1E-16	1.66E-16	2.83E-17
BF		100	100	40
NF		1		
VAF	volt	infinite	200	80
IKF	amp	infinite	7E-3	0.1E-3
ISE	amp	0		
NE		1.5		
BR		1	1.1	4
NR		1		
VAR	volt	infinite	26	40
IKR	amp	infinite		
ISC	amp	0		
NC		2		
RE	ohm	0	3	20
RB	ohm	0	150	400
RBM	ohm	RB		
IRB	amp	infinite		
RC	ohm	0	800	1400
CJE	farad	0	1.35E-12	0.85E-12
VJE	volt	0.75	0.964	0.663
MJE		0.33	0.5	0.5
CJC	farad	0	1.35E-12	1.18E-12
VJC	volt	0.75	0.663	0.663
MJC		0.33	0.5	0.5
XCJC		1		
CJS	farad	0		
VJS	volt	0.75		
MJS		0		
FC		0.5		
TF	sec	0	1E-9	100E-9
XTF		0		
VTF	volt	infinite		
ITF	amp	0		
PTF	degree	0		
TR	sec	0	100E-9	100E-9
EG	eV	1.11		
XTB		0	1E-12	1E-12
XTI		3		
KF		0		
AF		1		

TABLE II

DATA SHEET AND SIMULATED VALUES FOR CMRR, AVOL, IS, IBT, IOS, VOS, VOL, & VOH

PARAMETER	TEST CONDITIONS A	SIMULATED VALUE	DATA SHEET LIMIT
CMRR	VIN = CMR	79 dB	75 dB MIN
AVOL		29 V/mV	20 V/mV MIN
IS	RL = OPEN ALL INPUTS LOW	50 uA	325 uA MAX
IBT		58 nA	100 nA MAX
IOS		0.5 nA	20 nA MAX
VOS		.003 mV	3 mV MAX
VOL	RL = 20 kohms	-2.83 V	-2.6 V MAX
VOH	RL = 200 kohms	2.92 V	2.5 V MIN

UNLESS SPECIFIED TEST CONDITIONS A ARE : VS+ = 3 V VS- = -3 V RL = 10 Mohms ISET = 10 uA TEMP = 25 C

PARAMETER	TEST CONDITIONS B	SIMULATED VALUE	DATA SHEET LIMIT
CMRR	VIN = CMR	86 dB	75 dB MIN
AVOL		84 V/mV	50 V/mV MIN
IS	RL = OPEN ALL INPUTS LOW	0.7 mA	3.75 mA MAX
IBT		308 nA	400 nA MAX
IOS		28 nA	60 nA MAX
VOS		6 uV	3 mV MAX
VOL	RL = 20 kohms	-14.6 V	-14.6 V MAX
VOH	RL = 200 kohms	14.9 V	14.5 V MIN

UNLESS SPECIFIED TEST CONDITIONS B ARE : VS+ = 15 V VS- = -15 V RL = 2 Mohms ISET = 100 uA TEMP = 25 C

TABLE III

DATA SHEET AND SIMULATED VALUES FOR SLEW RATE

ISUPPLY (uA)	RSET (kohms)	-SR SIMULATED (V/us)	-SR DATA SHEET (V/us)	RELATIVE ERROR (%)
200	536.25	72	100	-28
400	268.125	95	137	-31
600	167.578	120	163	-26
800	127.3	133	185	-28
1000	100.44	146	200	-27

ISUPPLY (uA)	RSET (kohms)	+SR SIMULATED (V/us)	+SR DATA SHEET (V/us)	RELATIVE ERROR (%)
200	1019	5.2	2	+160
400	496.031	10	3.7	+170
600	322.335	15	5.5	+173
800	237.165	21	7.4	+184
1000	182.942	26	9.3	+180

TEST CONDITIONS : VS+ = 15V VS- = -15V RL = 10 Mohms VIN = +/-100 mV CL = 10 pF TEMP = 25 C

TABLE IV

DATA SHEET AND SIMULATED VALUES FOR OVERDRIVE RESPONSE TIMES

ISUPPLY	RSET	OVERDRIVE	SIMULATED TIME	DATA SHEET TIME	RELATIVE ERROR
(mA)	(kohms)	(mV)	(us)	(us)	(%)
1.000	100.178	5	3.50	2.80	+25
1.000	101.222	20	1.55	1.20	+29
1.000	100.440	100	0.75	0.95	-21

TEST CONDITIONS : VS+ = 15V VS- = -15V RL = 10 M CL = 10 pF TEMP = 25 C VIN = 100 mV

ISUPPLY	RSET	OVERDRIVE	SIMULATED TIME	DATA SHEET TIME	RELATIVE ERROR
(mA)	(kohms)	(mV)	(us)	(us)	(%)
1.000	186.000	-5	3.95	3.80	+3.9
1.000	187.149	-20	2.15	3.40	-37
1.000	182.942	-100	1.56	3.30	-53

TEST CONDITIONS : VS+ = 15V VS- = -15V RL = 10 M CL = 10 pF TEMP = 25 C VIN = -100 mV