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1/f NOISE: A NONDESTRUCTIVE TECHNIQUE TO PREDICT MOS RADIATION HARDNESS?*

John H. Scofield and T. P. Doerr
Wright Physics Lab
Oberlin, College
Oberlin, OH 44074
(216) 775-8333

and

D. M. Fleetwood
Sandia National Laboratories, Div. 2147
P. O. Box 5800
Albuquerque, NM 87185
(505) 844-1825

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35-Word Abstract

We find a strong correlation between the preirradiation 1/f noise of pMOS transistors and their radiation hardness. This suggests that current fluctuations may provide a useful, nondestructive probe of defects in MOS devices.

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John H. Scofield and T. P. Doerr
Wright Physics Lab, Oberlin College, Oberlin, OH 44074
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The performance, reliability, and radiation hardness of MOS devices are strongly affected by defects at or near the Si/SiO_2 interface. In the last ten years, it has been demonstrated that 1/f noise is very sensitive to defects in semiconductors, as well as a wide number of other systems [1-5]. The 1/f noise of MOS devices is usually attributed to fluctuations in the occupancy of traps at or near the Si/SiO_2 interface, and/or changes in carrier mobility that accompany trapping or de-trapping events [4,6-8]. Because similar defects also determine the radiation hardness of MOS devices [9], we have performed a series of experiments to explore a possible connection between 1/f noise and the radiation hardness of MOS devices. We have found that the preirradiation 1/f noise of pMOS transistors correlates strongly with the radiation hardness of the oxide.

In this summary, we show results of 1/f noise measurements performed on pMOS transistors. A schematic diagram of the noise-measurement circuit is shown in Fig. 1. For these measurements, constant bias is applied to the gate of the MOS device, and a "constant" current is forced through a 100-kΩ resistor and the device channel. The device is ac-coupled to an amplifier so that only fluctuations of the channel current are sampled. This noise is amplified by a factor of 1000, and passed to a spectrum analyzer that performs a Fast Fourier Transform of the voltage noise to compute its power spectral density, $S_V(f)$, where f is the frequency. Each measurement of the noise power requires less than 10 min. to perform, and the noise magnitude is large enough that "heroic" shielding efforts are not required to ensure that the device noise dominates all background sources.

Noise measurements were performed on four types of devices. These devices were processed in the same lot (G1916A), but received different oxidation treatments and postoxidation anneals to vary their radiation hardness. A summary of the device processing is given in Table 1. Also shown for later reference are threshold voltage shifts due to oxide-trapped charge [10], ΔVot, following Co-60 irradiation (dose rate ≈ 1 Mrad/hr) to a dose of 100 krad(Si) at an oxide electric field of ≃ 3 MV/cm. As expected, devices with thinner oxides were relatively harder than devices with thicker oxides [11,12], and devices without high-temperature postoxidation anneals were harder than devices with the anneals [11,13,14].

Table 1. Process variations used in this study, and the oxide-trapped charge observed for each following Co-60 irradiation to 100 krad(Si).

Wafer No.	Gate Ox. Process	Post-Ox. Anneal	Ox. Thickn.	ΔVot (V)
22	850°C, 25 min. Wet	None	32 nm	-0.19
10	1000°C, 15 min. Dry	1100°C, 30 min. N_2	32 nm	-1.88
32	1000°C, 30 min. Dry	None	50 nm	-0.52
33	" , " "	1100°C, 30 min. N_2	50 nm	-3.53

In Fig. 2 we plot the noise magnitude as a function of frequency for hard and soft pMOS transistors. These measurements were performed at a gate bias of -3 V, and a drain current of 10 μA. At least three devices of each type were measured; values of $S_v(f)$ agree to within better than ± 10 percent for each type of device. S_v is inversely proportional to f for both kinds of devices, which is the defining feature of "1/f noise." The hard device is about 5-times quieter than the soft device.

In Fig. 3 we plot S_v(10 Hz) as a function of drain current for a gate bias of -3.5 V. In all cases, the noise magnitude is proportional to the square of the drain current. A quadratic dependence of S_v on I_d has been observed by other workers [15,16], and implies [1,4] that, at least in this (linear) range of device operation, the channel current does not create new defects, but only "samples" fluctuations in channel conductivity caused by existing defects [1,4]. Once again, harder devices are quieter than softer devices.

In Fig. 4 we plot S_v(10 Hz) as a function of ΔVot at 100 krad(Si) for the devices described above. Note that there is nearly a one-to-one correlation between <u>preirradiation</u> values of S_v and the postirradiation values of ΔVot. This suggests that preirradiation current fluctuations are caused by defects similar, or identical, to those that function as hole traps during subsequent irradiation. Experiments are underway to see whether a similar correlation exists for interface trap buildup. However, preliminary results suggest that any such correlation is much weaker than the correlation with oxide-trapped charge buildup. This difference may occur because interface traps are created by irradiation [9], while hole trapping sites are present before irradiation.

Based on previous work on the dependence of 1/f noise on sample geometry [4,6,15,16], we expect that the simple, <u>linear</u> relationship between S_v and ΔVot may not hold for devices made in different technologies, or for devices made with different geometries. Nevertheless, the fact that such a correlation can be demonstrated suggests that one could use noise measurements as a nondestructive screen of devices that are intended to have identical (acceptable!) radiation hardness. In this regard, 1/f noise has been applied as a successful reliability screen for JFETs and diode lasers [17,18], and may also be useful as a reliability screen for MOS devices.

It is interesting to explore the possible reasons for a link between the 1/f noise and the radiation hardness of MOS devices. Previous workers have attributed the 1/f noise of MOS devices to events in which carriers are exchanged with traps in the first 0.3-3 nm of the SiO_2 [4,6-8,15] via tunneling. These tunneling events can occur on time scales ranging from a few microseconds to many months or years, depending on the depth of the trap and its distance from the Si/SiO_2 interface, which is consistent with the observed frequency dependence of the noise [4,6]. Along these lines, it is interesting that the correlation between ΔVot and S_v in Fig. 4 is observed for pMOS devices, in which the channel carriers are holes, which presumably are captured and released by "hole traps." Experiments are underway to see whether nMOS devices on the same chips show a similar correlation with ΔVot, or whether the electrons might sense different defects. Results of these experiments, of experiments to examine the gate-bias dependence of the noise, and of the temperature dependence of the noise will also be discussed in the final paper. These results should provide additional insight into fundamental fluctuation phenomena in MOS devices, and on the connection between 1/f noise and the radiation hardness of MOS devices.

REFERENCES

1. P. Dutta and P. M. Horn, Rev. Mod. Phys. 53, 497 (1981).
2. D. M. Fleetwood and N. Giordano, Phys. Rev. B 31, 1157 (1985).
3. J. H. Scofield, J. V. Mantese, and W. W. Webb, Phys. Rev. B 32, 736 (1985).
4. M. B. Weissman, Rev. Mod. Phys. 60, 537 (1988).
5. J. Pelz, J. Clarke, and W. E. King, Phys. Rev. B 38, 10371 (1988).
6. A. L. McWhorter, in Semiconductor Surface Physics, edited by R. H. Kingston (University of Pennsylvania Press, Philadelphia, 1957), pp. 207-228.
7. E. H. Nicollian and H. Melchior, Bell System Tech. Journal, 2019, (Nov. 1967).
8. A. van der Ziel, Adv. Electron. Electron Phys. 49, 225 (1979).
9. See, for example, P. M. Lenahan and P. V. Dressendorfer, J. Appl. Phys. 55, 3495, and references therein.
10. P. S. Winokur, J. R. Schwank, P. J. McWhorter, P. V. Dressendorfer, and D. C. Turpin, IEEE Trans. Nuc. Sci. NS-31, 1453 (1984).
11. G. F. Derbenwick and B. L. Gregory, IEEE Trans. Nuc. Sci. NS-22, 2151 (1975).
12. H. E. Boesch, Jr. and J. M. McGarrity, IEEE Trans. Nuc. Sci. NS-23, 1520 (1976).
13. K. G. Aubuchon, IEEE Trans. Nuc. Sci. NS-18, 117 (1971).
14. J. R. Schwank and D. M. Fleetwood, Appl. Phys. Lett. 53, 770 (1988).
15. S. Christenson and I. Lundstrom, Solid-State Electron. 11, 797 (1968); 11, 813 (1968).
16. G. Blasquez and A. Boukabache, in Noise in Physical Systems and 1/f Noise, edited by M. Savelli, G. Lecoy, and J-P. Nougier (North-Holland, Amsterdam, 1983), pp. 303-306.
17. K. Kandiah, in Noise in Physical Systems and 1/f Noise, 1983, pp. 287-290.
18. L. K. J. Vandamme and L. J. van Ruyven, in Noise in Physical Systems and 1/f Noise, 1983, pp. 245-248.

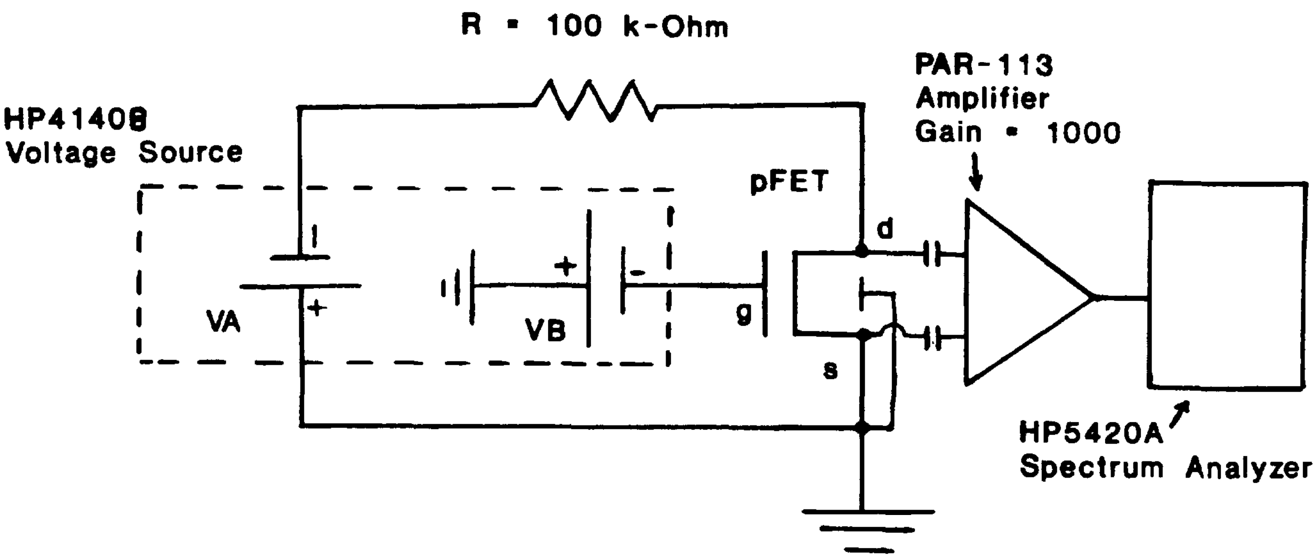

Fig. 1. Schematic diagram of noise measurement circuit.

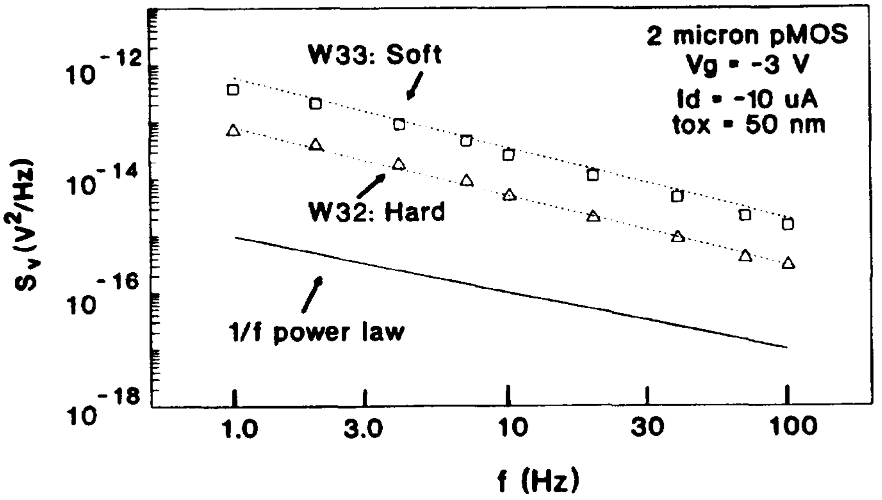

Fig. 2. 1/f-noise power spectral density as a function of frequency for radiation hard and soft pMOS transistors.

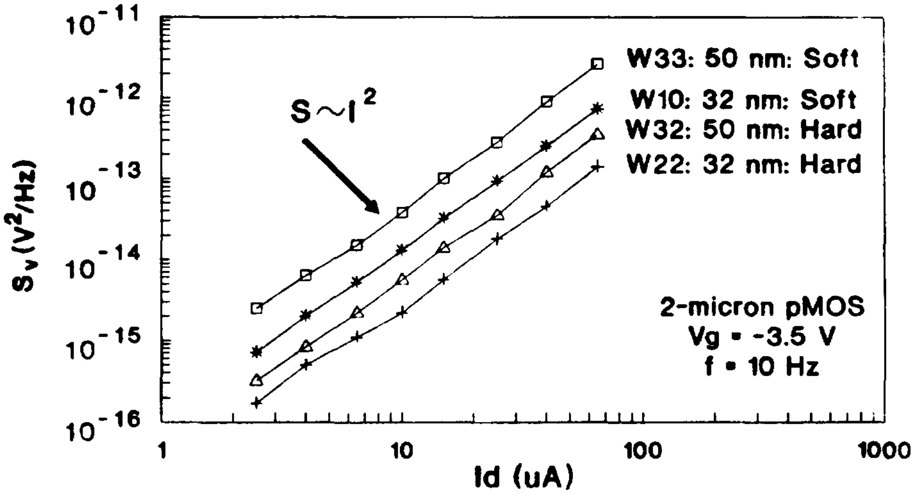

Fig. 3. 1/f-noise power spectral density as a function of channel current for hard and soft pMOS transistors.

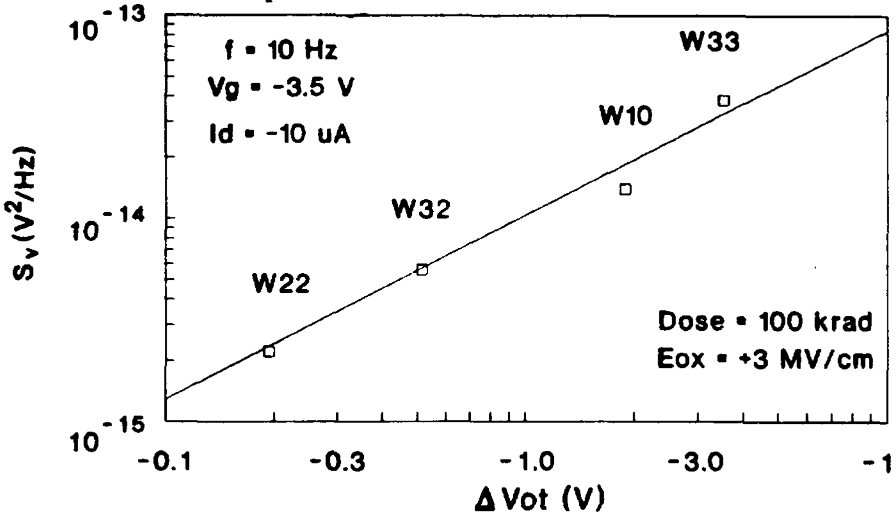

Fig. 4. Preirradiation 1/f-noise as a function of ΔVot after 100-krad(Si) Co-60 irradiation for pMOS transistors of varying hardness.