LEGIBILITY NOTICE

A major purpose of the Technical Information Center is to provide the broadest dissemination possible of information contained in DOE's Research and Development Reports to business, industry, the academic community, and federal, state and local governments.

Although a small portion of this report is not reproducible, it is being made available to expedite the availability of information on the research discussed herein.

LA-UR -83-1585

MASTER

Los Alamos National Laboratory is operated by the University of California for the United States Department of Energy under contract W-7405-ENG-36

TITLE PROGRESS IN DEVELOPING REPETITIVE PULSE SYSTEMS UTILIZING INDUCTIVE ENERGY STORAGE

AUTHOR(S) E. M. Honig

SUBMITTED TO 4th IEEE Pulsed Power Conference, June 6-8, 1983, Albuquerque, NM

DISCLAIMER

Los Alamos Los Alamos National Laboratory
Los Alamos, New Mexico 87545

PROGRESS IN DEVELOPING REPETITIVE PULSE SYSTEMS UTILIZING INDUCTIVE ENERGY STORAGE*

F. M. Honig
Los Alamos National Laboratory
Los Alamos, NM 87545

Summary

High-power, fast-recovery vacuum switches were used in a new repetitive counterpulse and transfer circuit to deliver a 5-kHz pulse train with a peak power of 75 MW (at 8.6 kA) to a 1-Ω load, resulting in the first demonstration of fully controlled, high-power, high-repetition-rate operation of an inductive energy-storage and transfer system with nondestructive switches. New circuits, analytical and experimental results, and feasibility of 100-kA and 100-kV repetitive pulse generation are discussed. A new switching concept for railgun loads is presented.

Introduction

The need for repetitive, high power pulse generators is emerging from a number of major programs within the DOE and DoD communities.[1,2] Requirements cover a wide range: kA-MA currents, kV-MV voltages, ns-ms pulse widths, and 1-30,000 Hz pulse repetition rates. If the output duty factor is low, economics generally requires an intermediate energy store between the power supply and the load. Inductive energy storage (IES) is advantageous because of its high energy density and decreasing ratio of cost to energy as size increases. With its fast discharge capability, IES is also attractive for pulse compression (using an inertial energy store, for instance). Both single shot and low repetition rate operations of inductive energy storage and transfer systems have been demonstrated at fairly impressive levels with good reliability.[3,4] However, future applications requiring operation at high power and high repetition rates (>100 Hz) will be the most demanding. Although such operation has been demonstrated with explosive opening switches and fuses,[5] actual systems will generally require high power, repetitive opening switches.

Approach

To meet the projected needs for repetitive, high power pulse generators utilizing IES, the Los Alamos National Laboratory initiated a program in late 1980 to investigate and develop high power, repetitive opening switches and associated circuits and to demonstrate high power pulse train feasibility.[6] By not being tied to the specific requirements of a particular program or application, the Los Alamos program was to explore the problem in general terms. The goal of achieving 10 kA, 10 kV pulses at a rate of 1-10 kHz was established to give some focus to the program and to address the various requirements presented at the opening switch workshop.[1]

There are two fundamental switch opening methods (direct interruption and counterpulse) and associated transfer circuits. With the direct interruption method, the impedance of the opening switch R(t) in the resistive transfer circuit (Fig. 1) is raised rapidly to a value much greater than the load impedance to force the current to transfer to the load. The load voltage therefore depends directly on the switch impedance risetime. The switch must conduct the full storage current, undergo a large impedance change, and then withstand the high recovery voltage immediately after transfer. In addition, the resistive transfer operation requires that the opening switch dissipate energy associated with the switch inductance L_{switch} and the load inductance L_2. The minimum energy dissipation in the switch E_{DIS} (for instantaneous switching) is related to the energy $E_{Lswitch}$ stored in the switch inductance and to the energy E_{L2} transferred to the load inductance by the equation

$$E_{DIS} = E_{Lswitch} + (1 + X)E_{L2} \quad , \qquad (1)$$

where $X = L_2/L_1$. The switch dissipation increases with increases in switching time.

With the counterpulse method, the current in the opening switch S_1 of the capacitive transfer circuit (Fig. 2) is momentarily reduced to zero by discharging the counterpulse capacitor C_2 through the switch in the direction opposing the main current. If the current zero time is long enough, the switch recovers and opens. The coil current then flows through C_2, rapidly raising its voltage to a value sufficient to force the current to transfer to the load. The switch is allowed to open naturally during the current zero time and the severity of the recovery voltage stress is reduced by the parallel counterpulse capacitor. Furthermore, there is no fundamental dissipation of energy associated with the stray inductances in a capacitive transfer circuit. The energy $E_{Lswitch}$ stored in the opening switch inductance L_{switch} is actually transferred back to the storage coil L_1 by the action of the counterpulse capacitor. The increase in stored energy ΔE_{L1} in L_1 is given by the equation

$$\Delta E_{L1} = (Y + Y)E_{Lswitch} \quad , \qquad (2)$$

where $Y = L_{switch}/L_1$. The energy associated with the counterpulse loop inductance L_2 and the load loop inductance L_1 is supplied directly by the capacitor, which in turn receives its energy from the storage coil. Therefore, except for the energy to charge C_2 the first time, all of the energy required to effect the transfer operations ultimately comes from L_1, the energy storage coil. The only dissipative losses are those associated with normal switch conduction.

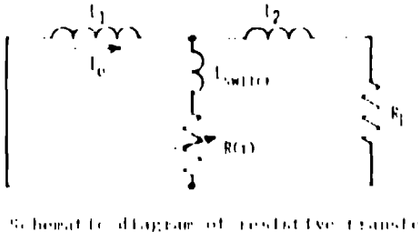

Fig. 1. Schematic diagram of resistive transfer circuit with stray inductances.

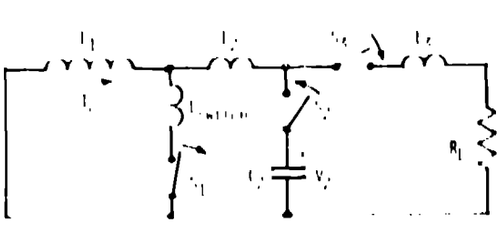

Fig. 2. Schematic diagram of capacitive transfer circuit with stray inductances.

*Work sponsored by the Los Alamos National Laboratory under auspices of the US Department of Energy.

The counterpulse method was selected as this program's primary approach due to its significant reduction in switching demands and elimination of the fundamental energy losses associated with stray inductances. To achieve repetitive operation, three different circuits capable of providing the counterpulse current repetitively were developed for various load requirements. Triggered vacuum switches[7,8] were selected for the repetitive opening switches due to their demonstrated current conduction and voltage standoff capability, fast recovery rate following a current zero, high repetition rate potential with the trigger system and relatively low cost.

New Circuit Concepts

Parallel Counterpulse Circuit

Operation. The first repetitive transfer circuit developed and tested to high power levels was the parallel counterpulse circuit (Fig. 3). The counterpulse capacitor C_2 is effectively in parallel with both the opening switch and the load. Simplified waveform representations (Fig. 4) and actual circuit waveforms (Fig. 5) from a 23-MW pulse train are shown to help illustrate the circuit operation described below. At time t_0, the start switch S_1 is closed to discharge the 1.44-mF energy storage capacitor bank C_1 through the 180-μH energy storage inductor L_1 and the vacuum interrupter opening switch VI. At t_1, switch S_2 closes at peak current to trap the energy in L_1. The 5-kA test current (Fig. 5a) through L_1 and VI then decays exponentially, depending upon L_1 and the total effective resistance of the storage loop. At t_2, the contacts of VI are mechanically parted to create a vacuum arc, a prerequisite for current zero interruption later. At t_3, the contacts are fully open, separated by a distance sufficient to withstand the eventual recovery voltage. The mechanical opening time of VI is several ms. At t_4, the precharged 30-μF counterpulse capacitor C_2 is discharged through VI and saturable reactor L_{SAT} (Fig. 5b, negative part) to produce a current zero in VI (Fig. 5a). At t_5, L_{SAT} comes out of saturation and introduces a large inductance into the counterpulse loop, "freezing" the current in VI at a near-zero value for a time dependent on the volt-second rating of the reactor and the average voltage remaining on C_2 (Fig. 5c positive part). If the current-zero time ($t_7 - t_5$) is long enough (about 20 μs) VI deionizes and opens at t_6, stressed by an initial recovery voltage equal to the voltage remaining on C_2 at that time. During the current zero time and after VI opens, the coil current is diverted from the opening switch into the counterpulse circuit, where it acts to reverse the polarity of C_2 (Fig. 5c). At t_8, when C_2 has recharged to a voltage slightly greater than the expected load voltage (Fig. 5c), the load isolation switch TVG_1 is closed to initiate the output current pulse (Fig. 5d) through the 1-Ω load resistor R_{LOAD}. The shape of the output pulse is determined by two separate circuit actions that occur on different time scales. First, the load pulse risetime is determined by the discharge of C_2 through the load and depends on the circuit parameters R_{LOAD}, C_2, and the stray inductance in the discharge loop. The rising part of the load pulse terminates when the current through the counterpulse switch TVG_2 attempts to reverse directions, i.e., when the capacitor discharge current through the load equals the coil current I_{L1} flowing through D_1, TVG_2, and C_2. The counterpulse switch effectively clips the load pulse, therefore, at the value I_{L1}, producing a fast rising pulse without overswing. The

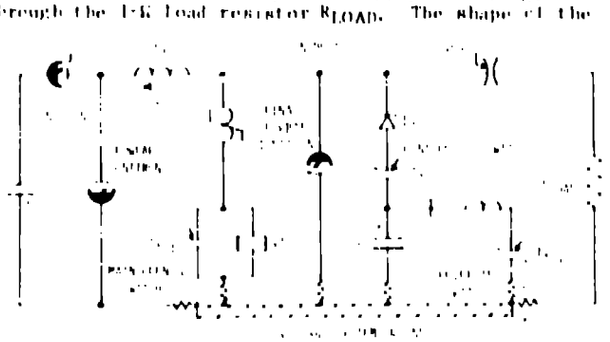

Fig. 3. Schematic diagram of parallel counterpulse, repetitive transfer test circuit.

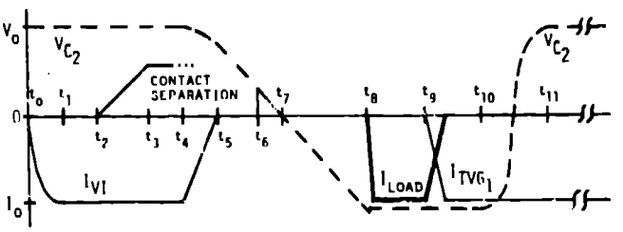

Fig. 4. Simplified waveform representations of repetitive transfer circuit operation.

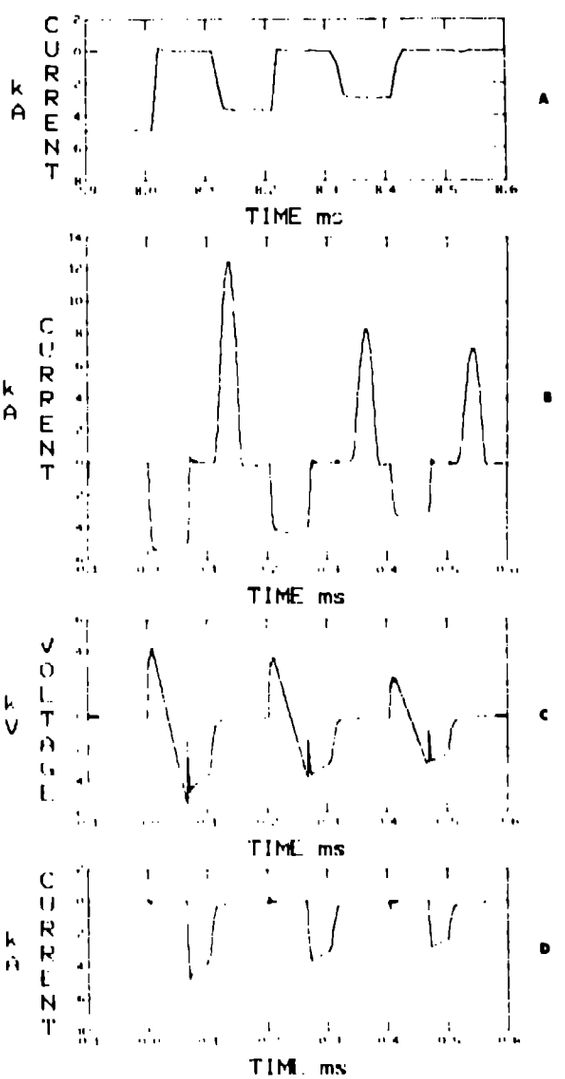

Fig. 5. Voltage and current waveforms showing 24-MW, 5-kHz operation of repetitive pulse circuit.

risetime of the load pulse can be decreased by increasing the voltage on C_2 by delaying the closing of TVG_3. This effect can be seen by the steeper risetime of the first load pulse versus the second load pulse (Fig. 5d) resulting from the higher overcharge of the capacitor during its first recharge (Fig. 5c) compared to its second recharge. Second, once TVG_2 opens to remove C_2 from the circuit (at t_8) the flat part of the load pulse is determined by the discharge of the storage inductor L_1 directly through R_{LOAD}, causing the load pulse to decay with an exponential time constant of $\mathcal{L}_1/R_{LOAD}$. If the energy in the load pulse is small compared with the total stored energy, the load current remains essentially constant. In this demonstration the load pulse energy was a significant fraction of the stored energy and the load pulse decay was appreciable (Fig. 5d). At t_9, closing the triggered main opening switch TVG_1 terminates the load pulse (Fig. 5d) and returns the system to the storage mode (Fig. 5a). Before the next transfer cycle can be initiated with another counterpulse operation, the polarity of C_2 must be reversed. This is accomplished by closing reversing switch TVG_4 at t_{10} to discharge C_2 through the small 30-μH inductor L_2 and then interrupting the reversing current (Fig. 5b positive part) at the peak reversed voltage at t_{11}. The complete cycle just described must then be repeated for each output pulse required. At the end of the pulse train, switch S_3 is closed to carry the remainder of the test current pulse and VI is closed to provide a low resistance path for coil recharging. Series diodes were required with TVG_2 and TVG_4 because their dI/dt duty was too great for reliable opening.

75-MW Results. The most significant repetitive pulse operation achieved (Fig. 6) was a seven-pulse, 75-MW pulse train delivering over 8.6 kA to the 1-Ω load at a 5-kHz rate. The pulses were 27 μs wide and had a risetime of 4 μs. The repetitive counterpulse and transfer circuit shown in Fig. 3, except with L_1 increased to 400 μH, was used. It should be noted that the system has some self-healing fault modes including triggering failures of the counterpulse switch, the reversing switch, and the load isolation switch. Pulse train recovery after load pulse dropout was actually observed during the 75-MW tests.

Bridge counterpulse circuit. The ultimate repetition rate of the repetitive transfer circuit shown in Fig. 3 is limited by the total of switch recovery times, the counterpulse operation, the counterpulse reset time, and the duration of the load pulse. The repetition rate limit could be nearly doubled if the counterpulse reset time, a significant fraction of the total cycle time, was eliminated. This was achieved by using the bridge counterpulse circuit (Fig. 7). This arrangement, also used for commutation capacitors in inverter circuits, was suggested by M. Parsons of Los Alamos. Let one half of the bridge (parts A and D) be used to counterpulse the opening switch. Then as soon as the capacitor has been recharged to the full reverse polarity, the other half of the bridge (parts B and C) can be used to provide another current counterpulse immediately. However, two additional current zero opening switches are required. This type of circuit was operated at 10 kHz and 15 kW using SCRs. A 50 A, 300 V pulse train with over 40 pulses was delivered to a 6-Ω load.

With this circuit, the ultimate repetition rate is limited by the total counterpulse time (which depends on the switch recovery times) and load pulse duration. From charge considerations the counterpulse recharge time (t_{10} - t_7 in Fig. 5) must equal the sum of the current zero time ($I_{1\text{-Zero}}$ (t_{10} - t_9)) and one half of the current fall time ($I_{1\text{-Fall}}$ (t_9 - t_8)) in the opening switch. Therefore, the total counterpulse delay time (t_{DELAY} and the minimum pulse interval) for

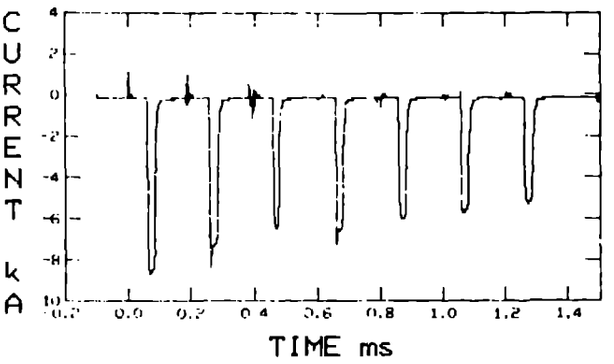

Fig. 6. Load current waveform of 75-MW, 5-kHz pulse train (repetitive pulse circuit, Fig. 3).

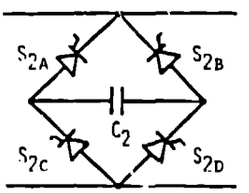

Fig. 7. Schematic diagram of bridge arrangement for high repetition rate counterpulse operation.

the bridge counterpulse circuit is given by

$$T_{DELAY} = 2T_{1\text{-Zero}} + 1.5T_{1\text{-Fall}} \quad (3)$$

Series Counterpulse Circuit

The third repetitive counterpulse and transfer circuit developed in this program is shown in Fig. 8. The counterpulse capacitor provides a current zero in the main opening switch S_2 by discharging in series through the load R_L and S_2. As with the regular parallel counterpulse circuit (Fig. 3), this circuit requires only four current zero opening switches. Furthermore, it has the advantage (as the six-switch, total, bridge counterpulse circuit, Fig. 7) of not requiring the counterpulse reset operation. The storage current I_0 initially flows through switches S_1 and S_2. When load switch S_4 closes, the precharged counterpulse capacitor C_2 discharges through R_L and the main opening switch S_2. Therefore, the initiation of the load pulse occurs simultaneously with the counterpulse initiation. When the load pulse reaches the value of the storage current I_0 flowing through S_2, the opening switch current is zero and S_2 opens. The energy remaining in C_2 is then transferred to R_L as the coil current continues to flow through S_1, C_2, S_4, and R_L. After the voltage on C_2 has reversed slightly, switch S_4 is closed to bypass C_2 and allow S_1 to open. The remainder of the load pulse current then flows through switches S_1 and S_4. The load pulse is terminated by reclosing S_2. The inverse voltage remaining on C_2 then acts to counterpulse the load switch S_4 and transfer the storage current back to S_2. An inverse clipping diode D_1 may be used in parallel with the load to reduce the energy requirement of the load counterpulse action. When the storage current has recharged C_2 to the voltage level required for the next main counterpulse, switch S_4 is closed to complete the transfer cycle and return the system to the storage mode. Compared to the parallel counterpulse circuit, this circuit produces load pulses with faster rise times and fall times, but has the disadvantage that the capacitor and switches must operate at twice the voltage level for the same load conditions. Operation at 20 A, 30 V, and 10 kHz was demonstrated with SCRs.

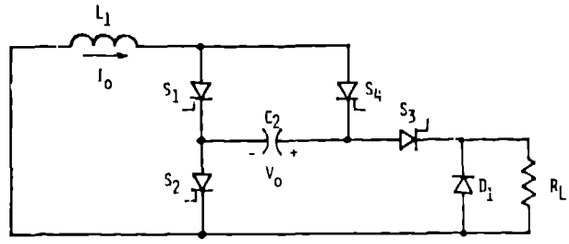

Fig. 8. Series counterpulse circuit schematic.

Analysis of Pulse Risetime

An analytical study was made to determine the effects of circuit parameters on the output pulse risetime. The circuit model used, Fig. 9 (inset), represents the circuit conditions of the parallel counterpulse circuit at the instant the load switch closes. For the case where the load inductance L_2 is much less than the storage inductance L_1, analytical solutions for the output waveforms and for the pulse risetime were obtained. A plot of the normalized risetime t_R/t_{R_0} versus the charge factor K is shown in Fig. 9, where $K = V_0/I_0R_L$, V_0 and I_0 are the initial conditions on C_2 and L_1 (resp.), the natural frequency $\omega_0 = (1/L_2C)^{1/2}$, the damping factor $\alpha = R_L/2L_2$, and the reference risetime $t_{R_0} = \pi/2\omega_0$ is for the undamped case ($\alpha = 0$). For the over-damped case ($\alpha/\omega_0 > 1$), there must be a minimum voltage on the counterpulse capacitor to achieve complete transfer to the load R_L.

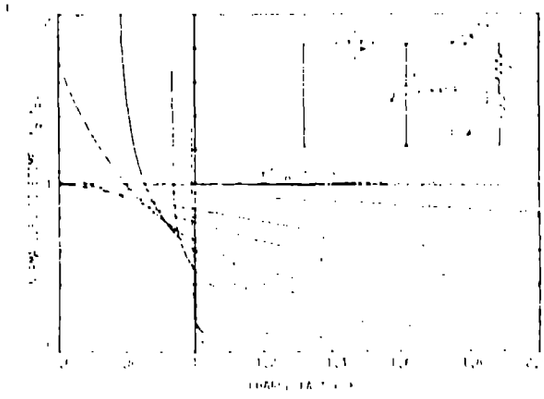

Fig. 9. Normalized risetime plot vs. voltage factor.

Potential for 10-GW, 1-kHz Pulse Generation

The upgrade potential of these repetitive pulse circuits depends primarily on developing better switches. A current zero opening switch with excellent high power, high repetition rate potential is the rod array triggered vacuum gap (RATVG), developed for the Electric Power Research Institute[11] for use in EV transmission lines. The best RATVG conducted a 150-kA (peak) ac half-cycle current pulse, interrupted at current zero, and withstood a recovery voltage of 135 kV within 150 μs.[11] Because the arc remained diffuse, similar performance is expected for current interruption duty with the fast counterpulse technique, giving the Los Alamos developed repetitive pulse circuits good potential for operating in the 100-kA, 100-kV, and 1-kHz range.

Railgun Applications

The current limit of RATVGs is still unknown. An early, experimental device carried a 250-kA (peak), ac half-cycle current pulse with an arc voltage of less than 20 V.[10] Potential for MA range operation is very good.[12] Therefore, RATVGs have potential railgun application as diverter switches to short the end of the rails as the bullet exits and as current zero opening switches to disconnect successive generators in staged drive systems. Furthermore, with an axial magnetic field applied transverse to the arc, RATVGs have potential application as repetitive opening switches required at the breech for repetitive railgun operation with inductive energy storage (Fig. 10). Transverse magnetic fields have produced arc voltages of several kV in vacuum interrupters.[13] An axial magnetic field applied to a RATVG should produce an arc voltage sufficient to force the current to transfer to a low impedance load, such as a railgun.

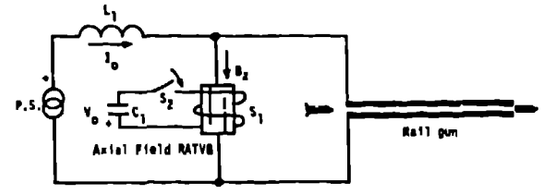

Fig. 10. Repetitive railgun using axial field RATVG.

Conclusions

New circuits and switching concepts have been developed and tested. Operation at 75 MW and 5 kHz with a 1-Ω load has proven the feasibility of using inductive energy storage for high power pulse generation at high repetition rates. Repetitive counterpulse and transfer circuits achieve highly efficient current transfer to the load and full interruption in the opening switch, and feature complete control (pulse-to-pulse) over pulse initiation, risetime, duration, and repetition rate. Risetimes faster than the μs range probably require intermediate pulse forming networks and/or magnetic switching. The transfer circuits also apply to capacitive and inductive loads. Rod array TVGs give these circuits upgrade potential to the 10-GW level.

Acknowledgments

The author thanks M. Kristiansen, J. Sarjeant, J. Rogers, and D. Sinha for technical assistance. Discussions with R. Warren, T. Burkes, A. Guenther, J. Rich, C. Goody, L. Harris, C. Kimblin, L. Hatfield, B. Nunnally, M. Parsons and others have been helpful.

References

1. S. A. Nasar and H. H. Woodson," Proc. 6th Symp. Engr. Prob. Fusion Res., San Diego, CA, IEEE Pub. No. 77CH1267-4-NPS, pp. 316-321, 1975.
2. M. Kristiansen and K. H. Schoenbach, Editors, "Workshop on Repetitive Opening Switches," NTIS Report No. AD-A110-770, 1981.
3. C. Stuerke, et al., Proc. 3rd IEEE Int. Pulsed Pwr. Conf., Albuquerque, NM, IEEE Cat. No. 81CH1662-6, pp. 328-333, 1981.
4. J. F. Barber and T. J. Trzaska, AF Wright Aero. Labs Report No. AFWAL-TR-82-2088, 1982.
5. R. P. Ford and I. M. Vitkovitsky, Proc. 13th Pulse Power Modulator Symp., Buffalo, NY, IEEE Pub. No. 78CH1371-4-ED, pp. 284-288, 1978.
6. F. M. Bonig, in Ref. 2, pp. 243-245.
7. General Electric, Schenectady, NY, Type ZR-7512.
8. EG&G, Inc., Boston, MA, Type GPV-64.
9. W. M. Parsons and F. M. Bonig, Patent application SN 341,374, filed January 21, 1982.
10. J. A. Rich, et al., IERI Report EL 1895, 1981.
11. J. A. Rich, et al., GE Report No. 81CRD321, 1981.
12. J. Rich, C. Goody, personal communication, 1982.
13. P. R. Image, et al., IEEE Trans. Plasma Science, Vol. PS-8, pp. 114-119, 1980.