A TEMPERATURE DEPENDENT SPICE MACRO-MODEL FOR POWER MOSFETS

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Abstract

A power MOSFET SPICE Macro-Model has been developed suitable for use over the temperature range -55 to 125 °C. The model is comprised of a single parameter set with temperature dependence accessed through the SPICE .TEMP card. SPICE parameter extraction techniques for the model and model predictive accuracy are discussed.

Introduction

SPICE (Simulation Program with Integrated Circuit Emphasis) has enjoyed great popularity as a circuit simulator with many versions available from industry. In the simulation of power circuits however, the active device models built into SPICE are often inadequate to properly emulate power semiconductor devices due to the integrated circuit emphasis implied in the code name. There are two choices in dealing with power semiconductor devices in SPICE, develop a new built in device model which results in a custom simulator or develop an equivalent circuit macro-model to emulate the device behavior. While a macro-model is not as robust or efficient as a built in device model, its transportability across many SPICE based circuit simulators makes the macro-model the method of choice when many simulators are used. A macro-model also has the advantage in that model behavior can often be estimated by simple inspection of the macro-model equivalent circuit.

A wide variety of SPICE macro-models for the power MOSFET have been proposed in the literature [1 - 6]. The SPICE macro-model discussed here is a compendium of the best features of those models. The resulting macro-model is shown in Figure 1. The model is quite complex and includes features that may be eliminated, such as subthreshold and leakage currents and the parasitic drain-source diode, if they are not important in the application being simulated. Because of space limitations only the dominant features of the macro-model will be discussed. Those include the core MOSFET parameters (M1), the parasitic drain, source and gate resistances (Rd, Rs and Rg) and the device capacitances (contained in Cgs, Dgd and Ddscap).

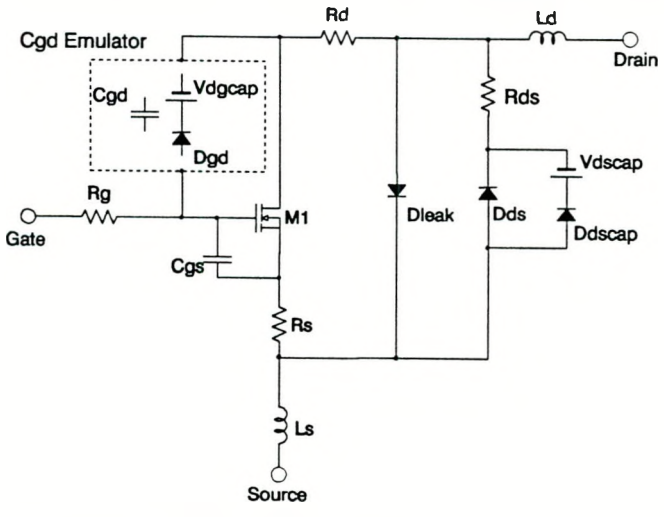

Figure 1. Power MOSFET macro-model.

The approach used to extract temperature dependent parameters is as follows. Device characteristics are measured over the temperature range of interest. Model parameters are then extracted with no compensation made for the temperature. Those "raw" parameters are then fit to the SPICE algorithms to obtain temperature coefficients for the model parameters. The temperature dependent model results are then compared to data to judge model validity and accuracy. The output of the process is a single model/parameter set valid over the temperature range.

In the discussion which follows, the sample device used to illustrate the techniques is the IRF110 power MOSFET.

DC Parameters

Core MOSFET

The IRF110 DC parameters measured at -55, -35, -15, 0, 27, 50, 75, 100 and 125 degrees centigrade are summarized in Table 1. The methods described in [2] were used to extract the threshold voltage, V_{th} and source resistance, R_s. The surface mobility, U, was obtained from a measurement of the drain current, Id, in saturation by noting that [7]

$$U = \frac{2I_dL}{WC'_{ox}(V_{gs}-V_{th}-I_dR_s)^2} = \frac{2I_dLT_{ox}}{W\epsilon_{ox}(V_{gs}-V_{th}-I_dR_s)^2}$$

where

V_{gs} = Applied gate-drain voltage (V)
W = Device width (m)
L = Device length (m)
U = Surface mobility ($m^2/V\cdot s$)
C'_{ox} = Oxide capacitance per unit area (F/m^2)
ϵ_{ox} = Permittivity of SiO_2 (F/m)
T_{ox} = Oxide Thickness (m).

TABLE 1 IRF110 MEASURED PARAMETERS VERSUS TEMPERATURE

T (K)	V_{th} (V)	R_s (Ω)	U ($cm^2/V\cdot s$)	R_d (Ω)
218	4.342	0.272	1724	0.0234
238	4.255	0.290	1582	0.0351
258	4.168	0.306	1442	0.0565
273	4.094	0.317	1324	0.0776
300	3.980	0.332	1155	0.1060
323	3.875	0.345	1024	0.1426
348	3.764	0.357	897	0.1840
373	3.661	0.370	803	0.2280
398	3.563	0.379	721	0.2698

DISCLAIMER

The gate width, length and oxide thickness for the IRF110 were estimated as 14.2cm, 3μm and 0.1μm respectively through construction analysis of the die.

The drain resistance, R_d, was extracted from a single current measurement in the linear regime of device operation ($V_{ds}<V_{gs}$). Circuit analysis of the macro-model in that regime yields

$$R_d = \frac{-(V_{gs}-V_{th}) + V_{ds}}{I_d} + \sqrt{\left(\frac{V_{gs}-V_{th}}{I_d} - R_s\right)^2 - \frac{2LT_{ox}}{I_d U W \epsilon_{ox}}}.$$

where V_{ds} = Applied Drain-Source Voltage (V)

and all other quantities have been previously defined.

The first parameter examined for temperature dependence is the threshold voltage. From [7], the threshold voltage is given by

$$V_{th} = -\frac{E_g}{2q} + \frac{kT}{q} ln\left(\frac{N_A}{n_i}\right) + \frac{T_{ox}\sqrt{2\epsilon_s N_A kT}}{\epsilon_{ox}} ln\left(\frac{N_A}{2n_i}\right). \quad (1)$$

where Eg = Silicon bandgap energy
k = Boltzman's constant = 1.38×10^{-23} J/K
q = Electronic charge = 1.6×10^{-19} C
T = Temperature (K)
N_A = Channel doping concentration (cm^{-3})
n_i = Intrinsic silicon carrier concentration
ϵ_s = Permittivity of silicon = 1.05×10^{-12} F/cm

and all other parameters have been previously defined. In addition to the temperatures that appear explicitly in Equation 1, E_g and n_i are also functions of temperature, implemented in SPICE as follows [7],

$$E_g = 1.16 - \frac{\alpha T^2}{T + \eta} \quad (2)$$

and

$$n_i = n_{io}\left(\frac{T}{T_{nom}}\right)^{3/2} e^{(E_{gnom}/2kT_{nom} - E_g/2kT)} \quad (3)$$

where
α = 7.02×10^{-4} eV/K
η = 1108 K
T_{nom} = 300 K
n_{io} = 1.45×10^{10} cm^{-3}
E_{gnom} = E_g(300 K) = 1.115 eV.

Examination of Equation 1 shows that the only free parameter, N_A, can be implicitly calculated from V_{th} at room temperature (3.98 V). That calculation yields

$$N_A = 7.66\times10^{16}\ cm^{-3}.$$

Thus, there is no external control over the behavior of the temperature dependence of V_{th} in SPICE. In other words, there are no temperature coefficients to extract.

The threshold voltage versus temperature data for the IRF110, listed in Table 1, is shown in Figure 2. Also shown in Figure 2 are SPICE predictions for V_{th} through use of the algorithms given by Equations 1 through 3. Agreement with the data is good though SPICE underestimates V_{th} at high temperatures. That behavior will cause overestimation of drain currents at high temperatures.

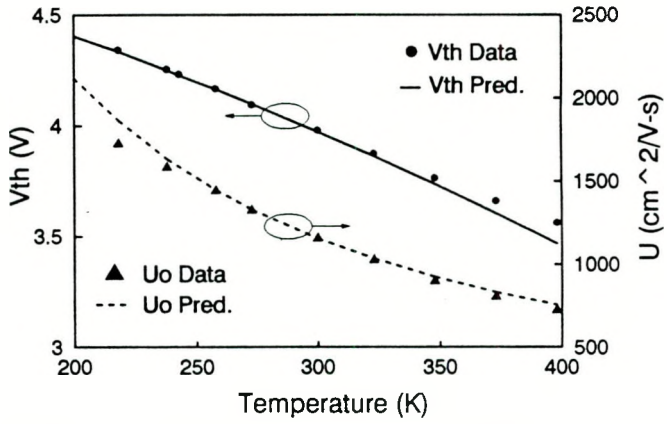

Figure 2. IRF110 V_{th} and U versus temperature.

The temperature dependence of the surface mobility, U(T), is calculated in SPICE through [7]

$$U(T) = U_o\left(\frac{T}{T_{nom}}\right)^{3/2} \quad (4)$$

where U_o is the surface mobility at 300 K. Like the threshold voltage, there are no free temperature parameters to extract in Equation 4.

The surface mobility versus temperature data for the IRF110, listed in Table 1, is also shown in Figure 2 along with the SPICE prediction for U(T) through use of the algorithm given by Equation 4 and the room temperature surface mobility, U_o. Agreement with the data is good though SPICE overestimates the surface mobility at low temperature.

Drain and Source Resistors

The next parameters discussed are the source and drain resistances, R_s and R_d. SPICE allows for variation of resistance with temperature through the following algorithm [7]

$$R(T) = R_o\{1 + X_{T1}(T-T_{nom}) + X_{T2}(T-T_{nom})^2\} \quad (5)$$

where
R(T) = Resistance at T (Ω)
R_o = Resistance at T_{nom} (Ω)
X_{T1} = Linear resistance coefficient (K^{-1})
X_{T2} = Quadratic resistance coefficient (K^{-2})

Equation 5 can be manipulated to yield

$$\frac{R(T)/R_o - 1}{T-T_{nom}} = X_{T1} + X_{T2}(T-T_{nom}). \quad (6)$$

If the left side of Equation 6 is plotted versus $T-T_{nom}$, a straight line results with slope X_{T2} and intercept X_{T1}. Such a fit was done for the R_s data listed in Table 1. The fitted line yielded,

$$X_{T1} = 1.77\times10^{-3}\ K^{-1} \quad \text{and} \quad X_{T2} = -3.63\times10^{-6}\ K^{-2}.$$

The R_s data is plotted in Figure 3. Also shown in the figure, as the solid line, is Equation 5 evaluated with the temperature coefficients given above. Agreement between the algorithm and data is good.

A similar analysis done on the R_d data listed in Table 1 yields the following coefficients for R_d,

$$X_{T1} = 1.1\times10^{-2}\ K^{-1} \quad \text{and} \quad X_{T2} = 1.3\times10^{-5}\ K^{-2}.$$

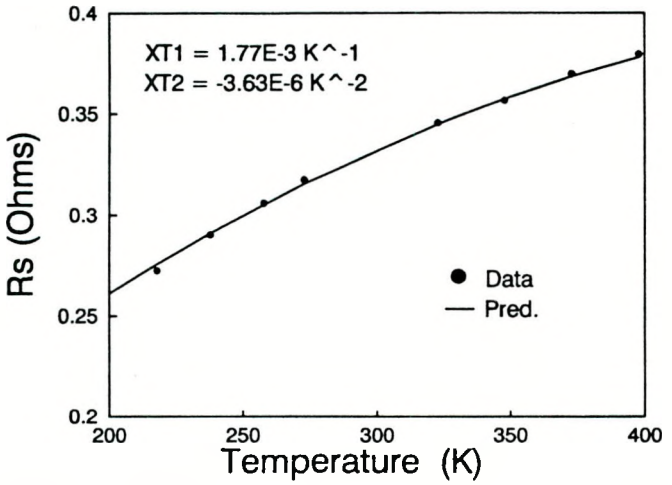

Figure 3. IRF110 source resistance versus temperature.

The parameters extracted above were used in the SPICE macro-model to calculate IRF110 DC characteristics over temperature. Figure 4 shows drain current versus gate voltage at -55, 27 and 125 °C. Symbols denote data while the solid lines are the SPICE results. Agreement with the data is acceptable noting that the current at 125 °C is overestimated due to underestimation of V_{th} as shown in Figure 2.

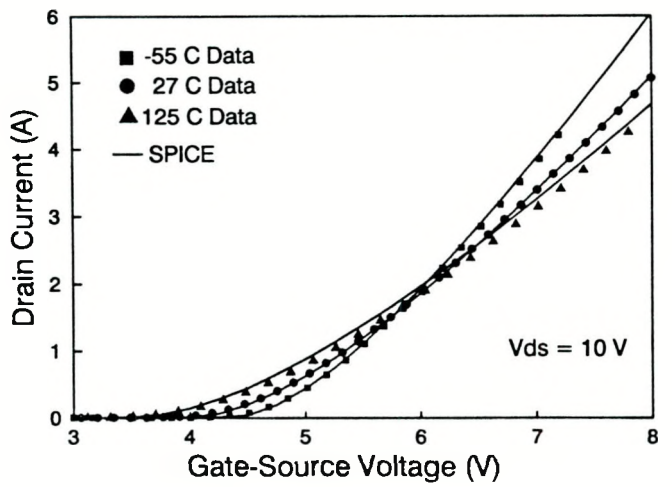

Figure 4. SPICE results compared to data at three temperatures for the IRF110 transfer characteristic.

Figure 5 shows drain current versus drain voltage for fixed gate bias at -55, 27 and 125 °C. Symbols denote data while the solid lines are the SPICE results. Agreement with the data is good again noting that the current at 125 °C is overestimated.

AC PARAMETERS

As discussed in the introduction, the only AC parameters of concern for simulation at temperature are the device capacitances. The internal capacitances, C_{gd}, C_{gs} and C_{ds}, are calculated from the input, output and reverse capacitances, C_{iss}, C_{oss} and C_{rss}, through

$$C_{gd} = C_{rss} ,$$

$$C_{gs} = C_{iss} - C_{rss} ,$$

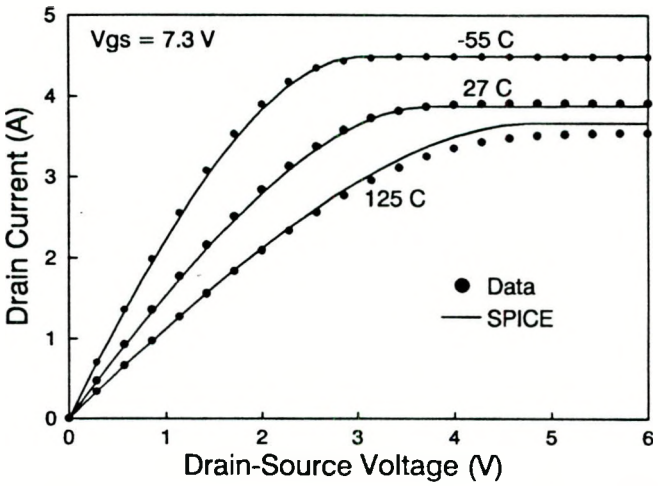

Figure 5. SPICE results compared to data at three temperatures for the IRF110 linear characteristic.

and

$$C_{ds} = C_{oss} - \frac{(C_{iss} - C_{rss})C_{rss}}{C_{iss}} .$$

When the drain is biased positive with respect to the source and gate, C_{gd} and C_{ds} have strong bias dependencies similar to those of reverse biased diodes. Thus, diodes are used to simulate those capacitances, as shown in Figure 1. C_{gs} is a fixed capacitor and shows no temperature dependence.

As discussed above, C_{ds} and C_{gd} will be emulated as diode capacitances. Reversed biased diode capacitance in SPICE is simulated through the following relation [7],

$$C = C_{jo}\left(1 + \frac{V_{ds}}{V_j}\right)^{-m} \qquad (7)$$

where

C_{jo} = Junction capacitance @ 0 V (F)
V_j = Built-in junction potential (V)
m = Junction grading coefficient (unitless).

Note that the convention is such that V_{ds} is positive when the junction is reverse biased. The parameters are extracted by fitting Equation 7 to capacitance versus bias data, typically over the range 0 to 40 V.

Table 2 summarizes the extracted parameters for the IRF110 capacitances at four temperatures. Note from the Table that C_{gs} shows no significant variation with temperature, as expected. The C_{gd} parameters

TABLE 2 IRF110 CAPACITANCE PARAMETERS

		D_{dscap} Capacitance			D_{gd} Capacitance		
T (K)	C_{gs} (pF)	C_{jo} (pF)	m	V_j (V)	C_{jo} (pF)	m	V_j (V)
218	278	426	0.386	0.443	248	0.612	0.181
300	284	473	0.391	0.375	247	0.608	0.150
348	282	519	0.402	0.322	255	0.622	0.180
398	284	585	0.407	0.255	259	0.623	0.174

also show little variation with temperature. However, the gate-drain capacitance will be treated here as SPICE will adjust the diode capacitance parameters with temperature, with no way to disable that feature. Thus, a means must be found to remove the temperature tracking in SPICE for diode capacitances.

Of the three diode capacitance parameters, C_{jo}, m and V_j, SPICE adjusts only C_{jo} and V_j with temperature as the grading coefficient, m, should show no temperature dependence. The junction potential, V_j, is calculated as a function of temperature by [7]

$$V_j(T) = V_{jo}\frac{T}{T_{nom}} - \frac{3kT}{q}ln\left(\frac{T}{T_{nom}}\right) - \frac{E_{gnom}T}{qT_{nom}} + \frac{E_g(T)}{q} \qquad (8)$$

where $E_g(T)$ is given by Eq. 2 and $V_{jo} = V_j(300\ K)$. The zero bias capacitance, C_{jo}, is given by [7]

$$C_{jo}(T) = C_{jo}(T_{nom})\left\{1+m\left[0.0004(T-T_{nom})+1 - \frac{V_j(T)}{V_{jo}}\right]\right\} \qquad (9)$$

Equation 8 is plotted for diodes D_{gd} and D_{dscap} in Figure 6 as a function of temperature based on the V_{jo} listed in Table 2. Also shown in the figure is the rest of the V_j data from Table 2. Note that the temperature dependence given by Equation 8 does not track with the data. Also, the calculated value of V_j at 125 °C is negative for D_{gd}. That value causes Equation 9 to yield complex values for C_{jo} at 125 °C. Since complex values of C_{jo} are not allowed in SPICE, the simulation would cease due to a computational error. Thus, SPICE cannot simulate the MOSFET at 125 °C given the value of V_{jo} for diode D_{gd}.

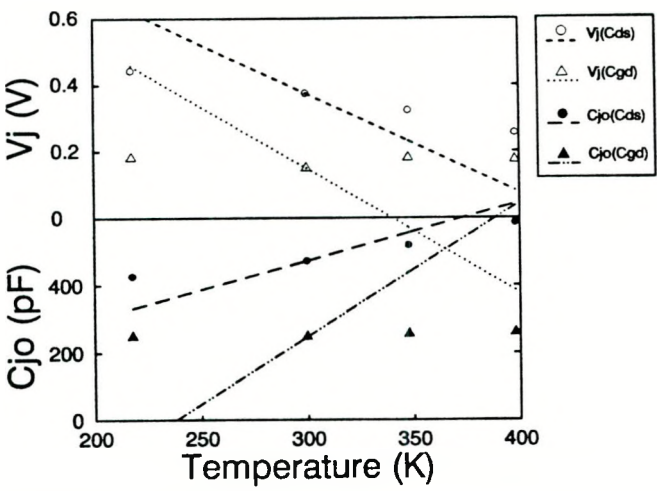

Figure 6. V_j and C_{jo} versus temperature for the IRF110 C_{gd} and C_{ds} simulation diodes.

Equation 9 is plotted in Figure 6, for diodes D_{gd} and D_{dscap}, as a function of temperature based on the room temperature C_{jo} listed in Table 2. Also shown in the figure is the rest of the C_{jo} data from Table 2. Note that the temperature dependence given by Equation 9 does not track the D_{gd} data though it does follow the D_{dscap} data fairly well. Also, the calculated value of C_{jo} at -55 °C is negative for diode D_{gd}. Negative capacitance will cause convergence problems in the simulation. Thus, SPICE cannot simulate the MOSFET at -55 or 125 °C given the values of V_{jo} and C_{jo} listed in Table 2 for diode D_{gd}.

Since $C_j(T)$ depends on $V_j(T)$ in Equation 9, the place to start in trying to achieve the correct temperature dependence of the capacitances is with $V_j(T)$. From Figure 6, it is apparent that the slopes of the calculated junction potentials do not match those of the data. The slope of the junction potential versus temperature is found by taking the derivative of Eq. 8

$$\frac{\partial V_j}{\partial T} = \frac{V_{jo}}{T_{nom}} - \frac{3k}{q}ln\left(\frac{T}{T_{nom}}\right) - \frac{3k}{q} - \frac{E_{gnom}}{qT_{nom}} - \frac{\alpha T}{T+\eta}\left(2-\frac{T}{T+\eta}\right). \qquad (10)$$

Evaluating Equation 10 at T = 300 K yields,

$$\left.\frac{\partial V_j}{\partial T}\right|_{T=300\ K} = \frac{V_{jo}}{300\ K} - 4.275\times10^{-3}\ V/K. \qquad (11)$$

Thus, the slope of the junction potential with respect to temperature at room temperature depends upon V_{jo}. The approach used is to select a new V_{jo}, V_{jo}', based upon the measured temperature dependence and adjust the other parameters of the capacitance simulation diodes to compensate for V_{jo}'.

Straight lines were fit to the data in Figure 6. The slopes from those fits were used with Equation 11 to determine values of V_{jo}' which gave the correct slope. Performing that analysis resulted in the following,

D_{dscap}: $V_{jo}' = 0.963$ V
D_{gd}: $V_{jo}' = 1.293$ V.

Now that V_{jo}' has been found it is necessary to find a value of $C_{jo}'(T_{nom})$ to give the correct capacitance characteristic. Since the capacitances should be equal at all biases, Eq. 7 yields, for large bias,

$$C_{jo}'(T_{nom}) = C_{jo}(T_{nom})\left(\frac{V_{jo}}{V_{jo}'}\right)^m. \qquad (12)$$

Substituting the values of Vjo' calculated above into Equation 12 yields

D_{dscap}: $C_{jo}'(T_{nom}) = 325$ pF
D_{gd}: $C_{jo}'(T_{nom}) = 66.7$ pF.

The new Cjo' for the capacitance simulation diodes will severely underestimate the capacitance at low bias. To compensate for that effect, a battery is added to each diode to reduce the magnitude of the effective bias across the diode. Those batteries are depicted in Figure 1. Analysis shows that the battery voltage should equal Vjo'-Vjo for each capacitance simulation diode.

A summary of the procedure for extracting parameters for the temperature compensated diode/battery follows,

1) Find the slope of V_j versus T at 300K
2) Calculate V_{jo}' from Equation 11
3) Calculate C_{jo}' from Equation 12
4) $V_{cap} = V_{jo}' - V_{jo}$.

The procedure outlined above was performed for the IRF110 capacitance versus temperature data. The simulation results are compared to the data in Figure 7 for the drain-source and gate-drain capacitance simulation diodes respectively. Agreement between simulation and measured data is good.

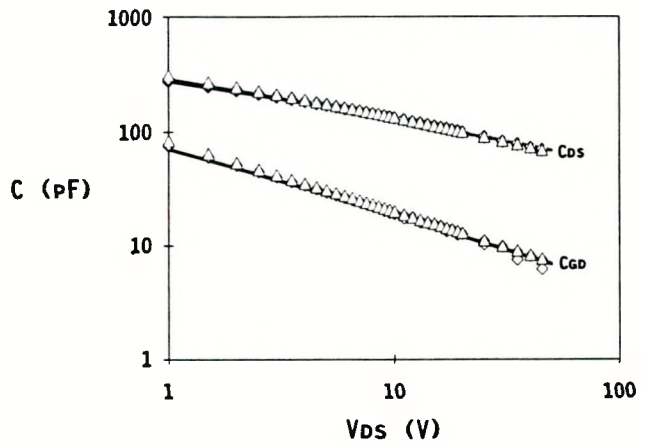

Figure 7. IRF110 gate-drain and drain-source capacitance simulations compared to data at three temperatures.

Gate Resistance and Switching Speed

The gate resistance shows no temperature dependence. A transient analysis yields the following expression for the gate resistance extracted from switching speed data,

$$R_g = -\frac{t_{on}}{C_{gs} ln\left(1 - \frac{V_{th}}{V_o}\right)} - R_s$$

where V_o = Gate drive source voltage (V)
V_{th} = Threshold voltage (V)
C_{gs} = Gate-source capacitance (F)
R_s = Source resistance of gate drive (Ω)
R_g = Gate resistance (Ω).
t_{on} = Time to turn on (s).

Data for the IRF110 yielded R_g = 18.5 Ω. An example of a switching speed waveform is shown in Figure 8. There, the gate and drain voltages are shown as a function of time. The measured data is represented by the noisy lines. The smooth lines are SPICE simulations using the macro-model shown in Figure 1 with the parameters extracted in this paper. Agreement between simulation and data is good.

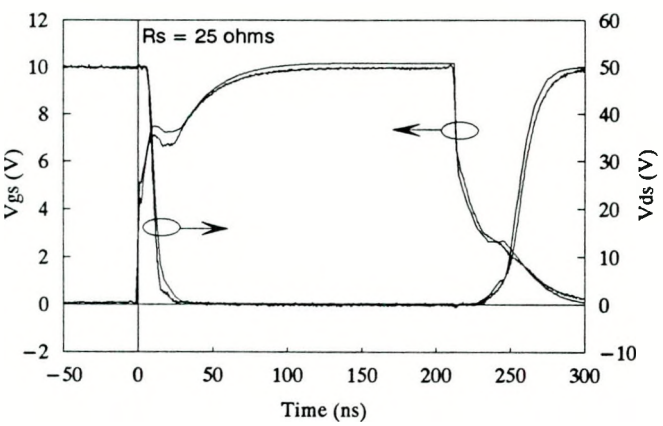

Figure 8. Switching speed simulation compared to data for the IRF110.

Summary and Conclusions

A temperature dependent SPICE macro-model for power MOSFETs has been presented for the first time. Through use of the SPICE built in temperature functions, it is possible to accurately simulate the power MOSFET response over the temperature range of interest. Though complex, the model and approach to parameter extraction is straightforward. As all the parameter extraction algorithms are analytic in nature, automation of the extraction process is straightforward and requires no special optimization routines. The addition of a power MOSFET model to the SPICE code would result in more robust and efficient simulations. However, the lack of transportability among the plethora of SPICE based simulators makes that approach attractive only in situations where a standard simulator is used throughout a design organization.

Acknowledgments

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