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HIGH-POWER RADIO-FREQUENCY BINARY PULSE-COMPRESSION EXPERIMENT AT SLAC*

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Using rf pulse compression it will be possible to boost the 50- to 100-MW output expected from high-power microwave tubes operating in the 10- to 20-GHz frequency range to the 300- to 1000-MW level required by the next generation of high-gradient linacs for linear colliders. A high-power X-band three-stage binary rf pulse compressor has been implemented and operated at the Stanford Linear Accelerator Center (SLAC). In each of three successive stages, the rf pulse-length is compressed by half, and the peak power is approximately doubled. The experimental results presented here have been obtained at power levels up to 25-MW input (from an X-Band klystron) and up to 120-MW output (compressed to 60 nsec). Peak power gains greater than 5.2 have been measured.

The principle of operation of a binary pulse compressor (BPC) is described in detail elsewhere.¹ Conceptually, time-intervals of a klystron pulse are separately delayed by different amounts, and then recombined into a shorter pulse of greater amplitude, as shown in Figure 1. A schematic of a two-stage BPC is shown in Figure 2. It works as follows: Two rf inputs are phase-coded into four time-bins with phases 0 or π , denoted by "+" or "-", respectively. A 3-dB coupler or "hybrid", labeled H1 in Figure 2, acts as the "switch" in Figure 1. The hybrid combines the two inputs and directs the combined power to either output port, depending on the relative phase of the two inputs. In this way, the hybrid can produce output pulses with half the pulse-length and twice the peak power of the input pulses (in the "ideal" lossless case), properly phase-coded for the next stage.

The compressed pulses are sequential, not coincident. They are made coincident at hybrid H2 by delay D1. In the second stage, H2 again doubles the peak power and halves the pulse-length. The two compressed pulses again are made coincident by delay D2 (half as long as D1). A three-stage system requires another hybrid and delay-line, and more complicated phase-coding. The two output pulses from any number of stages may be used separately to energize a linac, or may be combined (by an additional hybrid) into a single higher-power pulse.

Experiments at SLAC with a low-power (non-vacuum) two-stage X-band BPC,² and low-power experiments with the three-stage high-power BPC,³ have already been reported. Here, we report on recent high-power tests of the

three-stage X-band BPC that resulted in 120-MW compressed pulses.

In reality, the BPC peak power gain per stage is less than two because of losses in the delay-lines, the hybrids, and other components. For practical application to linac rf systems, the losses must be sufficiently small to produce reasonable efficiencies. Therefore, we have chosen to work with the low-loss TE₀₁ mode in overmoded 2.81-inch-diameter circular waveguide (WC281) for the delay-lines, and standard rectangular X-band waveguide (WR90) for the non-delayed connections.

Our hybrids are designed with one TE₀₁-mode input of 1.84-inch-diameter circular waveguide (WC184), and one input of WR90 rectangular waveguide. Similarly, one output is WC184, and the other is WR90. Trombone bends of 180° are necessary to place the start and end of each delay-line in close physical proximity. All our delay-line bends are fabricated from corrugated 1.84-inch-diameter circular guide. Linear tapers are used for transitions between WC281 and WC184. We use mode transducers to convert from the fundamental TE₁₀ mode in rectangular guide to the circular TE₀₁ mode in circular guide.

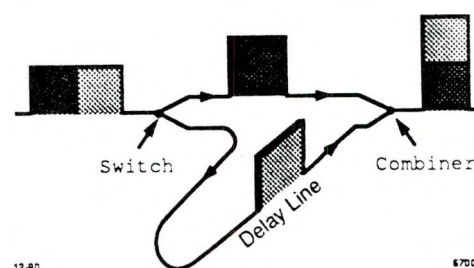


Figure 1: The concept of a binary pulse compressor (BPC).

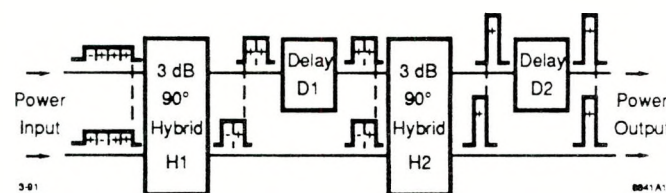


Figure 2: Electrical schematic of a two-stage BPC.

The insertion losses of the individual components have been measured separately, except for the circular waveguide loss which was calculated. The hybrid losses differed depending on whether power was combined into the circular or rectangular output ports, and were not the same for all four hybrids, indicating that better design could reduce the losses. The component losses are given in Table 1, and can be used to predict the distribution of power losses, and therefore the power gain expected, in a BPC system.

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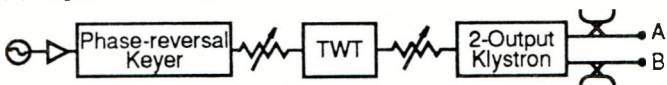
Table 1: Insertion losses of individual components.

| Component | Insertion Loss | |
|--|-----------------|--------------|
| WC281 (2.81-inch-I.D.) | 1.1 dB/ μ s | 22%/ μ s |
| WC184 (1.84-inch-I.D.) | 3.6 dB/ μ s | 56%/ μ s |
| WR90 (0.9 \times 0.4-inch ²) | 0.1 dB/m | 2%/m |
| H1 circular output port | 0.12 dB | 2.8% |
| H2 circular output port | 0.11 dB | 2.6% |
| H3 circular output port | 0.10 dB | 2.2% |
| H4 circular output port | 0.08 dB | 1.9% |
| H1 rectangular output port | 0.35 dB | 7.7% |
| H2 rectangular output port | 0.35 dB | 7.8% |
| H3 rectangular output port | 0.32 dB | 7.1% |
| H4 rectangular output port | 0.33 dB | 7.4% |
| Mode transducer | 0.07 dB | 2% |
| Bend, phase-shifter, tapers | 0.1 dB | 2% |
| Taper (2.81-to-1.84-inch-I.D.) | 0.01 dB | 0.2% |

An electrical schematic of the three-stage high-power X-band BPC is shown in Figure 3. The corresponding physical assembly is shown schematically in Figure 4. Since only a single X-band klystron currently is available at SLAC,⁴ we have configured the BPC phase-reversal keying and delay-line lengths for two identically phase-modulated inputs, shifted in time by three bins by delay D1 in Figure 4, following a suggestion by Latham.⁵ The klystron has two output ports, both phase-modulated identically.

Variable phase-shifting in the delay-lines is necessary to obtain proper relative phasing of the two inputs to each hybrid. This high-power phase-shifting is accomplished using motor-controlled bellows to stretch the delay-line trombone bends by up to 720° of rf phase in steps of 3°.

(a) High-Power Input Circuit



(b) Three-Stage Binary Pulse Compressor Circuit

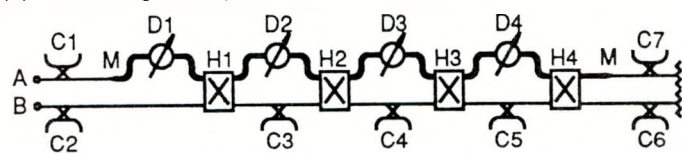


Figure 3: Electrical schematics of (a) the high-power input circuit and (b) the binary pulse compressor. "H" indicates 3-dB couplers (hybrids). "D" indicates delay-lines with trombone phase-shifters. "C" indicates 55-dB directional couplers. "M" indicates rectangular-to-circular mode transducers.

Each of the two outputs of Stage-3 could be used to power an accelerator section. However, the three-stage BPC we have implemented has a fourth hybrid (H4) which permits the two Stage-3 outputs to be combined into a single output by adjusting the high-power phase-shifter in delay-line D4. While some power is lost in the combiner H4, this highest-power single output is expected to be useful for high-power studies of test cavities and accelerator structures.

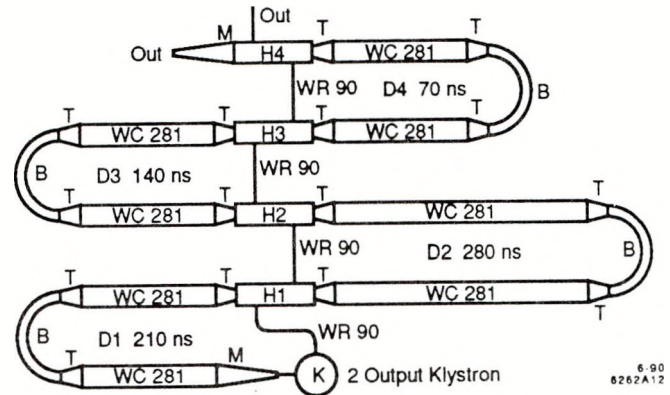


Figure 4: Physical layout of the BPC components. "WR90" is rectangular waveguide. "WC281" is 2.81-inch-diameter circular waveguide. "H" indicates 3-dB couplers (hybrids) that couple WR90 to WC184. "B" indicates WC184 bends with phase-shifters. "T" indicates linear tapers from 1.84-inch to 2.81-inch-diameter. "M" indicates rectangular-to-circular mode transducers.

The three-stage BPC is brought into operation by phase-modulating the low-level input rf in 70-nsec time-bins, using the phase-reversal keyer in Figure 3a. Then, stage-by-stage, the high-power phase-shifters in the delay-lines (D1, ..., D4) in Figure 3b are adjusted to obtain the relative phasing of the two inputs to each hybrid (H1, ..., H4) appropriate for maximum power multiplication.

We have tested the three-stage BPC by compressing 1-kW traveling-wave-tube pulses, and 5- to 25-MW klystron pulses. Rf power measurements were made at the 55-dB directional couplers following each stage (C1, ..., C7 in Figure 3b), using tunnel diode detectors and a fast oscilloscope. Absolute power resolution is about 5%. We have checked the power reflected at each stage and found that it is less than 4% of the forward power.

The pulse compression process, stage-by-stage starting from the klystron pulse, is shown by experimentally observed pulses in Figures 5 and 6. The rise-time of the compressed pulses appears to be dominated by the switching time of the low-power phase reversing electronics. The output pulses are not quite flat, possibly due to suspected phase variation in either the klystron or the BPC.

The highest peak power levels attained to date are 25 MW from the klystron, and 120 MW from the BPC. Stage-by-stage peak power gains (defined as the sum of outputs divided by the sum of inputs) are given in Table 3. The measured losses of individual components (Table 1) have been used to predict the distributed losses in each stage of the three-stage BPC, and to predict the power gain expected at each stage. The expected gains are shown in Table 3, and are consistent with the measured gains. The peak power gain of the three-stage BPC is greater than 5.2 at all power levels. There is no evidence that we have reached the threshold of electrical breakdown with 120-MW compressed pulses.

The amplitude variation in the compressed pulse of Figure 6 has not gone unnoticed. In the near future, we hope to study the phase and amplitude stability of the compressed pulses. As the performance of X-Band

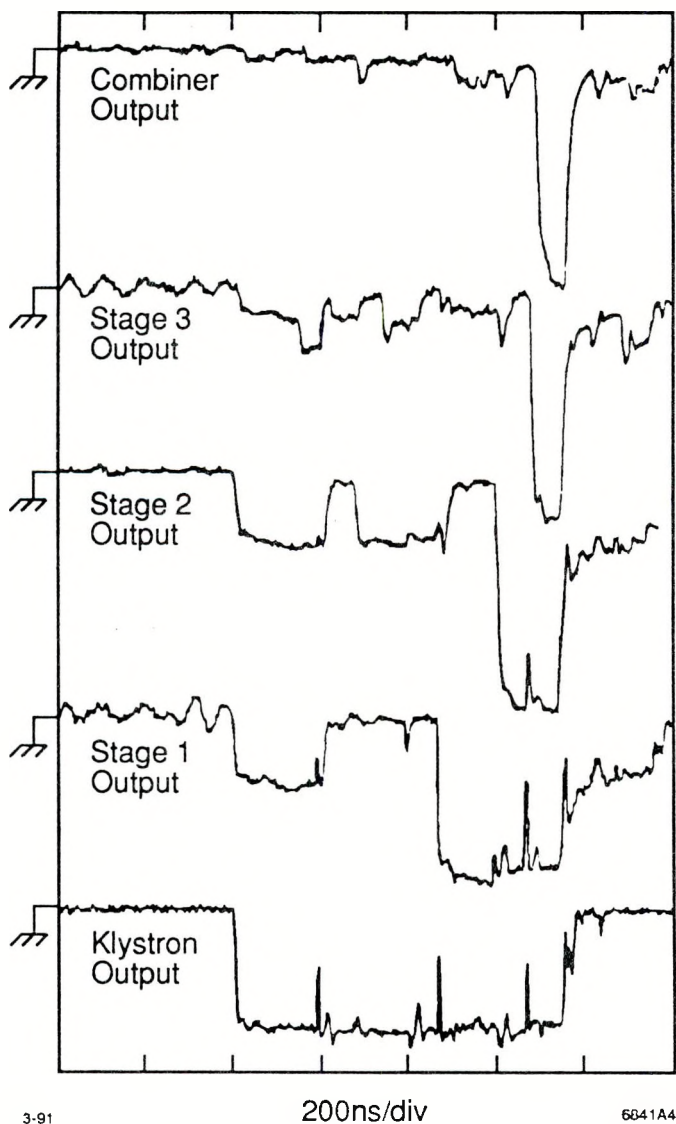


Figure 5: Rf power pulses measured at each stage of pulse compression. The combiner pulse is the sum of the two Stage-3 outputs.

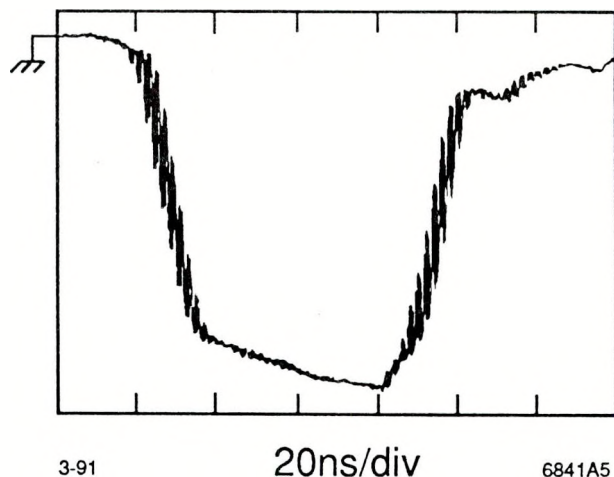


Figure 6: Rf power pulse measured at the output of the combiner.

Table 3: Peak power gains.

| | Stage 1 | Stage 2 | Stage 3 | Stages 1-3 |
|---------------|---------|---------|---------|------------|
| Lossless Gain | 2 | 2 | 2 | 8 |
| Expected Gain | 1.8 | 1.8 | 1.8 | 6.1 |
| Measured Gain | | | | |
| 1-kW Input | 1.8 | 1.8 | 1.8 | 5.8 |
| 5-MW Input | 1.8 | 1.8 | 1.8 | 5.4 |
| 20-MW Input | 1.7 | 1.6 | 1.9 | 5.2 |

klystron prototypes⁴ improves, we hope to test the three-stage pulse compressor at higher power levels, approaching 100-MW input and 500-MW compressed pulse output. When two X-Band klystrons become available, the binary pulse compressor can be reconfigured to utilize both of these high-power sources. If each klystron produces 100 MW, we expect up to 1-GW compressed pulses after combining to a single output. At this power level, the peak surface fields in the hybrid slots and in the WR90 guides are estimated to be only 80 MV/m, well below the expected threshold for breakdown.

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References

1. Z. D. Farkas, "Binary Peak Power Multiplier and Its Application to Linear Accelerator Design," *IEEE Trans. MTT-34* (1986), p. 1036-1043.
2. Z. D. Farkas, G. Spalek, and P. B. Wilson, "RF Pulse Compression Experiment at SLAC" (SLAC-PUB-4890), in Proceedings of the 1989 IEEE Particle Accelerator Conference (Chicago, Illinois), IEEE Catalog No. 89CH2669-0, pp. 983-986.
3. T. L. Lavine, G. Spalek, Z. D. Farkas, A. Menegat, R. H. Miller, C. Nantista, P. B. Wilson, "Binary RF Pulse Compression Experiment at SLAC" (SLAC-PUB-5277), in Proceedings of the 2nd European Particle Accelerator Conference (Nice, France, June 12-16, 1990), Editions Frontières, Gif-sur-Yvette, France, 1990, pp. 940-942.
4. A. E. Vlieks *et al.*, "100-MW Klystron Development at SLAC" (SLAC-PUB-5480), published in these proceedings.
5. P. E. Latham, "The Use of a Single Source to Drive a Binary Peak Power Multiplier," 1988 Linear Accelerator Conference (Williamsburg, Virginia), CEBAF-R-89-001, pp. 623-624.