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AUTOMATED ARRAY ASSEMBLY, PHASE II

Quarterly Report No. 5, January 1—March 31, 1979

By
R. V. D'Aiello

March 1979

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RCA Laboratories
Princeton, New Jersey

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Solar Energy

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R. V. D'Aiello
RCA Laboratories
Princeton, New Jersey 08540

QUARTERLY REPORT NO. 5

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The JPL Low-Cost Silicon Solar Array Project is funded by DOE and forms part of the DOE Photovoltaic Conversion Program to initiate a major effort toward the development of low-cost solar arrays.

Prepared Under Contract No. 954868 For

JET PROPULSION LABORATORY
CALIFORNIA INSTITUTE OF TECHNOLOGY
Pasadena, California 91103

PREFACE

This Quarterly Report, prepared by RCA Laboratories, Princeton, NJ 08540, describes the results of work performed from January 1, 1979 to March 31, 1979 in the Energy Systems Research Laboratory, B. F Williams, Director; Materials and Process Laboratory, Solid State Division, Somerville, NJ, R. Denning, Manager; and at the Advanced Technology Laboratory, Government and Commercial Systems, Camden, NJ, F. E. Shashoua, Director. The Project Scientist is R. V. D'Aiello and the Project Supervisor is A. H. Firester, Head, Process and Applications. Others who participated in the research and writing of this report are:

E. C. Douglas C. Wu	-	Ion implantation
K. Bube	-	Screen printing
W. Kern	-	Spray-on AR coating
J. Toner	-	Cost analysis
R. Scott P. Coyle	-	Interconnect and panel assembly
L. Guarino	-	Processing

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SECTION I

SUMMARY

The work reported for this quarter represents a new phase of activity directed toward a cost and performance evaluation of three manufacturing sequences designed to convert silicon sheet and wafers into solar-cell array modules. Section III describes the details of these sequences and provides a near-term cost analysis for each.

Section IV describes the progress made during this quarter in materials acquisition, mask design, equipment setup and qualification, process verification and refinement, and new equipment design and construction. Some highlights are:

(1) Installation and qualification of a production model screen printer for thick-film metallization and autocoater for spray-on antireflection (AR) coating.
(2) Laminations of three 4-ft-square double-glass panels.
(3) Design and construction of an automatic electrical test system.

Section V discusses the status of our overall program plan and outlines plans for the next quarter.

SECTION II

INTRODUCTION

In our previous work, we have identified cost-effective processes for large-scale silicon solar-panel production, brought those processes needing development to a state of technological readiness, and verified each process by experimental production of solar cells and panels. A selling price of less than $500/kW requires that these processes be assembled to form a manufacturing sequence with internal compatibility and the capability of operating at the estimated high throughput and yield.

In this present program, three such manufacturing sequences were selected and will be evaluated and compared on the basis of their cost/performance effectiveness. This evaluation will be performed by studying the production flow for each sequence involving the processing of 2420 solar cells, which will be used in the fabrication of 20 solar panels. The present production plan includes the fabrication of 1040 cells of the 2420 cells from EFG ribbon and web silicon* with the remainder made in "solar-grade"** so that we can evaluate and gain experience in the handling of sheet silicon and test the sensitivity of these sequences to the starting silicon characteristics.

*EFG ribbon to be purchased from Mobil-Tyco Solar Energy Corp., Waltham, MA. Web silicon to be purchased from Westinghouse Research and Development Center, Pittsburgh, PA. The quantity of cells and production scheduling depend on the delivery schedule from these vendors.

**"Solar-grade" silicon is a product of the Monsanto Corp., St. Louis, MO. These are 3-in.-diameter n- or p-type, 1/2 to 2 Ω-cm, round silicon wafers, received in a "saw-cut" form.

SECTION III

DESCRIPTION OF MANUFACTURING SEQUENCES AND COST ANALYSIS

This quarterly report describes the first phase of a 9-month effort to assess the cost and performance of three candidate manufacturing sequences for the production of silicon solar panels. These sequences were assembled from processes whose costs were analyzed and found to be in an acceptable range [1] and for which a technical verification in the form of experimental production was conducted [2]. The three manufacturing sequences are shown schematically in Figs. 1 and 2, and a detailed listing of each process is given in Tables 1, 2, and 3. The number of cells and panels to be produced with each manufacturing sequence is given in Table 4.

A. COST ANALYSIS

As a first step in evaluating these sequences, a cost analysis was performed for each. These estimates assume existing or near-term technologies and equipment and have excluded the starting silicon cost. An annual production rate of 30 MW/year was assumed for each sequence, and a cell efficiency of 14% was assumed for sequences I and II and 16% for sequence III since in our experience, $p^+/n/n^+$ cells have yielded higher average efficiency than $n^+/p/p^+$ cells [3,4].

The results of these cost analyses are given in Tables 5, 6, and 7.* The cost differential between the first two and the third sequence is due primarily to the high cost of the ion-implantation step since existing implanters which have relatively low throughputs were assumed. Although sequence I has the lowest calculated cost, several technical questions discussed below concerning the aluminum p^+ back surface contact process must be answered before final conclusions on relative costs can be made. In addition, each process has technical merits which, when considered in the light of future developments in the

1. R. V. D'Aiello, Automated Array Assembly, Final Report, prepared under Contract No. 954352 for Jet Propulsion Laboratory, DOE/JPL-954352-77/4, December 1977.
2. R. V. D'Aiello, Automated Array Assembly, Phase II, Interim Report, prepared under Contract No. 954868 for Jet Propulsion Laboratory, DOE/JPL-954868-79/1, January 1979.
3. M. S. Bae and R. V. D'Aiello, Appl. Phys. Lett. 31, 285 (1977).
4. J. G. Fossum and E. L. Burgess, Appl. Phys. Lett. 33, 238 (1978).

*All figures reflect 1978 dollars.

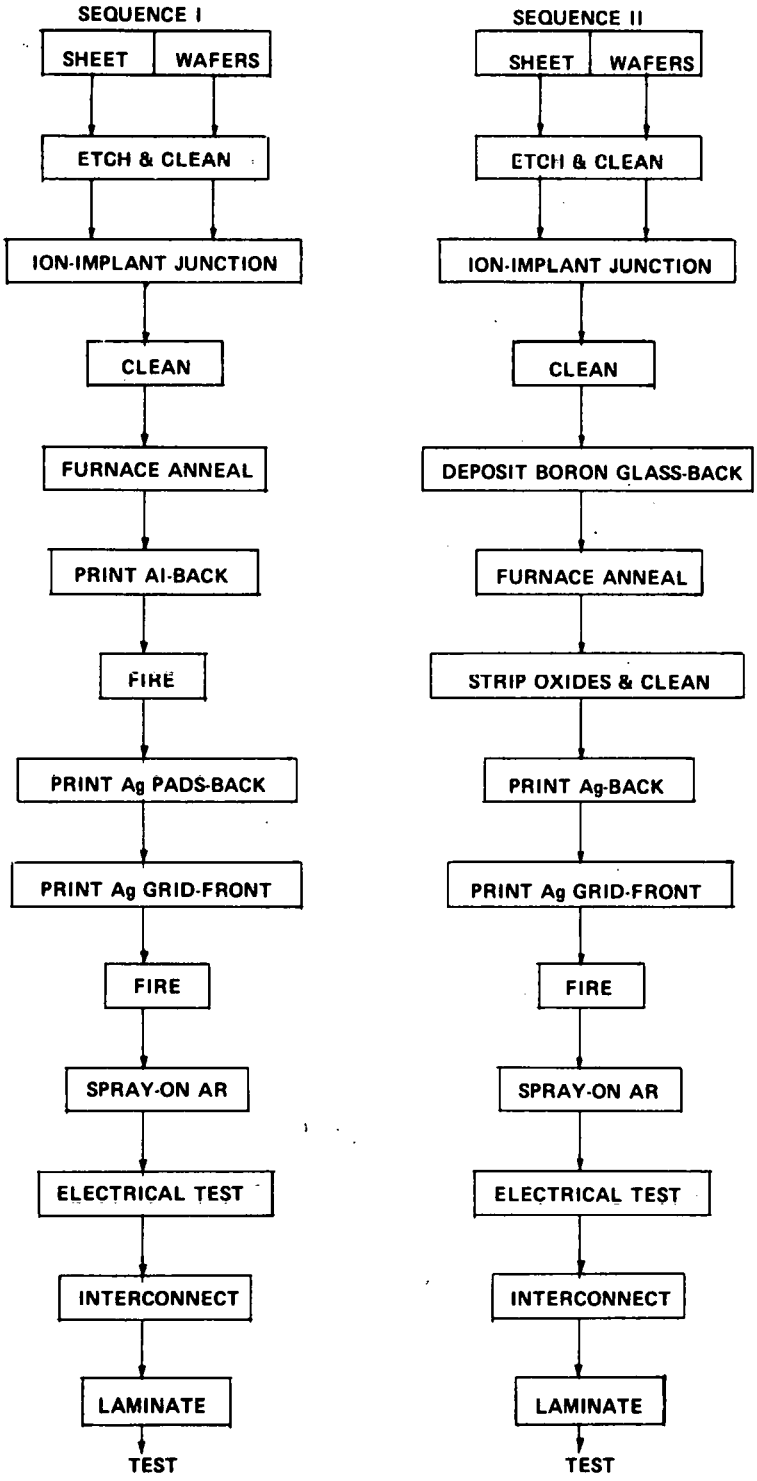


Figure 1. Manufacturing sequences I and II.

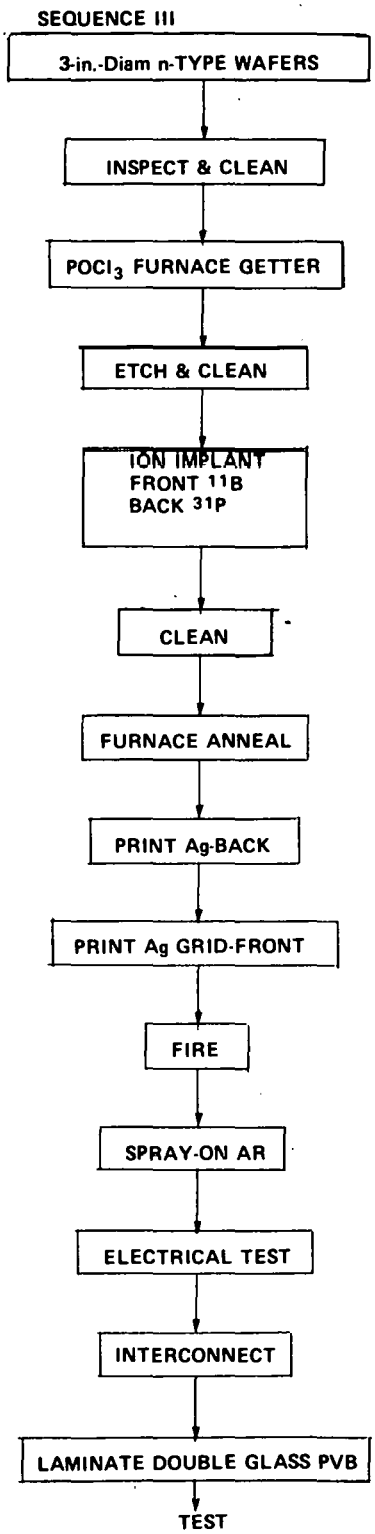


Figure 2. Manufacturing sequence III.

TABLE 1. SEQUENCE I DETAILS

Step	Description
1.	Starting Silicon - Sheet* and 3-in.-diam "solar-grade" silicon** equally divided.
2.	Etch and clean.
3.	Ion implant junction side, ^{31}P, $2x10^{15}$ A/cm^2, 10 keV.
4.	Clean.
5.	Furnace anneal (3 step) - 500°C, 2 h; 850°C, 15 min; 500°C, 2 h.
6.	Print aluminum ink on back and dry.
7.	Fire.
8.	Clean.
9.	Print silver pads on back, dry.
10.	Print silver grid on front, dry.
11.	Fire (IR lamp).
12.	Spray-on AR coating, dry.
13.	Electrical test.
14.	Interconnect - reflow solder - radiant heat.
15.	Laminate - double-glass PVB.

*To be determined based on availability of Web silicon or EFG ribbon or the equivalent.
**Monsanto solar grade wafers (p-type).

TABLE 2. SEQUENCE II DETAILS

Step	Description
1	Starting silicon - Sheet* and 3-in.-diam "solar-grade"** equally divided.
2	Etch and clean.
3	Ion implant junction side ^{31}P, $2x10^{15}$ A/cm^2, 10 keV.
4	Clean.
5	Deposit boron glass - back.
6	Furnace anneal, 900°C, 30 min.
7	Strip oxides, clean.
8	Screen print back, silver ink RCA p-type, dry.
9	Screen print front grid, silver ink RCA n-type, dry.
10	Fire, IR lamp.
11	Spray-on AR coating, dry.
12	Electrical test.
13	Interconnect - reflow solder, radiant heat.
14	Laminate - double-glass PVB.

*To be determined based upon availability of Web silicon or EFG ribbon or the equivalent.
**Monsanto solar grade p-type wafers.

TABLE 3. SEQUENCE III DETAILS

Step	Description
1	Starting silicon - 3-in.-diam n-type "solar-grade"* wafers.
2	Inspect and clean.
3	$POCl_3$ diffusion gettering - 900°C, 30 min.
4	Etch and clean.
5	Ion implant: junction side - ^{11}B, $2x10^{15}$ A/cm^2, 10 keV. back - ^{31}P, $4x10^{15}$ A/cm^2, 30 keV.
6	Clean.
7	Furnace anneal 900°C, 30 min.
8	Clean.
9	Screen print back, silver, dry.
10	Screen print grid, silver, dry.
11	IR lamp fire.
12	Spray-on AR coating.
13	Electrical test.
14	Interconnect, reflow solder, radiant heat.
15	Laminate, double glass PVB.

*Monsanto solar grade, n-type, 1/2 to 2 Ω-cm, saw cut.

TABLE 4. FABRICATION PLANS

	SEQUENCE				
	I		II		III
	Sheet*	Wafer	Sheet*	Wafer	Wafer
Silicon	4x11.4 cm	3 in. Diam	4x11.4 cm	3 in. Diam	3 in. Diam, n-type
0.36x1.2-m panel	3 panels	3 panels	3 panels	3 panels	2 panels
cells/panel	80	60	80	60	60
1.2x1.2-m panel	1 panel	1 panel	1 panel	1 panel	2 panels
cells/panel	280	225	280	225	225
cells/category	520	405	520	405	
cells/sequence	925		925		570
Total cells	2420				

*Size and quantity of cells are subject to change based upon availability and delivery of sheet material.

TABLE 5. COST ANALYSIS - SEQUENCE I

COST ANALYSIS:SEQUENCE I:3" WAFER;14% CELL;30MW;AG FRONT;AL+AG BACK. 06/14/79 10:09:41 PAGE 1

PROCESS COST OVERVIEW-$/WATT

ASSUMPTIONS: 0.669 WATTS PER SOLAR CELL AND 7.8 CM (3") DIAMETER WAFER
CELL THICKNESS: 10.0 MILS. CELL ETCH LOSS: 3.0 MILS. CELL KERF LOSS:10.0 MILS.

STEP	YIELD	PROCESS		MAT'L.	D. L.	EXP.	P. OH.	INT.	DEPR.	SUBTOT	SALVG.	TOTALS	%	INVEST	%
1	95.0%	SODIUM HYDROXIDE ETCH:3 MILS	(A)	0.0	0.052	0.001	0.007	0.001	0.001	0.062	0.0	0.062	7.3	0.006	0.6
2	99.5%	MEGASONIC CLEANING	(B)	0.0	0.006	0.003	0.002	0.001	0.001	0.011	0.0	0.011	1.3	0.005	0.6
3	99.0%	ION IMPLANTATION:P,2.E+15,10 KEV	(B)	0.0	0.058	0.026	0.053	0.084	0.100	0.321	0.0	0.321	37.3	0.700	73.6
4	99.5%	MEGASONIC CLEANING #2	(B)	0.0	0.006	0.003	0.002	0.001	0.001	0.011	0.0	0.011	1.3	0.005	0.6
5	98.0%	4 HR. FURNACE ANNEAL	(B)	0.0	0.010	0.003	0.002	0.003	0.006	0.023	0.0	0.023	2.7	0.021	2.2
6	99.0%	POST DIFFUSION INSPECTION:10%	(B)	0.0	0.000	0.000	0.000	0.001	0.001	0.002	0.0	0.002	0.3	0.005	0.5
7	98.0%	THICK AL METAL:100% BACK & FIRE	(B)	0.041	0.006	0.006	0.007	0.004	0.005	0.068	0.0	0.068	8.0	0.032	3.4
8	99.5%	MEGASONIC CLEANING #3	(B)	0.0	0.006	0.002	0.002	0.001	0.001	0.011	0.0	0.011	1.3	0.005	0.6
9	98.0%	THICK AG METAL:2% BACK PAD & DRY	(B)	0.005	0.006	0.005	0.007	0.003	0.003	0.029	0.0	0.029	3.4	0.023	2.5
10	98.0%	THICK AG METAL:9% FRONT & FIRE	(B)	0.023	0.006	0.007	0.008	0.004	0.005	0.053	0.0	0.053	6.1	0.034	3.6
11	99.0%	HF DIP	(B)	0.0	0.002	0.001	0.000	0.000	0.000	0.004	0.0	0.004	0.4	0.003	0.3
12	99.0%	AR COATING:SPRAY-ON	(B)	0.001	0.006	0.000	0.003	0.001	0.002	0.013	0.0	0.013	1.5	0.012	1.3
13	90.0%	TEST	(B)	0.0	0.005	0.000	0.004	0.005	0.006	0.020	0.0	0.020	2.3	0.041	4.3
14	98.0%	REFLOW SOLDER INTERCONNECT	(B)	0.002	0.011	0.0	0.004	0.004	0.004	0.025	0.0	0.025	2.9	0.029	3.1
15	99.5%	GLASS/PVB/CELL ARRAY ASSEMBLY	(B)	0.156	0.028	0.0	0.005	0.003	0.004	0.196	0.0	0.196	22.8	0.027	2.8
16	100.0%	ARRAY MODULE PACKAGING	(A)	0.007	0.002	0.0	0.000	0.000	0.000	0.010	0.0	0.010	1.1	0.001	0.1
	72.8%	TOTALS		0.236	0.207	0.056	0.109	0.114	0.139	0.860	0.0	0.860	100.0	0.951	100.0
			%	27.47	24.06	6.48	12.62	13.27	16.10	100.00					

FACTORY FIRST COST,$/WATT: 0.18 DEPRECIATION,$/WATT: 0.01 INTEREST,$/WATT: 0.02
LAND COST,$/WATT: 0.0 INTEREST,$/WATT: 0.0

NOTE: (A)=EXISTING TECHNOLOGY; (B)=NEAR FUTURE; (C)=FUTURE ANNUAL PRODUCTION: 30.0 MEGAWATTS.
345 DAYS OF FACTORY PRODUCTION PER YEAR. 8.00 HOURS PER SHIFT. NO. OF SHIFTS PER DAY VARIES BY PROCESS STEP
EQUIPMENT NOT SHARED. FULL ALLOCATION TO PROCESS.

TABLE 6. COST ANALYSIS - SEQUENCE II

COST ANALYSIS:SEQUENCE II:3" WAFER;14% CELL;30MW;AG FRONT;AG BACK. 06/14/79 10:09:41 PAGE 1

PROCESS COST OVERVIEW-$/WATT

ASSUMPTIONS: 0.669 WATTS PER SOLAR CELL AND 7.8 CM (3") DIAMETER WAFER
CELL THICKNESS: 10.0 MILS. CELL ETCH LOSS: 3.0 MILS. CELL KERF LOSS:10.0 MILS.

STEP	YIELD	PROCESS		MAT'L.	D. L.	EXP.	P. OH.	INT.	DEPR.	SUBTOT	SALVG.	TOTALS	%	INVEST	%
1	95.0%	SODIUM HYDROXIDE ETCH:3 MILS	(A)	0.0	0.052	0.001	0.007	0.001	0.001	0.062	0.0	0.062	6.8	0.006	0.7
2	99.5%	MEGASONIC CLEANING	(B)	0.0	0.006	0.003	0.002	0.001	0.001	0.011	0.0	0.011	1.2	0.005	0.6
3	99.0%	ION IMPLANTATION:P,2.E+15,10 KEV	(B)	0.0	0.058	0.026	0.053	0.084	0.100	0.321	0.0	0.321	34.8	0.700	76.0
4	99.5%	MEGASONIC CLEANING #2	(B)	0.0	0.006	0.003	0.002	0.001	0.001	0.011	0.0	0.011	1.2	0.005	0.6
5	98.0%	BORON DEPOSITION	(B)	0.0	0.020	0.069	0.004	0.001	0.001	0.095	0.0	0.095	10.3	0.010	1.1
6	98.0%	900C. DEG. DIFFUSION:1/2 HR.	(B)	0.0	0.010	0.003	0.002	0.001	0.003	0.019	0.0	0.019	2.1	0.012	1.3
7	99.0%	GLASS REMOVAL	(B)	0.0	0.002	0.001	0.001	0.001	0.001	0.005	0.0	0.005	0.5	0.005	0.6
8	99.0%	POST DIFFUSION INSPECTION:10%	(B)	0.0	0.000	0.000	0.000	0.001	0.001	0.002	0.0	0.002	0.2	0.005	0.5
9	98.0%	THICK AG METAL:33% BACK & DRY	(B)	0.049	0.006	0.005	0.007	0.003	0.003	0.074	0.0	0.074	8.0	0.024	2.6
10	98.0%	THICK AG METAL:9% FRONT & FIRE	(B)	0.023	0.006	0.007	0.008	0.004	0.005	0.053	0.0	0.053	5.7	0.035	3.8
11	99.0%	HF DIP	(B)	0.0	0.002	0.001	0.000	0.000	0.000	0.004	0.0	0.004	0.4	0.003	0.3
12	99.0%	AR COATING:SPRAY-ON	(B)	0.001	0.006	0.000	0.003	0.001	0.002	0.013	0.0	0.013	1.4	0.012	1.3
13	90.0%	TEST	(B)	0.0	0.005	0.000	0.004	0.005	0.006	0.020	0.0	0.020	2.2	0.041	4.4
14	98.0%	REFLOW SOLDER INTERCONNECT	(B)	0.002	0.011	0.0	0.004	0.004	0.004	0.025	0.0	0.025	2.8	0.029	3.2
15	99.5%	GLASS/PVB/CELL ARRAY ASSEMBLY	(B)	0.156	0.028	0.0	0.005	0.003	0.004	0.196	0.0	0.196	21.3	0.027	2.9
16	100.0%	ARRAY MODULE PACKAGING	(A)	0.007	0.002	0.0	0.000	0.000	0.000	0.010	0.0	0.010	1.0	0.001	0.1
	72.4%	TOTALS		0.239	0.218	0.118	0.104	0.110	0.132	0.921	0.0	0.921	100.0	0.921	100.0
			%	25.96	23.64	12.78	11.28	11.99	14.33	100.00					

FACTORY FIRST COST,$/WATT: 0.16 DEPRECIATION,$/WATT: 0.01 INTEREST,$/WATT: 0.02
LAND COST,$/WATT: 0.0 INTEREST,$/WATT: 0.0

NOTE: (A)=EXISTING TECHNOLOGY; (B)=NEAR FUTURE; (C)=FUTURE ANNUAL PRODUCTION: 30.0 MEGAWATTS.
345 DAYS OF FACTORY PRODUCTION PER YEAR. 8.00 HOURS PER SHIFT. NO. OF SHIFTS PER DAY VARIES BY PROCESS STEP
EQUIPMENT NOT SHARED. FULL ALLOCATION TO PROCESS.

TABLE 7. COST ANALYSIS - SEQUENCE III

COST ANALYSIS:SEQUENCE III:3" WAFER:16% CELL:30MW:AG FRONT:AG BACK. 06/14/79 10:09:41 PAGE 1

PROCESS COST OVERVIEW-$/WATT

ASSUMPTIONS: 0.764 WATTS PER SOLAR CELL AND 7.8 CM (3") DIAMETER WAFER
CELL THICKNESS: 10.0 MILS. CELL ETCH LOSS: 3.0 MILS. CELL KERF LOSS:10.0 MILS.

STEP	YIELD	PROCESS		MAT'L.	D. L.	EXP.	P. OH.	INT.	DEPR.	SUBTOT	SALVG.	TOTALS	%	INVEST	%
1	99.5%	MEGASONIC CLEANING	(B)	0.0	0.006	0.002	0.002	0.001	0.001	0.011	0.0	0.011	1.1	0.005	0.4
2	99.0%	POCL3 DEPOSITION AND DIFFUSION	(B)	0.0	0.003	0.012	0.003	0.002	0.004	0.024	0.0	0.024	2.3	0.019	1.3
3	95.0%	SODIUM HYDROXIDE ETCH:3 MILS	(A)	0.0	0.044	0.001	0.006	0.001	0.001	0.053	0.0	0.053	5.0	0.005	0.4
4	99.5%	MEGASONIC CLEANING #2	(B)	0.0	0.006	0.002	0.002	0.001	0.001	0.011	0.0	0.011	1.1	0.005	0.4
5	99.0%	ION IMPLANTATION:B,2.E+15,10 KEV	(B)	0.0	0.050	0.022	0.046	0.072	0.086	0.275	0.0	0.275	26.3	0.600	42.3
6	99.0%	ION IMPLANTATION:P,2.E+15,30 KEV	(B)	0.0	0.050	0.022	0.046	0.072	0.086	0.275	0.0	0.275	26.3	0.600	42.3
7	99.5%	MEGASONIC CLEANING #3	(B)	0.0	0.006	0.002	0.002	0.001	0.001	0.011	0.0	0.011	1.1	0.005	0.4
8	98.0%	900C. DE6. DIFFUSION:1/2 HR.	(B)	0.0	0.010	0.003	0.002	0.001	0.003	0.019	0.0	0.019	1.8	0.012	0.9
9	99.5%	MEGASONIC CLEANING #4	(B)	0.0	0.006	0.002	0.002	0.001	0.001	0.011	0.0	0.011	1.1	0.005	0.4
10	99.0%	POST DIFFUSION INSPECTION:10%	(B)	0.0	0.000	0.000	0.000	0.001	0.001	0.002	0.0	0.002	0.2	0.005	0.4
11	98.0%	THICK AG METAL:33% BACK & DRY	(B)	0.043	0.005	0.004	0.006	0.002	0.003	0.064	0.0	0.064	6.1	0.020	1.4
12	98.0%	THICK AG METAL:9% FRONT & FIRE	(B)	0.020	0.005	0.006	0.006	0.004	0.004	0.045	0.0	0.045	4.3	0.029	2.1
13	99.0%	HF DIP	(B)	0.0	0.002	0.001	0.000	0.000	0.000	0.004	0.0	0.004	0.3	0.003	0.2
14	99.0%	AR COATING:SPRAY-ON	(B)	0.001	0.006	0.000	0.003	0.001	0.002	0.013	0.0	0.013	1.3	0.012	0.9
15	90.0%	TEST	(B)	0.0	0.004	0.000	0.003	0.004	0.005	0.017	0.0	0.017	1.6	0.035	2.5
16	98.0%	REFLOW SOLDER INTERCONNECT	(B)	0.002	0.011	0.0	0.004	0.003	0.004	0.024	0.0	0.024	2.3	0.028	2.0
17	99.5%	GLASS/PVB/CELL ARRAY ASSEMBLY	(B)	0.137	0.028	0.0	0.005	0.003	0.004	0.176	0.0	0.176	16.9	0.027	1.9
18	100.0%	ARRAY MODULE PACKAGING	(A)	0.006	0.002	0.0	0.000	0.000	0.000	0.009	0.0	0.009	0.8	0.001	0.1
	72.4%	TOTALS		0.209	0.240	0.081	0.140	0.170	0.204	1.044	0.0	1.044	100.0	1.417	100.0
			%	20.05	22.97	7.71	13.40	16.29	19.58	100.00					

FACTORY FIRST COST,$/WATT: 0.20 DEPRECIATION,$/WATT: 0.01 INTEREST,$/WATT: 0.02
LAND COST,$/WATT: 0.0 INTEREST,$/WATT: 0.0

NOTE: (A)=EXISTING TECHNOLOGY; (B)=NEAR FUTURE; (C)=FUTURE ANNUAL PRODUCTION: 30.0 MEGAWATTS.
345 DAYS OF FACTORY PRODUCTION PER YEAR. 8.00 HOURS PER SHIFT. NO. OF SHIFTS PER DAY VARIES BY PROCESS STEP
EQUIPMENT NOT SHARED. FULL ALLOCATION TO PROCESS.

interaction of processing steps with the selection of starting silicon materials, could reduce or eliminate the cost differentials calculated.

B. TECHNICAL DISCUSSION OF MANUFACTURING SEQUENCES

Sequence I is devoted to the production of $n^+/p/p^+$ solar cells using both sheet silicon and "solar-grade" 3-in.-diameter wafers. The major difference between sequences I and II is the back-side doping and contacting process. In sequence I, an aluminum paste screened onto the back and fired-in is used to form both a p^+ back-surface field (BSF) and a conductive surface. However, since in our manufacturing sequence reflow soldering is to be used in the interconnection of cells, silver pads must be subsequently screened onto the back and fired separately.

The application and firing of aluminum into the back of wafers and sheet silicon is a complex process involving many variables. This process has not been previously qualified at RCA, and, consequently, we have formulated a number of technical questions to be evaluated experimentally. A discussion of these questions along with a description of our initial experiments is given in subsection IV.D below

Sequence II is also designed to manufacture $n^+/p/p^+$ solar cells but represents a different approach to the application of the p^+ back surface. In the work conducted at RCA [2], it has been shown that the application of a boron-glass followed by furnace annealing results in both a p^+ back-surface field and an effective gettering, yielding a long diffusion length in the bulk silicon. The p^+ doping allows for the application of silver ink to the back with reduced contact problems. This method should have particular advantage when applied to low-cost silicon materials which are expected to contain lifetime killing impurities, since the boron-glass acts as a getter during furnace annealing.

In sequence III, n-type silicon will be used in the production of $p^+/n/n^+$ cells because it has been observed at RCA [3] and elsewhere [4] that high efficiency (16%) cells are more readily achieved with $p^+/n/n^+$ solar cells than with cells of the $n^+/p/p^+$ variety. In addition, n-type silicon appears to be more tolerant to the presence of some undesireable impurities than p-type silicon.

SECTION IV

PROGRESS

A. PLANNED PROCESS FLOW

Solar-cell processing did not begin until the latter part of this quarter because of a delay in the delivery of "solar-grade" wafers from Monsanto. Also, although purchase agreements have been made with Mobil-Tyco and Westinghouse for EFG ribbon and web silicon, delivery of these items has not been made on schedule and is not expected until after this quarter. Because of this, work during the period was restricted to the following:

(1) Grid and diagnostic pattern mask design for screen printing and photomasks.

(2) Equipment setup and testing of production-type screen-printer and spray-on autocoater.

(3) Initial qualification testing for an aluminum p^+ back-contact process following process specifications supplied by JPL.

(4) Refinement of the double-glass panel lamination process.

(5) Design and construction of an automatic calculator-controlled, illuminated electrical test system for high-speed testing of completed solar cells.

B. GRID MASK AND DIAGNOSTIC PATTERN DESIGNS

Because of improvements which we have made in screen-printing and contact-firing techniques, a new grid mask with reduced area coverage was designed. This pattern is shown in Fig. 3. The fine-grid fingers are 0.005 in. wide on 0.100 in. centers. A three-section tapered bus-bar arrangement is used to essentially halve the distance over which the fine-grid fingers must extend before they reach a bus, thus reducing the risk of open lines. The total fractional area coverage (shadowing) for this pattern is 9% compared with 14% in our previous design.

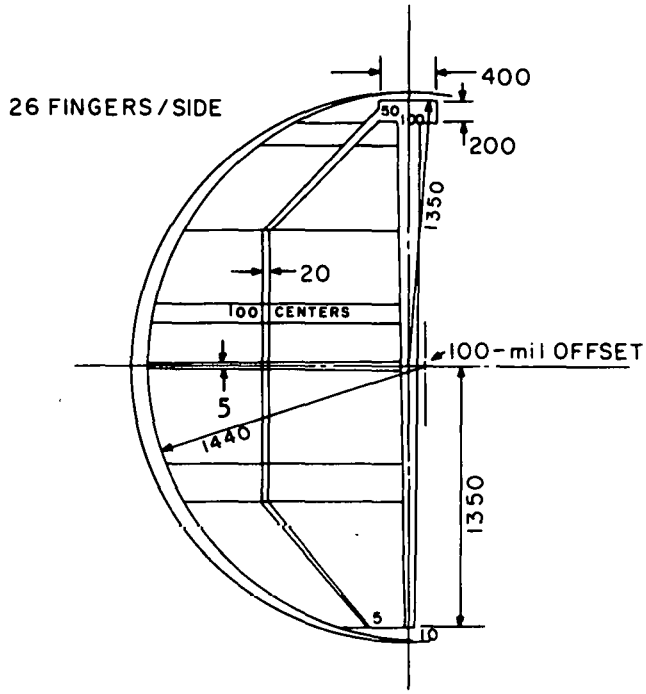


Figure 3. Grid mask.

For purposes of control tests and to obtain measurements of critical printed-contact parameters, a diagnostic mask was designed. The layout of this pattern is shown in Fig. 4 with letter keys designating the specific test elements. The patterns were intentionally repeated and spread over the 3-in. area to test for aerial uniformity. The test elements and their specific functions are:

A. Serpentine for the measurement of metal sheet resistance. The serpentine is 6300 mil long by 10 mil wide, resulting in 630 squares.

B. These lines are for testing the ability to print fine lines over a length of 1-½ in. The thickest line is 20 mil wide, and the finest line in this group is 3 mil wide, a value which is below our present printing capability.

C. These pads are for testing solderability, adhesion, and bond-strength.

D. Three bull's-eye patterns. Each pattern can be used to measure the metal-to-silicon contact resistance. The bull's-eye pattern may be used in several different ways to obtain the contact resistance of a chosen annulus. One straightforward method which is based on a lumped resistance model is illustrated in Fig. 5. The sensitivity of this measurement is related to the ratio R_c/R_s. To obtain a reasonably large value for this ratio, the distance between

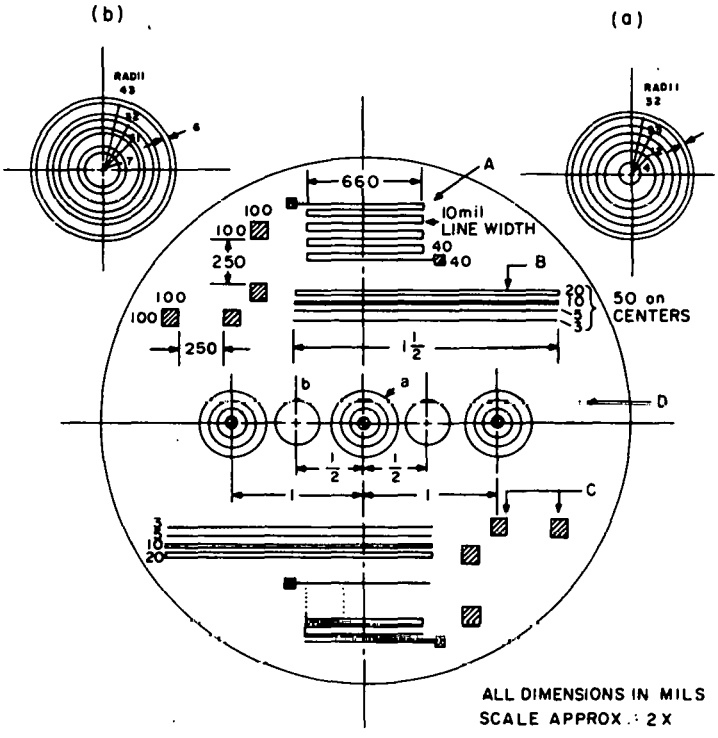


Figure 4. Diagnostic mask pattern.

annuli and the contact area should be kept small. For screen-printed patterns where line resolution is limited to about 5 mil and for typical surface-layer sheet resistances of ~50 Ω/□, the sensitivity of this pattern is limited to accurate measurement of specific contact resistivity greater than 10^{-3} Ω-cm^2. This value is low enough to ensure a negligible contribution to the total series resistance.

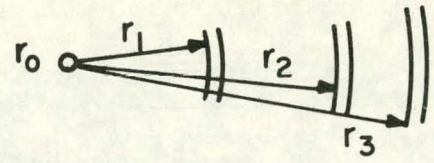
C. EQUIPMENT SETUP AND TESTING

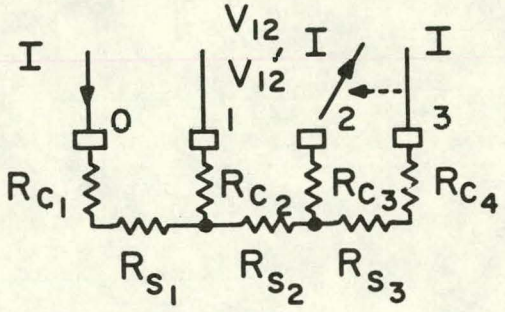
1. Model CP885 Thick-Film Screen Printer*

A model CP-885 production thick-film screen printer was received and setup during mid March. This machine has the capability of accepting screens up to 12x12 in. A photograph of this printer with optional collocator is shown in Fig. 6. The collocator is a belt synchronized to the printing rate which moves the wafers from the print-head to a desired location (e.g., dryer-belt). A list of the options purchased is given below:

- 51B 24-in. collocator.
- Squcegee speed readout clock.
- Printed parts counter.

*Manufactured by AMI-PRESCO, North Branch, NJ.





$$\frac{V_{12}}{I} = R_{s_2} = \frac{R_{\square}}{2\pi} \ln\left(\frac{r_2}{r_1}\right) \text{ (current probes on pads 0 and 3)}$$

$$\frac{V_{12}'}{I} = R_{s_2} + R_{c_3} \quad \text{(current probes on pads 0 and 2)}$$

where $R_{c_3} = \frac{\rho_c}{A_3}$

ρ_c = Specific contact resistivity (Ω-cm^2)

A = Area of metal contact to silicon

Figure 5. Resistance model.

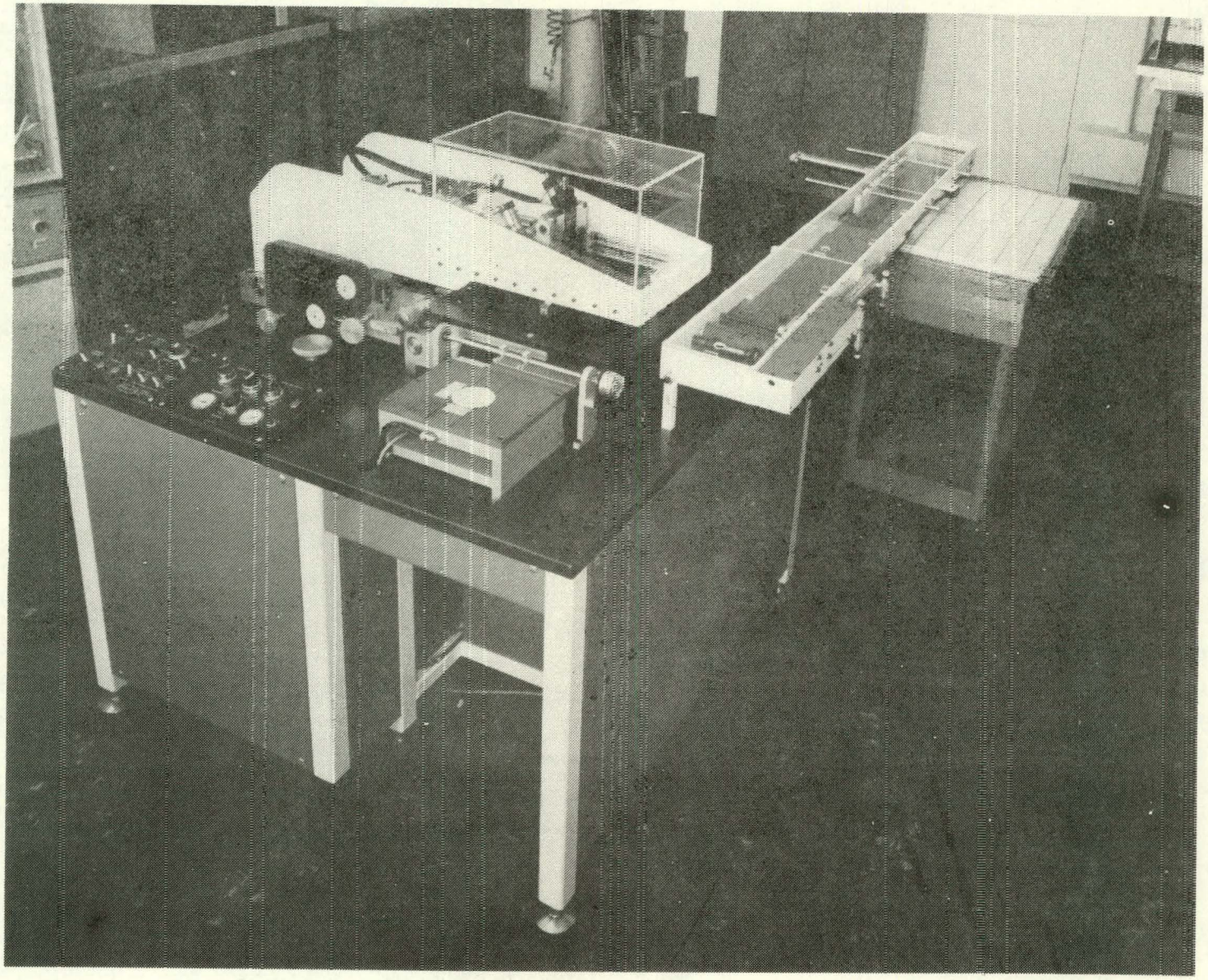


Figure 6. Thick-film screen printer with collocator.

- Plexiglass print head cover.
- Double print pass.
- High pressure hydraulic pump squeegee drive (enables higher squeegee speeds, easier setup, and lower long-term maintenance than the standard air-over-oil system).
- 4 CFM vacuum pump installed in console with motor starter.
- Camber sensor fail-safe (prevents printing overly-cambered substrates. Provides screen protection in that squeegee will not cycle unless a substrate is present).
- "SOS" sensor fail-safe ("stuck-on-screen"; automatically shuts down machine in the event of substrate sticking to screen).
- Extra screen frame mounting plate assemblies (specify screen frame size).
- SEG-1 screen emulsion thickness gauge.
- STG-5 screen tension gauge.

Functional machine checkout included printing the desired front-grid pattern on 3-in.-diameter silicon wafers 0.010 in. thick. Examination of the printed pattern revealed good line definition: the minimum designed linewidth (0.005 in.) printed at an average width of 5½ mil (see Fig. 7). All mechanical functions and adjustments of the machine and accessories performed well.

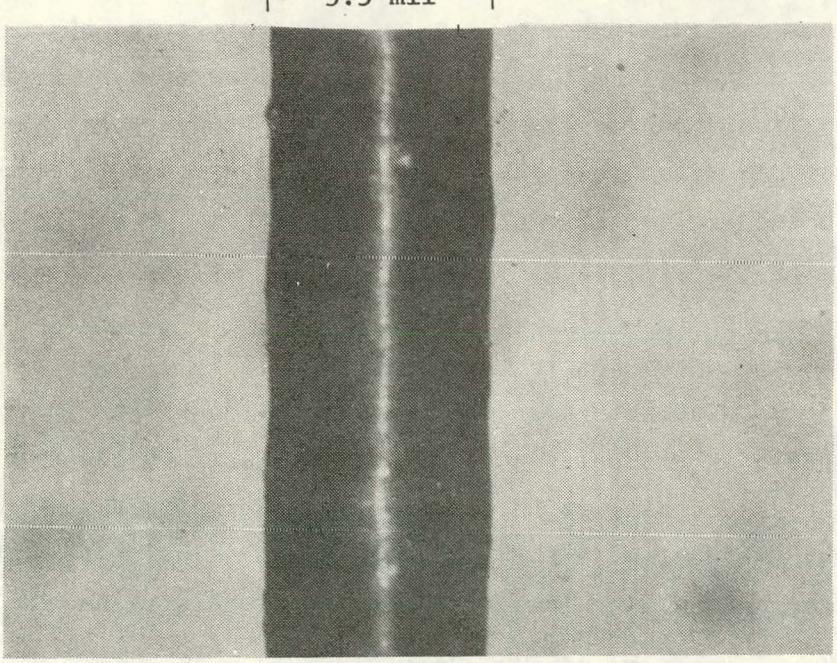


Figure 7. "As-printed" grid line.

2. Model 9000 Zicon Autocoater* (Spray-On AR Process)

a. Installation of a Zicon Series 900 Autocoater at RCA Laboratories

Spray deposition studies in the past were carried out by us at Zicon Corporation on a rental basis of their equipment and facilities. Early in this quarter we purchased and installed in our laboratory a Zicon Series 9000 Autocoater and prepared it for processing large numbers of cells entirely on our own premises. The system was described in the Interim Report [2]. Figures 8, 9, and 10 illustrate the machine, the spray gun assembly, and the gun unit.

In the process of spray testing we found that ambient humidity can be more critical than was previously observed. Excessively high levels of air humidity in the spray booth can affect the quality of the coating, leading to hazy films, probably due to gas phase nucleation in the atomized spray solution. An air conditioning unit is being installed at the inlet of the HEPA filter to lower and control the air humidity to a value not exceeding 45% relative humidity.

b. Comparison of Commercial Spray Equipment Produced by Different Manufacturers

Spray tests were conducted with RCA I TiO_2 AR coating solution at Advanced Design Equipment, Inc. in Bristol, RI, to compare the performance of their spray-coating equipment with that of the Zicon Autocoater. We concluded that the ADE spray machine is similar to the Zicon Autocoater in function except for a few minor differences, including a continuous-substrate drive which results in a sawtooth spray pattern, and the incorporation of an in-line 20-μm Millipore filter in the liquid source reservoir. However, there seems to be no clear advantage over the Zicon equipment. Although we could not optimize machine parameters in the limited time of testing available, we decided that the quality of the resulting AR films is potentially as good as that obtainable with the Zicon machine.

An ultrasonic spray nozzle ("Sonimist") unit is also being considered. This equipment is manufactured by Heat System Ultrasonics, Inc. in Plainview, NY and is capable of producing a fine, evenly dispersed cloud of extremely small droplets. According to this company, a sonic field is created at the gas orifice of the nozzle as the gas reaches the velocity of sound. These sound waves impinge on a hollow cavity at the tip of the nozzle causing resonant

*Zicon Corp., Mount Vernon, NY.

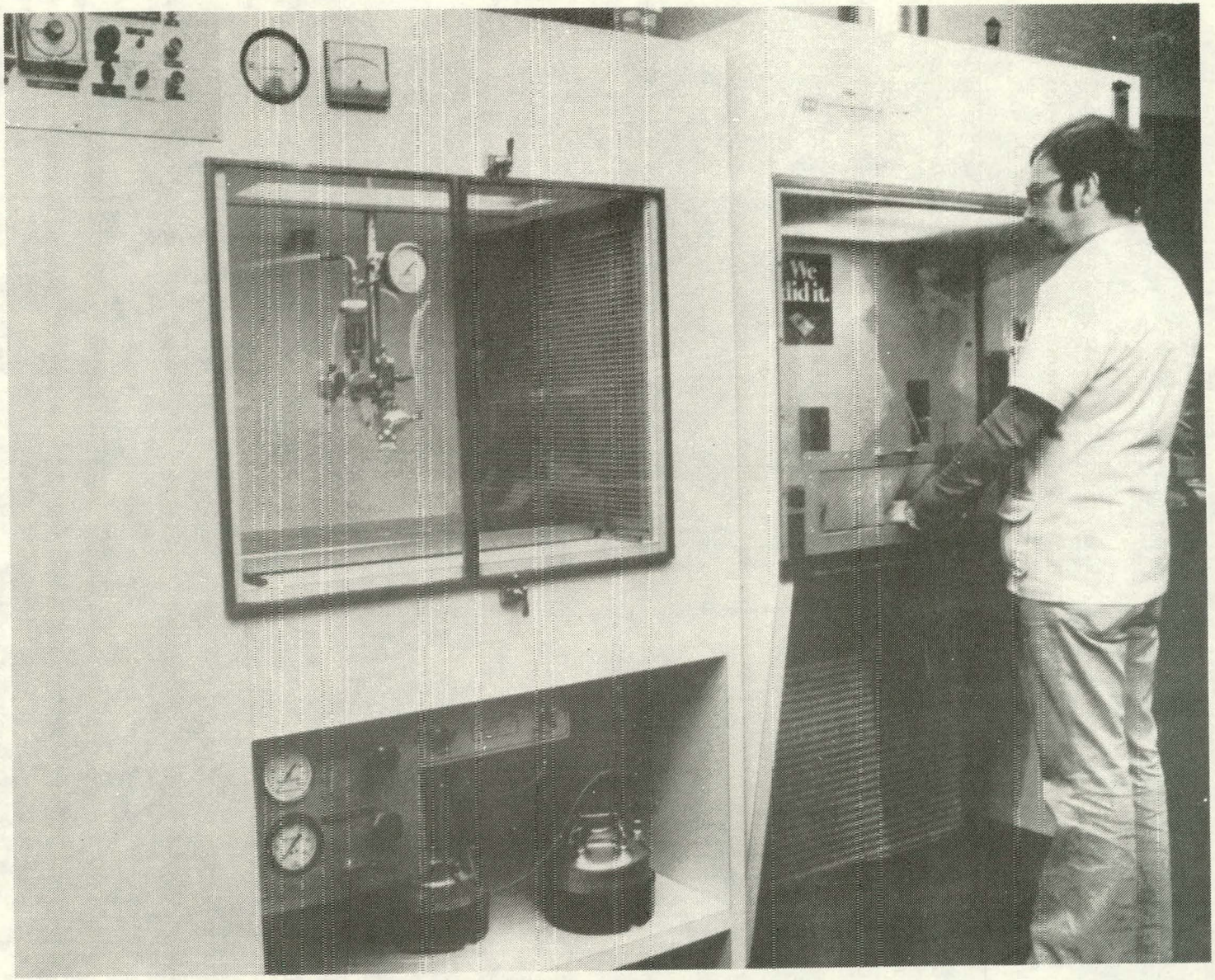


Figure 8. Photograph of Zicon Series 9000 Autocoater.

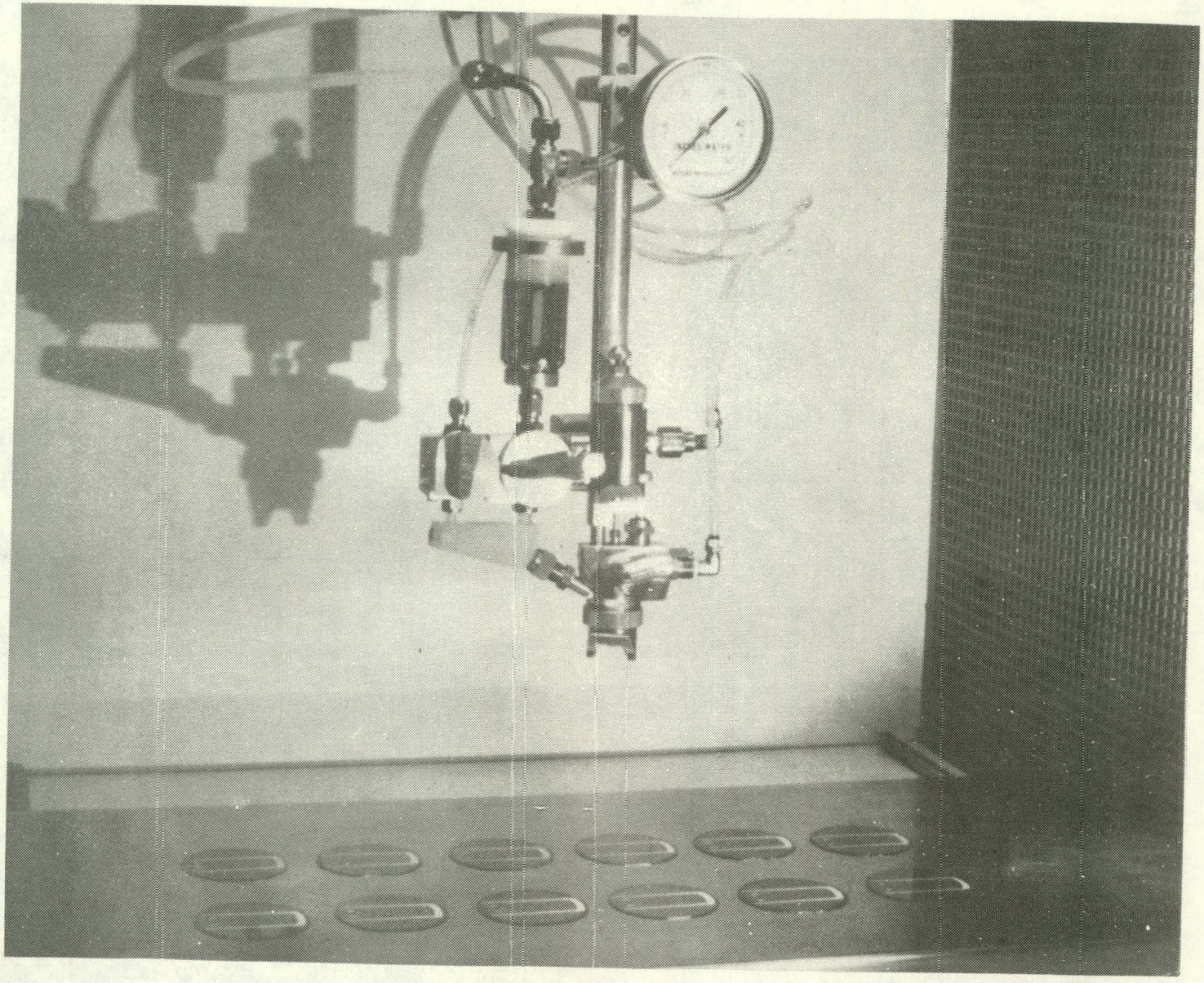


Figure 9. Photograph of spray gun assembly.

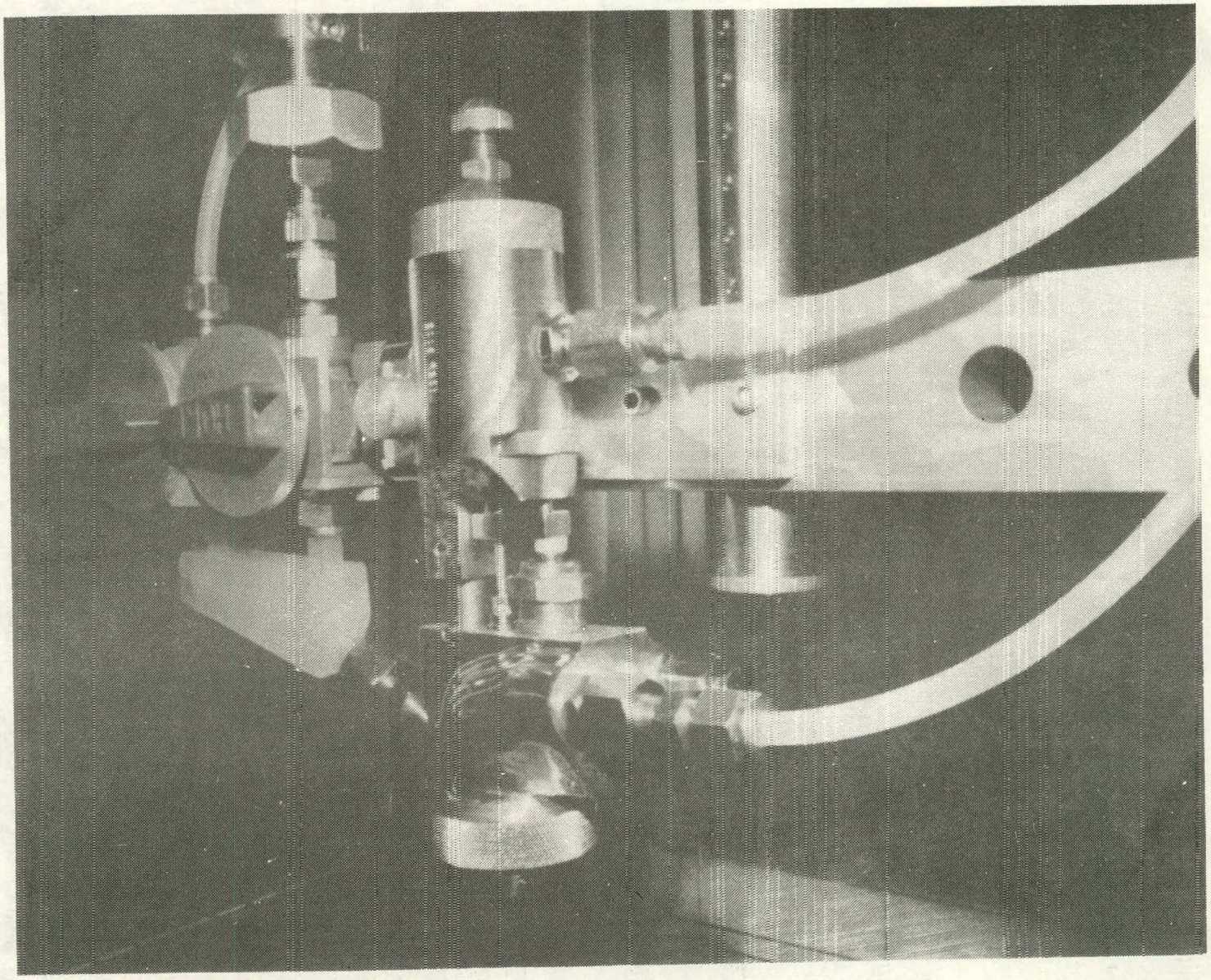


Figure 10. Photograph of the gun unit.

vibrations. Liquid is injected through openings near the resonant cavity and is atomized by the sound waves. The frequency of the radiating waves is determined by the shape on the cavity and its position relative to the nozzle orifice. Droplet size is determined by the frequency and the flow rate and surface tension of the liquid. No actual spray tests with our solutions have been conducted as yet.

c. Updated Cost Analysis

A complete revision of the cost analysis for the RCA I TiO_2 type AR spray coating has been completed. The changes are based on 1978 dollars and reflect the simplifications we introduced due to shortened post-deposition heating cycles and the substantial cost reduction achieved by synthesizing our own source liquid. The direct total cost is 1.08 cents/3-in. wafer, or 1.97 cents/W. A summary of the cost analysis is presented in Table 8.

D. ALUMINUM p^+ BACK CONTACT PROCESS

Sequence I of our manufacturing processes requires the application of an aluminum p^+ BSF contact to the back of the cells. This process was not previously conducted at RCA. A process specification sheet provided by Spectrolab* was obtained from JPL, and we have attempted to verify this process and adapt it into our sequence I processing schedule. The critical step appears to be the "spike" firing of the screened-on aluminum paste. Accordingly, we have experimented with both furnace and infrared-lamp firing of the paste at several temperatures. Initial tests were conducted by screening the paste onto the back of 3-in.-diameter, p-type (1.5 Ω-cm) silicon wafers, drying, and firing in air at temperatures from 675 to 900°C for ∿1 min. In these tests, the aluminum partially oxidizes and leaves an easily removable powder uniformly over the back of the wafer. Initial tests involved removing the powder (HCl + water + agitation) and performing a spreading resistance depth profile measurement to assess penetration and active p^+ doping into the back of the silicon wafers. These measurements show progressively increased doping with increased firing temperature, as shown in Figs. 11, 12, and 13. Little or no doping was measured in samples fired at 675°C, and a somewhat irregular doping profile extending from the back surface ∿10 μm into the silicon with surface concentration of $\sim 10^{17} A/cm^3$ was obtained by firing at 850°C in the furnace and 850°C under the lamp (see Figs. 13 and 14).

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*Spectrolab, Inc., Sylmar, CA.

TABLE 8. SUMMARY OF COST ANALYSIS FOR AR SPRAY-ON COATING

Assumptions

30-MW Annual Production

12% Cell Efficiency (0.548 W/Wafer)

3-in.-Diameter Cell (7-8 cm)

12% Cost of Capital

7-Year Equipment Life

1978 $ Basis

Capital

Zicon Model 11000 Autocoater

$185K

4500 Wafers/Hour Thruput

90% Uptime

Material

AR Coating At $4.15/Liter Spray Liquid

0.1 cm^3/Wafer Needed

Cost Summary

	¢/Wafer	¢/Watt
Material	0.04	0.07
Direct Labor*	0.44	0.80
Direct Expense	0.06	0.10
Indirect Labor*	0.27	0.50
Interest & Depreciation	0.27	0.50
Direct Costs	1.08	1.97

*Includes Employee Service Expense

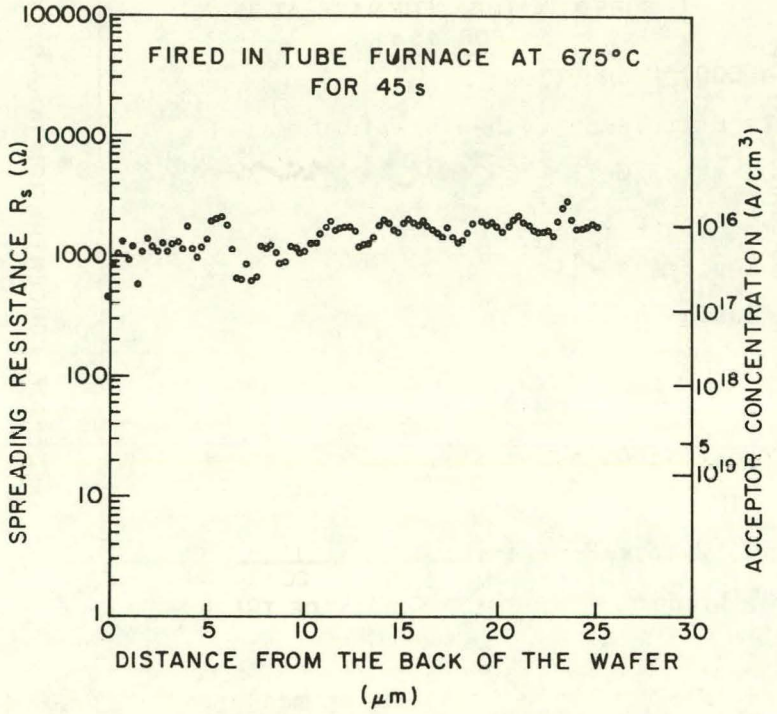


Figure 11. Spreading resistance measurements, fired in tube furnace at 675°C for 45 s.

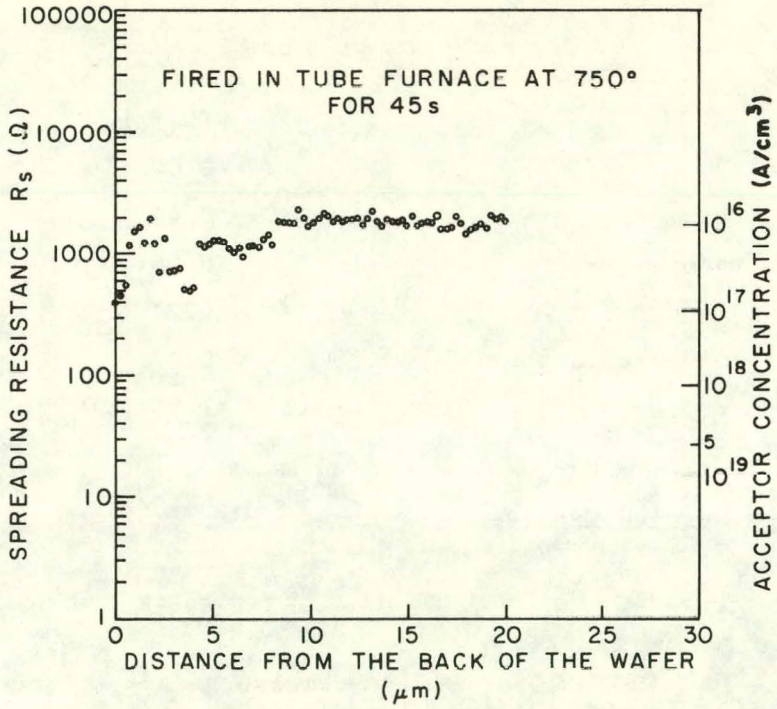


Figure 12. Spreading resistance measurements, fired in tube furnace at 750°C for 45 s.

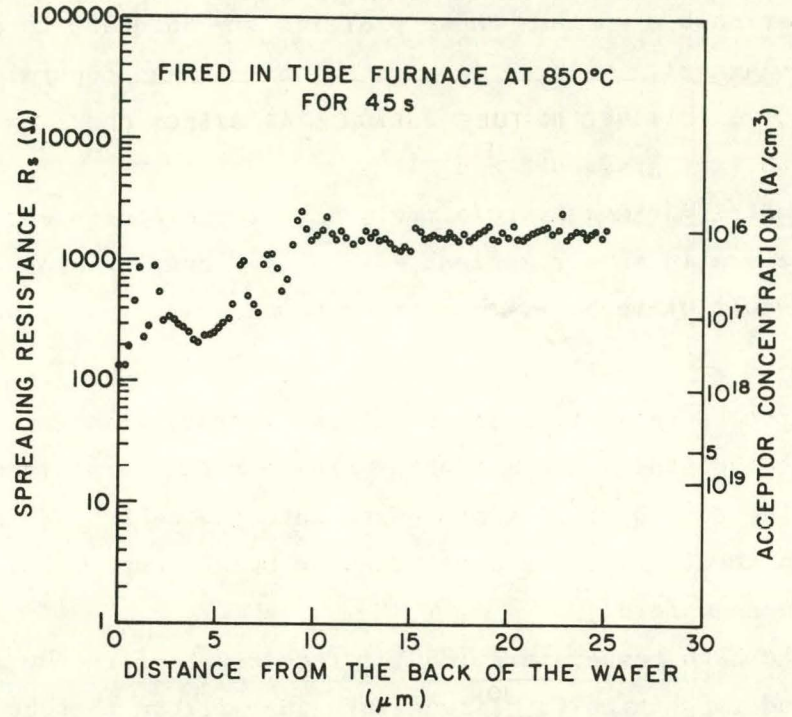


Figure 13. Spreading resistance measurements, fired in tube furnace at 850°C for 45 s.

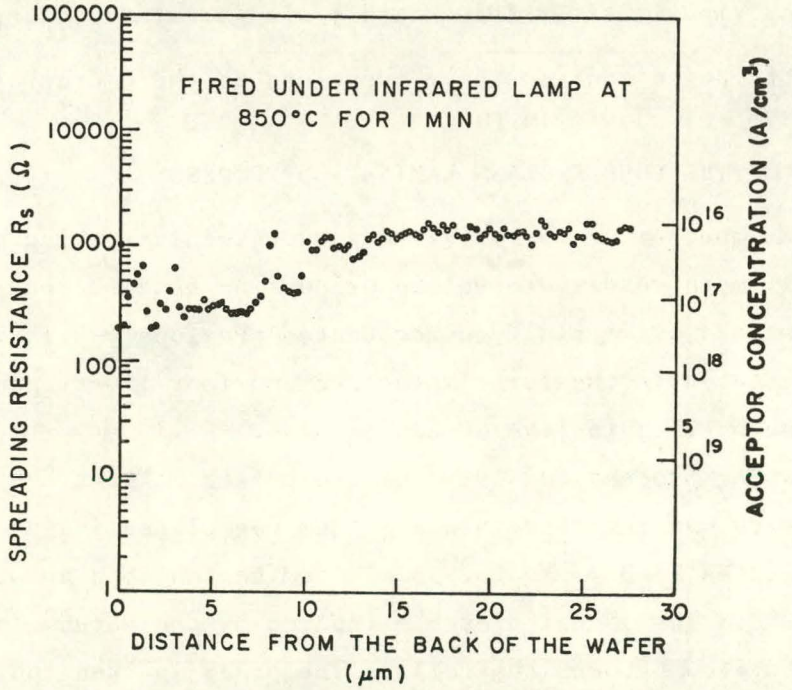


Figure 14. Spreading resistance measurements, fired under infrared lamp at 850°C for 1 min.

It is questionable whether these profiles are adequate to obtain a strong BSF effect. Solar cells will be fabricated on test and control wafers to examine this. Further, we believe that the motion of aluminum under these conditions is controlled by thermal gradients and alloying.

The short firing times at relatively high temperatures and the rapid transition in temperature in an air ambient make this a complex process and we have formulated a number of technical questions to be evaluated in our subsequent work:

- o What process parameters (temperature, thermal gradient, gas ambient) control the doping and motion of aluminum in the silicon?
- o In firing the thick aluminum paste into the back of thin and/or stressed silicon sheet, will the sheet warp or break, especially in the case of large-area wafers?
- o Will the high temperature (850°C) required to fire the aluminum cause unwanted impurities to diffuse into the silicon thereby reducing the bulk diffusion length?
- o In the case of sheet silicon which may be polycrystalline, will aluminum, or other impurities diffuse rapidly along grain boundaries?

We will attempt to address these questions in the course of our work.

E. REFINEMENT OF THE DOUBLE-GLASS LAMINATION PROCESS

During this quarter we investigated a two-step laminating process which will lend itself more readily to volume production than the one-step continuous process which we had successfully demonstrated previously. Three 4-ft-square panels were laminated in the large autoclave and four 1x4-ft panels were laminated in the small autoclave at Saftee-Glass.*

The laminating process consisted of two phases. First the glass/PVB/cell/PVB/glass sandwich was inserted into a vacuum bag placed inside the autoclave. The bag is evacuated to 3 mm Hg for 15 min and heated at a constant external pressure to 150°C. The 15-psi pressure induced by the vacuum is sufficient to cause the PVB to flow between the cells. The panel is then cooled with the vacuum maintained until the temperature of the PVB is below 60°C. The vacuum is then terminated, and the panel is extracted from the vacuum bag and inspected

*Saftee-Glass, a division of Chromalloy, King of Prussia, PA.

for lamination defects. The prelaminated panel is then autoclaved at 150-psig hydrostatic pressure. With the exception of "bubbles" at the perimeter, panel numbers 012979 (Fig. 15), 012478 (Fig. 16), 011879 (Fig. 17), 021079, and 030379 were very good laminations. The majority of these perimeter bubbles are ported to the outside.

Although the exact nature and formation process of these bubbles are unknown at present, there are two potential models for the bubble formation. One is that they originate from air dissolved in the PVB which comes out of solution as the temperature of the PVB is elevated and the pressure is decreased. In the second model the bubbles are of external origin. These bubbles or voids are sucked into the PVB as it volumetrically shrinks during cool-down. Although vacuum is maintained throughout the cool-down sequence, the forces created by the PVB shrinkage could easily exceed the 15-psi force exerted by the vacuum. The occurrence of bubbles is decreased markedly along the panel edges which contain the 0.250-in.-wide x 0.015-in.-thick copper bus-bar. This fact tends to lend more credence to the external origin rather than internal origin bubble model. This fact also reveals a possible solution to the edge bubble problem: the addition of a plastic strip along the two edges of the panel not occupied by the bus-bars.

A small array (11x4) of live cells had been laminated in December 1978 (#120878) and this was bubble-free. The lamination was done in a continuous process. The key process step appears to be the introduction of 15-psig pressure after the PVB had achieved 150°C and prior to terminating the vacuum. This step tends to apply a pressing force on the faces of the panel causing the PVB to flow completely to the edge. This will be investigated during the next quarter.

Panel 022479 was severely broken during autoclaving (Fig. 18). The cause was a combination of insufficient heating during the prelamination stage and failure to securely lash the panel in the autoclave. The panel shown in Fig. 19 (012279) is also broken but not as severely. This too was caused by insufficient heating during the prelamination step.

Development of a two-phase laminating process is critical to the automation of panel fabrication. In our automated-process concept, panels are first prelaminated in vacuum fixtures by conductive heating elements located adjacent to the glass sheet. The panels are then cooled in the vacuum fixture, removed, and then placed in batches in the autoclave for the final high-pressure bond

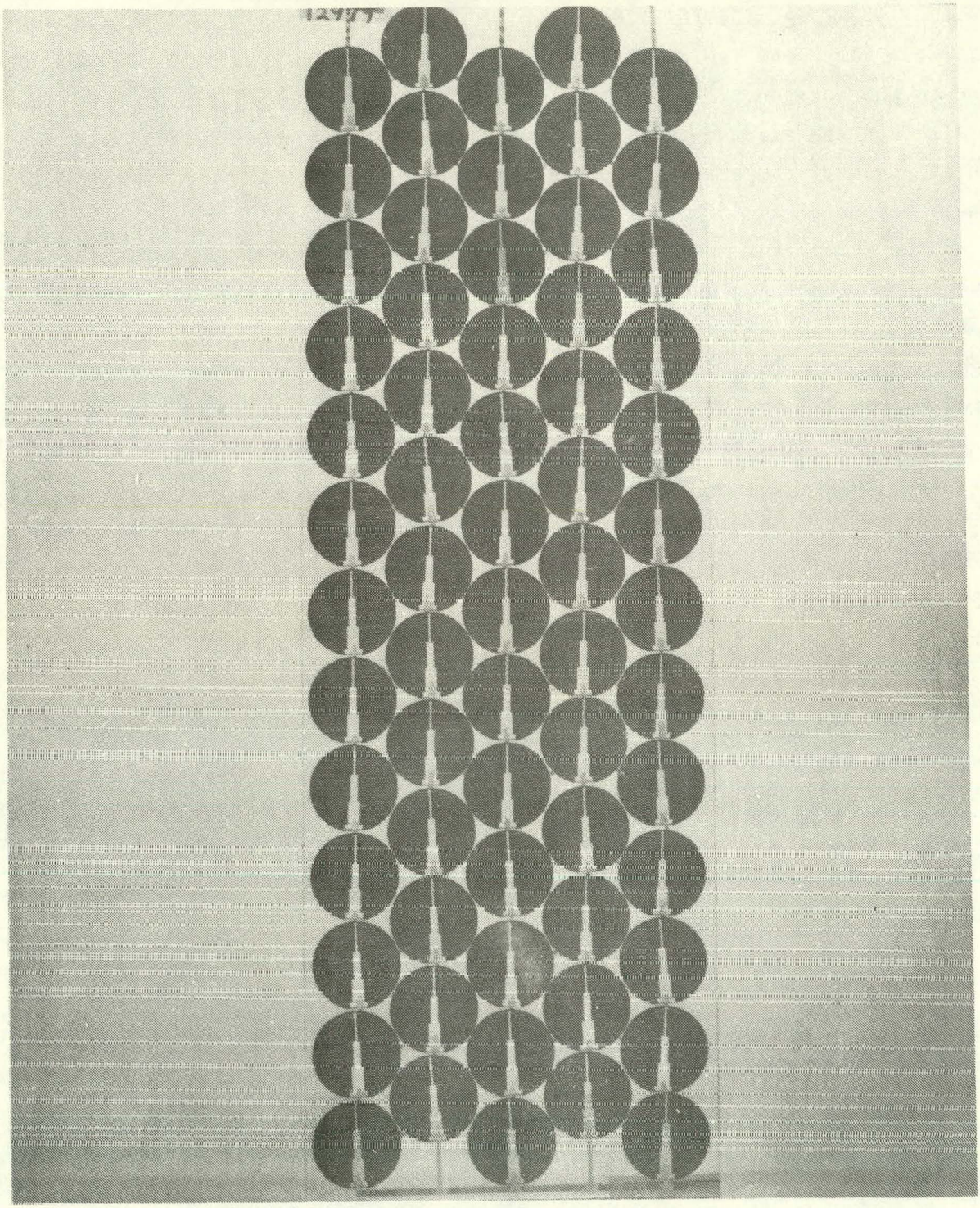


Figure 15. Photograph of panel 012979.

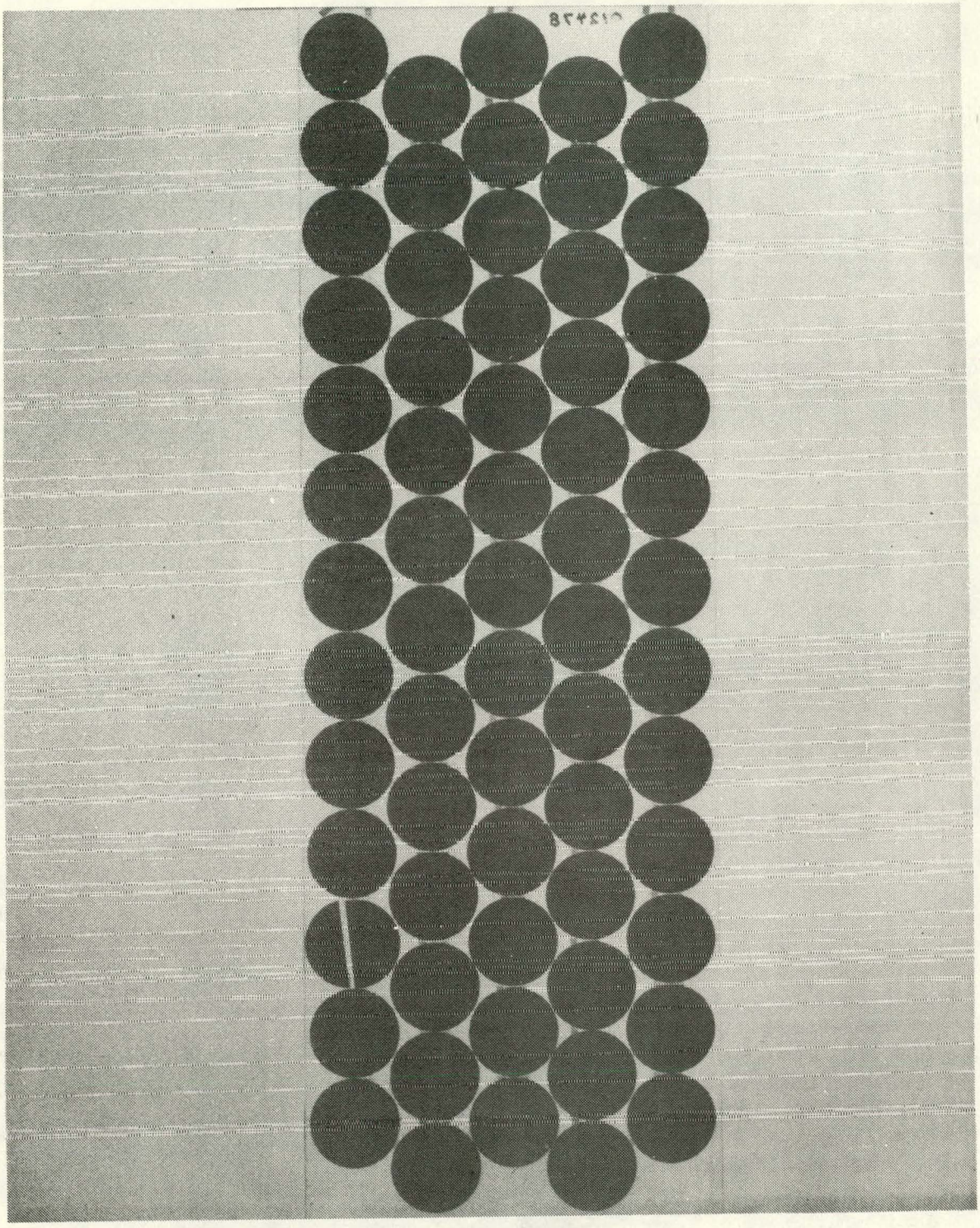


Figure 16. Photograph of panel 012478.

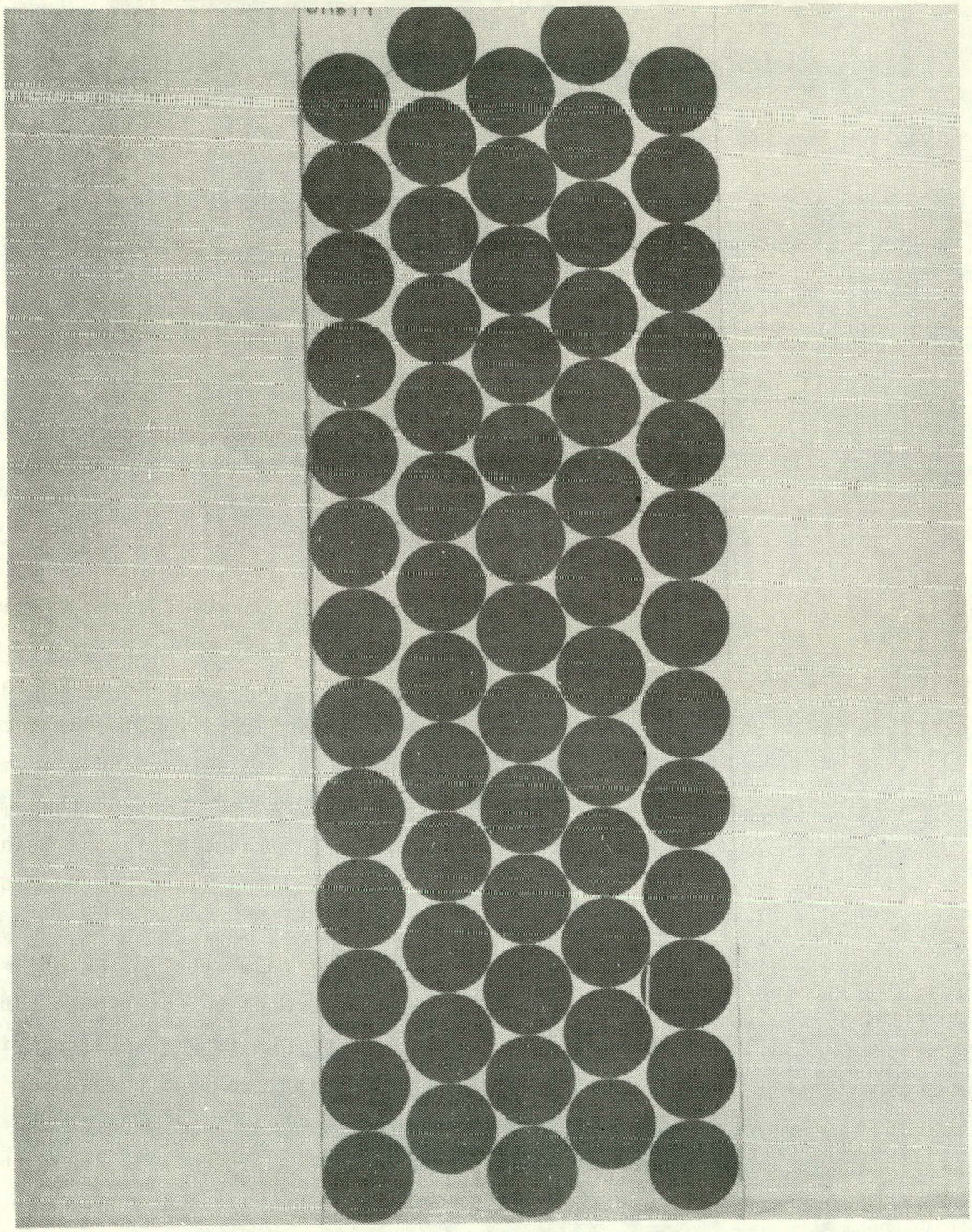


Figure 17. Photograph of panel 011879.

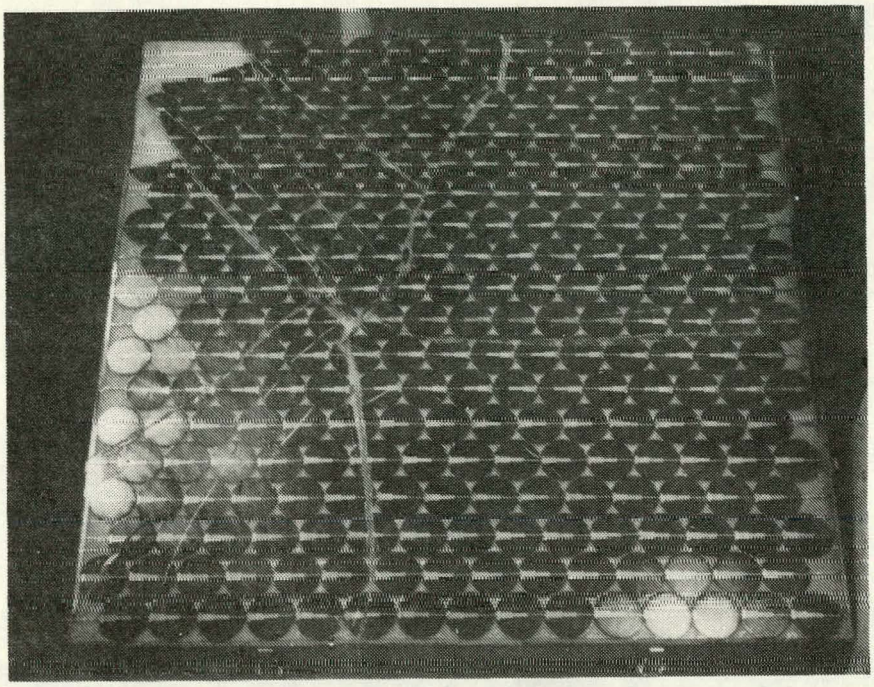


Figure 18. Photograph of panel 022479 broken during autoclaving.

enhancement process known as autoclaving. The heat-up rate for the prelaminated panel in the autoclave is rapid due to the enhanced heat transfer of air pressurized at 10 atmospheres. A single-step process carried out entirely in the autoclave would require that many individual vacuum-bagged panels be placed in the autoclave at once. The panel must be heated at ambient pressure to avoid fracturing the solar cells. This constraint increases the heat-up time markedly. This factor, coupled with the multiple vacuum seals and connections which must be made, renders the single-step lamination process less desirable and more costly for automation.

A lamination trial was conducted on a small 9-cell array using EVA* as the encapsulant. The lamination was conducted as suggested in Springborn Lab's** literature using a vacuum bag inside a cover. The EVA flowed well and filled the voids between the cells. The quality of the laminate was comparable to PVB laminates made in the same equipment. However, the bond strength of the EVA to the glass is apparently inferior to that of the PVB. This is based on the observance of delamination of the EVA as excess was being trimmed from the edge of the panel.

*EVA = ethylene-vinyl acetate.
**Springborn Laboratories, Inc., Enfield, CT.

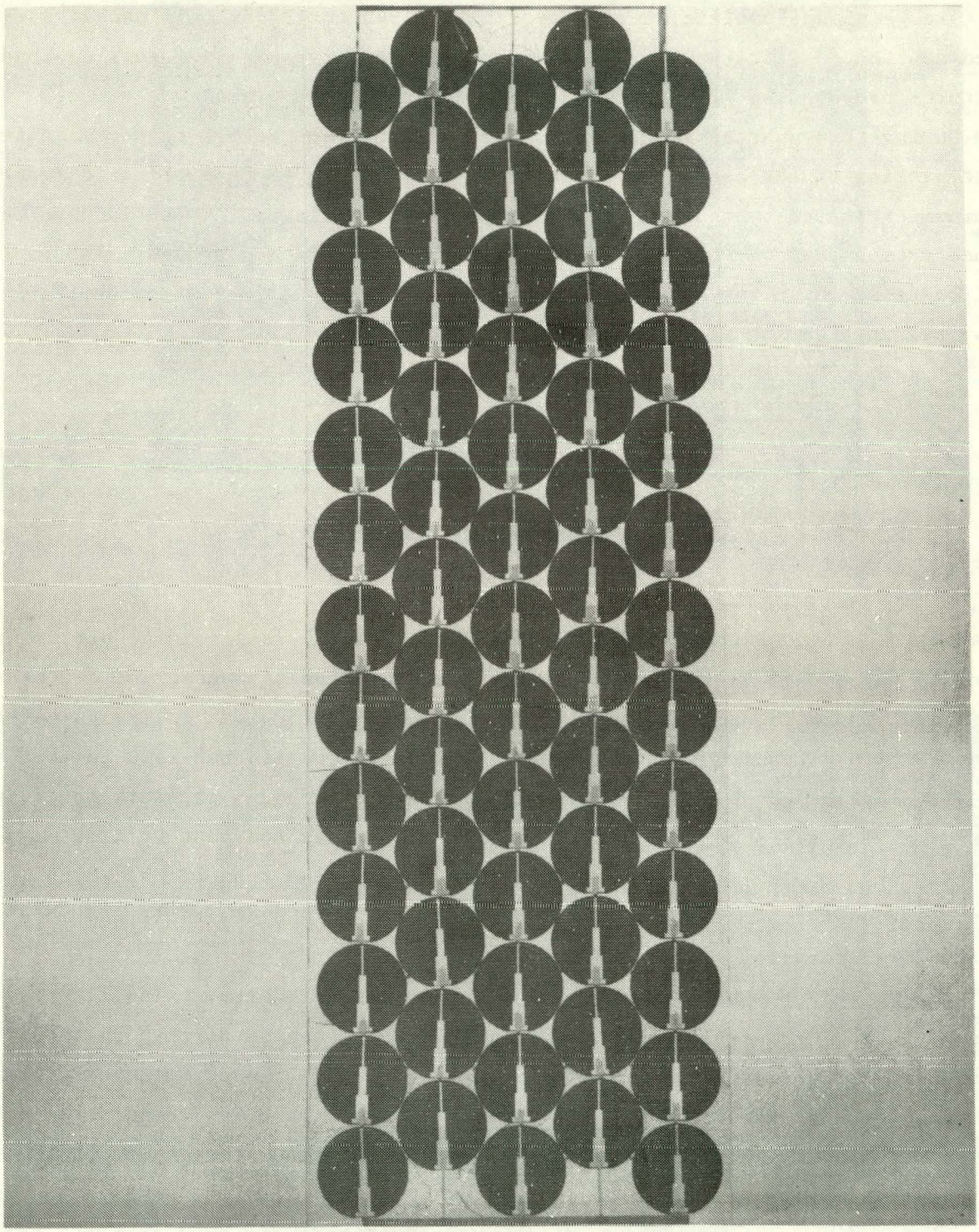


Figure 19. Photograph of panel 012279, broken during autoclaving.

Limited thermal cycling was performed on panels produced during this quarter and the last. Five 1x4-ft panels and two approximate 4-ft-square panels were put through three complete thermal cycles from -40 to +90°C. All panels survived unaffected with the exception of one of the large panels. This one had fractures propagating from a pre-existing defect in the glass.

During this quarter we have also refined the frame design to accommodate tight packing of the panels into arrays. The frame is to be fabricated from aluminum extrusions which have an exterior mounting flange. Channels have been formed from sheets which approximate the eventual extrusion design. The panel will be retained in the frame by either a "U"-shaped snap-on extrusion (Fig. 20) or by swaging the lip of the frame over the glass (Fig. 21).

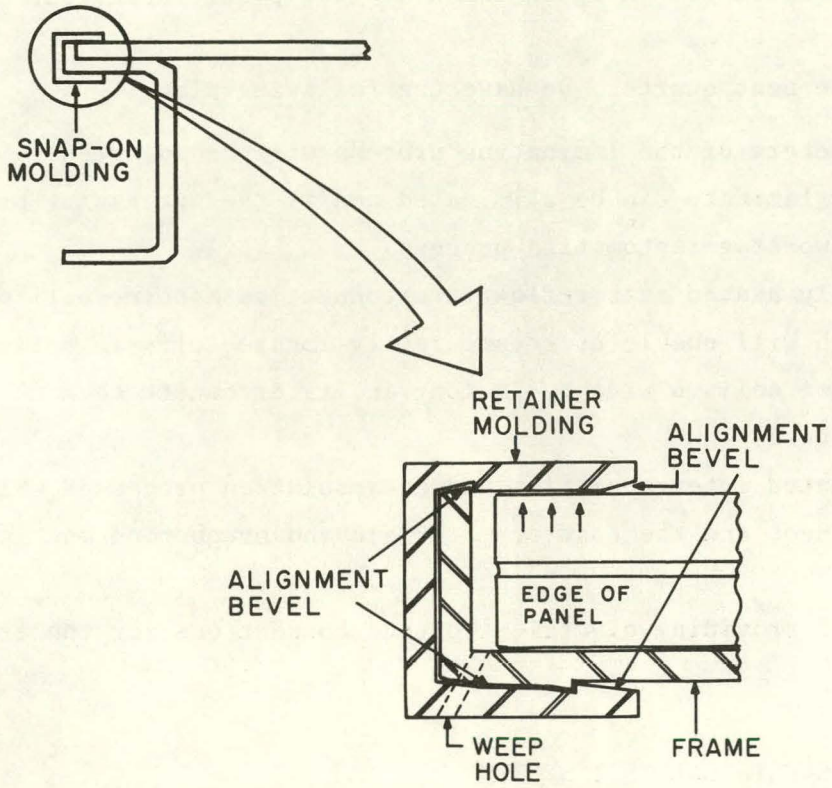


Figure 20. "U"-shaped snap-on extrusion panel retention.

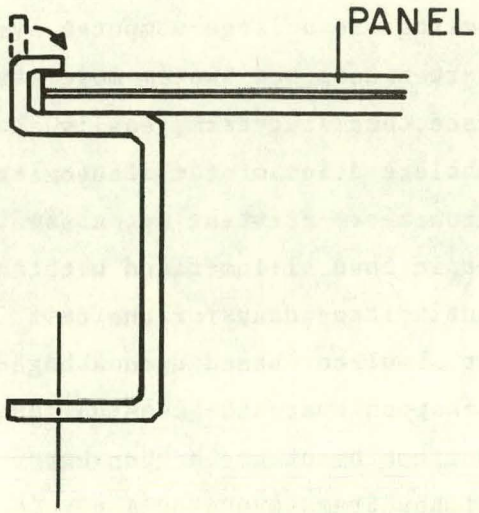


Figure 21. Swaging technique for panel retention.

During the next quarter, we have the following plans:

(1) The parameters of the laminating process will be adjusted to see if edge bubbles in the laminate can be eliminated and if the successful process can be adapted to a two-stage automation process.

(2) A radiantly heated mass reflow interconnection machine will be designed and built which will enable us to accurately locate cells in a tightly packed configuration of cells 6 wide by 15 long and interconnect them in a single continuous process.

(3) The automated interconnection and encapsulation processes will be more precisely defined, and the cost of materials and production machines will be established.

(4) Methods of providing electrical output connections for the arrays will be investigated.

F. AUTOMATIC ELECTRICAL TEST SYSTEM

Complete testing of the illuminated I-V characteristics of photovoltaic devices is necessary for process control and quality assurance. This requires an automated test technique which is fast and accurate and conveniently handles the information obtained. Our automated data acquisition system comprises a calculator, digital voltmeter, and multiplexer. These are interfaced with an AM1 illumination source and an electronic load. The data, raw I-V characteristics and calculated parameters, are initially recorded on magnetic tape cassettes

and subsequently transmitted to a large computer system which supports a data base structure. The larger computer system more easily provides formated output, statistical analyses, and long-term, easily accessible data storage.

Figure 22 shows a block diagram of the automated test system which we have developed during this quarter. For testing, a solar cell must be electrically connected to an electronic load, illuminated with AM1 insolation, and the load swept to provide current voltage data for the cell. The AM1 illumination source is an Oriel* 1-kW solar simulator based upon a high-pressure xenon lamp. It provides uniform illumination over a 3-½x3½-in.-square area. The electronic load is an RCA-designed instrument which upon external triggering sweeps the I-V characteristics of the solar cell from I_{sc} to V_{oc}. The overall sweep rate can be adjusted on this instrument; however, the sweep is not a simple linear ramp. In the region of the solar-cell knee, when dI/dV is decreasing rapidly, the voltage ramp slows up so that adequate data can be obtained in this critical region. This instrument also incorporates separate buffered outputs for both the cell voltage and current. Additionally it provides a "cell power" output obtained by internal analog multiplication of cell voltage and cell current; however, this feature is not used in our test procedure.

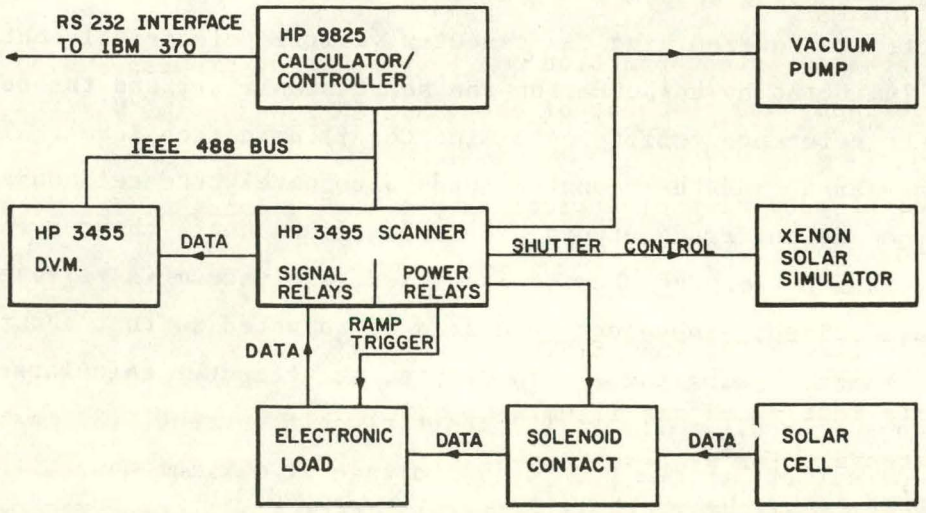


Figure 22. Automated test system block diagram.

*Oriel Corporation, Stamford, CT.

A Hewlett-Packard* 9825A calculator controls the entire system, handling all outputs, inputs, calculations, and instrument controls. The calculator uses the IEEE bus to control and communicate with the digital voltmeter and the scanner. Actual measurements are made by the digital voltmeter which is set to the correct range and function by the calculator. The scanner multiplexes the various inputs to the digital voltmeter and controls other system actions by means of a bank of relays. The power relays actuate the solar simulator light shutter, the cell vacuum hold down, and the cell contact actuator. The input multiplexing portion of the scanner switches the digital voltmeter input between current and voltage outputs of the electronic load, contact resistance checks, and illumination and temperature monitors.

Figure 23 shows a cell-testing stage with a 3-in.-diameter solar cell in the test position. A reference solar cell, visible on the right-hand side, measures the illumination level prior to each cell-testing sequence. A copper-constantan thermocouple is also part of the cell test fixture to monitor the fixture temperature during each I-V test. On the right is a solenoid-actuated contact to the metallization on the sun-side of the cell. This contact consists of two electrically isolated probes so that a resistance check between these probes can be made to ensure proper contact to the solar cell under test. Back contact to the solar cell is made via the entire fixture surface area.

The cell-testing sequence begins with vacuum being applied to the cell; the contacts are lowered, and the computer verifies electrical contact. The cell is illuminated by unshuttering the solar simulator, and the computer measures the reference cell to determine the illumination level. The electronic load is triggered, and the computer reads alternately the cell current and voltage from the buffered outputs. This continues until the current decreases to zero, at which time the shutter is closed, the vacuum is released, and the contacts are raised. The electronic load is adjusted so that about 100 data points are taken. Using these data points, the computer calculates the following: (1) open-circuit voltage, (2) short-circuit current, (3) maximum power output, (4) current at maximum power, (5) voltage at maximum power, (6) fill factor, (7) efficiency, (8) series resistance, (9) shunt resistance, (10) illumination level during the test, and (11) fixture temperature during the test. This

*Hewlett-Packard Corp., Palo Alto, CA.

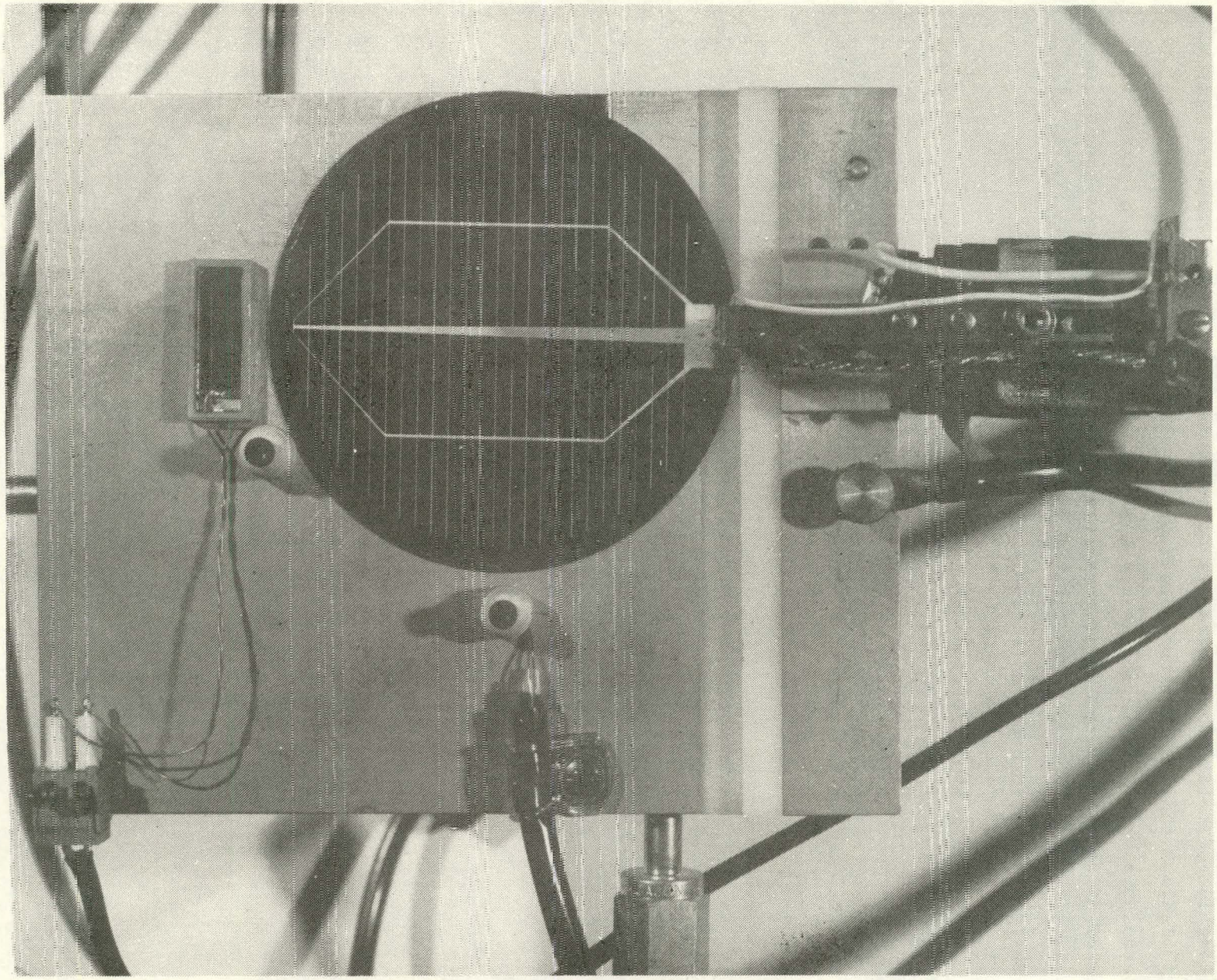


Figure 23. Photograph of cell-testing stage of testing system.

information is recorded on the magnetic tape cassette.* Following the testing of one lot of cells, these data are communicated to a larger computer system.

Table 9 shows a formated output of the data transmitted by the calculator to the data base. Table 10 shows a histogram of cell efficiency versus the number of cells for one lot of commercial solar cells. Features such as these as well as other statistical analyses are readily available through simple on-line commands within the data base language structure.

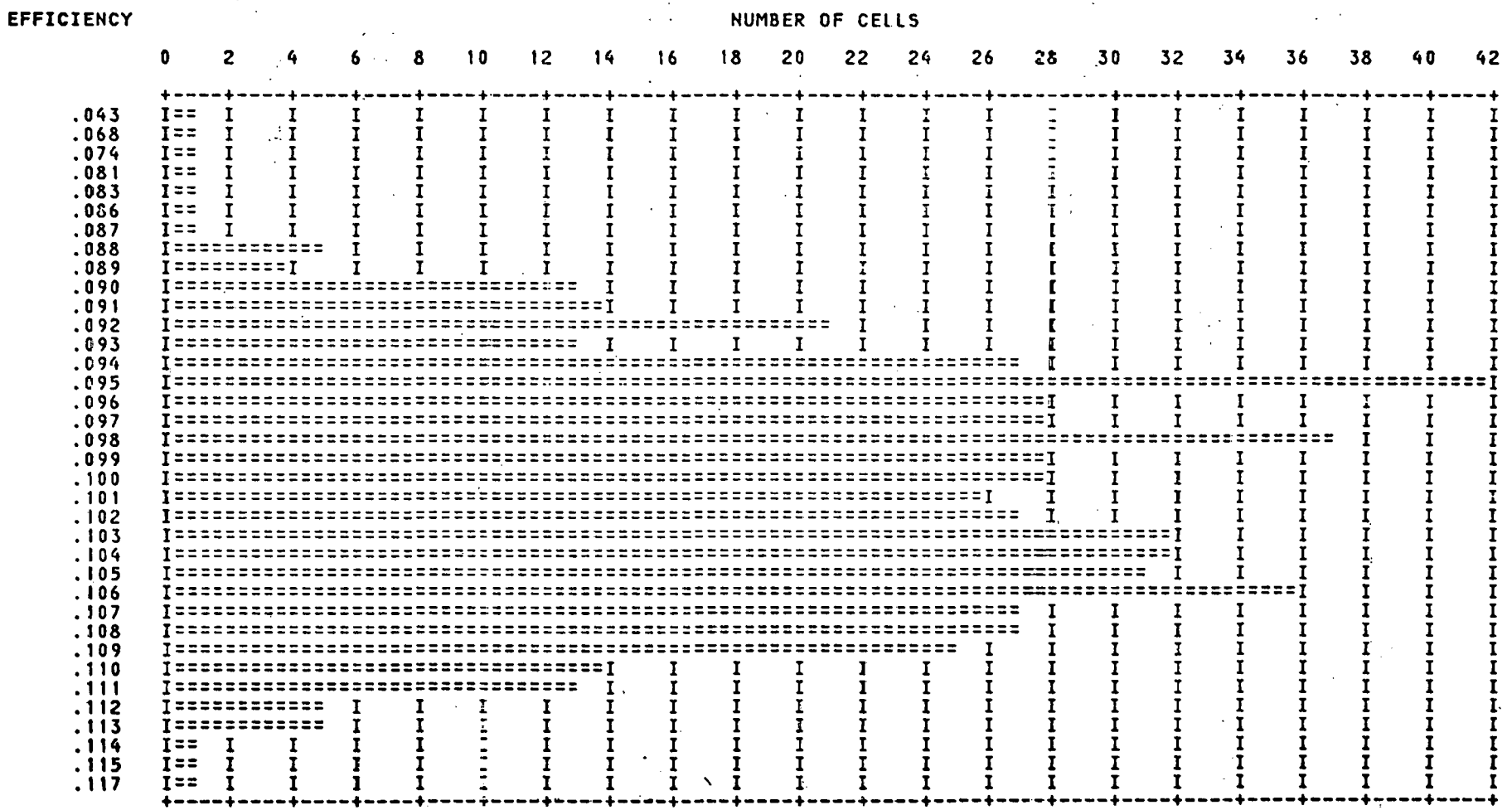
*The time required to accomplish all of this is about 20 s/cell, including the time required to load the cell.

TABLE 9. DATA TRANSMITTED BY CALCULATOR TO DATA BASE

LOTNO	TESTDT	AREA	CELL NUMBER	IRRADANCE	OPN CIR VOLT	CELL CURRENT	MAX POWER	FILL FACTOR	SERIES RESIS
4	79/04/05	45.00	OCLI004051	102.0	.575	1,210.	10.90	.708	.068
			OCLI004052	102.0	.574	1,190.	10.80	.713	.064
			OCLI004053	101.0	.570	1,220.	9.83	.637	.093
			OCLI004054	101.0	.571	1,190.	10.50	.699	.073
			OCLI004055	100.0	.573	1,220.	10.80	.693	.072
			OCLI004056	101.0	.575	1,260.	11.00	.682	.075
			OCLI004057	101.0	.572	1,200.	10.80	.710	.069
			OCLI004058	100.0	.574	1,250.	11.10	.699	.067
			[illegible]059	100.0	.568	1,190.	10.40	.692	.073
				101.0	.574	1,240.	10.90	[illegible]	.071
				100.0	.572	1,250.	10.60		.076
				[illegible]9	.574	1,230.	11.2[illegible]		.066
					.574	1,190.	[illegible]		062
					.573	1,180.	[illegible]	.739	[illegible]
					[illegible]	[illegible]	10.70	.739	
						[illegible]	11.00	.698	
			[illegible]			[illegible]	10.50	.696	.06[illegible]
			OCLI0049[illegible]			1,190.	10.80	.713	.067
			OCLI004094			1,150.	10.30	.704	.067
			OCLI004095	[illegible]	[illegible]	1,160.	10.[illegible]0	.689	.073
			OCLI004096	100.0	.567	1,130.	10.40	.725	.067
			OCLI004097	100.0	.574	1,240.	11.30	.712	.065
			OCLI004098	100.0	.568	1,190.	10.50	.701	.071
			OCLI004099	100.0	.568	1,150.	10.40	.720	.065
			OCLI004100	101.0	.573	1,220.	10.80	.694	.067

SHUNT RESIST	JCT DEPTH	SHEET RESIST	CONTACT RST	METAL RST	PMAX CURRENT	PMAX VOLTAGE	EFFICIENCY	BASE TEMP
5.03	1.00	1.0	1.00	1.00	1,110.	.442	.107	27.5
16.60	1.00	1.0	1.00	1.00	1,070.	.454	.106	27.8
13.90	1.00	1.0	1.00	1.00	1,070.	.415	.098	28.0
24.60	1.00	1.0	1.00	1.00	1,070.	.443	.105	23.1
4.34	1.00	1.0	1.00	1.00	1,030.	.448	.107	28.1
10.50	1.00		1.00	1.00	1,130.	.437	.109	28.1
3.08	1.[illegible]		[illegible]0	1.00	1,100.	.443	.108	28.0
4.61		1.0		1.00	1,130.	.443	.111	28.[illegible]
10.10		1.0	1.0[illegible]	1.00	1,090.	.432	.104	
3[illegible]	.00	1.0	1.00	1.00	1,130.	.437	.108	
	1.00	1.0	1.00	00	1,110.	.431		[illegible]
	1.00	1.0	1.00		1,130.	.448		28.0
.44	1.00	1.0	1.00		1,110.	.448	[illegible]	28.2
4.55	1.00	1.0	1.00	1.	[illegible]070.		.106	28.0
7.08	1.00	1.0	1.00	1.00			.112	28.1
5.06	1.00	1.0	1.00	1.00			.110	23.2
7.39	1.00	1.0	1.00	1.00	1,0[illegible]	.454	.108	27.9
4.59	1.00	1.0	1.00	1.00	1,060.	.443	.105	28.1
27.10	1.00	1.0	1.00	1.00	1,090.	.448	.108	28.2
7.39	1.00	1.0	1.00	1.00	1,100.	.438	.106	28.2
10.90	1.00	1.0	1.00	1.00	1,110.	.455	.112	28.4
3.55	1.00	1.0	1.00	1.00	1,100.	.453	.109	28.3
307.00	1.00	1.0	1.00	1.00	1,070.	.443	.105	28.6
3.00	1.00	1.0	1.00	1.00	1,120.	.426	.106	28.4
3.75	1.00	1.0	1.00	1.00	1,130.	.437	.109	28.6
3.87	1.00	1.0	1.00	1.00	1,050.	.442	.102	23.4
5.96	1.00	1.0	1.00	1.00	1,030.	.453	.103	27.[illegible]
7.58	1.00	1.0	1.00	1.00	1,090.	.437	.105	
11.60	1.00		1.00	1.00	1,080.	.454	.1[illegible]	
17.50	[illegible]		[illegible]	1.00	1,090.	.454		
2.33				1.00	961.	.448		
208.00				1.00	1,030.	.43[illegible]		
[illegible]				[illegible]	1,130.			
					1,100.			
					1,090			

TABLE 10. HISTOGRAM OF EFFICIENCY AT P_{MAX} VS CELLS (500 CELLS)



SECTION V

PROGRAM PLAN AND PLANS FOR NEXT QUARTER

A. PROGRAM PLAN

The time schedule in our Process Development Plan (Fig. 24) called for the beginning of solar-cell production in the first month of this quarter with "solar-grade" wafers for all three manufacturing sequences. Because of delays in the delivery of these wafers, the starting time of this portion of the plan will be moved back by two months. This will require some acceleration in cell processing so that panel assembly will not lag too far behind. In addition, no sheet silicon has been received to date, and by the vendor's* estimates, the earliest date expected for the first shipments is the end of July. This delay will require some readjustments of the amount of evaluation devoted to sheet silicon in this program.

Since no "in-house" solar cells were available for panel assembly, and until cell production catches up, that portion of the program will be devoted to refinement of the double-glass lamination process with a goal of verifying a two-step lamination process as described in Section IV.E. In addition, a radiant-heated reflow solder assembly suitable for large (up to 4x4 ft) panels is under design and construction.

B. PLANS FOR NEXT QUARTER

The items planned for next quarter are:

(1) Begin process evaluation testing of solar cells produced with "solar-grade" wafers to include evaluation of the implanted junction, screen-printing of contacts and spray deposition of AR coatings.

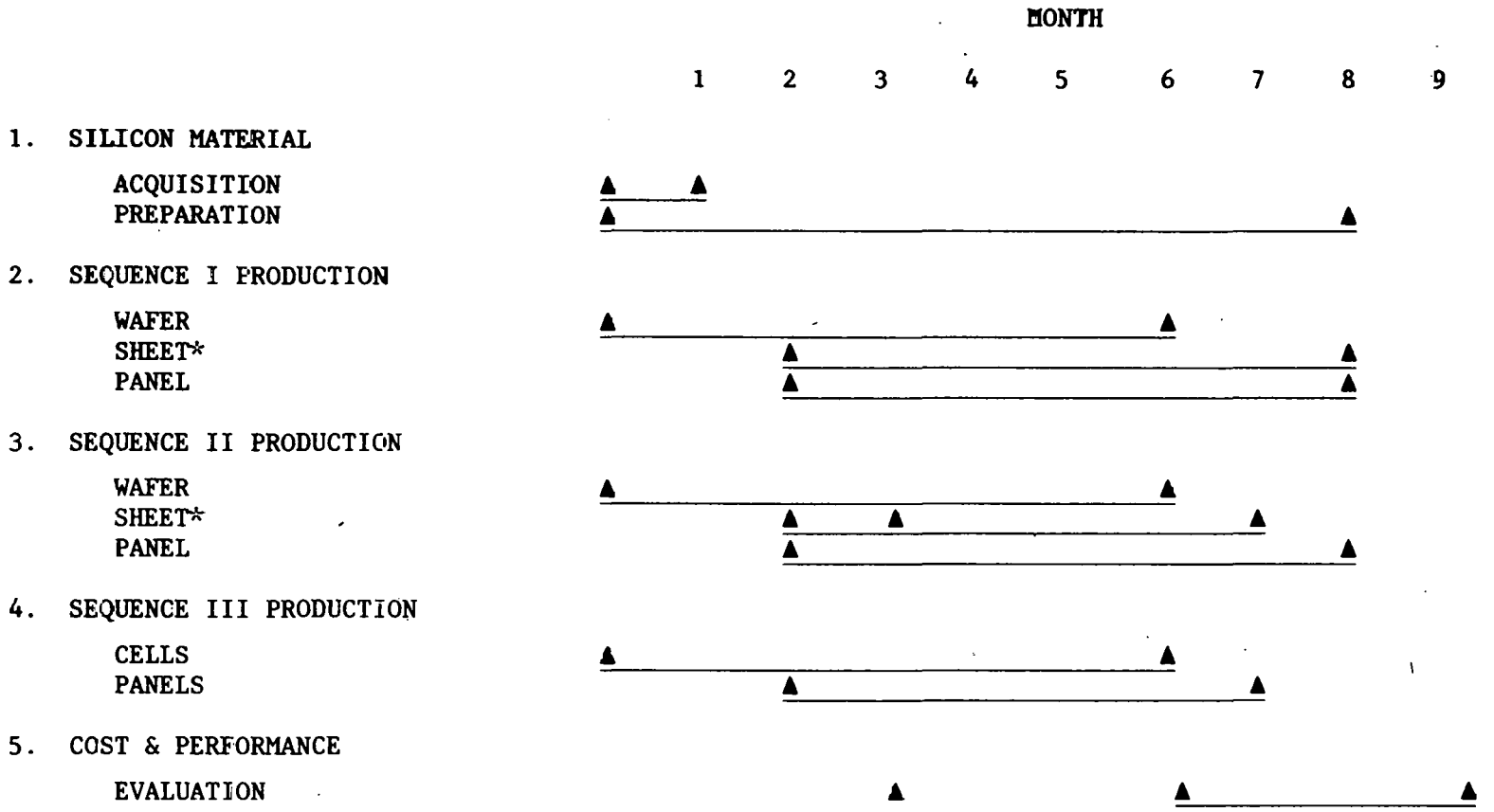
(2) Further evaluations of the quality of AR coatings sprayed-on with the Zicon 9000 autocoater.

(3) Additional experiments in the qualification of an aluminum p^+ BSF process.

(4) Initial testing of a radiant-heated solder reflow assembly.

(5) Qualification tests of our automatic electrical testing system will be conducted.

*Mobile-Tyco Solar Energy Corporation, Watham, MA and Westinghouse Electric Corporation Research and Development Center, Pittsburgh, PA.



*Time plan based on availability and delivery of sheet silicon.

Figure 24. Milestone Plan.

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