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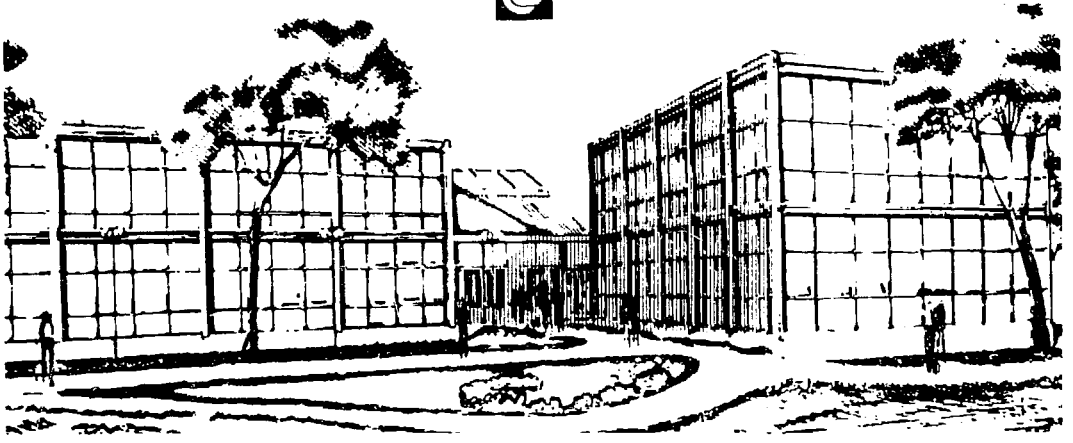

DESIGN OF A FIBER OPTIC MULTI-TAPPED COMPUTER BUS FOR A PULSED POWER CONTROL SYSTEM APPLICATION*

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ABSTRACT

Control system techniques developed and proven on the Shiva laser have been extended to incorporate new electronic and electo-optic devices as well as conform to unique operational requirements of the 300 terawatt Nova laser system. This paper describes one segment of the control system being designed for the Nova laser currently under design/construction at Lawrence Livermore Laboratory. The specific segment covered is the control system bus structure responsible for power conditioning and real-time control functions.

Redundant Digital Equipment Corp. LSI-11 microprocessors are used as front end processors each with its' Q-BUS serialized and extended throughout the laser system. Each fiber optic bus is operated at 10 Mbps and is tapped at each major laser system device that is controlled, monitored, or synchronized. Design of the bus structure is heavily influenced by the need to operate in a hostile environment of high voltages (25 kV), high currents (20 MA), and extreme fields during the 400,000 megawatt pumping of the laser amplifiers and optical shutters. Operational requirements for redundant bus operation and system synchronization are also incorporated into the bus structure.

*Work performed under the auspices of the U.S. Department of Energy by the Lawrence Livermore Laboratory under contract no. W-7405-Eng-48.

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Background

At Lawrence Livermore Laboratory, high energy laser systems are being used to investigate the physics associated with inertial confinement fusion. To carry out this research, a succession of increasingly more powerful lasers have been constructed. The latest of these lasers (Shiva) is capable of delivering 27 terawatts of 1.06 μm light onto a small deuterium/tritium pellet. The successor to Shiva, now in the design phase, will be a 300 terawatt laser called Nova. Nova is scheduled to begin operation during the first quarter of calendar year 1983.

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Associated with a large laser system is the need to deliver large amounts of pulsed electrical power to laser amplifiers and optical shutter devices. The subsystem responsible for managing the electrical energy portion of the laser is called the power conditioning system. For Nova, the power conditioning system must deliver some 400,000 megawatts of power to laser components at shot time. The required energy is taken from the commercial power grid over a period of many seconds and stored in capacitors. Just prior to the switchout of the laser pulse, the capacitors are discharged to pump the laser amplifiers and activate optical shutters.

Pulsed power systems have traditionally been controlled using "hard wires" because of their limited control requirement and the hostile environment in which they function. However, as pulsed power systems increased in complexity, the need for more versatile control techniques became mandatory. During the past ten years, automated control systems have been successfully used with large pulsed power systems e.g., the Shiva laser at Livermore. Problems caused by high voltages, high currents, and high fields have been overcome in a variety of ways.

Major controlled components of the pulsed power systems includes high voltage power supplies (25 kV), ignitron switches, and electrical distribution racks. In addition the control system monitors the safety interlock system, ensures operational readiness of the overall laser, and synchronizes all subsystems during the countdown and switchout of the laser pulse.

Introduction

This paper deals with the architecture of the bus system associated with the power conditioning control system. The Nova control system is an upgrade of the Shiva system and uses a similar architecture. Both systems are structured around an extended computer bus for distribution of control signals. The main difference between systems is that Shiva uses a parallel copper bus and Nova will use a serial fiber optic bus. There are advantages and disadvantages to both implementation methods. Copper bus systems can be readily tapped but comparable connections are difficult with fiber bus systems. On the other hand, isolation requirements for pulsed power applications are easily satisfied with a fiber bus but requires extensive segmentation (electrically isolated segments) of a copper bus. The remainder of this paper will summarize some of the tradeoffs related to choosing the bus architecture for the Nova control system and will briefly describe how laser system devices are interfaced to the control system.

Extended Computer Bus

Computer systems are made up of devices interconnected by a combination of bus systems and communication links. The choice of interconnecting method is usually based on a tradeoff between speed and cost. Typically a CPU and memory exchange data via a parallel bus whereas a CPU and a teletype exchange data via a serial communication link. Rarely is the CPU bus extended much beyond the chassis containing the CPU i.e., 50 feet is a long bus. Further bus extensions can generate timing problems with asynchronous bus systems being more tolerant than synchronous bus systems. However, extended bus systems do offer advantages that are very attractive from a control system viewpoint.

First, the software that controls the bus is greatly simplified since the bus extension is transparent to the software. Secondly, the efficiency of the bus for handling data (data bandwidth) is not degraded by the protocol associated with a communication link. Together these two characteristics provide for an efficient hardware/software data transport system typically required for a real-time control system.

Figure 1 illustrates the basic concept of an extended bus. When utilized with pulsed power devices, a significant amount of isolation is required to allow for ground displacements of several hundred volts. Using Shiva as an example, figure 2 shows that each device is isolated from other devices on the bus and that the entire bus system is isolated from the control room. Devices are optically isolated from each other by 3 kV and the control room is isolated by 60 kV.

Fiber optic technology was insufficiently mature to be used for Shiva but has rapidly progressed over the past three years. Inherent features of fiber optic communication makes it a natural choice for use with pulsed power systems. Fiber systems do not conduct electricity, they are immune to external electromagnetic fields, and they have very wide bandwidths. Furthermore, prices for fiber optic devices are now so low that in many cases they compete with copper systems on cost alone.

An inherent weakness of fiber systems appears in the fiber optic receiver which converts the optical signal to an electrical signal at TTL levels. The receiver must have a very high gain-bandwidth product due to the low power level of the incoming wide bandwidth optical signal. As with any high-gain, wide-bandwidth device, the receiver tends to be susceptible to noise; this necessitates careful design consideration of grounding, shielding and filtering.

Serial or Parallel Bus

The Digital Equipment Corp. LSI-11 computer uses a multiplexed parallel bus for communications between devices within a chassis. This bus, known as the Q bus, is asynchronous in structure and uses handshaking control signal between bus devices. Each bus transaction is completed within about 10 microseconds or a timeout occurs. Any extension of the bus must take into account the additional delay incurred and ensure that bus timeouts do not result. If propagation delays were the main concern, the bus could be linearly extended for thousands of feet, but differential delay between bus lines (skew) turns out to be the limiting parameter for optically isolated parallel buses. For example, 500 nanoseconds was required to deskew the 20 parallel line Shiva Q-bus for each isolation stage. Thus, Shiva bus transactions are delayed by 4-6 microseconds.

Skew is not a problem with a serial bus since there is only a single line. However differential delays as a result of differences in turn-on and turn-off switching times cause problems which, when resolved, result in an increased propagation delay. The main timing consideration for serial systems is multiplexing the original parallel bus data, sending it over a single signal channel, and converting the returning serial data to the parallel bus format. Such a multiplexing system necessitates the serial system operation at relatively high speeds. Using a 10 megabits per second system, the Q-bus can be serialized with an overhead of less than 4 microseconds. As explained later, complex bus structures increase this overhead to 6-7 microseconds which is well within the timeout interval.

Figure 3 illustrates some of the relative merits between a serial fiber optic bus and a parallel copper bus. The arrow indicates the current trends in technology advances favoring one or the other.

Bus Networks

The three basic structures for an extended bus network are shown in Figure 4. For large networks there are many parameters that influence the choice between these three types and in general the resulting network is a combination of the basic types. Factors that have a significant influence on the bus configuration for Nova include:

1. Number of nodes
2. Availability of bus elements
3. Failure modes
4. Cost

The choice of network can greatly affect the implementation cost for a large bus system such as that for Nova, where there are 140 nodes to service 10 laser arms. The central control network is the most expensive with the tapped "T" being the least expensive. Limitations of available fiber optic receivers, transmitters, and couplers introduce additional restrictions on the bus network architecture. New and improved fiber optic devices are constantly being developed and the Nova schedule allows for incorporation of new devices through calendar year 1980. Specific limitations are:

1. Transmitter output power
2. Receiver dynamic range
3. Coupler, cable, and connector losses
4. Differential switching times
5. Propagation delay

The network that is most easily implemented is the repeater chain. Its major fault is that any one element fails, the network fails i.e., the "christmas tree light" effect. Tentative solutions to this particular

problem are shown in figure 5. Repeaters efficiently resolve the first four limitations listed above but propagation delays add with each repeater in the chain. The first repeater in a chain delays each bus transaction by up to 3.4 microseconds and each additional repeater adds up to 200 nanoseconds of delay. Thus a chain of fifteen repeaters could delay each bus cycle by 6.2 microseconds, and repeater chains with greater than 33 serial repeaters could delay 10 microseconds and cause the processor to timeout.

As mentioned previously, the Nova bus has about 140 nodes. Allowing an average of 10 nodes per chain requires that the Nova network have between 10 and 20 parallel chains. Thus the control computer bus is first fanned out into a number of parallel chains and later fanned in to a single chain. The technique used to cope with differential propagation delays among chains is explained later. Figure 6 depicts one half of the envisioned bus network for Nova. The second half is a redundant network that also interfaces with all devices of the power conditioning system.

Message Format

The LSI-11 Q-bus is comprised of some 56 discrete signals with 16 being for data, 18 for address, and 22 for control. The Q-bus is both asynchronous and multiplexed with each bus transaction sequenced by "handshake" signals between the device initiating the bus cycle (normally the CPU) and the responding device. The selection of which Q-bus signals to send and in what order to send them over the serial bus involves many tradeoffs. The serialized message must contain address bits, data bits, and control bits. How many of each and in what configuration determines the message format. Primary factors influencing the Nova format are the following design goals:

1. Transparent to all CPU operations
2. Compatible with multi-tapped bus networks
3. Incorporate global (address independent) control capability
4. Compatible with active or passive starred networks
5. Inherent error checking
6. Compatible with redundant bus operations

The resulting message format is shown in figure 7. Each message begins with a start bit followed by 12 address bits and an input/output bit to designate if the message is a request for input data or an output command. The next two bits are global command bits and also provide the necessary delay between the address bits and the data bits. The global master reset command supports redundant bus operations and the universal trigger bit supports system synchronization. Both global commands are explained later in this paper.

The highlight of this message format is the placement of the reply bit just prior to the data bits. The reply bit is set by a remote device when it receives a message and recognizes the address as its own. Placing the reply bit in this position accomplishes two functions. First it is early in the wavetrain and thus returns to the CPU after only minimum delay. The returned reply bit allows the CPU to procede with bus sequencing thus minimizing bus transaction delays. Secondly it greatly facilitates the usage of starred networks without differential delay problems.

Differential Delay

An inherent problem associated with starred networks i.e., networks incorporating fan-out and fan-in devices, is how to cope with the different propagation times between chains from the fan-out star to the fan-in star. An obvious solution, but not really practical, is to add appropriate amounts of delay to the various chains such that each chain has the same delay and thus no differential delay exists. A more realistic approach to the problem is to design a "smart" fan-in star that looks at the data arriving from each chain and decides which single chain to output. Such a "smart" star would contain active components and could not be an optical coupler.

An alternative scheme, which was selected for Nova, is to incorporate some intelligence within the network structure. The Nova network incorporates repeaters with enough intelligence such that only one chain transmits into the fan in star for any given message. Such intelligence would normally require an additional delay since the decision to transmit or not transmit is based on information within the message. This delay is avoided by formatting the serial message such that the output message is a subset of the input message.

The last repeater in each chain is designed such that it does not repeat the start bit, address bits, I/O bit, or global control bits. It does repeat the reply bit and data bits if and only if the reply bit has been set by a device on its chain. Since each device address is unique, only one repeater will transmit into the fan-in star, with the reply bit becoming the start bit for a shortened message. Thus the full message, referred to as "long mode" is repeated by all repeaters except the last repeater in each chain. The last repeater transmits the truncated message, referred to as "short mode", if there was a reply by a device on its chain.

Error testing

Error testing on output command [illegible] implemented since the output command is looped back to the CPU. More extensive error testing is possible during diagnostic testing, since in this mode all repeaters in the chain containing the addressed device can be operated in the long mode. The entire message is then looped back to the CPU for error testing. Note that the previously mentioned differential delay problem does not manifest itself since no other chain contains the addressed device and thus will not transmit beyond the last repeater.

The merits of incorporating additional error detection capability in the message format are questionable. The arguments in favor of additional error detection are generally related to ensuring a single command or message is error free. For communication systems this is a very valid argument. Control systems on the other hand must ensure not only that the message was received error free, but more importantly that the device responded correctly. This requires feedback from the device, not just feedback from the bus interface. The message format readily incorporates expanded error detection, as shown in figure 7, merely by appending a cyclic redundancy check (CRC) pattern to the tail end of the message. Prototype bus interface hardware has been built without CRC mainly because of space limitations on the bus repeater and LSI-11 interface printed circuit boards; but also because control systems must measure and cope with errors in a global sense. Knowledge that an error occured in one segment of the system is diagnostically interesting but of limited operational value.

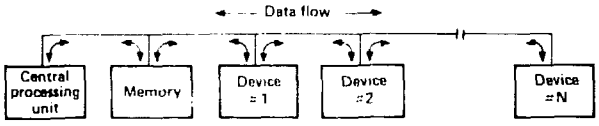
Dual Bus Operation

Each device on the power conditioning bus is serviced by two identical bus systems. Either bus can perform all control and monitoring required for each device. Part of the justification for the incorporation of a redundant bus is related to reliability. Should a segment of the primary control system become inoperative for any reason, the redundant bus can be used to continue laser operations. Such increased reliability can be easily jeopardized if bus interface failures can "lock up" the device. For example, the most complicated logic performed by a device interface is the decoding of bus addresses and the transfer of data when its address is recognized. If this logic should fail it would be impossible to remove an existing command to the device. To alleviate failures of this general type, the bus format contains a master reset bit that is not associated with a device address. When the master reset bit is asserted all command bits in all device interfaces are reset.

A greater benefit of having a redundant bus is related to operational considerations of the entire Nova system. The operation of the power conditioning system is essential for other laser systems to operate since nearly all real-time funcitons are controlled, monitored, initiated, or synchronized via the power conditioning bus. Such a tightly coupled operation is highly desireable from a system integration viewpoint but it requires that the bus system be continually operating. Should a new device be connected to the bus there is always the possibility of "bringing down the bus". Troubleshooting or maintenance activities are always risky as they may inadvertently interfere with an on-going sequencial operation. With redundant buses, technical personnel can

operate the laser system from one bus while system development, troubleshooting, and maintenance activities on the redundant bus. When a new capability is installed and validated on the secondary bus, it is incorporated into the operational system merely by changing control to the opposite bus. Such a technique has proved to be highly beneficial for the operation of the Shiva laser.

BUS COMMUNICATION



- All BUS information is available to all devices
- Each device has an unique identification (address)
- BUS implementation may be single line serial or multi-line parallel
  - Combination serial-parallel BUS designs are common
- Devices vary with respect to intelligence
- BUS signals include address bits, data bits, and control bits

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Figure 1: Block diagram showing how devices communicate using a common bus.

SHIVA POWER CONDITIONING CONTROL SYSTEM

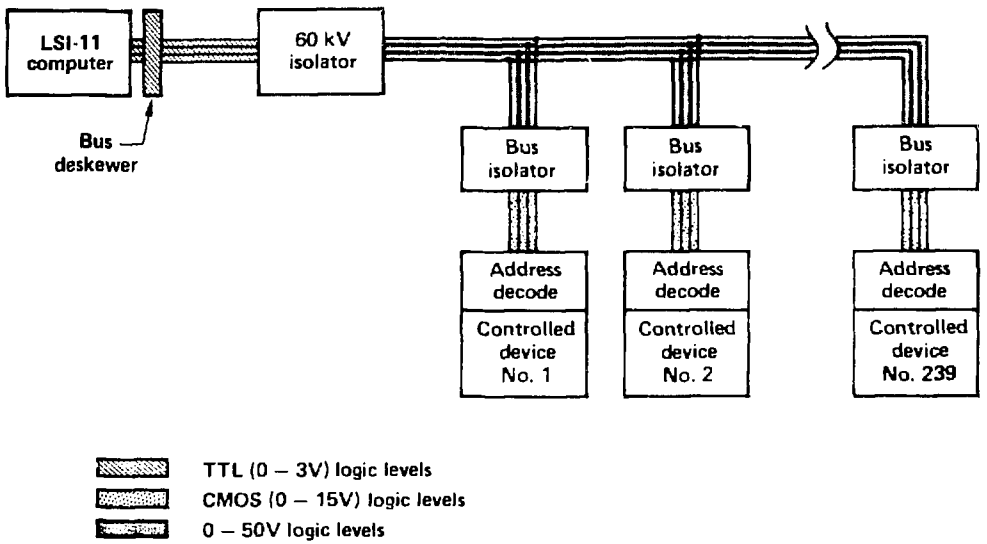

Figure 2: Devices of the Shiva power conditioning system are controlled by an isolated bus system.

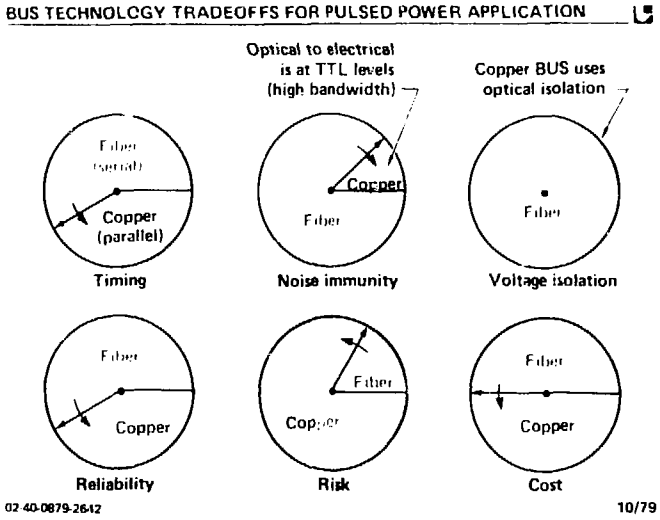

Figure 3: Factors influencing the choice of bus implementation for controlling a pulsed power system

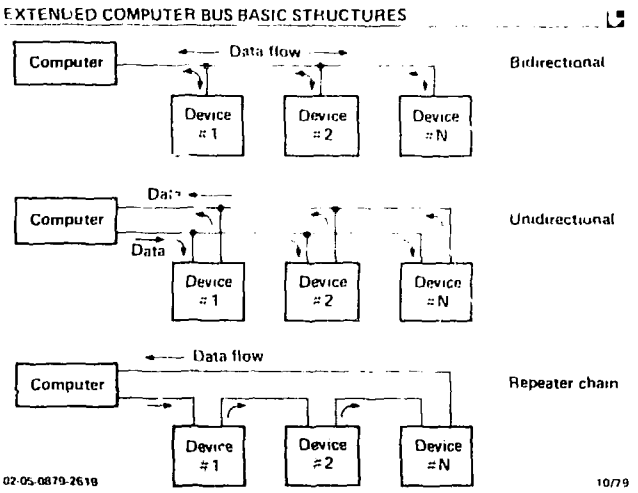

Figure 4: Basic extended bus structures.

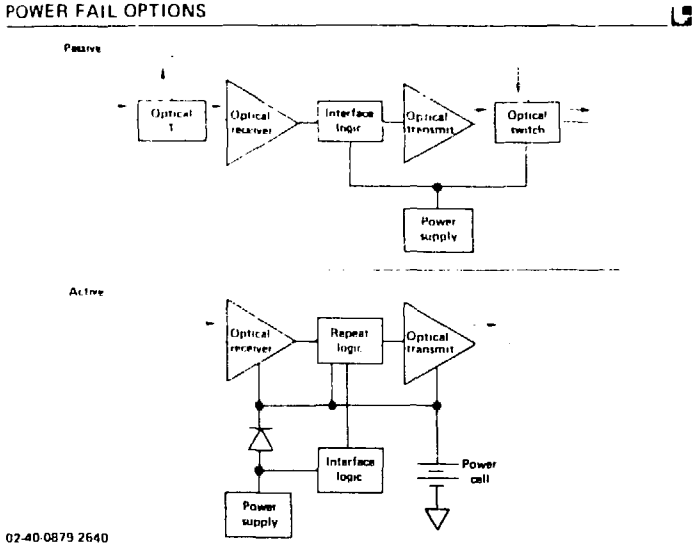

Figure 5: Potential solutions to bypass a single bus repeater in the event of a local power failure.

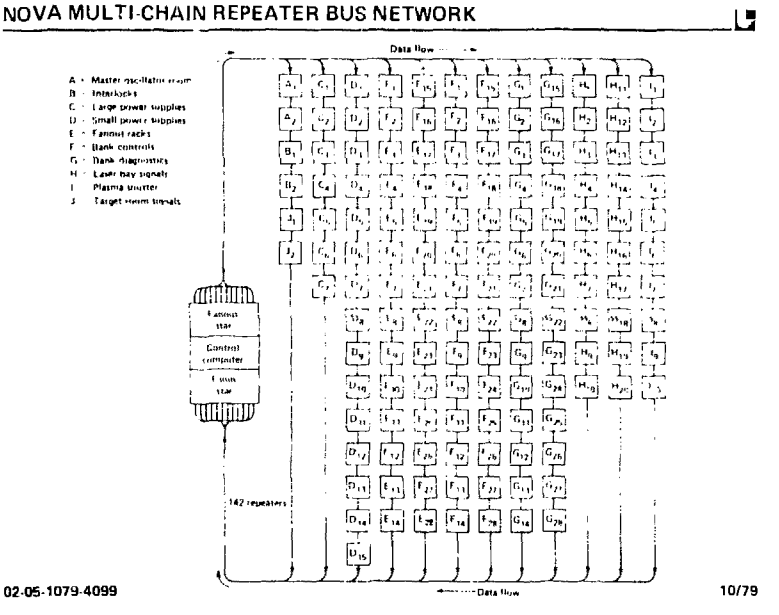

Figure 6: Block diagram showing the Nova power conditioning bus network.

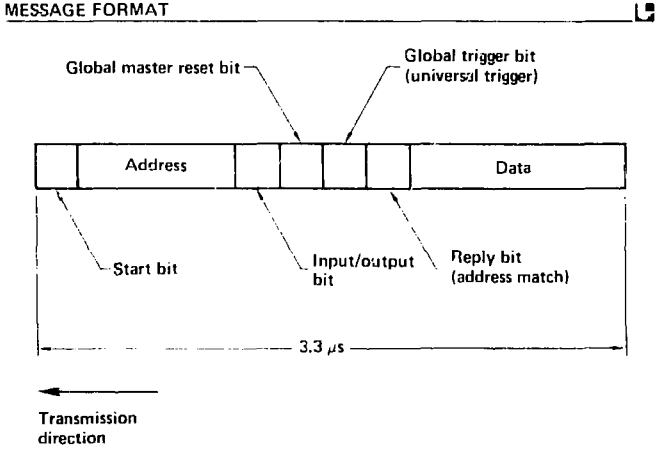

Figure 7: Message format of the Nova power conditioning bus network.