DSE-4042-T5

CADMIUM SULFIDE/COPPER SULFIDE HETEROJUNCTION CELL RESEARCH

Quarterly Technical Progress Report, February 26, 1979—May 31, 1979

By
John A. Thornton

July 31, 1979

Work Performed Under Contract No. EG-77-C-01-4042

Telic Corporation
Santa Monica, California

and

Solar Energy Research Institute
Golden, Colorado

U.S. Department of Energy

Solar Energy

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By John A Thornton

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July 31, 1979

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ABSTRACT

This report covers the work performed by Telic Corporation for the approximate period February 26, 1979 to May 31, 1979.

All-vacuum sputter deposited heterojunction solar cells of the CdS/Cu_2S and $Cd_{1-x}Zn_xS/Cu_2S$ types have been fabricated on glass substrates by dc reactive sputtering using cylindrical-post magnetron sputtering sources and Ar-H_2S working gases. The rear electrode is Nb. The top grid electrode is Au sputter deposited through a mechanical mask. Preliminary measurements on nonoptimized cells have yielded efficiencies of about 0.4% with short circuit currents of about 3 mA/cm^2, open circuit voltages of about 0.35V and fill factors of about 0.37. Extensive modifications are being made to the deposition apparatus which will permit greater control over the process variables and optimization of the cells.

A series of experiments are reported which indicated that at the high deposition temperatures used for the Cd(Zn)S deposition ($\sim 300^{o}C$), an electrically active impurity, capable of influencing both the series resistance and the junction behavior of the cells, may pass from the Nb into the Cd(Zn)S.

1. PROJECT DESCRIPTION

The program objective is to investigate and evaluate the application of cylindrical-post magnetron reactive sputtering for the production of solar cell quality thin films of CdS/Cu_2S for large-scale terrestrial photovoltaic energy conversion. The reactive sputtering process is being investigated at Telic Corporation. The coating and device characterization is being done at the Lockheed Palo Alto Research Laboratory.[1]

Under a preceding DOE contract a deposition apparatus was assembled which mounts four cylindrical-post magnetron sputtering sources, of the type shown in Fig. 1, surrounding a rotatable substrate holder containing a substrate heater. The apparatus, shown schematically in Fig. 2, permits all-vacuum solar cell structures to be formed.[2] Devices were prepared on glass substrates by dc sputtering. One sputtering source was used to deposit the rear electrode. Niobium was used for most of the work. A second source was used to deposit CdS or $Cd_xZn_{1-x}S$ by sputtering from a Cd or a Cd/Zn alloy target in an Ar-H_2S working gas. A third source was used to deposit the Cu_2S layer by sputtering Cu in an Ar-H_2S mixture. The fourth magnetron served as an auxiliary source for doping by co-deposition and/or for depositing a layer of modified composition at the rear electrode to assure an ohmic contact.

The following observations were made during the course of the previous work.

1) A tendency for cathode arcing was observed to occur at high current densities during the CdS or $Cd_xZn_{1-x}S$ deposition, particularly after sustained periods of dc operation in working gases containing a significant partial pressure of H_2S. The cause was tentatively identified as a form of unipolar arc[3] resulting from charge accumulation at insulating deposits on the cathode surface. The use of rf power eliminated the arcing. However dc was used throughout most of the program.

2) At the substrate temperatures of interest for the CdS and $Cd_xZn_{1-x}S$ deposition ($\geq 200^{\circ}C$), re-evaporation was found to limit the CdS accumulation rate to the extent to which the Cd can interact with the S flux and form CdS. At low H_2S injection rates, the CdS accumu-

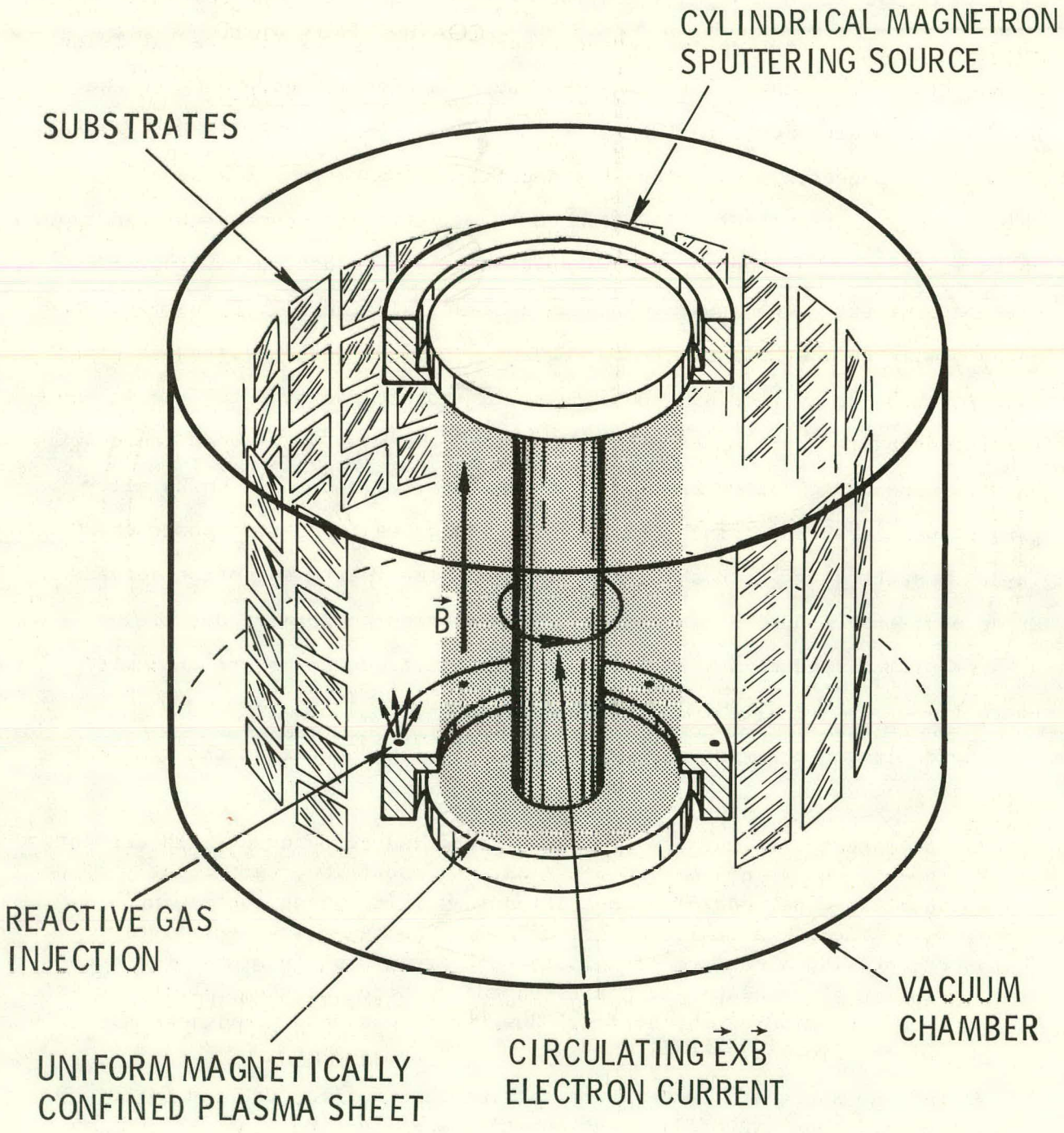

FIG. 1. Schematic representation of cylindrical-post magnetron sputtering source.

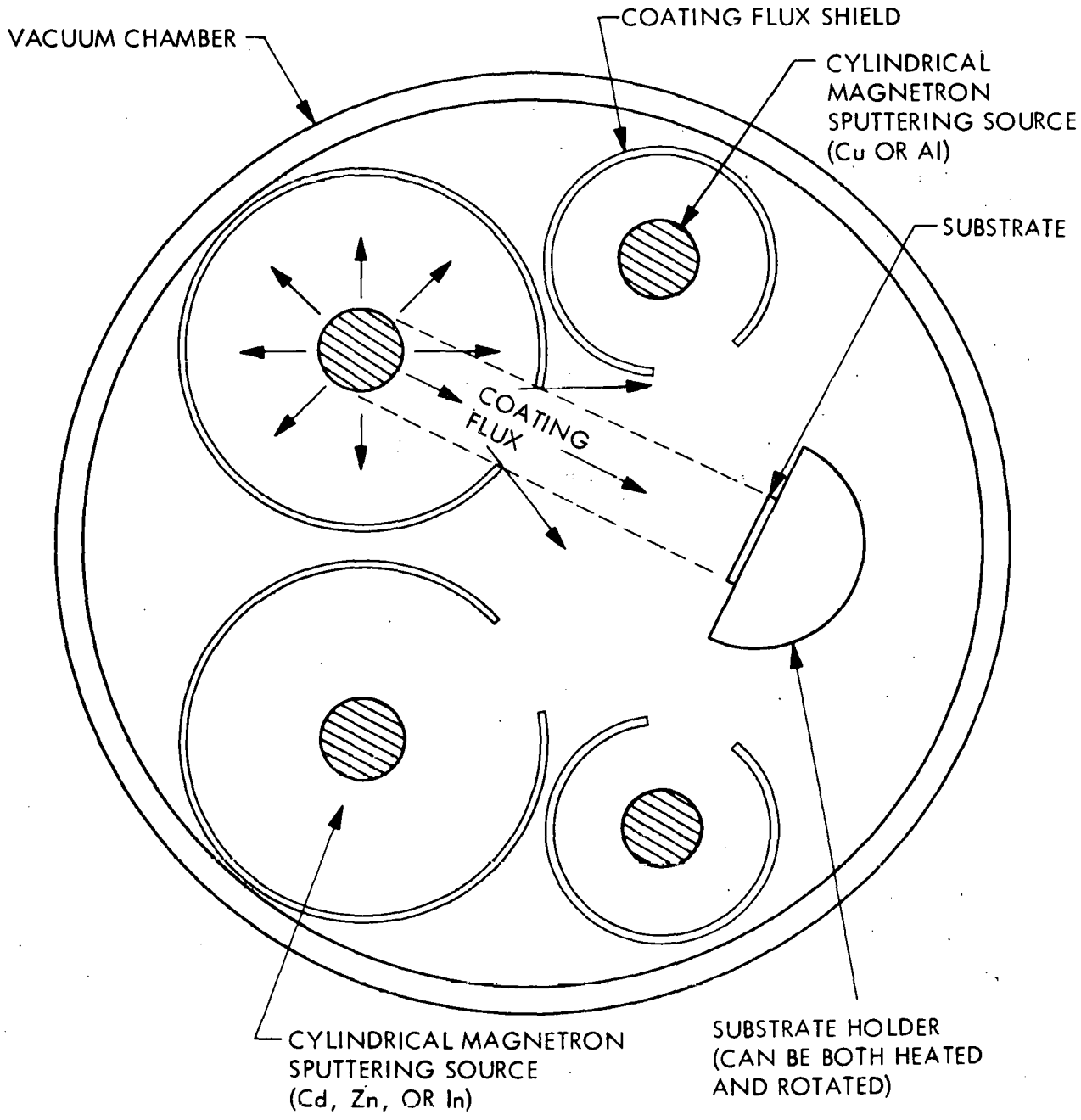

FIG. 2. Schematic diagram of multi-source deposition apparatus assembled during previous program[2] for fabricating all-vacuum heterojunctions.

lation is rate-limited by the available S flux. At high H_2S injection rates, the CdS accumulation rate is limited by the available Cd flux. The process is similar to three temperature evaporation.[4] Stoichiometric CdS tends to be formed under all conditions.

3) The resistivity of both CdS and $Cd_xZn_{1-x}S$ coatings could be controlled by indium doping. The required doping levels were established by co-deposition studies. It was concluded that a 2 atomic percent In concentration could provide $Cd_{0.9}Zn_{0.1}S$ with a resistivity of about 30 Ω-cm and that 1 atomic percent In could provide CdS with resistivity of about 3 Ω-cm. Deposition from a $Cd_{0.9}Zn_{0.1}$ target containing 2 atomic percent In yielded the expected 30 Ω-cm coatings at a substrate temperature of 300°C.

4) All-vacuum solar cell structures were fabricated with sputter-deposited $Cd_{0.9}Zn_{0.1}S$ and Cu_xS layers. Photovoltaic behavior was observed, but efficiencies were very low (~0.03%). Several deficiencies were identified in the experimental apparatus which made precise control over the deposition process and therefore optimization of the solar cell structures difficult. These included (1) the accumulation of deposits on the cathode shields and the release from these deposits of active species which can shift the operating point of the reactive sputtering process; and (2) the requirement for better control over the substrate temperature, particularly with respect to time delay (~20 minutes) required for substrate cooling between the CdS deposition, which was typically done at 300°C, and the Cu_xS deposition, which was done at 150°C or less.

The present program is structured to address the problems identified in the above observations. In particular, the program includes the following tasks.

Task 1: Deposition Process Development

This task calls for modification of the deposition equipment and procedures to overcome the deficiencies identified during the previous program. The modifications include: (1) reconfiguring the cathode shielding to remove foreign surfaces from the proximity of the cathodes and the substrates; (2) installing a vacuum interlock so that substrates can be inserted without exposing active cathode and shield surfaces to the atmosphere; and (3) redesigning the substrate holder to provide better substrate temperature control and more rapid substrate cooling. The task also includes an investigation of the use of

rf-reactive sputtering as a means for achieving higher deposition rates with the absence of arcing.

Task 2: $Cd_xZn_{1-x}S$, CdS Deposition Studies

This task concentrates on gaining improved control over the deposition of the specific semiconductor layers required for the cells. In the case of the CdS or $Cd_xZn_{1-x}S$ layer, the emphasis is on controlling the coating resistivity, either by In doping or by achieving off-stoichiometry deposits through the use of special deposition techniques or post-deposition heat treatment. In the case of the Cu_2S, the emphasis is on gaining control of the properties of Cu_xS deposited over CdS layers. (In the previous program the specific properties of the Cu_2S had been investigated only for coatings deposited on glass substrates.[2])

Task 3: Device-Material Parameter Optimization

Throughout all stages of the program solar-cell structures will be deposited and their performance evaluated as photovoltaic devices.

This report is organized with respect to the progress made during the first quarter on each of the program tasks.

2. DEPOSITION PROCESS DEVELOPMENT

2.1 Investigation of rf Reactive Sputtering

The current flow in a capacitively coupled rf sputtering apparatus is governed by the following considerations:

1) At the frequencies used (2 to 20 MHz) only the electrons can follow the temporal variations in the electric field.
2) The total electron and ion current to a given electrode over each rf cycle must balance to zero.
3) The electron flux to a given electrode is much greater than the ion flux under equivalent conditions because of the greater electron mobility.

The rf glow discharge can be pictured as an electron cloud oscillating back and forth between the electrodes at the applied frequency in a sea of relatively stationary ions. An asymmetric charge accumulates on the system

capacitance such that the average potential of both electrodes is negative with respect to the plasma potential. This potential limits the electron flux to the electrodes. Thus the oscillating electron cloud makes contact with a given electrode for only sufficient time to pass an electron flux equivalent to the ion flux throughout the rf cycle. The ions respond to the average electrode potential and bombard both electrodes throughout the rf cycle. Thus, in contrast to the dc case, both electrodes are subject to sputtering. The voltage drop in each of the electrode plasma sheaths depends on the sheath capacitances and therefore on the electrode areas in contact with the plasma. An approximated analysis suggests that the ratio of these sheath-voltage-drops varies inversely as the electrode area ratio to the fourth power.[5]

Two approaches are used in conventional sputtering sources to avoid unwanted sputtering. The so-called "double ended" approach makes both electrodes identical sputtering targets. The second, "single ended" approach uses a counter-electrode with an effective area that is much larger than that of the sputtering target. This makes the counter-electrode sheath capacitance large, so that the sheath voltage drop is less than the sputtering threshold. This is the approach used in most of the conventional planar diode sputtering sources.

Magnetron sputtering technology is basically a dc concept. Cathodes are shaped so that, in concert with the magnetic field, they form electron traps with $\vec{E} \times \vec{B}$ symmetry.[6] In a well designed system anodes are placed to collect electrons which diffuse out of the trap. In the rf case a double-ended approach can be used with special designs which provide independent magnetron traps for both electrodes but allow magnetic coupling between them, so that electrons leaving one trap can diffuse freely to the vicinity of the other trap.[7] In the present case we require that the same magnetron that was used for the dc reactive sputtering work be used for the rf studies. This dictates a single ended design. The requirements for the counter-electrode are:

1) That it have an area that is larger than that of the sputtering target.

2) That it make contact with the magnetron plasma so that the required

current can be drawn.

3) That it operate without inducing a large voltage drop. This requires that it have an effective electrode shape that is compatible with the magnetic field applied to the magnetrons.

Preliminary rf sputtering experiments were conducted during the first quarter to assist in the design of the modified apparatus. During the experiments rf power was simply applied to the Cd sputtering source with the circular cathode shield and chamber walls (Fig. 2) grounded and serving as the counter-electrode. The working gas was Ar-H_2S injected under the same general range of conditions that were used in the dc experiments. The experiments established the following.

1) The circular shields form an efficient counter electrode from an electrical point of view. The apparatus operated effectively with the plasma confined primarily within the shielded cavity. The shield area is about four times larger than the target area. This should reduce the shield voltage to an acceptable level with respect to sputtering. However, even a low energy plasma bombardment on the shield surface is undesirable, since it can be expected to remove absorbed species and influence the reactive sputtering. When the the shields were removed the chamber walls and other surfaces within the chamber were forced to serve as the counter-electrode. The axial magnetic field offered a strong impedance to the radial electron motion from the magnetron plasma to these surfaces. Consequently a discharge glow filled the entire chamber, with brighter glows apparent on the substrate holder and other internal surfaces. It is therefore concluded that the modified apparatus design should provide a counter-electrode surface of suitable size below the magnetron source, so that electrons can pass relatively freely along magnetic field lines from the edges of the magnetron plasma to the counter-electrode.

2) The observation that rf sputtering greatly reduced the tendency for cathode arcing[2] was reconfirmed. However, mirror arcing was observed, even with the rf power, when the sputtering discharge was operated at relatively high working gas pressures ($>$10 mTorr) and cathode current densities ($\sim$10 mA/cm^2- rms).

3) Deposition rate measurements confirmed that the CdS deposition rate per unit of discharge current for rf reactive sputtering is identical to that for the dc case when the rms rf current is equated to the dc current. The use of rf power should permit the deposition rate used in previous work ($\sim$0.3 nm/s) to be approximately doubled. The limitation in the rf case is the ability of the system pumps to remove

the hydrogen that is liberated by the reactive sputtering ($Cd + H_2S \rightarrow CdS + H_2$).

2.2 Cathode Arcing Observations

It is important to note that at the substrate temperatures being used (200 to 300°C), no correlation has been seen between the occurrence of arcing during dc reactive sputtering of CdS and the properties of the resulting coatings. The only observed effect is loss of precise control over deposition rate (coating thickness) because of the cessation of sputtering during an arc.

A working hypothesis, that the arcs are a form of unipolar arc[3] resulting from charge accumululation at insulating deposits on the cathode surface, has been used in seeking a method for avoiding their occurrence. Thus the reduced occurrence of arcing in the case of rf sputtering may result because the polarity reversal reduces the charge accumulation on such deposits. However, the question still remains as to why offending deposits form at localized regions on the surfaces of the high purity cathodes.

The possibility of virtually arc-free, dc reactive sputtering has been established in our recent work. CdS and Cd(Zn)S coatings of the desired thickness (3 to 6 μm) have been deposited with less than one non-sustaining arc per hour (the occurrence of arcs is monitored with a recorder). These observations permit several possible causes for the insulating deposits to be excluded. In particular, the occurrence of severe arcing does not correlate with: (1) the vacuum chamber having been open to the atmosphere for an extended period of time prior to the run in question; (2) the number of deposition runs following a change in the experimental configuration, including shield cleaning, at least for sequences involving as many as ten runs; nor (3) the presence of chips, flakes, or other debris on the anode and on the cathode end flanges. (See Fig. 1.)

Two approaches that may permit reliable arc-free operation with direct currents are also under investigation. First, it was observed during the previous program that a cathode which had drifted into a state of severe arcing could be renewed and passed into a condition of smooth operation by

simply operating for a short period (several minutes) in pure Ar. Presumably this operation sputtered the offending deposits from the cathode surface. During the present program experiments have been conducted in which the H_2S injection has been periodically ceased in an attempt to promote the formation of nonstoichiometric deposits (see Section 4.3). Preliminary observations indicate the arcing is eliminated if the off-time of the H_2S injection is of sufficient duration. Finally, in an independent Telic-sponsored project a new dc power supply with an improved arc suppression circuit has been designed and is being constructed for use on the project.

2.3 Apparatus Modifications

The specific objectives of the apparatus modifications are to:

1) Reconfigure cathode shielding to reduce the shield surface area adjacent to the sputtering sources and the substrates.

2) Install a vacuum interlock so that substrates can be inserted without exposing the cathode and shield surfaces to the atmosphere.

3) Redesign the substrate holder to permit rapid cooling of the substrates between the CdS and the Cu_2S depositions.

4) Install a movable mask to restrict Cu_2S deposition at the cell edge.

The vacuum chamber and shield surfaces can influence the reactive sputtering process in the following ways.

1) By absorbing atmospheric gases (particularly, water vapor) when they are exposed to the atmosphere during substrate loading, and the release of these species when they are placed under vacuum.

2) By acting as a catalytic surfaces for the reaction between the sputtered flux and the working gas.

3) By accumulating thick deposits after extended use and by releasing volatile reactive species from these deposits, particularly under the influence of heating.

All of these effects are exacerbated by the accumulation of thick coating deposits. Such deposits are often porous in nature (because of changing deposition conditions) and therefore present large surface areas for the absorption and reaction of gases. The close proximity of the circular shields shown in Fig. 2 to the magnetrons causes these deposits to be particularly thick (1 mm

thick deposits are routinely removed). Occasionally these deposits break loose from the shields during exposure to the atmosphere (probably because of stress formation during oxidation), thereby dumping debris onto the cathode surface.

Therefore it was concluded that the modified design should significantly increase the distance between the sputtering sources and the shields. It was also concluded that provisions should be made for cooling the shields so that the release of volatile reactive species due to shield heating could be suppressed. The vacuum interlock should greatly reduce effects due to the absorption of atmospheric gases and should also decrease the chamber cycle time for depositing coatings.

In a practical substrate holder design of the type that could be used in production coating, the substrates must be heated and cooled by radiation (methods such as the use of low melting point metals to assure thermal contact to a heated surface, although useful in research, are not believed to be practical for large scale production). Thus the minimum radiation cooling time for the 25 mm x 25 mm x 1.2 mm glass substrates currently being used is determined by the mass and heat capacity of the glass and the emissivity of the surface. The minimum cooling time for a starting temperature of 330°C and a final temperature of 50°C is about 1 minute for unity emissivity. Thus it was concluded that the approach should be to mount the glass on a holder of the smallest possible thermal mass and then to move the holder quickly from the position of heating to a cooling position where it would receive little radiation from the surrounding structure.

In evaluating the above design requirements, it became immediately apparent that the existing coating chamber was too small to permit the expanded shielding, a larger substrate holder, and the gate valve to be installed. Once it was decided that a larger chamber should be fabricated, a number of design options became possible. Therefore the apparatus modification was delayed in order to explore several of these possibilities in detail. For example, the possibility of an extensive modification that would have changed the basic configuration of the apparatus and made it more like a

production coating system was examined in some detail, but concluded to be inappropriate at the present time. The design that was finally selected is very similar in its basic features to the one which is presently in use. It is shown schematically in Fig. 3.

In the modified apparatus, substrates will be loaded onto a frame of low thermal mass and placed in a vacuum interlock chamber located above the coating chamber. After the interlock chamber is evacuated, the substrates will be passed down through a 2-inch CVC gate valve onto a carrousel type mounting frame of low thermal mass, which permits them to be rotated and passed into four different coating positions. Fixed substrate heaters are located behind the carrousel at each of the coating positions. The substrate will be quickly cooled by rotating the carrousel to pass them away from a substrate heater to a cooling position. Shields partition the chamber into compartments within which the magnetron sputtering sources are mounted. The shields are located much farther from the sources than in the old apparatus shown in Fig. 2 and have provisions for water cooling.

It is hoped that the modified apparatus can be placed in operation during the second quarter, as originally scheduled. However, several long lead time items (gate valve and magnetic field coils) are expected to delay completion until the third quarter.

3. DEVICE-MATERIAL PARAMETER OPTIMIZATION

The cells fabricated during the first quarter of the present program were of the general form shown in Fig. 4. The substrates are 7059 glass plates, 25 mm x 25 mm x 1.2 mm. A Nb rear electrode 0.10 μm thick was deposited onto the glass substrates in a separate pumpdown. These precoated substrates were then stored and used in the multi-source deposition chamber as required. A set of three substrates were coated at one time in the multi-source chamber. Predeposition pumping was typically to a pressure of 10^{-4} to 10^{-3} Pa (7×10^{-7} to 7×10^{-6} Torr). CdS or $Cd_xZn_{1-x}S$ layers, 3 to 5 μm thick, were generally deposited at a substrate temperature of 300°C, over an In layer about 0.05 μm thick. The In layer was used to assure an ohmic contact to the Nb electrode.

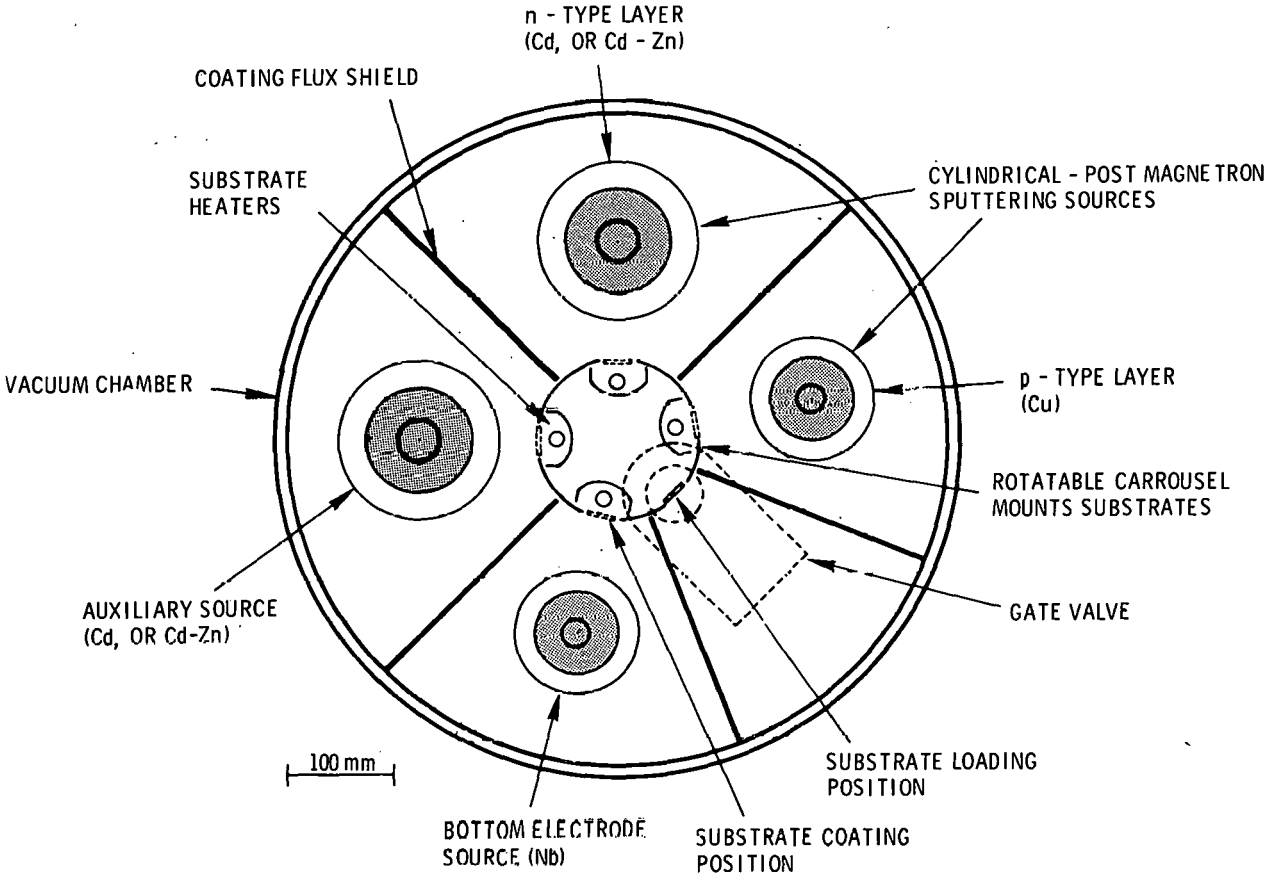

FIG. 3. Schematic diagram of modified multi-source deposition apparatus being assembled on the present program.

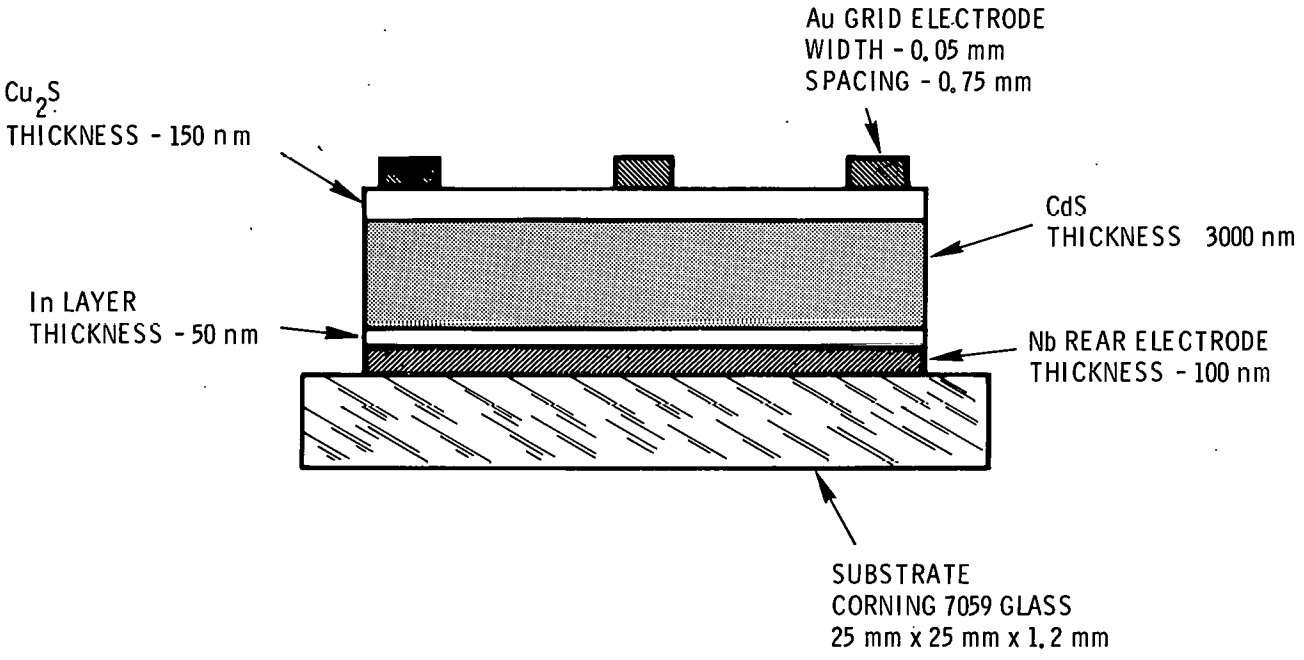

FIG. 4. Configuration of all sputter-deposited solar cells fabricated during the first quarter.

The substrates were then allowed to cool in H_2S to 150°C (requires about 20 minutes), and the Cu_xS layer was deposited. The Cu_xS layer was typically 0.15 μm thick. Finally a Au top grid electrode was applied in a separate chamber by sputter deposition, using a mechanical mask. The grid consists of 1 μm thick lines, 0.05 mm wide, spaced on 0.75 mm centers. An antireflective top layer is not being used at the present time.

Heterojunction devices fabricated during the previous program were characterized by a low short circuit current (0.19 mA/cm^2) and fill factor (0.28). The open circuit voltage was about 0.30V and the efficiencies were about 0.03%. The low short circuit current was due in part to the use of a Au pad rather than a grid top electrode. A first objective in the present program was to improve the quality of the Cu_xS layer. The cells on the previous program were fabricated by exposing the CdS coated substrates to the Cu_xS reactive sputtering flux almost immediately after igniting the Cu_2S source, while using operating conditions that had been identified in a previous study[8] to yield coatings with Chalcocite optical properties on glass substrates. Two changes in this procedure were examined during the first quarter, for two reasons. First, good sputter deposition practice suggests that a source be operated for a period of time to stabilize the operating conditions prior to exposing the substrates. Second, it was apparent that slightly modified deposition conditions were required to obtain Cu_2S coatings having the desired properties on CdS as opposed to glass substrates. Accordingly cells were fabricated with the Cu_xS source operated for a period of 4 minutes before the substrates were exposed (conditioning times are considerably shorter for magnetrons than for conventional sputtering sources because of the higher magnetron current densities). Cu_xS films deposited in this way possessed a low resistivity (10^{-2} to 10^{-3} Ω-cm) typical of Djurlete. It was not possible to increase the resistivity by decreasing the H_2S injection rate. When the cathode preconditioning step was eliminated, high resistivity coatings (10^2 Ω-cm), presumably with a high Chalcocite content, were again obtained.

It is believed that the preconditioning step may have heated the circular

shield surrounding the cathode (see Fig. 2), thereby causing the release of sulfur or sulfur-bearing species from the thick Cu_xS deposit which had accumulated there, as discussed in Section 2.3. This release removed the control which is normally afforded by the H_2S injection rate and produced coatings with a higher than expected S-content. In fact it was found that Cu_xS coatings could be deposited for an extended period, even after the H_2S injection rate was reduced to zero. This difficulty should be eliminated with the modified apparatus which places the shields further from the source and cools them, as discussed in Section 2.3.

Therefore it was concluded that (1) the fabrication of evaluation cells, prior to the availability of the modified apparatus, should be done without a preconditioning step; and (2) the Cu_xS property-versus-deposition-condition relationship for CdS substrates should be determined with the circular shields removed, in anticipation of the conditions that will be available with the modified apparatus.

Additional cells were fabricated without the Cu_xS preconditioning step. The Cu_xS was deposited using a reduced H_2S injection rate (0.1 to 0.125 Torr-liters/sec) compared to what had been used in the previous program (0.15 Torr-liter/sec) in order to assure a high resistivity Chalcocite-type Cu_xS layer. The n-type layers were deposited from a $Cd_{0.90}Zn_{0.10}$ cathode containing 2 atomic percent In, while using a substrate temperature of 300°C. The performance of these cells, although poor, was a distinct improvement over what had been achieved before. Two cells yielded a conversion efficiency of about 0.4%. Short circuit currents were improved partly from the improved grid and partly from the improved Cu_xS, but were still low ($\sim$3 mA/cm^2), as were the fill factors ($\sim$0.37). The open circuit voltages were about 0.35V. The poor fill factors were due to a high series resistance in combination with an apparent photosensitive shunt capacitance.[1] The junction characteristics were strongly influenced by deep trap levels on the $Cd_{1-x}Zn_xS$ side of the heterojunction.[1]

During the fabrication of the cells a reference sample of the CdS coating was deposited on a glass substrate over diagnostic electrodes arranged in a

van der Pauw configuration, as shown in Fig. 5. These samples yielded $Cd_{0.9}Zn_{0.1}S$ resistivities in the desired range ($\sim$100 Ω-cm). However, resistances measured through the cell thickness were inconsistently large and varied considerably from cell to cell. Therefore cell fabrication was terminated to address this problem. Work described in Section 4.1 suggests that this behavior may result from the diffusion of an electrically active species into the $Cd_xZn_{1-x}S$ or CdS from the Nb rear electrode at the relatively high deposition temperatures (300°C) being used.

Cu_2S/CdS cells were fabricated during the first quarter. These devices were characterized by an inordinately high series resistance. This was traced to the use of a sputtering target which had been mislabeled by the manufacturer as consisting of Cd doped with 1 atomic percent In but which in fact was pure Cd. (See Section 4.2.)

During fabrication of the cells it was found that the Au grid electrodes were often shorted to the Nb rear electrode because of pin-hole flaws in the Cd(Zn)S layer. Pin-hole problems in vacuum deposition can generally be traced to one of the following.

1) Particulates which enter the coating chamber on the substrates. (If the coating is done in a clean room environment such particulates are usually the result of a poor final rinsing step in the substrate cleaning.)

2) Poor adhesion because of localized regions of poor substrate preparation or of coating internal stress.

3) Debris from the shields and walls within the coating chamber which pass onto the substrates before or during deposition.

The problem in the present case was traced to poor handling procedures for the glass substrates between the time of deposition of the Nb rear electrodes and the time of cell fabrication. Improvements are also being made in the final substrate rinsing procedures.

4. CdS, $Cd_xZn_{1-x}S$, AND Cu_2S DEPOSITION

4.1 Influence of Rear Electrode on CdS

It was noted in Section 3 that resistances measured through thickness

of the CdS or $Cd_xZn_{1-x}S$ layers in the cell structures were inconsistent with van der Pauw measurements of the resistivity in reference coatings deposited at the same time. This led to a more detailed examination of the van der Pauw samples.[1] It was found that the electrical properties of CdS deposited over glass were significantly different from the properties over Nb-coated substrates. Indium contacts were pressed onto the CdS deposited over Nb metallized and unmetallized regions of the substrate, as shown in Fig. 5.[1] Contacts over the glass (positions A and B) yielded ohmic behavior when connected to each other or the Nb diagnostic electrodes. However, In contacts located over the Nb (positions C and D) were blocking in one polarity. The effect was observed for CdS, with and without an In underlayer, and for $Cd_{0.9}Zn_{0.1}S$ deposited from a cathode doped with 1 atomic percent In.

These observations, along with concern over the influence of the Nb substrate on the occurrence of pin-hole type flaws in the CdS, led to a more detailed investigation of the surface features of CdS coatings that were deposited on Nb and other substrates under various conditions. This work has resulted in the following observations.

1) The structure and surface topography of CdS coatings formed on freshly deposited Nb are strongly dependent on the substrate temperature. This is expected.[9] However, the particular results are new, since most of our previous SEM work had pertained to coatings deposited on glass substrates. SEM photomicrographs of surface topographies and fracture cross sections are shown in Fig. 6. Coatings deposited at 300°C (6A) possess a smooth glass-like surface and a dense cross section with only the slightest hint of a columnar structure. The surfaces of coatings deposited at 275°C (6B) show the appearance of distinct faceted growths protruding out of a smooth background surface of the type observed in (6A). The surfaces of coatings deposited at 250°C are dominated by the faceted surface features and exhibit a more clear columnar cross section (6C). The coatings deposited at 200°C have a rougher, more random surface (6D) and distinct columnar cross section. It should be noted that the temperatures cited above were determined from reference substrates mounted adjacent to the deposition substrates and, although reproducible, are approximations of the true physical temperatures on the substrate surface.

2) CdS coatings deposited at 300°C on Nb metallized layers, that had

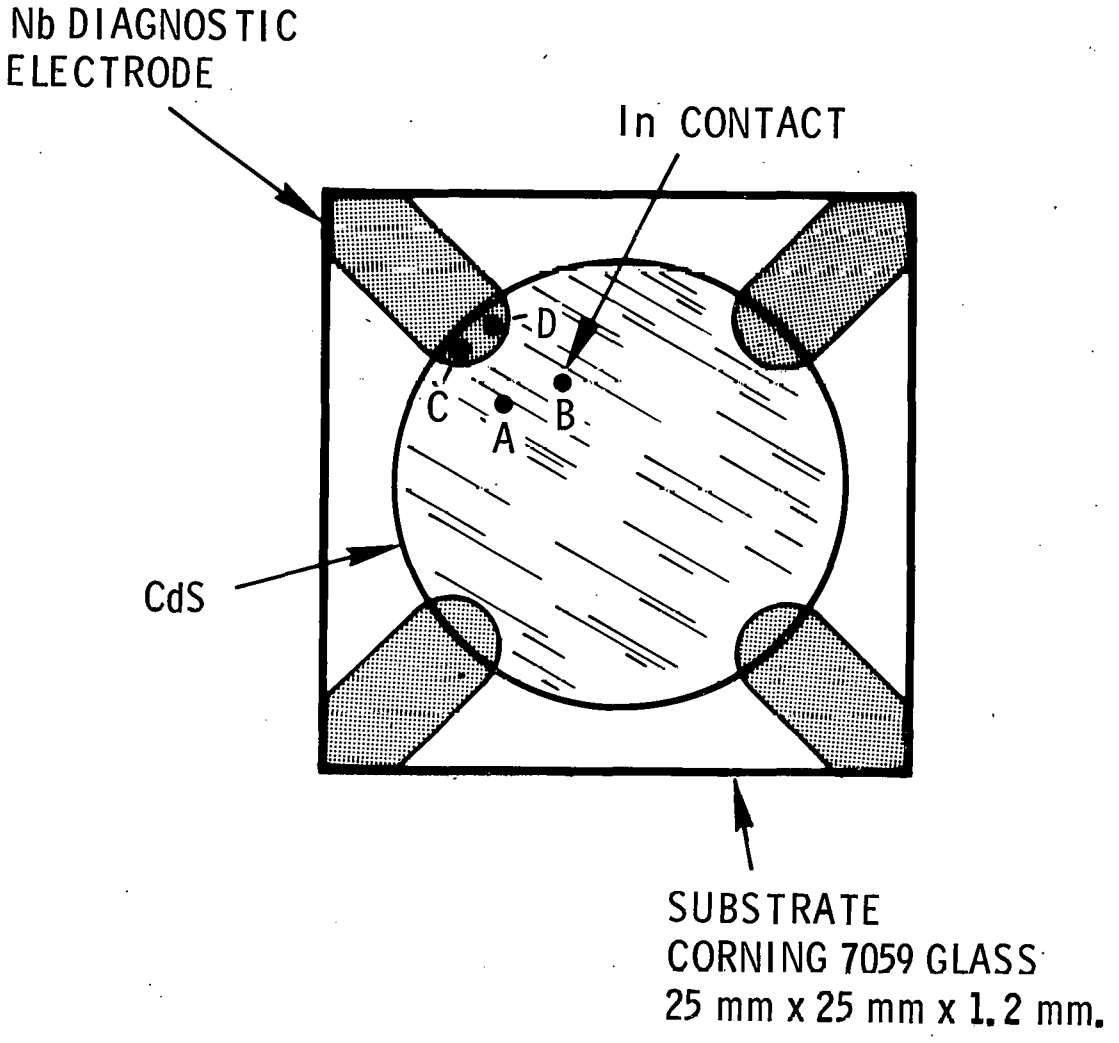

FIG. 5. Diagnostic electrode configuration used for measuring resistivity of semiconducting coatings.

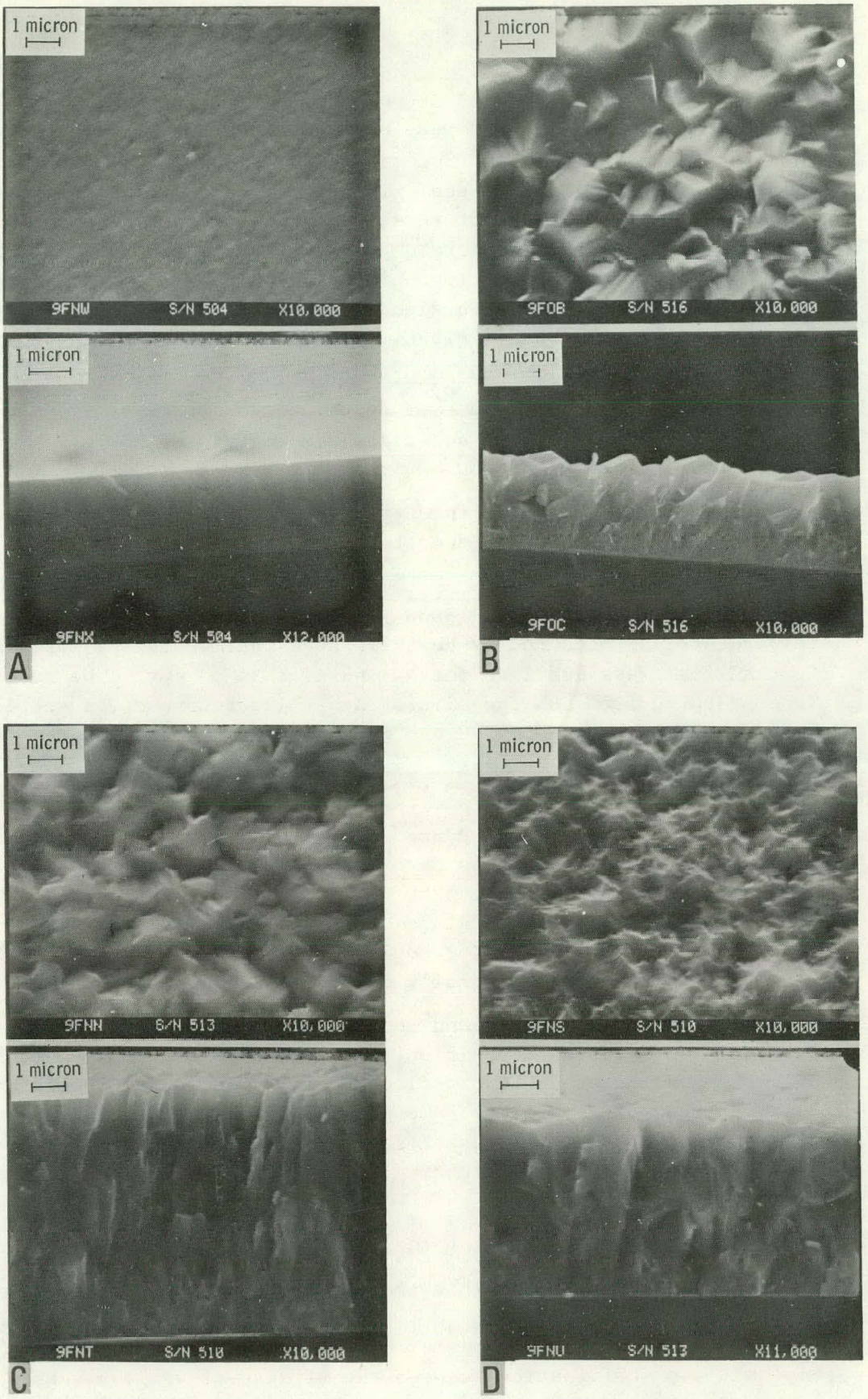

FIG. 6. Scanning electron microscopy photomicrographs showing surface topographies and fracture cross sections of CdS coatings deposited on Nb coated glass substrates by reactive sputtering at various substrate temperatures; A-300°C, B-275°C, C-250°C and D-200°C.

been stored prior to the CdS deposition, exhibited surface hillocks about 2 to 5 μm in diameter growing out of a smooth background of the type shown in Fig. 6A. Such a surface is shown in Figs 7A and 7B. Depressions are also seen. These hillocks are faceted in a nature similar to the structure seen in Fig. 6B, but larger in size. See Figs 7C and 7D. Microprobe analysis showed them to be CdS. They appear to form at inhomogeneities or points of contamination on the substrate. Thus when a poorly rinsed substrate was coated as a test, the hillock distribution formed a pattern which decorated the "water marks".

3) The faceted hillocks of the type described in item 2 above were significantly reduced at a substrate temperature of 250°C. They were virtually absent at 200°C.

4) The density of hillocks of the type described in item 2 appeared to be absent on CdS coatings deposited at 300°C over glass or over Al, Cr, or Mo metallizations.

5) The CdS reactive sputtering deposition rate at a fixed substrate temperature, as measured by the reference thermocouples, was less for Cr than for glass and less for Nb and Al than for Cr. The rates were measured from SEM photomicrographs of fracture cross sections. The data are shown in Fig. 8 and compared with previously reported results.[2]

6) Indium contacts placed on CdS deposited over Nb metallization at 300°C were blocking, while those placed on CdS deposited over adjacent glass regions were ohmic, as described above. However, In contacts placed over CdS deposited at 250°C were ohmic, independent of whether the CdS was deposited over glass or over a Nb metallization. In this case consistent resistivities could be deduced from sets of contacts which passed a current laterally or vertically through the CdS.

7) The Nb metallization was found to make ohmic contact to the CdS over the range of CdS deposition temperatures examined (200 to 300°C). Silver was ohmic at 250°C but blocking at 300°C (possibly because of the formation of a sulfide). Copper formed an interfacial sulfide. Aluminum was blocking (because of oxide), as observed in our previous work.[2] Chromium yielded blocking behavior for In contacts placed over the CdS, as in the Nb case.

Referring to Fig. 8, it seen that the more precise deposition rate data obtained on the present program exhibit the same temperature dependence as those deduced from the work on the previous program.[2] Furthermore, the new data, which permit a discrimination between the effects of various substrate metallizations, bracket the old data, implying that the scatter in the old data

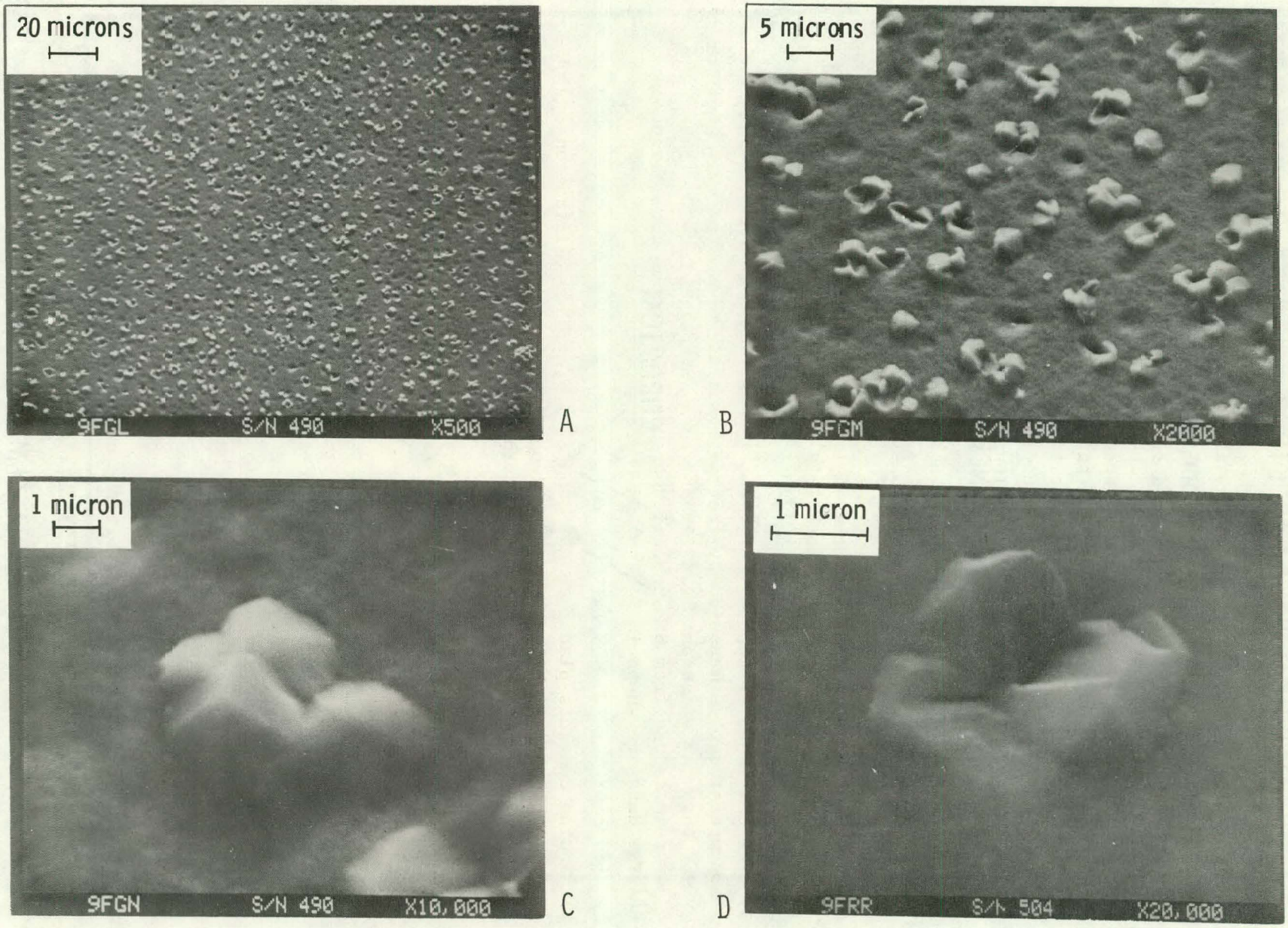

FIG. 7. Scanning electron microscopy photomicrographs showing surface topographies of CdS coatings deposited at a substrate temperature of 300°C on Nb coated glass substrates that had been stored.

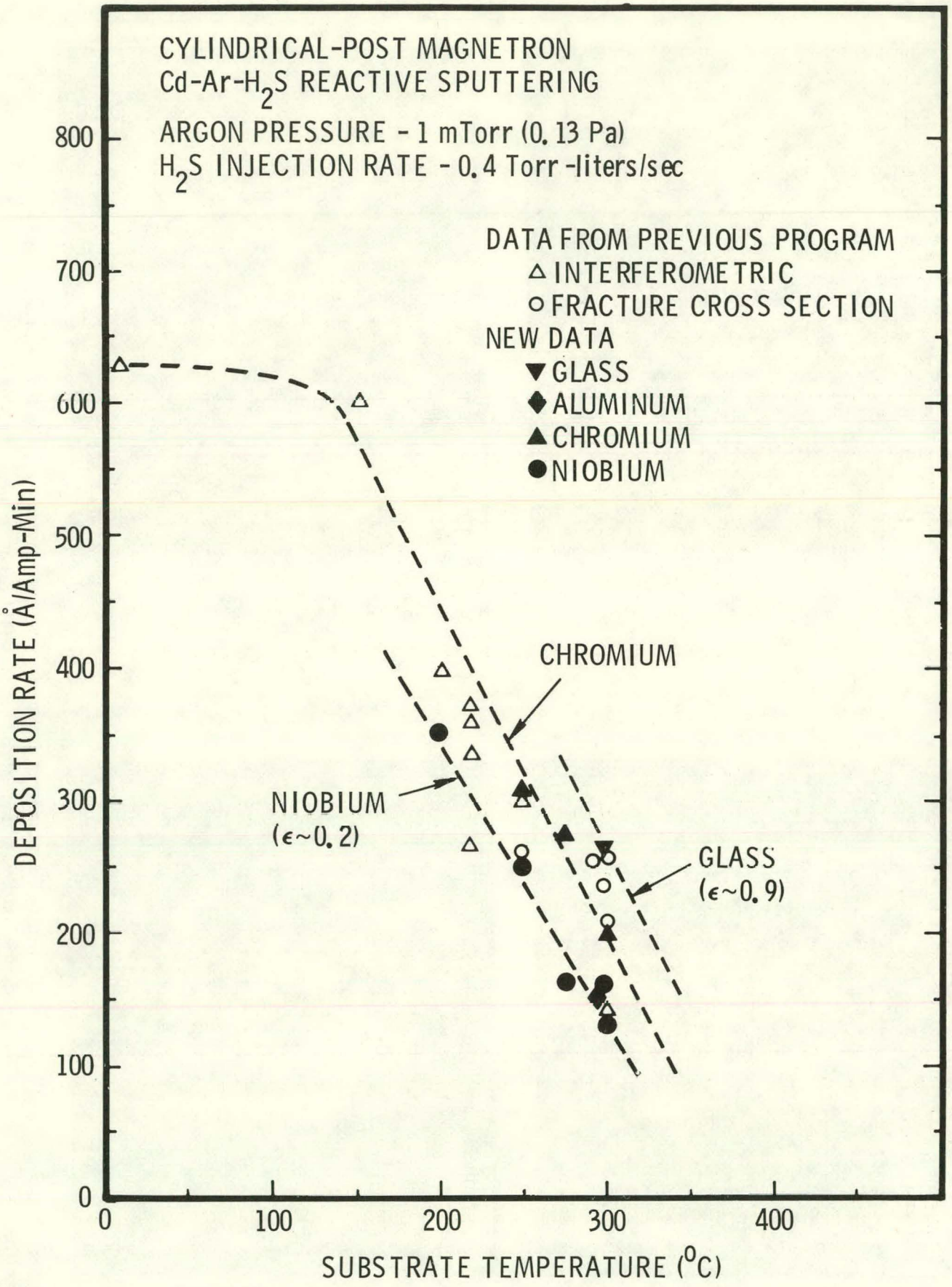

FIG. 8. CdS deposition rate versus substrate temperature (as indicated by reference thermocouples) for glass with various surface metallizations. Comparitive data from previous program[2] is also shown.

was due at least in part to the fact the several substrates were used.

It is believed that the differences in CdS deposition rate for the various substrate metallization materials can be explained by variations in the substrate temperature because of differences in the emissivities of the metallization layers. The substrates are heated by a lamp which is controlled by thermocouples on the reference substrates. The substrate temperature is determined by the rate at which energy is delivered to its rear surface by the lamp and the radiation losses from the front and rear surfaces. A substrate with a low emittance metallization on the front surface will therefore equilibrate at a higher temperature than, for example, would the glass by itself. The data in Fig. 8 are seen to obey this trend. The highest deposition rates are found for glass ($\epsilon \sim 0.9$)[10] and the lowest for Nb ($\epsilon \sim 0.2$)[11] and Al ($\epsilon \sim 0.1$, surface oxidized).[11] The Cr metallization which had become oxidized ($\epsilon \sim 0.4$)[10] yielded an intermediate rate. A simple radiation balance calculation based on a glass emissivity of 0.9 and a Nb emissivity of 0.2 predicts that a glass substrate at 300°C would rise in temperature to 370°C if one surface were metallized with Nb. This is consistent with the data in Fig. 8, where it is seen that the difference in the deposition rates for glass and Nb corresponds to substrate temperature difference of about 60°C. This interpretation was also verified experimentally. Two glass substrates were prepared with thermocouples buried into them by melting the glass. One was metallized with 0.15 μm of Nb. They were mounted on the substrate holder and the heater was adjusted so that the unmetallized substrate was at a temperature of 300°C. The heater current was consistent with that used in the CdS deposition experiments. The thermocouple in the Nb coated sample indicated a temperature of 360°C. Relatively small temperature changes ($\sim$5°C) occurred when CdS was then deposited over the two substrates.

The dense smooth surfaced, CdS deposits shown in Fig. 6A may be related to an effect suggested by Vincett, Barlow and Roberts.[12] They observed that an optimum occurs in the structure-sensitive properties (surface smoothness, crystallographic order, and charge mobility) for many compounds such as CdS

at a substrate temperature of within a few percent of $^1/_3$ T_b, where T_b is the boiling point of the compound (^oK). For CdS this corresponds to a temperature of about 200^{o}C. They suggest that $T/T_b \sim ^1/_3$ is that point at which evaporation from poorly crystallized or amorphous regions becomes significant. Film quality improves up to $^1/_3$ T_b because the existence of such regions decreases. At higher temperatures the more extensive evaporation degrades the film properties.

The procedure in the present program has been to use a substrate temperature of 300^{o}C for depositing the CdS. This temperature had been selected, despite the reduced deposition rate, because the dense film and smooth surface (shown in Fig. 6A) are attractive for fabricating planar junction devices. However, the failure of In contacts to form ohmic contacts on CdS deposited over Nb at 300^{o}C suggests that an electrically active species may be passing from the Nb metallization into the CdS and influencing the CdS surface.[1] Therefore the use of a reduced substrate temperature ($\sim$250^{o}C) is being explored.

The substrate diffusion problem can be expected to be more severe in our work than in typical evaporation studies, because the combination of the high substrate temperature and moderate deposition rate in our case may cause the impurity diffusion rate to exceed the film growth rate.

The possibility of film contamination by the Nb metallization at high substrate temperatures may explain a number of the other observations made on the present program. These include the large and varied series resistance seen in the cells (Section 3), the presence of deep trap levels within the CdS[1], and the apparent failure of the Nb to form an ohmic contact to CdS under some conditions. The latter observation led to use of the thin In layers over the Nb, as discussed in Section 3.

4.2 Resistivity Control by Doping

The formation of reactive sputtered coatings on substrates at elevated temperatures is similar to a three-temperature evaporation process, as described in Section 1. Thus stoichiometric deposits tend to form under a wide range of deposition conditions. This is an advantage as far as process control is con-

cerned, but presents a problem in achieving the desired resistivity. Therefore In doping is being explored. The required doping levels were established by co-deposition studies during the previous program.[2] It was concluded that for a substrate temperature of 300°C, a cathode In concentration of 2 atomic percent was required to provide $Cd_{0.9}Zn_{0.1}S$ with a resistivity of about 30 Ω-cm, and that 1 atomic percent In would provide CdS with a resistivity of about 3 Ω-cm. Deposition from a $Cd_{0.9}Zn_{0.1}$ target containing 2 atomic percent In verified the prediction at least for that material.[2]

The relatively poor efficiency of the In doping in providing electrons to the conduction band is a well recognized behavior in CdS because of the tendency for compensation. It is not a consequence of the specific properties of the sputtering coatings. Recent measurements report doping efficiencies of about 3% for CdS single crystals.[13] Similar results have been reported for evaporated coatings.[14,15]

The objective in the present program is to investigate In doping of CdS in sufficient detail to determine whether the high doping levels required compromise the performance of cells. CdS rather than $Cd_xZn_{1-x}S$ is selected because of the greater available data base on the performance of CdS solar cells. Accordingly, two high purity (99.9999%) sputtering targets were ordered at the beginning of the present program, one containing 1 atomic percent In and the other of pure Cd (for use in nonstoichiometric studies, see Section 4.3).

Progress has been delayed because of two problems with these targets. First, the vendor inadvertently reversed the identifications on the doped and undoped targets, so that a first series of experiments that were conducted, using what was thought to be the In-doped target, were in fact being conducted with the pure Cd target. The problem was not immediately identified because the coatings were deposited with a .05 μm thick In contact layer over the Nb. This layer provided some doping of the relatively thin CdS coatings (~3 μm) and obscured the problem until thicker films, and films without the In layer, were deposited. These films had a high resistivity and were highly photosensitive. The mislabeling was then verified by spectrochemical analysis of samples taken

from the targets. This lack of controlled doping is presumably the cause of the high series resistance that was observed in the Cu_2S/CdS cells fabricated during the first quarter (see Section 3).

The second problem was vacuum leaks through the $^1/_2$-inch thick walls of of the target cylinders because of poor casting procedures. When the misidentification was discovered an attempt was made to resume the doping studies using the true In-doped target. This target was found to have a vacuum leak. A replacement In-doped target was also found to have a leak. A third pure Cd target was discovered by the supplier to have leaks prior to shipment. It is important to note, however, that prior the present difficulties, the supplier had provided targets of pure Cd, $Cd_{0.9}Zn_{0.1}$ with 200 ppm In, $Cd_{0.9}Zn_{0.1}$ with 1 atomic percent In, and pure Zn, all of good quality. The vendor is working on the casting problem and a solution is expected in the near future.

4.3 Resistivity Control by Off-Stoichiometry

There are two potential disadvantages to the use of In doping. The first is the cost of In. The second is the possibility that the In may compromise the performance of the solar cells. Therefore the formation of off-stoichiometric CdS deposits is being investigated. Two approaches are being examined. One is post-deposition annealing in hydrogen. The other is to use special deposition techniques such as pulsed reactive gas injection.

Various groups have reported the successful reduction of the resistivity of CdS by heating in H_2. For example, Mitchell, Farenbruch, and Bube successfully reduced the dark resistivity of 2 μm thick vacuum evaporated CdS films from 10^5 Ω-cm to 0.13 Ω-cm by annealing in H_2S at temperatures up to 400°C for periods of the order of 30 minutes.[16] Even more effective annealing may be possible by using atomic hydrogen. Thus, for example, recent experiments indicate that amorphous-Si can be hydrogenated in the presence of atomic hydrogen but not in molecular hydrogen.[17]

Post-deposition hydrogen annealing experiments are just beginning. The annealing is being done in-situ following the CdS deposition. Results thusfar are inconclusive. However, they do indicate that the use of a glow discharge

to dissociate the H_2 enhances the process. When using such a method, care must be exercised to keep sputtered contaminates from the glow discharge electrodes from reaching the substrates.

In non-stoichiometric CdS it is difficult to decide whether S vacancies or Cd interstitial atoms are the main ionized donor.[18] However, in either case it is important that Cd vacancies not be present in large numbers because of their compensating effect. Any environment which prevents the formation of Cd vacancies can therefore be expected to promote the formation of low resistivity material. In equilibrium terms a high Cd partial pressure is desired. The nature of the Cd-H_2S reactive sputtering process is such that under most operating conditions an energetic flux of reactive gas radicals (S and S-bearing species) is believed to be produced at the cathode and to accompany the sputtering flux to the substrates.[2] The excess S is rejected at the high temperature substrate, and a stoichiometric film results. If the H_2S injection rate is reduced, the excess Cd is rejected, again producing a stoichiometric film. An approach is being investigated whereby the H_2S injection rate is being periodically terminated, thereby permitting the cathode to periodically deliver a very high Cd flux to the substrate surface. The tendency for the Cd to re-evaporate will remain. However, under the correct conditions the equilibrium density of Cd adatoms on the surface of the growing coating may be increased. This work is in its preliminary stages and the results are inconclusive. Figure 9 shows the variation in gas pressure and discharge voltage during such an experiment. The discharge voltage variation reflects changes which occur on the surface of the cathode because of variations in the composition of the working gas.[2]

4.4 Cu_2S Material Studies

During the previous program the electrical and optical properties of thin (0.15 μm) Cu_xS coatings deposited on glass substrates were determined as a function of the deposition conditions.[8] Subsequent work has indicated that the Cu_xS properties are modified when the coatings are deposited over CdS. See discussion in Section 3. Therefore a series of experiments are beginning

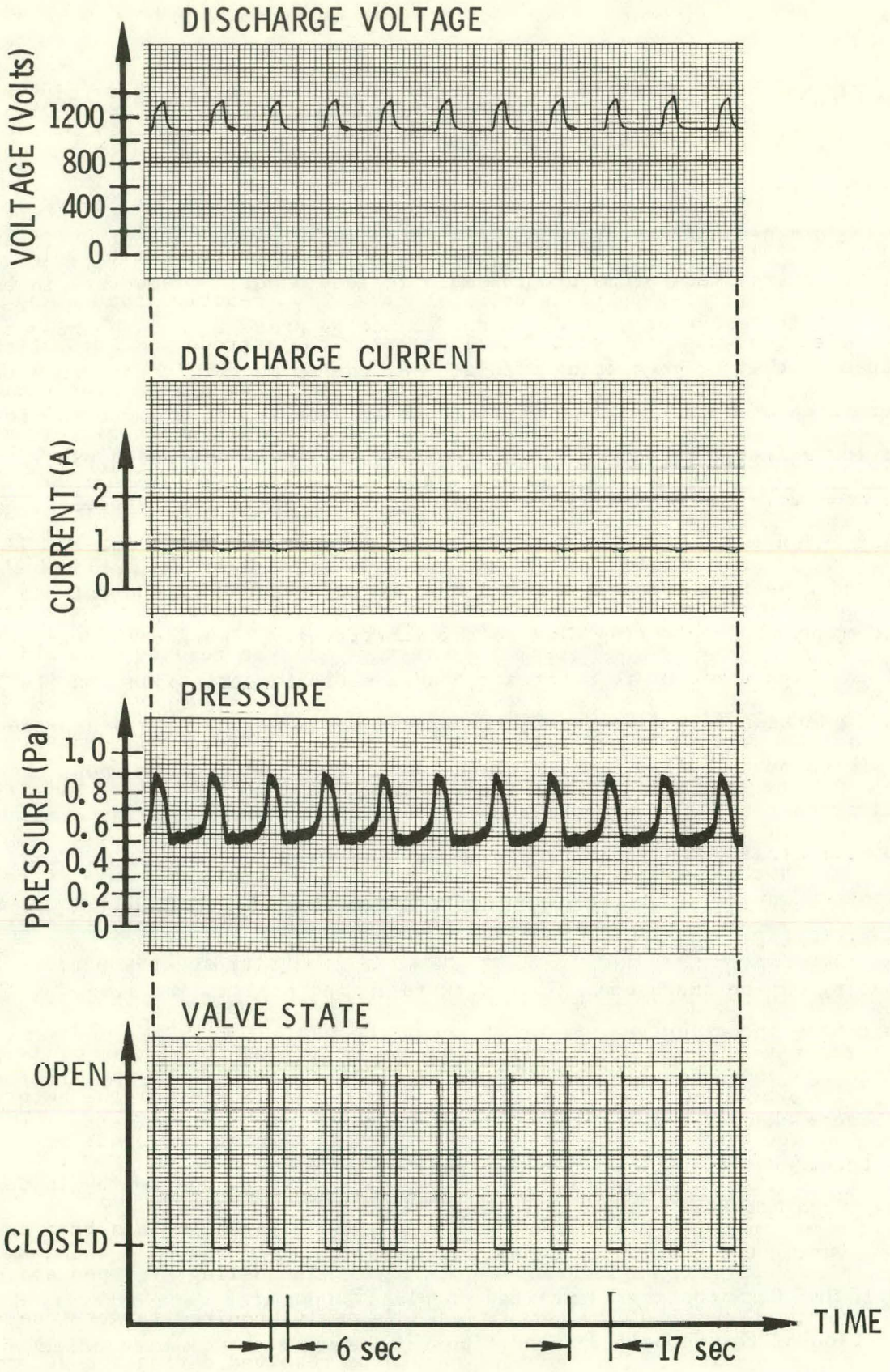

FIG. 9. Temporal variation of working gas pressure and discharge voltage during reactive sputtering of Cd in case where H_2S injection is pulsed. Constant discharge current of 1A.

in which the electrical properties of Cu_xS deposited over thin layers ($\sim 0.3\,\mu m$) of high resistivity of CdS will be determined.

4. SUMMARY STATUS

All-vacuum CdS/Cu_2S and $Cd_xZn_{1-x}S/Cu_2S$ heterojunction solar cells have been fabricated on glass substrates using dc reactive sputtering. The rear electrode was sputtered Nb. The top grid electrode was Au sputter-deposited through a mechanical mask. Preliminary measurements on nonoptimized $Cd_{0.9}Zn_{0.1}S$ Cu_2S cells have yielded efficiencies of 0.4% with short circuit currents of about 3 mA/cm^2, open circuit voltages of about 0.35V, and fill factors of about 0.35.

A modified deposition apparatus is being fabricated which will permit greater control over the process variables, particularly those associated with the Cu_2S deposition. Cell optimization will be resumed when this apparatus is available.

A problem of pin-hole shorts on the Au gridded cells has been traced to poor handling and storage procedures for Nb pre-metallized substrates. Corrective measures are being taken.

The procedure has been to deposit the Cd(Zn)S coatings at relatively high temperatures ($\sim 300^{\circ}C$). Evidence has been obtained which indicates that under these conditions an electrically active impurity species passes from the Nb into the Cd(Zn)S and affects the electrical properties of the Cd(Zn)S. This may explain the high series resistance and poor fill factor of the cells as well as the presence of deep trap levels on the Cd(Zn)S side of the heterojunction. The use of lower deposition temperatures is being explored.

Progress in developing Cd(Zn)S conductivity control by In doping and by off-stoichiometry produced by deposition or annealing has been delayed during this reporting period because of vendor mislabeling of doped and undoped sputtering targets and by vacuum leaks in newly acquired targets due to poor casting procedures. This problem should be resolved during the second quarter and the resistivity control studies will be resumed.

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