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# Design and Experimental Evaluation of a 3rd Generation Addressable CMOS Piezoresistive Stress Sensing Test Chip[1]

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## ABSTRACT

Piezoresistive stress sensing chips have been used extensively for measurement of assembly related die surface stresses. Although many experiments can be performed with resistive structures which are directly bonded, for extensive stress mapping it is necessary to have a large number of sensor cells which can be addressed using CMOS logic circuitry. Our previous test chip, the ATC04, has 100 cells, each approximately 0.012 in. on a side, on a chip with a side dimension of 0.45 in. When a cell resistor is addressed, it is connected to a four terminal measurement bus through CMOS transmission gates. In theory, the gate resistances do not affect the measurement. In practice, there may be subtle effects which appear when very high accuracy is required. At high temperatures, gate leakage can increase to a point at which the resistor measurement becomes inaccurate. For ATC04 this occurred at or above 50°C. Here, we report on the first measurements obtained with a new prototype test chip, the ATC06. This prototype was fabricated in a 0.5 micron feature size silicided CMOS process using the MOSIS prototyping facility. The cell size was approximately 0.004 in. on a side. In order to achieve piezoresistive behavior for the implanted resistors it was necessary to employ a non-standard silicide "blocking" process. The stress sensitivity of both implanted and polysilicon blocked resistors is discussed. Using a new design strategy for the CMOS logic, it was possible to achieve a design in which only 5 signals had to be routed to a cell for addressing vs. 9 for ATC04. With our new design, the resistor under test is more effectively electrically isolated from other resistors on the chip, thereby improving high temperature performance. We present data showing operation up to 140C.

## INTRODUCTION

### Background

The use of piezoresistive stress sensing test chips to measure mechanical stresses in integrated circuit (IC) packaging is now a well established technique. Resistors are produced in single crystal Si by either diffusion or implantation of ions into a thin layer at the Si surface of the wafer. The resistor value depends both on the geometry of the resistor and the sheet resistance of the implanted layer. When mechanical stress is applied to the Si, the resistance changes as a result of both dimensional changes and a sheet resistance or resistivity shift. The fundamentals of piezoresistance in Si have been discussed by Sweet (1993) and detailed equations useful for design have been presented by Bittle, Suhling, Beaty, Jeager, and Johnson (1991). Because single crystal Si is anisotropic, resistors in different crystallographic directions usually respond differently to an applied stress. In addition, the resistor sensitivity to stress changes depends both on the density and the type (p or n) of the implanted dopant atoms. As a result, considerable information may be obtained through the use of different types of strain rosettes on a Si die.

Highly accurate stress measurements can be made with IC die containing only implanted resistors and the necessary metal circuitry to connect these resistors to bond pads on the die. However, this type of circuitry restricts the number of sensing cells which can be placed on the die. For example, in most resistor basic measurement circuits, two connections are required to apply a current *bias* to the resistor under test while two more connections are needed to measure the voltage drop across the resistor. As the number of cells on the die increases, the number of bond pads increases and the on-chip conductor wiring becomes more complex, necessitating the used of multi-level metal to facilitate cross-over circuitry.

In order to make a map of stresses over a die surface it is desirable to have a large number of sensor cells. A reduction in the required amount of chip wiring can be achieved if the cells can be addressed through a common address bus rather than individually wired to bond pads. The first reported chip of this type was presented by Gee, van den Bogert, and Akylas (1988). The subsequent use of this chip to map surface stresses was presented by the same authors (1989). This n-MOS chip had 64 n-type sensor cells or rosettes, each 220 μm on a side, on a square die, 4.5 mm on a side.

An addressable CMOS piezoresistive chip was first discussed by Sweet, Peterson, and Emerson (1994). This chip, designated ATC04, was 5.8 mm on a side and had 25 addressable cells with four n-type and four p-type resistors in each cell, oriented at 0,

[1] Sandia is a multiprogram laboratory operated by Sandia Corporation, a Lockheed Martin Company, for the U. S. Department of Energy under contract DE-AC04-94AL85000.

45, 90, and 135° with respect to a die edge. The cell area occupied by the rosettes was square, about 320 μm (0.012 in.) on a side. Since the chip bond pads were replicated on each side of the die, the ATC04 could be employed in an array format to simulate a larger die. The use of the ATC04 in a 2x2 array format to measure stresses in molded packages has been presented by Sweet, Burchett, Peterson, Hsia and Chen (1997). The measurement of stresses in a flip-chip part has been given by Peterson, Sweet, Burchett, and Hsia (1997). In this work, the cell size is too large to facilitate fine spatial resolution of stress variations produced by the attachment solder balls. The solder ball pitch was 0.010 in., about the size of an individual cell.

## Design Goals

**Reduction in cell size** The first major goal was the reduction in cell size. This could be realized either by redesigning the cell to have a smaller net area or by using a semiconductor technology with a smaller minimum feature size. The minimum feature size of the ATC04 chip was 2 μm and mature CMOS technologies available now have minimum feature sizes in the range 0.35-0.5 μm.

**Use of standard CMOS processing** In many ways, basic digital CMOS technology is not optimum for making piezoresistive test chips. The only standard resistors available are either the heavily doped source-drain implant resistors or the heavily doped polysilicon which is used to make MOS transistor gates. The source and drain implants result in very high surface doping, $\gtrsim 10^{19}$ carriers/cm$^3$. At such high doping levels, the piezoresistive coupling coefficients are small in magnitude although the temperature dependence of these coeffients is also small, a desirable feature. In addition, using (100) Si wafers limits the number of stress tensor components which can be measured.

In spite of the above limitations, use of standard CMOS processing enables the fabrication of the test chips on a standard wafer fabrication line and also enables prototyping via the MOSIS facility (1998). We feel that these advantages overcome the limitations inherent in using (100) Si and highly doped resistors.

**Improved resistor isolation to facilitate high temperature measurements** An implanted resistor in a Si die is isolated from the rest of the circuitry on the die by a reversed biased distributed p-n junction at the resistor to well boundary, where the well is the lightly doped Si region into which the resistor dopant is implanted. As the temperature increases, the junction leakage current also increases. If the leakage current becomes an appreciable fraction of the resistor measurement current, then the resistor measurement becomes erroneous.

On the ATC04 chip, the cell being addressed is connected to an output measurement bus through CMOS transmission gates, a type of logic gate which either blocks current flow by turning transistors in series with the resistor under test off or enables flow by turning these transistors on. These gates can also leak at high temperature and produce measurement errors. In ATC04 the maximum measurement temperature which could be achieved without excessive leakage errors was $\lesssim 50$°C. In order to measure mold compound curing stresses, we wanted to extend the high temperature limit to 150°C.

**Capability of placing cell below top level metal features** The ATC04 chip was built in a technology with two levels of Al conductor metal. Due to the cell complexity, both levels were required to wire the test resistors and associated logic circuitry. As a result, there was no ability to place metal structures over the sensor cells.

With newer CMOS technologies, there are three or more metal layers available to the designer. As a result, we wanted to be able to place bond pads directly over cells to measure the stresses produced by the wire bond process.

**Intermediate taps on resistors to enable smaller value resistors** The nominal value of the piezoresistors in the ATC04 cells was in the range 8 – 10 kΩ. Values in this range resulted in maximizing the change in resistor voltage produced by stress while simultaneously maintaining the resistor voltage drop below the magnitude of the power supply voltage, $V_{DD}$. All of our measurements in the past have been made at or near room temperature and hence electrical Johnson or white noise has not been too much of a problem. However, for measurements at high temperatures we felt that lower resistance values might be desirable. In a recent experiment reported by Palmer, Benson, Peterson, and Sweet (1998), an ATC04 test chip was instrumented in a mold press and stress measurements were made during the transfer molding porcess at temperatures $\approx 175$°C. In these measurements, noise was a problem and we hoped to improve the measurement by using lower value resistors.

In the new design we wanted to include resistor "taps" or intermediate connection points so that low value resistors could be used, if desired. A major goal was to accomplish this without increasing the cell size.

**Common layout for all cells** The layout of the ATC04 die was done by mirroring a basic cell which included the 4 n-type and 4 p-type resistors, a diode, and local resistor addressing circuitry. This scheme minimized layout work and resulted in the addressing circuitry always being on the same side of a cell. In theory, this mirroring should not have introduced any observable difference. However, if there are small but systematic errors in the resistor geometries introduced by this mirroring, then nearby mirrored cells may not produce the same resistance changes for a given applied stress. Some of our data using a "quad" or 2x2 die array showed this type of behavior for sensors adjacent to the die centerline.

In our new design we wanted all cells to have the same orientation. As a result we would be required to move the addressing circuitry around to facilitate cell interconnect.

## SI (100) STRESS SENSOR CELL DESIGN

### Cell Fundamentals

The fundamentals of piezoresistive stress sensor cell design in (100) Si have been presented by Jaeger, Suhling, and Ramani (1994). Here we review the basic cell design concepts and compare them with the design we have used in ATC04. A fundamental four resistor stress sensor cell layout is shown in Fig. 1 and an SEM micrograph of two adjacent ATC04 stress sensor cells is shown in Fig. 2.

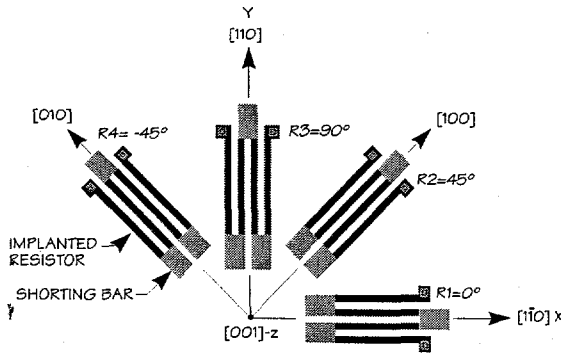



**Fig. 1 Resistor layout in a stress sensor cell on (100) Si. The chip edges are in the x=[1$\bar{1}$0] and y=[110] directions and the chip diagonals are in the <100> directions.**

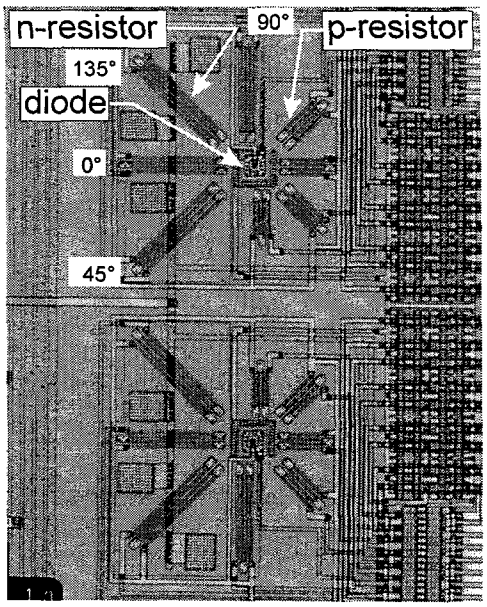



**Fig. 2 SEM micrograph of two sensor cells showing the resistor layout and some of the cell and resistor addressing circuitry. At the center of each resistor rosette there is a diode used for cell thermometry.**

We number the resistors sequentially, 1-4, starting with the resistor directed along the x axis. We note that Jaeger et. al (1994) number the cell resistors differently (See their Fig. 7). They label the 0 and 90° resistors 1 and 2 and the 45 and 135° resistors 3 and 4, respectively.In the natural coordinate system associated with the cell shown in Fig. 1, the diagonal stress tensor components $\sigma_{xx}$ and $\sigma_{yy}$ are directed along the chip x and y axes and $\sigma_{zz}$ is directed vertically or in the [001] direction. In most cases of interest in electronic packaging, $\sigma_{zz}$ is small in magnitude except possibly very near the chip perimeter.

Although the Si implanted resistors have an appreciable stress dependence, they also have a very strong temperature dependence. If an initial measurement is made at some initial stress level, $\vec{\sigma}_1$, and temperature, $T_1$, and a final measurement made at a new stress tensor level, $\vec{\sigma}_2$, and temperature, $T_2$, then part of the change in resistance between final state 2 and initial state 1, $\Delta R_i = R_{i2} - R_{i1}$, for the $i^{th}$ resistor is produced by the stress change $\Delta\vec{\sigma} = \vec{\sigma}_1 - \vec{\sigma}_2$ and part is due to the temperature change, $\Delta T = T_1 - T_2$.

It can be shown that all stress data depend on the $\Delta R$ values for a given resistor type only through the sum S(+) or difference D(-) of the relative resistor shifts of two resistors oriented 90° apart. These quantities, designated $\delta R_{ij}^{S,D}$, where i and j are 1 and 3 (0°, 90°) or 2 and 4(45°, 135°), are given by,

$$\delta R_{ij}^{S,D} = \left( \frac{\Delta R_i}{R_{i1}} \pm \frac{\Delta R_j}{R_{j1}} \right) \qquad (1)$$

In the case of $\delta R^D$, any shift in resistance values produced by the temperature shift $\Delta T$ between initial and final measurements cancels out. Thus stresses which depend only on a $\delta R^D$ value are intrinsically temperature compensated in that they do not require a correction for the temperature shift. In the case of stresses which depend on $\delta R^S$ values, a correction term, $2\alpha\Delta T$ is required, where $\alpha$ is the relative temperature coefficient of resistivity for the given resistor type, the fractional change in resistance per unit temperature change at constant external stress.

Jaeger et. al(1994) show that temperature insensitive or "compensated" measurements can be made of the in-plane shear stress, $\sigma_{xy}$, and the difference of the in-plane diagonal components, $\sigma_{xx} - \sigma_{yy}$. Through a consideration of the magnitudes of the piezoresistive coupling coefficients, the authors suggest that an "optimal" cell for making temperature compensated measurements in (100) Si would use diagonal (45-135° or 2-4) n-type resistors to determine $\sigma_{xy}$ and horizontal-vertical (0-90° or 1-3) p-type resistors to determine $\sigma_{xx} - \sigma_{yy}$. Hence, a cell to determine just these quantities could be made with only four resistors, thus reducing the cell size somewhat from the eight resistor cell shown in Fig. 2. A recent example of the use of cells of this type is given by Zou, Suhling, and Jaeger (1998).

The temperature compensated quantities which may be derived from $\delta R^D$ measurements, the in-plane shearing stress $\sigma_{xy}$ and the difference of in-plane compressive stresses, $\sigma_{xx}$-$\sigma_{yy}$, are

given by,

$$\sigma_{xy} = \frac{\delta R_{24}^{D}}{2\pi_{D}}, \qquad (2)$$

and,

$$\sigma_{xx} - \sigma_{yy} = \frac{\delta R_{13}^{D}}{\pi_{44}}. \qquad (3)$$

The quantity $\pi_D$ in Eq.(3) is given by $\pi_D = \pi_{11} - \pi_{12}$, where $\pi_{11}$, $\pi_{12}$, and $\pi_{44}$ are the fundamental coupling constants or "pi" coefficients which relate stress changes to resistance shifts. $\pi_D$ has a large magnitude only for the n-type resistors, so the diagonal or 2-4 n-type resistor data are used to derive $\sigma_{XY}$. In the case of $\sigma_{XX}$-$\sigma_{YY}$, $\pi_{44}$ for the p-type resistors has about five times the magnitude of the n-type $\pi_{44}$, so the p-type data are used to derive the in-plane compressive stress difference from Eq. (3).

A relation for a linear combination of $s_{XX}$ and $s_{ZZ}$ may be derived but it requires use of temperature compensation. The relation, from Sweet et. al, (1997) is,

$$\sigma_{xx} + (\pi_{12}/\pi_{S})\sigma_{zz} = \frac{\left(\delta R_{24}^{S} - 2\alpha\Delta T\right)}{2\pi_{S}} + \frac{\delta R_{13}^{D}}{2\pi_{44}}, \qquad (4)$$

where $\pi_S = \pi_{11} + \pi_{12}$. Since the magnitude of the quantity, $(\pi_{12}/\pi_S)\sigma_{ZZ}$ is small relative to the magnitude of $\sigma_{xx}$ except very near the die edges, Eq. (4) essentially gives the value of $\sigma_{xx}$.

## ATC04 cell design

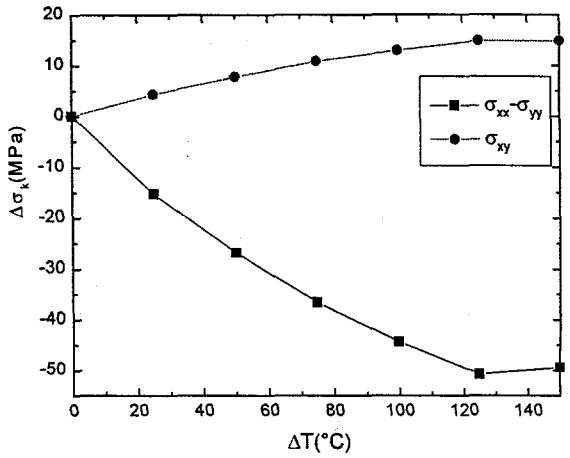
If the temperature variation, $\Delta T$, can be measured and the dependence of resistance on temperature in a "stress-free" environment is known, then the variation in resistance caused by temperature can be removed and the residual $\Delta R$, presumably, is due only to the stress variation. In ATC04 we accomplish this by measuring temperature with a diode, centered in the cell. In this way, we determine a quantity, $\sigma_{XX} + k\sigma_{ZZ}$, where k is related to the piezoresistive coefficients, as discussed by Sweet et. al, (1997). Since $k \approx 1.2$, the quantity $k\sigma_{ZZ}$ is usually small in magnitude compared to $\sigma_{XX}$.

We feel that the ATC04 design provides certain advantages if it can be implemented in a suitably small size. Considering first the p-resistor rosette, as discussed above we determine $\sigma_{XX} - \sigma_{YY}$ from the p-type $R_1$ and $R_3$ resistors. The diagonal p-type resistors are very insensitive to stress variations and hence they can be used as resistance thermometers. In the use of ATC04, we examine the temperature variation as measured both with the diode and the 2-4 p-type resistors. To consider a measurement with a $\Delta T$ between initial and final states valid, we require that both types of thermometry produce essentially the same result.

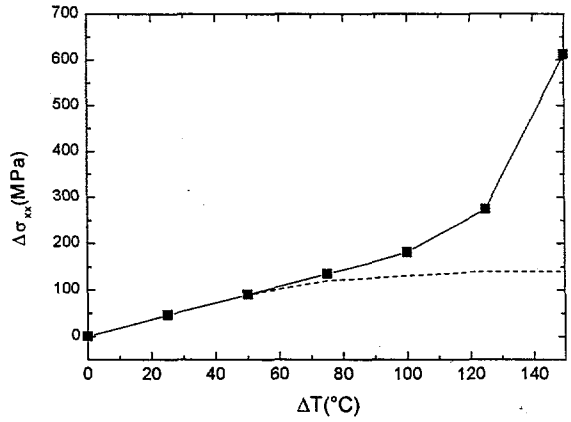
In the case of the n-type resistors, the quantity $\sigma_{XX} + k\sigma_{ZZ}$ can be found from either the 1-3 or the 2-4 resistor pairs. As discussed by Sweet et. al (1997), the sum of the variations of the 1-3 resistor pair should be theoretically equal to the sum of the variation of the 2-4 pair. As a result, the proper functioning of a cell can be judged by how well this equality is satisfied. In measurements with ATC04 we frequently observe a difference ~ 15% between the two quantities. This difference is not understood.

## ATC04 MEASUREMENTS

### Encapsulation Stresses




(a)




(b)

**Fig. 3 Measured stress changes from the ATC04 thermal stress measurement experiment. (a) Shearing stress, $\Delta\sigma_k=\sigma_{xy}$ and compressive stress difference, $\Delta\sigma_k=\sigma_{xx}-\sigma_{yy}$, functions. These measured quantities are temperature compensated and do not require an explicit temperature correction. (b) $\Delta\sigma_{xx}$ for the same part. The solid line and points are the measured data. The dashed line represents the expected variation of $\Delta\sigma_{xx}$ vs. Temperature.**

In an initial thermal stress measurement we used a liquid encapsulated DIP with a single ATC04 die, as described in Sweet et. al (1995). The part was placed in an oven and the temperature was varied over the range 25 - 175°C. The chip diode measured temperature at steady state agreed well with the oven temperature as measured by thermocouple. At each temperature hold point, the stress tensor components were measured with reference to the ambient, $T_1 \approx 25°C$. The measured stress component shifts or changes as a function of $\Delta T = T - T_1$ are shown in Fig. 3.

The shearing stress change is shown in Fig. 3(a) for a corner cell, a location where the amplitude of $\sigma_{xy}$ is a maximum. The stress difference $\sigma_{xx}$-$\sigma_{yy}$ is shown in Fig. 3(a) for a cell near the midpoint of a die edge where it has a maximum amplitude and the compressive stress $\sigma_{xx}$ is shown for a cell in the die center in Fig. 3(b). Since both of the measured quantities in Fig. 3(a) are intrinsically temperature compensated, any temperature induced shift in one resistor value is presumably matched by the same shift in the other resistor, leaving only stress induced shifts to produce a difference in the $\Delta R/R$ values for the two resistors used to calculate the stress component. From the data in Fig. 3(a) it can be seen that both $\Delta\sigma_{xy}$ and $\Delta(\sigma_{xx}-\sigma_{yy})$ achieve a constant magnitude at $\Delta T \approx 125°C$. This corresponds to a temperature $T \approx 150°C$ which is near the glass transition temperature, $T_g$, for the encapsulant. At $T_g$ the encapsulant enters a rubbery state and presumably communicates little or no stress to the die. Further heating to 175°C produces little stress, presumably because the epoxy die attach is also in a rubbery state.

In contrast to this behavior, the uncompensated $\sigma_{xx}$ in Fig. 3(b) continues to increase and at a more rapid rate as the temperature becomes higher. The dashed line in Fig. 3(b) shows the expected variation in $\sigma_{xx}$. These $\sigma_{xx}$ data suggest that the ATC04 temperature compensation is not working correctly. Examination of the primary resistance data showed that the resistance values actually start to decrease with temperature at the higher $\Delta T$ values, indicating that there is a source of extra resistance in parallel with the resistor under test(RUT). This parallel resistance appears to decrease with increasing temperature, with the result that the resistance of the RUT eventually becomes dominated by the extraneous resistance.

## Resistor Leakage Measurements

The ATC04 wafer has a number of test structures which are used for process monitoring and various test functions. One of these structures is a test piezoresistance cell in which the resistors and associated well bias connections can be directly bonded, facilitating the measurement of leakage currents for a single resistor with no other attached components. The results of such a measurement for a p-type implanted resistor are shown in Fig. 4 as a function of temperature with the reverse bias voltage VR as a parameter.

The data from Fig. 4, along with similar measurement data for the *n*-type piezoresistor were used to develop model parameters for the SPICE circuit modeling program. An Excel spreadsheet was used to develop model parameters that brought the simulation into convergence with the measured values of the p and n-type diodes over the temperature range using a multivariable variation method.

A detailed SPICE circuit simulation model was then developed to test the leakage current hypothesis. This model simulated the combined effects of 50 *p*-type and 50 *n*-type reversed biased junctions in a single ATC04 test chip during stress measurement. A schematic diagram of an implanted resistor is shown in Fig. 5. The resistor transverse current $i_r$ flows laterally between the resistor metal contacts. The distributed resistor leakage current $i_\ell$ flows across the reverse bias resistor-well depletion region. The measurement current $i_t$ is related to the other currents by $i_t = i_r + i_\ell$.

The distributed leakage currents shown in Fig. 5 were simulated by five diodes for each resistor. Using the derived SPICE parameters for these diodes, we verified in a semiquantitative way that the leakage current model could account for the observed variation of implanted resistor value vs. temperature. From this result, we determined that one resistor with its associated well leakage current would work well over the temperature range of interest and that the relatively simple design change of adding additional transmission gates to the common side of each resistor would serve to isolate the RUT from other resistors on the chip. Although there is still leakage to the well of the RUT at high temperature, the resistor-well surface area for one resistor is not large enough to cause a measurement error, at least in the temperature regime in which we are interested.

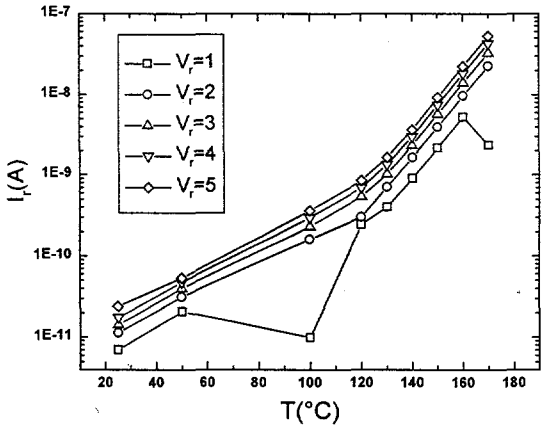



**Fig. 4. Measured reverse bias leakage current from single *p*-type piezoresistor in a test structure as a function of temperature with well to substrate reverse bias voltage VR as a parameter. In normal operation, VR= -5 V.**

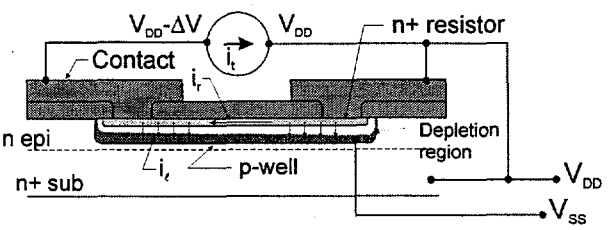



**Fig. 5 Schematic diagram of an n+ implanted resistor in a p-type well. The resistor transverse or through current is $i_r$ and the distributed leakage current is represented by $i_\ell$.**

## NEW CHIP, ATC06 DESIGN

### Design Overview

The experimental ATC06 stress sensing chip was designed and fabricated in Hewlett Packard's 0.5 μm CMOS14TB process, using MOSIS scalable SCMOS design rules. This process is a three level metal 0.5 μm feature *silicided*-process. Modern CMOS ICs with small feature size utilize a silicide process over the n+ and p+ source and drain ion implanted regions in order to reduce the sheet resistance of these regions.

In one variant of this process, as described by Wolfe (1990), a thin layer of Ti and a layer of amorphous Si are sputter deposited onto the wafer after the source drain implantation. The amorphous Si is patterned using a photolithography-etch process and then a 600°C anneal is performed to react Ti and Si into $TiSi_2$ in regions where Ti is in contact with Si, poly-Si or deposited amorphous Si. This results in lower sheet resistance in the source-drain implanted regions and in the poly-Si transistor gates. Unfortunately, the piezoresistive effect depends on the single crystal properties of Si and these will be perturbed by an overlying silicide layer. In our design we used a non-standard silicide blocking mask step to prevent formation of the silicide over the piezoresistors in some of the cells. An important secondary goal of this work was to verify that this process step would work. In addition, we wanted to directly compare the stress sensitivity of rosettes fabricated with and without silicide blocking.

The ATC6.0 chip MOSIS chip is ≈ 2.5mm on a side. It contains a total of addressable eighteen and four independent stress sensor cells, as shown Fig. 6. Each implanted stress cell is a rosette consisting eight separate resistors; four $n^+$ and four $p^+$, a diode for temperature monitoring, and address and gating circuitry. The layout of one cell is shown in Fig. 7. In the case of polysilicon resistor cells, all resistors were sized equally. Also on-chip are three ring oscillators, each using different metal interlinks between inverter stages. Bond pads have been located directly over a few of the stress rosettes, giving the potential for measuring stress during the bonding process. Two stress cells have been placed the extreme corners of the die for comparison of stresses from center to edge.

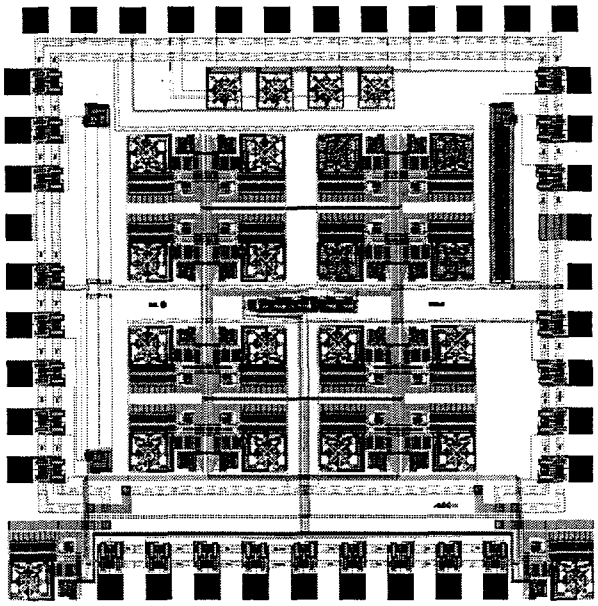


**Fig. 6 Layout of the ATC06 stress sensing evaluation test chip. The chip is ≈ 2.5 mm on a side. At the bottom corners, the two corner located stress sensor cells can be seen. Not shown are the bond pads located over the four stress cells in the upper right hand quadrant. The four cells at the top can be measured without addressing and are used for calibration.**

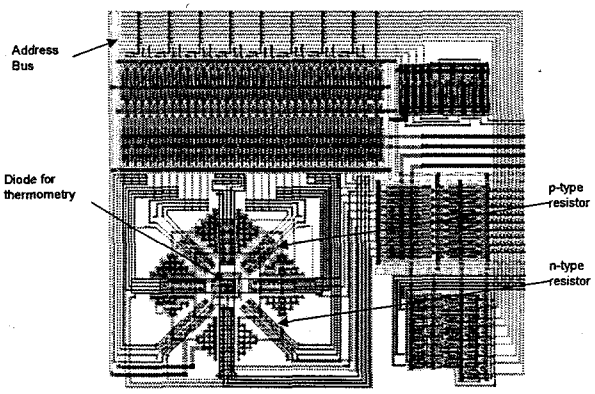



**Fig. 7 Stress sensor cell showing the piezoresistors, centrally located diode, and CMOS logic circuitry for addressing and data readout. The four short resistors are p-type and the four long resistors n-type.**

In addition, there is a test strip of directly measurable piezoresistive cells containing all the types of resistors available in process: 1. Silicided p+, n+ implant, 2. Non-silicided n+, p+ implant, 3. Non-silicided polysilicon, 4. silicided polysilicon.

A micrograph of one stress sensor cell is shown in Fig. 8. Visible in this micrograph are the three levels of metal interconnect used to "wire" the chip. Metal lines from the lowest level, metal 1, run directly over the implanted resistors.

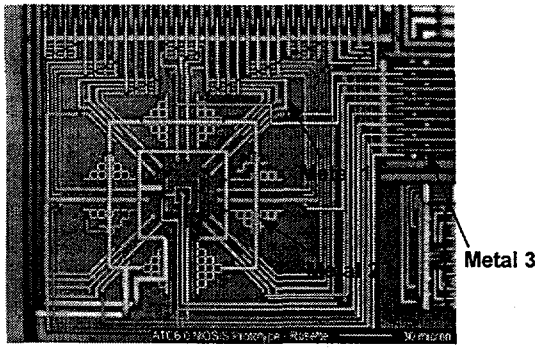



**Fig. 8 Micrograph of an ATC06 piezoresistor cell showing three levels of metal. The level closest to the Si is metal 1 and the top level is metal 3. Metal 1 lines run over the implanted piezoresistors.**

## EXPERIMENTAL MEASUREMENTS WITH ATC06

### Resistance vs. Temperature

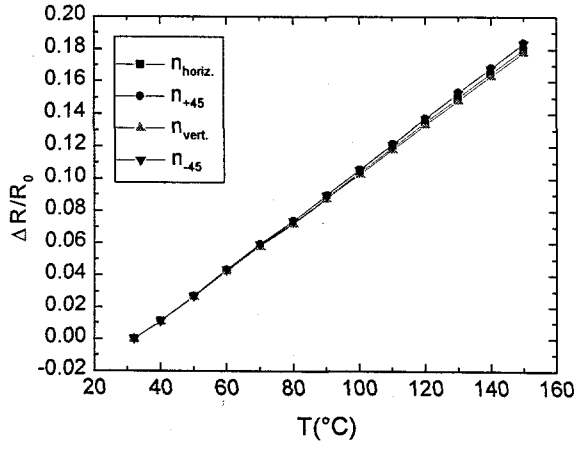



**Fig. 9 Temperature dependent average fractional change in resistance of the n-type resistors from 6 ATC06 cells with blocked resistors.**

In order to see if the high temperature leakage current problem had been solved we measured the resistance of all resistors in all cells on a die as a function of temperature. In this measurement, we set the input bits for the resistor taps to select the full value of the resistors. The results for blocked n-type resistors in six cells are shown in Fig. 9. These data show that the resistance change with temperature is quite linear over the range 30-150°C. Hence the cell should be suitable for measurement of thermal stresses over the required temperature range.

### Resistance vs. Load

In a normal piezoresistive chip calibration experiment, a strip of die is cut from a wafer and one of the die is wire bonded to an adjacent pin structure, as described by Sweet et. al (1994). The strip is then loaded in a four-point bending structure, producing a uniaxial stress in the strip at the test die location. The resistors are then measured as the load is varied to derive the stress sensitivity. If the parts are fabricated by the Mosis facility, only individual die are available and a four-point bending calibration cannot be performed. In this case, we use a single point bending method in which the chip is epoxy bonded to a 40 pin ceramic chip carrier. Use of this technique with the ATC04 die has been discussed by Sweet et. al (1994). The substrate is supported at both ends by a holder and the load is applied by a single knife edge on the backside, as shown in Fig. 10.

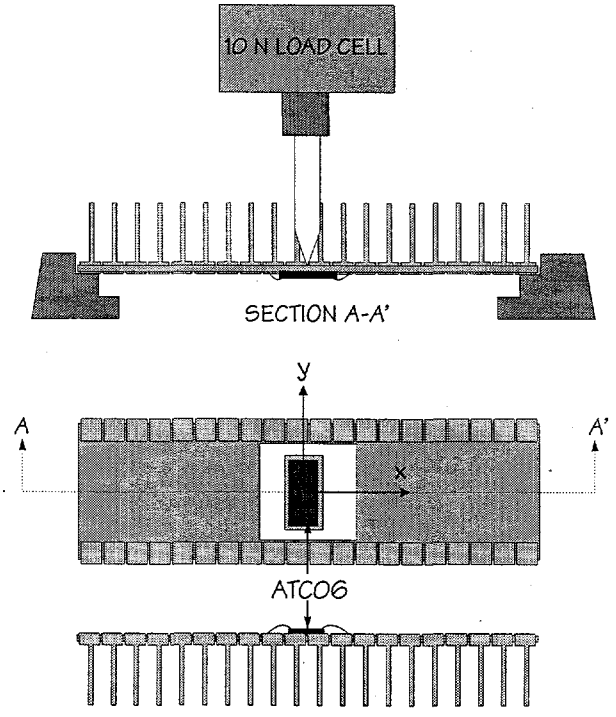



**Fig. 10 Experimental setup for the single point bending experiment using a die epoxy bonded to a ceramic substrate.**

When the load is applied, the surface of the die is placed in a state of tension, with the stress being approximately uniaxial at

the die center. However, two effects can produce a more complex state of stress. The die may become misaligned to the substrate during the epoxy die attach and cure process. This misalignment, usually several degrees, results in the development of in-plane shearing stress, $\sigma_{xy}$, at the die center, with a magnitude proportional to the angular misalignment. Additionally, the substrate may become misaligned in the bending fixture, resulting in a biaxial stress state at the die center.

Although we did not know the values of the piezoresistive coefficients to use in Eqs. (1)-(4) for data reduction, we could estimate that their magnitudes were approximately the same as those in the ATC04 chip, since both used heavy or degenerately doped implantations for the source-drain regions. The results from the bending experiments for both types of die with a 10 N force applied are shown in Table 1. The stress components and the equations from which they are derived are shown in the top row. The first row of data are from the center cell of an ATC04, part, using our most recent estimates for the values of the $\pi$ coefficients for data reduction. The row marked "ATC06 open" is for an open cell with blocked resistors located near the die center. The row marked "ATC06 under bond pad" is for a cell with blocked resistors under a top level metal bond pad. In both cases, ATC04 derived $\pi$ coefficients were used for data reduction. It is evident that there is quite close agreement between the results for the two different chips, In addition, the presence of a bond pad over a cell in ATC06 does not appear to perturb the stresses significantly.

**Table 1 Stress measurement results for a center located sensor cell in single point bending. The ATC04 measurements are from Sweet et. al (1994), with a minor correction for improved $\pi$ coefficient data. The ATC06 measurements are from this work.**

| Stress Comp. → Die/Loc. ↓ | $\sigma_{xx}$ (MPa) Eq.(4) | $\sigma_{yy}$* (MPa) (4)-(3) | $\sigma_{xx}$-$\sigma_{yy}$ (MPa) Eq.(3) | $\sigma_{xy}$ (MPa) Eq.(2) |
|---|---|---|---|---|
| ATC04 center | 25.8 | 0.3 | 25.5 | -2.7 |
| ATC06 open | 27.5 | 4.0 | 23.5 | 2.3 |
| ATC06 under bond pad | 26.5 | 2.2 | 24.26 | 2.0 |

In Table 1 the $\sigma_{yy}$ results are derived from the measured $\sigma_{xx}$ and $\sigma_{xx}$-$\sigma_{yy}$ data.

### Stress response of Unblocked and Polysilicon Resistors

Both Si and poly-Si unblocked resistors with a silicide overcoat showed little or no stress sensitivity, as predicted. The silicide layer effectively shorts out the piezoresistance. The unblocked poly-Si resistors demonstrated appreciable stress sensitivity. Both the longitudinal and transverse piezoresistive coefficients were negative, with the transverse coefficient having the larger magnitude.

## CONCLUSIONS

We have demonstrated an addressable CMOS piezoresistive test chip fabricated in a MOSIS 0.5 μm three level metal technology. With the source-drain silicide layer blocked, the resulting implanted p and n-type resistors showed a stress sensitivity much like our previous chip, the ATC04 fabricated in the Sandia Microelectronics Development Laboratory in a 1.25 μm CMOS process. The new rosette size in the cell size was approximately 110 μm on a side, just slightly larger than a standard bond pad.

We demonstrated a sensor cell under a top level metal bond pad and showed that the sensitivity of this cell was similar to that of an open or uncovered cell. This type of cell should be useful for measuring die stresses produced by wire bonding.

The junction leakage problem at high temperatures was much reduced relative to the ATC04 case. The observed resistance variation with temperature for blocked implanted resistors was quite linear over the temperature range 25-150°C.

We feel that the basic ATC06 design, as demonstrated in the MOSIS chip described in this paper would be suitable for scaling up to larger chip sizes with a larger number of stress sensor cells. Design work to do this is currently in progress.

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