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RAD-HARD ELECTRONICS STUDY FOR SSC DETECTORS

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ABSTRACT

The radiation environment in a SSC detector operating at a luminosity of 10^{33} $cm^{-2}s^{-1}$ will put stringent requirements on radiation hardness of the electronics. Over the expected 10 year life-time of a large detector, ionizing radiation doses of up to 20 MRad and neutron fluences of 10^{16} neutrons/cm^2 are projected. At a luminosity of 10^{34} $cm^{-2}s^{-1}$ even higher total doses are expected. The effect of this environment have been simulated by exposing CMOS/bulk and CMOS/SOS devices from monolithic processes to neutrons and ionizing radiation. Leakage currents, noise variations, and DC characteristics have been measured before and after exposure in order to evaluate the effects of the irradiations. As expected the device characteristics remained virtually unchanged by neutron irradiation, while ionizing radiation caused moderate degradation of performance.

INTRODUCTION

At a luminosity of 10^{33} $cm^{-2}s^{-1}$ the total dose inside a SSC detector during its projected ten year life-time can be as high as 20 MRad of ionizing radiation and 10^{16} neutrons/cm^2. A change in luminosity to 10^{34} $cm^{-2}s^{-1}$ will further increase the dose. Radiation damage is strongly dependent on detector geometry and distance from interaction point [1]. The dependence of the dose on distance from interaction region and pseudo-rapidity in a SSC detector [4] is shown in Fig. 1.

The read-out electronics is one of the most radiation-sensitive systems of a detector. Response time and number of channels dictate that the electronics for many detector elements must be placed closed to the interaction point (such as the silicon tracking system and liquid argon calorimeter). The challenge to the electronics designer posed at the SSC by high event rate and large channel count is then further compounded by the severe radiation damage experienced by some detector elements.

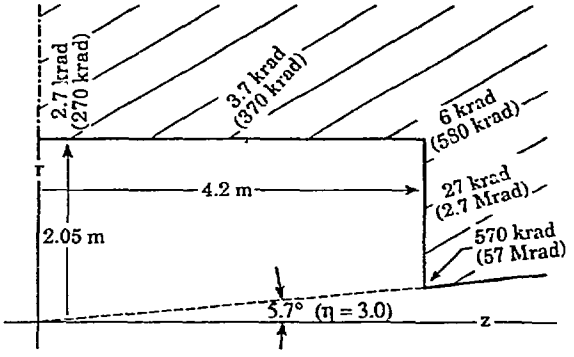

Figure 1: Total dose at several locations in a SSC detector. This figure is for an electromagnetic calorimeter of the SDC collaboration. Maximum dose occurs at shower maximum and dose indicated is for a standard SSC year at 10^{33} $cm^{-2}s^{-1}$, and (in parenthesis) for 10 years at 10^{34} $cm^{-2}s^{-1}$. Figure is taken from [4].

The effects of radiation damage on electronics have been studied by scientists associated with the military and space science community for the last 30 years, and a large body of data has been accumulated. Commercial rad-hard processes have also been developed, so the technological know-how to fabricate rad-hard electronics already exists. The purpose of this study have been to evaluate radiation resistant processes from several vendors and previous results have been published on JFETs [2] and BiCMOS processes [3].

RADIATION DAMAGE MECHANISM IN FETS

Radiation damage at the SSC is expected to be primarily caused by neutrons and ionizing radiation. A calculation of the expected neutron spectrum from a uranium/scintillator calorimeter is shown in Fig. 2. Neutrons cause damage in semiconductor materials mainly by kinematic displacements of silicon atoms from their sites in the crystal lattice. This creates recombination centers that decrease the life-time of minority carriers. Since MOSFET devices are majority carriers, they are effectively uneffected by neutrons. Some secondary processes, like ionization from recoil ions, will cause small damage in MOSFETs.

The main mechanism for radiation damage in MOSFET devices is ionizing radiation [5]. Ionizing radiation degrades the performence of FETs in two ways:

- Shift in the threshold voltage V_{th}, and
- Decrease in carrier mobility.

When an ionizing particle pass through the gate oxide it generates electron-hole pairs. As long as the device is biased during irradiation, the electrons are swept out of the oxide by the applied electric field, due to the higher mobility of the electrons, while the holes are trapped. This "hole trapping" in the gate oxide cause the the

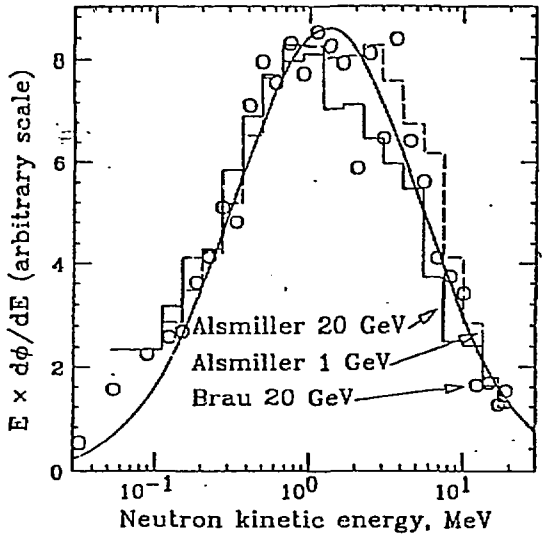

Figure 2: The calculated neutron spectrum for a uranium/scintillating calorimeter at the SSC. Figure is taken from [1].

threshold voltage to shift towards more negative va'ues, making it easier to invert a NMOS and more difficult to invert a PMOS device. This effect can be minimized by using devices with a thin gate oxide since

$$\Delta V_{th} = -\frac{Q_{ss}}{C_{ox}} = -\frac{Q_{ss} t_{ox}}{\epsilon_{ox}}. \tag{1}$$

The threshold shift will be smaller for smaller t_{ox} since Q_{ss} is volume effect, decreasing with decreasing t_{ox}. The threshold shift caused by charge trapping in the oxide will saturarate at a maximum value, after which this mechanism will cause no further shift. Ionizing radiation also causes a build-up of interface states at the silicon/oxide interface. These states traps carriers and further shifts the threshold voltage. In NMOS devices the interface states cause a shift towards more positive V_{th} and in PMOS-devices the shift is negative.

The total effect on V_{th} in NMOS devices is a shift towards negative voltages followed by a turn-around when the "hole trapping" saturates and then a shift towards positive voltages due to the interface state build-up. In PMOS-devices the two effects are cumulative and we see a continous shift towards more negative voltages.

The interface states created by ionizing radiation also decreases the carrier mobility by providing additional scattering centers for carriers. This will translate into higher thermal noise of the channel since the effective resistance, R_{eff} is given by

$$R_{eff} = \frac{1}{g_m} \propto \frac{1}{\mu}, \tag{2}$$

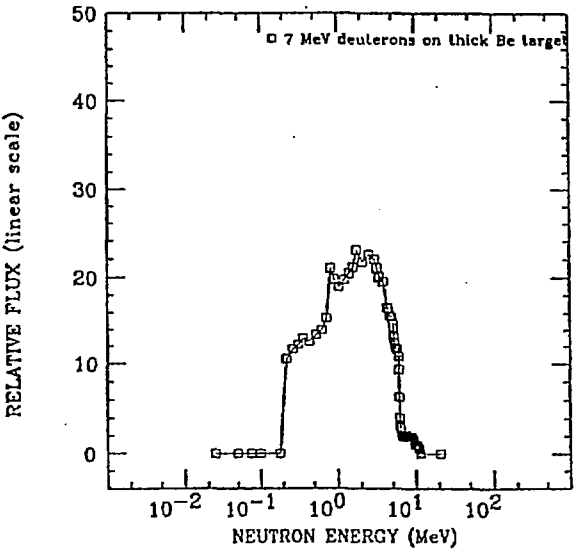

Figure 3: Neutron spectrum at fast neutron generator at Argonne, used in neutron irradiations.

where μ is the mobility.

MEASUREMENT TECHNIQUE

We performed irradiations on individual transitors from monolithic rad-hard CMOS/bulk and CMOS/SOS processes with both neutrons and ionizing radiation. The CMOS/SOS process is "Hughes 1 Mega Rad Hard SOS Process" and the CMOS/bulk process is UTMC 1.5 μm rad-hard UTDR process. The neutrons doses were between 3.5×10^{13} and 2×10^{14} neutrons/cm^2. Neutron irradiations were done at the fast neutron generator at the Engineering Physics Division at Argonne which generates neutrons by accelerating 7 MeV deuterons on a beryllium target. The spectrum (see Fig. 3) peaks at 2.5 MeV and produces a flux of 10^{10} neut/cm^2/sec. The devices were irradiated with ionizing radiation doses of 1 Mrad(Si), 3 Mrad(Si), and 10 MRad(Si). Irradiations were done at the high level gamma room at the Biology and Medical Research Division at Argonne. The source is a Cobalt-60 source rated up to 2 MRad(Si)/hr. A detailed description of the radiation sources at Argonne is given in [2]. The high dose rate at both the neutron and ionizing radiation source enabled us to simulate a ten year SSC dose in 4 – 8 hours, four orders of magnitude difference in dose rate. We have not addressed the issue of dose rate effects in this paper.

Parameters measured before and after irradiations include leakage currents through gate oxide, I-V curves ($I_D = f(V_{DS}, V_{GS})$, transconductance (g_m), and series noise at frequencies up to 100 kHz. Noise measurements were done using a Quantech Noise Analyzer and a HP 4145B Parametric Analyzer was used to aquire the other device characteristics. All devices were biased at $V_{DS} = 5$ V and $I_D = 100$ μA, corresponding to the digital low state of an inverter, both during measurements and irradiations. All devices were kept at room temperature during and after irradiations.

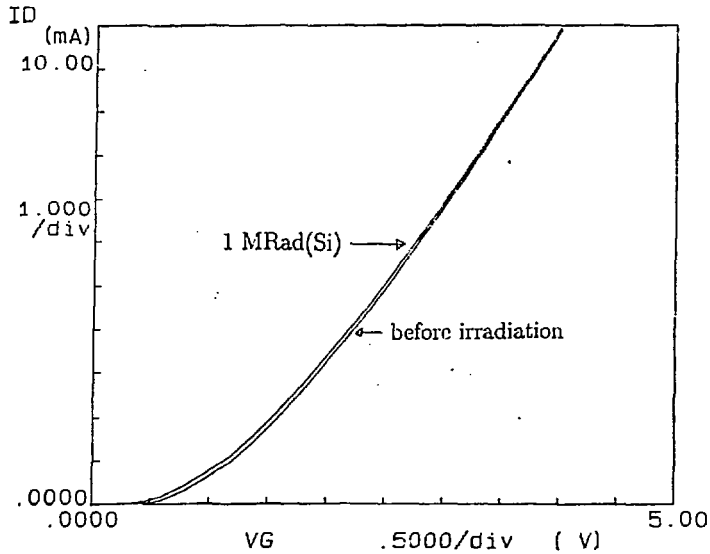

Figure 4: Threshold shift in NMOS-device from "Hughes 1 Mega Rad Hard SOS Process" after 1 MRad(Si) of ionizing radiation.

During all neutron irradiations the chip-packages were activated and all post-radiation measurements were performed between three and four weeks after exposure. The devices irradiated by ionizing radiation were all measured approximately three to four days after irradiation, but several were re-measured four to six months later and showed no additional degradation or annealing effects during that time.

RESULTS

The DC-characteristics of CMOS/SOS devices showed practically no change after irradiation with up to 10^{14} neutrons/cm^2 as expected. However the low-frequency series noise increased by a factor of two at 2×10^{14} neutrons/cm^2. The transconductance remained unchanged indicating that the series noise increase is limited to the low-frequency flicker noise, not effecting the thermal noise. 1 MRad(Si) of ionizing radiation introduced a small negative shift in V_{th}, see Fig. 4, and also caused an increase in series noise by a factor of two, but these changes are within wafer to wafer variations. Transconductance was reduced by $\sim$ 10 percent indicating a slight increase in thermal noise of the devices. Although this process is not rated up to 10 MRad(Si) of ionizing radiation, we still investigated the effects of this dose. The threshold voltage shifted with several volts and the low-frequency noise increased with a factor of two. This noise increase was accompanied by a reduction in transconductance of approximately 30 percent. No increase in gate leakage currents were noted for any of the devices.

CMOS/bulk devices were irradiated with neutron fluences between 3.5×10^{13} and 2×10^{14} neutrons/cm^2, and ionizing radiation between 1 MRad(Si) and 10 MRad(Si). At 3.5×10^{13} neutrons/cm^2 both V_{th} and noise characteristics were unchanged, while at the higher dose a small shift in the V_{th} of the PMOS device was noticed. The series noise of the p-channel device increased with a factor of two.

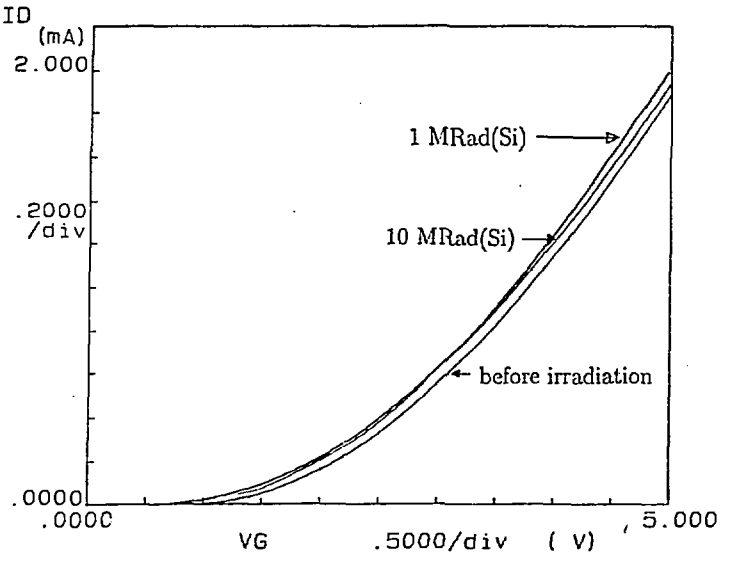

Figure 5: Threshold voltages in UTMC 1.5 μm rad-hard UTDR process for 1 MRad(Si) and 10 MRad(Si) of ionizing radiation compared to pre-rad value.

1 MRad(Si) of ionizing radiation caused a negative threshold shift of ~150 mV in both the n-channel and the p-channel device. A small increase in series noise were noted for both devices as well. With increasing radiation doses the n-channel devices went through the saturation point of "hole trapping" in the oxide and the threshold started to shift positive, partly cancelling the initial negative shift. At a dose of 10 MRad(Si) the turn-around can be seen but the positive going shift due to the inteface states is not enough to bring V_{th} more positive than it was in the pre-rad device, see Fig. 5. In the PMOS the shift is negative for all doses and the effect of additional irradiation is just to shift V_{th} even further away from the pre-rad value, making the total shift for 10 MRad(Si) approximately 200 mV. The series noise of the n-channel devices shows the effect of the continous build-up of interface states with increasing noise for each additional dose, Fig. 6. There was no change in transconductance by ionizing radiation, so the series noise increase was confined to the low-frequency flicker noise.

CONCLUSIONS

We have irradiated transistor level devices from two monolithic rad-hard MOSFET processes: UTMC 1.5 μm rad-hard UTDR CMOS/bulk process, and "Hughes 1 Mega Rad Hard SOS Process." Irradiations were performed at sources at Argonne and the doses were between 3.5×10^{13} and 2×10^{14} neutrons/cm^2 and between 1 MRad(Si) and 10 MRad(Si) of ionizing radiation.

MOSFETs are majority carrier and are not effected by neutron irradiation and we found that to be the case with our test devices. Threshold shifts caused by neutrons did not exceed 50 mV and series noise increased by a factor of two. These changes are within the variations seen in devices between different wafers and from

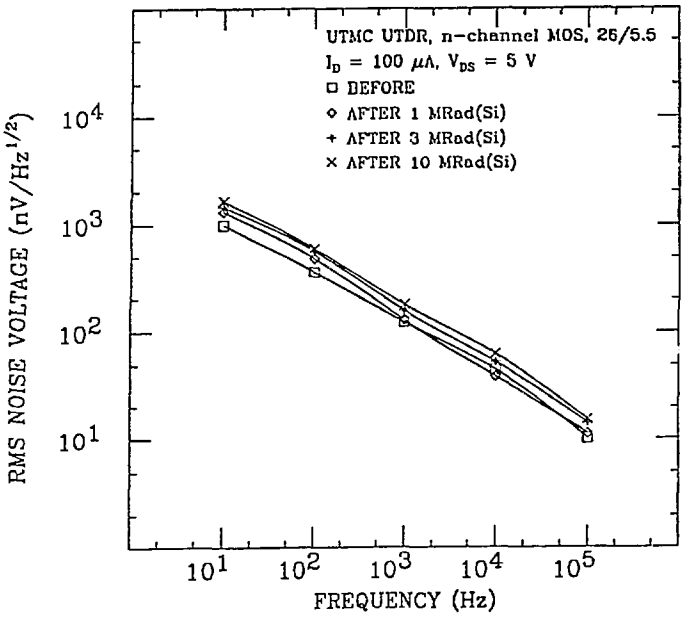

Figure 6: Series noise in UTMC 1.5 μm rad-hard UTDR process in 26/5.5 $(\mu m)^2$ n-channel device pre-rad and after 1 Mrad(Si), 3 MRad(Si), and 10 MRad(Si).

lot to lot in production. There was no change in transconductance indicating that the noise increase was limited to the low-frequency flicker noise and did not cause an increase in thermal noise, the main noise source at the fast shaping times of SSC signal processing.

Ionizing radiation is the main damage mechanism in MOSFETs thru the charge trapping in the gate oxide and the increase in surface state in the silicon/oxide interface. "Hughes 1 Mega Rad Hard SOS Process" is rated to 1 MRad(Si) of ionizing radiation and performed very well up to that dose: threshold shift was less than 100 mV and the noise increase was by a factor of two. At 10 MRad(Si) the device was still functional but threshold shift were large and noise had increased further.

UTMC 1.5 μm rad-hard UTDR CMOS/bulk process performed well up to the maximum dose of 10 MRad(Si) with threshold shifts confined to 200 mV in the worst case: p-channel threshold shift at 10 MRad(Si). The series noise increased by a factor of two at 10 MRad(Si) but no change in transconductance was noted. This indicates that the degradation in noise performance was limited to the low-frequency flicker noise.

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