HIGH TEMPERATURE ELECTRONICS FOR GEOTHERMAL WELL-LOGGING APPLICATIONS

Proceedings of a Workshop Held at The University of Arizona

April 28, 1978

Division of Geothermal Energy
DEPARTMENT OF ENERGY

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DISCLAIMER

TABLE OF CONTENTS

I. INTRODUCTION

These are the proceedings of a Workshop on High Temperature Electronics for Geothermal Well Logging, held at The University of Arizona, Tucson, Arizona, on April 28, 1978. Work has been in progress for eighteen months at The University of Arizona on passive components for high temperature operation; this work is supported by the Geothermal Energy Division of the Department of Energy. The workshop had two major objectives:

1. To present a report on the status of the work at The University of Arizona;
2. To indicate directions for future work and to obtain suggestions on these directions and on future needs from workshop participants.

To provide the proper perspective on high temperature work, participants from Sandia Laboratories and Los Alamos Scientific Laboratory were also invited to present summaries of the work in progress at their respective institutions.

An agenda for the workshop is given in Section II; the technical presentations are summarized in Sections III through VI, and the afternoon discussion session is summarized in Section VII. A list of participants is given in Section VIII.

Special thanks are due Mrs. Freida Long, L. N. Nelson, M. Aramrattana, S. J. Cosentino, and E. Morcomb for their efforts in arranging the workshop and preparing materials.

II. AGENDA

AGENDA FOR WORKSHOP ON HIGH TEMPERATURE ELECTRONICS

Meeting Place: Room 256, Student Union, The University of Arizona

Friday, April 28, 1978

8:00 - 8:30	Registration
8:30 - 8:45	Introductory Remarks
8:45 - 9:15	Review of High Temperature Work at Sandia Laboratory.
9:30 - 10:00	Review of High Temperature Active Device Work at Los Alamos Scientific Laboratory.
10:15 - 10:30	Refreshment Break
10:30 - 11:30	Passive Component Development at The University of Arizona.
11:30 - 12:00	Passive Component Integration
12:00	Lunch - Room 251, Student Union
1:00 - 2:00	Tour of Laboratory Facilities
2:00 - 3:00	Panel Discussion of Future Work
3:00 - 3:15	Refreshment Break
3:15 - 4:30	Continue Panel Discussion

III. HIGH TEMPERATURE CIRCUIT DEVELOPMENT AT SANDIA LABORATORIES

John D. McBrayer

25°C - 300°C Electronics

Sandia Labs

25°C - 300°C Electronics

With the immediate need for hardware down-hole in geothermal wells Sandia Labs has taken the approach of fine tuning existing technologies. To facilitate this need, several requirements have been defined (see Figure 1). Variations to these basic requirements have been made mostly in the form of circuitry that is in a captured environment, i.e., stable temperature containers.

Figure 2 shows the basic 300°C technology used to date. This technology comes in the form of printed circuit boards and hybrid circuits. Both have been oven tested to 300°C for 1000 hours. To date all field models are of the PC board version. Data on the various components of this technology are shown in Figure 3 thru Figure 11. It might be mentioned that although commercial components are available careful characterization of the various components must be made. This is particularly true of the active devices (Figure 12 thru 14). The present technology uses silicon JFET's and careful characterization must take place.

To obtain this characterization and to achieve other advantages (see Figure 15) several methods of pretesting active devices have been developed (see Figure 16).

The ceramic chip carrier method uses 2 x 2mm ceramic chips with thick film metallization pads on the chip carriers. The devices are eutectically attached and electrically connected to the ceramic carrier with Aℓ wire. The carrier pads had Au ribbon leads parallel gap welded in place. After passing screening tests the carrier was epoxied into the circuits (other attachments have been developed but won't be addressed here) and the Au ribbon welded to the hybrid metallization. Thermocompression Au wire bonding should be used for the last step if MOSFET's are involved.

A second method, if only a few devices had to be carefully screened per hybrid, is to isolate the hybrid bonding metallization for the device from the rest of the hybrid circuit. Au ribbon leads were used to tap into the device which was mounted on its own island on the hybrid. If the device was satisfactory the ribbons were removed and the island was connected to the rest of the hybrid by a Au ribbon jumpers. If the device was rejected, it was simply rubbed off and a new device attached in its place.

A method of prescreening for the future is a polyimide tape carrier with electrically isolated lead patterns. In order to use unbumped chips, it is possible to put conductor bumps on the carrier leads. The Au-Aℓ bonding problem should be soluble by correcting copper lead metallization. One system to address these problems is being fabricated by Pactel Corp. In this case the copper leads are Au plated on one surface with 2 mil square Ni bumps. The bumps are coated with evaporated Aℓ to enable an Aℓ-Aℓ interface on the chip.

The interconnect problem has been overcome with the use of standard bonding techniques to the conductive inks (see Figure 3 thru 6) and by the development of buffer pads, (Figure 18).

Three types of buffer pads were successful during 1000 hour 300°C tests: (1) Ni disks 30 mils in diameter, 2 mils thick, with 1μm of evaporated Au on one surface, (2) similar disks with Au on one surface and 1μm of evaporated Al on the other, and (3) silicon die with Au on one side and Al on the other.

The advantage of these discrete pads over pads plated or deposited directly on the hybrid lies in their large grain size and easily obtained thickness, both factors in lengthening the time to diffusion failure. The disadvantage of the discrete pads lies in the amount of time needed to attach the pads

to the hybrid. The metal pads were thermocompression bonded to the thick film using a wobble bonder, Kulicke & Soffa 576-1. The Si chip pads were scrubbed down using standard eutectic die down procedures. The metal pads were purchased from Cominco American Inc., and the silicon pads were made at Sandia.

To improve our 300°C technology, the emphasis will be on improving active devices and increasing circuit performance. In parallel work toward higher temperatures will continue.

As a first approach to this improvement a small scale CMOS integrated circuit has been designed and processing is under way. This circuit contains such devices as several types of flip-flops, a transmission gate, an inverter and several types of matched transistors. Hopefully this type of circuitry will help circuit designers improve upon our present technology.

In addition to the CMOS project, work is being planned to build GaAs diodes. GaAs diodes would immediately improve our 300°C technology since GaAs has a wider band gap than silicon and thus goes intrinsic at a higher temperature (see Figure 18). This less leaky diode would offer our circuit designers a great deal toward the improvement of their work. Also, GaAs diodes may be extended to GaAs transistors which could cause a great leap in overall high temperature circuit use. This would depend on the development of other components as well, i.e., cables, passive components and interconnects.

In conclusion it should be emphasized that a field tested high temperature technology (1000 hours @ 300°C) is available and is not a laboratory one of a kind. This technology can be made by any one willing to take the care needed.

GEOTHERMAL ELECTRONICS REQUIREMENTS

1. Operation from 25 to 300°C
2. Commercially Available
3. Life at 300°C of 100 to 1000 hours
4. Microelectronics (Volume, Cost)
5. Upgradeable to 400°C Operation

Figure 1

HIGH TEMPERATURE MICROCIRCUITS

SUBSTRATE:	96% Alumina
CONDUCTOR:	Fritless Au/Dupont 9910
RESISTORS:	Thick Film (TCR minimized at 150°C Cermalloy 530 Lot 2430)
CAPACITORS:	1. Thick Film (DuPont 8299) less than 10,000 pF
	2. Al Solid Electrolyte (Phillips) greater than 2 μF
	3. Avoid .01-2.0 μF range.
BONDING:	1. Welded Au Ribbon
	2. Beam Lead
	3. Al Wire to Thick Film or Au-Al Disk
ACTIVE:	Si JFET's (Motorola)

Figure 2

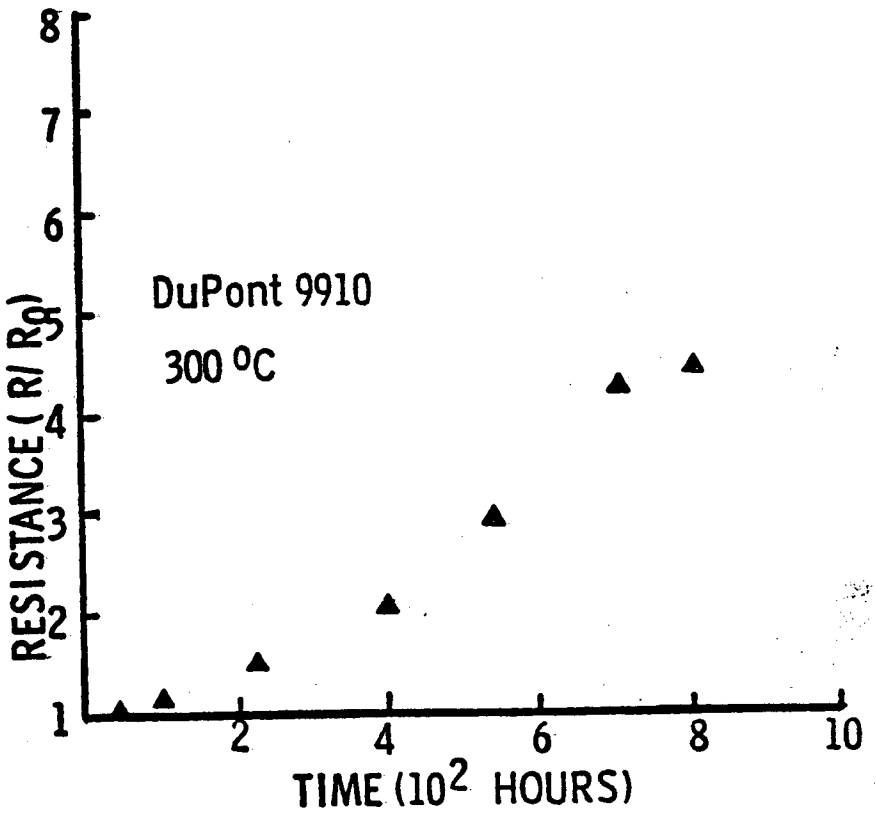

DuPont 9910
300 °C
RESISTANCE (R/ R0)
TIME (10² HOURS)
1
2
3
4
5
6
7
8
2
4
6
8
10

Figure 3

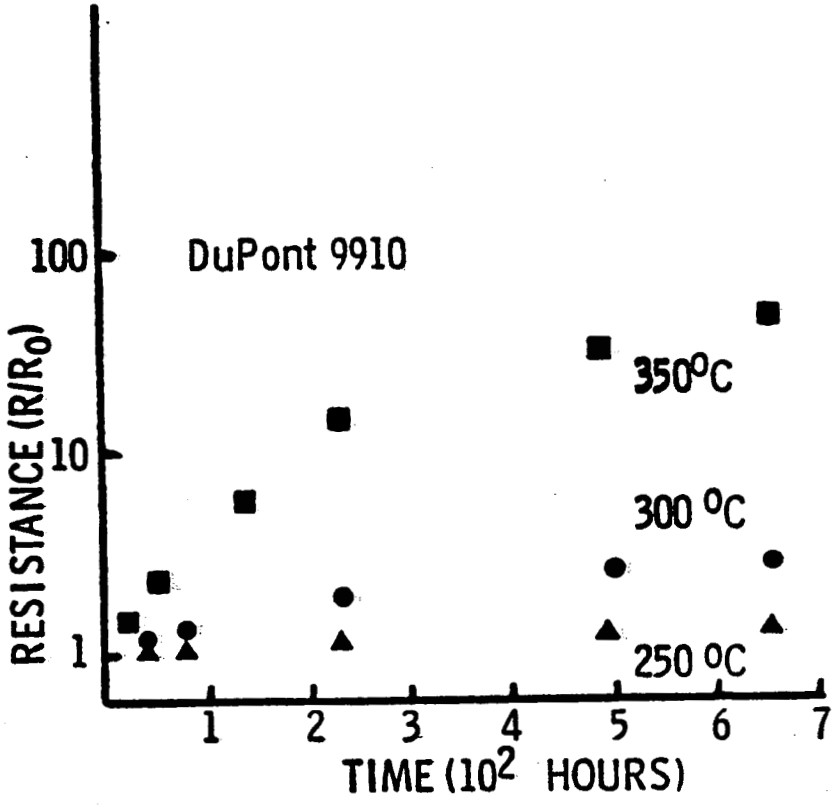

DuPont 9910
RESISTANCE (R/R0)
100
10
1
350°C
300 °C
250 °C
1
2
3
4
5
6
7
TIME (10² HOURS)

Figure 4

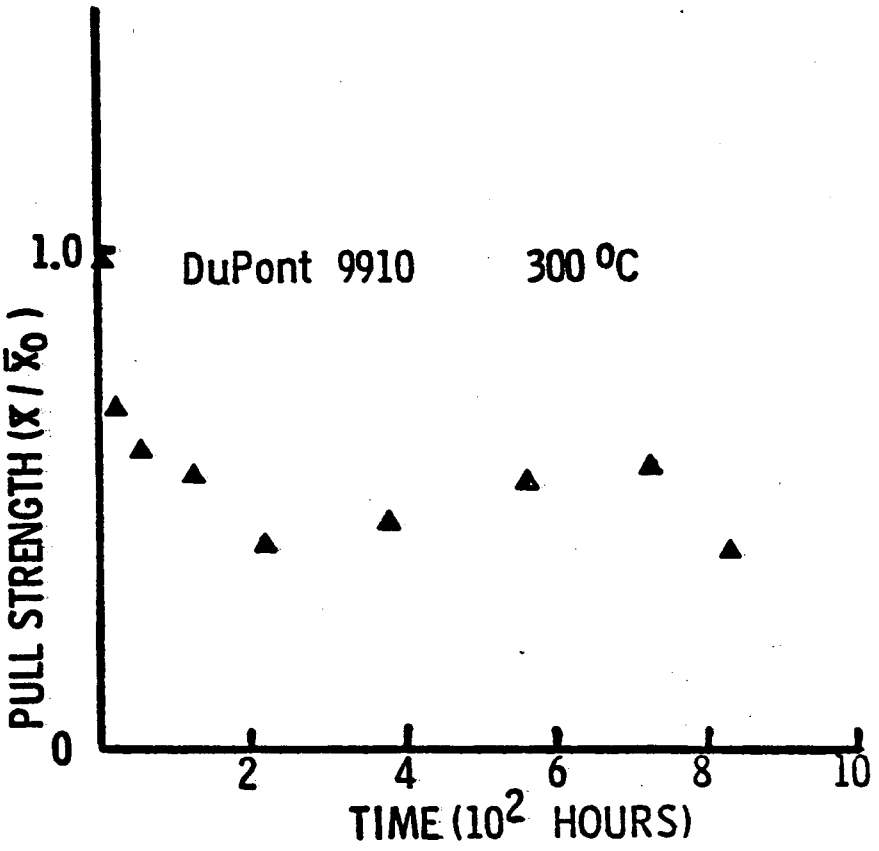

1.0
DuPont 9910
300 °C
PULL STRENGTH (x / x̄o)
0
2
4
6
8
10
TIME (10² HOURS)

Figure 5

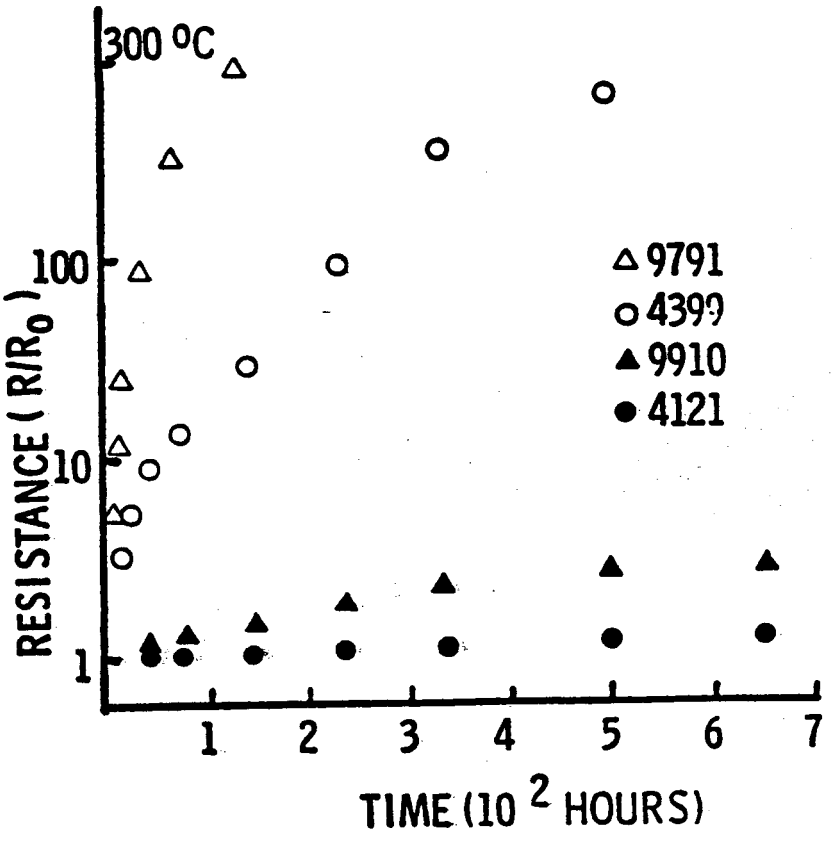

300 °C
100
10
1
RESISTANCE (R/R0)
△ 9791
○ 4399
▲ 9910
● 4121
1
2
3
4
5
6
7
TIME (10 2 HOURS)

Figure 6

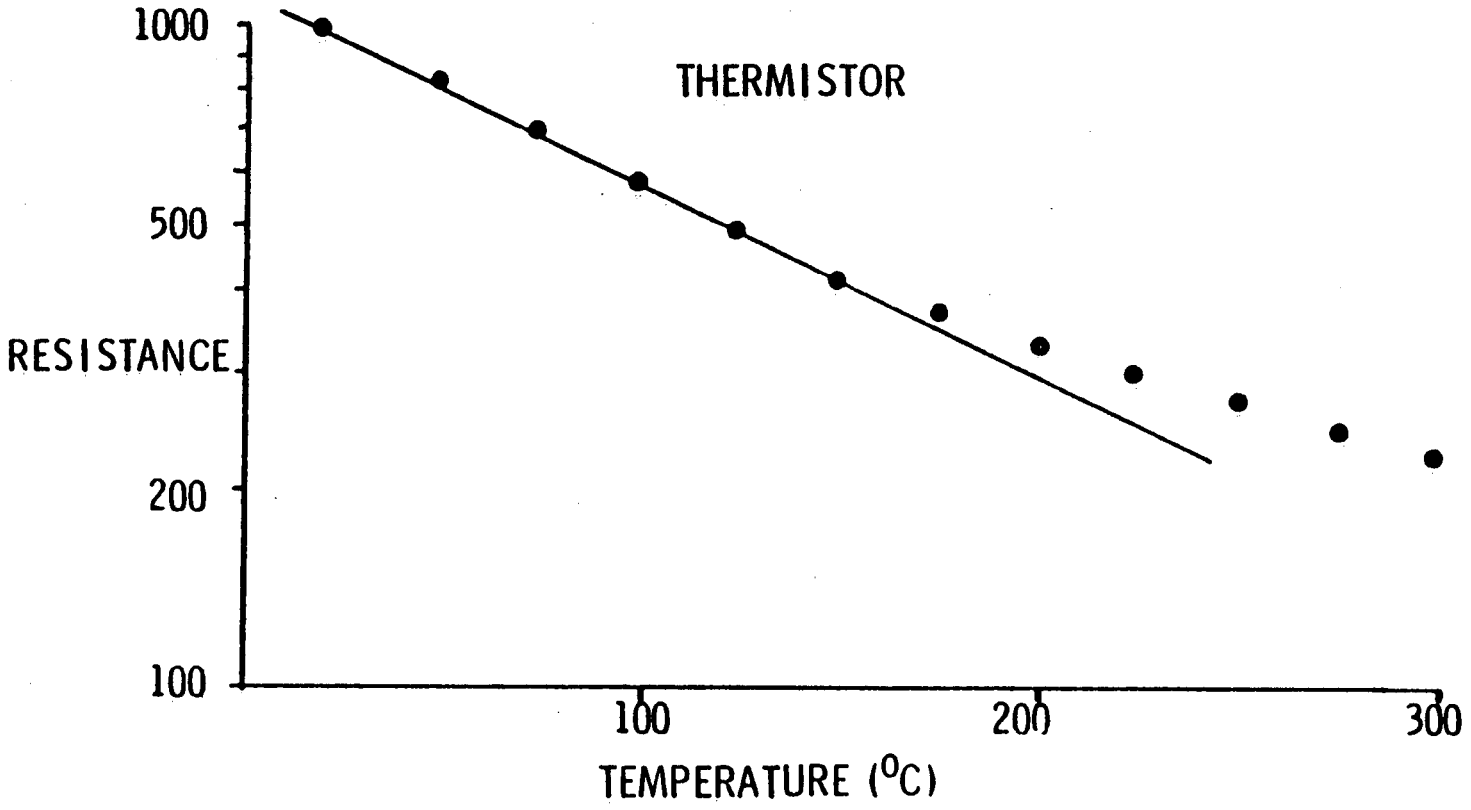


Figure 7

THE RESISTANCE OF A THICK FILM THERMISTOR HAS A TEMPERATURE DEPENDENCE SIMILAR TO A BULK SEMICONDUCTOR.

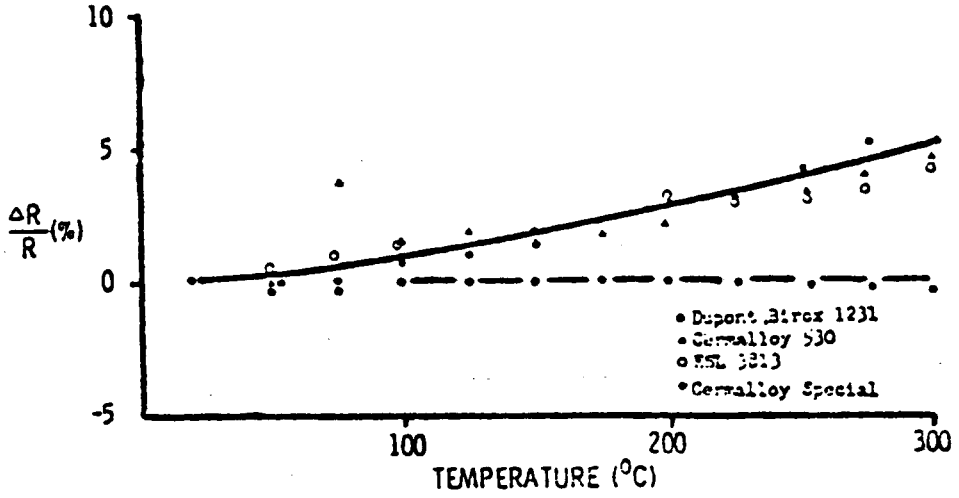
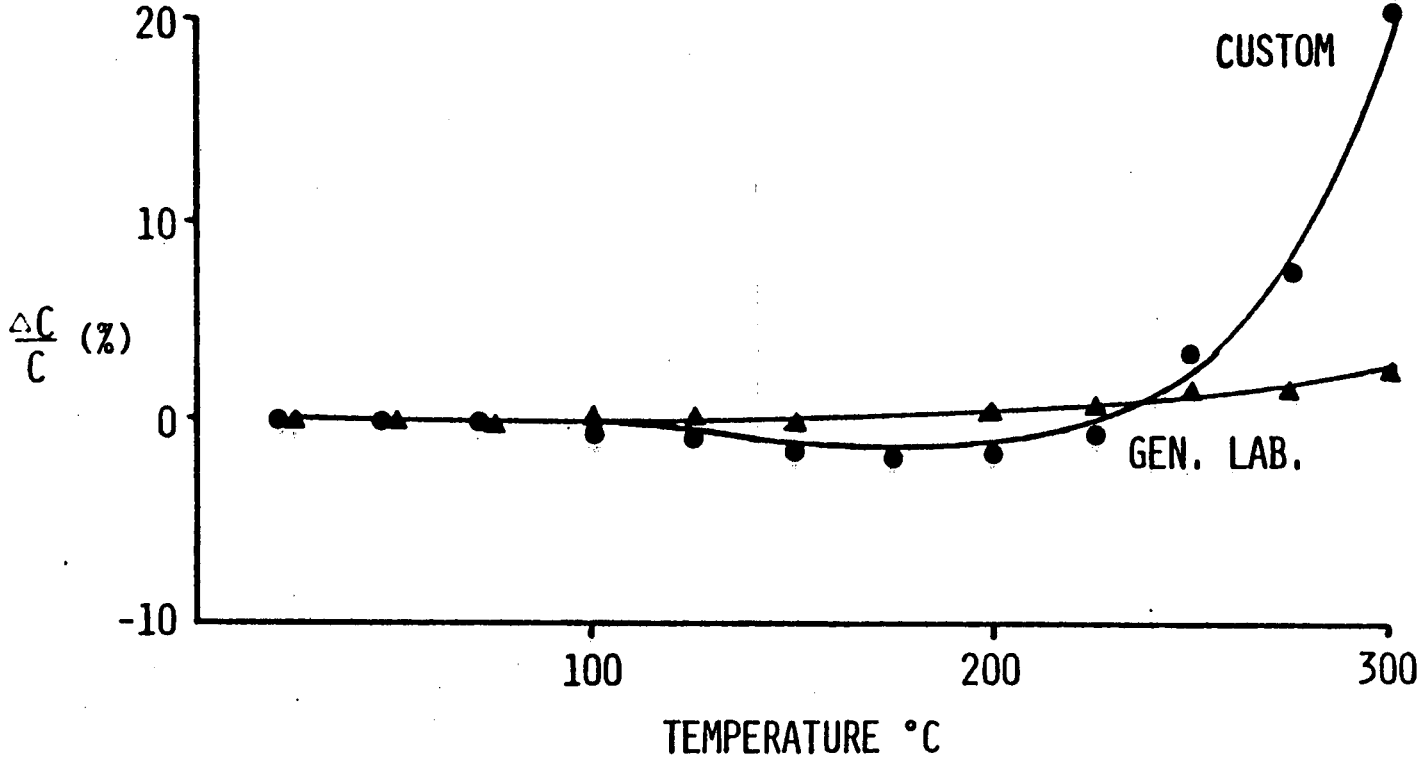
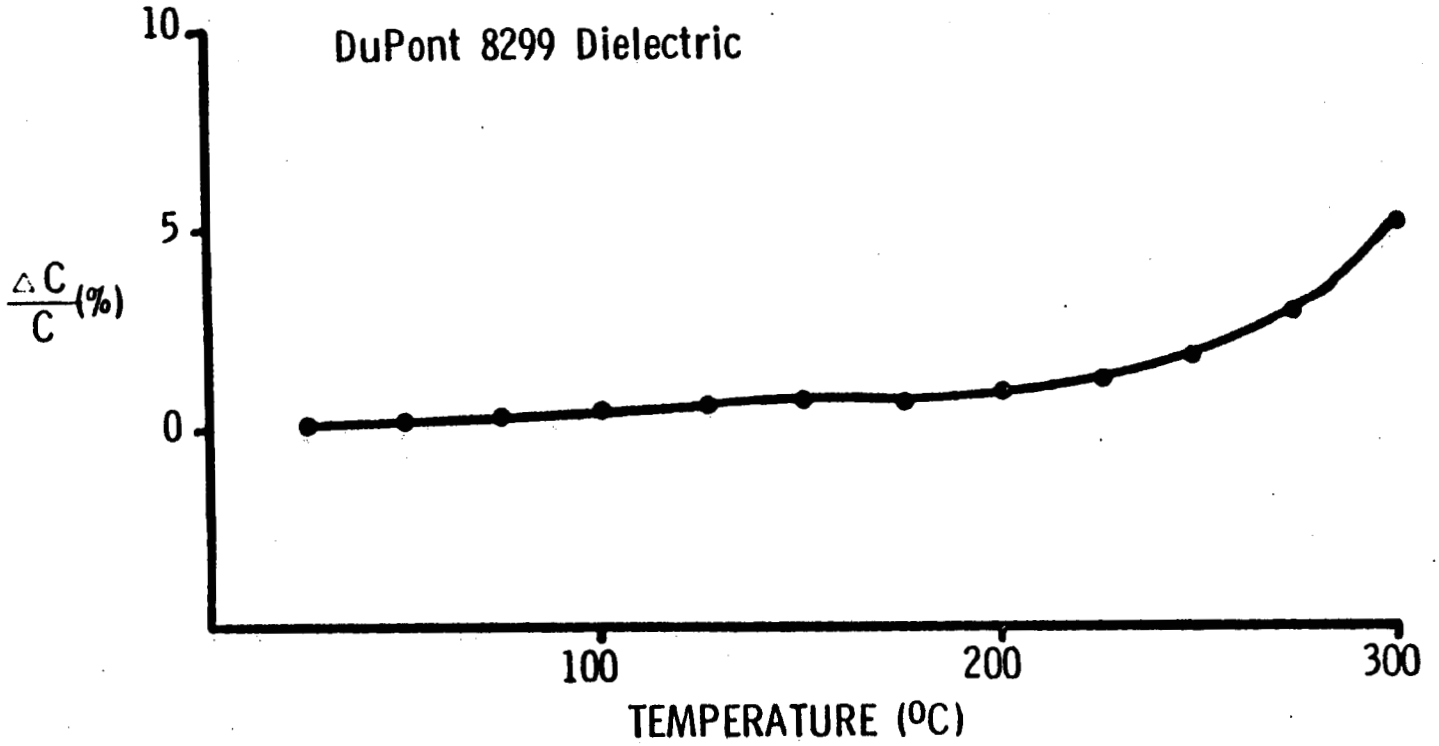

10
5
0
-5
ΔR/R (%)
100
200
300
TEMPERATURE (°C)
• Dupont Pyrex 1231
• Cermalloy 530
o RSL 3313
• Cermalloy Special

Figure 8



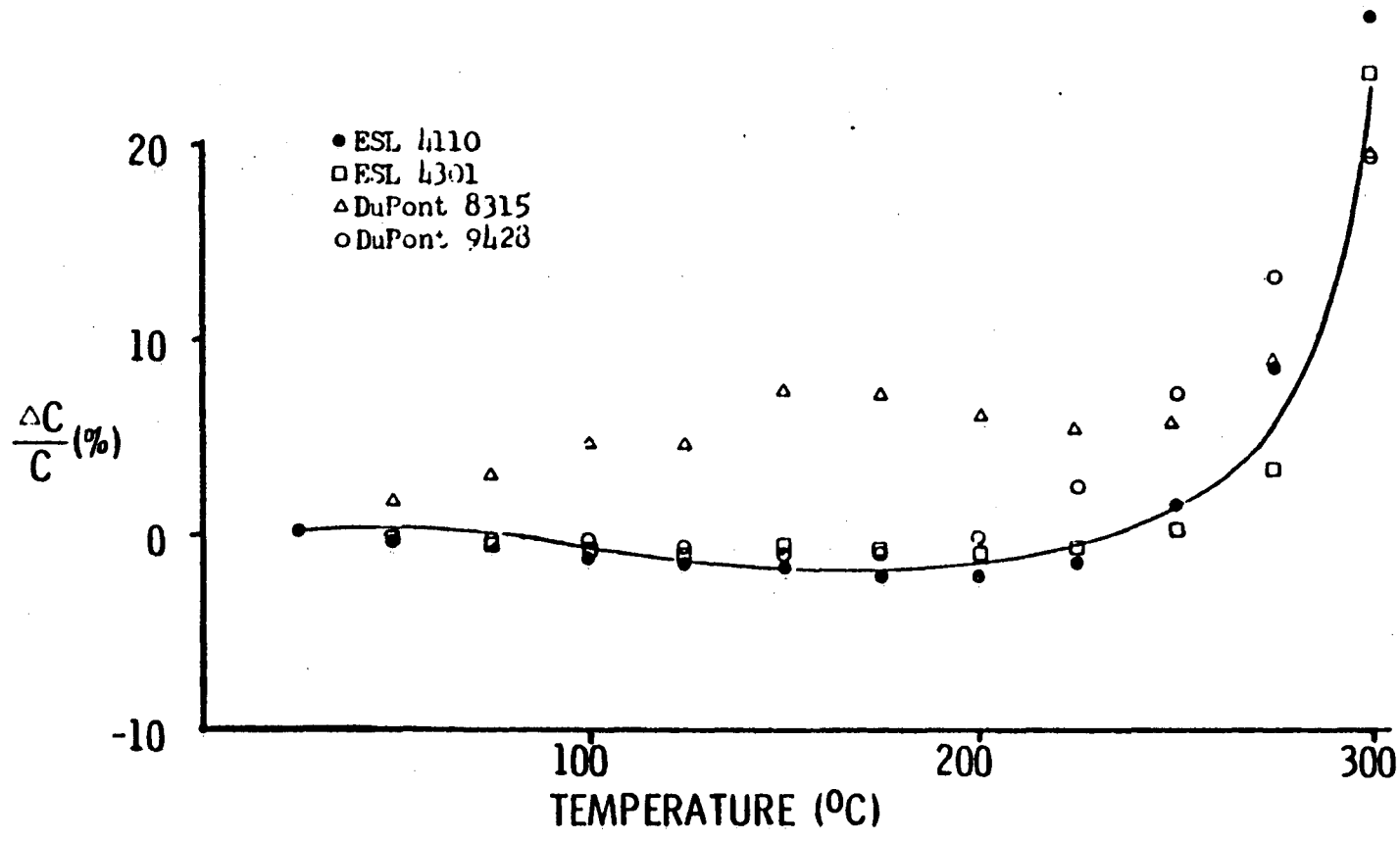
TEMPERATURE CHANGE OF CAPACITANCE OF RECONSTITUTED PAPER MICA CAPACITORS FROM TWO COMPANIES. CAPACITOR FROM CUSTOM WAS ONLY RATED TO 260°C SO THIS TEST IS AN OVER TEST. CUSTOM P/N CHR3A1545SP, GENERAL LABORATORY ASSOCIATE 500 V/0.1 μF NO PART NUMBER GIVEN.

Figure 9



IN OUR HANDS DUPONT 8299 DIELECTRIC INK GAVE THE MOST CONSISTENT, USEFUL DIELECTRIC PARAMETERS. THE CAPACITANCE CHANGED ONLY ABOUT 5% FROM 24 TO 300°C. BECAUSE OF A DIELECTRIC CONSTANT OF 8-10 THIS INK IS ONLY USEFUL FOR SMALL CAPACITANCES.

Figure 10



TEMPERATURE CHANGES OF CAPACITANCE OF THICK FILM CAPACITORS. THESE CHANGES ARE REVERSIBLE WITH CHANGES IN TEMPERATURE. THESE DIELECTRIC INKS HAVE ADVERTISED DIELECTRIC CONSTANTS OF 10-15 DEPENDING ON FABRICATION PROCEDURES.

Figure 11

Active Devices Considered

Si: Bipolar, MOSFET's, and: JFET's

GaAs: MESFET's and: JFET's

Ceramic Vacuum Tubes

Figure 12

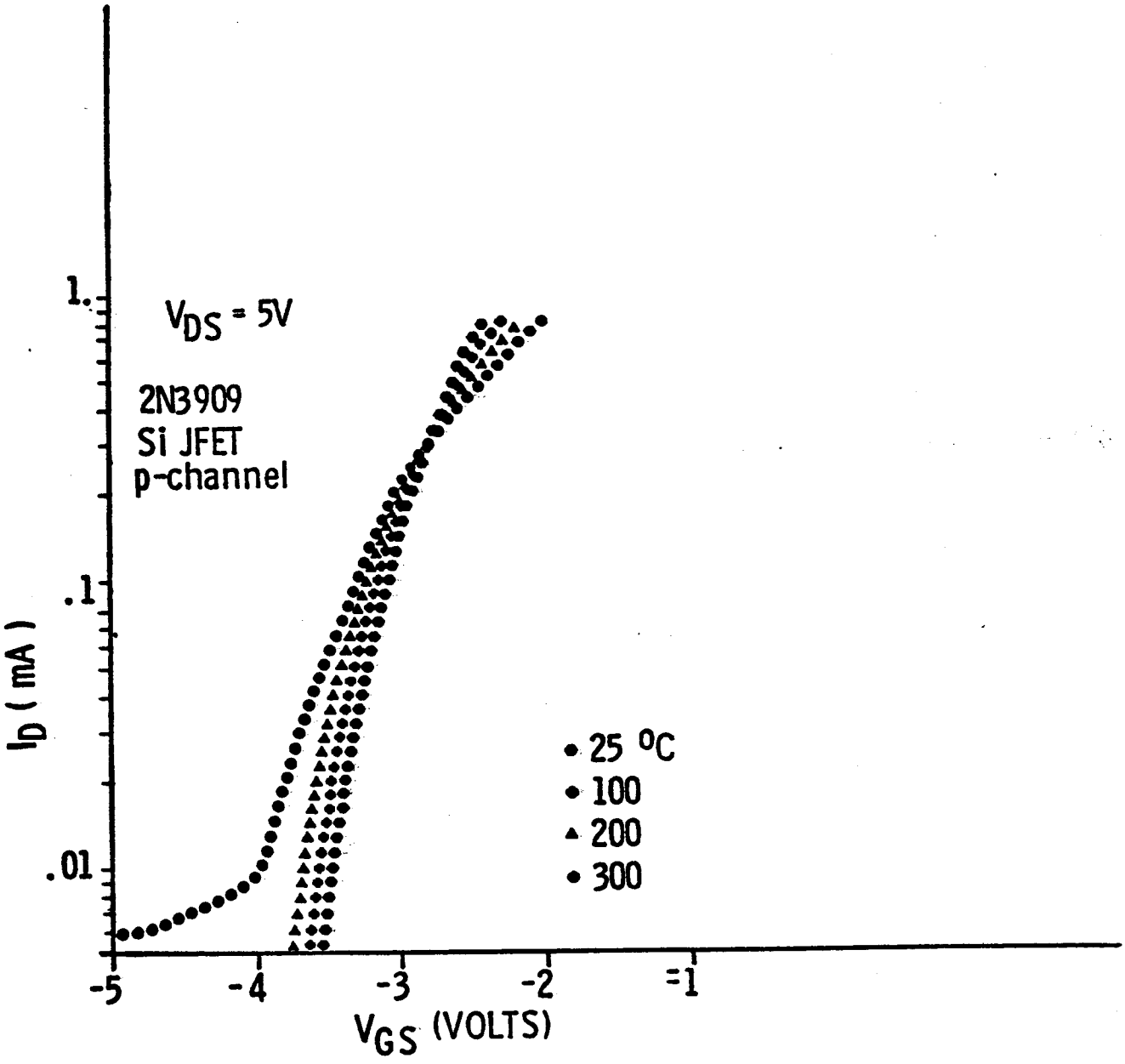

1.
.1
.01
I_D (mA)
V_{DS} = 5V
2N3909
Si JFET
p-channel
• 25 °C
• 100
▲ 200
• 300
-5
-4
-3
-2
=1
V_{GS} (VOLTS)

Figure 13

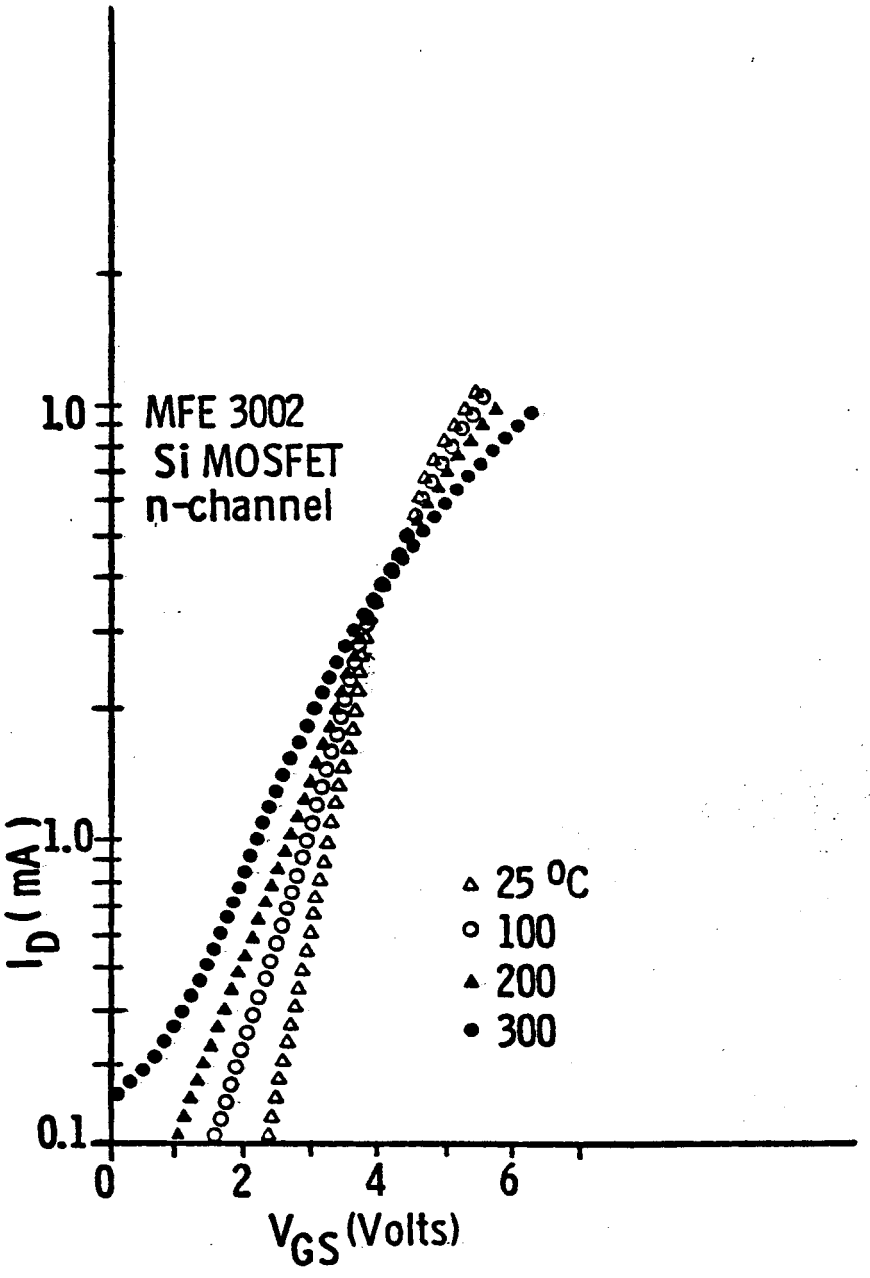

MFE 3002
Si MOSFET
n-channel
1.0
0.1
I_D (mA)
25 °C
100
200
300
0
2
4
6
V_{GS} (Volts)

Figure 14

300°C Pretesting of Devices Allows

1) Extreme Temperature Dependent Device Rejection

2) Tailoring to Exact Device Charcteristics

3) Matching Devices

4) Eliminating Infant Mortality

Figure 15

Methods of 300°C Pretest

1) Ceramic Chip Carrier

2) Segregation Within the Hybrid

3) Polyimide Chip Carrier

Figure 16

CHIP BONDING

BUFFER PADS

AL WIRE BONDING TO DUPONT 9910

Figure 17

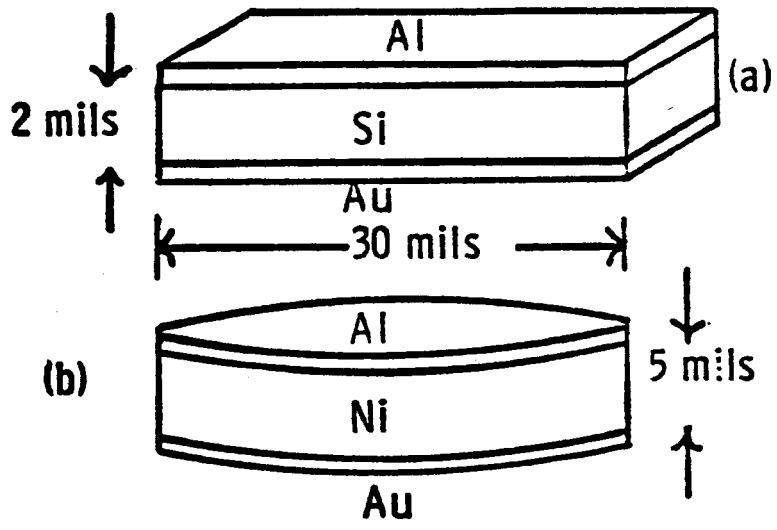


Figure 18

Active Device Improvement

CMOS - Small Scale Integration

GaAs - Diodes and Discrete Transistors

Figure 19

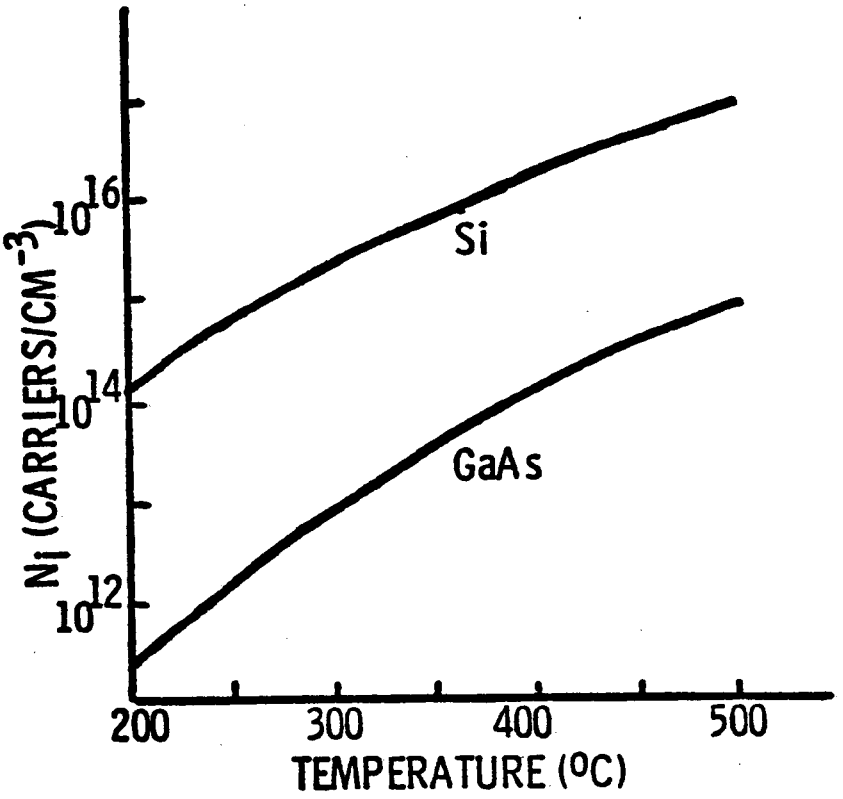

N_i (CARRIERS/CM^{-3})
10^{16}
10^{14}
10^{12}
Si
GaAs
200
300
400
500
TEMPERATURE (^{o}C)

Figure 20

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IV. HIGH TEMPERATURE ACTIVE DEVICE RESEARCH AT LOS ALAMOS SCIENTIFIC LABORATORY

J. Byron McCormick

Structure and Characteristics of Integrated Thermionic Devices

Integrated thermionic devices are microminiature devices operating in a vacuum and possessing terminal characteristics similar to those of a 6SL7 triode vacuum tube. These devices were invented at Stanford Research Institute in the late 1960's; recent work has been carried on by Los Alamos Scientific Laboratory, with assistance by University of Arizona personnel. Operating temperature of the devices is in the range 650°C to 1000°C; no semiconductor devices can operate at these temperatures. In addition to being capable of operation at high temperature, the thermionic devices are much more radiation-resistant than semiconductor devices. They are candidates for circuits in geothermal well-logging tools, coal gassification monitoring and control, and nuclear reactor instrumentation and control.

The basic device construction is shown in Fig. 1. On a sapphire substrate molybdenum electrodes are deposited by sputtering, chemical vapor deposition (CVD), or electron-beam evaporation, and delineated by photolithography. Grid and cathode lines are interdigitated as shown, and a heater is deposited on the reverse side of the substrate. Cathode material is mixed with photoresist and deposited on the wafer; selective delineation of the cathode material on the cathode electrodes is accomplished by appropriate exposure of the photoresist through a photomask. A second substrate with anodes of molybdenum delineated by photolithography is placed above the first substrate and aligned. The entire structure is placed in an envelope which is evacuated. The substrate containing the cathode-grid structure is heated to 900°C with proper voltages applied to the electrodes, and the cathodes are thus activated. During activation a vacuum pump is

attached to the envelope and the activation products are monitored by a mass spectrometer. Upon successful activation, the envelope is sealed and the devices are ready for use. A set of characteristics for a typical device is shown in Fig. 2; this device has five cathode stripes 50 mils in length and 1 mil wide interdigitated with six grid stripes 50 mils in length and 1 mil wide. Separation between stripes is 1 mil, and separation between the anode and the grid-cathode is 120 mils. It is to be noted that fewer stripes of shorter dimensions can be used; the size of an individual device thus approaches the size of an individual device in early silicon integrated circuits.

Grid linewidths and grid-cathode spacing of 0.1 mil (2.5 micrometers) can be achieved with ordinary integrated-circuit photolithography techniques. Therefore a large number of these devices can be placed on a single substrate, with the advantages not only of small size but also of matching and tracking of characteristics.

Considerable work has been done at Los Alamos Scientific Laboratory, not only on development of the fabrication technology, but also on computer-aided modeling of integrated thermionic structures. Two important results, which have been experimentally confirmed, are:

1. The amplification factor μ is a linear function of d/a, as shown in Fig. 3, where d is the distance between anode and cathode, and a is the spacing between grid and cathode stripes. This result has important consequences for integrated thermionic circuits. Since all devices on a given substrate will have the same anode-cathode distance d, both high-μ and low-μ devices can be fabricated on the same substrate merely by using different grid-cathode spacing for different devices.

2. The anode $I_p - V_p$ characteristics for a given device are given by

$$I_p = K(V_G + V_p/\mu)^{3/2}$$

where K is the perveance. This has been verified by computer analysis as shown in Fig. 4, and also experimentally. Since K is proportional to cathode area, all devices on a given substrate will have K values in the ratio of their cathode areas. Thus both high-current and low-current devices can be fabricated on the same substrate merely by choosing the proper cathode areas.

It should be noted that integrated thermionic devices operate in a space-charge-limited regime. Even if small temperature differences exist across the cathode substrate, these will not cause differences in device characteristics. Therefore, properties similar to those of silicon integrated circuits exist in integrated thermionic circuits, namely:

1. Matching of devices is controlled by matching their geometry. Characteristics can be ratioed this way also. Since the geometry is delineated by photolithographic techniques, precise control of geometry can be obtained.
2. Tracking of the characteristics of all devices on the same substrate can be realized.

Results

During the past year all fundamental device characteristics necessary for use in realistic circuitry have been demonstrated. Devices have been fabricated with voltage amplification factors from 10 to over 100 while

transconductances in excess of 1000 micromhos have been observed for .1" x .1" devices. These values are comparable to those of commercial vacuum triodes over 100 times larger. The experimental device characteristics have been accurately modelled by an extended version of the conventional triode equation, and design rules for device sizing, layout and spacing have been derived and proven. Experimental yields on these first devices have exceeded 90%, and in the initial lifetime tests devices have been operating successfully for three months at 700°C and continue to operate. Elementary multiple device circuits (amplifiers) have been constructed using several devices on a single substrate with externally connected passive components. These early results indicate that no fundamental barriers exist to the fabrication of complete circuit functions on a single wafer.

In order to satisfy the ultimate circuit needs for geothermal instrumentation, functional building blocks such as operational amplifiers, multiplexers and line drivers, etc., will be necessary. In preparation for the development of these circuits, the program to date has emphasized basic circuit design techniques and computer circuit analysis.

The design of ITC circuits is in many ways similar to the design of conventional integrated circuits. ITC design techniques, therefore, utilize the advantages gained from the simultaneous fabrication of many devices on the same substrate. The inherent matching of device characteristics and the tracking of those characteristics over temperature and life are exploited. Functional circuit elements such as differential stages, current sources and circuits which use active devices as loads have been fabricated and their performance verified against theory.

Along with the development of basic circuitry, ITC device models have been successfully incorporated into circuit analysis programs, NET-2, SCEPTRE, and SPICE.

Package

Since the ultimate goal of the research is to develop devices which can be used in down-hole instrumentation circuits, it has been recognized since the inception of the program that a high-temperature package would have to be developed. However, package development was not begun until good device performance was obtained, in order that the package requirements relative to compatibility with devices could be better established. The ultimate temperature limit of the ITC is expected to be determined by the package, since devices have been operated successfully with substrate temperatures of 1000°C (1832°F). The immediate goal is a package that will operate at 500°C (932°F).

A package configuration to demonstrate high temperature feasibility has now been designed and several materials approaches, including glass-ceramic and metal-ceramic, are under development. Orders for packages have been placed, and delivery of metal packages using ceramic pin seals is expected in approximately six months. If these packages meet expectations, high temperature operation of packaged devices should be demonstrated within a year.

Once high temperature operation has been demonstrated, a geothermal prototype package for down-hole operation will be designed and fabricated.

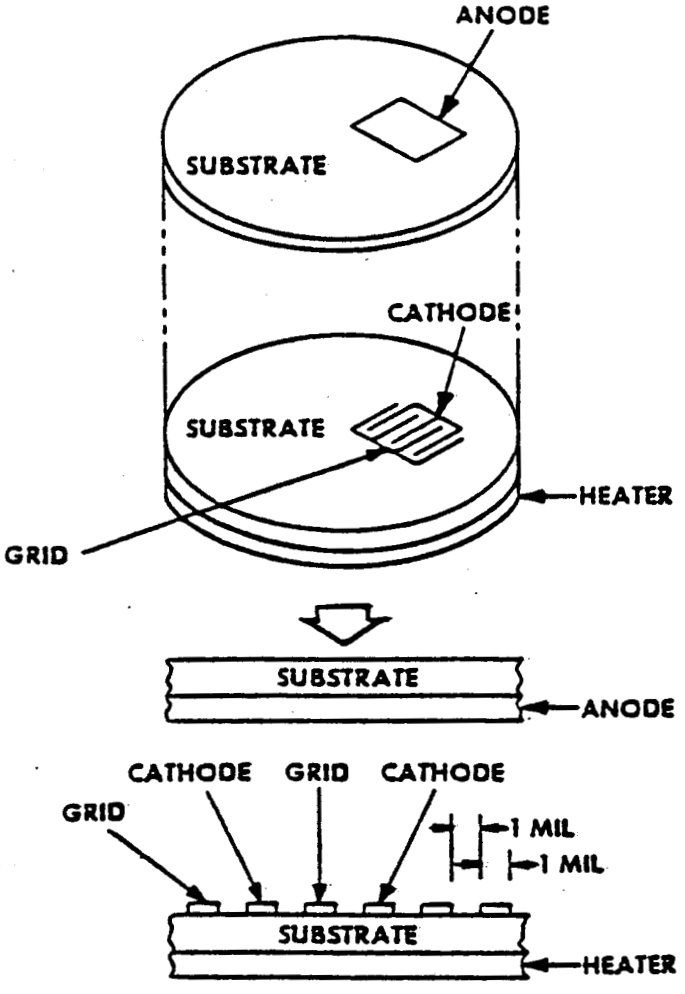


Figure 1

Sketch of the Integrated Thermionic Device Structure

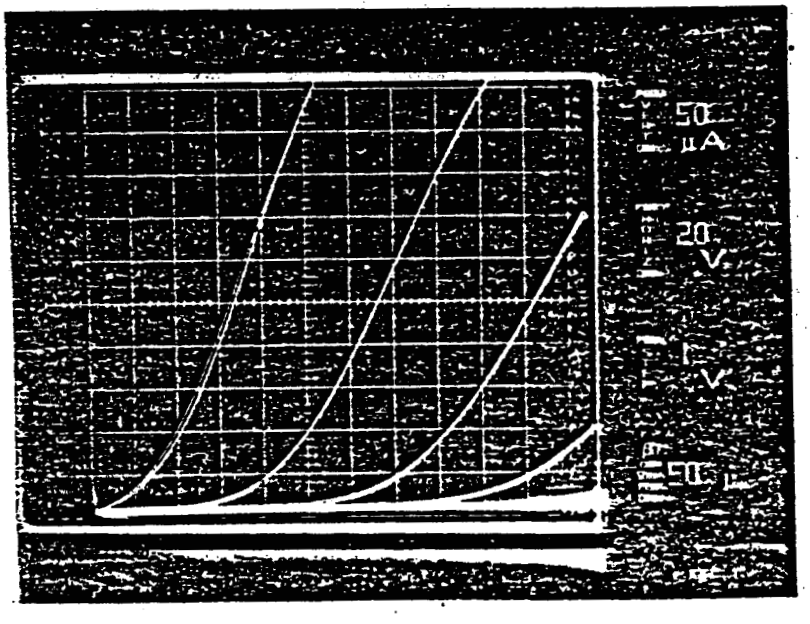


Figure 2

Anode V-I Characteristics for a Device with 1 mil grid and cathode lines and spaces, 120 mil anode space.

V_G = 0, second trace from left
Grid voltage steps: 1 volt
Vertical: 50 μamp/division
Horizontal: 20 volts/division

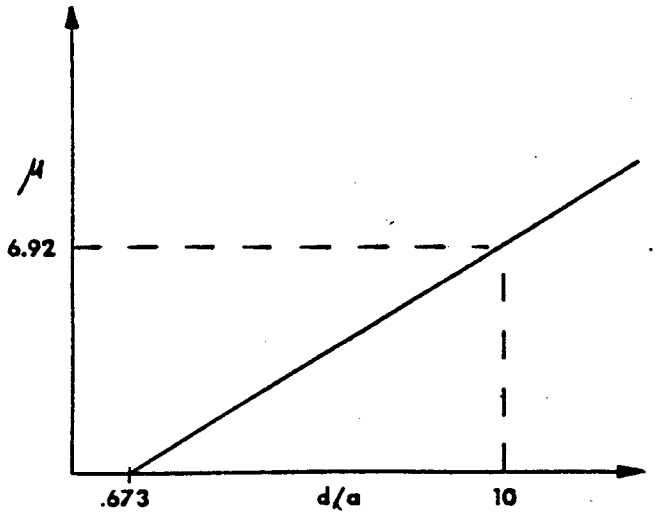


Figure 3

Relation between μ and geometry

d = anode-cathode distance
a = grid-anode spacing

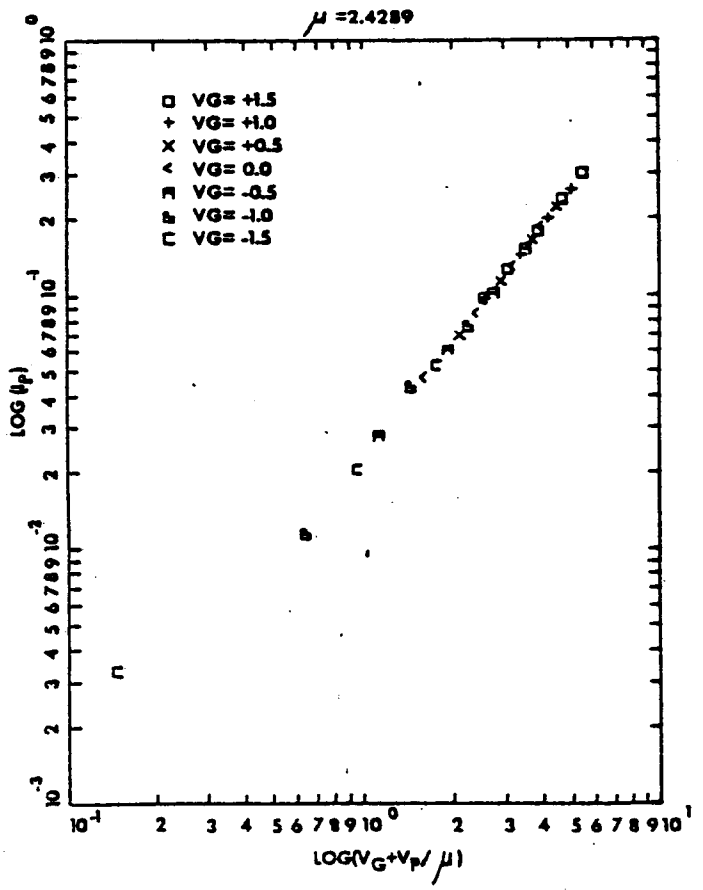


Figure 4

Demonstration of the 3/2 law relationship in

$$I_p = K(V_G + V_p/\mu)^{3/2}$$

V. HIGH TEMPERATURE PASSIVE COMPONENT DEVELOPMENT AT THE UNIVERSITY OF ARIZONA

Leonard S. Raymond

For the past eighteen months The University of Arizona has been developing passive components for high-temperature operation. These include resistors, capacitors, interconnections and passivation. Goals for this work are given in Fig. 1; note that the upper temperature limit is 500°C. It should be emphasized that these components must operate satisfactorily over the entire temperature range 25°C to 500°C; this includes the present near-term goal of 300°C used in other geothermal instrumentation circuit development. Since typical failure modes accelerate exponentially with temperature, devices which have acceptable performance at 500°C can be expected to exhibit superior performance at 300°C.

It is desirable to be able to integrate the fabrication of passive components so that all types can be fabricated on a single substrate in a single processing sequence. The devices described here meet that criterion; Fig. 2 shows a cross-section diagram of such an integrated combination. It is to be emphasized that the drawing is not to scale; the technology used here is a thin-film technology and the film thicknesses are of the order of several thousand Angstroms while the lateral dimensions are typically hundreds of micrometers.

The materials used in the process are listed in Fig. 3; these have been chosen because they meet the requirements listed in Fig. 1.

Details regarding each of the components are given in Figs. 4 through 7. The salient feature of the fabrication process is the use of chemical vapor deposition. As is shown in Fig. 8, this is accomplished by indirect heating of the substrates in a quartz reaction tube into which is admitted a mixture of gases containing the proper constituent elements. A chemical reaction occurs at the hot surface of the substrates, causing the deposition of the desired film. For example, to deposit a tungsten-silicon

film for resistors, the gases tungsten hexafluoride and silane are injected into the tube together with an appropriate carrier gas. Variables which are controlled to produce the desired results are temperature, flowrates, gas mixtures, and deposition time. Some of the advantages of this method are listed in Fig. 9.

A photomicrograph of the resistor test pattern used for evaluation is shown in Fig. 10. This pattern contains several resistors, as well as a Van Der Pauw pattern for measuring sheet resistance. The overall chip size is 100 x 100 mils, and minimum linewidth in the pattern is 1 mil. Plots of resistance versus temperature for several resistors are shown in Fig. 11; it should be noted that:

1. The temperature range is 27°C to 550°C.
2. The plots are for one complete cycle of the temperature range, starting at and returning to 27°C. No hysteresis is observed.
3. The resistance variation with temperature is small, and it is also linear, indicating that the temperature coefficient is approximately constant.

A photomicrograph of the capacitor test pattern is shown in Fig. 12; again, the chip size is 100 x 100 mils. Plots of capacitance versus temperature for several capacitors are shown in Fig. 13; again, no hysteresis is observed, and the temperature coefficient is approximately constant. In these plots the temperature range is 27°C to 350°C; this is because passivation was not used and the tungsten metallization oxidizes at temperatures above 350°C. Capacitors now being processed have passivation, as well as platinum bonding pads.

Conductivity of the silicon nitride dielectric is shown in Fig. 14; for comparison a curve published by Kingery is also plotted. It will be noted that two different samples are shown, one with 900 Angstroms thickness and one with 5475 Angstroms thickness. In both cases the conductivity is a function of the average electric field in the dielectric.

No pinhole problems have been observed with the capacitors; this is because the process has been specifically designed to self-heal any pinholes which occur. The result is that while a pinhole may appear in the metal pattern, it will not appear in the dielectric; therefore, there will be no conducting path through the dielectric.

Capacitor leakage current density is shown in Fig. 15 for three different temperatures; note that the temperatures are given in degrees Kelvin, and correspond to 23°C, 227°C and 327°C. For purposes of comparison, a capacitor made with the 5140 Angstroms dielectric of Fig. 15 would have a capacitance of about 155 pF/mm^2. From Fig. 15 we see that a 1 mm^2 capacitor operating at 327°C with 60 volts applied would have a leakage current of 10^{-8} amp.

In order to test the integration of resistors, capacitors, interconnections and passivation on the same chip, a third-order Butterworth RC-active filter is being fabricated. The circuit is shown in Fig. 16; only the portions enclosed by the broken line are on the chip. Details of the circuit design are given in Section VI. A photomicrograph of the chip is also shown in Fig. 16. Chip size is 100 x 100 mils and minimum linewidth is 1 mil.

In order to connect our passive components to active devices, hybrid circuits, or other passive components, some form of interconnections

different from those on the chip is necessary. We have used platinum bonding pads and 1 mil diameter platinum wire for this purpose; the bonding between wire and pad is done ultrasonically. Figure 17 shows a photomicrograph of a 1 mil platinum wire bonded to a platinum pad. This bond is mechanically strong and the platinum will withstand high temperatures. Similar bonding methods are used in the Los Alamos Integrated Thermionic Devices operating at temperatures in excess of 600°C.

In order to expedite measurements and life testing, we have incorporated a Hewlett-Packard Data Acquisition System, together with a HP9825A calculator and a plotter. Programming for this system has now been completed to the point where the system can monitor devices on the probe station, make measurements, process the data and plot the results. A plot for a resistor is shown in Fig. 18. (This resistor has a sheet resistance of 1500 ohms per square.) On this particular plot only R vs T is shown; however, the programming also permits plotting of temperature coefficient, printout on the plot of average TCR between any two temperatures, plotting of tracking coefficient for two resistors, and printout of the plot of average tracking coefficient.

Work has just been initiated on cycling and life testing. Preliminary results are shown in Fig. 19 for one resistor on a wafer cycled as described in the figure. Note that on this wafer the sheet resistance was 5000 ohms per square. The change in the resistance after the cycling was 0.19%. A plot of R vs T for the resistor after cycling is shown in Fig. 20; the rather high average TCR was expected because of the high sheet resistance. Also, the irregularities in the plot are believed to be due to mechanical motion of the probes on the bonding pads. This is observed on all samples when platinum pads are probed with tungsten probes, because both materials are quite hard. When

aluminum pads are probed, the irregularities do not occur. It is expected that they will not occur when platinum bonding wires are used instead of probes.

A summary of the important parameters for the passive components is given in Fig. 21.

The present contract terminates September 30, 1978. Figure 22 shows the anticipated status of the work by that date.

GOALS FOR PASSIVE COMPONENT DEVELOPMENT

OPERATION FROM 25°C TO 500°C (77°F TO 932°F)

STABLE

MATERIALS COMPATIBLE WITH EACH OTHER

MATERIALS COMPATIBLE WITH ACTIVE DEVICES

COMPATIBLE FABRICATION PROCESSES

GOOD PROCESS CONTROL

WIDE RANGE OF ELEMENT VALUES

LASER TRIMMABLE

WITHSTAND HOSTILE ENVIRONMENT

Figure 1

PASSIVE COMPONENT STRUCTURE
(CROSS-SECTION)

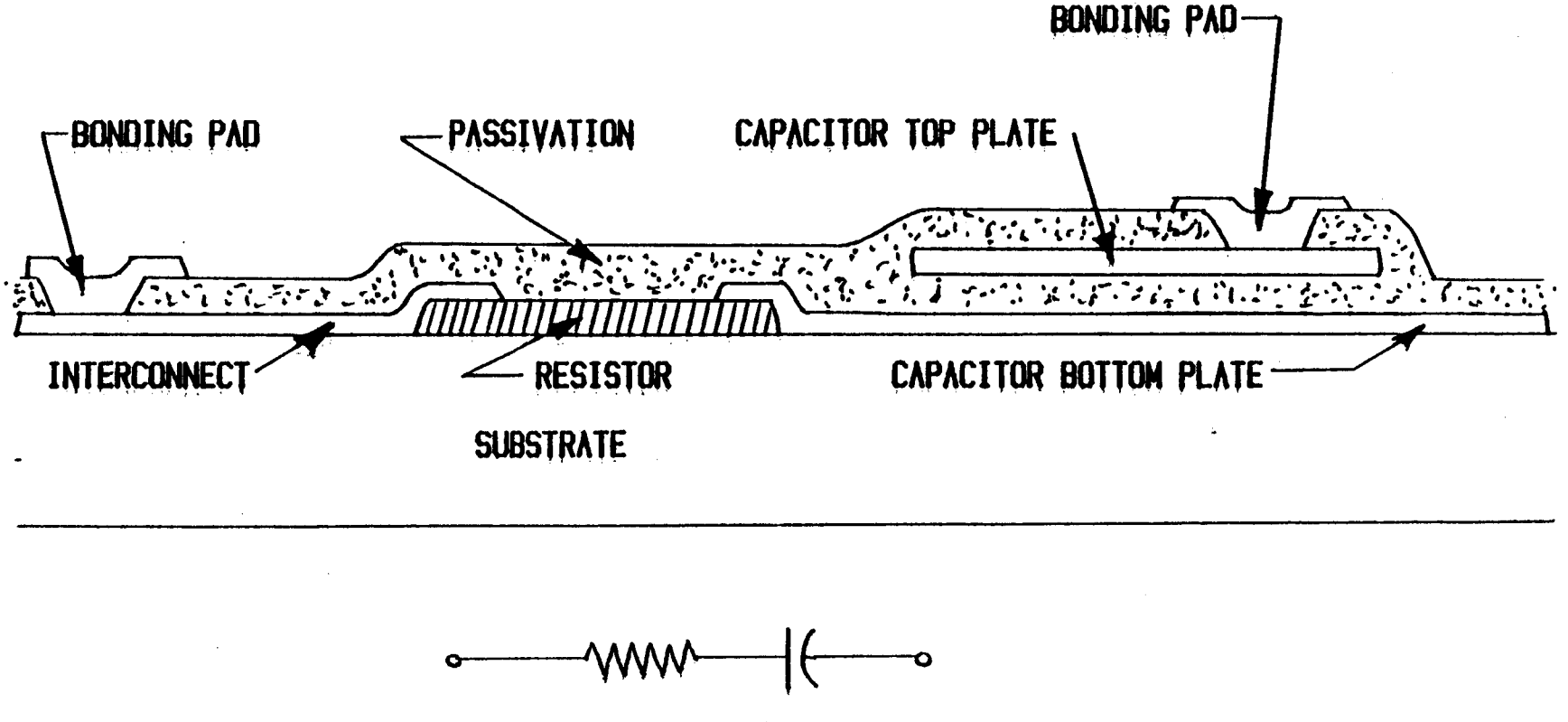


Fig. 2 Cross-sectional View Illustrating the Integration of Components

MATERIALS

INTERCONNECTIONS: TUNGSTEN

DIELECTRIC: SILICON NITRIDE

RESISTORS: TUNGSTEN SILICIDE

PASSIVATION: SILICON NITRIDE
OR SILICON DIOXIDE

Figure 3

RESISTORS

TUNGSTEN - SILICON

TYPICAL RESISTANCE: 100 OHMS TO > 1 MEGOHM

TEMPERATURE COEFFICIENT: < 100 PPM/°C
POSITIVE OR NEGATIVE
PROCESS-CONTROLLABLE

OPERATING TEMPERATURE: 25°C- 500°C

SHEET RESISTANCE: 50 TO 500 OHMS PER SQUARE

Figure 4

CAPACITORS

3-LAYER TUNGSTEN-SILICON NITRIDE-TUNGSTEN

TYPICAL CAPACITANCE (2000 ANGSTROMS): 400 pF/mm^2

TEMPERATURE COEFFICIENT: <±100 PPM/°C

OPERATING TEMPERATURE: 25°C - 500°C

BREKDOWN VOLTAGE: 200 VOLTS (2000 ANGSTROMS)

Q > 100

Figure 5

INTERCONNECTIONS

METAL: TUNGSTEN

TYPICAL RESISTIVITY: 6 MICRO-OHM CM

TYPICAL SHEET RESISTANCE: < 1 OHM PER SQUARE

BONDING PADS AND BONDING WIRES: PLATINUM

Figure 6

PASSIVATION

SILICON NITRIDE OR SILICON DIOXIDE

TYPICAL THICKNESS: 3000 ANGSTROMS

TYPICAL RESISTIVITY: $> 10^8$ AT 500°C

Figure 7

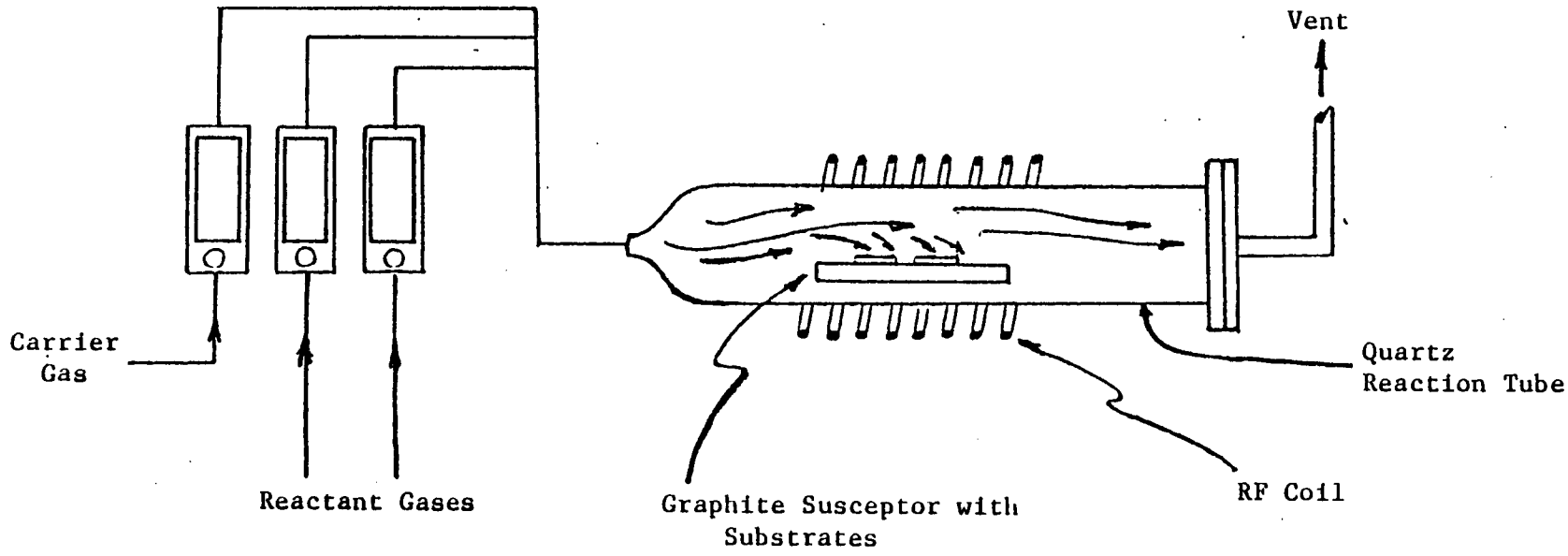


Fig. 8 General Deposition System for Chemical Vapor Deposition

The reactant gases, along with a carrier gas, are introduced into a quartz reaction chamber where they react on the heated substrate surfaces to form the desired materials.

ADVANTAGES OF CVD

HIGH TEMPERATURE PROCESS

AFFORDS CONTROL OF COMPOSITION

PERMITS DEPOSITION OF MANY DIFFERENT MATERIALS

FLEXIBILITY

Figure 9

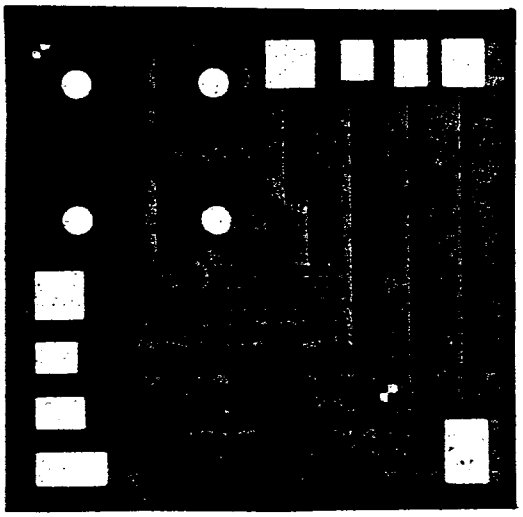


Fig. 10 Resistor Test Chip with Platinum Contacts

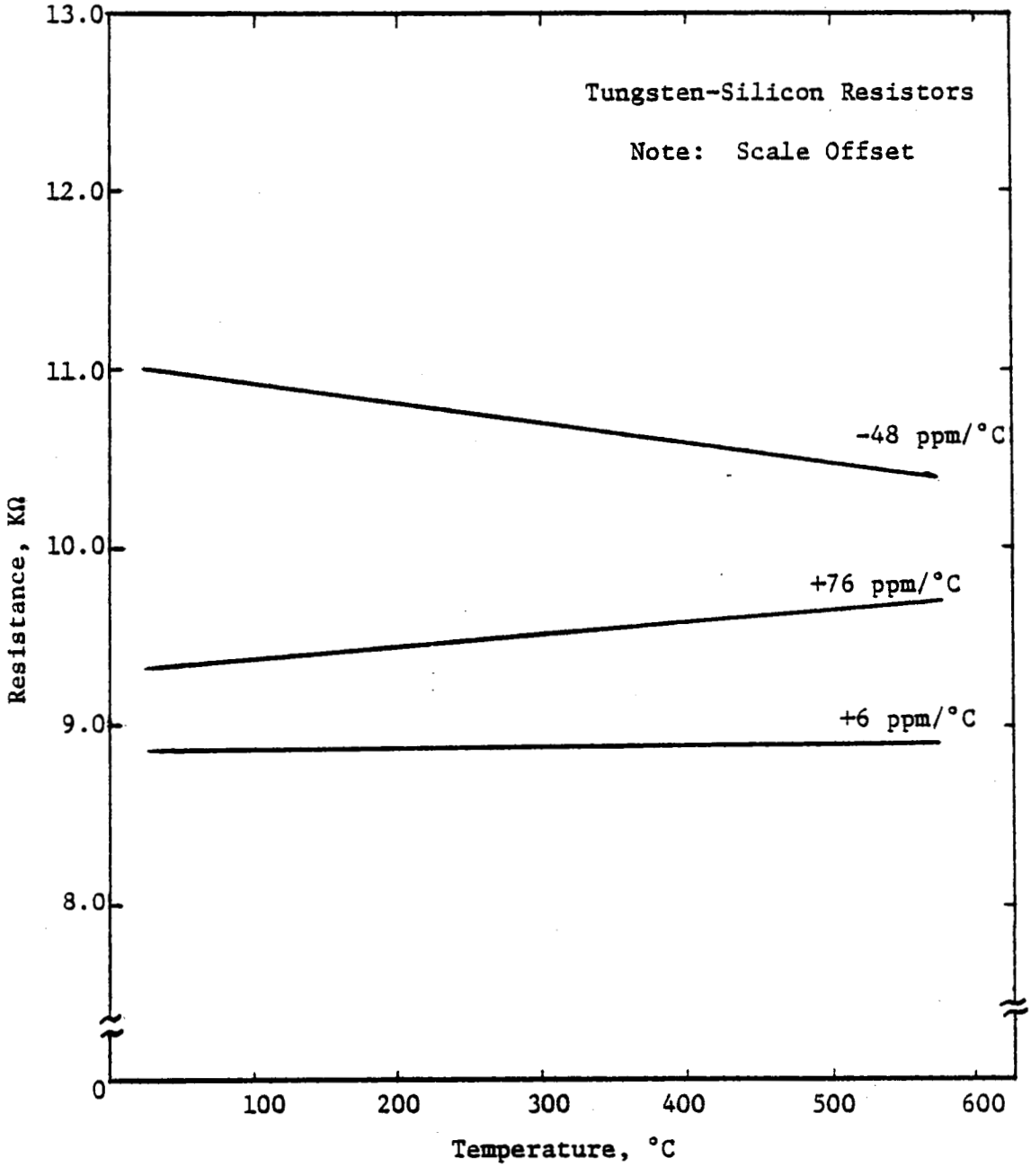


Fig. 11 Resistance versus Temperature for Three Tungsten-Silicon Resistors. Temperature Range of Measurement: 25 to 550°C.

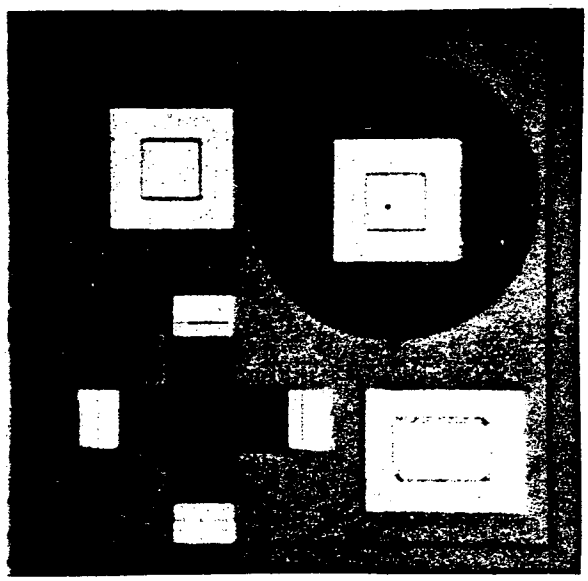


Fig. 12 Capacitor Test Chip with Platinum Contacts

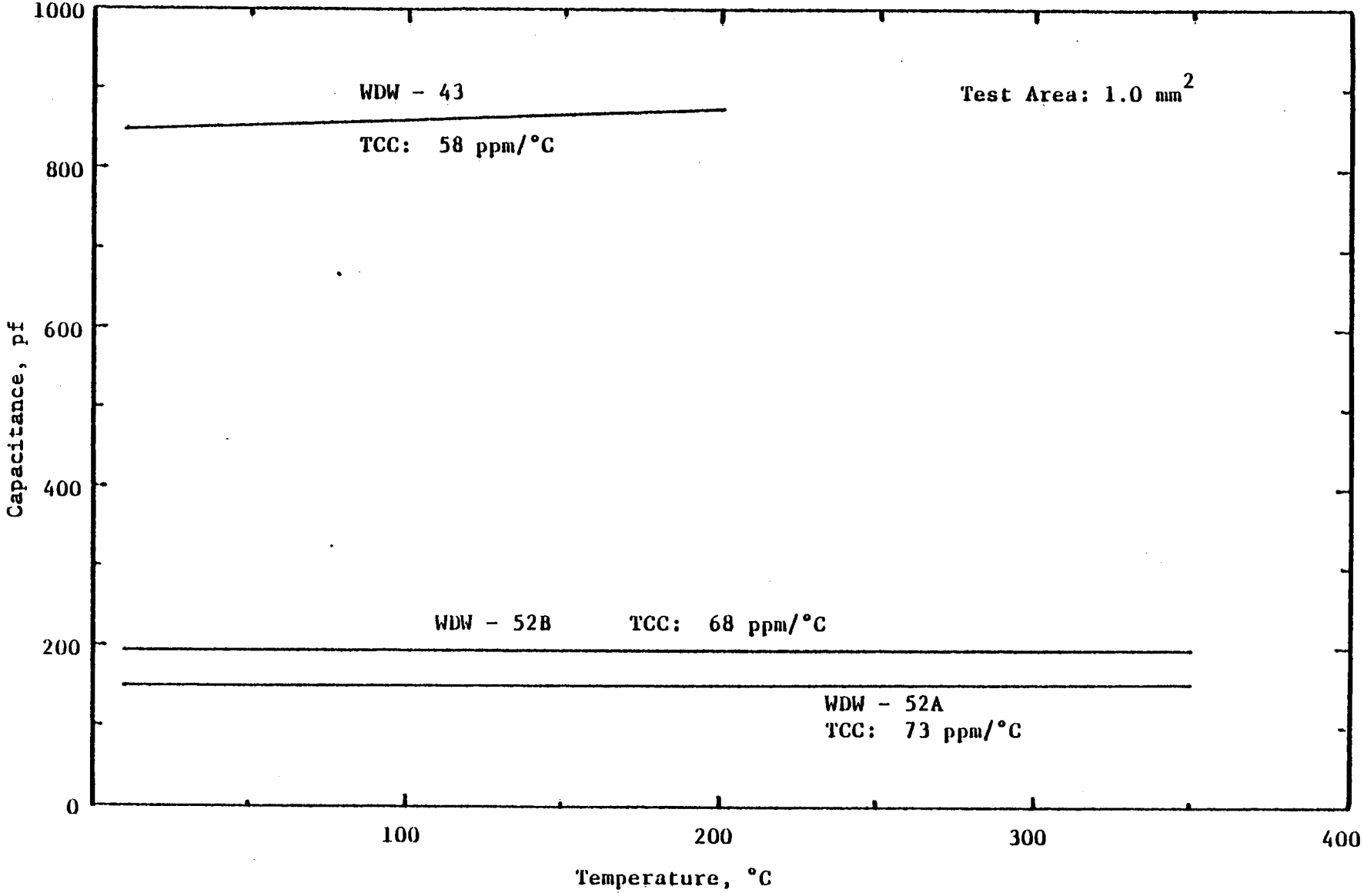


Fig. 12 Capacitance versus Temperature Curves for Three High Temperature Capacitors

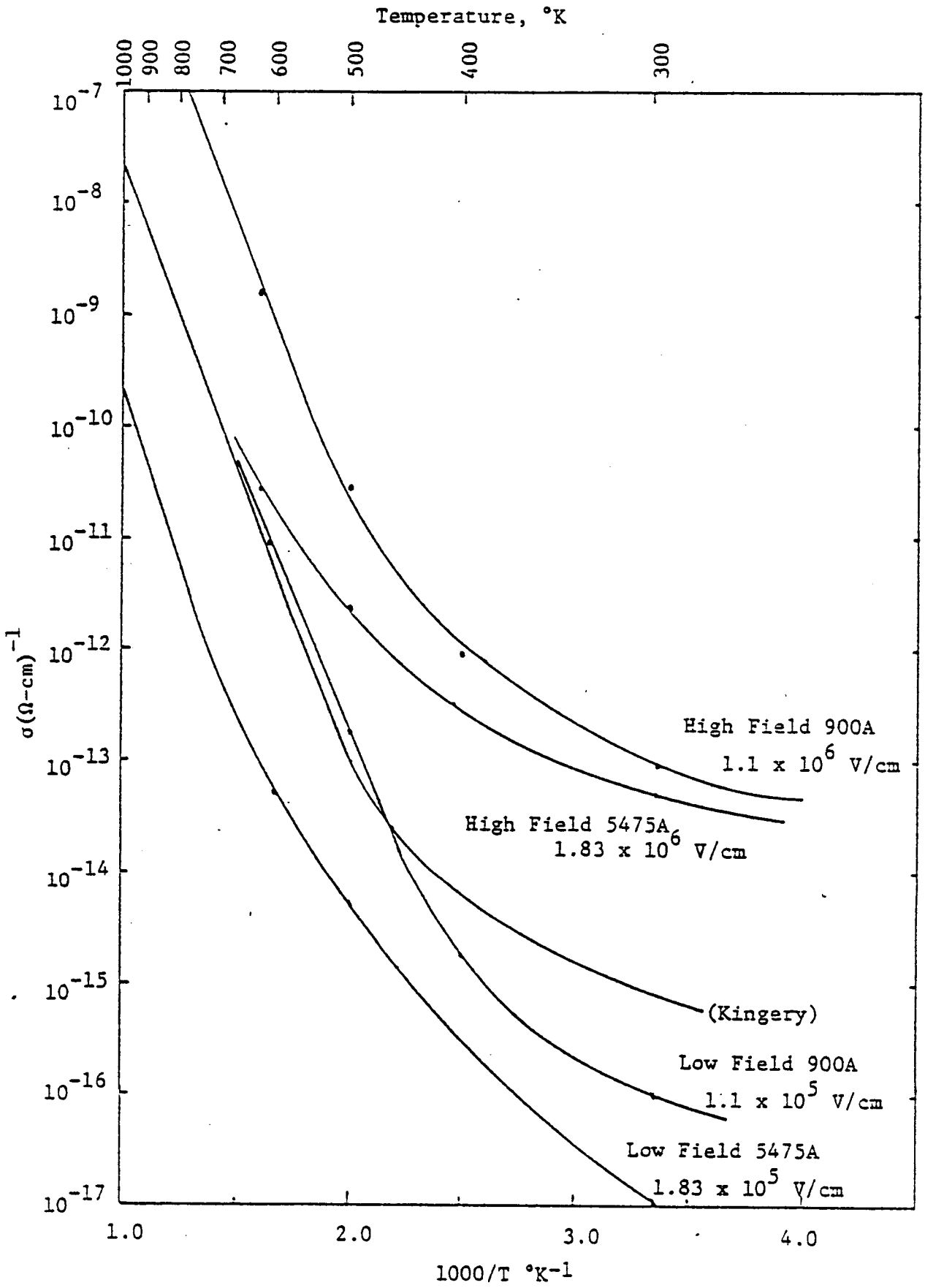


Fig. 14 Conductivity versus Inverse Temperature of the Silicon Nitride Dielectric Layer

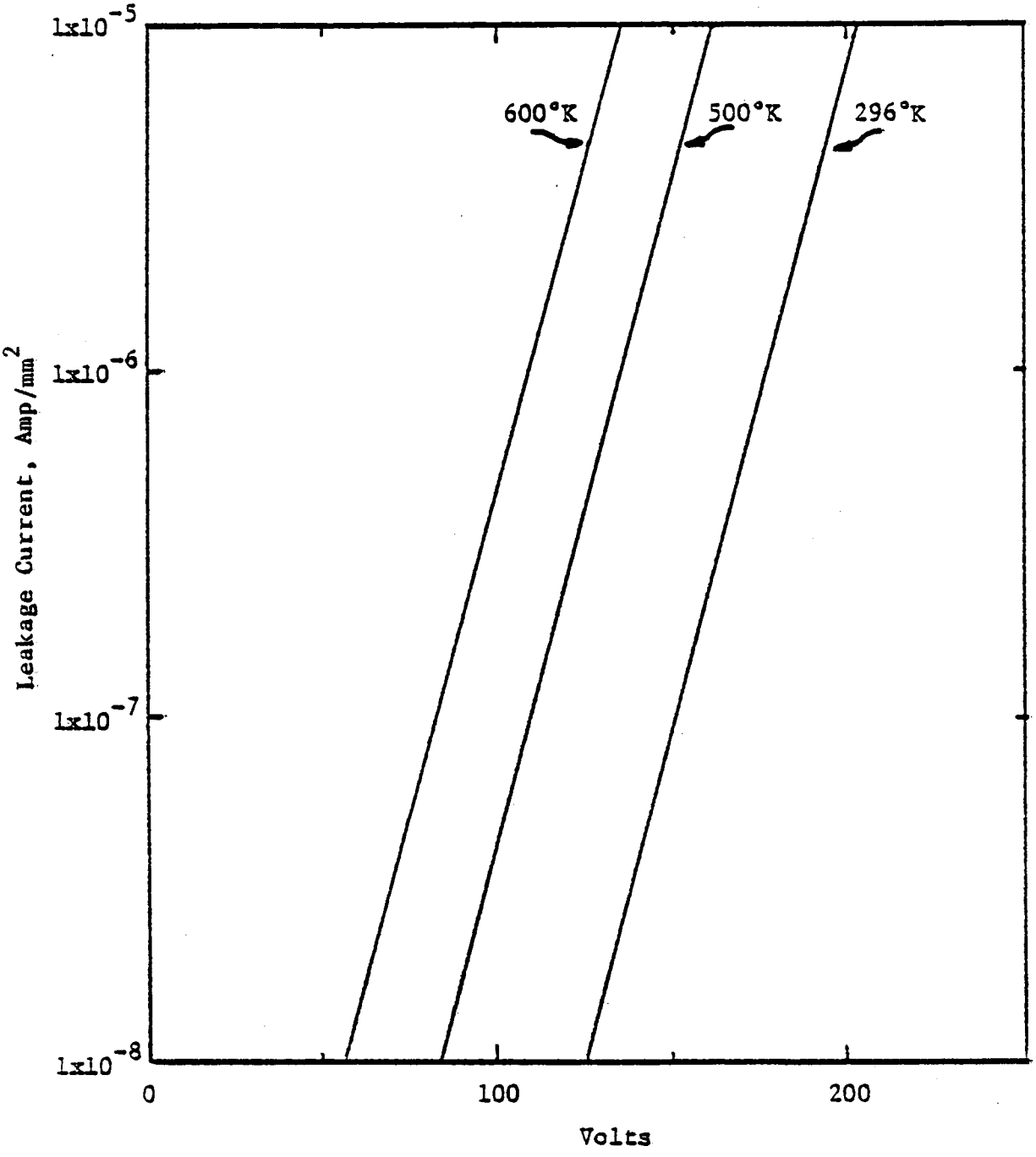
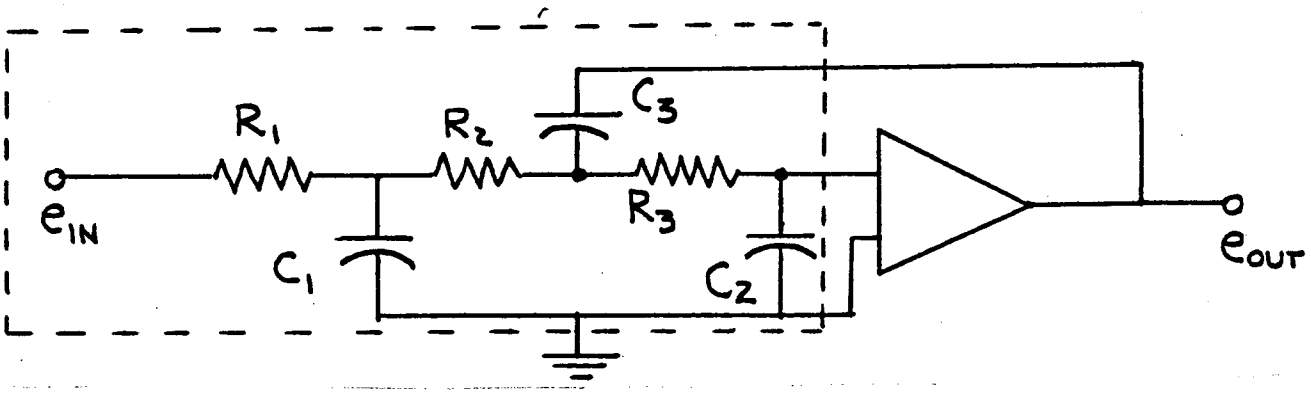


Fig. 13 Capacitor Leakage Current as a Function of Applied Voltage and Temperature

Dielectric: Si_3N_4

Thickness: 5140A

WDW - 52A



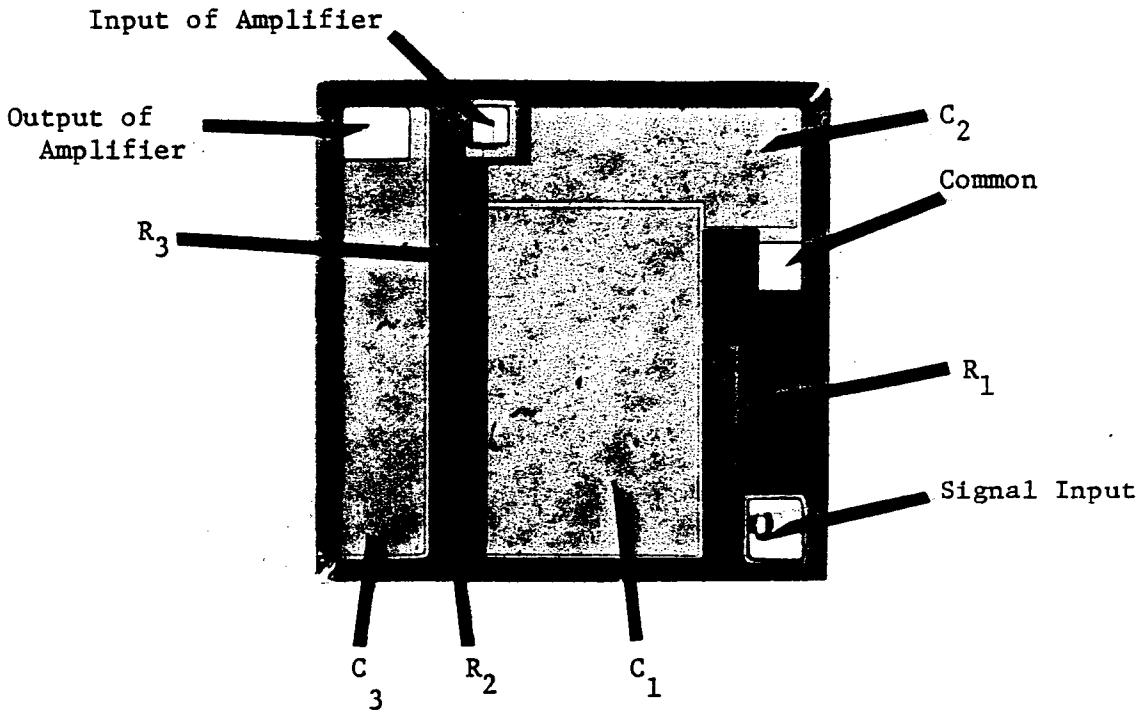


Fig. 16 Third-Order Butterworth RC-Active Filter

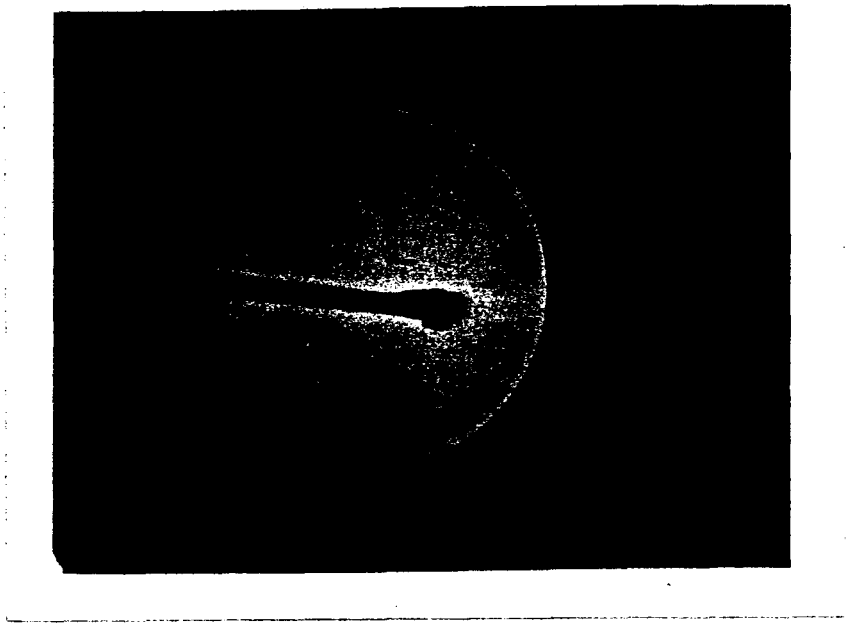


Fig. 17 Platinum Wire Ultrasonically Welded to a Platinum Bonding Pad. Wire diameter is 0.001".

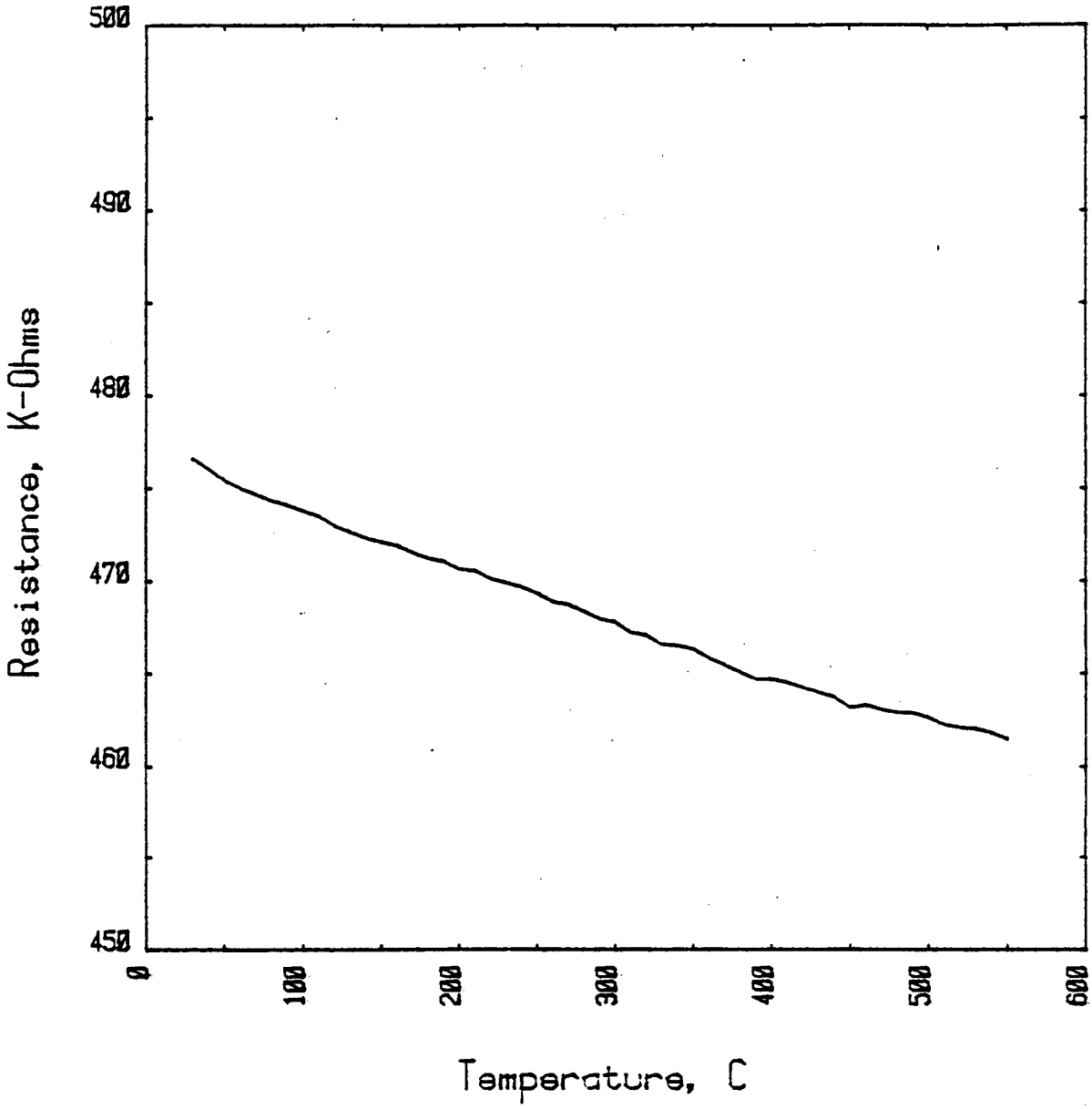


Fig. 18 Output of Data Acquisition System for a Resistance versus Temperature Measurement Cycle

PRELIMINARY

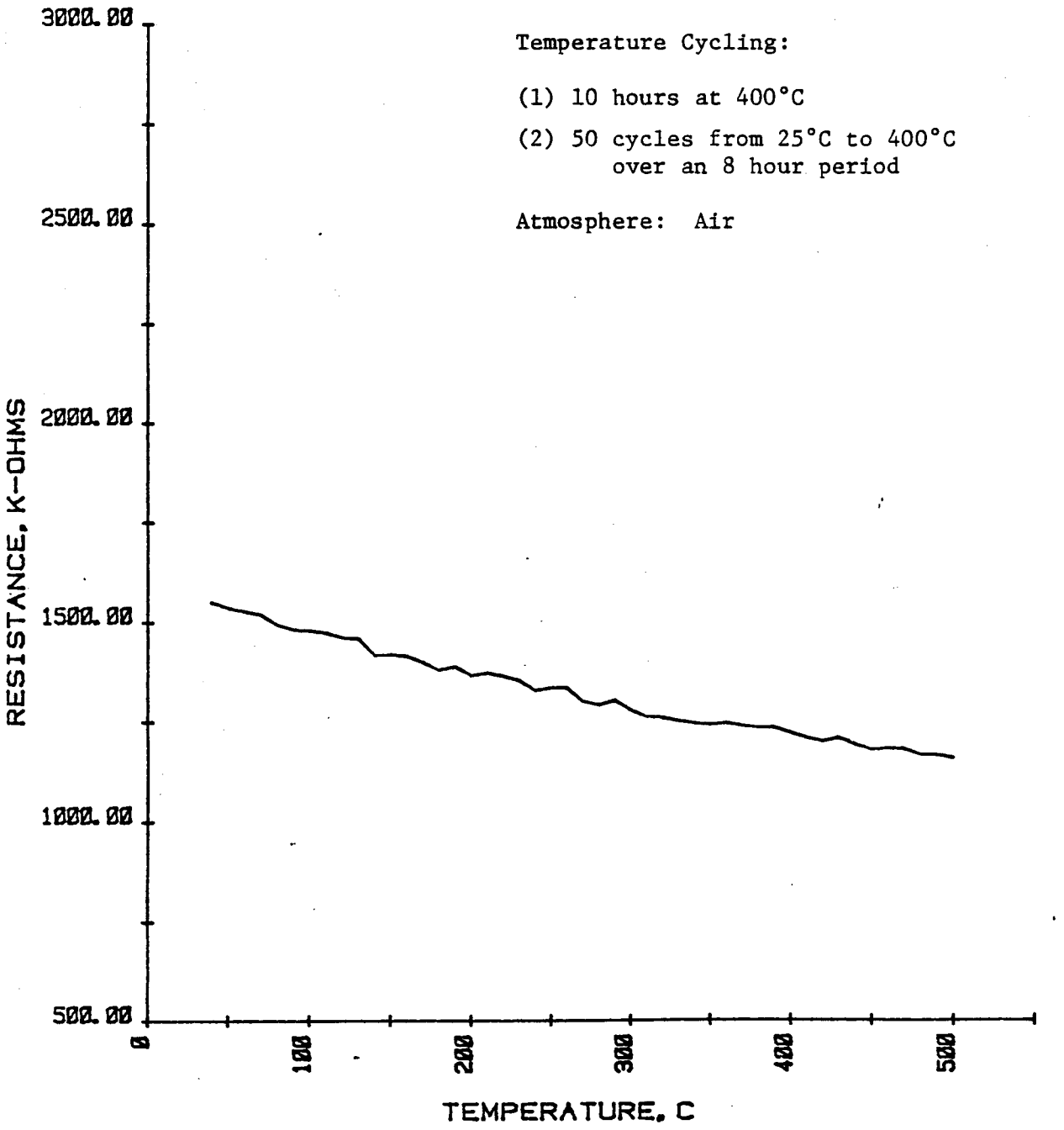
TEMPERATURE CYCLING RESULTS

RESISTOR WAFER
SHEET RESISTANCE: ~5000 OHMS PER SQUARE

INITIAL RESISTANCE	1565.9 K OHMS
AFTER 10 HOURS IN AIR AT 400 °C	1573.4 K OHMS
AFTER 50 CYCLES, 25 °C TO 400 °C, AIR	1569.0 K OHMS

1-MIL LINE WIDTH, 300 SQUARES

Figure 19



WAFER NUMBER : 1
RESISTOR NUMBER : 23
PATTERN : W-Si

MAXIMUM RESISTANCE = 1549500.00 OHMS
MINIMUM RESISTANCE = 1157220.00 OHMS

Fig. 20 Resistance versus Temperature Measured after Temperature Cycling

PASSIVE COMPONENT PARAMETERS

COMPONENT	MATERIAL	RESISTIVITY OHM CM	DIELECTRIC CONSTANT	SHEET RESISTANCE OHMS/	TEMPERATURE COEFFICIENT PPM/ C
RESISTOR	TUNGSTEN-SILICON	1000×10^{-6} TO 2000×10^{-6}		50 TO 1000	$<\pm 100$
CAPACITOR	SILICON NITRIDE		8.6		$<\pm 100$
INTER-CONNECTS	TUNGSTEN	6×10^{-6}		< 1	2900
PASSI-VATION	SILICON NITRIDE OR SILICON DIOXIDE	10^{8} AT 500°C	8.6 3.9		

Figure 21

ESTIMATED BY SEPTEMBER 30

FINISH PRELIMINARY PROCESS CHARACTERIZATION

FINISH PRELIMINARY MATERIAL CHARACTERIZATION AND ANALYSIS

1 MONTH TEMPERATURE CYCLING DATA

1 MONTH HIGH TEMPERATURE LIFE TEST

PRELIMINARY TESTING TO FAILURE

CHIP TO HEADER BONDS

HEADER TO INSTRUMENTATION LEAD BONDS

PASSIVE COMPONENT INTEGRATION PROCESS

Figure 22

VI. INTEGRATION OF PASSIVE COMPONENTS

William J. Kerwin

To illustrate the integration of passive components, we have chosen a third-order Butterworth active-RC filter. The configuration chosen produces a low-pass filter with low sensitivity to gain and to element values, while the Butterworth characteristic produces a maximally-flat amplitude response with frequency. The circuit is shown in Fig. 1; here the element values have been normalized to an impedance level of 1 ohm and a cutoff frequency of 1 radian per second. Only the passive elements are integrated on the chip; the gain block is external. All resistor values have been made equal and the circuit is designed to use an amplifier with a gain of 2. Note that for these conditions there is only a ratio of 2.5:1 between maximum and minimum capacitance values.

These element values can be scaled to any desired impedance level and any desired cutoff frequency. In Fig. 2 the scaling is shown for an impedance level of 10K ohms and a cutoff frequency of 10 KHz. As was described in Section V, this filter has been designed for processing on a 100 x 100 mil chip. However, test chips are not yet available. To verify the design, the filter was constructed from discrete components and a standard operational amplifier, and operated at room temperature. Figure 3 shows the results that were obtained; here the magnitude is normalized to the value at zero frequency. Note that the cutoff frequency is 10 KHz and the magnitude falls off at 60 dB per decade, as anticipated.

In anticipation of the possible use of the filter with an integrated thermionic circuit as a gain element, we have also simulated the ITC by using discrete ceramic triodes and discrete resistors. The circuit for the gain-of-2 amplifier is shown in Fig. 4; this circuit has been operated at 300°C for one week. When filter chips are available for testing, these will be combined with the amplifier circuit as shown in Fig. 5.

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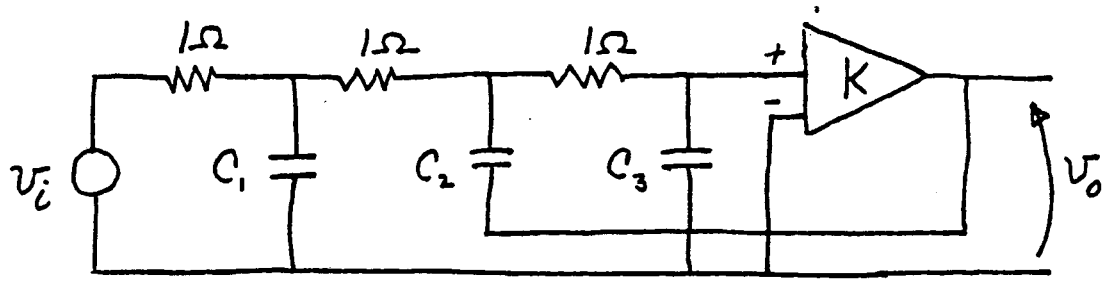

$$\frac{v_o}{v_i} = T(p) = \frac{K}{C_1C_2C_3p^3 + [2C_3(C_1+C_2) + C_1C_2(1-K)]p^2 + [C_1 + 3C_3 + 2C_2(1-K)]p + 1}$$

BUTTERWORTH 3rd ORDER $\quad T(p) = \dfrac{K}{p^3 + 2p^2 + 2p + 1}$

FOR $K = 2$

$$\begin{aligned} C_1C_2C_3 &= 1 \\ 2C_3(C_1+C_2) - C_1C_2 &= 2 \\ C_1 + 3C_3 - 2C_2 &= 2 \end{aligned} \quad \Longrightarrow \quad \begin{aligned} C_1 &= 1.7058\ F \\ C_2 &= 0.8671\ F \\ C_3 &= 0.6761\ F \end{aligned}$$

ACTIVE RC 3RD ORDER BUTTERWORTH FILTER

Figure 1

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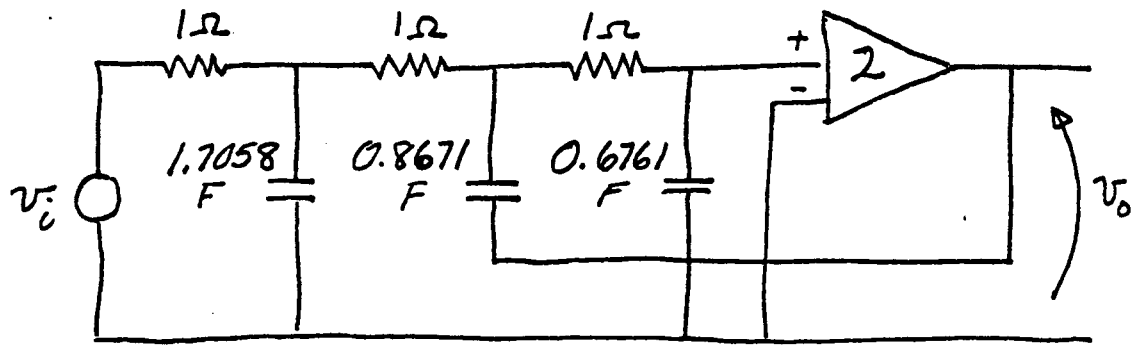
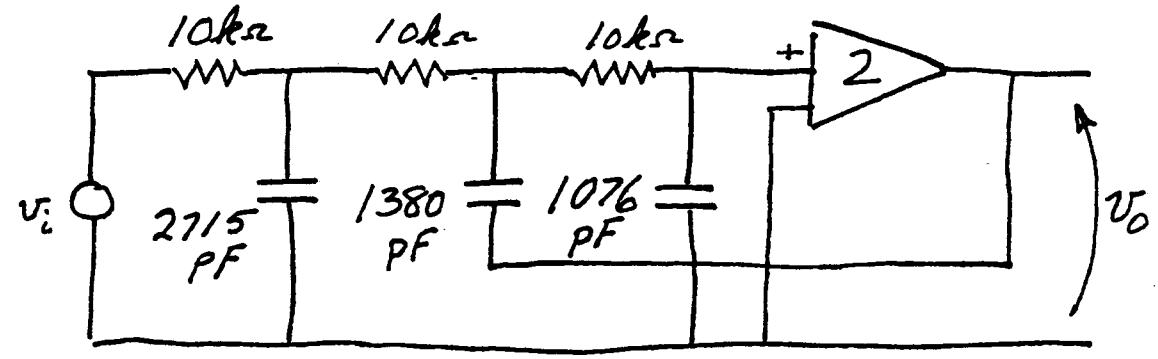


SCALING TO $R = 10k\Omega$

$f_{-3dB} = 10kHz$



FINAL 3RD ORDER FILTER DESIGN

Figure 2

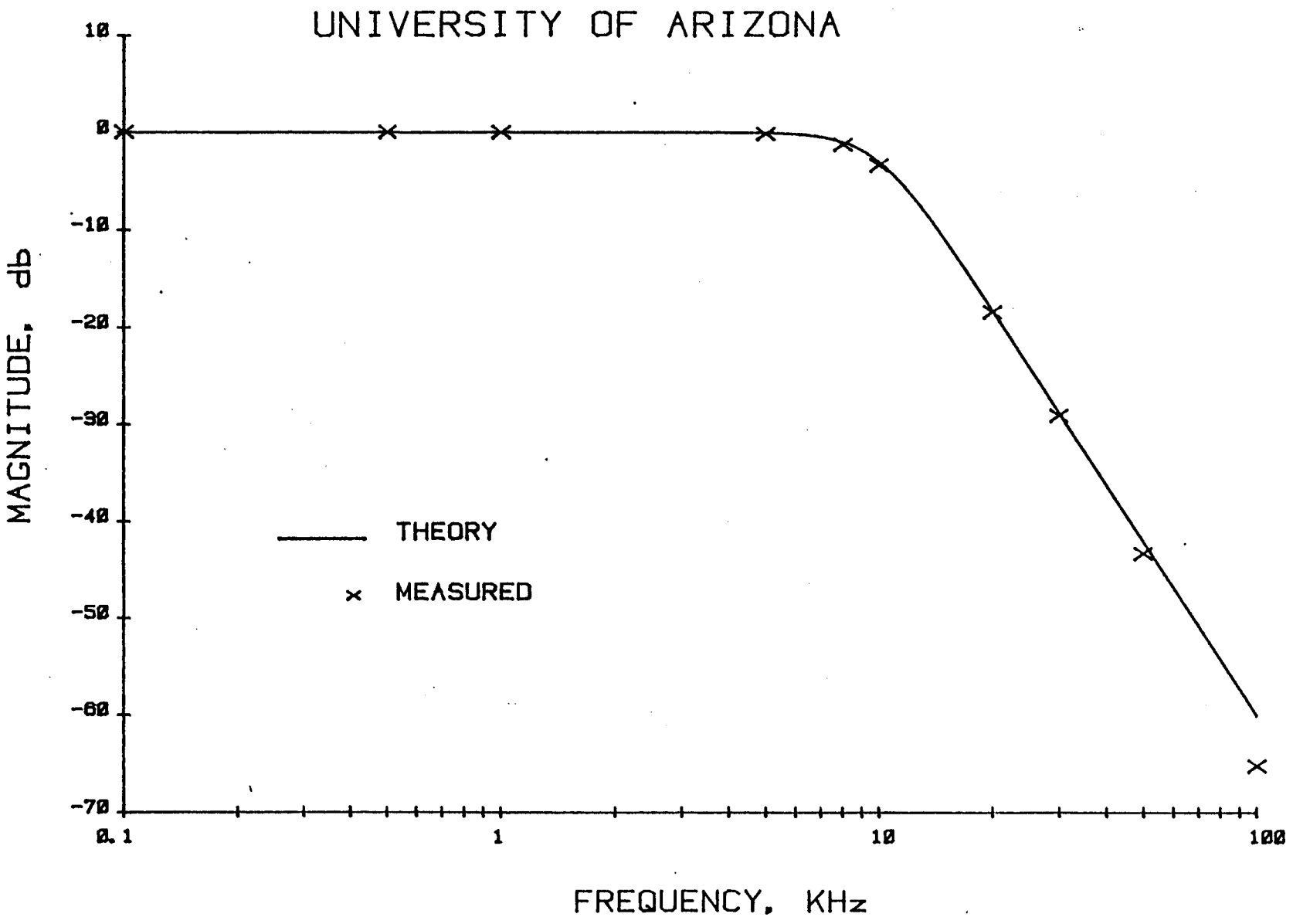

UNIVERSITY OF ARIZONA
10
0
-10
-20
-30
-40
-50
-60
-70
MAGNITUDE, db
THEORY
MEASURED
0.1
1
10
100
FREQUENCY, KHz
3RD ORDER BUTTERWORTH FILTER

Figure 3

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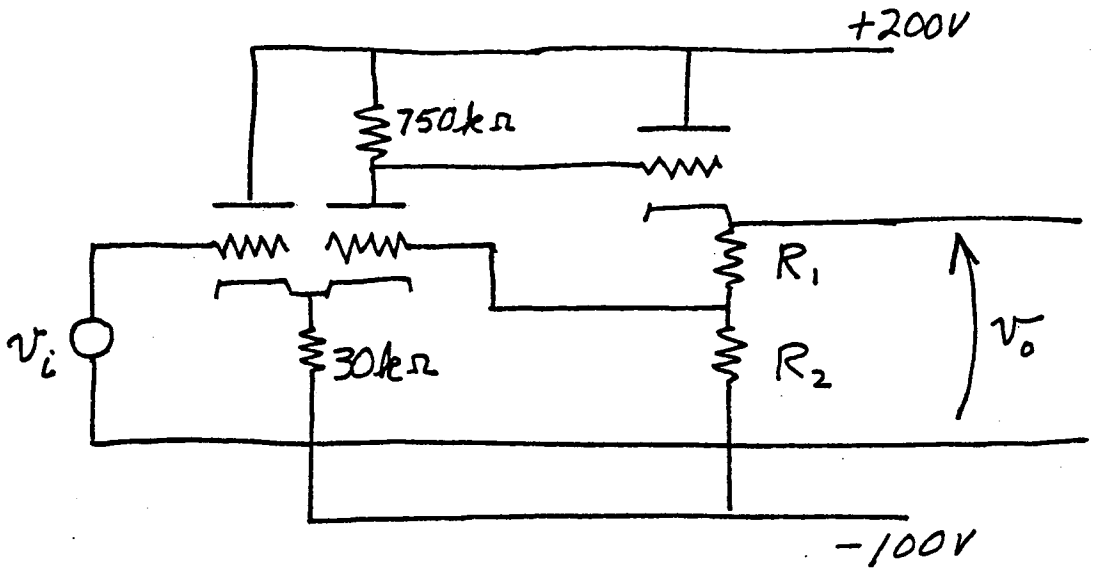

CERAMIC TRIODES TYPE 7552

FOR $R_1 = R_2 = 100k\Omega$

$$\frac{v_o}{v_i} = \frac{A}{1+A\beta} = \frac{(0.92)(0.88)(70)}{1+(56.7)(\frac{1}{2})} = 1.93$$

FOR $R_1 = 100k\Omega$, $R_2 = 93k\Omega$

$$\frac{v_o}{v_i} = \frac{56.7}{1+56.7(0.482)} = 2.00$$

ITC OPERATIONAL AMPLIFIER

Figure 4

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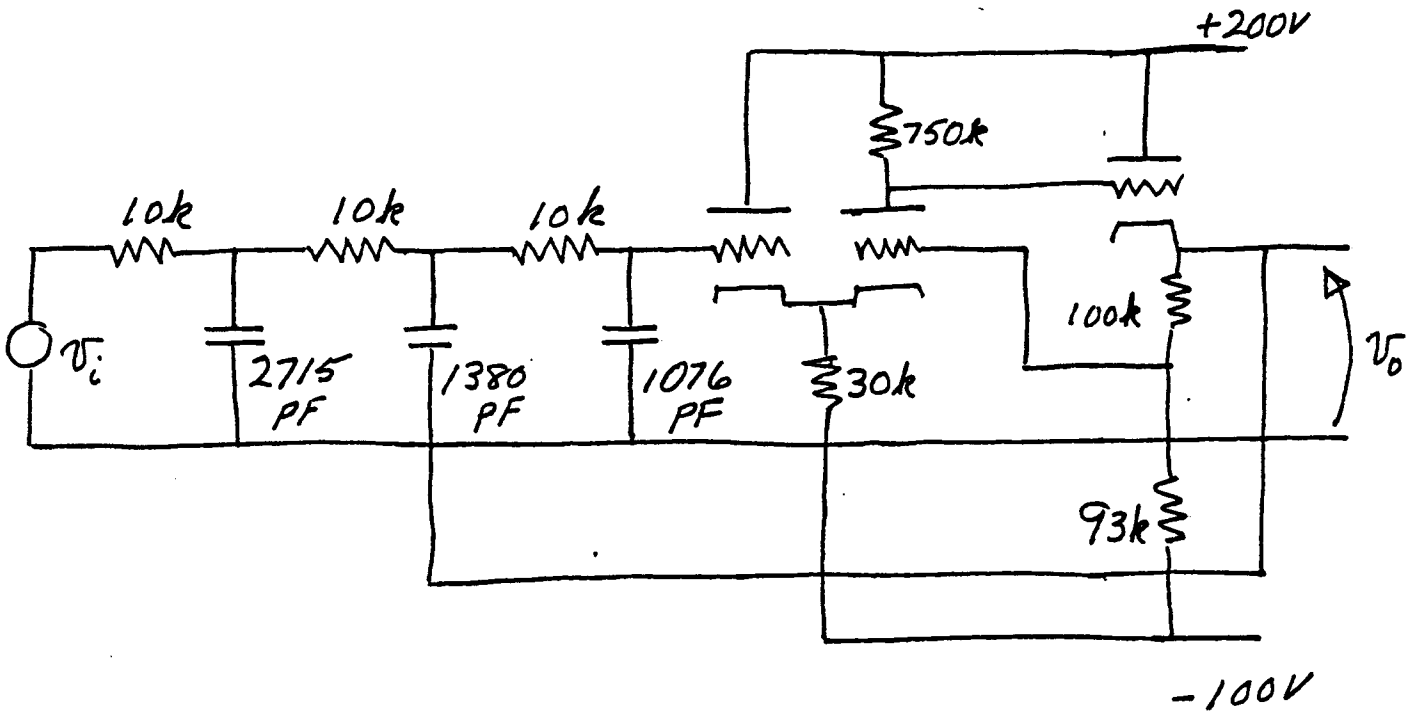

COMPLETE FILTER CIRCUIT

Figure 5

VII. DISCUSSION

A. Future Work - Douglas J. Hamilton

B. Comments - Discussion by Participants

A. Future Work

Professor Douglas J. Hamilton, The University of Arizona

We feel that future work in the area of passive components should have as its broad objectives the refinement of the technology, and the fabrication of samples for evaluation for potential application in down-hole instrumentation. To this end, we believe that the four general categories of effort shown in Fig. VII-1 should be pursued.

As is shown in Fig. VII-2, Process Optimization includes the development of design charts which would enable the designer to select the process parameters required to fabricate components for a given set of specifications. Process uniformity and repeatability need to be established. The process for integrating passive components needs to be optimized, and some attention given to the fabrication of crossovers, since these are certain to be necessary as circuit complexity increases. Finally, reliability studies must be conducted by cycling and long-term life testing of components at elevated temperatures. Such studies would allow a failure model to be evolved; they would also provide samples which have been "burned-in" at high temperatures. These samples would then be sent to various users for their evaluation.

To advance the technology for passive components, three areas of work are proposed, as is shown in Fig. VII-3; these all are directed toward the implementation of technology transfer. Since much chemical vapor deposition in the semiconductor industry is being done by the hot-wall method and since semiconductor companies are likely to be the manufacturers of well-logging components, some effort should be devoted to adapting our processes to hot-wall CVD. This is likely to require expensive equipment.

Because the integrated thermionic devices are now being made by an electron-beam evaporation process, we feel that some effort should be given to adapting the passive component process to E-beam evaporation. Again, this is likely to require expensive equipment.

In the area of advancing the materials technology, we feel that molybdenum and molybdenum-silicon should be investigated for interconnections and resistors. Again, this has to do with technology transfer. The ITC devices use molybdenum for metallization; if passive components using Mo and Mo-Si can be developed with performance similar to those using W and W-Si, compatibility with ITC devices will be greatly increased.

Methods of making large-value capacitors, including the use of multilayer structures, should be investigated. Such capacitors would be very useful in hybrid circuits even if their maximum temperature were only 350°C.

Finally, upper limits on the operating temperature range of components should be investigated. Here the main thrust should be for resistors, since it is unlikely that a dielectric material for capacitors can be found which is satisfactory above 600°C. For resistors, if the deposition can be done at temperatures of the order of 1000°C, it may be possible to obtain resistors which would operate as high as 800°C. These would be important in integrated thermionic circuits since they could then be placed on the same substrate as the active devices.

In order to achieve the goal of functional electronic circuits operating down-hole, it will be necessary to integrate the passive components with active devices as is shown in Fig. VII-4. As far as integration with discrete components and hybrid circuits is concerned, the principal problems are expected to be bonding and packaging. We have already worked out wire

bonding techniques using ultrasonic bonding of platinum wires, and a Sandia package is available which can be used up to 450°C. Our samples in chip form and in packages need now to be evaluated by users.

Since the MOS process is probably the most promising candidate for producing semiconductor devices that can operate up to 300°C, some attention should be given to integrating our passive components with MOS devices. We have already made some progress in this direction through a small contract funded by Sandia Laboratories to fabricate test structures using CVD tungsten as gate metal.

The integration of passive components with integrated thermionic structures should also be investigated, as previously discussed, to see what process compatibility problems arise. The ITC devices are the most promising candidates for operation above 500°C, so their integration with passive components should be investigated as part of the long-term goals of geothermal instrumentation research.

Finally, some attention to the circuit design involving use of passive and active devices should be initiated. Design rules need to be developed, and some specific circuits investigated.

A final area, which may be considered exploratory, is the investigation of transducers for logging tools. We feel that in particular our process has the potential for producing two types of transducers: temperature and pressure. Both would use the tungsten-silicon CVD process. Because our resistors have exhibited very stable characteristics with no hysteresis with temperature, we feel that resistors deliberately fabricated with high temperature coefficient could be used as temperature sensors. This should be investigated.

One of the principal problems with strain gauges has always been their temperature dependence. Since we can fabricate W-Si resistors with temperature coefficients of a few parts per million per degree, we feel that the strain properties of these resistors should be investigated. If the strain properties are acceptable, a pressure cell could be designed by using a thin diaphragm of some material such as silicon on which have been deposited W-Si resistors.

B. Comments

Discussion by Participants

Following the presentation of the proposed directions for future work by The University of Arizona, the meeting was opened for informal discussion by workshop participants. The discussion was initiated by a request that participants comment on the proposed future work. Professor Hamilton had pointed out in his presentation that there was considerably more work needing to be done than could be handled under anticipated staff and budget limitations, and he had suggested priorities. He now requested suggestions from participants regarding these. There was not much discussion, and upon further questioning by Prof. Hamilton it was determined that there was general agreement among the participants on the proposed directions and priorities.

The discussion then turned to some of the more specific requirements foreseen by participants. Mr. Lyman Edwards of Dresser Industries pointed out that there is an urgent need by both NSF and DOE for a high-temperature pressure transducer. Present geothermal applications need a device for 3000 psi at temperatures up to 300°C. Within four to five years the magma geothermal program will need transducers that can operate in the 300°C to 1000°C range at pressures up to 20,000 psi. Oil wells also need transducers for 20,000 psi at 250°C - 300°C. Typical pressure transducers should have a sensitivity of one part in 20,000, be stable over a 15 minute to 1 hour period, have down-hole amplification, provide 5 volts full-scale output, and be capable of driving five miles of cable.

Mr. Edwards also noted that high temperature instrumentation, particularly pressure and temperature measurements, are needed for coal

gasification and liquefaction. These applications require circuits which can operate in the 500°C - 1000°C range. NASA Venus probes require high-temperature instrumentation as does the proposed NASA project for converting solar energy at a satellite to microwave energy.

With regard to filters, Mr. Edwards indicated that signal-to-noise ratio problems often determine filter needs. There are some requirements for low-pass filters with fractional-Hertz cutoff frequencies that can operate at 300-500°C.

Finally, Mr. Edwards noted that there is a need for a radiation detector of the scintillation-counter type that can operate up to 1000°C.

Mr. Sloughter of Wellex described some of their circuit needs. They would like an amplifier with open-loop gain of 10^4, bandwidth 5 Hz or better, to operate from 0°C - 350°C. Also they need an A/D converter, 12 bits, 5 volts full scale, for the same temperature range. Eventually they would like to have a microprocessor down-hole, and a line-driver so that signals would be sent in digital form to the surface.

Dr. DeLorenzo of Oak Ridge Laboratory noted that while he is not involved in well-logging, he has a number of high-temperature requirements. In many cases his instrumentation must also withstand a high radiation environment. He has requirements for transducers which can produce wireless data output. One method is to use temperature and pressure transducers, amplify the signals at the site and drive acoustic transducers for acoustic transmission of the data. Such instrumentation must operate in the 300°C - 700°C temperature range and withstand a total radiation dose of 10^{18} rads per year. Pressure transducers for 10-200 psi are needed. A differential pressure transducer for measuring sodium flow is also needed. This device

must be capable of measuring a 10-15 psi differential pressure across a venturi. Small size is also a requirement, and stability is important.

Dr. DeLorenzo also noted that he has a need for capacitors with capacitance in the range 0.1 - 2 microfarad to operate at 50 volts in a 300°C environment with no radiation.

Mr. McBrayer of Sandia indicated that The University of Arizona capacitors were of particular interest to Sandia. He felt that inteconnections would be a problem, and mentioned the need for bonding to Dupont inks. Dr. McCormick of LASL commented that they have successfully done wirebonding of platinum wire to both nickel and molybdenum; thus he felt that interconnection would not be too difficult.

Mr. Burnett of Sandia noted that Sandia is not interested in developing new technologies but rather in adapting existing technologies for operation up to 300°C. He also noted that Sandia is not presently interested in temperatures above 300°C because present geothermal wells require only 300°C instrumentation and also because there are other major materials problems which impose limitations at 300°C. Examples of these are cables and seals.

FUTURE WORK

I. PROCESS OPTIMIZATION

II. ADVANCED TECHNOLOGY
(Processing and Materials)

III. INTEGRATION WITH ACTIVE DEVICES

IV. TRANSDUCERS

Figure VII-1

I. PROCESS OPTIMIZATION - PRESENT PROCESS

A. PARAMETER CONTROL
Development of design curves for processing: deposition times, temperatures, etc., related to thickness, sheet resistance.

B. FILM THICKNESS, SHEET RESISTACE, TEMPERATURE COEFFICIENT
Design curves for components

C. PROCESS UNIFORMITY, REPEATIBILITY

D. PROCESS OPTIMIZATION FOR INTEGRATION
Compatibility, simplicity
Crossovers

E. RELIABILITY STUDIES
Cycling
Long term life testing

Figure VII-2

II. ADVANCED TECHNOLOGY

A. PROCESSING

1. Hot-wall CVD
2. E-Beam processes

B. MATERIALS

1. Molybdenum metallization
2. Mo-Si resistors
3. Capacitor structures
   - Large-value capacitors
   - Multi-layer structures

C. INCREASED OPERATING TEMPERATURE RANGE

Figure VII-3

III. INTEGRATION WITH ACTIVE DEVICES

A. DISCRETE COMPONENTS

Vacuum tubes
Semiconductor devices
Interconnections with discrete passives

B. HYBRIDS

Same interface problems as with discretes

C. FULL INTEGRATION WITH MOS STRUCTURES

Process compatibility

D. FULL INTEGRATION WITH ITC STRUCTURES

Process compatibility

E. CIRCUIT DESIGN

Use of passives with active devices
for filters, functional blocks.

Figure VII-4

IV. TRANSDUCERS

A. TEMPERATURE SENSORS

High TCR resistors

B. PRESSURE TRANSDUCERS

Investigate properties of low-TCR resistors as strain sensors

Figure VII-5

VIII. LIST OF PARTICIPANTS

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