345/80
1-10-80

MASTER

Q, 551

DSE-3412-T1 1495

PHOTOVOLTAIC MECHANISMS IN POLYCRYSTALLINE THIN-FILM SOLAR CELLS

Quarterly Technical Progress Report No. 1, September 27—December 27, 1978

By
K. Zanio

June 1979

Work Performed Under Contract No. ET-78-C-01-3412

Hughes Research Laboratories
Malibu, California

U.S. Department of Energy

Solar Energy

DISCLAIMER

Available from the National Technical Information Service, U. S. Department of Commerce, Springfield, Virginia 22161.

Price: Paper Copy $4.50
Microfiche $3.00

DSE-3412-T1 1495
Distribution Category UC-63e

PHOTOVOLTAIC MECHANISMS IN POLYCRYSTALLINE THIN-FILM SOLAR CELLS

Quarterly Technical Progress Report No. 1

For period 27 September 1978 through 27 December 1978

K. Zanio

June 1979

Contract ET-78-C-01-3412

Prepared for

DEPARTMENT OF ENERGY
Division of Distributed Solar Technology
Photovoltaic Program Office
Golden, CO 80401

Hughes Research Laboratories
3011 Malibu Canyon Road
Malibu, CA 90265

TABLE OF CONTENTS

ABSTRACT

Preliminary studies were initiated to examine and alleviate the deleterious effect of grain boundaries in solar cells fabricated from InP. The planar reactive deposition system was modified so that the InP substrate temperature could be reduced below the single crystalline to polycrystalline transition temperature and the effects of grain boundaries on p-n junctions can be more readily and reproducibly separated out. A model for grain boundaries intersecting a p-n junction was introduced. In the model, the grain boundary is treated as a two-dimensional array of lower bandgap material which enhances the leakage current at the p-n junction. The effect of various etchants on grain boundaries in InP was also examined as a preliminary step toward passivating the grain boundaries. An anodic oxide and InGaP, both candidates as passivation layers, were deposited on single-crystal InP.

FOREWORD

This report was prepared by Dr. Kenneth Zanio of the Hughes Research Laboratories (Malibu, California), a division of Hughes Aircraft Company, for the Photovoltaic Branch of the Division of Solar Energy of DOE under Contract ET-78-C-01-3412. The technical monitor was Dr. Kim Mitchell at SERI in Golden, Colorado.

The program is being undertaken by personnel in the Chemical Physics Department under the supervision of Dr. R. Knechtli, Dr. G.S. Picus, Mr. M. Braunstein, and Dr. E. Rudisill. The program manager and principal investigator is Dr. Zanio. Important contributions to the program were made by Dr. L. Fraas, presently with Chevron Research, and are being made by Messrs. F. Krajenbrink, R. Turk, P. Hoberg, and H. Montano.

SECTION 1

INTRODUCTION

Polycrystalline solar cells are generally less efficient than are single-crystal cells because of the adverse effect of grain boundaries. Consequently, several programs have been initiated by the Department of Energy (DOE) to understand and control the electrical properties of grain boundaries in semiconductors. This report summarizes efforts at Hughes Research Laboratories (HRL) for the first quarter under DOE Contract ET-78-C-01-3412 using the InP/CdS heterojunction system as a vehicle to study grain boundaries in polycrystalline solar cells. An initial step in these efforts included establishing the effect that grain boundaries have on solar cell performance. Section 2 discusses the studies we have begun towards separating out grain boundary effects from bulk effects. These studies should be helpful in establishing a tentative grain boundary model such as described in Section 3. Adequate performance from polycrystalline cells, especially in the III-V systems, will most likely require some degree of grain boundary passivation. We anticipate that our model will provide some guidance. Results from our preliminary passivation studies are presented in Section 4. The final objective of this program is to use these passivation techniques to improve the efficiency of polycrystalline InP/CdS cells. This is a longer range objective and work in this area has not yet begun. Our plans for achieving this objective are summarized in Section 5.

SECTION 2

ISOLATION OF GRAIN BOUNDARY EFFECTS

The presence of grain boundaries on the III-V systems has the effect of increasing the leakage current and consequently of reducing the open-circuit voltage V_{oc}. In the InP/CdS system, the Bell Laboratories group[1] achieved significantly higher open-circuit voltages in their single-crystal system than in their polycrystalline system. Slightly but not significantly higher short-circuit currents were obtained in the single-crystal system. In an earlier contract[2] supported by DOE to investigate the InP/CdS system, our preliminary results were in general agreement. Unfortunately, the single-crystal and polycrystalline cells were prepared under different conditions and therefore a direct comparison between the parameters in single-crystal and polycrystalline solar cells was not justified to separate out the effects of grain boundaries. For example, at Bell Laboratories, the InP for the single-crystal cells was grown from the melt, but the InP for the polycrystalline cells was grown from the vapor. Although we used the same planar reactive deposition (PRD) process to prepare both single-crystal and polycrystalline light-absorbing InP layers, the surfaces of the InP single-crystal substrates were not reproducible. Since then we have improved our processing procedures and are able to prepare single-crystal InP at substrate temperatures as low as 320°C. We intend to prepare polycrystalline InP on clean InP single-crystal substrates by lowering the substrate temperature (Figure 1). Subsequently, we will deposit an n-type film under identical conditions (i.e., similar temperatures and the same pump down) onto the p-type single-crystal and polycrystalline films. The difference between the current-voltage (I-V) characteristics of the single-crystal and polycrystalline diodes should reflect the effect of the grain boundaries.

Under this program, we have begun to lower the substrate temperature to obtain polycrystalline films. We have found that, for the InP substrate at and above 320°C, we obtained single-crystal epitaxy. These results (Table 1) agree with the work of Farrow, who found the

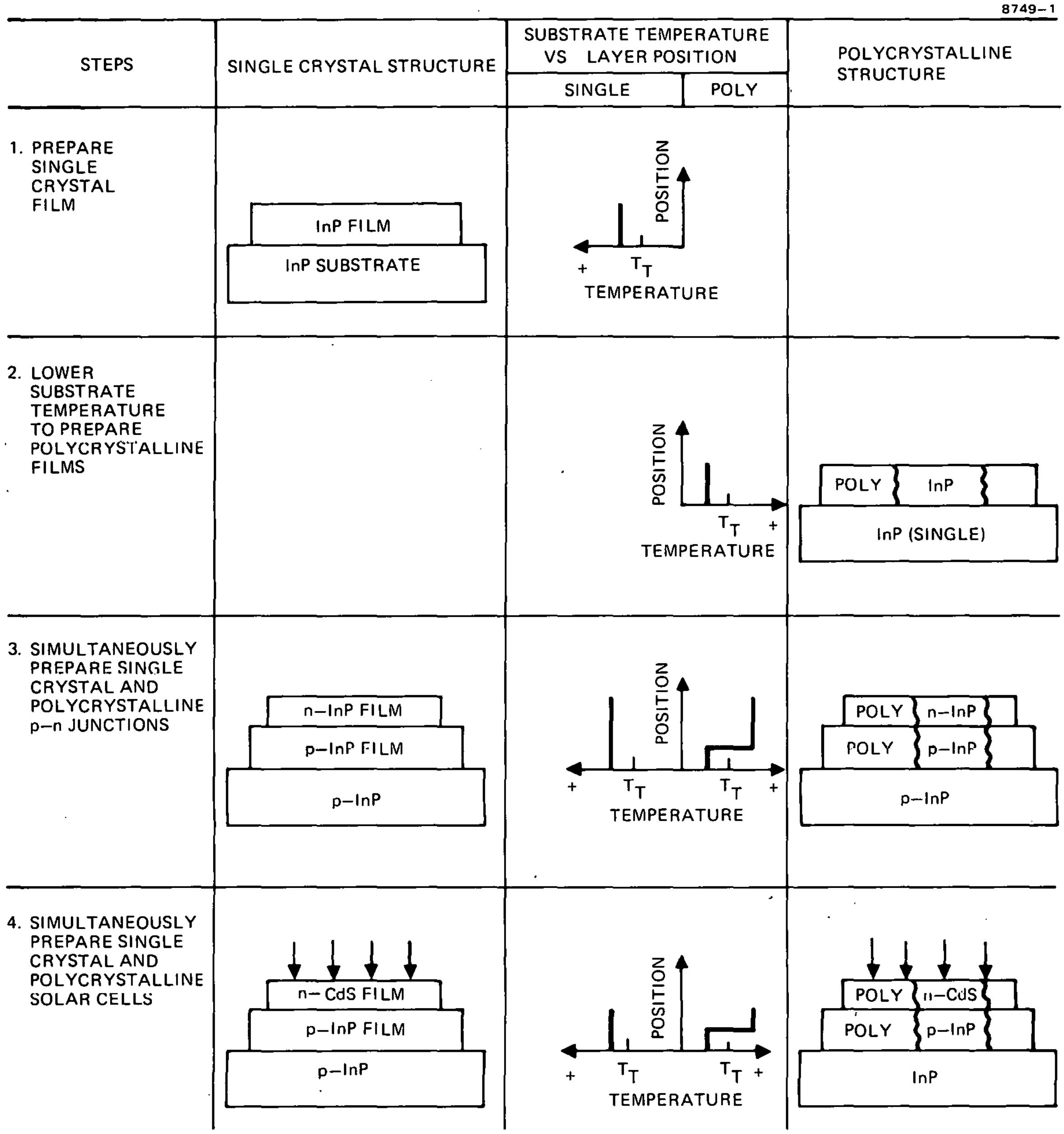
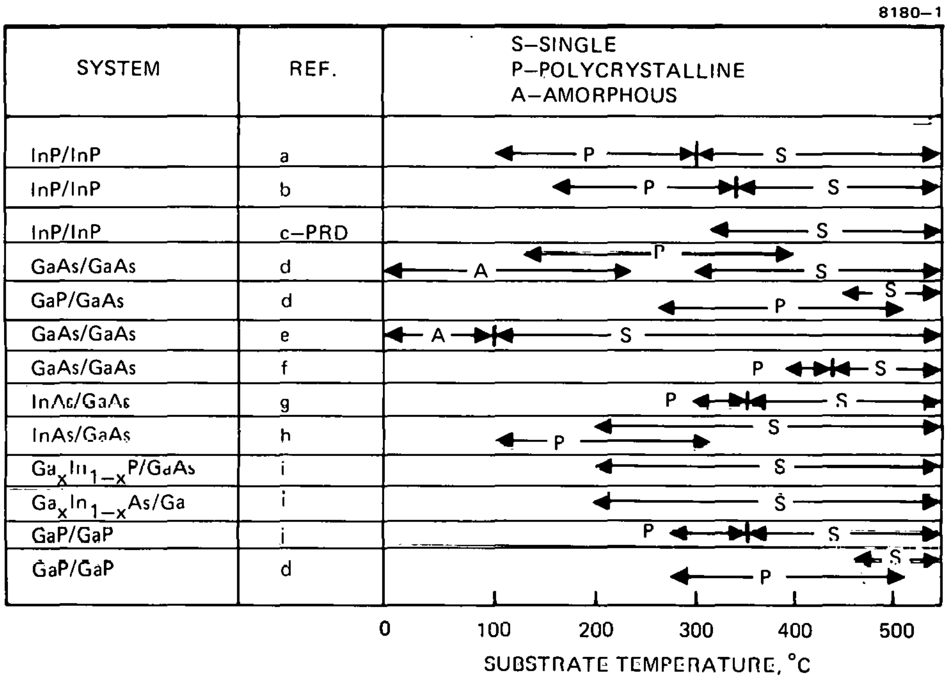


Figure 1. General approach in separating grain boundary effects from single-crystal effects in polycrystalline structures. (T_T refers to transition temperature between single crystal and polycrystalline films.)

Table 1. Temperature Range of the Different Phases of Some Thin Films of III-V Compounds Deposited onto III-V Substrates by Molecular Beam Epitaxy



a. R.F.C. Farrow J. Phys. D:Appl. Phys. 7, L121(1974)

b. J.H. McFee, B.I. Miller, and K.J. Bachmann, J. Electrochem., Soc 124, 259 (1977).

c. K. Zanio, L. Fraas, F. Krajenbrink, and L. Hershenson, presented at Electronic Materials Conf., Boulder, Co., June 1979

d. M. Naganuma and K. Takahashi, Phys. Stat. Sol. (a) 31, 187 (1975)

e. J.H. Neave and B.A. Joyce, J. Crystal Growth 44, 387 (1978).

f. S. Gonda, Y. Matsushima, Y. Makita, and S. Mukai, Jap. J. Appl. Phys. 14, 935 (1975)

g. M. Yano, M. Nogami, Y. Matsushima, and M. Kimata, Jap. J. Appl. Phys. 16, 231 (1977).

h. B.T. Meggitt, E.H.C. Parker, and R.M. King, Appl. Phys. Lett. 33, 528 (1978)

i. C.T. Foxon and B.A. Joyce, J. Crystal Growth 44, 75 (1978).

single-crystal-to-polycrystalline transition temperature to be about 300°C. Our results disagree with those of McFee et al., who found 340°C to be the transition temperature. However, this may be due to differences in substrate orientation and whether or not H_2 was present. The results of the epitaxial deposition of other III-V compounds given in Table 1 also seem to favor a lower transition temperature. To enhance the formation of polycrystalline films, we used a GaAs substrate. Although the mobilities decreased, the film remained single crystal.

Presently our substrates are limited to a lower temperature of 320°C. This temperature refers to the steady-state temperature with the radiant heaters off and the substrate being heated by the source. To lower the substrate temperature, we redesigned the heat shields. A test of the heat shields showed that initially in the run the substrate temperature was lower. However, in the steady state, the temperature of the substrates was only a few degrees less than it had been before the heat shield was redesigned.

Consequently, during this quarter we modified the right PRD chambers so that the substrates can be cooled to below 100°C. The top of Figure 2 shows a schematic view of the heating/cooling assembly incorporated into the deposition chamber and located above the Knudsen cell. The upper portion of this assembly is rigidly mounted to the walls of the PRD chamber. The lower portion, consisting of a stainless-steel plate, makes pressure contact to three substrate holders positioned on the rotatable plate. Stainless-steel bellows provide a nonrigid but pressure contact between the lower and upper portions of the assembly. During the preparation of polycrystalline films, a gas at atmospheric pressure is present within the bellows. The bellows consequently expand, providing pressure contact between the lower portion of the assembly and the substrate holders. When it is necessary that the substrates either be rotated or not view the Knudsen cell, as during outgassing, the bellows are evacuated and the lower plate of the assembly contracts and separates from the substrate holders. A heater and thermocouple are located in the bottom plate of the assembly. During the next period, we will correlate the temperature in the lower plate to the temperature in the substrate holder, undertake our first depositions in the modified assembly, and determine the single-crystal-to-polycrystalline transition temperature.

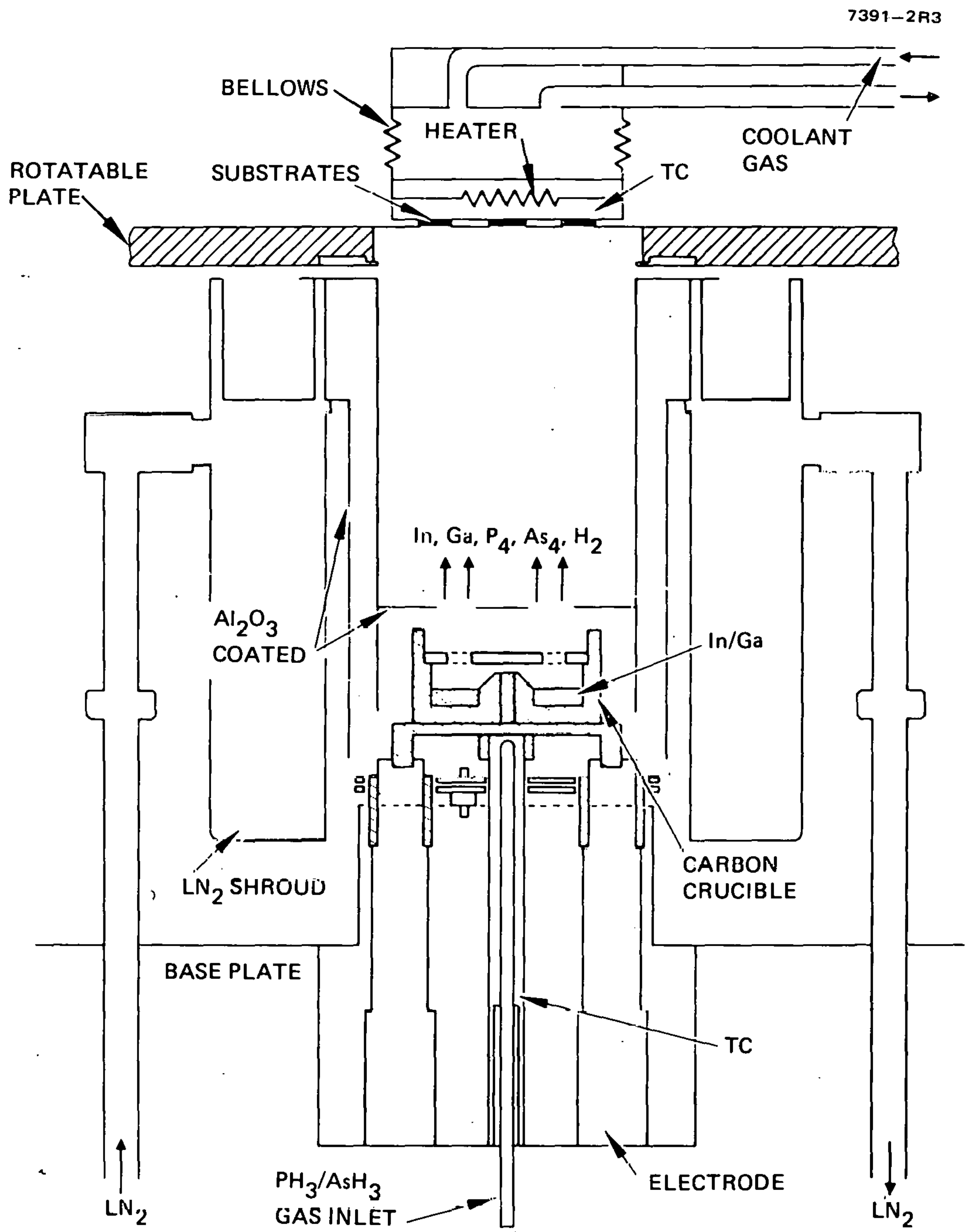


Figure 2. Modified PRD source/substrate assembly.

SECTION 3

GRAIN BOUNDARY MODEL

To assist in the interpretation of our experimental results, we are developing a grain boundary model that is consistent with the equivalent circuit of a polycrystalline film containing a p-n junction (Figure 3).

A. THE LOWER BANDGAP GRAIN BOUNDARY

In this model, the grain boundaries have been represented by two-dimensional periodic arrays of dislocations.[3,4] Recent transmission electron microscope photographs of a grain boundary in Ge show this representation to be quite realistic (Figure 4). We contend that the degree of periodicity and continuity found at the grain boundaries[5,6] is sufficient to treat the grain boundary region as a thin sheet of semiconducting material having a bandgap, E_{GB}, lower than the bandgap, E_G, of the grain. We carry this concept one step further. We consider a p-n junction orthogonal to a grain boundary as in the central region of Figure 5. The characteristics of the resulting device are to a first approximation determined by the properties of a p-n junction in a thin sheet of semiconducting material in parallel with the p-n junction of the grain. A p-n junction at the grain boundary has already been considered to contain localized defect states.[7] However, to our knowledge, this is the first time that a p-n junction in a grain boundary region has been considered to consist of a semiconductor with its own band structure.

A portion of the grain on the right in Figure 5 was removed from the bicrystal to expose the grain boundary. Included on the right side of Figure 5 is an energy diagram of the p-n junction through the grain boundary material. Deep levels having a concentration of N_R are also present. The bottom (top) of the conduction (valence) band of the adjacent single-crystal material is superimposed on the band structure of the energy levels. Separate schematics of the energy bands for material orthogonal to the grain boundary in both n- and p-type materials are shown in the figure. The degree of band bending in the conduction

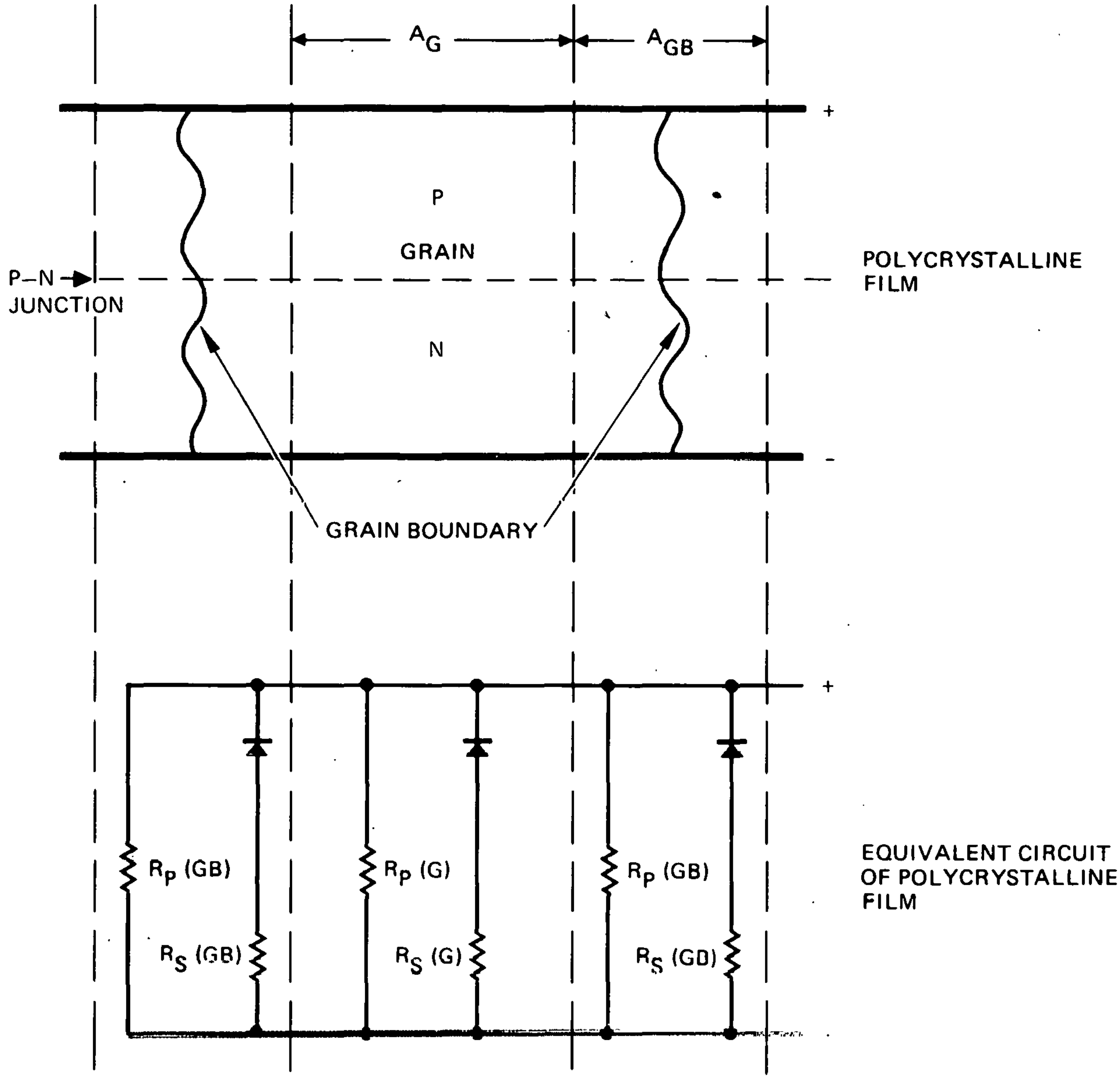


Figure 3. (Top) Polycrystalline film represented as (bottom) an array of parallel diodes.

7730-12

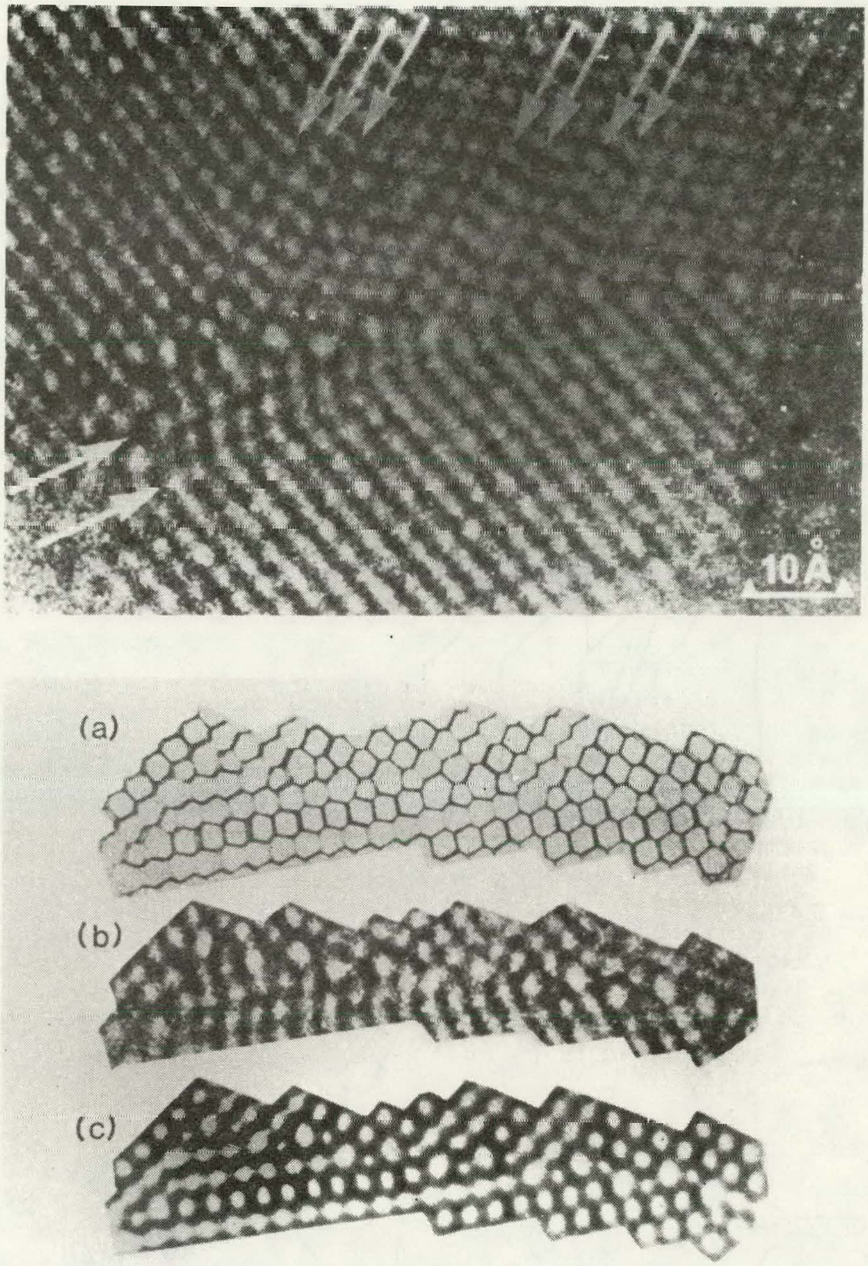


Figure 4.
(Top) Transmission electron microscope picture of grain boundary region separating single crystals A and C of Ge. (Bottom) A comparison of (a) the model (b) the TEM picture, and (c) the blurred image of the model (from Ref. 6).

7660–4

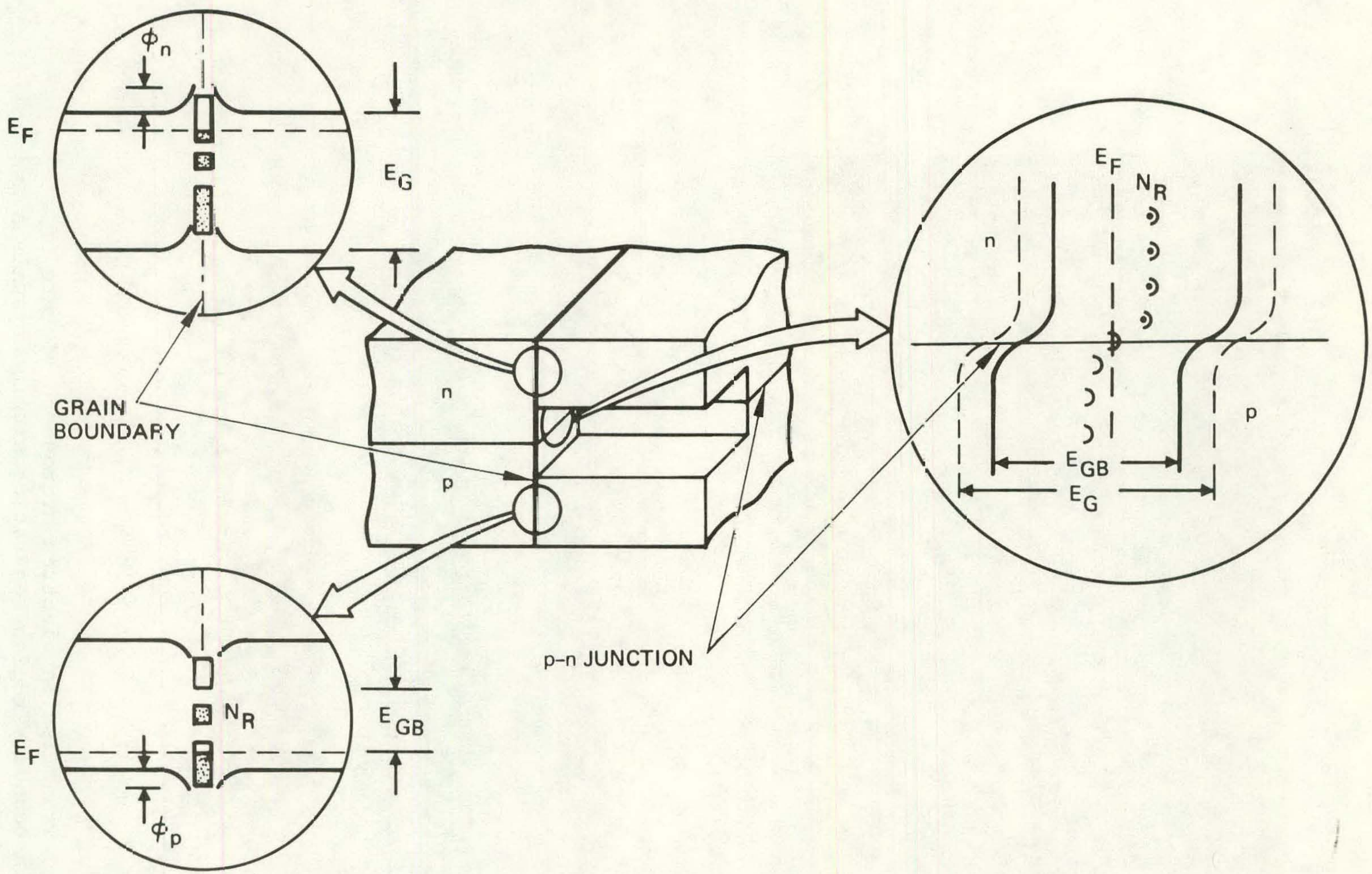


Figure 5. (Center) P-N junction in bicrystal orthogonally intersecting grain boundary. (Left) Schematic of energy diagram across grain boundary region in n-type (top) and p-type (bottom) material. (Right) Schematic of energy diagram grain boundary material intersecting the p-n junction. Dashed lines refer to band edges of adjacent single crystal.

1495

(valence) band of the single-crystal grain due to the transfer of electrons (holes) from the single-crystal grain to the intergranular material in n-type (p-type) material to attain equilibrium is ϕ_n (ϕ_p).

B. EFFECT OF REDUCED BANDGAP ON DIODE PERFORMANCE

In modeling the grain boundary at the p-n junction, we assume that the dark current of the composite structure is generation-recombination limited. Majority carriers at the p-n junction in the single-crystal region are thermally activated across the p-n junction through the potential E_G and recombine through centers near the middle of the bandgap. Majority carriers at the grain boundary are likewise thermally activated, but through the potential $E_G-\phi_n-\phi_p$. The dark current density in this region is likely to be higher, not only because carriers must be activated through a lower potential but also because the grain boundary region has a higher concentration N_R of recombination centers. Because the dark current through the diode will increase as the ratio of the area of the grain boundary region to the area of the single-crystal region increases, it is desirable to increase the grain size. Unfortunately, the dependence of the dark current on grain size is not presently known. When the dark current at the grain boundary region dominates the dark current of the polycrystalline film, I_o can be exclusively associated with the material parameters of the grain boundary. A simple approximation relating the grain boundary parameters to the dark current is

$$I_o = \frac{en_{GB}w}{\tau^+} \exp\left[-\left(\frac{E_G-\phi_n-\phi_p}{2kT}\right)\right] , \qquad (1)$$

where n_{GB} is the effective number of electrons in the grain-boundary region, and w is the width of the grain boundary region. The lifetimes of electrons and holes, τ^+, are assumed to be equal. An equal current and a similar expression exists for holes. When the dark current of the device is dominated by the recombination-generation current at the grain boundary, the open-circuit voltage of the device is reduced over that found in a single-crystal device and is given by:

$$V_{oc} = \frac{A_o kT}{g} \ln \left[\frac{I_{sc}}{I_o} + 1 \right] , \qquad (2)$$

where I_{sc} is the light-generated short-circuit current, and A_o is the diode factor. The effect of the increased I_o in polycrystalline material is to lower the open-circuit voltage. Lower V_{oc} in polycrystalline materials is the main reason why the efficiencies of cells prepared from polycrystalline materials are less than those of cells prepared from single crystals.

Considering the polycrystalline film to be an array of parallel diodes, as in Figure 3, and assuming a range of material parameters, we have calculated the grain sizes below which the leakage current at the grain boundary dominates the total leakage current of the cell. The density of majority carriers available for thermal activation across the p-n junction in both the grain boundary region and the grain were assumed to be equal, and the width of the grain boundary region was assumed to be 10 Å. Table 2 shows that for τ_G/τ_{GB} to equal 10 and $E_G - E_{CB}$ to equal 0.2 eV, the grain size must be larger than 0.5 μm or the leakage current at the grain boundary will dominate the cell leakage current. Here τ_{GB} is the majority carrier lifetime at the p-n junction in the grain and is assumed here to be 1 μsec. Preliminary measurements of barrier heights indicate that $E_G - E_{GB}$ ranges from 0.2 eV to 0.5 eV. Therefore, although grain sizes of a few micrometers may be adequate to obtain good short-circuit currents, a few micrometers may not be adequate to obtain a large open-circuit voltage. If the grain size cannot be increased, passivation techniques may be necessary.

Table 2. Grain Sizes Below Which Grain Boundary Currents Dominate the Cell Leakage Current

$E_G - E_{GB}$, eV	τ_G/τ_{GB}	Grain Size, μm
0.2	10	0.5
0.3	10	4
0.4	10	30
0.5	10	200
0.2	100	5
0.3	100	40
0.4	100	300
0.5	100	2,000

6657

C. ELECTRICAL MEASUREMENTS IN SUPPORT OF MODEL

The effective bandgap of the grain boundary material ($E_G-\phi_n-\phi_p$) and the number of available carriers for recombination n_{GB} can be determined by electrical measurements parallel to the film (i.e., perpendicular to the grain boundary). Such measurements were begun under DOE Contract EY-76-C-04-3717. Since these studies will be continued in the present program, we include the preliminary results here for convenient reference. Before discussing these results, a model for inspecting transverse film measurements is summarized.

The polycrystalline film consists of two regions: a low-resistivity region in the crystallites and a current-blocking region at the grain boundaries. For this case, where the doping level is relatively high and therefore the resistivity in the crystallites is sufficiently lower than that in the grain boundaries, the observed resistivity is described by[8,9,10]

$$\rho = (ne\mu)^{-1} \propto \exp(\phi/kT)\ \exp(E_A/kT) \quad , \tag{3}$$

where $\bar{n}$ is the average carrier concentration in the films as determined by Hall measurements. The mobility of the carrier is limited by a barrier ϕ at the grain boundary and corresponds to ϕ_n or ϕ_p in Figure 5, depending on whether the film is n type or p type. The term E_A is the activation energy of electrons (holes) from donors (acceptors) if the grains are n (p) type. The barrier height and activation energy for polycrystalline n-type InP films prepared in our laboratory on sapphire substrates at 400°C are shown in Figure 6. The value for ϕ_n was 0.14 eV. A more detailed description of the model is available in the final report to Contract EY-76-C-04-3717 and will be included in later reports when polycrystalline films on semi-insulating substrates are available.

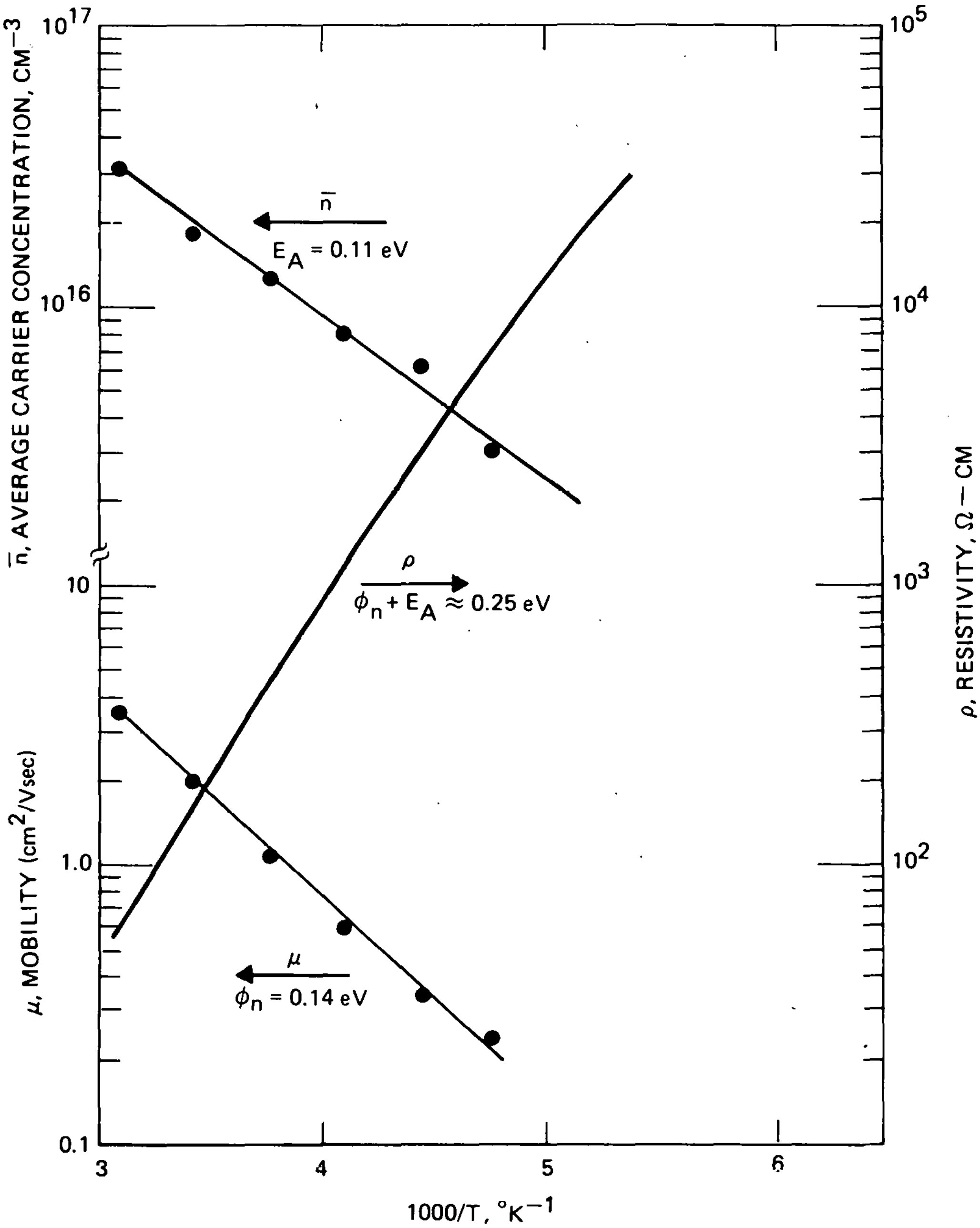


Figure 6: Resistivity (ρ) and Hall ($\bar{n}$) measurements for polycrystalline n-type InP films prepared on sapphire at 400°C. ϕ_n and E_A are defined in Eq. 3 and Figure 5.

SECTION 4

GRAIN BOUNDARY PASSIVATION

Grain size may not be adequate to prevent excessive leakage currents in polycrystalline solar cells. Consequently, we have begun complementary grain boundary passivation studies. A process that preferentially attacks the InP grain boundaries might be useful in passivating a buried p-n junction (Step 1 in Figure 7). We are examining two approaches.

The first approach is to etch the polycrystalline structure anodically. Preferential oxidation should occur at the lower resistivity grain boundary, and an insulating oxide layer might penetrate beyond the buried p-n junction. In preparation for this study, we determined the voltage (Figure 8) required to deposit an oxide layer of given thickness in single-crystal material. The thickness of the layers was determined by using an interference microscope to measure the height of an aluminum-coated step formed by the oxide layer and the original InP surface stripped of the oxide by an HF etch. During the next quarter, we will examine the effect of anodic oxidation at the grain boundaries.

The second approach is to first remove the grain boundary beyond the p-n junction as in Step II of Figure 7 and then passivate as in Step III. We have examined the effect of 0.4N $FeCl_3$ in HCl, NaOH potassium fericyanide, and NaOH ferrocyanide on bulk polycrystalline wafers. These etches attack InP. The effectiveness of 0.4N $FeCl_3$ as a dislocation etch after 30 sec is shown in Figure 9 (top). The etch pit density here is about 2×10^5 cm^{-2}. A 20-sec etch of the wafers clearly reveals the grain boundaries (bottom) in a bulk polycrystalline wafer. In an examination with an optical microscope, it was not evident whether the grain boundaries had been preferentially etched or whether different crystal planes had been etched at different rates, resulting in a step at the grain boundaries. During the next period, we will examine in more detail the nature of the grain boundary.

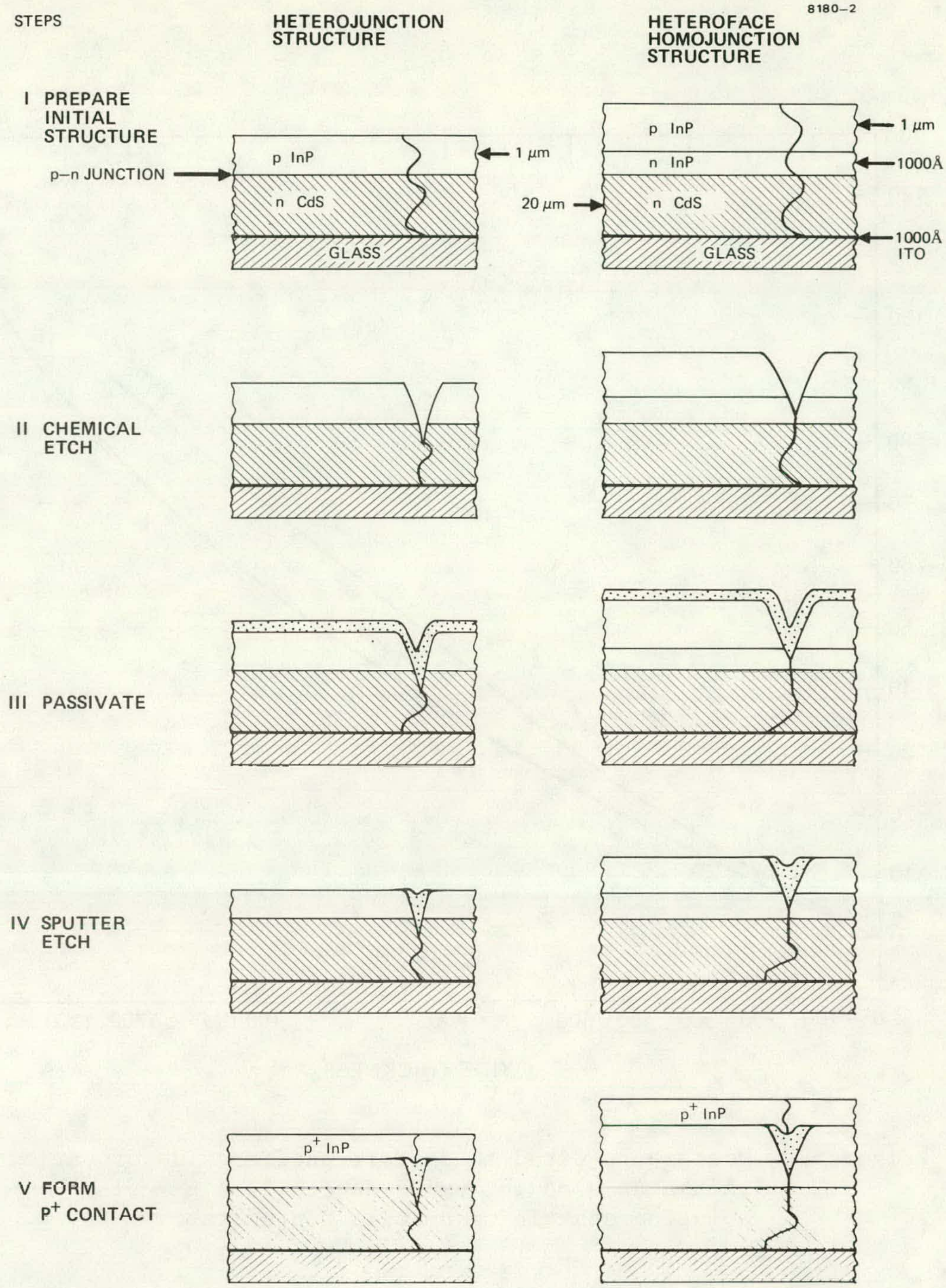


Figure 7. Etch/passivation sputter-etch scheme on the all-thin-film InP/CdS/glass system to prepare polycrystalline devices with reduced grain boundary leakage currents.

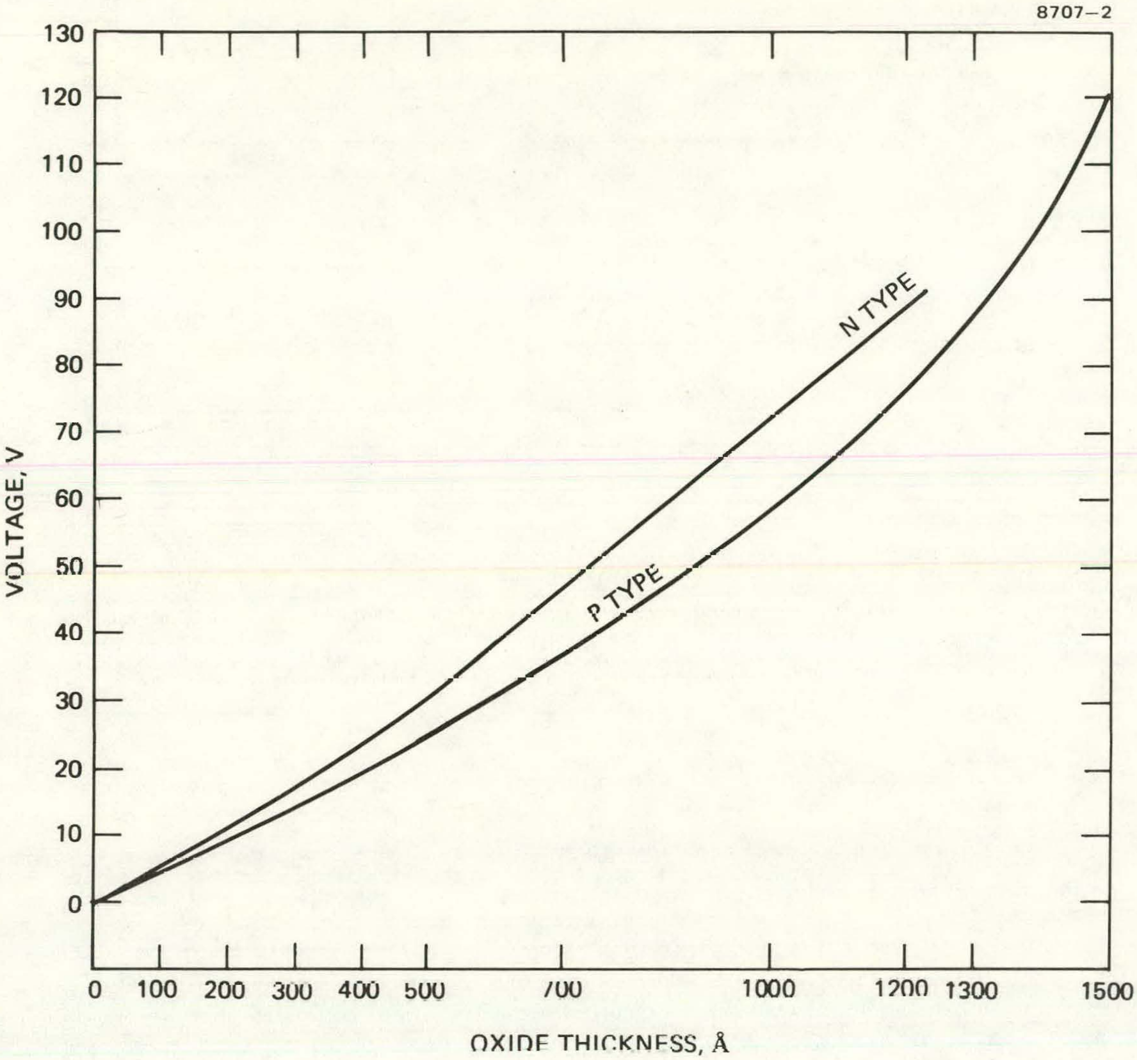


Figure 8. Voltage required to deposit anodic oxide of various thicknesses on InP using an ethylene glycol solution containing ammonia pentaborate.

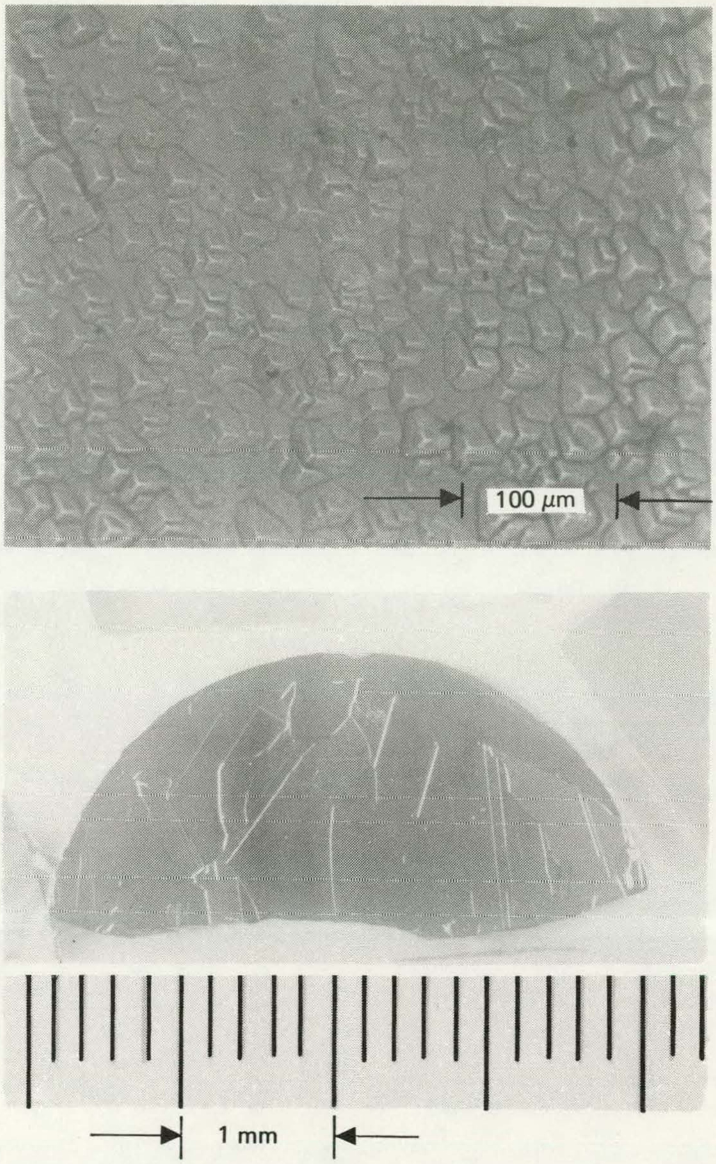


Figure 9. (Top) Etch pits and (bottom) grain boundaries in bulk InP revealed by etching 0.4 N $FeCl_3$ in HCl.

Alternative methods of passivating the grain boundary are to deposit, as in Step 3, either an anodic oxide or the higher bandgap semiconductor InGaP. In preparation for undertaking the latter approach, we have epitaxially deposited InGaP onto InP and GaAs substrates. X-ray examination of the layers with a Read camera showed the layer on InP substrates to be of good crystalline quality even for a 3.4% lattice mismatch. The extent to which such a lattice mismatch will introduce recombination states is not known. However, a modification of the PRD process would have the desirable feature of grading the layers from InP to GaP to alleviate a mismatch.

SECTION 5

SUMMARY AND FUTURE WORK

During this quarter, we modified our deposition system to cool our substrate well below 300°C so that both single-crystal and polycrystalline InP films can be prepared in the same run. During the next quarter, we intend to define the single-crystal-to-polycrystalline transition temperature and use this information to prepare single-crystal and polycrystalline InP diodes by preparing, respectively, films above and below the transition temperature. We have also introduced a model for grain boundaries intersecting a p-n junction. Transverse electrical measurements on our polycrystalline layers will provide data to substantiate our model. The effect of various etchants on grain boundaries in InP was also examined as a preliminary step toward passivating the grain boundaries. An anodic oxide and InGaP, both candidates as passivation layers, were deposited on single-crystal InP. During the next quarter, we intend to determine if these layers can be deposited into channels formed by grain boundary etching.

REFERENCES

1. S. Wagner, J.L. Shay, K.J. Bachmann, E. Buehler, and M. Bettini, J. Crystal Growth 39, 128 (1977).

2. K. Zanio and L. Fraas, "Indium Phosphide/Cadmium Sulfide Thin Film Terrestrial Solar Cells," DOE EY-76-C-04-3717.

3. E. Kamienicki, J. Phys. C. Solid State Phys. 9, 1211 (1976).

4. H. Mataré, Defect Electronics in Semiconductors, Wiley Interscience N.Y. (1971).

5. J.W. Matthews and W.M. Stobbs, Phil. Mag. 36, 373 (1977).

6. O.L. Krivanek, S. Isoda, and K. Kobayashi, Phil. Mag. 36, 931 (1977).

7. H.C. Card, IEEE Trans. on Electron Devices 24, 397 (1977).

8. T. Saitoh and S. Matsubara, J. Electrochem. Soc. 124, 1065 (1977).

9. J. Seto, J. Appl. Phys. 46, 5247 (1975).

10. T. Kamins, J. Appl. Phys. 42, 4357 (1971).

☆U.S. GOVERNMENT PRINTING OFFICE: 1979—640-258/1495