COMPARISON OF METALLIZATION SYSTEMS FOR THIN FILM HYBRID MICROCIRCUITS

Part II: Corrosion Susceptibility and Solderability

By M. K. Raut and R. A. Hines

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**The Bendix Corporation
Kansas City Division
P. O. Box 1159
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COMPARISON OF METALLIZATION SYSTEMS FOR THIN FILM HYBRID MICROCIRCUITS

Part II: Corrosion Susceptibility and Solderability

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ABSTRACT

Corrosion susceptibility and solderability were evaluated for thin film Cr/Pd/Au, Ti/Pd/Au, and the currently used evaporated chromium/gold system. Both evaporated and electroplated gold were included in the Cr/Pd/Au and Ti/Pd/Au samples. For the corrosion susceptibility evaluation, circuits from each system were exposed to various solutions used in the fabrication process, and the percent change in interface resistance was measured as a function of time. For the solderability evaluation, solder filled via resistance and solder bond strengths were measured after temperature cycling. The electroplated gold systems with a palladium layer showed better corrosion resistance and solderability than evaporated chromium/gold.

INTRODUCTION

Recurring seasonal reduced yields in thin film network manufacturing have occurred because of the corrosion susceptibility of evaporated chromium/gold metallization used to produce hybrid microcircuits at Bendix Kansas City. This reduced yield led to studies comparing the corrosion susceptibility of various metallization systems to the etchants

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normally used in thin film processes. This study compares the corrosion susceptibility of evaporated chromium/gold to evaporated chromium/palladium/gold, evaporated titanium/palladium/gold, and titanium/palladium/pattern-plated gold. Corrosion susceptibility was determined by measuring changes in interface resistance of the thin films after exposure to the etchants used in photolithography. In addition to the corrosion susceptibility tests, the solderability of chromium/gold was compared to chromium/palladium/pattern-plated gold by measuring the changes in via resistance after soldering and temperature cycling and the differences in shear strength of soldered capacitors.

EVALUATIONS

Corrosion Susceptibility

At least two thin film networks from each metallization system were used for the corrosion susceptibility evaluation. The study included both vapor and immersion exposure to the corrosives. For the vapor exposure, the networks were kept in petri dishes with lids, and these dishes were enclosed in ground glass joint weighing bottles containing the corrosive solutions for a given time period. Care was taken to ensure that the monitors did not come in contact with the solutions. For the immersion exposure, the networks were immersed in a given corrosive solution for a period of time, rinsed in deionized water for 1 minute, and blown dry with dry nitrogen. The tantalum/conductor interface resistance of the network was measured before and after exposure. The interface resistance measurements were repeated every 8 to 10 hours up to at least 200 hours. The detailed procedures for each type exposure are shown in Figures 1 and 2.

The pattern used for measuring the interface resistance between the conductive and resistive (tantalum) layers is shown in Figure 3. The pattern includes two resistors of equal design value: (1) a control resistor in a typical meandering configuration and (2) a series of small resistors totaling the same value as the control resistor. Both resistor patterns contain 98 squares of resistor material. The control has two interfaces, and the series short has 196 interfaces. Both resistors are 0.005 inch wide, large enough for good photolithography processing but sufficiently narrow so that interface resistance, an inverse function of width, can be significant. For a good, typical film, interface resistance would be about 28 ohms for the control and 2800 ohms for the series short, or 0.28 and 28% respectively, of the total value of the resistors.

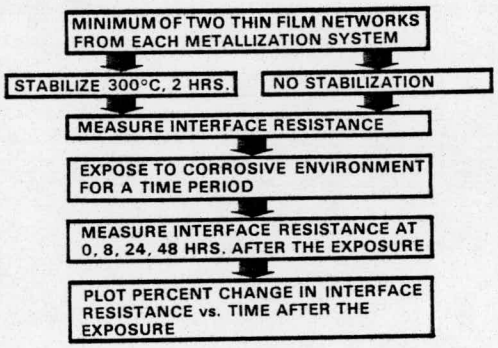

Figure 1. Vapor Exposure Test

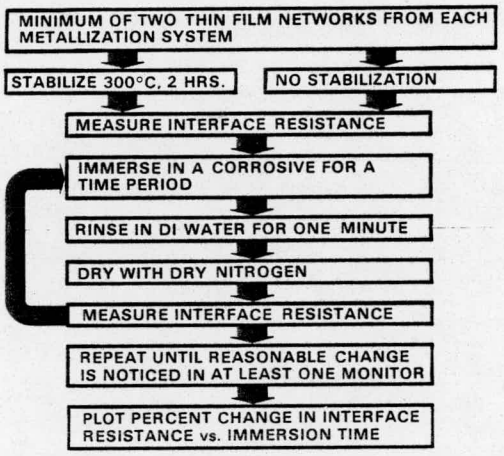

Figure 2. Immersion Exposure Test

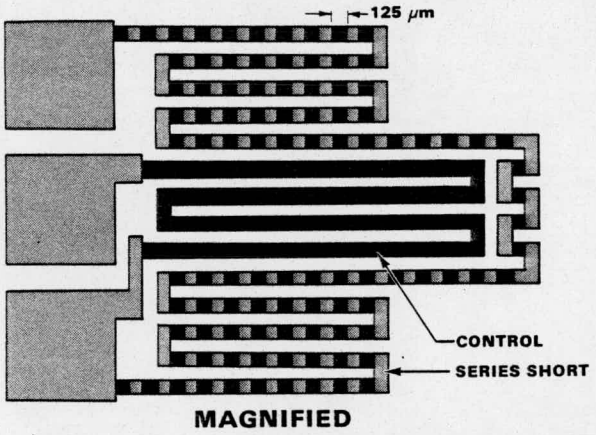

Figure 3. Interface Resistance Pattern Used to Evaluate Corrosion Susceptibility

Table 1. Composition of Corrosive Solutions

CORROSIVE	COMPOSITION
Au ETCHANT	1.5 N I_2 + 4.0 N KI
Cr ETCHANT	164 g $(NH_4)_2$ Ce $(NO_3)_6$ + 135mL HNO_3 PER LITER SOLUTION
Ta ETCHANT	3.4 PARTS HF: 1 PART HNO_3: 10 PARTS CH_3CO_2H
Pd ETCHANT	0.5 M LiCl + 0.2 M Mg $(ClO_4)_2$ IN ETHYLENE GLYCOL
Ti/Pd ETCHANT	100 g $FeCl_3$ + 500 mL HCl 50 mL HF + 500 mL H_2O

The corrosives used during the vapor exposure study were gold etchant (KI/I_2 solution), chromium etchant (ceric ammonium nitrate-nitric acid solution), tantalum etchant (hydrofluoric-nitric acid solution), and titanium/palladium etchant (ferric chloride-hydrochloric and hydrofluoric acid solution). For the immersion exposure studies, the corrosives used were palladium etchant, chromium etchant, and water. Chemical composition of each etchant is shown in Table 1.

After several interface measurements, the change in interface resistance for a period of time after the exposure was plotted versus time. Typical plots are shown in Figures 4 and 5. Table 2 shows the change in interface resistance for various metallization systems after given time periods. The study showed that evaporated Cr/Au was much more susceptible to the corrosive environments, as compared to the tri-metal systems. The highest corrosion rate was observed when the Cr/Au system was exposed to the gold etch vapors.

Solderability

In addition to corrosion resistance, a thin film metallization system used for HMC manufacturing must be solderable and must withstand specific environmental tests after HMC assembly. Lead 50-Indium 50 solder is used at Bendix to solder capacitors and other components to chromium/gold thin films. A comparison study was made to test the solderability of lead-indium solder to evaporated chromium/gold versus chromium/palladium/pattern-plated gold. A total of seven (5 with electroplated gold and 2 with evaporated gold) 95 by 114 mm substrates (Herman) with vias were used for the study. Vias are metallized holes which act as intraconnections between the frontside conductor-resistor network and the backside ground phase. Soldered TFNs were subjected to three different tests. Visual examination, via resistance, and capacitor shear strength were needed to evaluate the solder joints (Figure 6). Solder Test I (Figure 7) included extensive vacuum baking and temperature cycling. The results from the test are shown in Table 3 and Figures 8 through 12. Solder Test II simulated the conditions to which soldered product is exposed during production, along with extended periods of temperature exposure. The procedure for this test is shown in Figure 13, and the results obtained are shown in Table 4 and Figure 14. Solder Test III was an extended baking cycle. The samples in this test were baked at 125°C for 16 hours a total of four times. The procedure of this test is shown in Figure 15, and results are shown in Table 5 and Figure 16. Via resistance change between pre- and post-soldering and during temperature cycling was found to be greater with evaporated gold metallized vias as compared

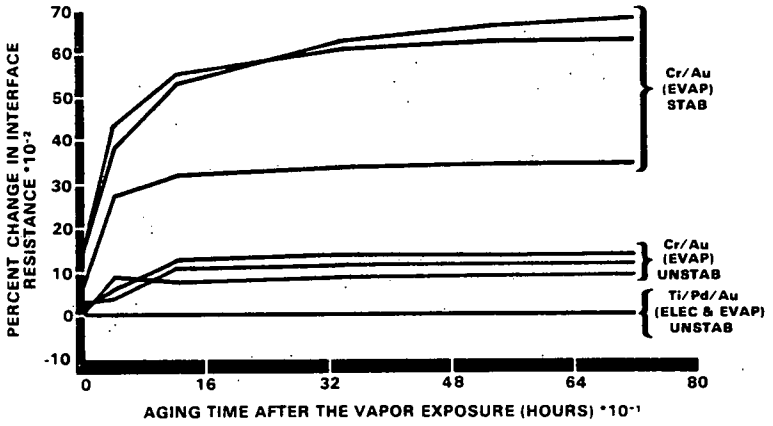

Figure 4. Au Etch Vapor Exposure

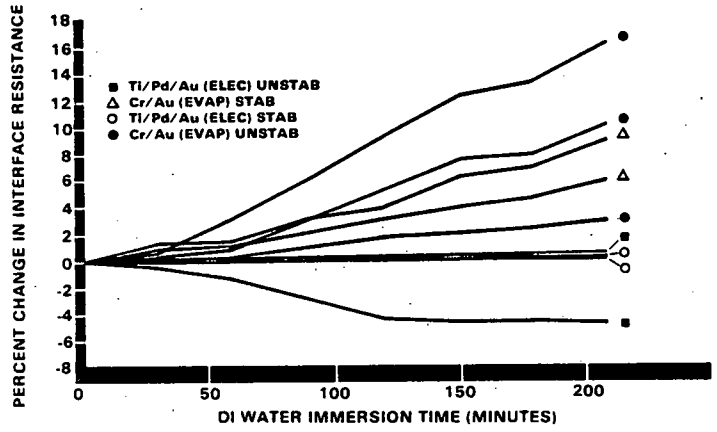

Figure 5. Water Immersion

Table 2. Percent Change in Interface Resistance

		Cr/Au (EVAP)		Cr/Pd/Au(EVAP)		Ti/Pd/Au(EVAP)		Ti/Pd/Au(ELEC)	
	SOLUTION (TIME)	STAB	UNSTAB	STAB	UNSTAB	STAB	UNSTAB	STAB	UNSTAB
VAPOR EXPOSURE STAB - 20 MIN UNSTAB - 2 HR	Au ETCH (529 H)	34.4	293.7	0.03	0.07	0.07	-1.95	0.00	-0.35
	Cr ETCH (529 H)	17.57	8.9	0.22	0.08	1.9	-2.3	0.09	0.20
	Ta ETCH (529 H)	16.59	5.75	0.63	0.01	0.0	13.4	0.33	-3.1
VAPOR EXPOSURE 2 HR	Ti-Pd (718 H)	337.8	162.6					-0.03	0.09
	Ta ETCH (718 H)	74.8	28.9					-0.01	0.30
	Au ETCH (718 H)	5479.	1155.					-0.04	0.06
IMMERSION	H_2O (210 M)	7.4	9.7					0.0	-1.73
	Cr ETCH (142 M)	23.6	44.3					0.0	0.89
	ANODIC (20 M*)	55.2	442.6					0.0	0.15

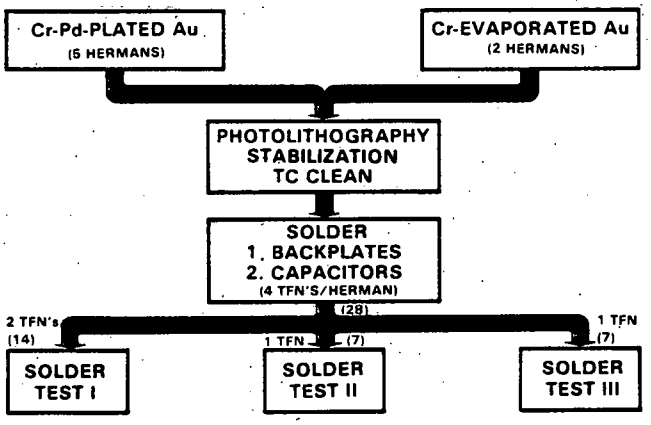

Figure 6. Solder Evaluation

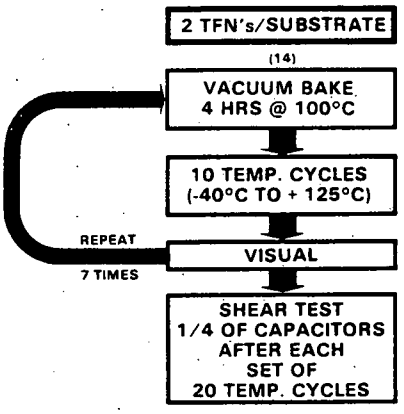

Figure 7. Solder Test I

Table 3. Solder Evaluation, Solder Test I Sequence

	CAPACITOR SHEAR STRENGTH (LB.)				
TEMP. CYCLES →	20	40	60	70	80
Cr/Pd/Au (PLATED)	2.6	2.0	3.6	2.9	3.6
	2.6	2.3	2.7	3.5	4.3
	2.3	3.0	2.4	2.6	3.0
	2.9	2.8	2.4	2.2	3.6
	3.0	3.6	2.0	2.8	2.3
	1.8	2.5	2.9	3.1	4.1
	2.7	2.3	3.2	4.4	2.5
	2.7	3.5	3.8	3.0	3.4
	2.8	2.6	3.1	3.3	2.7
	3.4	3.2	4.8	4.4	3.3
Cr/Au (EVAPORATED)	2.9	2.3	3.1	2.9	4.4
	2.7	2.8	2.2	3.6	4.8
	1.9	2.8	2.8	2.1	3.6
	2.5	2.8	2.9	4.7	3.0

= FAILURE AT SOLDER/METALLIZATION INTERFACE
(ALL OTHER FAILURES OCCURED IN SOLDER FILLET)

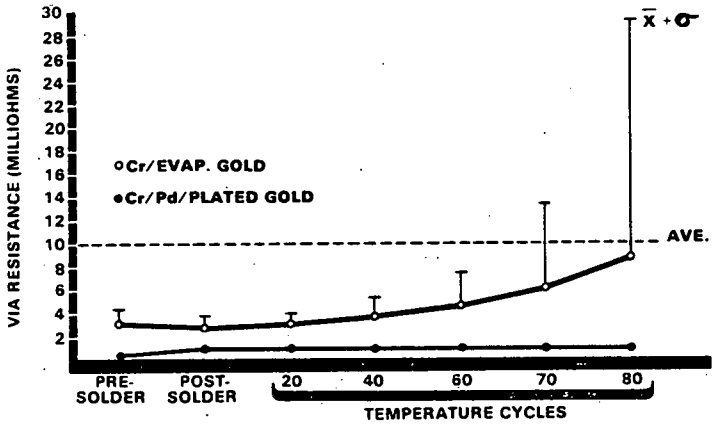

Figure 8. Soldered Via Resistance, Solder Test I

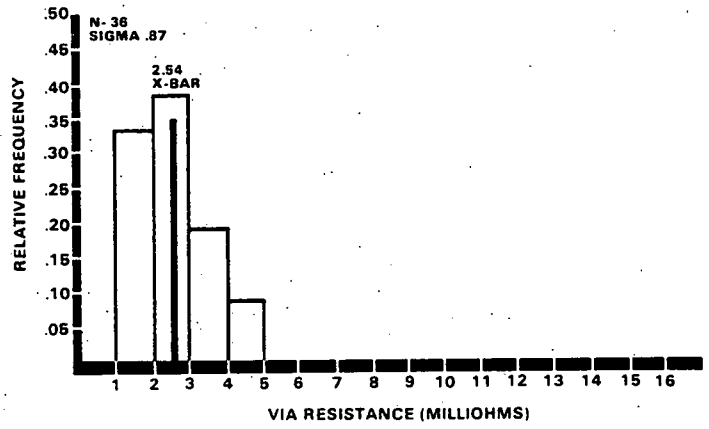

Figure 9. Evaporated Cr/Au, Post-Solder

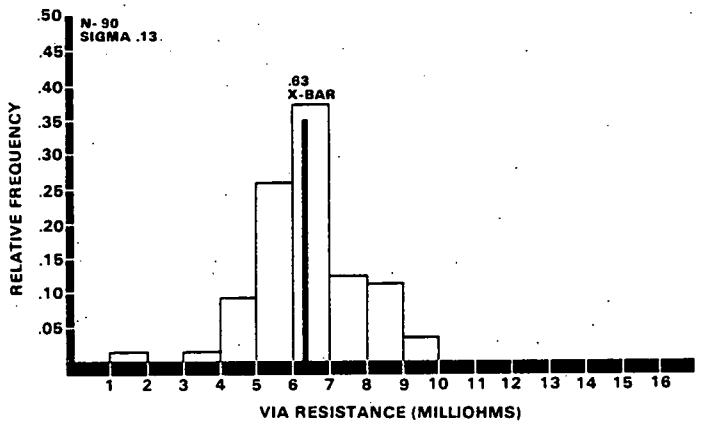

Figure 10. Cr/Pd/Plated Gold, Post-Solder

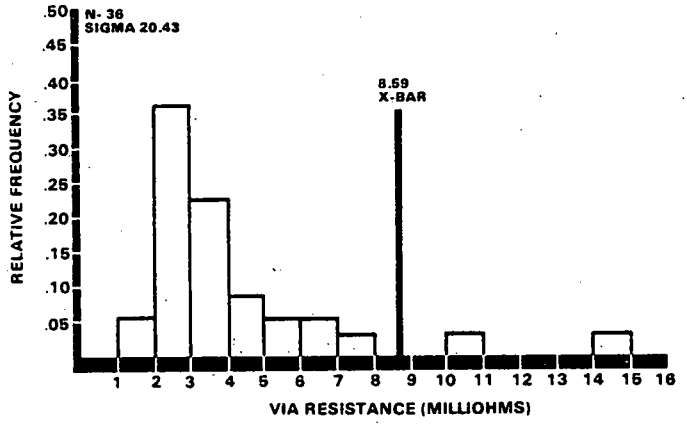

Figure 11. Evaporated Cr/Au, After Temperature Cycles

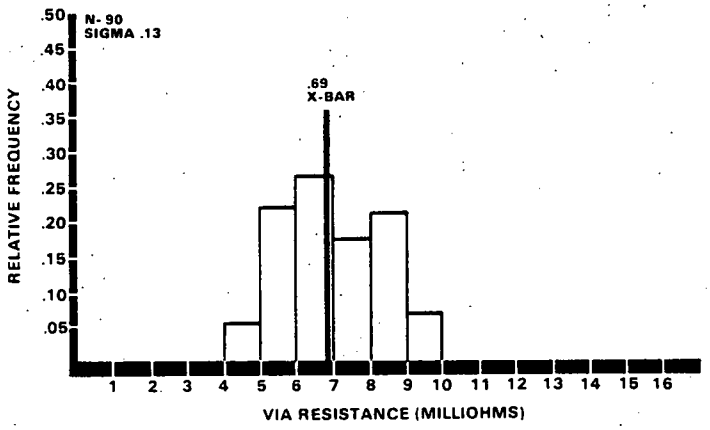

Figure 12. Cr/Pd/Plated Gold, After Temperature Cycles

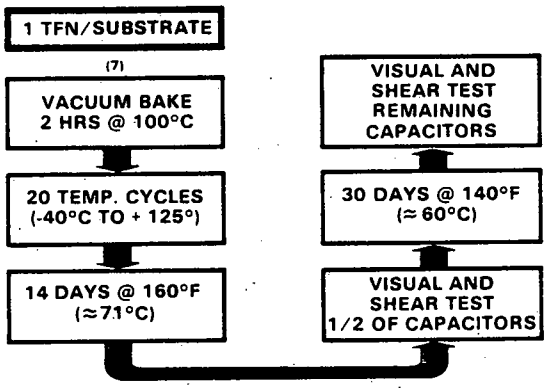

Figure 13. Solder Test II

Table 4. Solder Evaluation, Solder Test II Sequence

CAPACITOR SHEAR STRENGTH (LB.)

	2 HR. VACUUM BAKE (100°C) + 20 TEMP. CYCLES + 14 DAYS @160°F	+ 30 DAYS @140°F
Cr/Pd/Au (PLATED)	2.0, 2.2 2.4, 3.0 1.8, 2.9 2.8, 3.0 2.2, 2.4	2.8, 3.0 3.0, 2.7, 3.6 4.6, 2.7, 3.9 3.0, 3.2, 3.7 2.8, 2.0, 2.8
Cr/Au (EVAPORATED)	2.5, 2.3 2.0, 2.4	3.2, 2.3, 2.5 2.4, 1.6, 1.9

☐ = FAILURE AT SUBSTRATE METALLIZATION INTERFACE
(ALL OTHER FAILURES OCCURED IN SOLDER FILLET)

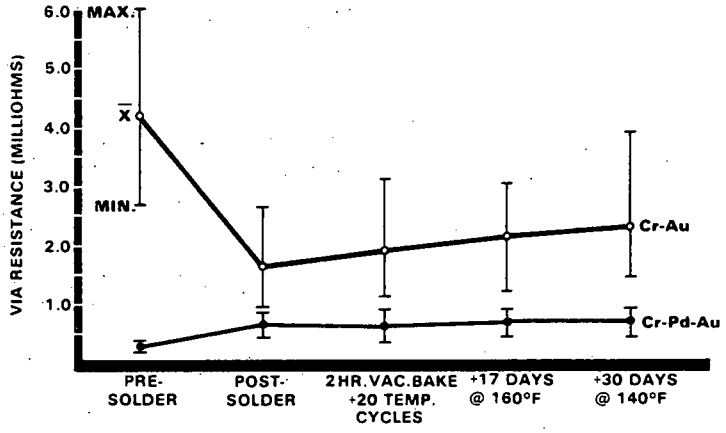

Figure 14. Soldered Via Resistance, Solder Test II

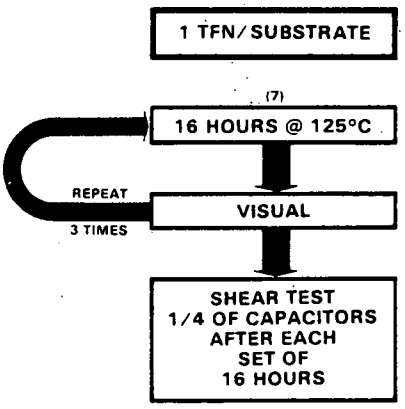

Figure 15. Solder Test III

Table 5. Solder Evaluation, Solder Test III Sequence

CAPACITOR SHEAR STRENGTH (LB.)

HOURS →	16	32	48	64
Cr/Pd/Au (PLATED)	2.9 4.0 2.2 2.7 3.0	2.6 3.9 2.5 3.7 3.2	2.7 2.9 3.7 3.4 5.0	2.6 4.0, 3.0 3.7, 4.9 3.9, 2.8 4.6, 4.0
Cr/Au (EVAPORATED)	2.0 2.2	2.7 3.0	4.0 3.5	2.2, 3.5 2.3, 2.2

□ = FAILURE AT SUBSTRATE METALLIZATION INTERFACE
(ALL OTHER FAILURES OCCURED IN SOLDER FILLET)

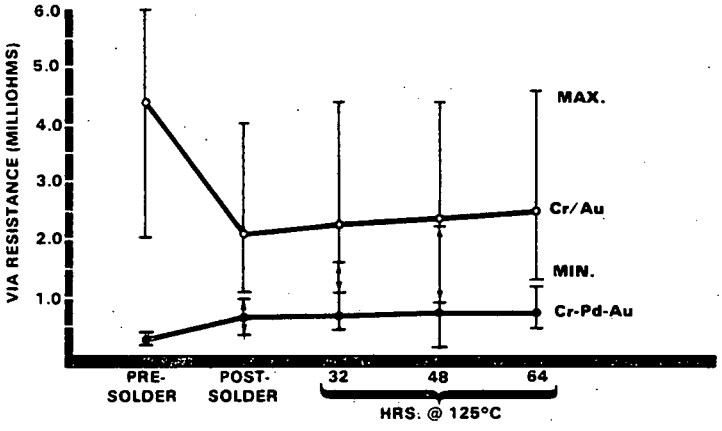

Figure 16. Soldered Via Resistance, Solder Test III

to the electroplated gold metallized vias. All three tests showed that, under normal conditions, shear strength of capacitors soldered on electroplated gold was equivalent to evaporated gold. However, after exposing the substrates to excessive temperature cycles, soldered capacitors on evaporated gold had low shear strength failures at metallization-solder interfaces.

CONCLUSIONS

Metallization systems with a palladium layer and electroplated gold were superior to the evaporated chromium/gold system with respect to both corrosion susceptibility and solderability. The highest corrosion rate was observed when the chromium/gold system was exposed to the gold etch vapors. Stabilized chromium/gold films are more susceptable to corrosion than unstabilized chromium/gold films. Addition of a palladium layer beneath the gold layer improved the corrosion susceptibility. The average via resistance of evaporated gold was approximately 7 to 10 times higher than electroplated gold prior to soldering. After soldering, via resistance of chromium/gold systems was decreased. Resistance increased when samples were exposed to excessive temperature cycling. Soldered capacitor shear strength initially were the same for electroplated and evaporated gold samples. However, after a few temperature cycles, solder/metallization interface failures were observed on the evaporated gold substrates. No such failures occurred on plated gold samples.

ACKNOWLEDGEMENTS

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