

## LOW COST SIMULATOR FOR STRATEGIC RADIATION ENVIRONMENTS

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Recent experimental works on the effect of dose rate on the total dose failure threshold of MOS devices have shown that the failure level is strategic environments may be less than the failure level measured in the laboratory by a factor of 3 to 10. This difference in dose rate response raises concerns about using laboratory sources to predict the radiation hardness in strategic environments. A solution to the problem of determining the total dose hardness of piece parts is to perform lot acceptance testing at relevant dose rates such that the time dependent effects can be directly observed. A low cost method of measuring the total dose hardness of piece parts in the laboratory at requisite dose rates is presented.

### 1.0 Introduction

The "total dose hardness" of a piece part is defined as either a functional or parametric failure. Functional failure is defined as the total dose level at which the integrated circuit simply stops working. Parametric failure is defined as the total dose level at which an integrated circuit parameter exceeds a preset specification, e.g., timing, power supply current drawn, etc. [1].

Using either definition leads to the conclusion that the system will fail if one or more essential components fail. The conventional method of accepting piece parts for use in a strategic system is to estimate the hardness margin of each wafer lot, and reject each lot that has less than the acceptable minimum hardness margin. Data is typically obtained at moderate dose rates (100 to 1000 rad(Si)/s) using laboratory Co-60 or x-ray sources. This is because reactor or accelerator facilities that accurately simulate strategic environments are expensive and difficult to use.

**The missing piece in the hardness estimates is that there appears to be a strong relationship between total dose failure thresholds and the applied dose rate.**

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## 2. Effects of Dose Rate on Total Dose Hardness.

Over the last several years many groups have reported shifts in the total dose failure thresholds for MOS devices as a function of dose rate [1-10]. Typical reductions in total dose hardness range from a factor of 3 to an order of magnitude or more. This effect has been observed across several microelectronics technologies in both unhardened and hardened processes.

The dependence of total dose hardness on dose rate apparently results from the interplay of two phenomena, oxide-trapped charge and interface trap charge. The different types of charges dominate in different regions of dose rate (see fig. 1). In strategic environments failure may occur due to large negative threshold voltage shifts in n-channel transistors caused by oxide-trapped charge. An example of this type of failure is shown in fig. 2. The output of a radiation-hardened analog-to-digital converter to an input square wave is shown as a function of time (1 output frame per ms). At about 350 ms the MOS device is exposed to a 500 krad(Si), 32 ms FWHM reactor pulse with a peak dose rate of about 1.0E+7 rad(Si)/s. The part fails, but then rapidly recovers over the next 150 ms. Simply exposing the part to a 500 krad(Si) total dose in a Co-60 cell does not produce the same integrated circuit response, and thus does not measure the hardness margin of the piece part for strategic environments.

Efforts to develop a piece-part lot acceptance test procedure for strategic applications have focused on correlating integrated circuit parameters with the oxide-trapped charge contribution to the threshold voltage shift that occurs in test transistors at the higher dose rates, and then overtesting at the lower dose rates to compensate for the rapid hole annealing. Figs. 3-5 illustrate a serious problem with this approach. In fig. 3 the Sandia SA3000 microprocessor has been exposed to a continuous dose rate of 2.0E+4 rad(Si)/s until it functionally failed at 9.5 Mrad(Si). At functional failure the radiation exposure was terminated. Shown as a function of the time during irradiation are the power supply current drawn (squares), the package temperature (circles), and the t-RK timing parameter (diamonds). (The t-RK parameter is the time between the falling edge of READ and the rising edge of the next CLOCK-OUT.) Note that near functional failure there is a rapid increase in the power supply current drawn, and a large degradation in the t-RK parameter.

The test was repeated at a linac with a higher, average dose rate of 5.0E+5 rad(Si)/s with very different results (fig.4). The total dose failure level is much higher (16.4 Mrad(Si)), there is almost no change in the power supply current drawn, and there is less degradation in the t-RK parameter. Because the dose rate of the radiation exposure in fig. 4 is higher than in fig. 3, the package temperature rises more rapidly. Higher temperatures increase the rate of annealing of oxide-trapped charge, and thus decrease the amount of oxide-trapped charge that accumulates per unit dose. Thus, in terms of transistor

parameters, preheating the SA3000 during a lower dose rate exposure should produce a response similar to a high dose rate exposure. But this is not what happened.

In fig. 5 the SA3000 was preheated to 125 degrees-C before starting the  $2.0E+4$  rad(Si)/s radiation exposure. Note that the total dose failure level is decreased rather than increased, and there is still a rapid increase in the power supply current drawn near functional failure.

Extrapolating high dose rate integrated circuit responses from Co-60 or x-ray data may be difficult (and impractical) and pose a serious challenge to any hardness assurance program. Simple overtesting in a Co-60 cell may not accurately measure the hardness margin for strategic environments. In ref. [9] it is shown that the SA3000 can be overtested in a Co-60 cell by a factor of 2 to 8 and still not produce the parametric degradations seen in figs. 3-5. Even if such an extrapolation is possible an intimate knowledge of the circuit design and performance, and knowledge of the transistor performance and the integrated circuit failure modes in simulated strategic environments is likely to be required.

### 3. Low Cost Simulation of Strategic Environments.

The problem of correlating the responses of an integrated circuit from laboratory to simulated strategic dose rates can be avoided if an inexpensive high-dose-rate radiation source can be developed. The alternative is expensive high-dose-rate lot acceptance testing at reactor or large accelerator facilities.

Development of a low cost, small electron accelerator will allow the time dependent effects of an integrated circuit's high dose rate, total dose response to be directly observed. The small electron accelerator is conceptually simple -- a large vacuum tube diode. The source of the electrons is a hot filament that produces 1 mA. The filament is tied to a -600 kV potential, and the piece parts to be irradiated are located on the ground plane. The 600 keV electrons have about a 0.1 cm free path in silicon, and have an energy loss of at least 0.3 keV/micron. The energy loss is approximately constant over the first 700 microns depth. The large majority of microelectronics devices are fabricated within this depth. Thus the small electron accelerator produces a continuous radiation exposure of dose rates up to 1 Mrad(Si)/s.

The small electron accelerator can be built for less than \$100,000 because of recent advances in high voltage power supply technology. The power supplies operate at RF frequencies rather than line frequencies. This means that the filter capacitors are orders of magnitude smaller and thus much less expensive than line frequency filters. Higher operating frequencies also reduce the size of transformers and inductors, further reducing the cost and weight of the power supply. Power losses are also reduced at RF frequencies, resulting in cooler operation and increased

reliability. Smaller capacitors are also an important safety consideration. Since the stored energy is proportional to capacitance the power supply can be designed with a stored energy less than 4 joules. Thus the high voltage power supply does not pose a lethal threat to operating personnel. The lower stored energy also reduces the current the output cable and connector must support under short circuit conditions.

Another method of reducing the cost of the high voltage power supply is to use air insulation rather than vacuum or gas-filled encapsulated high voltage components. In addition to reducing cost, the weight of the power supply is reduced and serviceability improved. Corona-free operation in air also improves reliability since catastrophic failure due to creepage paths caused by delamination of the encapsulation is avoided. Atmospheric contamination is reduced by operating the power supply within an enclosure, which also minimizes the danger of serious injury to operating personnel. A 600 kV, 1 mA power supply costs about \$15,000.

Since the electrons penetrate to a depth of only 0.1 cm in silicon, trapped charge will build up in device technologies with insulating substrates, i.e., SOS and SOI technologies. (Biased or grounded silicon substrates permit the electrons to reach the ground plane through the integrated circuit power supply connections.) However, the sapphire and silicon dioxide substrates are sufficiently photoconductive such that dielectric discharges do not occur. The photoconductivities and dielectric constants of these materials are 2.0E-14 and 6.0E-15 (mho/m)/(rad/s), and 3.8 and 8.8, respectively [11]. Assuming no reverse current density due to conductivity the maximum electric fields at 1 Mrad(Si) total dose are 2.3E+5 and 1.0E+5 volts/cm, which is less than the observed threshold for dielectric discharge of 1.0E+6 volts/cm. At an electric field strength of 1.0E+6 volts/cm the reverse current densities are 2.0E-4 and 5.9E-5 A/square cm, which are greater than the current density corresponding to a dose rate of 1 Mrad(Si)/s (7.8E-6 A/square cm). Thus as the electric field builds up, the radiation-induced conductivity allows sufficient current to flow back to the surface to limit the electric field strength to an asymptotic value less than the threshold for dielectric discharge.

Dielectric discharges might occur in other insulating materials used in the fixturing of the device under test. This problem can be avoided by using a metal mask with cutouts such that only the integrated circuit die are exposed to the electron flux, and the rest of the fixture is shielded. The metal mask can be biased positively with a few volts to minimize secondary emission.

The small electron accelerator depends for its operation on the flow of electrons through a high vacuum. The electrons are emitted from the filament (cathode) surface as a result of thermionic emission, which obeys the Richardson-Dushman equation

$$J = 70 T^2 \exp(-52200/T) \quad (\text{A/square cm})$$

where T is the filament temperature in degrees kelvin. The filament is designed for low temperature operation (1800 degrees kelvin) as opposed to a bright filament used for lighting (2575 degrees kelvin). The low temperature increases the filament life by reducing the evaporation rate of the tungsten. The power required to operate the filament is about 30 watts, which can be provided by two 12.5 Ah nickel-cadmium batteries discharged at a 15 A rate. At this discharge rate the batteries can maintain a cell voltage greater than 1 volt for about 30 minutes.

Nickel-cadmium batteries require little maintenance and can take considerable abuse. They can be stored in either the charged or discharged condition without damage. Cycle life is excellent -- over 1000 deep discharges. The batteries can be rapidly recharged, and reasonable overcharging has no detrimental effect.

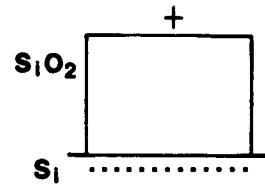
The dose rate to which the device under test is exposed can be controlled by regulating the voltage applied to the filament. Thus a worst-case total dose vs. dose rate history can be implemented using a fiber optically isolated, programmable voltage regulator. A very accurate simulation of a strategic environment could be achieved by colocating the small electron accelerator with a flash x-ray machine, such as a Febetron, to obtain the very high dose rates in combination with the sustained high dose rates provided by the small electron accelerator.

### References

- [1] P. S. Winokur et al., IEEE Trans. Nucl. Sci., NS-34 (1987) 1488.
- [2] A. H. Johnston, IEEE Trans. Nucl. Sci., NS-31 (1984) 1427.
- [3] J. R. Schwank et al., IEEE Trans. Nucl. Sci., NS-31 (1984) 1434.
- [4] P. S. Winokur et al., IEEE Trans. Nucl. Sci., NS-33 (1986) 1343.
- [5] A. H. Johnston and S. B. Roeske, IEEE Trans. Nucl. Sci., NS-33 (1986) 1487.
- [6] D. Schiff, IEEE Trans. Nucl. Sci., NS-33 (1986) 1698.
- [7] J. Thomlinson et al., IEEE Trans. Nucl. Sci., NS-34 (1987) 1803.
- [8] R. D. Schrimpf et al., IEEE Trans. Nucl. Sci., NS-35 (1988) 1536.
- [9] J. S. Browning et al., IEEE Trans. Nucl. Sci., NS-35 (1988) 1557.
- [10] R. Ellis, Proc. 3rd Meeting SUBWOG-6P, Aldermaston, England, Oct. 6-9, 1987, AWE report SUBWOG-6P/M3 vol. 3 (1988) 48.
- [11] V. A. J. van Lint, *Mechanisms of Radiation Effects*, John Wiley and Sons (1980) 239.

**A. SPACE**

1 to  $10^{-5}$  rad ( $S_i$ )/s  
(depending on spacecraft  
shield and orbit)



**SUBSTANTIAL OXIDE TRAPPED CHARGE ANNEALING OCCURS;  
EFFECTS MAY BE DOMINATED BY THRESHOLD VOLTAGE SHIFT  
AND MOBILITY DEGRADATION DUE TO INTERFACE STATE  
FORMATION (rebound).**

**B. LABORATORY**

(e.g. Cobalt - 60 cell)  
100 rad ( $S_i$ )/s



**BOTH TYPES OF TRAPPED CHARGE ARE PRESENT IN LARGE  
QUANTITY; THRESHOLD VOLTAGE SHIFT MINIMIZED BY  
COMPENSATION OF CHARGES.**

**C. STRATEGIC**

**High Dose Rates**



**INTERFACE STATES HAVE NOT TIME TO FORM; THRESHOLD  
VOLTAGE SHIFT DOMINATED BY OXIDE TRAPPED CHARGE  
(Transient recovery).**

**D. STRATEGIC**

**Very High Dose Rates**



**OXIDE TRAPPED CHARGE LIMITED IN QUANTITY BY SPACE  
CHARGE AND "RAIL SPAN COLLAPSE" OF THE APPLIED  
CIRCUIT BIAS.**

Figure 1. Schematic of the different accumulations of radiation-induced charges as a function of dose rate at the oxide-silicon interface in an electric field.

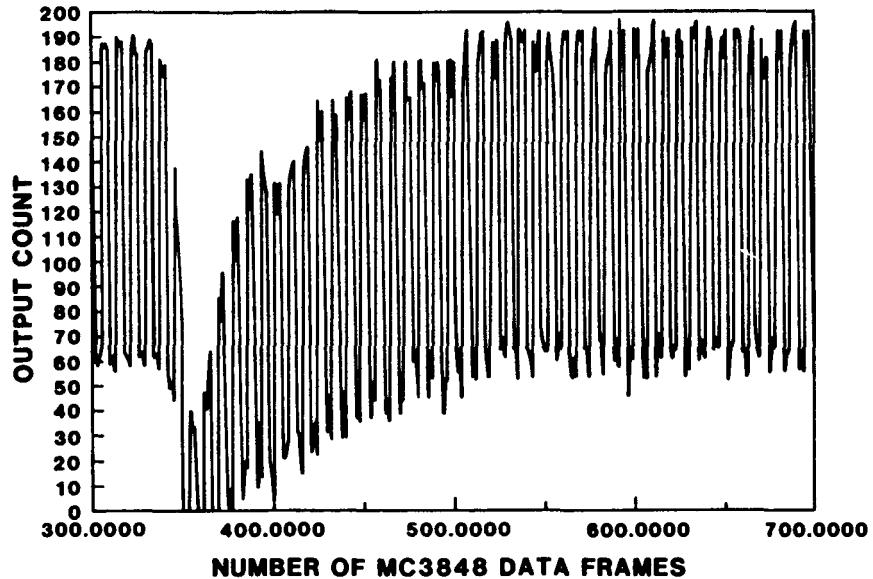


Figure 2. Time dependent response of a radiation hardened analog-to-digital converter exposed to a 500 krad(Si), 32 ms FWHM Annular Core Research Reactor pulse.

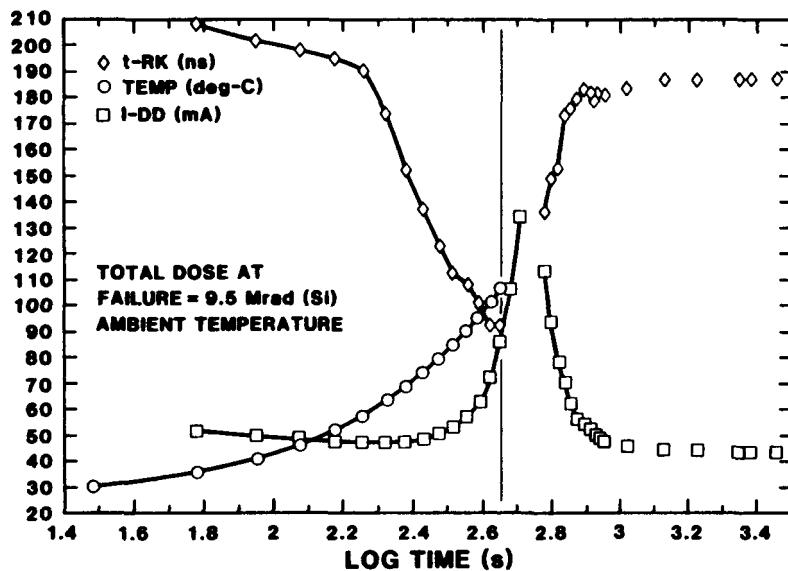


Figure 3. Example of the SA3000 microprocess response during a dose-to-failure test at the Annular Core Research Reactor (2.0E+4 rad(Si)/s dose rate, ambient temperature).

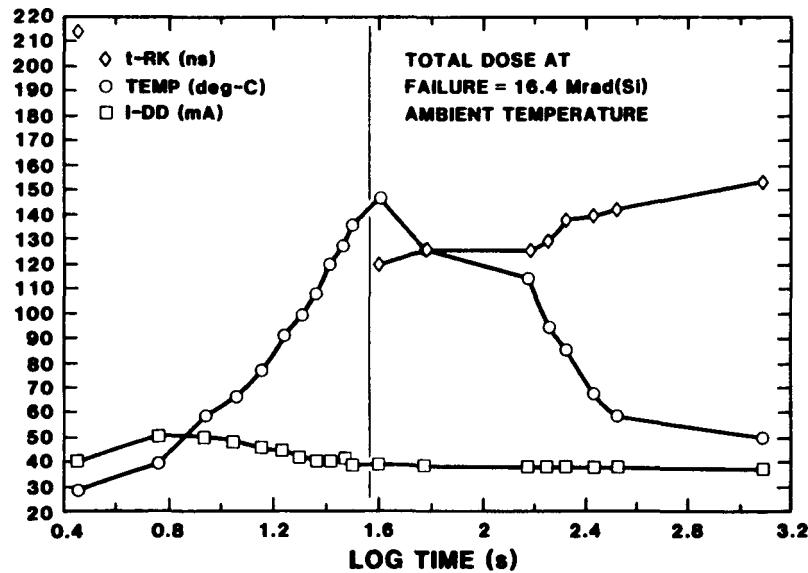


Figure 4. Example of the SA3000 microprocessor response during a dose-to-failure test at the Brookhaven Radiation Effects Facility (about  $5.0 \times 10^5$  rad(Si)/s average dose rate, ambient temperature).

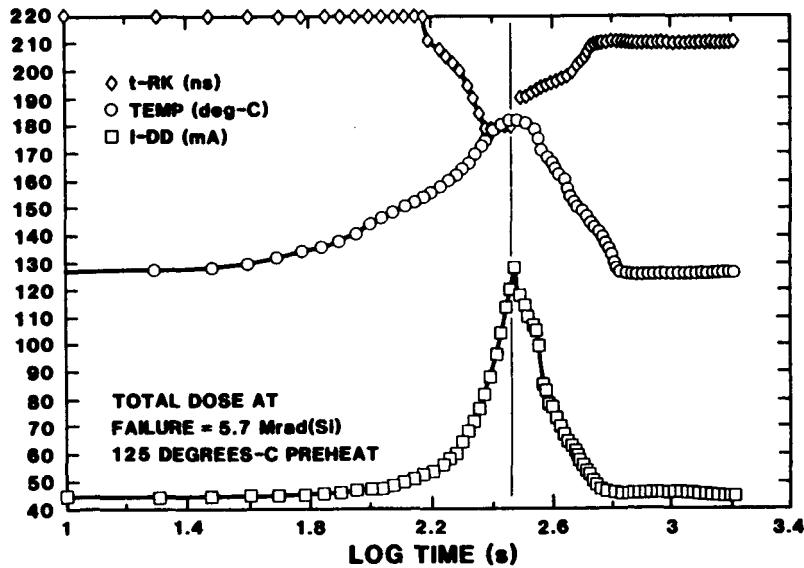


Figure 5. Example of the SA3000 microprocessor response during a dose-to-failure test at the Annular Core Research Reactor ( $2.0 \times 10^4$  rad(Si)/s dose rate, 125 degrees-C preheat).