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Application Specific Tester-On-a-Resident-Chip (TORCH™) Innovation in the Area of Semiconductor Testing

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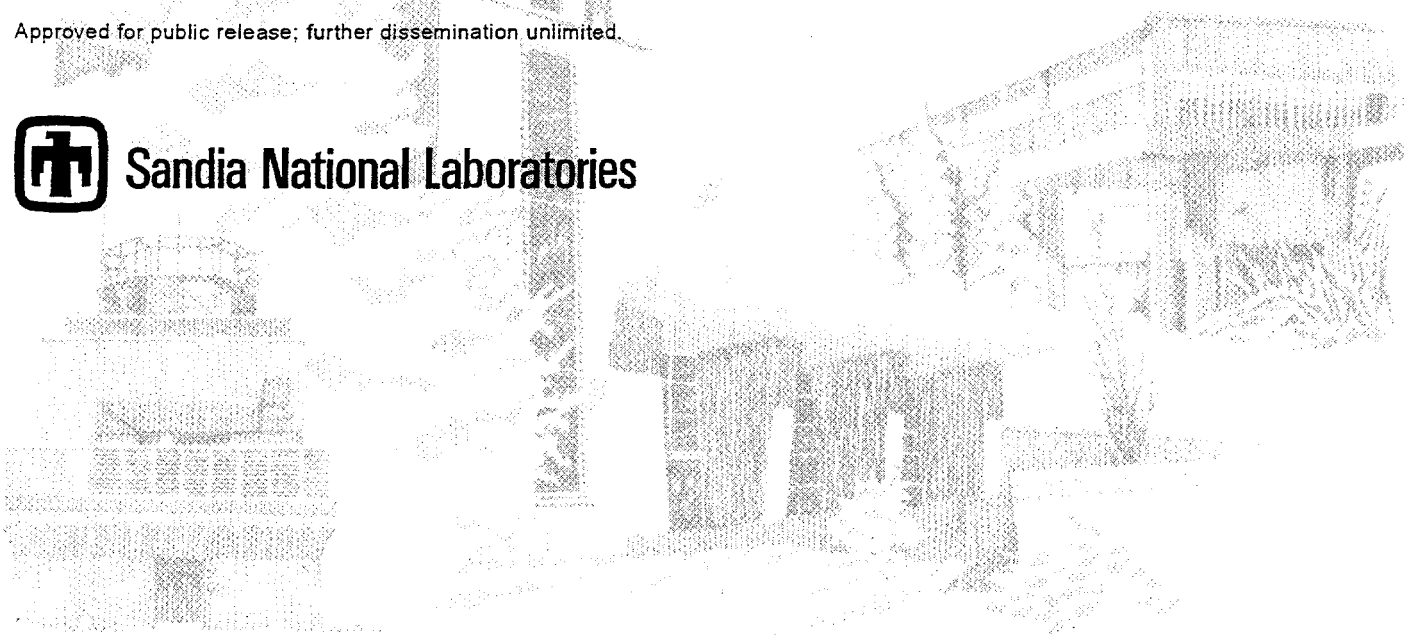

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Application Specific Tester-On-a-Resident-Chip (TORCH™)

Innovation In The Area Of Semiconductor Testing

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Abstract

Manufacturers widely recognize testing as a major factor in the cost, producability, and delivery of product in the $100 billion integrated circuit business: "*The rapid development of VLSI using sub-micron CMOS technology has suddenly exposed traditional test techniques as a major cost factor that could restrict the development of VLSI devices exceeding 512 pins and operating frequencies above 200 MHz*." -- 1994 Semiconductor Industry Association Roadmap, Design and Test, Summary, pg. 43. This problem increases dramatically for stockpile electronics, where small production quantities make it difficult to amortize the cost of increasingly expensive testers. Application of multiple ICs in Multi-Chip Modules (MCM) greatly multiplies testing problems for commercial and defense users alike. By traditional test methods , each new design requires custom test hardware and software and often dedicated testing equipment costing millions of dollars. Also, physical properties of traditional test systems limit capabilities in testing at-speed (> 200 MHz), high-impedance, and high-accuracy analog signals.

This project proposed a revolutionary approach to these problems: replace the multi-million dollar external test system with an inexpensive test system integrated onto the product wafer. Such a methodology enables testing functions otherwise unachievable by conventional means, particularly in the areas of high-frequency, at-speed testing, high impedance analog circuits, and known good die assessment. The techniques apply specifically to low volume applications, typical of Defense Programs, where testing costs represent an unusually high proportion of product costs, not easily amortized.

The **timely industry relevance** of TORCH is evident since Semiconductor International, June 1996 pp. 106 - 111 notes that "*semiconductor testers have improved, but remain large, bulky, expensive systems* and d*efense and commercial sectors have identified reliability testing as becoming an important part of parametric test*."

Table of Contents

Introduction

The Application Specific Tester On a Resident Chip (TORCH) LDRD project pushed the boundaries of integrating complex test functions directly on product IC, thereby eliminating or reducing the need for expensive, large and inflexible test equipment. The key parameter to the development this integrated circuit technology is the mating of a 4-wire IEEE-1149.1 Boundary Scan digital test bus with a (TORCH LDRD developed) 4-Wire Analog bus that allows Kelvin measurements directly on product test die. The boundary scan bus allows us to configure the IC using Commercial Off The Shelf (COTS) controller hardware and software. In addition, the boundary scan bus allows full IC functional and open/shorts test by designing circuits that are boundary scan compliant. With the combination of the boundary scan bus and the analog bus, combined with power and ground, an IC can be fully tested using less than 20 pins or connections to the IC. The 20 pin interface is revolutionary when compared to traditional "bed of nails" testers or other probing methods that require many hundreds of contact pins.

By creating stand-alone circuit blocks, we can easily create custom test configurations from a "library" of cells and modules. This dramatically reduces IC layout time as evidenced on TORCH-3. The basic IC structure used basic cells and building blocks from TORCH-1 and TORCH-2 and completed the entire layout in approximately 4 weeks as compared to 8 to 16 weeks for a typical layout.

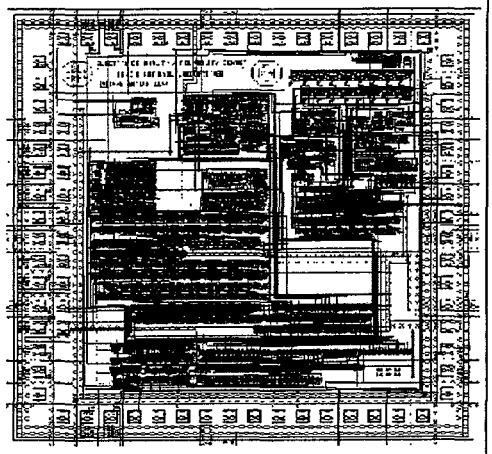
We have shown that automated integrated circuit tests (functional, reliability and parametric tests) were completed using TORCH technology. The focus of this SAND Report is Chapter 3: TORCH -- 3; Boundary Scan Controller IC Reliability and Parametric Test System.

Evolution of the TORCH Concept: TORCH 1, 2 and 3.

TORCH -- 1

Concept definition and verification occupied the tasks associated with TORCH -- 1. In this first year we had to determine how to technically reach our goals of miniaturizing and automating the test of integrated circuits. We chose boundary scan as our primary digital interface because of its low pin count and high clock speed. We developed a 4-wire analog bus for measurements, and created an on-chip switch matrix for routing signals to the test circuits. In addition, we attempted to create IC test building blocks such as the boundary scan Test Access Port (TAP), analog to digital converters, digital to analog converters, timing circuits and counters. We had mixed success in these areas. The control software and hardware were all custom built, and was therefore not easily configured and was difficult to use. An antiquated scripting language was adopted as the control software that made testing the part difficult. In addition, the IC was not designed with ease of use in mind, making the IC difficult to setup and use.

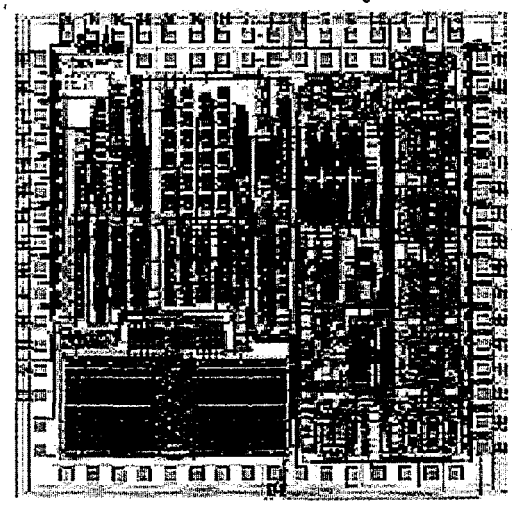
TORCH-1 IC Die Layout



TORCH -- 2

In year two of this LDRD we redesigned the application specific Tester On a Resident Chip (TORCH) Integrated Circuit (IC) and applied it to a real, functional design by applying it to a quiescent current (IDDQ) test function. The new design featured die-to-die communications more appropriate for Multi-Chip-Modules (MCM), an improved boundary scan interface, improved timing measurements, and programmable faults for testing IDDQ measurements. We added a method of measuring impedance of an IC pad, and simplified or improved analog functions. An MS Windows based hierarchical software system (LabVIEW^{TM}) controls the TORCH chip and collects data from internal registers. Control of the TORCH chip is a simple and portable system, involving a PC, COTS PCMCIA boundary scan controller cards, and an open software control system that allows complete freedom of design while adhering to the IEEE standard 1149.1 boundary scan conventions. A logarithmic auto ranging analog to digital converter was developed as part of TORCH-2. This technology has been put to use in other applications.

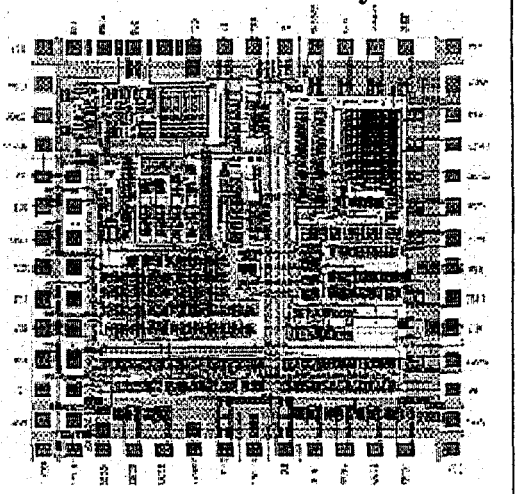
TORCH-2 IC Die Layout



TORCH -- 3: : A BOUNDARY SCAN CONTROLLED RELIABILITY TEST SYSTEM

In year three of this LDRD we compiled the learning from year's one and two and created a functional, simplified and portable IC reliability and parametric test system. TORCH-3 was created using existing boundary scan interface technology from TORCH-2 and analog switching technology from TORCH - 1 and TORCH -2.

TORCH-3 IC Die Layout



We created an automated reliability and parametric test system that automatically configures and tests ganged transistor and capacitor structures. TORCH -- 3 is the culmination of the knowledge gained from three years of research in application specific test IC's. Boundary scan protocols are used to setup the test structures and the analog bus is used to collect the parametric data from the structures under test. The IC control and data analysis system is based around COTS software and hardware. LabVIEW™ is an open software development system that allowed us to develop custom user interfaces that allow a hierarchical assembly of software modules to be developed. The end result is that the boundary scan protocols, key to the operation of the system, become transparent to the user, allowing the tester to concentrate on *testing* the part vs operating the IC. We have re-used the COTS boundary scan controller from TORCH -- 2, and have used external source-measurement units (SMU) for ease of prototyping. Future derivatives of TORCH technology should focus on replacing the external SMU units with on-chip SMU's derived from the logarithmic autoranging analog to digital converter developed in TORCH-2.

Chapter 1 -- TORCH 1

TORCH -- 1 Design

During the first phase, year 1 0f 3, of the Application Specific Tester-on-a-Resident-Chip (TORCH) LDRD, we gained significant experience with many aspects of integrated circuit testing. This knowledge has directly shaped the current implementation, but more importantly development of the first TORCH design has allowed us to evaluate the validity of these decisions, which impacted future designs positively. The details of these experiences are outlined below.

Ideal TORCH Concept

In our original concept, we expected to integrate all testing functions on wafer as an ideal solution. Although this may represent an ideal end solution, it does not represent a near term practical solution. A cooperative methodology, which optimizes the interaction of both on-chip and off-chip functions, appears as a more optimum solution for practical application. In particular, on-chip functions encompass those things that are expensive, impractical to do off-chip, or simplify what is needed off-chip.

A simple review of testing methods can clarify this point. The simplest testing method, referred to as wiggle testing, requires just proving functionality of all individual circuit functions. Wiggle testing suffices for many applications where part specifications are well within process variations and product must be assured good before next assembly application to avoid impacting yield. In general, wiggle testing techniques are easily achievable on wafer and are not process dependent. The next level of testing is referred to as acceptance testing and involves not just exercising a block for functionality but ensuring that the block functions within some predetermined bounds. Acceptance testing infers a designers uncertainty of a product's repeatability within the manufacturing process. From a testing standpoint, the uncertainty of product repeatability also infers uncertainty in tester repeatability when integrated on chip and a dependence of product as well as tester on specific technology. So while on wafer test circuitry can simplify and maybe even implement acceptance tests there is usually be a reliance on external stimulus and measurement functions. Finally, the highest level of testing referred to as parameterization, requires a degree of sophistication and precision that elude practical on chip integration, resulting in rapidly diminishing return of both design and layout resources.

Consider the following example of a design involving a 12-bit A/D, pushing the limits of the process technology of choice. A simple wiggle test may involve exercising the A/D with a generic 6-bit DAC, designed as a generic reusable and easily repeatable block. This test is not going to ensure ideal performance of the A/D, but does verify if it functions as an A/D. An acceptance test for this part might involve application of a few known (meaning reference or external) stimulus while looking for known responses such as specific output codes. Such a test is designed to prove the integrity of the A/D under expected use conditions. Parametric testing for this part might involve a very sophisticated test to characterize specific error terms such as integral and differential linearity. Such testing not only ensures the integrity of the part but accumulates a history of design margin over time.

The testing problem being pursued in this research focuses on application specific integrated circuits (ASICs). Full custom, high-volume products, such as memories and processors, can leverage economics of scale to amortize testing costs. But low volume ASICs, typical of DP products, require expensive testing without the advantage of scale to amortize. So based on the mentioned standard techniques and the target application, the ideal wafer level testing methodology to pursue might be called **cooperative testing**. That is, combining a set of on-wafer and off-wafer testing methods, stimulus, and measurements to achieve a high degree of testing with a minimum of design and test engineering cost investment. The basis for this approach involves a generic mixed-signal test port that directly supports lower level wiggle tests on chip and indirectly supports more sophisticated testing through a common interface to off chip hardware.

Boundary Scan Enhancements

We chose the IEEE standard 1149.1 boundary scan interface as the basis for our testing interface. No other testing interface enjoys as wide an acceptance and breadth of application. However, the boundary scan definition encompasses only digital design. To support analog, mixed-signal, and die-to-die circuits we developed a few enhancements to extend this interface. Our implementation works within the boundary scan specification to ensure compliance with all existing requirements.

DIE-TO-DIE PROTOCOL

In the first year effort, we have successfully defined a die-to-die protocol. The protocol as defined has direct application to wafer level development. This extension requires circuitry and operations beyond the IEEE 1149.1 boundary scan definition, but does not conflict with normal operation. A simplified version has application to board and multi-chip module designs.

By the protocol, a given die, termed the **device under test (DUT)**, is probed and tested via its boundary scan port. Assuming success, the controller can instruct this die to become what we term a **Host** die. In doing so it passes further test instructions onto a neighboring die, which now represents the DUT. Again assuming success, the present DUT is instructed to act as a **Relay** die so that the controller now interfaces to the Host that in turn interfaces to a Relay that in turn interfaces to a new DUT. Theoretically, with reasonable yields this process can continue until all the functional die of the wafer are connected in a single continuous chain and all have been tested. The boundary scan interface arbitrates, by direct instruction register control, to which neighboring die it communicates. If at any time throughout this process the Host or Relay communicates to a failed die site, other combinations can be tried to reroute the data stream until all possibilities are exhausted.

The implementation of this protocol for wafer level represents a probable worst case where each die must be capable of communicating via an external boundary scan port as well as each of 4 internal ports from the adjacent die. This suggests that you only need to probe one die on an entire wafer, whereas in conventional testing you must probe every die. Although a single probe site does not guarantee success, for a high yielding process it is likely that testing requires only one additional probe per wafer. Support of the die-to-die protocol results in hardware overhead for deciding which ports are functional and ensuring robust data flow in the event that a given

test port is terminated to a failed die. Support of these features leads directly to overhead in boundary

scan instructions as well. Furthermore, the complexity of arbitrating multiple neighbors has little use outside wafer level that justifies the complexity.

TEST PORT DEFINITION

We have established a standard test port definition that is suitable for a very high percentage of applications and supports both analog and digital functions.

Table 1 defines the pinout of the port. Pins 1-4 represent a 4-point Kelvin force/sense analog stimulus and measurement port. Pins 5 and 6 are reserved for an optional external reference. Pins 7-10 represent the IEEE boundary scan port definition. Pins 11-16 represent standard power supply voltages. Pins 17-20 are unused but intended for application as a second analog port if needed. The 2 by 10 pad arrangement was chosen for compatibility with existing test structures and probe equipment.

Function	Pin	Pin	Function
F+	1	20	unused
S+	2	19	unused
S-	3	18	unused
F-	4	17	unused
[REF+]*	5	16	VSSA
[REF-]*	6	15	VDDA
TDO	7	14	[VSSX]*
TDI	8	13	[VDDX]*
TMS	9	12	VSS
TCK	10	11	VDD

* signals marked in [] are optional

Table 1: Test Port Definition

The test port by itself seems like a trivial achievement, but in fact it represents a major simplification to the testing process. The unique pinout of ASICs dictates much of the hardware development and fixturing for testers. Analog or mixed-signal designs magnify this problem many folds because the loading sensitivity of most analog nodes is significantly higher than digital signals. For example, standardized opamp tests have existed for years, but when testing ASICs that incorporate various numbers of amplifiers and essentially random pinouts it requires custom test fixturing and switching networks for testing every ASIC. However, by making all the inputs and outputs accessible through a common interface, a common fixture can test each amplifier in succession independent of whether the ASIC has 3 or 13 or however many amplifiers.

The digital portion of the test port represents a standard boundary scan test port, which supports digital testing as well as control of the analog interface. The analog port allows for any precision

single-ended or differential 4-wire measurement or force and sense function. Mixed-signal tests are implemented by congruent operations of both the digital and analog ports.

The test port works directly with an on-chip crosspoint switch that ensures necessary internal nodes are connected as needed to the common location of the test port.

IDDQ Testing

The TORCH 1 design demonstrates an ability to perform full chip IDDQ testing under boundary scan control.

IDDQ testing allows for the detection of potential failures such as gate oxide defects that cannot otherwise be detected. The TORCH 1 design implements support for IDDQ testing by a dedicated 2-bit register. One bit, TQEN, serves to disable the quiescent power of all on-chip analog functions to place the chip in a zero power static condition. A second bit, TQV represents an independent test vector for controlling the state of digital nodes left floating by unpowered analog circuitry thus exercising all digital states. TQV can also be used to force the state of all internal latches to simplify 100% node toggle coverage necessary for IDDQ testing certainty. The IDDQ register is reset by a boundary scan reset sequence assuring a fully operational part under normal reset operations.

Real Time Measurements

By taking advantage of a generally unused state condition in the boundary scan controller we have implemented the ability to make real time frequency and timing measurement, either independently or in conjunction with analog signals.

When the TAP controller is left in the PAUSE state, the boundary scan specification requires that the Test Data Out (TDO) line be tristated. The TORCH 1 design extends this definition to allow the TDO line to be active under direct command (but otherwise default to a tristate condition). In this condition, real time signals, such as an on-chip oscillator, can be applied to the TDO line for direct external observation or measurement. During this time the data pattern on TDO is invalid and simply ignored.

In addition to outputting real time signals on the TDO line, we utilize the signal applied to the boundary scan test clock, TCK, as an external frequency reference. The initial TORCH design relies on TCK being continuous.

Software Design

We wrote an MS Windows compliant application using Visual Basic, implemented a test interface, and demonstrated a complete low cost system that can control "a chain of devices under test" (i.e., PC to die-to-die communication) via the parallel port of a standard PC or laptop. The software was written in a modular abstract form to support future development and enhancements.

Wizzard

The Wizzard represents the top level Windows application. It implements an integrated development environment that allows the end user to develop and debug "test scripts." The

current implementation involves simple text editing features and run-time transcripting to assist in observing execution of the scripts and data collection.

SCRIBE

The Scribe module implements a customized tiny BASIC interpreter that converts Scribe Command Language (SCL) scripts of test commands into sequences of functional boundary scan operations. Commands in SCL represent simple abstract "boundary scan independent" functions like RESET, MOVE, and SET. Data streams are automatically converted between various formats to support simple numeric data streams as well as virtually unlimited length data streams represented by strings.

SCANLIB -- SCANLIB.BAS

This module connects the low level hardware drivers to a high level test command language. This level of the code implements all of the boundary scan functionally to abstract both the hardware and test command's from the intricacies of the boundary scan definition. ScanLib takes simple SCL operators and data streams and provides all the necessary formatting and parsing needed to generate low level data streams for dumb hardware interfaces.

DRIVER -- PPLIB.DLL

This module represents a series of low level routines for interfacing the PC hardware interface to Windows. The specific drivers only understand the specific hardware to which they interface, not the data. All data passes through the interface independent of its content, thus abstracting the interface from both the DUT and the test functions. The current code supports a standard parallel port interface as a dynamically linked library. Other drivers can easily be added as the need arises.

PC Interface Design

We successfully designed, built, and used a wire-wrapped version of a hardware interface for application between a PC parallel port and the TORCH die. The TORCH design works in conjunction with a PC based controller. This requires a custom interface function to connect the standard boundary scan test port to some standard PC interface.

Parallel Port

For the first supported interface, we selected the parallel port. This interface is relatively simple and provides a relatively high data throughput for testing. The design actually implements two boundary scan ports. One is intended for use in testing and the other implements an 8-bit I/O port for support functions using a commercial boundary scan compliant octal buffer chip. Additional capability exists through unused interface lines to expand this interface to include simple, low-cost analog stimulus and measurement.

Development Changes

Through the development of the first TORCH design, we made many tradeoffs. The next iteration implemented several changes intended to simplify the integrated circuit and make the test modules and cells repeatable across a broad range of technologies.

SINGLE DIE-TO-DIE BOUNDARY SCAN PROTOCOL

An alternative approach, yet untried, offers more utility and simpler die-to-die implementation. It involves supporting only a single connecting port instead of the four required for adjacent die. In this approach a die either acts as a DUT or pass through much like the boundary scan standard and does not have to arbitrate or discriminate multiple paths. Once tested, a die is instructed to add the next die to the chain, assuming the specific chain path was predetermined. This is not applicable to wafer level, but directly applicable to both multi-chip modules and board level designs where a single scan path is normally implemented. The advantage of this approach over the standard boundary scan methodology is that this approach allows testing to verify functionality of all die in the loop up to a point of failure whereas the standard boundary scan interface requires all devices in the chain to be functional or the method fails leaving little indication as to the point of failure.

DUAL REDUNDANT BOUNDARY SCAN INTERFACE

The boundary scan interface is intended for increasing integrated circuit test accessibility, but there is no reason why the same interface can not be used for normal control and data flow of a given design. This is achieved without modification of the standard design. However, many Sandia weapons and space applications need very reliable communications. In support of this we can demonstrate a dual redundant interface.

BOUNDARY SCAN PAD CELL(S)

The initial TORCH design does not implement normal pad cell digital scanning. This is a mature boundary scan concept and therefore was considered a low priority. This was added to the next design for completeness. A possible enhancement allowing measurement of pad impedance may impact this cell design.

REAL TIME MEASUREMENT

As noted, the TORCH 1 design uses the boundary scan TCK signal as a frequency reference, which must be continuous. A somewhat ambiguous specification requires that the testing interfaces must be able to stop the clock for the benefit of the part under test. Unfortunately some vendors have interpreted this to mean the interface can stop the clock for its benefit. Although both cases comply with the boundary scan definition there exists an incompatibility between the TORCH 1 design and some commercial interface products. We removed this restriction in the next version of the design.

SIMPLIFIED ANALOG FUNCTIONS

The present A/D and D/A designs represent very extensive designs in an attempt to parameterize on-chip circuit elements. Simplified designs are required in order for TORCH to have technology independent application. The approach for TORCH -- 2 next design was to create simple, repeatable, and portable "building block" designs. The same philosophy was applied to all the analog functions. The A/D design involves a range encoding 4-bit Log Base 2 converter that offers reasonable accuracy across a very wide dynamic range. Simple calibration sources were included. A small DAC and FIFO were used to construct a simple arbitrary function generator.

SPECIALIZED TEST CIRCUITS

We have identified a few specialized test circuits that have broad application and merit investigation for solutions to certain industry testing problems. These include:

1. **High-Speed timing Measurement.** A circuit to make very fast timing measurements in the range of a few nanoseconds with sub-nanosecond resolution. This has direct application to optimizing SRAM design. A charge integration scheme shows promise.
2. **Pad Z Measurement.** A circuit to measure impedance at I/O pads has application in modeling and debugging layout related problems such as shorts and opens as well as use in characterizing various technologies.
3. **Operational Amplifier Test Circuit.** A standard opamp test circuit has existed for many years. It requires location of external components close to the device under test. ASIC pinouts make this impossible without custom fixturing. In conjunction with the analog port a solution is possible.
4. **RF Port.** As IC speeds increase the need to access RF type signals become increasingly important. An adaptation of the analog port or separate RF port is necessary to support such signals.
5. **IDDQ Measurement.** Attempts to implement on-chip IDDQ measurements have not shown much success to date. There is potential for demonstrating this function completely under BS control, suggesting possible in-situ testing, including stockpile assessment.

Software Upgrades

Based on our test experiences, implementation of all potential test functions on an integrated tester is improbable with the visual basic based scripting software system. An open system such as LabVIEW™ replaces the year 1 custom system.

PC Interface Mods

Analog portions of the PC interface have not been completed and the digital portion has seen some modifications. Plans are to implement a breadboard of the analog functions to verify the design and then develop a PC board layout for construction of a new interface. A second effort may involve design of a buffered interface chip that can automate the software overhead associated with formatting and parsing the BS data streams. This part has direct use in future applications incorporating BS. The part needs to support TMS and TCK control, variable data register size, continuous data looping, and block data buffering.

General Lessons Learned

In the development of TORCH several experiences led to a better appreciation of specific testing problems and sharpened our understanding of the solutions.

- **D/A and A/D Design.** Design of both DAC and ADC converters that have rail-to-rail dynamic range represent extremely difficult designs. In other words, for a part designed to operate from a standard 5 volt supply, only 5 volts is available to the analog circuits to achieve measurements that may have to range from 0 to 5 volts. This makes for very challenging design. At some (early) point it becomes obvious that the testing function requires more resources than the application design and value to the tester being on-chip is diminished by the effort required to do so.

- **Parametric Measurements.** We had originally anticipated that "simple DC parametrics such as threshold voltage" represented an easy task. But such testing requires maximum measurement resolution and sophistication to achieve.
- **Boundary Scan Interface.** The simple interface of the boundary scan Test Access Port (TAP) led us to underestimate on-chip TAP Controller design and software development needed. Still, we believe the flexibility and standardization of this interface proves it was the right choice.
- **Test Circuits.** We implemented too many difficult functions without sufficient test circuits and probe points to allow for adequate debugging of individual functions.
- **Degrees of Freedom.** What we anticipated as a fairly focused solution with a broad vision of application still involved many more degrees of freedom than anticipated. Our future focus now narrows toward a specific approach having more immediate application.
- **Secondary Factors.** Necessary libraries and design procedures were not sufficiently developed at the start of the project to support the magnitude of this design.

Test Results

Feedback from TORCH 1 wafer testing.

External Test Setup Comments: Wizzard Enhancements.

1. Wizzard should detect when the PPIU is turned off.
2. Wizzard needs to automatically save the screen setups (via a checkbox in preferences) . It needs to save sizing info, and the active script.
3. Add Menus to allow changes to the current *.dev and *.inf files.
4. Need a user selectable "HOT KEY" on the keyboard to run scripts.
5. Add an option to repeat a script "X" times and auto record data into Excel or Access.
6. Add an HPIB interface to automate voltage/current stim. and data collection from voltmeters, counters, scopes, etc.
7. Add a function to autodetect the Parallel Port address and open and modify the parallel *.inf file on command.
8. Wizzard needs to 'clean up' the parallel port when exiting.
9. Need an optional direct register load function. Assign a register name and length and allow bit toggling, to use after running a setup script. This allows dynamic register loading. <<< A key feature making testing TORCH-1 difficult.
10. Add a "Crosspoint Grid" to easily open and close crosspoint switches with the mouse. <<< A key feature making testing TORCH-1 difficult.

IDEAS for the next TORCH Interface, I.E. TORCH-2.

1. Develop a standard test box with Boundary Scan to Boundary Scan interface, and miniaturize the PC - Boundary Scan interface. Allow multiple interfaces to connect to the Test Box.
2. Reduce the size but increase the functionality of the current Parallel Port Interface and Test Box. Add analog stimulus and measurement to the Test Box.

3. Improve power control, automate battery charging, and go to an external battery pack for the Test Box. Add PPIU power control via Wizzard (Scribe Command).
4. Develop a PCMCIA interface for the Test Box. (We chose to eliminate the parallel port interface completely for TORCH-2 and used a COTS PCMCIA boundary scan interface from Corelis Corporation.)

Chapter 2 - TORCH 2

TORCH 2 DESIGN FOCUS

Based on decisions made by the principal investigator at the beginning of the FY 1996, the following outline provided a baseline for the TORCH 2 Design. **The focus of the FY 1996 LDRD was to demonstrate on-chip IDDQ Measurement and its application at board level.** The design effort involved the following aspects:

- **Multi-channel IDDQ Measurement.** This involved muxing several channels into the A/D with at least 8 channels for off-chip measurement of other die.
- **IDDQ IREF and Calibration Functions.** Standalone block to exercise the A/D for sanity.
- **Log Base 2 A/D.** A range encoding 4-bit A/D design with a dynamic range in excess of 50K:1.
- **Analog IDDQ Test.** Demonstrate bias current measurement for an independent analog circuit function.
- **Known Fault Test Circuit.** A simple logic block with controllable fault conditions.
- **Pad Z-Measurement.** Circuitry to measure pad impedance: resistance from any pad to any pad and capacitance loading of any pad.
- **Simplified TAP Design.** A simplified TAP design in comparison to the existing design, but implemented in multiple versions to demonstrate redundancy, single die-to-die protocol, etc.
- **Pad Cell.** Boundary scan pad cell design.

IDDQ Measurement Issues

- **Measurement Resolution.** It is believed that what is required is well within the reach of a technology independent solution using an autoranging A/D topology.
- **Distributed Measurement.** IDDQ measurement for large VLSI designs is masked by background leakage. The proposed approach implements distributed measurement seen as a work around to this problem.
- **IDDQ Measurement involving Analog Circuits.** The relatively large bias current of analog circuits complicates IDDQ measurements.

Project Accomplishments for FY 1996

- We met all technical goals, all FY 96 milestones were completed.
- TORCH technology was spun-off to another program.

Fiscal year '96 was the second phase of the TORCH LDRD. We gained insight from the first year that positively impacted our second year design into a more general, technology independent design of the basic TORCH building blocks. Additionally, we included more specific applications such as Iddq fault testing and PADZ impedance testing. The table below summarized the performance and schedule objectives for the tasks defined in the original and continuation proposals. A more detailed description of the technical accomplishments follows.

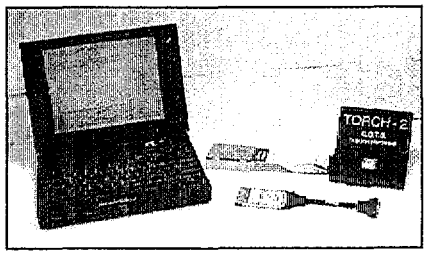
Summary of Accomplishments

Task	Performance	Schedule	Comments
Simplify TORCH-1 Architecture	Exceeded Goals	Due: 1/96 Done Early: 12/95	IEEE Compliant, Analog Port, Re-useable components
Die-to-Die Protocol for MCM's	Met Goals	Due: 1/96 Done Early: 12/95	Improved design, simplified usage.
Design Specialized Test Circuits	Exceeded Technical Goals	Due: 1/96 Done: 4/96	All functions in, plus added optional functions.
Fabricate Prototype	Met Goals	Due: 4/96 Rec'd: 7/96	18,000 Transistors. Had to change Foundry mid-year.
PC Interface and Software	Exceeded Goals	Due: 4/96 Done: 4/96	Interface + Software in place. Final Hardware in Fab.
Control TORCH Chip	Completed	Done: 7/15/95	Test Software / Hardware in place, awaiting TORCH-2 ICs.
Demonstrate Die-to-Die for MCM testing	Completed	Done: 8/2/96	Test Software / Hardware in place
Perform Pad Impedance Measurement	Completed	Done: 8/16/95	Test Software / Hardware in place
Perform Iddq Testing	Completed	Done: 9/15/96	Test Software/ Hardware in place

Our specific accomplishments for the second year include:

1. **We applied the TORCH topology to a "real functional design" as a refinement to on-chip testing**. A direct digital synthesizer (DDS) is used to generate arbitrary signals by storing a digitized sine wave in memory and using digital signal processing techniques to pass samples of the sine wave through a digital-to-analog converter (DAC). We designed a DDS with TORCH circuitry to test a mixed-signal (both analog and digital) integrated circuit. This is a significant IC with digital logic, analog, random access memory (RAM), read only memory (ROM) built in CMOS technology that also used bipolar junction transistors.
2. **We simplified the die-to-die communications making it more applicable to MCM and circuit board configurations**. The first year we demonstrated a die-to-die protocol for the wafer level. This used a lot of overhead circuitry to allow for bypassing faulty, untested devices. We removed the overhead and enhanced the die-to-die circuitry to accommodate communications between tested, known-good devices used in multi-chip modules and printed circuit boards.
3. **We simplified the analog functions of TORCH**. The second year TORCH design used simpler, repeatable analog modules that are portable to future designs. An example of this is the analog port which is a four wire bus traversing the IC that may be used for external four point Kelvin measurements.

4. **We improved the boundary scan interface.** We improved several areas of the interface. The boundary scan on TORCH is now fully compliant with IEEE standard 1149 and is no longer dependent on a continuous TCK signal. We have boundary scan pad cells for IC to IC interconnect testing as well.
5. **We simplified and improved the timing measurement unit.** In the original TORCH there was one timing measurement unavailable because of a design oversight. We have corrected this and in the process simplified the boundary scan-to-timing measurement interface.
6. **We designed a logarithmic analog to digital converter.** We have incorporated a logarithmic analog to digital converter for measuring signals over a very broad dynamic range. *This design is already being used in an application specific integrated circuit for a real system. We are seeing immediate payback to TORCH research investments.*
7. **We designed a PADZ cell for measuring pad impedance.** This cell was used to measure the impedance presented to the interface pad of an IC used in MCM or on printed circuit boards. This aids in characterizing MCM interconnects leading to better simulations and virtual prototyping of multi-chip modules. Eventually, this may be used to evaluate the reliability of printed circuit boards, solder joints, and MCM interconnects.
8. **We designed programmable faults for Iddq testing.** The second year TORCH design has seven programmable faults that may be turned on or off through the boundary scan interface. These faults represent each of the fault classes found in CMOS processing. This is useful for evaluating the Iddq testing method of detecting faults in integrated circuits.
9. **Control of the TORCH2 chip from a PC using Commercial Off The Shelf (COTS) hardware and software.** We continued to use the IEEE 1149.1 Boundary Scan interface and have added a COTS mixed signal digital/analog interface to support signal acquisition. In addition, the Boundary Scan interface and the digital/analog interface are implemented in PCMCIA format for ease of use. The boundary scan controller was provided by Corelis Corporation Model #PCMCIA 1149.1 and the digital/analog interface was provided by National Instruments, model #DAQCard 1200. The LabVIEW™ programming environment version 3.1.1 under Windows 3.1 provided the platform for the control software. The software structure is hierarchical and is totally integrated with the IEEE-1149.1 and IEEE-488.2 standards and our mixed signal interface. A PC board interface was designed and built which allowed connections to the Corelis 1149.1 boundary scan controller, the National Instruments DAQCard 1200 d/a board and the TORCH 2 IC. A socket was provided to accept a 68 pin J-lead package that held the TORCH 2 die. Packaging of the TORCH 2 die in the 68 pin J-lead package was done at the Microelectronics Development Lab at Sandia.



Control of TORCH-2 is via miniature COTS hardware and software for portability.

Main Conclusion and Findings

We verified operation of the improved boundary scan interface, verified IDDQ test circuits, and extensively tested the logarithmic analog to digital converter. The simplified analog switch matrix worked, and we made an external pad impedance measurement.

We found design margin problems in a critical timing generation block, compounded by converting our design to the new Orbit manufacturing specifications. This rendered some of the mixed signal modifications inoperative. This problem has since been corrected in design and we submitted modifications to our production facility. Follow on testing verified that the fixes were effective.

Results and Recommendations for TORCH 3

The digital circuitry in TORCH 2 was verified operational via boundary scan testing. We are confident that the TAP controller can be used in future designs. Measurements show that the timing circuit is not generating proper clock signals to drive the analog to digital converter circuitry correctly, preventing accurate measurements in-situ. Circuit loading was found to be higher than simulations indicated, requiring increased rise time and drive strength.

We now have a better appreciation of the intricacies involved in designing, simulating and producing complex mixed signal circuits such as the timing generation block that gave us problems. The goals for TORCH 2 were excessively high due to the overly ambitious project engineer in FY 1996.

Chapter 3 - TORCH 3: Boundary Scan Controlled IC Reliability and Parametric Tester.

Focus of Sandia Report

The third year of the application specific TORCH IC culminated by automating reliability testing and parametric testing of IC structures, specifically transistors and gate oxide capacitors. As such, TORCH -- 3 is the state of the art. In this chapter we provide significant detail about the construction of the entire system, our test plans, and results from testing the structures. Thus, this chapter is the focus of the Sandia Report.

Scope

This chapter defines the system requirements and IC design goal requirements for the third generation application specific Tester-On-a-Resident-CHip (TORCH-3) evaluation device. The focus of this design is to develop an integrated test system to perform IC reliability and/or parametric tests on chip. The final products are a stand alone wafer level or packaged part test system and a SAND report detailing the outcome of the mixed-signal design and test project. Motivators for this project include low cost and simplified reliability testing, more effective testing by ganging structures, and automated PC-based reliability testing.

Concept

The TORCH-3 design implements a self contained reliability test system for executing hot-carrier and oxide degradation tests. All control occurs through an IEEE Std.1149.1 boundary scan compliant serial test port. Auxiliary test stimulus and measurement occur through a 4-wire Kelvin analog port. In essence, TORCH-3 demonstrates mixed-signal control and test of reliability structures. The Hot Carrier structure is also be used to perform basic transistor parametric tests.

Application

TORCH-3 test philosophy and test procedures guided the design goals. The **objective** of the project was to demonstrate simultaneous stressing and sequential parametric measurement of ganged reliability structures, to be accomplished utilizing the technology and knowledge gained in year's one and two of this LDRD.

The **goal** of this LDRD is **proof of concept** of embedded reliability testing. Reuse of existing test structure designs, proven TORCH circuit designs, and working control hardware and software (from TORCH-2) were maximized, with ease-of-use a primary goal. The TORCH-3 design maintained the existing standard 20-pin mixed signal test port. The fabrication facility was Orbit, as this is the process currently applicable for both TORCH circuitry and test structures.

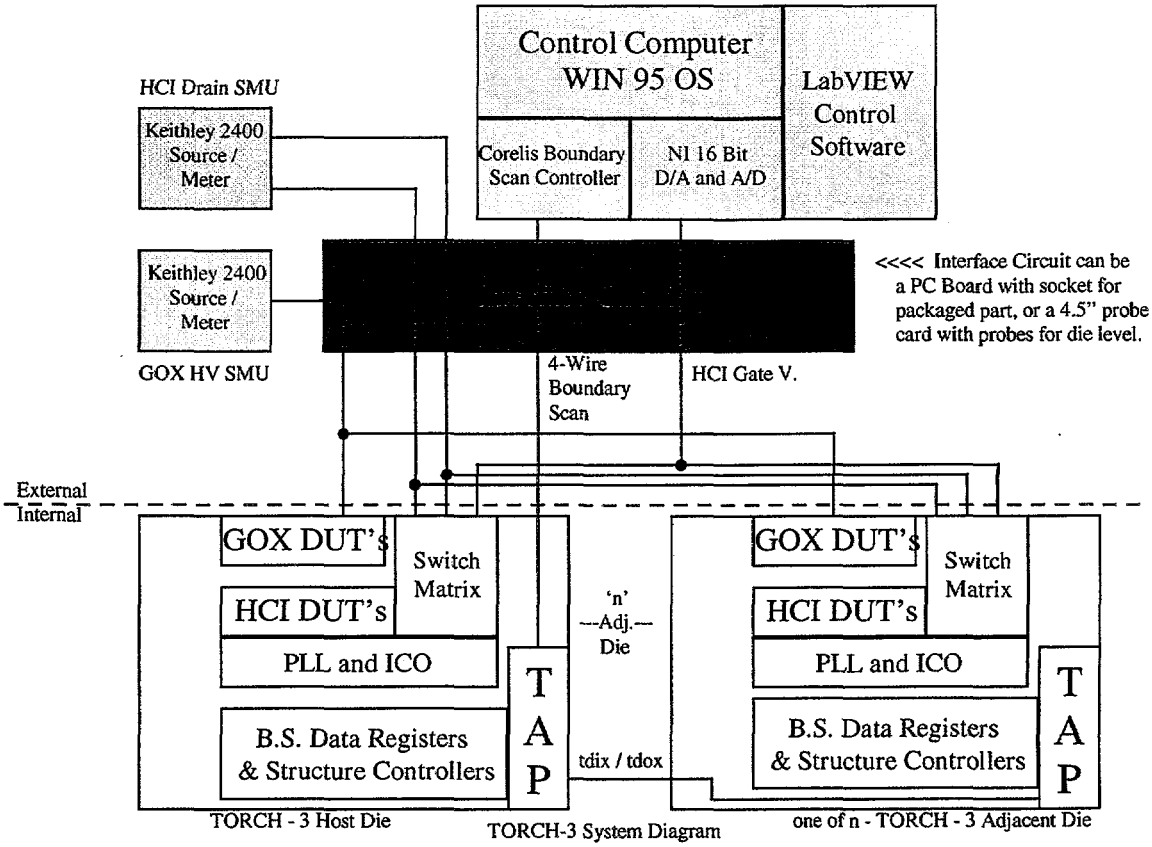
Programmatic Alignment

The final version (year-3) of the Application Specific Tester on a Resident Chip is the basis of a solution to the classic problem of the self-monitoring system. When tied into current technology initiatives for improving the reliability of the nation's stockpile electronics, this program becomes essential. TORCH-3 becomes one-third of an extremely valuable technology triad. The

technology triad consists of the TORCH-3 Reconfigurable Tester, Precursors to Failure Reliability Modeling, and Advanced Test Structures. The end result of combining these three technologies to culminate in a system that can interrogate itself for basic and advanced health indicators and report status. Limited self-repairing capabilities can now be done.

System Components

TORCH - 3 SYSTEM DIAGRAM



TORCH -- 3 SYSTEM DESCRIPTION

- The TORCH-3 system consists of external and internal components that comprise an integrated system to accomplish the feat of inexpensive and fast reliability testing. The combination of off the shelf components and the modular architecture make it an effective tool for reliability testing. The system is designed around ganged stressing of Gate Oxide Capacitors (GOX) and Hot Carrier (HCI) stressing of N and P type FETS. The external components provide the stimuli and measurement and control capabilities, while the IC provides the GOX and HCI ganged structures, boundary scan compliant control hardware, on-board current controlled oscillators for AC stressing, and appropriate switching matrices.
- External components include a host computer, operating system, LabVIEW™ software environment, a Corelis Boundary Scan Controller (BSC), two Keithley Model 2400 Source / Measurement Units (SMU), a National Instruments 16-bit A/D and D/A converter with 16 bit counter, and an interface board.
- The interface is comprised of a mixed signal interface comprised of a 4-wire boundary scan interface for digital control, a 4-wire analog interface for stimulus and measure. Main

components include a boundary scan state machine and instruction decoder (TAP), boundary scan data registers, a current controlled oscillator (ICO) and phase lock loop (PLL), and the GOX and HCI ganged structures. The analog signals are also routed through switch matrices.

CONTROL COMPUTER/OPERATING SYSTEM

The control computer has the following characteristics: Desktop or Laptop (Pentium class), >20Mb ram, >800Mb HD, two PCMCIA ports, CD_ROM, 1 parallel port for connecting NI IEEE-488 interface. The operating system for TORCH-3 control computer consists of Windows 95 with LabVIEW™ 4.1 installed.

CONTROL SOFTWARE

The control software is National Instruments' LabVIEW™ 4.1 based. This allows a hierarchical data structure to be created and maximizes the ease of use of the software. In addition, LabVIEW™ based control software allows dynamic connectivity to Windows based data analysis software, an essential feature for reliability testing. Reuse of TORCH-2 control software architecture was maximized. The software allows automatic testing of the TORCH-3 (T3 IC) reliability structures, and is based on the boundary scan register arrangement of the T3 IC. The control software works in conjunction with the Corelis boundary scan function dynamic link library, and the National Instruments WinDAQ95 data acquisition and control software. The Corelis library and the National Instruments software are a sub layer of the control software, and is transparent to the user. An understanding of the TORCH-2 software is essential to the ease-of-use design of the T3 IC.

BOUNDARY SCAN CONTROLLER

The Corelis PCMCIA 1149.1a boundary scan controller is the hardware used to convert software commands into boundary scan data chains to control and retrieve data from the T3 IC. This controller is in the PCMCIA (or PC Card) format for use in a laptop PC or a desktop PC with a PCMCIA drive installed. The Corelis PCMCIA 1149.1a requires the Corelis scan function dynamic link library to function.

DIGITAL /ANALOG PORT

Analog connection to the T3 IC is provided by the National Instruments NI 16Bit A/D, D/A ISA interface card (multifunction D/A, A/D, 24 bit digital port). This card requires the WinDAQ95 control software to operate. The NI 16Bit A/D, D/A provides direct connectivity to the T3 Analog Port for 4-wire force /stimulus capability on the F1, S1, F2, S2 lines. Analog signals are created or measured by the LabVIEW™ control software using this hardware. The DAQCard 1200 works in conjunction with a custom interface card that allows automatic switching between force or sense operations on the analog port. Portions of the 24 bit digital port on the NI 16Bit A/D, D/A are used for the automatic configuration.

POWER

+5V at 1A power to the T3 IC is provided by the National Instruments NI 16Bit A/D, D/A ISA interface card (multifunction D/A, A/D, 24 bit digital port). A custom interface card connects the NI 16Bit A/D, D/A to the T3 IC and scales the +5Vdc input power into +/- 3.3Vdc or other voltages. Portions of the 24 bit digital port on the NI 16Bit A/D, D/A is used for power switching and control. In addition, the custom interface card has the capability to measure the input current, Idd, into the T3 IC.

VOLTAGE STRESS

Stress Voltages for the GOX Vramp test are supplied by external power sources and routed to the T3 IC through the interface card. The GOX stress voltage may range up to 40 Vdc, but is limited by the T3 IC to 27 Vdc. HCI stress can not go above 8 Vdc on the drains of the NMOS FETs. HCI stress can not go below 0 Vdc on the drains of the PMOS FETs

POWER REQUIREMENTS

With the exception of the GOX stress voltages, the power consumption of the T3 IC cannot exceed the supply capability of the NI 16-bit A/D board which is 5Vdc at 1A (5 watts). Power requirements exceeding this specification are provided externally, such as the stress voltage sources.

SOFTWARE COMPATIBILITY

The T3 IC was designed with the control software in mind. Goals of the operation of the system are ease-of-use and automation. Where possible, the design incorporated features that make test setups, test execution, and data collection simple. Universal flexibility of the T3 IC is not necessary in this design, and adds to increased complexity and less functionality in the control software, i.e., the more flexible the T3 IC design is, the more complex the TORCH-3 software design becomes. The T3 IC design was tailored to only perform the setups and tests necessary to perform reliability testing on the Hot Carrier, and Gate Oxide DUT's.

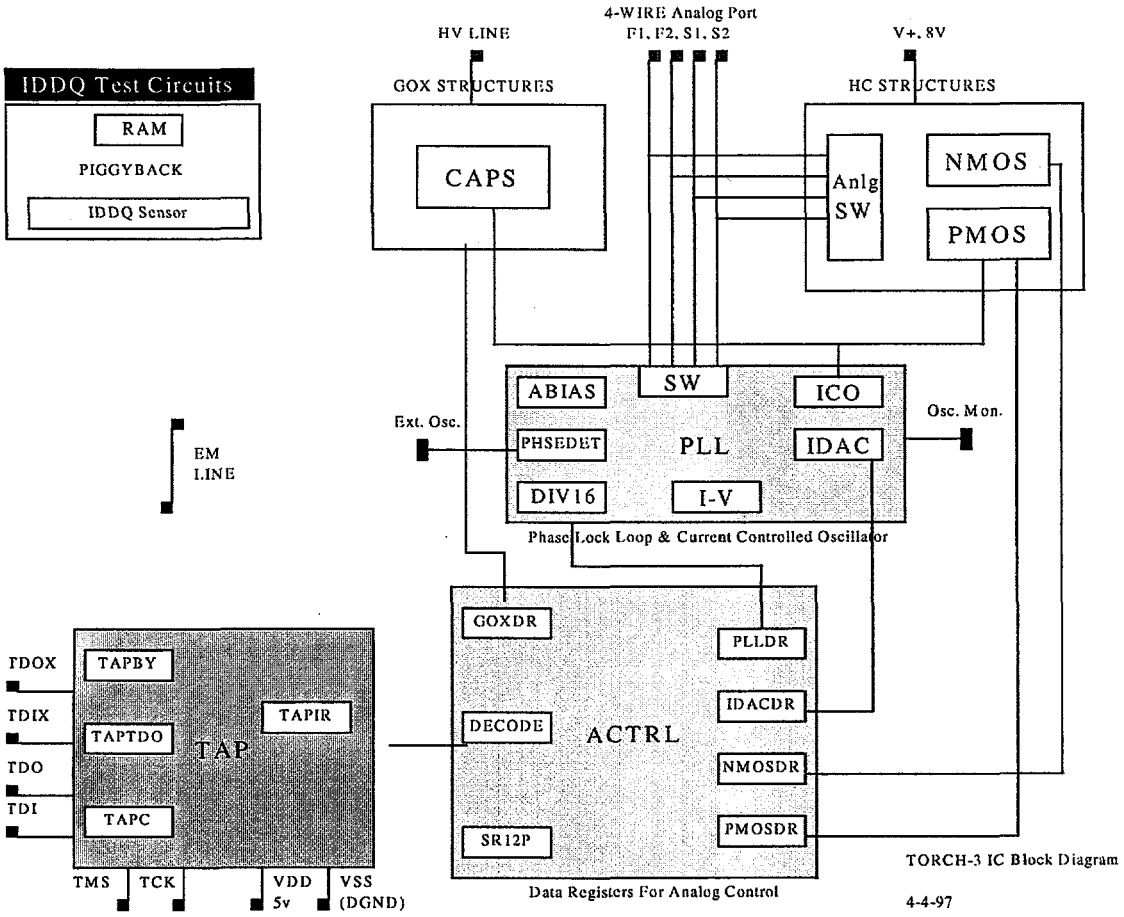
IC Design Description

TORCH -- 3 IC DESIGN

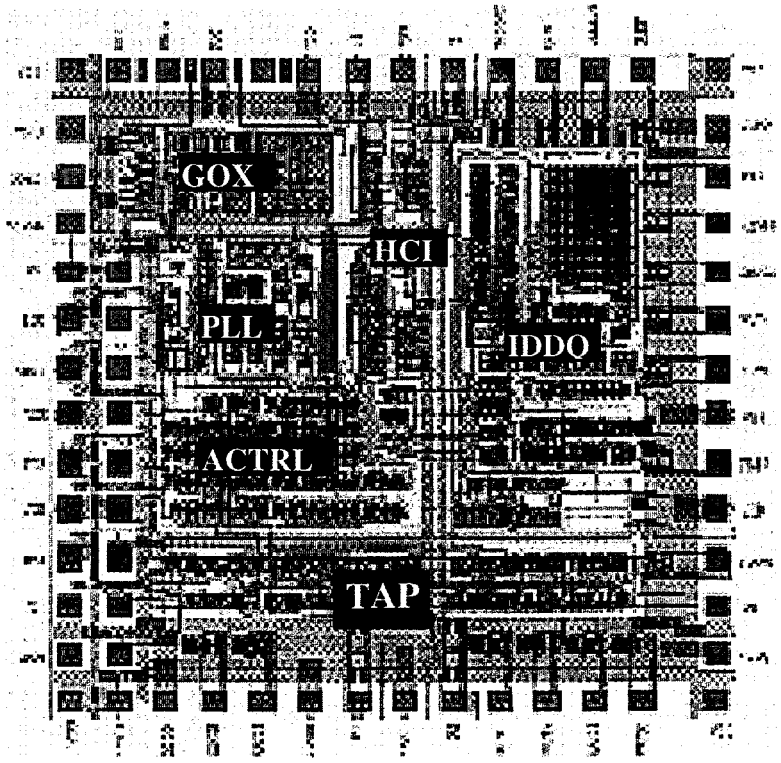
The TORCH-3 Design involves 6 functional building blocks: TAP, Analog Port, PLL, GOX DUT's, HCI DUT's, and the Current Controlled Oscillator (ICO). The TAP is the re-used TORCH-2 IEEE Std. 1149.1 boundary scan Test Access Port. The Analog Port connects the NI 16Bit A/D, D/A and the Keithley 2400 Source /Meters to the DUT's. The GOX DUT's are ganged gate oxide structures with built in stress control and measurement switching. The HCI DUT's are ganged on-die hot carrier structures with built in stress control and measurement switching. The ICO is a dual current controlled oscillator.

TORCH-3 operates from +5 volts for digital circuits and +8Vdc for analog circuits. The GOX and HCI DUT arrays have independent external stress voltage sources.

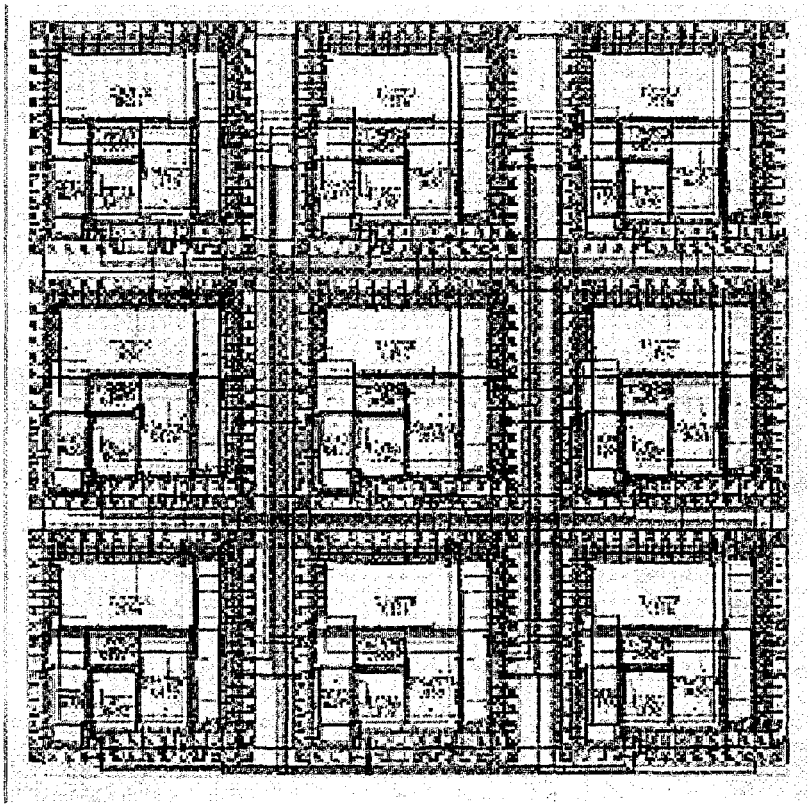
TORCH - 3 IC System Diagram



TORCH 3: Single Die



TORCH 3; 3 X 3 ARRAY OF TORCH 3 DIE



Design of TORCH 3 Die Array - Circuit Aspects

TORCH 3 Design - 3 x 3 Array of TORCH 3 Die

The Torch3 die array consists of a 3x3 array of interconnected sub-dice. For die to die communication, the sub-dice have serial communication data lines employing the Boundary Scan standard (IEEE Std 1149). The sub-dice are connected in a daisy-chain fashion with two data lines connecting neighboring sub-dice (one data line connects the TDOX signal of one sub-die to the TDI signal of a neighboring sub-die, the other connects the TDIX signal of the former sub-die to the TDO signal of the latter sub-die). A particular sub-die can serve as a host for any downstream (in the daisy-chain) sub-die. Routed in parallel to all 9 sub-dice are the non-communication interconnects. These include: 4-wire analog port lines (F1, F2, S1, S2), VDD, VSS, V+, HV, and the Boundary Scan control signals (TCK, TMS).
Each sub-die in the 3x3 array has the following test structures: Gate Oxide - DC test, Gate Oxide - High Frequency test, NMOS Hot Carrier (used for both DC and High Frequency testing), PMOS Hot Carrier (used for both DC and AC testing), and an Electromigration strip.

Gate Oxide - DC test
The DC Gate Oxide structure consists of 4 poly to n-well capacitors with the following areas: $320uM^2$, $100uM^2$, $32uM^2$, and $10uM^2$. Any combination of these capacitors can be selected for simultaneous stressing for gate oxide evaluations. While a high voltage, HV, (up to 27 volts) is applied to the poly side of all the capacitors, individual high-voltage level shifters connect the n-well side of their respective capacitor to either ground or the HV line depending on whether the level shifter input is high or low respectively. The level shifter inputs are set via the boundary scan interface. The high voltage level shifter is described below.

Gate Oxide - High Frequency Structures
The High Frequency Gate Oxide structure consists of 2 poly to n-well capacitors with the following areas: $32uM^2$, and $10uM^2$. Any combination of these capacitors can be selected for simultaneous stressing for gate oxide evaluations. While a high voltage, HV, (up to 27 volts) is applied to the poly side of both the capacitors, individual high-voltage level shifters connect the n-well side of their respective capacitor to either an alternating HV line - ground combination (at the oscillator frequency) or just the HV line depending on whether the level shifter input is high or low respectively. The level shifter inputs are set via the boundary scan interface. The high voltage level shifter is described below.

NMOS, PMOS - Hot Carrier Structures

These structures each consist of 5 MOS devices. Since the PMOS and NMOS structures share access to the 4-wire analog port, simultaneous stressing of NMOS and PMOS devices together is not possible, however, within each structure, any combination of the devices can be simultaneously stressed. The 4-wire analog port provides access to all the NMOS gates (via F2) and drains (via F1) while the NMOS sources are all hardwired to ground. Configurable via the boundary scan interface is a 12-bit data register. Different bit settings will determine which

NMOS devices are connected to the 4-wire analog port. Measurement of the NMOS drain and source voltages is accomplished via the analog port S1 and S2 sense lines. The PMOS array has all device sources hardwired to V+ (8 volts for Torch3) while the drain and gate voltages are set

via the F1 and F2 analog port lines. Similar to the NMOS structure, measurement of the PMOS drain and source voltages is accomplished via the analog port S1 and S2 sense lines.

The 4-wire analog port lines are connected to the NMOS and PMOS devices using pass-gates (controlled by the bits set in the respective 12-bit data registers) The forcing pass gates were designed to have an impedance of approximately 250 ohms while the sensing pass-gates have an impedance around 2000 ohms.

Electromigration Test Structure

Each sub-die in the 3x3 array has a stand alone Electromigration Test structure.
There are 4 I/O pads (EM_F1, EM_F2, EM_S1, and EM_S2) and no interfaces with the boundary scan control. The structure is a 800uM long, 2.2uM wide, strip of Metal1 (Orbit 1.2uM process).

High-Voltage Level Shifter (HVLS)

The HVLS blocks are designed to switch voltages as high as 27 volts based on a control signal of 5 volts (digital voltage level for Torch3 design). These blocks are essential for proper operation of both the DC and High Frequency gate oxide structures and guarantee that the n-well side of test structure capacitors are either pulled-up to the high voltage (no stress across the capacitor) or pulled to ground (capacitor is stressed). One concern with the HVLS blocks is the voltage withstand rating. It is assumed that by placing two high voltage PMOS devices in series the high voltage will divide evenly across each device (then each PMOS device only has to block 27/2 or 13.5 volts). Any differences between the PMOS devices could cause uneven voltage division with one device bearing a larger stress. The fact that only one high voltage NMOS device is used to block up to 27 volts should not be an issue since similar devices have blocked much larger voltage levels. ORBIT claims that the N-well to p-substrate breakdown voltage is 45 volts and the "junction breakdown" voltage is 15 volts.

DESIGN OF TORCH3 DIE ARRAY - LAYOUT ASPECTS

Layout of the Torch3 die demanded various considerations and tradeoffs.
Both at the 3x3 array and sub-die level, a top priority was to ensure proper operation of the 4-wire analog port. To limit noise pickup, the sense lines were routed together between the force lines and away from any clock signals. The force lines were made as wide as practical to limit their resistance. A worst case loading condition by the NMOS hot carrier array was used to determine force line widths.
The phase-locked loop (PLL) block was centrally placed to minimize the oscillator line run lengths to the hot carrier and gate oxide structures. In addition, the oscillator line was routed between the VSS and VDD lines to provide shielding.
Also, great care was taken in routing the high voltage (HV) line since it would have voltages as high as 27 volts.
In order to limit damages caused by gate oxide breakdown the gate oxide capacitors were surrounded with P+ guard rings to collect breakdown currents.

SIGNAL INTERFACE

The TORCH-3 design maintains the EQRC standard 20-pin Test Interface Port (TIP). For

TORCH-3 this port is renamed the Test Interface Port (TIP) to eliminate confusion with the IEEE 1149.1 boundary scan TAP definition. This interface includes 3 power inputs, digital ground, analog ground, TAP (4-wire Boundary Scan), 4-wire Analog Port. High voltage input for GOX stressing is supplied via pad.

TEST INTERFACE PORT (TIP)

The Test Interface Port (TIP) provides the main interface to the TORCH-3 IC. This port incorporates the digital boundary scan (TAP) interface defined by IEEE Std. 1149.1 as well as a 4-wire analog port extension. The analog port extension does not interfere with the IEEE 1149.1 specification.

Function	Pin#	Pin#	Function
HV	1	2	HV SENSE
TDOX	3	4	S 2
TDIX	5	6	S 1
VSS	7	8	n/c
TCK	9	10	F 1
VDD	11	12	n/c
TMS	13	14	F 2
V+	15	16	n/c
TDO	17	18	n/c
VSS	19	20	TDI

TEST ACCESS PORT (TAP)

1. TDO (Test Data Out) Boundary scan serial test data output.
2. TDI (Test Data In) Boundary scan serial test data input.
3. TMS (Test Mode Select) Boundary scan test state control signal for internal test access port controller.
4. TCK (Test Clock) Clock for Test Circuits. Input signals, TDI and TMS, change on the falling edge of TCK and are captured on the rising edge of TCK and output TDO changes on the falling edge. The maximum TCLK frequency acceptable by TORCH-3 is 1 MHz. The Corelis 1149.1 can deliver a TCK up to 25 MHz.

Analog Port

The Analog Port is a 4-wire interface. Signals are independently configured as force or sense.

F 1 (Analog Port 1 Force 1)
F 2 (Analog Port 2 Force 2)
S 3 (Analog Port 3 Sense 1)
S 4 (Analog Port 4 Sense 2)

TDOX/ TDIX (Extra Test Data Output/ Input)

TDOX and TDIX signals represent extra digital data interface for extending the BS interface for basic die-to-die communications.

VDD (Positive Digital Power)

This power input is +5Vdc with less than 100mv noise.

VSS (Digital Ground)

V+ (Positive Analog Power)

This input should be set to 8VDc.

High Voltage Input (HV), HV SENSE

HV provides the high voltage input to the gate oxide capacitor DUT's, VCAP 1 through VCAP 5. The range for VCAP (x) is 0 - 27 Vdc at 10 ma. The sense pad provides input to the sense input of the Keithley 2400 to eliminate supply line voltage drops.

TAP CONTROLLER (TAPC)

The TAPC represents an internal state machine for control of the test circuits. The TAPC handles the passing of data in and out of the test interface. It includes state generation logic, an instruction register, and multiple (distributed) data registers. Design of the TAPC complies with IEEE 1 149.1 standard. Bit I indicates LSB or the first bit received at TDI.

TAP Controller Decoding

The TAPC provides signals needed to decode unique addresses for each data register as defined for each data resister. All unused addresses default to the address of the bypass register and are decoded internal to the TAP. In addition, the TAPC decodes each of the following signals for use:

- The controller provides a data clock, CLKDR, for parallel loading during the CAPTURE DR state and shifting during the SHIFT DR state for capture and output of internal data.
- The TAPC provides a strobe indicating the CAPTURE DR state for parallel loading latched registers into data shift registers.
- The TAPC provides a strobe indicating the UPDATE DR state for parallel loading data shift registers into latched resisters.
- The TAPC decodes the controller reset state for use as a Master Reset, MRST, which overrides and initializes all functions.

TAP Instruction Register (IR)

The TAPC includes a single 4-bit instruction register for self control. The IR determines how incoming data sent to the TAP on TDI is processed as well as where data leaving the TAP on TDO comes from. Per the 1149.1 specification, the instruction register is cleared by the standard TMS reset sequence and loaded with the value [1001] during Capture-IR. The TMS signal controls TAP state sequencing, which provides for loading the instruction register from the TDI signal. The specific instructions loaded into the instruction register as a result of these sequences execute particular operations as defined by the designated TAP instructions.

TAP Instructions

Instruction	Binary	Address
EXTEST	0000	0
SAMPLE/ PRELOAD	0001	1
INTEST	0010	2
spare	0011	3
IDACDR	0100	4
NMOSDR	0101	5
PMOSDR	0110	6
PLLDR	0111	7
GOXDR	1000	8
spare	1001	9
spare	1010	10
spare	1011	11
SR12P VALUE	1100	12
LOOP	1101	13
CMDRST	1110	14
BYPASS	1111	15

TAP Data Registers

Details are provided in subsequent sections. IEEE Std. 1149.1 required TAP instructions include: EXTEST, SAMPLE/PRELOAD, INTEST, CMDRST, and BYPASS. Application specific TAP Data registers include Stress Clock (IDACDR), HCI N and P channel stress/measure (N,PMOSDR), Phase Lock Loop configure (PLLDR), GOX Stress /Measure (GOXDR), get value of SR12P by parallel load.

Extest [0000], sample/preload [0001], intest [0010].

Required public boundary scan instruction to support control of peripheral scan pad cells.

IDAC Data Register (Stress Clock)

Current source (IDAC)

The programmable IDAC provides a current source for the current controlled oscillator (ICO). Control of the IDAC (and thus the ICO) is provided by a BS data register. FOR simplicity, the IDAC may be configured for a fixed combination of current outputs (such as 8, 16 or 32 combinations).

IDAC Data Register [0011]

Linear/ Non-linear	Sink/ Source	IDAC range bit 6	IDAC range bit 5	IDAC range bit 4	IDAC range bit 3	IDAC range bit 2	IDAC range bit 1
B07- msb	**B06**	**B05**	**B04**	**B03**	**B02**	**B01**	**B00- lsb**

IDAC Register Decode

Bits 0 - 5 = IDAC Current magnitude setting

Bit 6 => 0 = Source, 1 = Sink

Bit 7 => 0 = Linear, 1 = Nonlinear

HOT CARRIER (HCI) STRUCTURES

HCI Stress/Measure

A 5 x 1 array of Hot Carrier degradation structures is configured for simultaneous stressing and individual measurement. P and N type hot carrier devices are tested. They are comprised of N and P channel MOSFET devices connected individually to the stress source via analog switches. Connection is made through the HCI Data Registers [1001].

HCI Data Registers for Hot Carrier Testing

Bit Selection is as follows; B11 = 1 selects the ICO as the gate source. B10 = 1 selects F2 as the source for DC gate bias, Bits 0 - 9 select the force and sense connections to the drains of each of the HCI FET's.

NMOSDR [0101]

AC Gate Bias	DC Gate Bias	NMOS 4,D F1	NMOS 4,D,G S1,S2	NMOS 3,D F1	NMOS 3,D,G S1,S2	NMOS 2,D F1	NMOS 2,D,G S1,S2	NMOS 1,D F1	NMOS 1,D,G S1,S2	NMOS 0,D F1	NMOS 0,D,G S1,S2
B11	**B10**	**B09**	**B08**	**B07**	**B06**	**B05**	**B04**	**B03**	**B02**	**B01**	**B00**

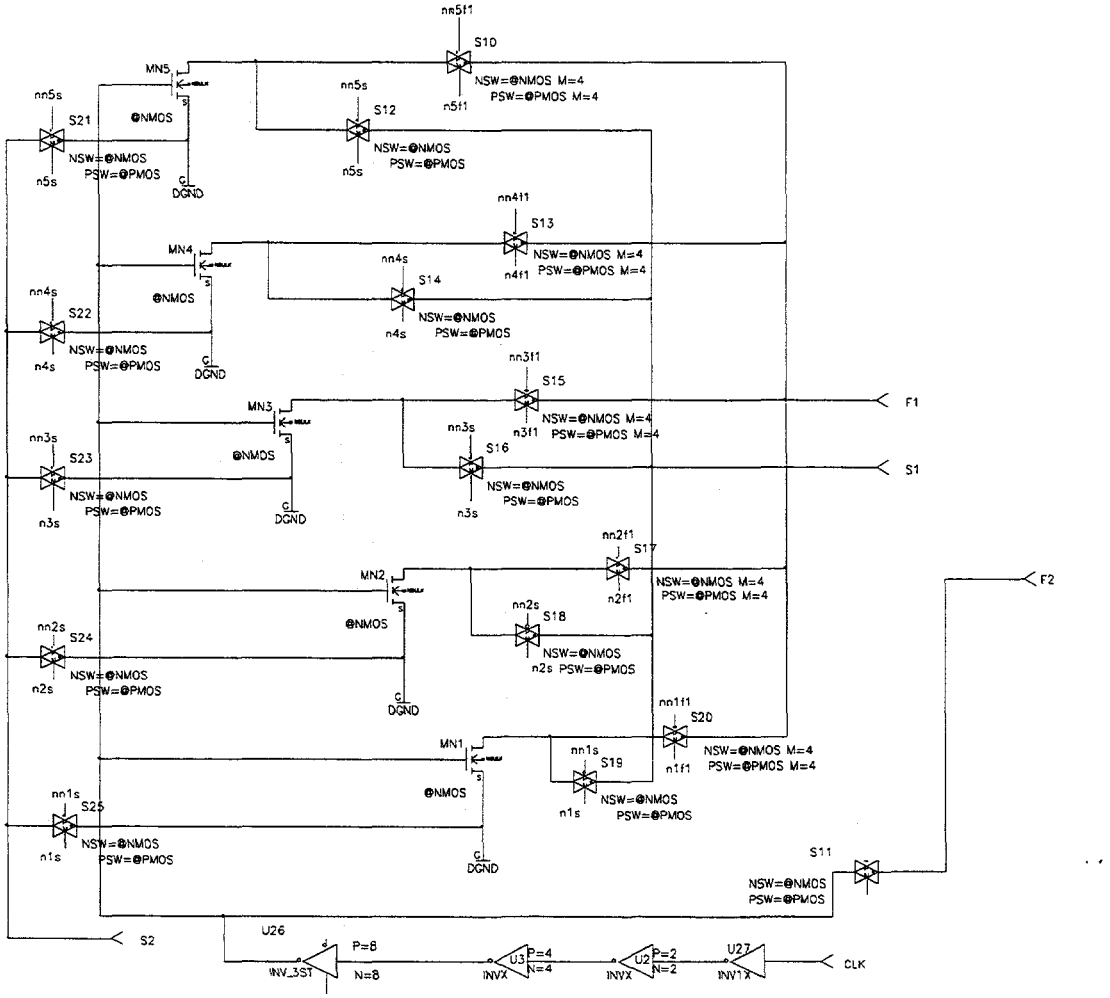
PMOSDR [0110]

AC Gate Bias	DC Gate Bias	PMOS 4,D F1	PMOS 4,D,G S1,S2	PMOS 3,D F1	PMOS 3,D,G S1,S2	PMOS 2,D F1	PMOS 2,D,G S1,S2	PMOS 1,D F1	PMOS 1,D,G S1,S2	PMOS 0,D F1	PMOS 0,D,G S1,S2
B11	**B10**	**B09**	**B08**	**B07**	**B06**	**B05**	**B04**	**B03**	**B02**	**B01**	**B00**

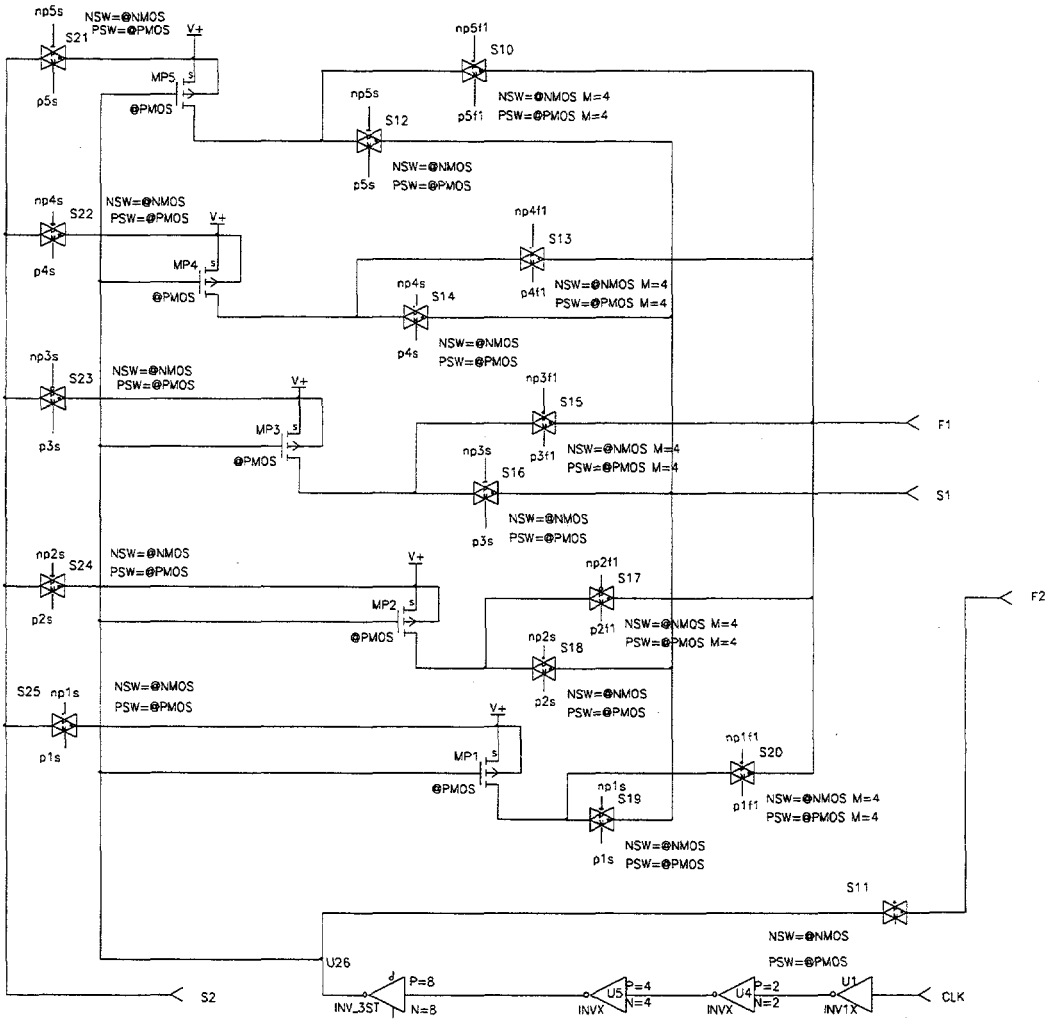
HCI Configuration Diagrams

The Hot Carrier DUT's are configured in the TORCH-3 design according to the schematics below:

Hot Carrier NMOS DUT's



Hot Carrier PMOS DUT's



HCI Structure Controller

The HCI Structure Controller controls the stimulus to the HCI DUT's by decoding the HCI NMOS and PMOS data registers.

HCI Measurement Matrix

The HCI measurement matrix determines which HCI DUT's are to be measured by decoding the HCI NMOS and PMOS data registers.

Phase Lock Loop (PLL)

Phase Lock Loop (PLL) Data Register [0111]

LOW VOLT BIAS EN	FREQ SEL MUX msb	FREQ SEL MUX lsb	IDAC EN	FILTER BUFFER EN	JOHNSON COUNTER EN	EXT EN	INT EN
B07	**B06**	**B05**	**B04**	**B03**	**B02**	**B01**	**B00**

PLL DATA REGISTER DECODING

Bit Number	Selection
0 - Internal Enable	0=dis., 1 = ICO reference currents come from on-chip
1 - External Enable	0=dis., 1 = ICO reference currents come via F1 & F2
2 - Johnson Counter Enable	0=dis., 1 = Enable
3 - Filter Buffer Enable	0=dis., 1 = Enable
4 - IDAC Enable	0=dis,. 1 = Enable
5 - Frequency Select Mux - lsb	00 = External Frequency, 01 = FREF
6 - Frequency Select Mux - msb	10 = OSC divided by 16, 11 = OSC
7 - Low Voltage Bias Enable	0=dis., 1 = Enable

10 Hz to 700 Mhz Current Controller Oscillator (ICO)

This design is re-used from the Orbit HF reliability test structures.

Dual Current sources for ICO

Current for the ICO can either be provided by the on-chip digitally controlled current source (IDAC) or by an off-chip current source via the analog port F1 and F2 lines.

GOX STRESS /MEASURE

Gate Oxide Integrity DUT Array

Two arrays of Gate Oxide Integrity structures are configured for simultaneous stressing and individual measurement. By allowing each DUT to be individually disabled, dynamic de-activation of failed DUT's is possible. An AC array or a DC array is configured for simultaneous testing. The AC array is comprised of a 31.6uM^2 GOX capacitor and a 10.0 uM^2 GOX capacitor. The DC array is comprised of a 316.0 uM^2 GOX cap, a 100 uM^2 GOX cap, a 31.6 uM^2 GOX cap, and a 10.0 uM^2 GOX cap.

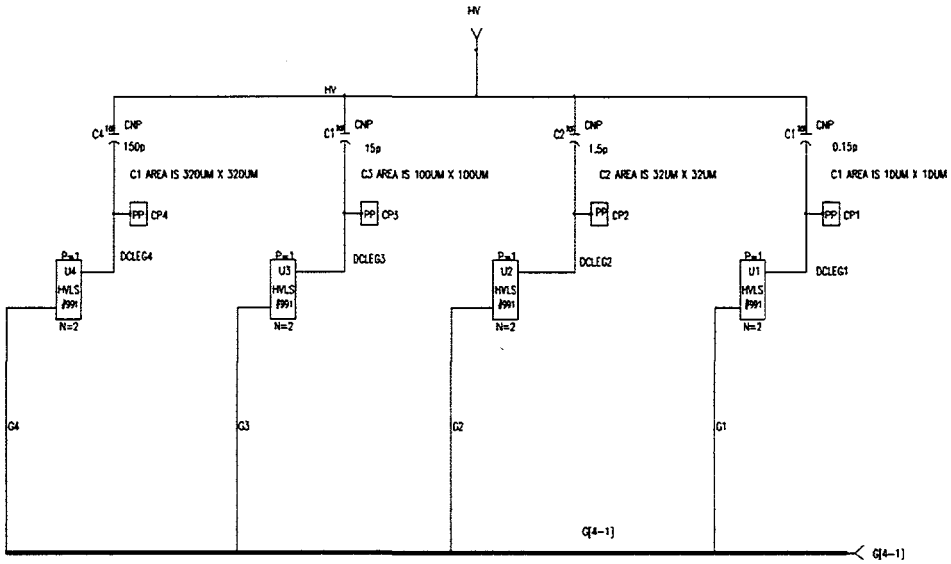
GOX Data Register [1000]

Spare	EN AC GOX 2	EN AC GOX 1	EN AC CLK	EN DC GOX 3	EN DC GOX 2	EN DC GOX 1	EN DC GOX 0
B07	**B06**	**B05**	**B04**	**B03**	**B02**	**B01**	**B00**

GOX Configuration Diagrams

The Gate Oxide DUT's are configured in the TORCH-3 design according to the schematics below:.

DC Gate Oxide DUT's



AC GATE OXIDE DUT's

GOX STRUCTURE CONTROLLER

The GOX Structure Controller controls the stimulus to the GOX DUT's by decoding the GOX data register, address 8 [1000].

SR12P VALUE [1100].

This command allows the next Capture Data Register (CDR) state to load internal die data into the 12-bit data register via its parallel port. This data can then be shifted out via the TDO port.

The data loaded includes: Bits 8-1 are the contents of the IDAC latch (configuration of the onboard current source), Bit 9 is the IDAC enable bit status, Bit 10 is the external current source enable (for the current controlled oscillator - ICO) bit status, Bit 11 is the internal current source enable (for the current controlled oscillator - ICO)bit status, and Bit 12 is the LOOP status bit.

LOOP [1101].
This command configures a particular die within the 3x3 array to become a data link between the host and target dice..

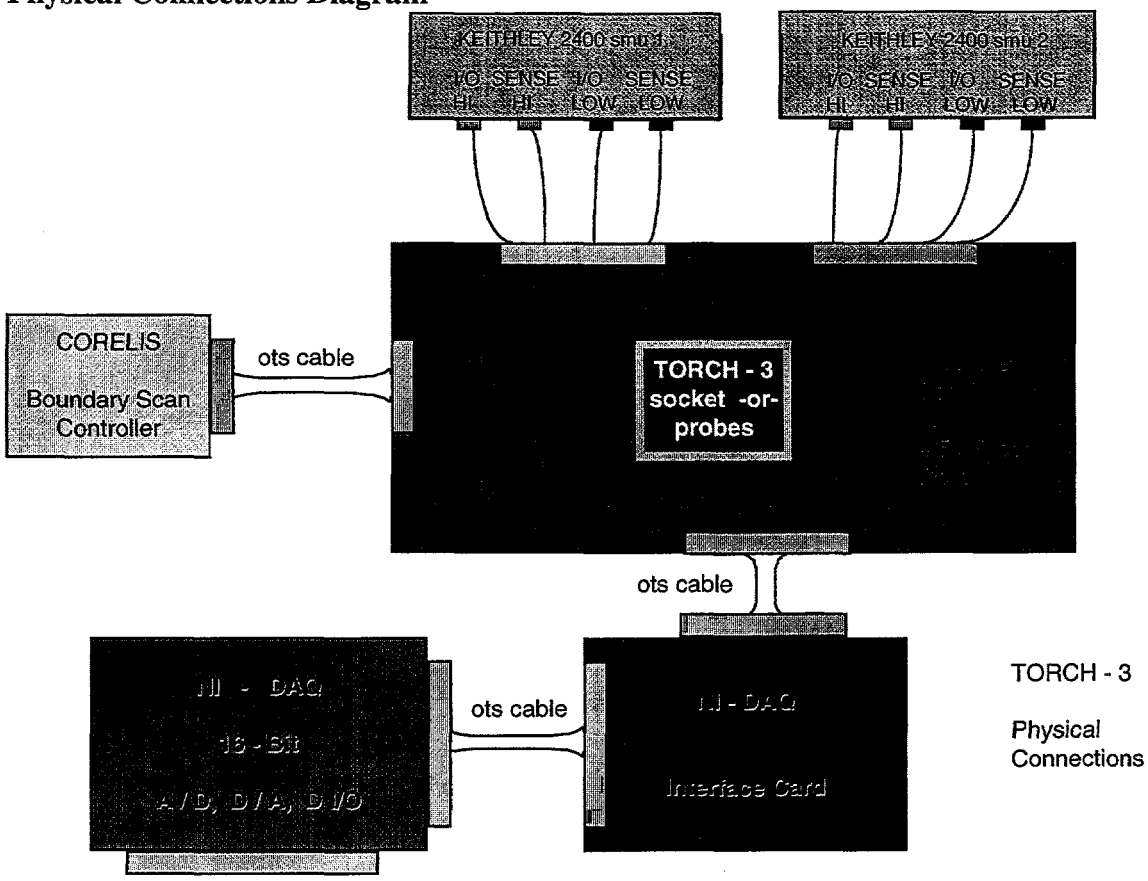
CMDRST [1110].
The CMDRST instruction implements a commanded reset operation for use by testing functions.

BYPASS [1111].
Required public boundary scan instruction. Bypass allows data streams to pass through any boundary scan compliant part with 1 and only 1 clock delay. The TAPC includes a 1-bit data register for bypass according to the boundary scan specification. The Bypass register represents an integral function of the TAP controller block. The Bypass register is cleared during the capture state. A TAP reset sequence causes the Bypass Register to be selected as the default data register. The bypass resister is located internal to the TAPC as a required function.

Interface Hardware and Control Software Design

Interface Hardware Description

Physical Connections Diagram

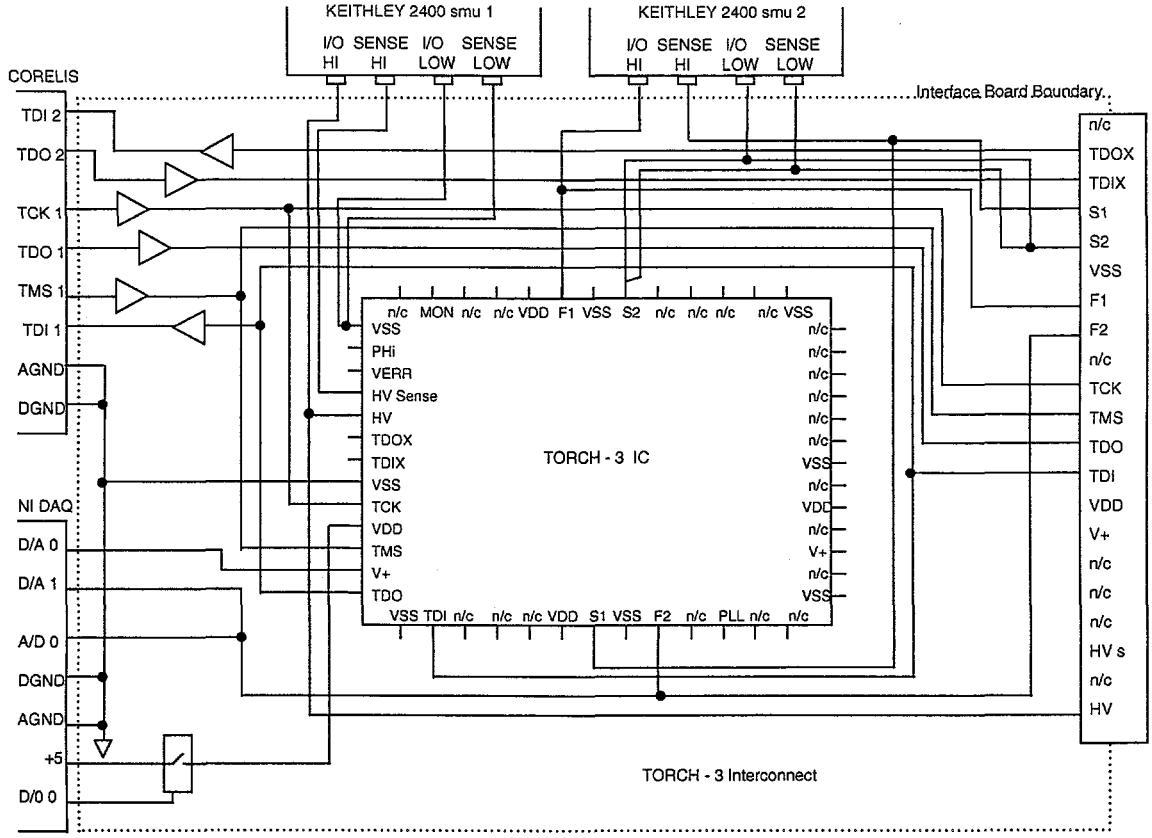


T3 Interface Board

The TORCH-3 interface board provides these main functions:

1. Provides a mechanical connection between the Corelis boundary scan controller and the NI 16Bit A/D, D/A ISA cards and the T3 IC, whether at package level or at wafer level.
2. Signal buffering and level shifting of the 4-wire boundary scan bus. (TTL to CMOS)
3. Power and power control to the T3 IC.
4. Automatic connection and switching of the 4-wire Analog Port from Force to Sense to External.
5. Capability to measure the current consumption of the T3 IC in real time.
6. Connection to external voltage or current sources.
7. Voltage conversion as required
8. Ancillary Test Points as required.

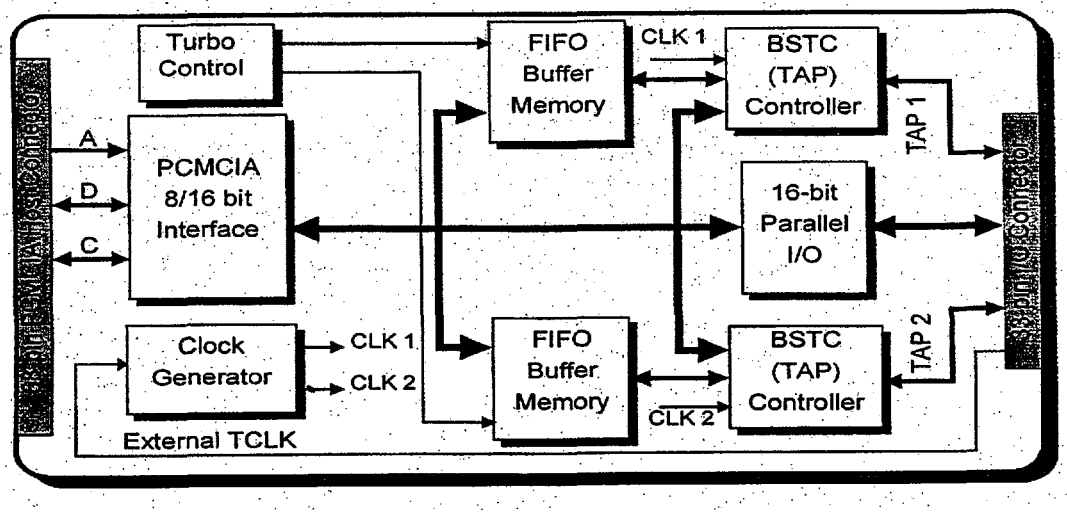
T3 System Wiring Diagram



Corelis Boundary Scan Controller

The Corelis PCMCIA 1149.1a boundary scan controller is a second generation PCMICA format IEEE-1149.1 compatible dual boundary scan controller. Two TAP controllers are included in the package. The controller provides TTL compatible TCK, TDO, TMS, and TDI boundary scan signals.

Corelis 1149.1 Block Diagram



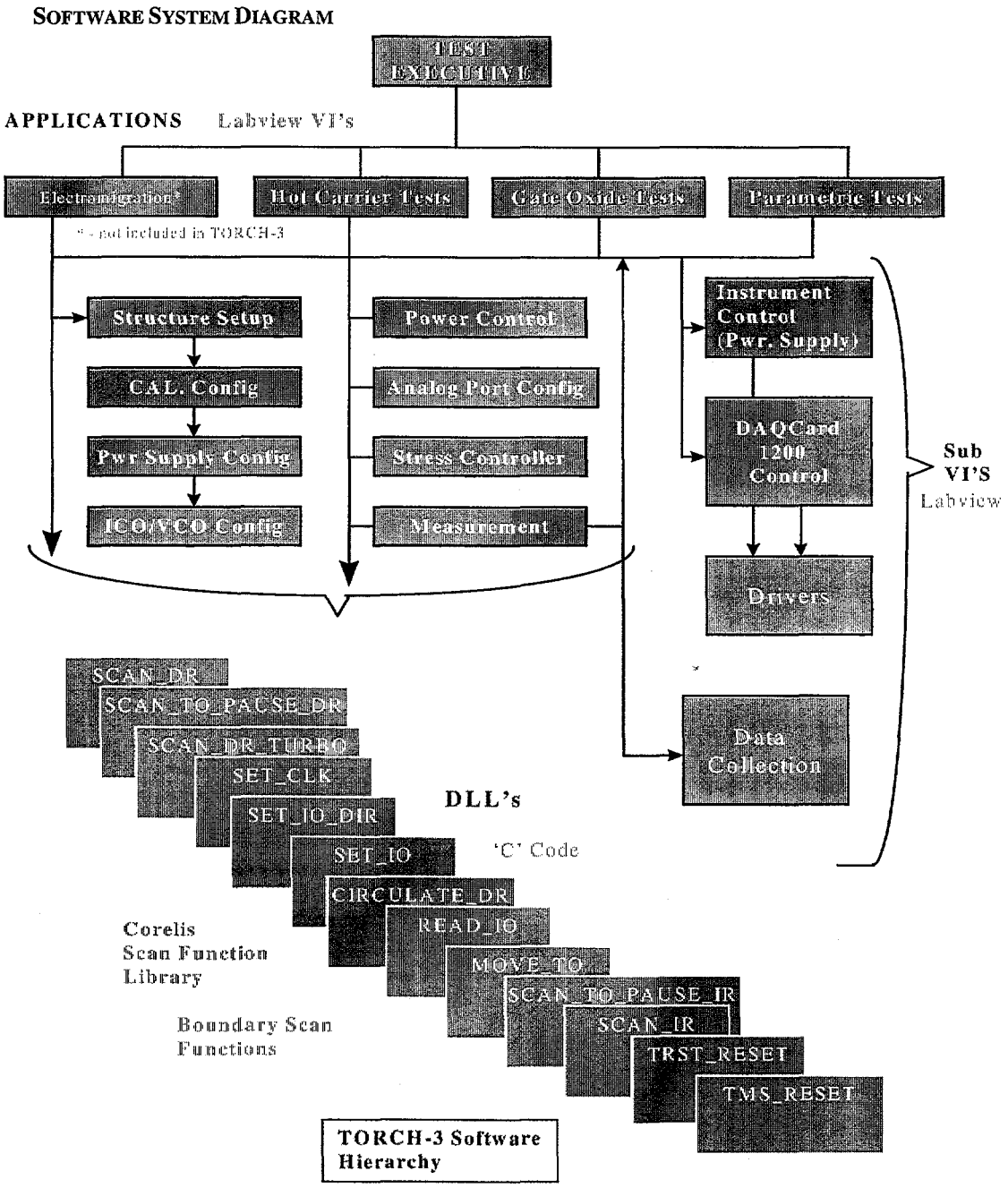
Corelis 1149.1 Signal Connections

J2 Pin	Signal Name	I/O (relative to card)	Description	I/O Interface Cable Connector
1	GND		Signal Ground	20,21
2	TCK1	out	Test Clock Channel 1	5
3	GND		Signal Ground	22,23
4	TMS1	out	Test Mode Select Channel 1	4
5	GND		Signal Ground	24,25
6	TDI1	in	Test Data In Channel 1	3
7	TDO1	out	Test Data Out Channel 1	2
8	TRST*	out	Test Reset Output	1
9	GND		Signal Ground	26,27
10	TCK2	out	Test Clock Channel 2	10
11	GND		Signal Ground	28
12	TMS2	out	Test Mode Select Channel 2	9
13	GND		Signal Ground	29
14	TDI2	in	Test Data In Channel 2	8
15	TDO2	out	Test Data Out Channel 2	7
16	FRZ	In	Test Clock Freeze Channels 1 & 2	6
17	PIO_0	bi	Parallel I/O bit 0	30
18	PIO_1	bi	Parallel I/O bit 1	12
19	PIO_2	bi	Parallel I/O bit 2	31
20	PIO_3	bi	Parallel I/O bit 3	13
21	PIO_4	bi	Parallel I/O bit 4	32
22	PIO_5	bi	Parallel I/O bit 5	14
23	PIO_6	bi	Parallel I/O bit 6	33
24	PIO_7	bi	Parallel I/O bit 7	15
25	GND		Signal Ground	11
26	PIO_8	bi	Parallel I/O bit 8/Ext TCK Input	34
27	PIO_9	bi	Parallel I/O bit 9	16
28	PIO_10	bi	Parallel I/O bit 10	35
29	PIO_11	bi	Parallel I/O bit 11	17
30	PIO_12	bi	Parallel I/O bit 12	36
31	PIO_13	bi	Parallel I/O bit 13	18
32	PIO_14	bi	Parallel I/O bit 14	37
33	PIO_15	bi	Parallel I/O bit 15	19

National Instruments NI 16Bit A/D, D/A

The National Instruments NI DAQ MIO 16: 16Bit A/D, D/A provides +5Vdc power, Quad 16-bit A/D conversion, Dual 16-bit D/A conversion, 24 bits of TTL compatible digital I/O, and three counter/timers. Refer to the manual for the NI DAQ MIO 16 for technical details.

Control Software Description



FUNCTIONAL DESCRIPTION

The control software is LabVIEW™ based and consists of user panels, VI's, Sub-VI's and Windows DLL's. User panels are graphical and operate from mouse selections. VI's and Sub-VI's are similar to main programs and sub routines except they are strictly object oriented and can function stand alone. The control software converts user inputs to boundary scan data chains for interpretation by the T3 IC. The user interface is graphical (GUI) and selections are made from a front panel for the desired test function. At the top level GUI, selections are available for power, and the desired test to run, i.e., Hot Carrier, Gate Oxide, or parametric tests. For convenience, parametric tests are included as a top level selection although they are a sub-vi because they are part of Hot-Carrier testing. Upon selecting a top level test, a second GUI pops up to select test parameters, desired output, etc. This test setup GUI is driven largely from the test procedure and the test structure design. Upon making selections, the user initiates the test with a "GO" button and a third GUI pops up to display test status and graphical data output. Miscellaneous selections are made from this screen to abort test, modify test, etc. Closing a GUI reverts the user back to a prior GUI. It is also possible to have simultaneous GUI windows open.

HIERARCHY

The control software is hierarchical which allows for ease of design, implementation and use. From a top-down perspective the software starts at a main level called Test Executive. Opening and running the test executive requires that all sub level VI's and DLL's be linked prior to execution. The test executive calls sub-VI's that control the test setup for reliability tests. These sub-VI's in turn call other sub-VI's to control setups for individual DUT groups, TMU setups, Analog Probe setups, Etc. These sub-VI's make calls to the Corelis DLL to transmit boundary scan instructions to the T3 IC for test setups. Upon finishing test setups, calls are made to equal level sub-VI's for test execution and monitoring. These sub-VI's also communicate with T3 via the Corelis DLL. Additionally, this level of sub-VI also makes necessary calls to the WINDAQ95 software for controlling the NI 16Bit A/D, D/A multifunction I/O card, and calls to IEEE-488 instrumentation if necessary. At the lowest level of the hierarchy is the Corelis DLL (Scan Function Library) and the driver for the NI 16Bit A/D, D/A.

RELATIONSHIP TO T3 REGISTERS

The Sub-VI's of the control software are configured to directly load and configure the setup registers of the T3 IC. A graphical representation of the setup register is displayed on the control panel. LabVIEW™ allows re-configurable registers through attributes selection, i.e., the graphical representation of the control register can change dynamically based on the "tag" bit(s) selected for that particular register. Thus the significance of carefully designing the T3 boundary scan registers becomes clear.

DATA COLLECTION

LabVIEW™ has powerful data collection, reduction, storage, manipulation, and display features. In addition, capabilities are provided for dynamic data exchange with other software packages. The TORCH-3 control software also has the capability to control and collect data from an HP-5400 series oscilloscope. The oscilloscope can be connected to the analog port and ancillary measurements can be performed via the control software through the oscilloscope.

DATA REDUCTION

Data reduction can occur directly in LabVIEW™, and is supported by Excel. Report generation is provided by National Instruments HiQ report generation software. These packages can run

concurrent with LabVIEW™ in Windows 95, and data can be transferred dynamically. An attempt to dynamically reduce the data during collection was made due to the large amount of engineering time required to manually perform this task.

CABLING

The Corelis PCMICA card connects to the T3 interface board via a supplied cable. The NI DAQ 16 Bit card connects to an interface card that is provided with the unit, and then connects to the T3 interface board via user supplied cables, that are easily made. A probe card was created to allow probing an unpackaged die. In addition, provision was made to allow a 20-wire interface to a probe card for wafer level testing of the T3 IC. External connections for voltage, current, or measurement are made through the T3 interface board.

PACKAGED PART FIXTURE

The packaged part fixture is not incorporated into the design of the T3 interface board.

WAFER LEVEL TEST PROBE CARD

An optional 4.5" wafer level test probe card provides interconnect to the 52 pin (13x13) TORCH-3 interface. In addition, an additional probe card incorporates the EQRC standard 2 x 10 pin interface, and has decoupling and buffering necessary to retain signal integrity. A 20-pin connector was provided to connect to the EQRC standard 20 pin probe cards if necessary. Connectors are provided for connection to the Corelis 1149.1 boundary scan controller and the NI DAQ MIO 16 multifunction board.

Test Plan and Procedure

Test Philosophy

Proof of Concept

The intent of this LDRD was to prove that reliability tests can be performed using an imbedded mixed-signal test system supported by a minimum of external support hardware and software. With this in mind, the goal of this LDRD was to demonstrate that equivalent reliability tests can be accomplished, but industry standard benchmarking is not a goal.

DUT Sample Size

On chip sample size was optimized for proof of concept. Enough DUT samples were ganged together to demonstrate ganged testing, but not too many as to complicate the T3 IC internal interconnect or complicate data collection from the IC. A goal of Five (5) ganged structures of each type provides sufficient sample size while keeping the internal interconnects required at a manageable level.

Representative Reliability Test

A representative reliability test is performed on each of the DUT types to prove the concept. The test conditions and run times are similar to actual benchmarking tests, however, the sample size is significantly smaller.

Data Collection

The T3 IC controls data collection off DUT structures. Types of data collected include:

Hot Carrier	Temperature
	Stress Time
	Frequency/ Duty Cycle of AC Stress signal
	Stress Voltage
	Parametrics: I vs. V curves at each stress interval
	Transconductance at each stress interval
Gate Oxide	Temperature
	Stress Voltage
	Stress Time
	Frequency/Duty Cycle of AC Stress Signal
	DC measurements at stress intervals

Test Plan

Pre-Test

Pre-test involves setting up stress conditions on each of the DUT groups and running short tests to verify operation of the circuits. In addition, this test is used to verify data collection from the

samples. A pretest to verify the integrity of the wafer-level HV GOX transistor switching components is performed prior to actual GOX testing. This test ensures that the switching transistors are not faulty, and that HV (to 27Vdc) can be applied to the structures without damaging the part. A second function of the GOX pretest is to determine actual level of HV that can be applied, which may be less than 27Vdc.

HOT CARRIER RELIABILITY TEST

Typical Hot Carrier reliability test: Run parametric tests on the N and P channel transistors (measure I vs. V and transconductance). Apply AC stress voltage for time, t to the gate of the transistors while maintaining a stress voltage on the drains of the N and P transistors. Remove the stress from the transistors. Re-measure the DC parameters of the N and P transistors. Repeat for the following intervals: 1, 3, 7, 10, 30, 70, 100, 300, 700, 1000, 3000, 7000, 10,000 seconds.

OXIDE DEGRADATION RELIABILITY TEST

Test performed is a typical Gate Oxide Degradation VRAMP reliability test: Measure DC parameters of the gate oxide capacitor at room temperature. Ramp AC field stress to the gate of the capacitor for time, t. until the capacitor breaks down or current compliance is attained in the power supply.

DATA REDUCTION

Data is reduced to charts and graphs, with lifetimes extrapolated from the data set. Issues for data reduction include the limited time available for manual data reduction. Instrumentation (I.e the Keithley source meters) dynamically reduces data to a graphical format while data gathering is in process.

REPORTING - SAND REPORT

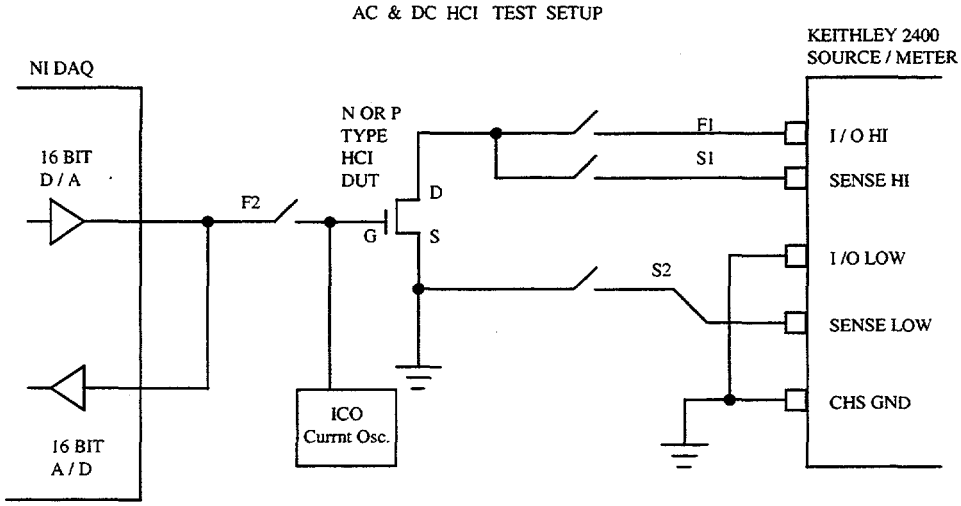
As the final year of the TORCH-3 LDRD, a SAND report is required. This report is submitted before the end of the 1997 fiscal year.

Test Procedure

HCI TEST PROCEDURE

The Hot Carrier test procedure consists of parametric pre-tests, timed over-voltage stressing, and post-test parametric tests. The TORCH-3 hot carrier test setup is shown below.

HCI Test Setup Diagram



OPERATION #1

TRANSISTOR CHARACTERIZATION:

1. Apply gate voltage --> 1 V, Vgs
2. Ramp Drain Voltage, --> Vds 0 --> 5V and monitor current, Id and D-S Voltage, Vds Record values per step, Calc. & plot I-V, Gm
3. Increment gate voltage, Vgs --> 2 V
4. Ramp drain voltage, Vds --> 0 --> 5 V and monitor current, Id and D-S voltage, Vds Record values per step
5. Repeat for gate voltages of 3, 4 and 5 votls

OPERATION #2

STRESS MOSFET FOR HCI DEGRADATION

1. Apply gate voltage of 2.5 V
2. Apply drain voltage of 6 - 8 V, Vstress
3. Measure and record drain voltage.
4. Remove stress after 1 sec.
5. Perform Operation #1 and record I-V and Gm.
5. Repeat 1 -3, and 5 for stress times of 3, 7, 10, 30, 70, 100 sec, etc.
6. Continue until parameters degrade >10%.

HCI Parametric Test Procedure

1. Values to be derived from HCI parametric testing include Threshold voltage Vt, transconductance (Gm), and drain current (Id) vs gate voltage (Vg).
2. The Keithley 2400 Source Meter is configured to simultaneously source Vd while measuring Id. The NI 16Bit D/A converter supplies the gate voltage, Vg.
3. Configure the HCI array to connect one of five HCI DUTs to the Keithley 2400 via F1, S1, and S2 of the analog port. Connect F2 to the NI D/A output.
4. Force the FET drain to source voltage, Vds of 0.1 volt, typically. Measure the applied voltage differentially via the Keithley 2400.
5. Using the NI D/A, sweep the Vgs from 0 to 5 Vdc, in 100 increments.
6. Use the feedback loop to measure the applied Vgs via the NI A/D converter. Record in an array.
7. Measure Ids at each step and record in an array vs. Vgs.
8. Plot Id vs. Vgs at Vds = 0.1.
9. From the Ids array, calculate the maximum slope of the Id vs Vgs data. This is the transconductance, Gm.
10. Repeat 1 through 8 for each of the HCI DUT's, testing one at a time.

HCI DC Stress Test Procedure

1. Using the HCI test setup, connect F1, S2,, S1 to the Keithley 2400 source meter and F2 to the NI 16 Bit D/A converter.
2. Apply the HCStress voltage Vds of 8 Vdc to the drains of the HCI DUTs.
3. Measure the applied Vds differentially via the Keithley 2400. Record.
4. Adjust Vds if necessary to recalibrate the Vds voltage.
5. Ready a timer (via LabView) to apply the gate voltage for a pre-specified time of 1, 3, 7, 10, 30, 70, 100, ...etc seconds up to 1000.
6. Start at 1 second for initial gate voltage application.
7. Enable all HCI DUT's.
8. Apply the gate voltage Vgs of 2.5Vdc via the NI D/A converter.
9. Leave stress on for the pre specified time.
10. Remove the stress voltage and gate voltage after the stress time is complete.
11. Perform the parametric test procedure to determine if the performance of the DUTs has decreased by 10%.
12. Repeat steps 1 through 11 until the HCI DUTs have degraded 10%.
13. If one but not all DUTs have degraded 10%, then this DUT may be removed from the stress conditions.

HCI AC Stress Test Procedure

1. The AC stress procedure is identical to the DC stress procedure, except that the gate voltage is applied internally via a clock signal instead of the NI D/A converter.
2. Configure the ICO (Internal clock) via its register.
3. Repeat steps 1 through 13 of the DC procedure, but do not connect the NI D/A via F2.

HCI Post Test Procedure

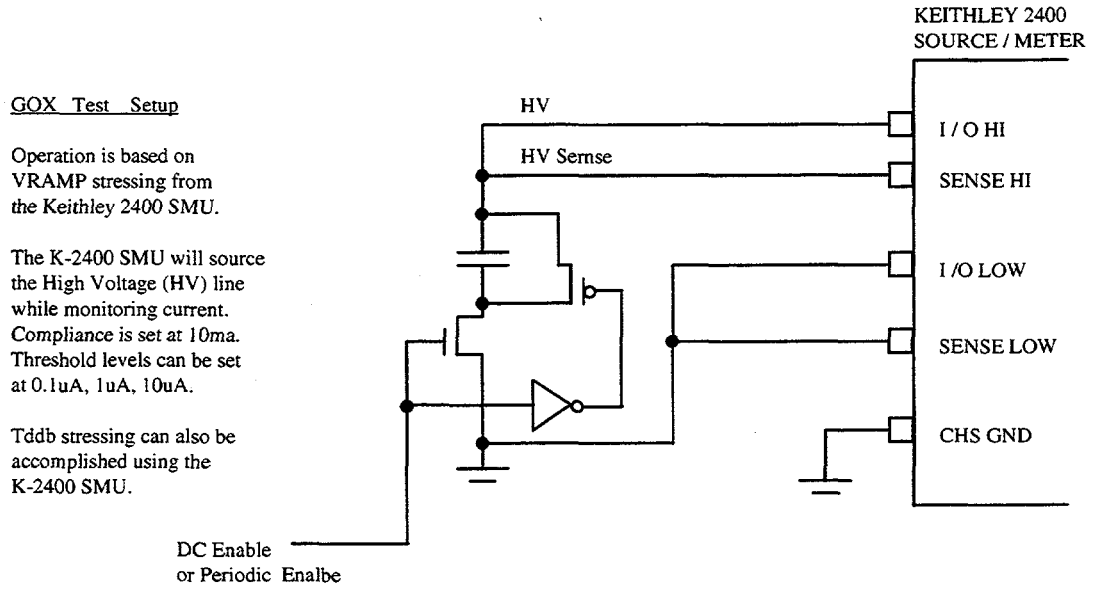
1. The HCI post test procedure is comprised of performing the parametric tests on each of the DUTs. In addition, typical transistor performance curves may also be generated.

GOX Test Procedure

The gate oxide test procedure consists of DC and AC tests as follows:

1. Perform the GOX pre test to determine the breakdown voltage of the DUT switching transistors.
2. Perform either the VRAMP test or the Tddb test.

GOX Test Setup Diagram



GOX Pre Test

1. The GOX DUT array uses high voltage MOSFETs to enable and disable each of the GOX DUTs. Manufacturing defects in these transistors can manifest at high voltages. A pre-test of each of the GOX DUTs is necessary to weed out faulty transistors prior to actual GOX testing. The procedure is as follows for each of the GOX DUTs under test.
2. Using the Keithley 2400 source meter, set a current compliance of 1uA.
3. Enable one GOX DUT.
4. Ramp the voltage until current compliance is reached, or 27 Vdc is reached.
5. This voltage becomes the maximum voltage that the switching transistors can withstand before breakdown is reached.
6. Use this voltage as the maximum ramp voltage for this DUT array.
7. Repeat for each DUT to determine the minimum DUT transistor breakdown voltage.

GOX DC Vramp Test

1. Enable the either the DC or AC GOX capacitor DUT array.
2. Prepare the Keithley 2400 source meter (K2400) for ramp of gate voltage from 3.3 to end voltage of 27Vdc, calculated from the 225A oxide thickness, knowing that 15 MV/cm is the maximum field.
3. Prepare the K2400 for the ramp rate of 1 Mv/cm sec.
4. Prepare the K2400 for current compliance of 10ma.
5. Ramp the gate voltage while monitoring the current and record both.
6. Detect breakdown of one of the DUTs by detecting rapid changes in the gate current, a ten fold increase in gate current, compliance of the K2400 is reached, or the maximum voltage is reached.
7. Disable all GOX DUTs.
8. Reset the current compliance on the K2400 to 1uA.
9. One by one, re-enable the GOX DUT's until 1uA compliance is reached.
10. Disable the GOX DUT that caused the compliance.
11. Resume the ramp test with the remaining DUTs at the previous gate voltage.
12. Continue ramping until compliance is reached again.
13. Repeat steps 7 thru 12 until all GOX DUTs are failed or you are tired.
14. Plot the results in real time.
15. Perform post test.
16. The AC test is identical, except the caps are only enabled for the duty cycle prescribed.

GOX DC TDDB Test

1. Calculate the stress voltage from the desired stress field and GOX area.
2. Perform leaky oxide test according to the pre-test section. Record Ileak.
3. Enable the GOX DUTs.
4. Apply the stress voltage via the K2400 and wait for breakdown to occur or max time.
5. Record the time periodically, according to calculations.
6. Record the values of breakdown field, Vbr, breakdown voltage, Fbr and breakdown time,Tbr.
7. Plot the results.

GOX AC TDDB Test

The GOX AC test is the same as the DC test except the DUT is enabled according to the duty cycle set during the structure setuptbd...

DATA REDUCTION - SAND REPORT

The Torch 3 die array layout was electronically sent on June 4,1997 to the Orbit Semiconductor Inc. Foundary to be made with their Foresight prototyping process. Since typical Foresight turn-around times are 6-8 weeks, this schedule would have allowed for finished dice to arrive at Sandia by the end of July 1997, leaving ample time to set-up and begin system evaluation testing before the end of FY1997. However, Orbit experienced unusual processing delays and, as of the writing of this report, had not delivered finished Torch 3 dice.

Based on the performance of the Torch 1 and 2 dice, there is high confidence in the potential performance of the Torch 3 die array. The only unknown involves the gate oxide test structures and what maximum voltage the high-voltage level shifters can withstand. Evaluation testing of the LabVIEW™ control software with discrete transistors and capacitors (see Appendix B) show

proper execution of the test procedures outlined above. Since, the funding for this 3 year LDRD ends FY1997, any testing of the system with the Torch3 die and addendums to this report to document that testing will be contingent on other funding sources and the availability of personnel.

Conclusion

Integrating complex test functions directly on product IC, the Application Specific Tester On a Resident Chip (TORCH) LDRD project reduces the dependence on expensive, large and inflexible test equipment. The 4-wire IEEE-1149.1 Boundary Scan digital test bus with the TORCH LDRD-developed 4-Wire Analog bus allows Kelvin measurements directly on product test die. Commercial Off The Shelf (COTS) controller hardware and software configures the IC while the boundary scan bus allows full IC functional and open/short testing. The combination of the boundary scan bus and the analog bus allows an IC to be fully tested using less than 20 pins or connections - a significant improvement when compared to traditional "bed of nails" testers or other probing methods that require many hundreds of contact pins.

In year three of this LDRD we compiled the learning from year's one and two and created an automated reliability and parametric test system that configures and tests ganged transistor and capacitor structures. Boundary scan protocols are used to setup the test structures and the analog bus is used to collect the parametric data from the structures under test. The IC control and data analysis system are based around the COTS program, LabVIEW™, an open software system that allows development of custom user interfaces. The end result is that the boundary scan protocols, key to the operation of the system, become transparent to the user, allowing the tester to concentrate on *testing* the part vs operating the IC. We have re-used the COTS boundary scan controller from TORCH - 2, and have used external source-measurement units (SMU) for ease of prototyping. Any future derivatives of TORCH technology should consider replacing the external SMU units with on-chip SMU's derived from the logarithmic autoranging analog to digital converter developed in TORCH-2

Appendix - A: Reliability Test Structure Notes

Electromigration: Orbit HF_EM_11,12 (not used in TORCH3)

This section on electromigration is provided for reference only.

THEORY OF OPERATION

A typical Electromigration failure is induced by the following sequence:

1. High current densities induce migration of metallic atoms.
2. Opens or hillocks form in the metal structure.
3. Results in an open in the EM line or a short to adjacent metal structures.

Refer to Dept. 1276 SWORD manual for wafer level EM algorithms to measure the time-to-failure of an electromigration test structure when Joule heating (current induced) is used. TORCH-3 EM structures will not incorporate heaters in addition to Joule heating to accelerate the failure mechanism.

This structure is used to examine electromigration at high frequencies (>400MHz). It consists of a current controlled oscillator which is used to stress an 800 micron line of metal 1 or metal 2. The ring oscillator converts DC currents into high frequency waveforms which are applied to the ASTM standard metal line. The AC stress is applied for a period, as determined by experiment design, and then removed. The metal line is then measured for resistance using a 4-wire Kelvin method to gauge the electromigration damage. The frequency of the ring oscillator can be varied from 10 Hz to 700 MHz and duty cycle can be varied from 10 to 50%. A polysilicon heater and temperature sensor are provided for examining temperature effects on the electromigration line. Two current controlled buffers drive the metal line. This permits precise control of the peak current through the metal line during AC stress. Two buffers are used in a push-pull arrangement to distribute the current through the line more uniformly.

The HF_EM_11,12 test structure has the capability of performing DC or pulsed DC testing.

EXTERNAL STIMULUS

The electromigration structure requires four external inputs that may not possible in a CMOS design. This requires that an external pad be allocated for each of the inputs. I IN and I OUT are DC Current inputs that may be as high as 5 ma each. VHTI is the polysilicon heater input and VHTO is the polysilicon heater output that may have voltage applied up to 40VDC at 300ma.

EM TEST STRUCTURE DESIGN RULES

All EM tests require a Kelvin (four terminal) measurement of resistance. A properly designed EM test structure is necessary for accurate measurement. The structure has voltage taps at ends of the structure; runs from the bond pads to the voltage and current taps are at least twice the minimum width of the metal structure under test.

The structure may have extrusion monitors, which are typically minimum pitch metal lines running parallel to the structure. The extrusion monitor is used to check for shorts due to

electromigration induced hillock growth. A vertical extrusion monitor can be created with a M2 plate over M1.

Hot Carrier: Orbit HF_HC_18

THEORY OF OPERATION

For MOSFET devices, small channel lengths lead to high electric fields in the drain region. These high electric fields cause energetic carriers - Hot Carriers - which create interface states or become trapped in the oxide. The damage to the SiO2 or SiO2/SI interface is reflected in the shifts of key transistor parameters such as threshold voltage or maximum transconductance. Accelerated hot-carrier-induced degradation of MOS transistors is performed by repeating a stress/measure sequence: applying a stress voltage at the gate, drain and bulk terminals for a specified time and then measuring the change in DC parameters, see Figure 2.2.1. Typically, the stress is repeated until a parameter changes the desired amount (typically 10%).

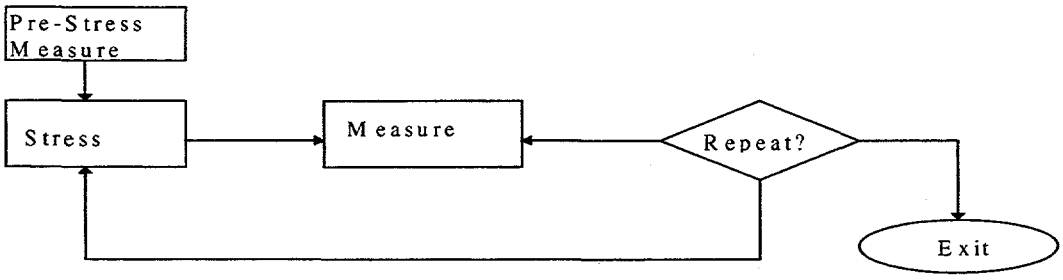


Figure 2.2.1 HCI Test Flow

The HF_HC_18 structure is used to examine hot-carrier induced degradation at high frequencies (>400MHz) and at DC. High Frequency testing is used to examine the effects of pulsed signals on HCI. The structure consists of a current controlled oscillator which stresses an inverter with a 1X load. The ring oscillator converts DC currents into high frequency waveforms which are applied to the capacitor. The AC stress is applied for a period, determined by experiment design, and then removed. The transistors in the inverter are then characterized for DC parameters (IV curve and transconductance) to determine hot carrier degradation. This can be used to verify the quasi static hot-carrier model for a particular technology. The inverter chain is provided to measure propagation delay as a function of hot-carrier induced degradation. The chain is stressed with AC signals and measured with AC signals and compared to the monitor output. The resultant change in propagation delay of the inverter chain is attributed to stress. The frequency of the ring oscillator is varied from 10 Hz to 700 MHz and duty cycle is varied from 10 to 50%. A polysilicon heater and temperature sensor are provided for examining temperature effects on oxide integrity.

The HC_HF_18 has the capability of DC or HF hot carrier degradation testing.

SIGNAL DEFINITIONS: ORBIT HF_HC_18EXTERNAL STIMULUS

The hot-carrier structure requires two external inputs that may not possible in a CMOS design. This requires that an external pad be allocated for each of the inputs. VH is a high voltage input for stressing the inverter transistors above the design margin of the part. This is typically 8 to 10

volts. VHTR is the polysilicon heater input which is deleted in the TORCH-3 design as the hot-carrier structure does not need a heater.

HOT CARRIER TEST STRUCTURE DESIGN RULES

The Hot Carrier Injection test Ss require an N-channel or P-channel MOSFET to perform hot-carrier-induced degradation. At a minimum, the device includes separate gate and drain contacts, but ideally include the following:

1. **Separate gate, source, drain and substrate terminals** which permit independent control over the gate voltage and drain voltage as well as independent monitoring of the substrate and gate currents.
2. **A large substrate contact encircling the device.** This reduces the source to substrate resistance which increases the maximum drain stress voltage. A larger drain voltage reduces the test time.

Gate Oxide Integrity: Orbit HF_OX_5

THEORY OF OPERATION

An oxide test algorithm forces a charge through an oxide until a failure is detected. Two methods are used to accelerate the failure. Voltage ramp algorithms increase the voltage across the oxide at a constant linear rate until the oxide breaks down. Beginning at the expected operating voltage of the oxide, the voltage is increased until either the oxide ruptures or current compliance on the source supply is reached. As the voltage and the electric field increases, the current flowing through the oxide increases due to Fowler-Nordheim tunneling until a short is produced in the oxide. The algorithm determines the voltage at breakdown and the field at breakdown. Refer to the SWORD manual for details concerning data collection, reduction and presentation.

This structure is meant to examine oxide integrity at high frequencies (>400 MHz) and at DC. It consists of a current controlled oscillator which is used to stress gate-oxide capacitors. The ring oscillator converts DC currents into high frequency waveforms which are applied to the capacitor. The AC stress is applied for a period, determined by experiment design, and then removed. The capacitor is then measured at DC for oxide breakdown. The frequency of the ring oscillator is varied from 10 Hz to 700 MHz and duty cycle is varied from 10 to 50%. A polysilicon heater and temperature sensor are provided for examining temperature effects on oxide integrity.

A typical Gate Oxide stress test for TORCH is at DC levels. However, pulsed DC at high frequency is used for lifetime comparison purposes.

EXTERNAL STIMULUS

The gate oxide structure requires two external inputs that may not possible in a CMOS design. This requires that an external pad be allocated for each of the inputs. VHTR is the polysilicon heater input and DGND is the polysilicon heater output that may have voltage applied up to 40VDC at 300ma.

TEST STRUCTURE DESIGN RULES

There are six basic rules for the design of gate oxide test structures, based on experience with over nine different designs.

1. **Minimize Conductor Length:** The conductor running to the gates and well/substrate/tub must be of a minimum length in order to minimize series resistance to the test structure. If it is not, there is a significant voltage drop in this line, especially at or near the currents used for rapid breakdown testing. If such voltage drop occurs, large erroneous Vbr readings result. Long lines of high resistance may also cause the opening of the line by fusing before the oxide test structure fails.
2. **Maximize Conductor Width:** All statements made pertaining to rule 1, above also apply here. Maximize the line width given the constraints imposed by other nearby structures.
3. **Maximize Number of Gate Contacts:** By maximizing the number of gate contacts, the structure has a minimum series contact resistance, thereby ensuring that nearly all of the stress voltage is dropped across the oxide. With one or only a few contacts, contact failure before or during oxide breakdown can occur. Such failures can result in abnormally large values of Vbr recorded, as well as a self-healing failure mimicked.
4. **Maximize the Number of Well/Substrate/Tub Contacts:** All statements pertaining to rule 3, above also apply here.
5. **Provide a Minority Carrier Source:** Most oxide breakdown measurements are conducted in accumulation, where there is no need for a minority carrier source. However, in the event that the oxides are ever to be biased in depletion or inversion, a source of minority carriers should be provided so that the results are not carrier limited. Use of light, although potentially appropriate for smaller capacitor structures, does not provide the needed number of minority carriers in the center of the larger gate area structures. By providing a permanent source of minority carriers, their correct operation of the capacitors over both bias polarities is ensured.
6. **Design Capacitors to Have Representative Areas:** The major purpose of capacitor test structures is to quantify the defect density of the gate oxide. It is important therefore to have a structure with an area equal to the total gate area of the technology in question. In the case of measuring the "Intrinsic' breakdown field of gate oxides, it has been shown that the field varies as 1.log(area) according to the extreme value distribution. Very small capacitors may lead to erroneously large values of Vbr. The best sets of oxide test structures have a series of capacitor areas, varying from the area of a single transistor gate, to the area of all the gates combined.

Common Functions of Reliability Structures

HEATER AND TEMPERATURE SENSORS

The Hot Carrier and Gate Oxide Structures can share heater designs and temperature sensor designs. For both of these structures the DUT and temp sensor are placed inside the heater. The structures can share the heater and temperature sensor designs found in Orbit HF_HC_18, HTR_TSENSORN.

VOLTAGE CONTROLLED/CURRENT CONTROLLED OSCILLATORS

The Electromigration, Hot Carrier and Gate Oxide structures can share the ICO_2 oscillator found in the Orbit structures HF_HC_18, HF_EM_11,12, and HF_OX_5. This oscillator may be

converted to a VCO design if necessary. However, current TORCH-2 design incorporates an IDAC that may be used with the ICO_2 oscillator.

BUFFER STAGES

Structures can share output buffer designs (INVX). The design can be re-scaled.

Appendix - B: Summer Student Report -

(THE FOLLOWING IS THE REPORT SUBMITTED BY TIMOTHY J. PETERSON FOR THE SUMMER STUDENT INTERN PROGRAM)

I. INTRODUCTION [1]

TORCH 3 emerges from the two previous versions of TORCH, and culminates the TORCH LDRD (Laboratory Directed Research and Development). TORCH stands for Tester On a Resident Chip, a project dedicated to prove the concept that embedded reliability testing using an integrated test system can perform IC reliability and/or parametric tests on chip. This LDRD is born from the concerns of the semiconductor industry, which are evident by this quote from the 1994 Semiconductor Industry Association Roadmap, Design and Test Summary, Pg. 43: "The rapid development of VLSI using sub-micron CMOS technology has suddenly exposed traditional test techniques as a major cost factor that could restrict the development of VLSI devices Exceeding 512 pins and operating frequencies above 200 MHz." TORCH 3 approaches this concern by developing a new test technique which involves integrating special test structures together with many functions that are presently outside the test wafer. By combining the circuitry into one IC, test frequencies up to 500 MHz and simultaneous stressing and sequential parametric measurement of ganged test structures are possible. TORCH 3 also uses an IEEE Std.1149.1 boundary scan compliant serial test access port (TAP) to access the test structures, thus eliminating superfluous hardware connections in exchange for data control. The TORCH 3 IC (T3-IC) does require external high voltage sources for stressing, but the design accommodates full automation by a control computer. The die to die interconnects of the TORCH 3 ICs enable single probing coverage of a tested wafer, eliminating expensive multiple re-probings. Motivations for this project include low cost and simplified reliability testing, more effective testing by ganging structures, and automated PC-based reliability test.

A. System Goals

In essence, TORCH-3 will demonstrate mixed-signal control and test of reliability structures, and the final product of TORCH 3 will be a stand alone wafer level test system. TORCH 3 will perform two standard reliability tests, accelerated hot carrier injection (HCI) and gate oxide testing (GOX). The TORCH 3 system is controlled by a PC platform, and two low cost, accurate, computer controllable Source/Measurement Units (SMU) perform the stress and measurement of the test structures. The SMU must be capable of 4 wire operation, so that the SMU's output voltage is compensated for lead-in resistance. Other lower power analog and digital control and measurement signals operate the T3-IC, so TORCH 3 uses a controlled I/O port, such as a data acquisition card. T3-IC's boundary scan compliant TAP requires the proper sequence of bits over 4 communication lines which will also be externally controlled. The physical interface between the external devices and the T3-IC must establish contact between the two and provide test points to verify system signals. The software must organize and sequence the set-up and test procedures; it must access desired test die, access desired test structures or oscillator control circuitry, and perform the particular test. The software must also recover data from the SMUs and provide analysis tools. To do this the computer has to control the data going

into the TAP, the operation of the SMUs, the operation of the data acquisition card, and the data and file management at the direction of the operator; all while remaining relatively flexible and easy to learn.

B. My Goals

The state of the system upon my arrival is given to clarify the extent of my involvement.. The T3-IC was sent to Orbit, the fabrication facility selected to produce the T3-IC, in early June; and I became familiar with the requirements to operate the chip and the software programming language LabView with which the control software would be written. Only a rough draft of the interface card existed and most of the buffering and switching had not yet been designed. The chosen SMUs, Keithley 2400s,were on site but the TORCH team had not yet learned to use them. The SMUs and the controlling computer both have GPIB standard interface capabilities. The data acquisition card, a NI-DAQ computer card, and its breakout box were also installed, but its operation had not yet been confirmed. A Corelis PCMCIA (a type of PC card) boundary scan controller card was included from TORCH 2 to simplify the execution of the boundary scan commands.

My goal became to complete the system so that T3-IC could be incorporated upon its arrival and the TORCH 3 system tested and completed in mid August. To meet this goal I had to design the software according to the TORCH 3 specifications, design and send out for fabrication the interface card, and verify the operation of the entire system.

C. Background of Physical Reliability

This next section discusses the relevance of physical reliability and the types of test performed by the TORCH system. Physical reliability of CMOS circuits (the most common type of integrated circuits) varies for several reasons, most of which are due to manufacturing inconsistencies. Physical reliability should not be confused with functional reliability where faults are caused by misplaced part arrangement, errors in design or errors in layout. Rather physical reliability is the measure of a circuit's ability to withstand the forces exerted on it by electrical or mechanical operations; it makes the prediction of how long the material will perform as intended to. Many phenomena have been linked to the reliability of CMOS circuits produced on silicon wafers. The TORCH 3 System evaluates hot carrier injection (HCI) and gate oxide degradation phenomena. The SWORD manual, a Sandia written wafer level reliability reference standard, provides details concerning test algorithms, data collection, reduction and presentation.

1. Theory of Operation, HCI[2]

For MOSFET devices, small channel lengths lead to high electric fields in the drain region. These high electric fields cause energetic carriers - Hot Carriers - which create interface states or become trapped in the oxide. The damage to the SiO_2 or SiO_2/SI interface causes shifts of key transistor parameters such as threshold voltage and maximum transconductance. Accelerated hot-carrier-induced degradation of CMOS transistors is performed by repeating a stress/measure sequence; applying a stress voltage across the transistor drain and source terminals with the transistor turned on (appropriate voltage at the gate) for a specified time and then measuring the change in DC parameters, see *Figure 1*. The stress is repeated until any parameter changes the desired significant amount (typically 10%) and the transistors lifetime is extrapolated.

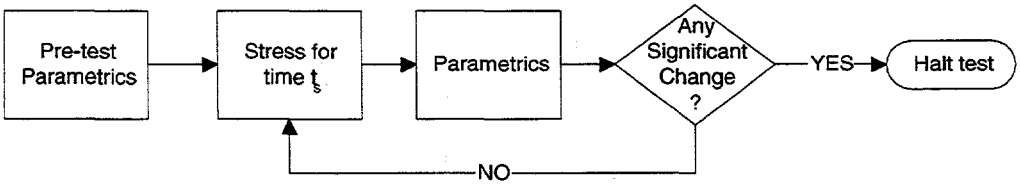


Figure 1: HCI Test Flow

The T3-IC incorporates specially designed NMOS and PMOS transistor arrays as test structures (DUTs). The variable frequency oscillator can turn the transistors on and off during an AC stress test. With high frequency testing, the TORCH 3 System examines the effects of pulsed signals on CMOS transistors.

2. Theory of Operation: GOX[3]

The oxide layer in CMOS Circuits is used as an insulator, or a dielectric material for capacitors and for field effect transistor (FET) gates. FET gates require a high quality oxide called gate oxide. TORCH 3 uses two SWORD methods to test the gate oxide layer, VRamp and TDDB. In the VRamp algorithm, the expected operating voltage is applied across the DUT and then the voltage increases at a constant linear rate and the characteristics of the resulting current vs. voltage curve are observed. As the voltage and the resulting electric field increase, the current flowing through the oxide usually increases due to a phenomena called Fowler-Nordheim tunneling, where the insulating oxide begins to conduct due to trapped ions. Eventually a short may be produced in the oxide; such shorts render capacitors or FET transistors useless. A second method for testing Oxides, TDDB (Time to Dielectric Breakdown) is to apply a constant high voltage until a short, dielectric breakdown, is achieved. The time this takes indicates the endurance of the wafer's oxide layers.

II. SYSTEM DESCRIPTION: The materials

The TORCH 3 System consists of 4 main Hardware sub systems, T3 IC die (yellow), the Computer/Operating System (blue), the SMUs (orange), and the Interface Circuitry (green). Each T3-IC die includes a test access port (TAP), GOX and HCI test structures or devices under test (DUT), the on-board oscillator circuit which is made up of a current controlled oscillator (ICO) and a Phase Locked Loop (PLL), the boundary scan data registers, and DUT switching matrices. The simplified system diagram is shown below. Note that several die can be linked together, and in fact the T3-IC part presently in fabrication contains nine interconnected test die.

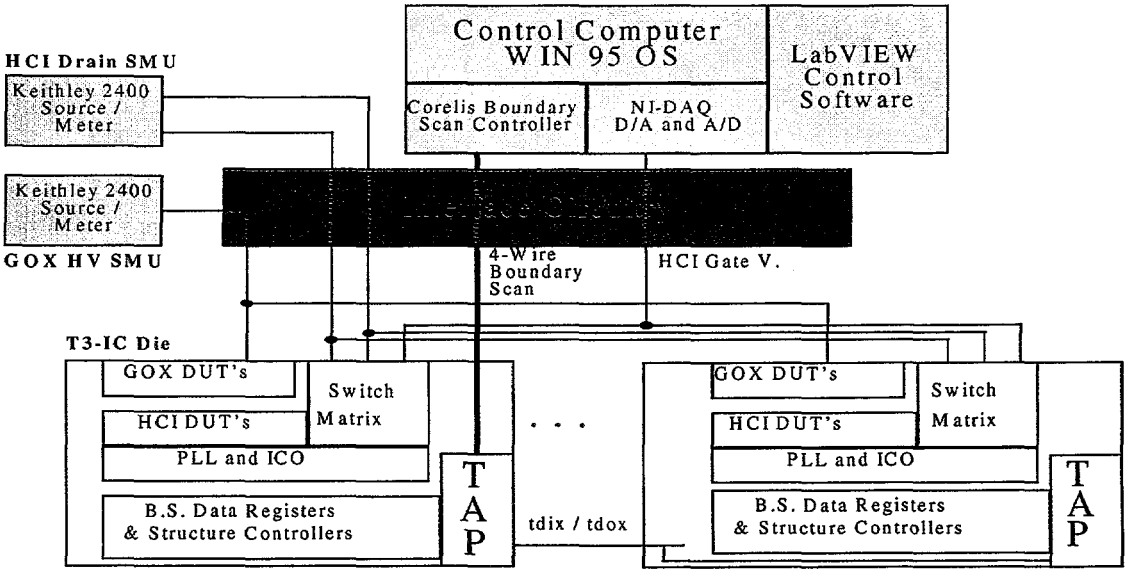


Figure 2: TORCH 3 System Diagram

A. The TORCH 3 integrated circuit, T3-IC

T3-IC is controlled via the TAP, and the structures are stressed via ports common to all the die. TORCH-3 operates from 0 to 5 volts for digital circuits and 0 to 8 Vdc for analog circuits. The GOX and HCI DUT arrays have independent external stress voltage sources accessible through analog ports. These analog ports are F1, F2, HV, S1, S2 and HV Sense, V+ and VSS(ground). The T3-IC 52 pin die also includes the 4 boundary scan connections TMS, TCK, TDI, TDO, the inter-die connections TDIX and TDOX, and circuit function checkpoints VERR, FREF, PHI, MON, and PUC.

There are several modes of operation for the T3-IC, HCI for NMOS, HCI for PMOS, PLL setup, ICO setup, GOX tests, and Bypass. The commands sent to the TAP reconfigure the data registers to setup a particular mode. For instance, if a command accesses the data register dedicated to the ICO, the subsequent command modifies the ICO circuitry. The controlling software coordinates the events at the analog ports with respect to the mode of the selected test die.

During the HCI for NMOS and PMOS the gates of the MOSFET DUTs are controlled at F2, the Drains at F1, and the transistor source is controlled by V+ for PMOS and by VSS for NMOS. S1 is the remote sense line for F1 and S2 is the SMU terminal that is switched to V+ during PMOS operation and VSS During NMOS operation. PMOS DUTs must be operated in the opposite polarity of the NMOS DUTs, but T3-IC is not capable of handling negative voltages, so V+ raises the PMOS transistor source voltage so that the gate and drain voltages are still positive. Mode selection through the TAP and commands to the HCI NMOS or PMOS Data registers accommodates the appropriate switching of S2, the selection of DUTs and the switching between AC and DC operation. There are five FET test structures in each NMOS and PMOS array. Any combination of the five may be stressed, but for accuracy the system must perform parametrics on one FET at a time. Additionally the system may stress the structures in DC or in AC at the frequency set by the ICO, but it must perform parametrics in DC.

The GOX tests use the HV and HV sense lines. HV is the high voltage stress supplied by a SMU and HV sense is the remote sense line for HV. The Substrate is the lower potential terminal

for the GOX DUT and is tied to VSS. The GOX data register includes selection for AC or DC test, enabling/disabling of two AC DUTs and four DC DUTs.

B. Control Computer

The control computer has the following characteristics: Desktop (Pentium class), 32Mb ram, 1.6Mb HD, two PCMCIA ports, with necessary keyboard, mouse and printing ports. The operating system is Windows 95, and additional required software includes LabView 4.1, HiQ, and appropriate device drivers. The additional components are the control software, the boundary scan controller, the data acquisition card, and the GPIB card. The Corelis PCMCIA 1149.1a boundary scan controller is the hardware used to convert software commands into boundary scan data chains to send and retrieve data from the T3-ICs TAP. This controller is in the PCMCIA (or PC Card) format for use in a laptop PC or a desktop PC with a PCMCIA drive installed. The Corelis PCMCIA 1149.1a requires the Corelis scan function dynamic link library to function. National Instrument's Data Acquisition card (NI-DAQ) provides control for the analog connection to the T3 ICs V+(PMOS FET source voltage), F2 (MOSFET gate voltage), and interface circuit's power-on switch. With this control computer the user is able to run the control software which in turn controls the SMUs, the NI-DAQ, and the boundary scan controller. The user is also able to evaluate the data, even while the computer performs stressing operations in the background.

C. The Source/Measurement Units, SMUs

The source measurement units supply the necessary high voltage stress to the DUTs as well as collect data, current, voltage and time. The torch team selected the Keithley 2400 because of its price, accuracy, and GPIB capabilities. The K-2400 is specified to perform 900 source/measurements per second to a GPIB call, providing ±210 volts at ±105 mA with an accuracy of better than 0.06% for current measurements within 100 mA at normal operating temperatures. TORCH 3 requires that the maximum voltage source be no more than 27 volts because of T3-IC limitations, the shortest source/measure cycle need not be shorter than 100 ms, and there are no heat requirements (where DUTs are heated for additional stress). Therefor, the K-2400 suffices. Among its most crucial features, remote sensing plays an important part in the accuracy of the TORCH system. Remote sensing is where the meter is able to compensate for voltage drop due to lead-wire resistance. The meter is able to adjust its voltage while simultaneously measuring current. With this capability and the specially designed switches in the T3-IC, the meter can perform very accurately. There are other GPIB programmable features of the K-2400. It is IEEE-488-1987.2 compliant and uses the 1995 Standard Commands for Programmable Instruments (SCPI). The TORCH 3 software uses these commands to perform various functions and settings of the K-2400. The two SMUs in TORCH 3 provide the following signals: SMU1 sources and remotely senses the MOSFET drain voltages and measures the drain current via F1, and its connection to S2 provides voltage reference. The Second SMU measures current and sources and remotely senses the positive voltage applied to the GOX DUTs via HV and HV sense with reference to its connection to VSS.

D. System Software

The control software is written in LabView. LabView uses a graphical programming language called "G" and creates an executable file called a Virtual Instrument (VI). A VI consists of user panels, the user interface, block diagrams, the programming arena, and Sub-VI's, where other VIs are called as subroutines. LabView is able to use the computer's operating

system to access plug in devices such as the Corelis, the NI-DAQ, and the GPIB Card, or any other device the computer has a device driver for. LabView accesses the devices and other programs in the

computer by the use of Windows Dynamic Linking Libraries, DLLs. User panels are graphical and operate from mouse selections, users make adjustments to variables and execute the program from here. VI's and Sub-VI's are similar to main programs and sub routines except they are strictly object oriented and can function stand alone.

III RESULTS: Control Software and Interface Card Design

The TORCH 3 control routine has a hierarchy designed to allow the user to perform the test without considering the details of the boundary scan commands, or the proper K-2400 settings. The only parameters that the user should be concerned about are the ones that apply to the test that is running, and those parameters are confined to the ranges that would not allow the user to adversely affect the system, for example the peak GOX DUT voltage is confined to the range 0 to 27V. The user is prompted if the range is exceeded. There are 3 main levels of hierarchy in the TORCH 3 software; the test executive, the test setup, and the test execution levels. The interface card is a custom probe card built according to my design. Semi-Probe Inc. in California is currently fabricating the card. The card should arrive at Sandia by the middle of August. For the interest of the SIP program, the administrative details that I personally handled concerning the card were collecting quotes, writing the Purchase Request, tracing the PO progress and discussing design adjustments with the engineers at Semi-Probe Inc.

A. The Test Executive, a Complete Control Software for TORCH 3

In the test executive the user makes selections from a front panel for the desired test function, either PLL setup, IDAC setup, HCI NMOS or PMOS test, or GOX TEST. The user also selects the die on which to perform the above function. Upon selecting a top level test, a second user panel pops up, and the user adjusts settings and/or runs the test. Controls on the user panel consist of the controls where the user adjusts variables and setting in the program, the run button by which the user executes the settings that are made, the abort button where the user can halt the program in an emergency, and the return to calling VI button where the user can return to the previous user panel. When the user selects the test die, only that die's registers are activated and all die in between are set to bypass mode. The test executive automatically activates the correct T3-IC data register for the test the user selected.

1. IDAC and PLL Setup

These Two VIs perform the interpretation of the user's command into the correct boundary scan signal. Both of these functions make an 8 bit data string. In the IDAC setup VI, the user adjusts the frequency of the onboard oscillator which continues in that frequency until changed or the part is turned off. The IDAC is the digital to analog converter that sets the frequency of the ICO. With this oscillator the AC stress tests are done. In the PLL setup VI, the user has the option to enable or disable the IDAC, select between internal (ICO) and external oscillators, and to select form other features like enabling or disabling a Johnson counter, a frequency divider, a filter buffer and a low voltage bias. The majority of all TORCH PLL setups will use the ICO frequency (internal) and have the IDAC enabled and all other settings disabled.

2. Hot Carrier Injection (HCI) NMOS and PMOS Virtual Instruments (VIs)

These VIs are nearly identical except for their treatment of the transistor source voltage and the direction of gate and drain sweeps. The user panel is from the VI called HCIExec.vi. This VI presents the user with the choices of which FETs to stress and test, and whether the stress will be AC or DC. If AC, the user must have configured the ICO before conducting the stress. The parametric part of the test is always done in DC and on one FET at a time. This VI programmatically sets the FETs in DC mode, and sequences through them during the parametric phase of the test. The VI also alerts the user that the parametric settings must be made before conducting the test, and presents the user an opportunity to make the setting by running the sub-VI titled HCI_Para_Exec.vi, which will be discussed later. The user sets the duration for the stress intervals in a sequence or by an exponential formula, the user can also set the stress voltage for each interval or have it remain a constant, the same goes for the gate voltage. Typical values for the stress times is a sequence like so: 1, 3, 7, 10, 30, 70, 100, 300, 700, and 1000 seconds. Typical values for the stress voltage and gate voltage are 8V and 2.5V respectively. It is also possible for the user to use a formula driven timing mechanism to stress at exponentially increasing times, following the equation:

$$t_s = c \cdot b^{x \cdot (i+1)} \tag{1}$$

where t_s is the stress time in milliseconds, b is the base, c is the multiplier, x is the exponent multiplier, and i is the interval count. The interval count is based on the count of the while loop that iterates the stress test, and begins at 0. HCIExec.vi executes according to the flow chart in *Figure 1*. The figure below, *Figure 3*, is an oscilloscope plot of the drain and gate voltage signals during an HCI stress sequence. It demonstrates the software's ability to sequence events according to *Figure 1*. The two 6V stress periods are 1 and 5 seconds long.

Figure 3: Annotated Oscilloscope Plot of an Stress Test Sequence by TORCH 3

The drain and gate voltage settings are magnitudes with respect to the voltage presented at the transistor source. The relation for NMOS and PMOS is shown below.

$$\begin{aligned} &For\ NMOS;\quad Vd_{nmos} = Vs_{nmos} + D_m;\quad and\quad Vg_{nmos} = Vs_{nmos} + G_m \\ &For\ PMOS;\quad Vd_{pmos} = Vs_{pmos} - D_m;\quad and\quad Vg_{pmos} = Vs_{pmos} - G_m \end{aligned} \qquad (2a\ \&\ 2b)$$

Where *Vd* is the actual drain voltage, *Vg* the actual gate voltage, D_m and G_m are the magnitude set by the user, and *Vs* is connected to VSS (0V) for NMOS and to V+ (+8V) for PMOS. This method produces correct operation [4].

a. A STRESS VOLTAGE VI: HCStress_II.vi

This program makes the K-2400 SMU produce a pulse for a duration from 5 ms to 1000 seconds with a confirmed accuracy within 1% of the input stress time, a more than satisfactory arrangement. The user makes settings to this VI by adjusting settings to its calling VI, HCIExec, so the user never really sees this VI's front panel. The program sets the K-2400 in 4-wire remote sense, Voltage source/Current measure, mode before the stress voltage begins. It uses the list function of the K-2400 to produce a set of voltages at a given value. The K-2400 takes at most 100 measurements during the list function, and the system produces a 5 ms initial pulse width. At these settings, the maximum stress duration is 500 ms, so the software calculates the necessary change to pulse width for larger desired stress times. The following algorithm is employed:

$$t_{sa} = C \cdot P_w;\quad where\quad C = floor\left(\frac{t_s}{P_w}\right);\quad and\quad P_w = \begin{cases} 5; & t_s < 500 \\ floor\left(\frac{t_s - 1}{100}\right) + 1; & t_s \geq 500 \end{cases} \qquad (3)$$

Where t_{sa} is the actual stress time in milliseconds, t_s is the desired stress time in milliseconds, and P_w is the pulse width in millisecond integers. *C* is the integer amount of values in the list, which never exceeds 100 using this formula. The floor function results in the integer quotient with the remaining decimal discarded.

HCStres_II follows the conventions in *Equation 2* concerning drain and gate voltages during PMOS operation. There some operational limitations of the Stress II VI. There can be no programmatic interruption during the Pulse, this is because the SMU completes the pulse operation before the data is sent to the computer. This presents a problem to the user if an unduly long duration is accidentally programmed of if some event requires the need for immediate shut-down of the SMU. The user can manually shut off the SMU output for any of these occasions and halt the operation of the VI then restart the test from the desired stress time. This anomaly is a trade off for a more accurate pulse times.

b. A PARAMETRICS VI: HCI_Para_Exec.vi

In this VI the user can configure the parametric test by changing the settings on the front panel or by recalling a saved setup from a specially design text file. The user can also save the settings for later use. During HCI test execution, all settings to the popped up panel of this VI

will take effect for all parametrics run in the test. This VI contains the option to run the parametrics alone without stressing. The user may select this option for any number of reasons to include testing of TORCH structures after exposure to harsh environments like radio activity, and the characterization of non TORCH transistors through simply modified connections. Another important function this VI, sequentially cycling through the DUTs that are selected in the stress test, is important because parametric must be performed on one DUT at a time. The VI does this programmatically, and assigns a DUT number to the data that is collected, so as to differentiate between curves in data analysis.

There are two sub VIs in HCI_Para_Exec.vi. The first one, Vg_curve.vi, produces a drain current vs. Gate voltage curve. The second, Id_vs_Vd.vi produces a drain current vs. drain voltage curve. The first is the most commonly used before and after stress iterations. The addition of the second provides the option to use both or either curve during the stress test and also provides complete stand alone parametric capabilities. Vg_curve turns on the SMU to a designated drain voltage and programmatically steps through the gate voltages with the NI-DAQ analog output connection to the gate via the F2 pin. The data returned is a two column matrix with the first column the Gate voltage and the second column the drain current. Gate voltage is sensed through a NI-DAQ analog input, and the drain current is collected by the SMU. Important data from this curve includes the FET threshold voltage and the maximum transconductance, which were mentioned earlier in the background. Future optimization includes automatically tracking these phenomena. The second curve is similar to the type generated by commercial curve tracers, and like the first it is capable of generating multiple steps. Id_vs_Vd sets a gate voltage via the NI-DAQ and F2, and uses the SMU's step function to finitely ramp a voltage across the FET drain via F1. The user can set the ramp step resolution, keeping in mind the increased resolution requires increased time and data storage. Default settings use 100 steps and three curves (different gate voltages). The data collected by this vi include a two column matrix with Drain voltage being the first and drain current being the second. Both are returned by the SMU. A demonstration of these VI performance is shown in *Appendix A*.

3. Gate Oxide (GOX) Tests

TORCH 3 uses three independent GOX tests, the pre test, VRamp, and TDDB. When the user selects to perform GOX test from the test executive the GOXEXEC VI front panel appears and reminds the user to setup the IDAC if AC test will occur. From GOXEXEC, the user selects the DUTs to use, the test mode, AC or DC, and one of the three tests to perform. The TORCH 3 specification strongly urges the test take place in this order: pretest, VRamp and TDDB. The pretest does two things: first it determines the condition of the high-voltage switches on T3-IC associated with a particular GOX DUT, and second it indicates the maximum voltage to be used in the other tests. The pretest applies the initial voltage to the DUT via HV. It then reads the current from the SMU and determines whether it has reached a user determined threshold. If the threshold current is not reached, then pretest proceeds to the next voltage level. This VI repeats the process until the threshold current is reached, and then it records the last voltage as the maximum stress voltage.

In VRamp, the user sets up a voltage sweep to be performed by the SMU, with the maximum voltage being less than or equal the maximum voltage defined by the pre test. VRamp causes the SMU to perform the sweep and the data returned by the SMU is a two column matrix with Voltage as the first and Current as the second. The VRamp VI borrows most of its routine from Id_vs_Vd.vi, the VI used in HCI analysis.

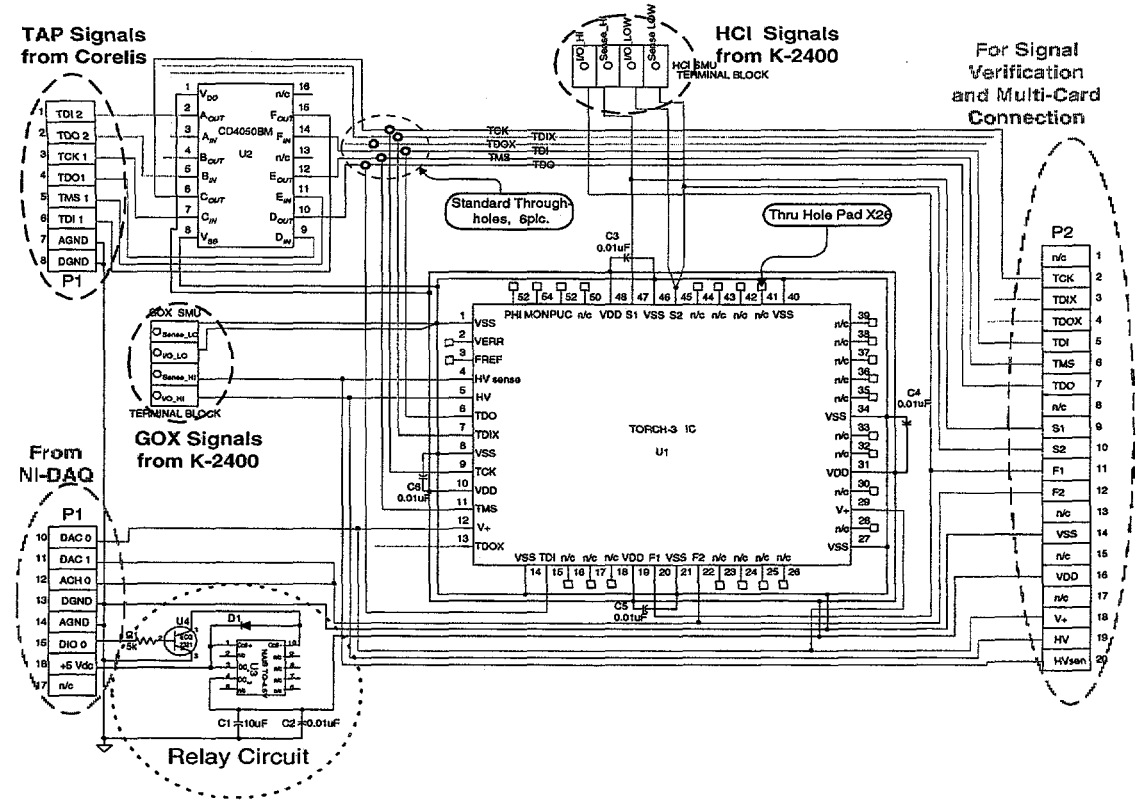
The last test is TDDB (time dependent dielectric breakdown). The user is warned that this should be the last of all test performed on any die because of the failure mode inflicted by the test. Here the DUT is stressed at the user set maximum voltage until the user set breakdown current reached; the time this takes is recorded. The program to do this is TDDB_ONE.VI., sets the SMU's Voltage to the user setting (which is less or equal to the Maximum Voltage defined by the

pre test) and sets the SMU current compliance to the breakdown current. It then applies the voltage and checks the current against the breakdown limit. It repeats this step until the limit has been reached or the user stops the test. The data is a two column matrix containing the current at each reading in one column and the time at each reading in the second column. Each iteration of the reading and time calculation requires from 40 to 60 ms because the iteration is done programmatically, and the time accuracy is within 100 ms of the recorded value, which meets the requirements considering the test usually is longer than 10 seconds. For AC test, TDDB applies the maximum voltage to the T3-IC and the ICO applies it to the DUT at the set frequency. The gate oxide test also incorporates the same setup save and recall options that the HCI test does.

B. Hardware Interface

1. The Interface Probe Card

My part of the Card design included buffer selection for boundary scan digital signals, relay circuit design to switch power to the T3-IC, probe type selection, and reporting probe tip coordinates. The card is a 4.5"X8" two layer fiberglass card with epoxy bound beryllium-copper probes set to T3-IC pad coordinates. There are three DIP packages on the card, a CMOS CD4050 for boundary scan signal conditioning, a packaged BJT, and a Dual throw, double pole 4.5 V relay. Also on the card are decoupling capacitors between VDD and VSS, a resistor and a diode for the relay circuit, and two capacitors to filter relay bounce out. Two four post terminal blocks provide connection for the two SMUs; a 48 pin edge connector provides connection for the Corelis boundary scan controller and the NI-DAQ; and a 20 pin right-angle header (RH) allows for breakout for signal analysis and serial connection for another card. In order to lower resistance between the T3-IC and the SMUs, the card design implements wider traces for F1, S1, HV, HV sense, VDD and VSS. Each these traces has a total width of 3 mm. A color coded schematic for the probe card is shown as *Figure 3*. Red wires are HCI lines, green are GOX lines, blue are TAP lines, gray are die interconnect line, and black are ground and power lines.



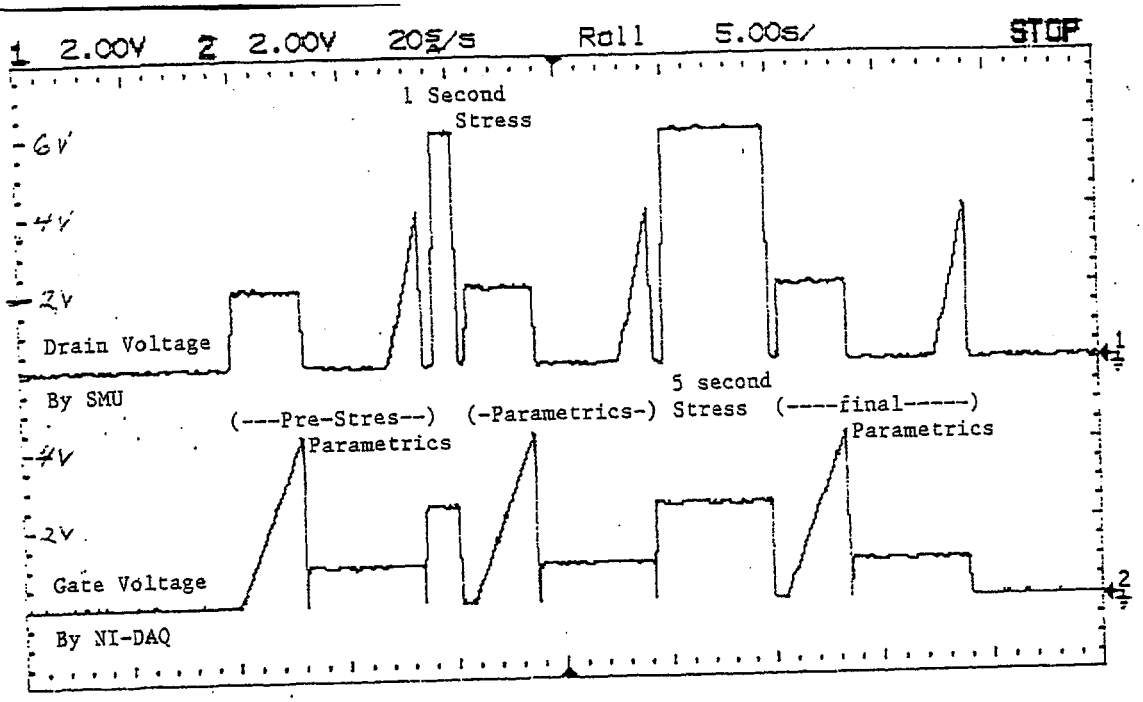


Figure 3: TORCH 3 Interface Probe Card Schematic and Signals

The relay circuit uses a dual throw mechanical relay to assure good continuity and low voltage drop for the VSS T3-IC voltage. This voltage is provided by the NI-DAQ board's VDD and the switch operation is performed by a NI-DAQ digital output. When the output is asserted

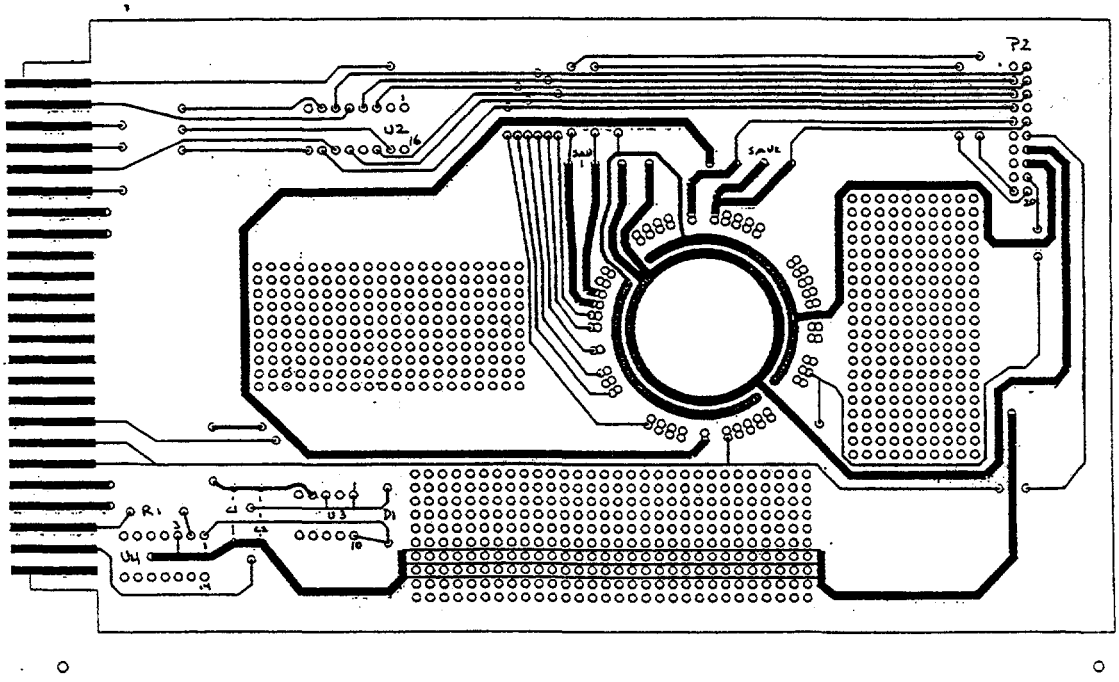
the relay connects the NI-DAQ power and the VSS terminal of the T3-IC. When the output is off, the relay connects VSS to Ground. Because of low switching resistance and the low current of the NI-DAQ digital output, a transistor is added to drive the switching signal.

C. Reference to Results shown in Appendices

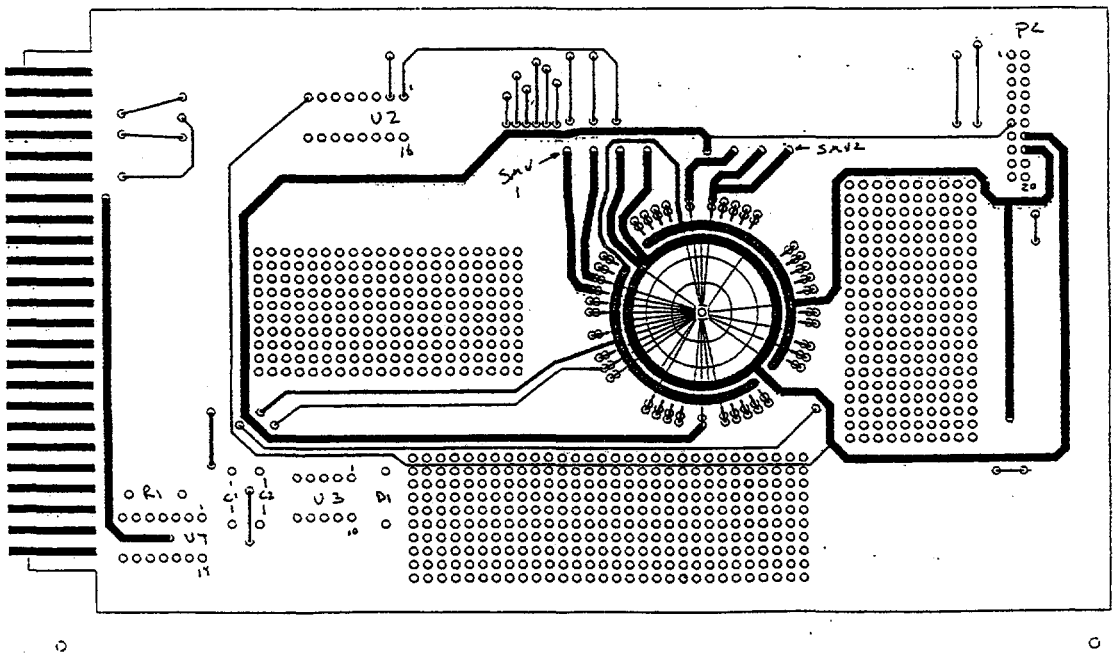
The curious reader is strongly urged to observe the figures in *Appendix A*, which are printouts of the Vg_curve.vi and Id_vs_Vd.vi front panels after the TORCH 3 system, (without the probe card and the T3-IC), performed parametrics on a packaged npn BJT Transistor. Each parametric test contains 4 characteristic curves. The curves are generated according to the settings shown. *Appendix B* contains the probe card layout sent for verification by Semi-Probe, the top and bottom layers. The thicker traces are VSS, VDD, and the SMU to T3-IC interconnects. The three rectangular regions with little circles are through-holes which accommodate additional components as needed. The circle near the middle made by VDD and VSS surrounds the 52 probe array that will touch-down on the T3-IC.

IV. CONCLUSION

As of the end of July 1997, the TORCH 3 system lacks only the T3-IC and the interface probe card, which are both in fabrication and due the week of August 8. The TORCH 3 software was tested for complete operation the last week in July using an oscilloscope, a logic analyzer, two packaged FETs, a capacitor, and the TORCH 3 system minus T3-IC and the Probe card. The test confirms correct operation and software optimization ideas have emerged, they included run time evaluation for tested parameters in software, an automatic shut off mechanism for the SMUs in the event of error, and limiting of variable to required ranges. I also recognize the need to write a users guide. The system will be completed when the other components arrive.



TORCH 3 TOP



TORCH 3 BOTTOM

The system should exceed the specification, and the software already does. It has the flexibility to be used in a variety of applications as is demonstrated by the versatility of HCI

parametric VI, it has the stress time accuracy that surpasses the existing cabinet based test system, and it has the future of runtime data reduction that the existing system has not employed. The software goes beyond the specified proof of principal quota, and begins to look and perform like a fully developed application. A good performance of the T3-IC gives Sandia an opportunity to patent a role changing reliability test system, one where small companies and fabrication facilities can cut costs while still affirming physical reliability to their customers; one where large operations and researcher can test the effects of AC stresses; and one where designers and researchers can conduct test confirming or disproving their beliefs about how environments, packaging methods and fabrication processes affect the physical reliability and lifetime of CMOS integrated circuits.

This summer internship brought me into a field I may have never chosen for myself, and it has challenged me to master a problem that I would not have encountered anywhere else. The intensity of my particular situation did not lend itself to much inattention, so that I fulfilled only the bare minimum of the S&TO calendar. Daily attention and focused pursuit overwhelmed the lofty formulation and theoretical development that I originally anticipated, but I understand the need to apprehend the latter. This is, perhaps, a critical lesson in electrical engineering. I hope for the sake of my group, my family, myself, and for S&TO that the work I performed this summer numbers among the useful contributions.

REFERENCES

[1] M.R. Bowels et al., "TORCH-3 System and Design Specification, Rev A" 1997, pp. 1-5

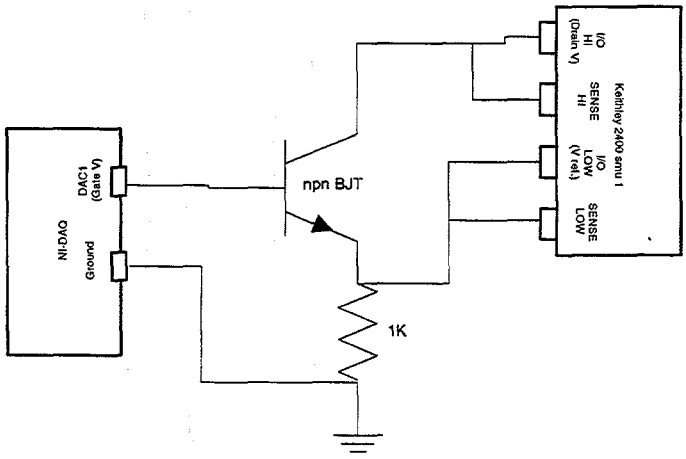
[2] Sandia Corporation, "WLR Introduction to HCI", SWORD: Sandia Wafer-Level-Reliability Software for HP 4062UX Parametric Test Systems, Ver. 2.00, copyright Sandia Corporation, 1993- 1996, pp. 5 of 10 - 9 of 10.

[3] Sandia Corporation, "WLR Introduction to Oxide Integrity", SWORD: Sandia Wafer-Level- Reliability Software for HP 4062UX Parametric Test Systems, Ver. 2.00, copyright Sandia Corporation, 1993-1996, pp. 4 of 6 - 6 of 6.

[4] A. S. Sedra and K.C. Smith, Microelectronic Circuits, 3rd-ed., Saunders Collage Publishing, 1991, pp. 312-315

HCI Parametric Demonstration on an npn BJT.

The following printouts are the front panels of Vg_Curve.vi and Id_vs_Vd.vi respectively. The setting on the panels are the ones used to create the curves in the plot window. A Bipolar Junction Transistor is the tested device, and the following connections are used and shown in the diagram below: The drain voltage from the SMU is connected to the BJT's collector, the BJT emitter/resistor node is the SMU reference node, and the gate voltage from the NI-DAQ connects to the BJT's base.



By observation of the Id-vg curves, (first panel), one notices that the threshold voltage of this BJT is about 0.7 V, and the maximum transconductance at Vd (Vce)=0.5V is 0.1025 amps/volt (the "Max Slope). From the second panel, one observes that the saturation region ends and the active region begins between 0.3 and 0.4 drain (Vce) volts for these Gate (Vbe) voltages. The curves produced here are similar to the ones that the T3-IC FETs will produce.