SEU CHARACTERIZATION OF A HARDENED CMOS 64K AND 256K SRAM*

SAND--89-0478C

DE90 000845

F. W. Sexton, J. S. Fu
R. A. Kohler**, and R. Kogas***

Sandia National Laboratories
Albuquerque, NM 87185

Abstract

The first single-event-upset (SEU) tests of the AT&T 64K and 256K SRAMs have been performed. Feedback resistor values for these parts ranged from 200kΩ to 1MΩ. All were fabricated using the 1-μm 2-level poly, 2-level metal process. Ions used for these tests were Ar, Cu, Kr, and Xe providing a range of effective LET values from 20 to 129 MeV-cm²/mg. With the 64K SRAM operating at 4.5 volts and 90°C, an upset threshold LET of 30 MeV-cm²/mg and saturation cross-section of 1.5 x 10^{-2} cm² were measured with a nominal room temperature feedback resistance of 450kΩ. In Adam's 10% worst-case environment using the Petersen approximation, this implies an error rate of 1.3 x 10^{-7} errors per bit-day. With a nominal 650kΩ feedback resistance, a 256K SRAM had a calculated error rate of about 3 x 10^{-8} errors per bit-day at 4.5 volts and 90°C. This data agrees well with earlier data for a 1K-bit test chip. The minimal feedback resistance required to prevent upset vs. LET is calculated by assuming an activation energy of 0.10 eV to estimate the decrease in feedback resistor value as a function of temperature.

Introduction

Single-event upsets have been a concern for integrated circuits used in space environments since 1975 when Binder, Smith, and Holman showed that galactic cosmic rays could explain the anomalous upsets observed in J-K flip-flops used in communications satellites [1]. Since that time, a large body of work has been done to characterize the physics of charge collection after a heavy-ion strike and the effects of collected charge on circuit performance [2]. As memory cell size shrinks, the probability that a heavy ion will intersect a critical node decreases. However, as shown by Fu et.al [3], this is offset by the smaller critical charge required to upset a logic node. The result is an increase in error-rate as geometries are scaled down. Since the trend for integrated circuits (ICs) in space systems is toward smaller geometries and more complex circuits, the SEU vulnerability of these circuits is an important consideration for system reliablity.

Recently, Lee et.al [4] described a 1-μm 2-level metal CMOS technology that was hard to 10 Mrad(Si) total dose at 500 rad(Si)/s dose rate. This technology is characterized by a twin-tub process on N/N+ epitaxial silicon. The field and gate oxides are intentionally hardened to total dose using special processing. Feedback resistors to harden against SEU are formed in second-level polysilicon. A 16K SRAM with 2-μm geometries was fabricated in the 1-μm technology. All structures and diffusions were representative of the 1-μm technology. SEU tests of this part showed an increase in threshold LET. As the memory cell size was scaled down, however, the SEU vulnerability increased [3]. This was caused by a combination of decreased restoring drive as the n-channel transistors were downsized, and decreased decoupling time as storage node capacitance decreased. Both of these effects increase SEU vulnerability. Last year, Kushner et.al [5] described the design architecture, process details, and performance margins as a function of supply voltage of a 256K SRAM in this technology. The memory cell is a 6-transistor design and has an area of 277 μm². Total dose tests at a dose rate of 500 rad(Si)/s to 1 Mrad(Si) showed that read access time changed by less than 1 ns and power supply leakage current increased from 25μA to 110 μA.

In this work we present the first complete characterization of 64K and 256K SRAMs fabricated in the 1-μm technology as a function of feedback resistance and temperature from 25°C to 90°C. Both of these parts rely on an identical memory cell design. The error rate was determined as a function of resistor value and temperature. Implications for the acceptable upper and lower limits of the feedback resistance to achieve desired SEU immunity are discussed. We compare these results to earlier measurements of the SEU vulnerability of this memory cell design made using a 1K-bit test chip, the TC-17 [3]. Errors caused by heavy ion strikes in peripheral circuitry are discussed. Since this circuitry may have a different sensitivity to heavy ion strikes than the memory, it

* This work supported by the Defense Nuclear Agency and the U.S. Department of Energy under contract DE-AC04-76DP00789.
** AT&T Bell Laboratories, Allentown, PA
*** Aerospace Corp., Los Angeles, CA

---

is important to characterize it as well. Finally, we present results which show a dependence of error cross-section on the ion species used in the SEU test.

Experimental Details

In this study we used ion beams of argon, copper, krypton, and xenon at the Lawrence Berkeley Laboratory 88-inch cyclotron. The energies and zero-angle LETs for these ions are shown in Table 1. Effective LET was varied by changing the angle of the device-under-test (DUT) relative to the ion beam. Ion fluence was measured using a scintillator and photomultiplier tube. In a typical test, parts were exposed until 100 errors were measured, or the exposure fluence reached about 20 x 10^6 particles per cm^2. This results in an uncertainty in the measured error rate of about 10%. Ion stopping power was measured with silicon surface barrier detectors. Fluence was known to ± 1 %, while ion energy was known to ± 2 %. The experimental setup and technique have been presented earlier [6]. Part temperature was increased above ambient using a resistive heater between the DUT and the socket. Part temperature was measured using a thermistor to ± 1 °C resolution. Power supply voltage was measured directly at the DUT to eliminate uncertainty in voltage caused by IR drops along cabling.

TABLE 1

Ion	Energy (Mev)	LET_0 (Mev-cm^2/mg)
Argon	175	15
Copper	283	30
Krypton	360	40
Xenon	575	63

TABLE 2

Part Type	Wafer Lot	Serial Number	Nominal R_{fb} (25°C)
64K	28217	20-7,14	200kΩ
64K	28071	09-16,6	450kΩ
64K	28217	20-9,11	1 MΩ
256K	29865	RK 1-05	650kΩ

Three 64K and one 256K SRAMs were tested for single event upset error cross-section. The wafer lot, serial number, and feedback resistance of each part are listed in Table 2. For the 64k SRAMs R_{fb} ranged from 200kΩ to 1 MΩ, while the feedback resistance of the 256K SRAM was 650kΩ. The feedback resistance for each part was inferred from a combination of test structure measurements on the wafer and from measurements of write time on the actual IC. There is some ambiguity in the actual resistance values for parts numbered 20-7,14 and 20-9,11 due to a large variation in resistance across the wafer from which these parts came.[1]

Results

Cross-section vs. LET curves for a 64K SRAM are shown in Figure 1 under dynamic operating mode (solid curves) as a function of temperature. Nominal feedback resistance is 450 kΩ when measured at 25°C. As the temperature increases from 25°C to 90°C, the threshold LET decreases from roughly 60 to about 30 MeV-cm^2/mg. This is a result of two effects. First, as temperature increases the polysilicon feedback resistance decreases due to the negative temperature coefficient of resistance for lightly doped polysilicon [7]. With a 0.10 eV activation energy, a 450 kΩ feedback resistor will drop to ~ 225 kΩ at 90° C. The decoupling time [3] is therefore halved for a voltage transient from the struck node to the unstruck node of a memory cell. Second, as temperature increases channel mobility decreases causing the restoring transistor drive to decrease by ~ 15 %. As a result, the recovery time at the struck node of a memory cell is increased. Both of these effects lower the threshold LET. At 90°C, the cross-section saturates at 1.5 x 10^{-2} cm^2. At 50° and 70°C saturation was not reached before an LET of 120 MeV-cm^2/mg. We would expect the saturation cross-section to be independent of temperature since it should equal the total sensitive area of the design. In a companion paper [8] the dependence of saturation cross-section on temperature is related to variation in feedback resistance across the memory array. The reader is referred to this paper for further discussion.

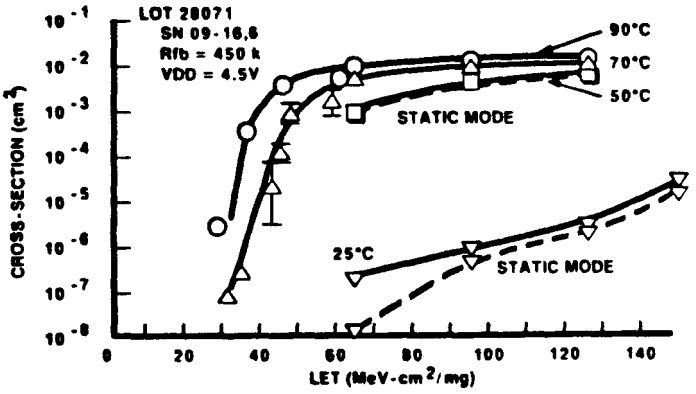

Fig. 1: Error cross-section vs LET as a function of temperature during irradiation for a 64K SRAM at 4.5 volts and 450 kΩ feedback resistance (measured at 25 °C). Nominal clock frequency during tests is 540 ns, while in static mode the clock input was held low during exposure.

1. A large variation in feedback resistance was observed on wafer 20 due to a variation in the polysilicon implant dose. Although we exploit this variation to determine dependence of LET threshold on feedback resistance, this is not representative of normal processing.

The shape of the 25°C curve shown in Figure 1 is much different from the higher temperature curves. Moreover, at 25°C the dependence of error cross-section on input clock rate is significantly different from that observed at higher temperatures. In one set of tests the SRAM was written to a known state and then held in a static bias condition (input clock signal was held at V_{SS}) during irradiation, as opposed to operating the part with a 540 ns input clock. The cross-section curves for static bias tests are shown as dashed curves in Figure 1. More than an order of magnitude difference in cross-section is seen between the static and dynamic operating conditions at room temperature with xenon at normal incidence (63.3 MeV-cm²/mg). As LET increases the cross-section curve in static mode approaches the curve in dynamic mode. At 50°C comparing the solid and dashed lines, no difference is seen between the clocked and static modes.

The response of a 256K SRAM with a feedback resistance of 650 kΩ is shown in Figure 2. At 4.5 volts and 25°C, a saturation cross-section of ~2 x 10^{-6} cm² was measured. Threshold LET was ~60 MeV-cm²/mg. No errors were measured in a static mode bias. (The upper limit in this case is calculated assuming one error at the measured fluence.) As temperature increased the LET threshold shifted to lower LET and saturation cross-section increased. At 90°C, the threshold LET was about 30 MeV-cm²/mg and the saturation cross-section was 7 x 10^{-2} cm², consistent with the expected sensitive area of this design (about four times the saturation cross-section of the 64K SRAM). The saturation cross-section showed the same qualitative dependence on temperature above 50°C as seen for the 64K SRAM in Figure 1.

SEU data for 64K and 256K SRAMs with different values of feedback resistance are compared in Figure 3 at 90° C. At 90°C, the

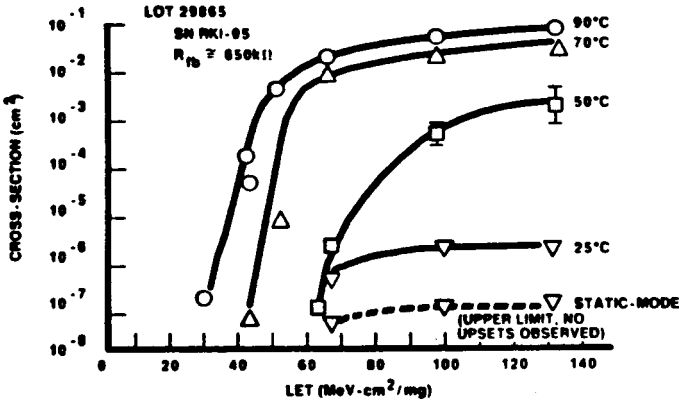

Fig. 2: Error cross-section vs LET as a function of temperature during irradiation for a 256K SRAM at 4.5 volts and 650 kΩ feedback resistance (measured at 25°C). The error cross-section in static mode at 25°C is an upper limit to the true cross-section, since no errors were detected.

threshold LET for the 200kΩ part is 20 MeV-cm²/mg, for the 450 kΩ part is 30 MeV-cm²/mg, and for the 650 kΩ part is 30 MeV-cm²/mg. Part SN 20-9,11 had a nominal R_{fb} of 1 MΩ. Cross-section values below 1 x 10^{-6} cm² were seen for this part at lower temperature indicating that for this R_{fb} the memory is effectively protected from upset up to 60 MeV-cm²/mg. Saturation cross-sections for the 64K and 256K SRAMs differ by a factor of four, as discussed earlier.

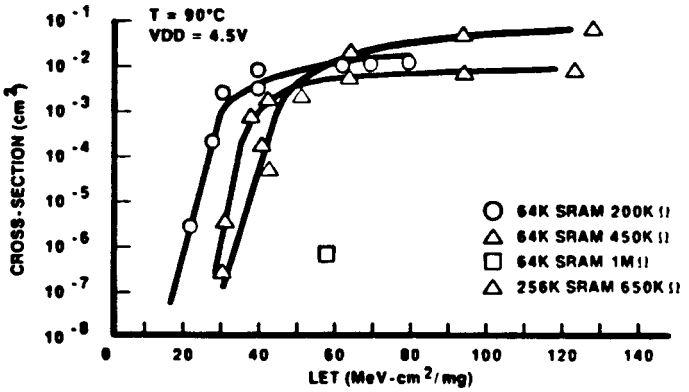

Fig. 3: Error cross-section vs LET at 90°C for 64K and 256K SRAMs as a function of feedback resistance.

The minimum feedback resistance required to prevent upset is shown in Figure 4 as a function of LET for both the 64K and 256K SRAM designs. This curve is obtained from minimal LET data taken from parts tested at different temperatures. For this curve, the polysilicon feedback resistance at test temperature is calculated[2] assuming an activation energy of 0.1 eV [9]. The drive of the "on" transistor at a struck node is also temperature dependent and, in the exact treatment, should be considered in the minimal LET calculation [10]. However, in this technology the saturated transistor drives at 90°C decrease only 10-15% from their value at 25°C [11]. Therefore, neglecting the temperature dependence of transistor drive is an acceptable approximation. The dependence of threshold LET on feedback resistance which we show here compares favorably with earlier data for the TC-17 test chip [3], shown as the horizontal bars in Figure 4. The TC-17 test chip is a 1K memory with the same memory cell design as the 64K and 256K SRAMs. The solid line is merely an aid to the eye.

The dependence of error rate on temperature and feedback resistor value at room temperature is shown in Figure 5. The error rate shown here was calculated using the Petersen formula for Adam's 10% worst case environment [12], which

2. The activation energy for the temperature coefficient of resistance for polysilicon feedback resistors depends on several process dependent parameters, including doping level. The actual value varies from 0.08 to 0.12 eV for these films, and 0.10 is an average.

approximates the error rate as

$$R = 5 \times 10^{-10} \frac{\sigma_L}{L_c^2}$$

where σ_L is the saturation cross-section in μm^2 and L_c is the threshold LET in $pC/\mu m$. This error rate is only a figure of merit, but is still valuable when used for part to part comparisons. For threshold LETs above 30 MeV-cm²/mg, this figure of merit can be as much as two or three orders of magnitude high estimated error rate. A better estimate could be made using an error rate code such as CREME or CRUM. We point out that with this figure of merit the error rate at 90° C and with 450 kΩ resistance is ~ 1 x 10^{-7} errors-per-bit-day. This meets the original program goals for this part. As resistance increases, the error rate decreases as expected. Also, as resistance increases the dependence on temperature increases, as seen by the increasing slope of the lines going from 200kΩ to 600kΩ. This is due to the increasing temperature coefficient of resistance as doping decreases for polysilicon films [7].

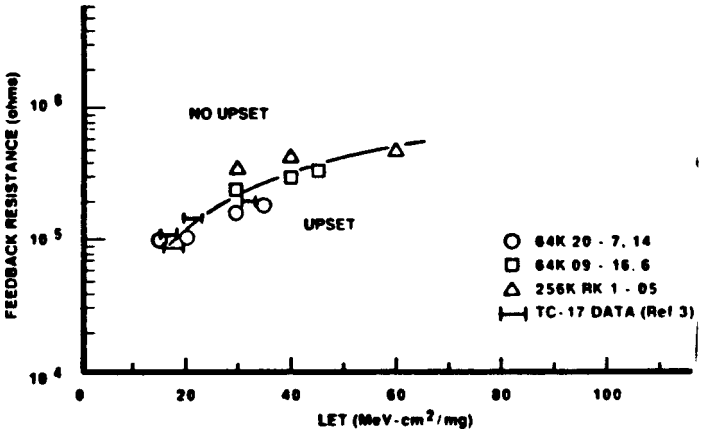

Fig. 4: Minimal feedback resistance required to prevent upset vs LET. The horizontal bars are data from a 1K-bit test chip (ref. 3). The solid line is an aid to the eye.

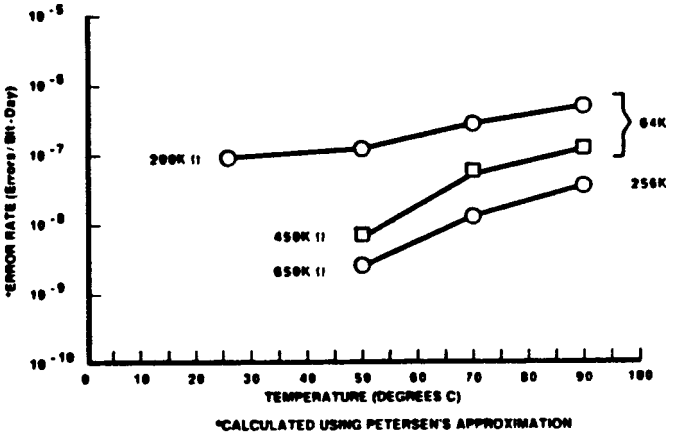

Fig. 5: Error rate vs. temperature in Adam's 10% worst-case environment as a function of feedback resistance at room temperature. Error rates were calculated using the Petersen approximation.

The dependence of measured error cross-section on ion species is shown in Figure 6 for a 256K SRAM (RK 1-05) at 90°C, using Cu, Kr, and Xe ion beams. For copper ions, the measured error cross-section increases from 4.5 x 10^{-5} for the ion beam at an angle of 0° relative to the part to 5.3 x 10^{-3} cm² at 60°. For Kr ions, the measured cross-section increases from 2 x 10^{-4} cm² at normal incidence to 2.5 x 10^{-2} cm² at 60°. The measured cross-section increases from 3.2 x 10^{-2} to 8.5 x 10^{-2} cm² as angle was increased from 0° to 60° with Xe ions. If the normal $1/\cos\theta$ correction for effective LET is valid we would expect the curves to overlap from one ion species to the next as effective LET increases. In this data, as the mass of the ion increases the measured cross-section vs LET curve shifts to lower LET, indicating that more charge is collected as the ion mass increases. Referring to Figure 6 at an LET of 60 MeV-cm²/mg, this results in a factor of two difference between the cross-section measured with Cu and Kr, while at an LET of 80 MeV-cm²/mg a difference of 1.6 was observed between Kr and Xe ions. In these tests, we took great care to eliminate any possibility of shadowing the ion beam with the package at high angles.

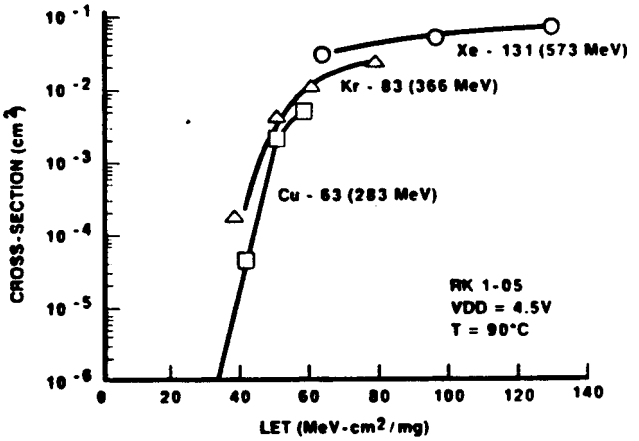

Fig. 6: Dependence of measured cross-section on ion species during exposure. The leftward shift of the cross-section curves as ion mass increases indicates that more charge is collected from a strike by a heavier ion.

Discussion

The shape of the error cross-section curves at 25°C and the dependence of cross-section on clocking mode can be explained if we consider the effect of errors in peripheral circuitry on these SRAM designs. In a clocked mode the measured upset rate is a combination of memory and control circuit upsets. In a static mode only memory upsets occur since the control circuitry is vulnerable for a very short fixed length of time after a clock edge. The upset rate due to memory hits alone is shown as the dash-dot line connecting the squares in Figure 7. If this is subtracted from the total observed error cross-section (solid line), the error

cross-section due to control circuit hits can be estimated. The dashed line in Figure 7 results. This implies that control circuit hits account for ~1 x 10^{-6} cm^2 in the measured cross-section with a threshold LET of less than 60 MeV-cm^2/mg. This is consistent with bit line upsets[3] (which include the pass transistor drains and sense amp circuitry) which are expected to have a saturation cross-section of about 9 x 10^{-7} cm^2 and a threshold LET of about 60 MeV-cm^2/mg. As temperature is raised to 50°C, there is no difference in cross-section between static and dynamic operation. Since the saturation cross-section is four orders of magnitude higher for memory upset than circuit upset, the measured error rate is dominated by memory hits which have become more susceptible to upset due to the lower feedback resistance at this temperature. In the 256K SRAM at 25°C, the measured upsets are due entirely to peripheral circuit hits, since no errors were measured in a static mode bias. The saturation cross-section of 2 x 10^{-6} cm^2 for peripheral circuit hits measured here is twice the magnitude measured for circuit hits in the 64K SRAM in the above discussion. In the 256K SRAM design, the number of rows were doubled over that in the 64K SRAM design. Based on this difference, a factor of two difference in peripheral circuitry sensitive area is exactly what we would expect.

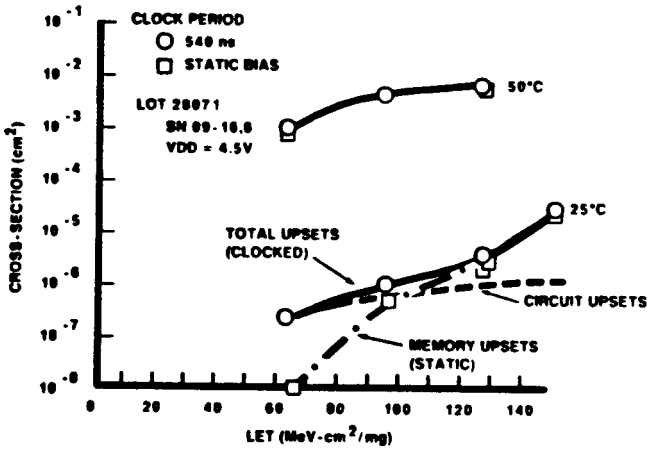

Fig. 7: Separation of errors in peripheral circuitry from memory errors. The circuit upsets are derived from the total upsets measured in a clocked mode minus the upsets measured in a static mode.

The dependence of error cross-section on ion species shown in Figure 6 cannot be explained in terms of geometry effects. In SEU tests, both the measured error cross-section and the LET are corrected by $1/\cos\theta$. As the areal dimension of sensitive regions (for this discussion this includes the depletion regions of vulnerable junctions) become small relative to their thickness, edge effects become increasingly important and the $1/\cos\theta$ correction must be adjusted. In Figure 8 we illustrate the case where additional charge is collected by those ion tracks that penetrate the sensitive volume below the surface as the angle of incidence increases. Funneling will cause charge to be collected from any strike that penetrates the sensitive volume [13-16]. We assume that the shape of the sensitive volume is a rectangular parallelpiped. Assuming a linear ion track, the collection volume is defined by the funnel depth as well as the sensitive volume as shown in Figure 8. In fact, funneling can occur for near misses if they are close enough to the sensitive volume such that the electron-hole plasma density is large relative to the background doping by the time the plasma has spread to the edge of the depletion region. In this simple model we include only strikes that penetrate the sensitive volume and neglect near misses. With this in mind, the projection of the actual area intercepted by the ion track increases by z $\sin\theta$ where z is the depth of the depletion region. If this additional area is considered, the error rate is corrected by

$$\sigma_0 = \sigma_m \left(\cos\theta + \frac{z}{x} \sin\theta \right)^{-1}$$

where σ_m is the measured error cross-section, σ_0 is the error cross-section at normal incidence, θ is the angle of incidence relative to the surface normal, and x and z are the width and depth of the sensitive volume, respectively. This results in up to 20% downward correction of the measured cross-section at 60°, making the difference due to ion species seen in Figure 6 even greater.

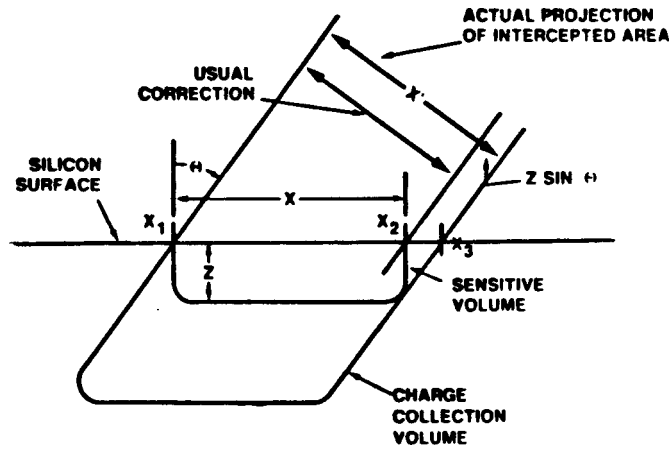

Fig. 8: Illustration of correction to error cross-section due to edge effects. The charge collection volume is defined by the funnel depth of any strike which penetrates the sensitive volume. The sensitive volume is the region defined by the junction plus depletion region.

3. The capacitance of the bit lines is estimated to be about 6 pF. Assuming that the sense amps can detect a difference of 200 mV the critical charge for upset would be about 1.2 pC. If charge is collected from a depth of 2-μm, a threshold LET of 60 MeV-cm^2/mg results. The total sensitive area of this circuitry is 5000 μm^2. Because this circuitry is vulnerable only 10 ns per cycle, at a 540 ns clock period the expected saturation cross-section is 9 x 10^{-7} cm^2.

A dependence of error cross-section on ion species has been observed by researchers in the past [17-20]. The data presented here again raises questions about the validity of the concept of effective LET. Stapor et.al [20] attributed a dependence on ion species to a difference in plasma densities along the ion track depending on the incident ion. They presented calculations which showed that as the mass of the incident ion increased the cross sectional area of the plasma path increases, resulting in a lower plasma density and decreased charge recombination. This effectively raises the amount of charge collected along the ion track, and shifts the threshold LET to lower values. This effect is in the correct direction to explain the results of Figure 6.

This result has important implications since the estimation of the error rate of an integrated circuit in space environments depends on an accurate measurement of the error cross-section vs LET. However, in most tests to characterize the single event upset sensitivity, only a limited range of ions and energies are available to simulate a strike by a heavy ion in the actual space environment. In practice, the effective LET of an incident ion is changed by varying the angle of incidence of the ion beam used in the test, and the effective LET of the incident particle is then calculated using the LET at zero angle of incidence from Ziegler's curves [21] for example, and increased by $1/\cos\theta$. The dependence on ion mass observed here may result in an underestimation of the error rate in the actual use-environment. Using simulations to predict the ion track cross-section, it may be possible to correct for the ion species used in SEU tests and arrive at a better estimate for the error cross-section. This will require 3-D simulations and improved modeling of the interaction of the ion with silicon. We have found in more recent tests that this effect may depend on subtle experimental conditions. Further work in this area is warranted.

Finally, the fact that the cross-sections saturated at 1.6×10^{-2} cm^2 for the 64K SRAM and about 7×10^{-2} cm^2 for the 256K SRAM at 90°C indicates that both the p- and n-drains regions are contributing to upsets. Earlier studies of a 16K SRAM indicated that the n-off drain regions would not be sensitive with resistance values above 50kΩ [22]. This more recent data implies that RAM designs in the 1.25 micron AT&T technology have a higher n-drain sensitivity than the earlier 2-μm technology. This will impact the possible advantage we might expect from novel designs using an L-RAM memory cell [22], for example. This may also indicate a limit to the effectiveness of these approaches in bulk silicon.

Conclusions

We have examined the effects of heavy ion strikes on AT&T radiation-hardened 1-μm 64K and 256K SRAMs. Key parameters in this study were temperature during irradiation, the magnitude of feedback resistance in the 6-transistor memory cells, clock frequency, and ion species. We found that as temperature increased from 25° to 90° C, the threshold LET decreased to 30 MeV-cm^2/mg for a 450 kΩ feedback resistance. This is caused by the negative temperature coefficient of resistance for lightly doped polysilicon resistors. We determined the minimum feedback resistance required to prevent upset as a function of LET. This data compared favorably with earlier data for a 1K SRAM test chip. Upsets in peripheral circuitry (bit line and sense amp circuitry) were observed by comparing the error rate with the part operated in a static versus a clocked mode. The threshold LET for these upsets was less than 60 MeV-cm^2/mg and the saturation cross-section was 1×10^{-6} and 2×10^{-6} cm^2 for the 64K and 256K SRAMs, respectively. We observed a dependence of measured error cross-section on ion species: as ion mass increased the measured error rate increased. This effect, which has been observed by other researchers, can be explained by a dependence of the plasma density along the ion track on ion mass. If the average plasma density decreases with increasing ion mass, recombination will also decrease. Increasing current with increasing ion mass results.

Acknowledgements:

We are indebted to P. S. Winokur for his support of this work, C. L. Axness and P. V. Dressendorfer for many helpful discussions, and W. T. Corbett for a critical review of this manuscript.

References

1. D. Binder, E. C. Smith, and A. B. Holman, "Satellite Anomalies from Galactic Cosmic Rays," IEEE Trans Nucl. Sci., NS-22, no 6, pp. 2675-2680 (Dec. 1975).
2. See for example the "Special Section on Space Radiation Effects on Microelectronics," ed. S. E. Kerns and K. F. Galloway, Proc. of the IEEE, vol 76, no. 11, pp 1401-1544 (Nov 1988).
3. J. S. Fu, K. H. Lee, R. Koga, F. W. Hewlett, R. Flores, R. E. Anderson, J. C. Desko, W. J. Nagy, J. A. Shimer, R. A. Kohler, and S. D. Steenwyk, "Scaling Studies of CMOS SRAM Soft-Error Tolerances -- From 16K to 256K," IEDM Tech. Digest, pp 541-543, (Dec. 1987).
4. K. H. Lee, J. C. Desko, R. A. Kohler C. W. Lawrence, W. J. Nagy, J.A. Shimer, S. D. Steenwyk, R. E. Anderson, and J. S. Fu,

"Radiation Hard 1.0-μm CMOS Technology," IEEE Trans Nucl. Sci., NS-34, no 6, pp. 1460-1463 (Dec. 1987).
5. R. A. Kushner, R. A. Kohler, S. D. Steenwyk, J. C. Desko, L. A. Alchesky, R. H. Arnold, C. A. Benevit, D. C. Clemons, D. A. Longfellow, and K. H. Lee, "Fabrication and Total-Dose Testing of a 256Kx1 RAdiation Hardened SRAM," IEEE Trans Nucl. Sci., NS-35, pp. 1667-1669 (Dec. 1988).
6. R. Koga, W. A. Kolasinski, and S. Imamoto, "Heavy Ion Induced Upsets in Semiconductor Devices," IEEE Trans Nucl. Sci., NS-32, no 1, pp. 159-162 (1985).
7. See for example: C. R. M. Grosvenor, J. Phys. C: Solid State Physics, 61, 1547 (1985) or C. H. Seager, Ann. Rev. Mater. Sci., 15, 271 (1985).
8. R. A. Kohler, R. Koga, F. W. Sexton, and J. S. Fu, "SEU Characterization of Hardened CMOS SRAMs Using Statistical Analysis of Feedback Resistor Population," to be presented at the 1989 Nuclear and Space Radiation Effects Conference, July 25-28, 1989, Marco Island, FL.
9. S. D. Steenwyck, private communication.
10. C. L. Axness, H. T. Weaver, J. S. Fu, R. Koga, and W. A. Kolasinski, "Mechanisms Leading to Single Event Upset," IEEE Trans Nucl. Sci., NS-33, pp. 1577-1580 (1986).
11. T. F. Wunsch, Sandia National Laboratories, Div 2115, private communication.
12. E. L. Petersen, J. B. Langworthy, and S. E. Diehl, "Suggested Single Event Upset Figure of Merit," IEEE Trans Nucl. Sci., NS-30, pp. 4533-4539, (Dec. 1983).
13. F. B. McLean and T. R. Oldham, "Charge Funneling in N- and P-type Si Substrates," IEEE Trans Nucl. Sci., NS-29, no. 6, pp. 2018-2023 (1982).
14. T. R. Oldham, F. B. McLean, and J. M Hartman, "Revised Funnel Calculations for Heavy Particles with High dE/dx," IEEE Trans Nucl. Sci., NS-33, no. 6, pp. 1646-1650 (1986).
15. C-M. Hsiegh, P. C. Murley, and R. R. O'Brien, "Collection of Charge from Alpha-Particle Tracks in Silicon Devices," IEEE Trans on Elec. Dev., ED-30, no. 6, pp. 687-693 (1983). funneling
16. H. L. Grubin, J. P. Kreskovshy, and B. C. Weinberg, "Numerical Studies of Charge Collection and Funneling in Silicon Devices," IEEE Trans on Nucl. Sci., NS-31, no. 6, pp. 1161-1166 (1984).
17. W. A. Kolasinski, 1986 SEU Symposium, Los Angeles, CA
18. T. L. Criswell, D. L. Oberg, J. L. Wert, P. R. Measel, and W. E. Wilson, "Measurement of SEU Thresholds and Cross Sections at Fixed Incidence Angles," IEEE Trans on Nucl. Sci., NS-34, no. 6, pp. 1316-1321 (Dec. 1987).
19. J. S. Browning, Sandia National Laboratories, Div 2321, private communication.
20. W. J. Stapor, P. T. McDonald, A. R. Knudson, and A. B. Campbell, IEEE Trans Nucl. Sci., NS-35, 1585 (Dec. 1988).
21. J. F. Ziegler, J. P. Biersack, and U. Littmark, "The Stopping Power and Range of Ions in Solids," Pergamon Press, New York, 1985.
22. H. T. Weaver, C. L. Axness, J. D. McBrayer, J. S. Browning, J. S. Fu, A. Ochoa, Jr., and R. Koga, "An SEU Tolerant Memory Cell Derived from Fundamental Studies of SEU Mechanisms in SRAM," IEEE Trans Nucl. Sci., NS-34, no. 6, pp 1281-1286 (Dec 1987).