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DEVELOPMENT OF HIGH EFFICIENCY (14%) SOLAR CELL ARRAY MODULE

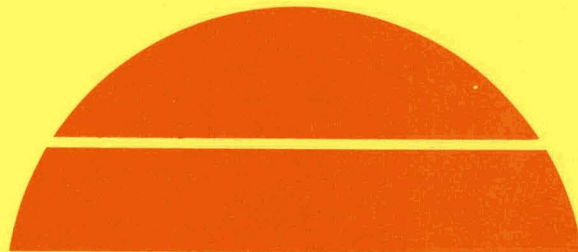
Second Quarterly Report, March 15—July 15, 1979

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MASTER

Work Performed Under Contract No. NAS-7-100-955217

Optical Coating Laboratory, Inc.
Photoelectronics Division
City of Industry, California



U.S. Department of Energy

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Solar Energy

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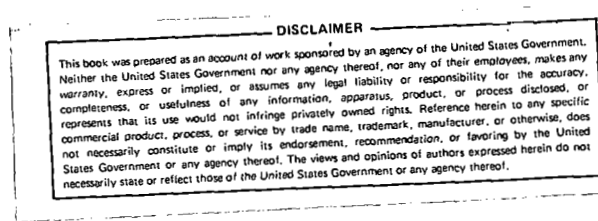
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DEVELOPMENT OF HIGH EFFICIENCY (14%)
SOLAR CELL ARRAY MODULE

SECOND QUARTERLY REPORT

FOR PERIOD COVERING

15 March 1979 to 15 July 1979

By

P.A. ILES, S. KHEMTHONG, S. OLAH,
W.J. SAMPSON, AND K.S. LING

JPL CONTRACT NO. 955217

OPTICAL COATING LABORATORY, INC.
PHOTOELECTRONICS DIVISION
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"The JPL Low-Cost Silicon Solar Array Project is sponsored by the U. S. Department of Energy and forms part of the Solar Photovoltaic Conversion Program to initiate a major effect toward the development of low-cost solar arrays. This work was performed for the Jet Propulsion Laboratory, California Institute of Technology by agreement between NASA and DOE."

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ABSTRACT

Considerable amount was expended in the development of large area, high efficiency P/N solar cells. The best performance achieved to-date on 3" diameter cells is 15.6% at AM1 and 28°C. Factors contributing toward the poor performance have not been identified and isolated. Work is continuing.

Minor modifications have been incorporated in the modular design. The 120 cells will be connected 8 in parallel and 15 in series to enhance the reliability of the modules. As a result of the changes, two junction boxes will be required as the P and N terminals will come out from the opposite sides of the module.

Designs for back contact soldering machine, vacuum pick-up, AR coating tooling, and test fixture have been completed. Fabrication of tooling has begun.

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1.0 INTRODUCTION

The initial phase of this program is to design and develop 3" diameter, P/N solar cells with the conversion efficiency of 16.5% or better at AM1 and 28°C. Upon completion of the cell development phase, OCLI is to design, fabricate, and deliver six (6) high efficiency modules, approximately 2' x 4', with a minimum output of 90 watts at AM1 and 28°C and with the design goal of 14% overall efficiency.

The second phase of this program is to design and fabricate production tooling for the manufacture of the high efficiency cells and modules. Twenty (20) verification modules are to be fabricated and delivered to JPL.

2.0 TECHNICAL DISCUSSION

Considerable amount of effort has been devoted to the development of high efficiency P/N solar cells. To-date the main causes contributing toward lower power output than that of N/P cells has not yet been identified or isolated. Work is continuing. Minor modifications have been made to the module design. Design of the tooling to be used specifically for this module and the center contact solar cells has been completed.

2.1 Comments on P/N Cell Development

In the previous quarterly report, some promising cells were reported, some with the required efficiency ($>16\%$ AM1). However, most of the high output cells were 4 cm^2 area, whereas simultaneous trials applying the same process steps to 3" diameter wafers (45 cm^2 area) did not

give the same efficiency. The repeat series of tests wherein the "best procedure" was repeated using both Czochralski and float-zoned silicon gave similar results, with reduced performance from 45 cm² cells.

A small part of this different behavior for larger sizes could be ascribed to the theoretically lower CFF (0.75) for the grid pattern used, compared to a CFF 0.77 for the smaller area cells. This difference arises in resistive losses in the grid patterns. However, this CFF decrease could not explain the major losses in power for the larger P/N cells.

Because the process steps appeared satisfactory as shown by the reasonable yield of good 4 cm² cells, the problem was re-examined to see if adverse interactions in the process steps could be responsible, or perhaps differences in a given process when larger slices were used. (Previous work on high efficiency P/N cells had generally been reported for cells <4 cm² area.)

Figure 1 repeats the process sequence given in the previous report.

In this sequence several steps can be identified as sensitive to the slice size.

The quality of the diffusion mask used in Steps 3 or 5 could vary, with adverse effects. For example if diffusants leak through the mask in small areas, some loss in CFF or V_{OC} could result. For the large area slices the masking process could be less effective (and in addition, the probability of failure is increased). Below a test of this hypothesis is described.

FLOW CHART

HIGH EFFICIENCY P+ N N+ CELLS

1. Grow Ingot, N-Type, 7-14 ohm-cm.
2. Prepare Wafers.
3. Apply Diffusion Mask to Front.
4. Diffuse N+ on Back to Form Back Surface Field.
5. Apply Diffusion Mask to Back.
6. Diffuse P+ to Form Junction.
7. Evaporate Back Contact (Al, Ti-Pd-Ag).
8. Apply Front Contact Mask (Photoresist).
9. Evaporate Front Contact (Ti-Pd-Ag).
10. Evaporate AR Coating.
11. Sinter.
12. Electrical Test.

FIGURE 1

Step 6, the boron diffusion used to form the shallow P+ layer involves as a source, boron nitride disks held close to the silicon in a quartz boat. This boat has retaining slots, and these can lead to small areas around the large slice perimeter which are less likely to receive full boron supply. These areas are removed when 4 cm² cells are made, but are still present on the 45 cm² cells. The cutting experiment described below is intended to show if these edge areas are a problem.

In addition, analysis of the cell losses (in I_{SC} , V_{OC} or CFF) has led to closer scrutiny of some of the processes used.

Some cells show good values of I_{SC} , V_{OC} but the CFF is reduced. No shunting is present, but the series resistance is high. The P+ layer is shallow (sheet resistance >150 ohm/square) but this high sheet resistance does not appear to be the main cause of reduced CFF. There are two possibilities.

(a) Step 7 applies a thin layer of aluminum to the N+ back surface. Al is used because it is a convenient way to obtain a reflecting back contact, and tests have shown that use of the Al can give 2-3% increase in I_{SC} , obtained from the additional pass of unabsorbed long wavelength photons.

This aluminum-silicon contact is not heated above 400°C, and therefore should not tend to form a Schottky rectifying barrier on the highly doped N+ layer. Nevertheless, in some cases if the N+ diffusion was not effective over the whole back surface, or if some boron has penetrated the diffusion mask over the N+ layer, the Al-N+ Si interface could add series resistance (or even decrease V_{OC} slightly).

(b) Some tests have shown that even after careful cleaning, there is a thin transparent layer on the surface of the P+ silicon after boron diffusion. This layer can reduce the AR coating gain and in addition could add series resistance to the cell.

Both (a) and (b) are affected by the sinter steps used; it is clear, however, that high sinter temperatures are not desirable, because they increase the chance of a resistive contact at the back surface or on the other face, could lead to partial penetration of the P+ layer, with increased shunting.

2.1.1 Back-Up Tests

Tests in progress to identify the problems mentioned above are described.

(a) Use of Better Diffusion Masks

Tests wherein a thicker, denser diffusion mask was used to protect the front of the N-silicon during formation of the N+ BSF layer were promising. The shunting effects decreasing CFF were removed, and V_{OC} was adequate. There was still some residual excess series resistance, and tests are in progress to see if this is caused by the thin boron-layer not being completely removed. There was some loss of I_{SC} , (reduced diffusion length from heating) but this could be corrected by somewhat reduced temperature in the masking process, and by controlled cooling after the mask is applied.

(b) Cutting Trial

This trial was designed to test the hypothesis that incomplete boron diffusion (or other effects) were occurring at the edge of large

slices. Several 45 cm^2 cells with known poor I-V curves were selected and measured, as selective reduction in cell area was achieved by carefully sawing off edge regions. The resultant cell size approached 4 cm^2 . The results of this test can be seen in Table 1. At least $1/4"$ was removed all around the edges after the second cuts were made. Even the polished cells showed improved CFF, for only one cell (B), and the resultant CFF was still inadequate. No increase in V_{OC} was observed after cutting. It appears that the shunting is not located on the periphery of the cell.

This last test included some P/N cells made with textured front surface, (as discussed in previous monthly reports) used to obtain 2-3% increase in I_{SC} . It has been shown that often textured surfaces have slightly reduced V_{OC} (predictable from the 75% larger surface area) and reduced CFF from shunting effects, so that the textured cells should be less likely to recover after cutting down in size.

2.1.2 Conclusions

The individual process steps, and their combination (and therefore any interactions) can yield satisfactory P/N cells 4 cm^2 in area, but are less successful for 45 cm^2 cells. Tests were described, aimed at reducing this area dependence. Repeat tests with intentional variations in diffusion masks are in progress, using most of the processes found successful for 4 cm^2 cells.

In addition alternate boron diffusion sources are being re-evaluated, and alternate reflecting back contacts are being tested.

TABLE 1

I-V Parameters After Two Successful Cuts
(To Remove Edge Areas)

CELL	SURFACE	START		FIRST CUT		SECOND CUT	
		V _{OC}	CFF	V _{OC}	CFF	V _{OC}	CFF
A	Textured	0.5	0.55	0.485	0.6	0.49	0.62
B	Polished	0.51	0.61	0.5	0.67	0.505	0.67
C	Textured	0.51	0.59	0.5	0.625	0.5	0.55
D	Textured	0.49	0.575	0.48	0.58	0.48	0.565
E	Polished	0.49	0.555	0.475	0.575	0.48	0.555
F	Polished	0.5	0.645	0.49	0.66	0.49	0.65

2.2 Module Design

The module design remains essentially the same as described in the first quarterly report with minor changes after the Design Review Meeting.

The detailed design is shown in Figure 1 and Figure 2 (OCLI Drawing Nos. D-202400, and D-202373, Revision B). The changes from the original design will be described in the following paragraphs.

2.2.1 Cell Interconnection

To enhance the reliability of the module, the 120 3" cells will be connected 8 in parallel and 15 in series to alleviate the hot spot problem in the event of a cell being shadowed or damaged. The cells will be cross-strapped every fifth row as shown in Figure 3 (OCLI Drawing No. D-202374, Revision B).

2.2.2 Junction Box

With the modification of cell interconnection, the positive and the negative terminals will be located at opposite ends of the module. Two junction boxes will be required as shown in Figure 1.

2.2.3 White Reflecting Surface

The original plan of applying white paint on Mylar to enhance electrical output was abandoned because no suitable white paint or adhesive could be found that would adhere to the Mylar sheet and maintain its white color after temperature cycling. Sample 36-cell modules have been fabricated using a sheet of 2 mil thick white Tedlar to replace the combination of Mylar and white paint. Mechanically, this approach eliminates one operation. Electrically, the gain after encapsulation remains the same.

2.3 Production Tooling

The design of the following tooling has been completed and modifications have been made after the Design Review. In addition to the drawings shown in this report, detailed drawings for components and subassemblies are available (see Appendix A). Fabrication of tooling has begun.

2.3.1 Back Contact Soldering Machine

The soldering machine as shown in Figure 4 (OCLI Drawing No. D-202458, Sheets 1-3) is semi-automatic. This consists of a phenolic template with 120 3" cavities which accommodate cells with mesh interconnect already soldered to the front contact. A Unitek resistance heating soldering machine mounted on two (2) 1 inch diameter metal rods is used. Indentations at 3.05" apart (3" diameter cell plus .050" spacing between cells) are provided on the rod. The soldering machine is manually moved from cell to cell, a step-repeat process. The fluxing and soldering will be done automatically, with the exception that fluxing during the soldering of the parallel strings will be done manually.

The machine is designed to solder 15 cells in series and 8 cells in parallel. The sequence of soldering is as follows:

(a) For Series Connections

Place template against stop on left with "Y" motion in the first hole. Move soldering machine to the right in "X" direction in 3.04" increments until 15 cells are solder-connected in series. Move template to the right against stop which offsets the template by 1.52" and locates

the staggered pattern of the next row. Move "Y" motion to the second hole and proceed with "X" motion to the left. Repeat above procedures until all 120 cells are soldered.

(b) For Parallel Connections

Remove dowel pin from stop on the right hand side and install the pin into the lower hole as appeared in the drawing. Move "X" and "Y" motions to their respective first hole. This will locate the first solder joint for the parallel circuit. A piece of copper mesh cut to the proper length is to be placed on the cells. Proceed to move "Y" motion into the second hole until 8 cells are connected in parallel. Move "X" motion to fifth, tenth, and fifteenth stop and repeat "Y" motion soldering.

2.3.2 Vacuum Pick-Up

To facilitate removal of the 120 cell assembly from the soldering template, a simple vacuum pick-up has been designed as shown in Figure 5 and 6 (OCLI Drawing Nos. D-202475 and D-202473). Two pieces of aluminum honeycomb, spaced 1/16" apart will be edge-sealed. One hundred and twenty (120) soft vacuum cups will be inserted into one side of the honeycomb. Each cup will be positioned over the bare contact of the cell. A vacuum valve will be installed on the opposite side. The in-house central vacuum system will be used to operate the pick-up.

2.3.3 AR Coating Tooling

The evaporator used for applying multi-layer anti-reflective coating has five (5) pie-shaped plates, each holding eleven (11) 3" cells. The

tooling is designed specifically for center contact cells as shown in Figures 7 and 8 (OCLI Drawing Nos. TDD-12333 and TDC-12333-1). Pins inserted into the mounting plate will locate accurately the positions of the cells. An epoxy fiberglass template with eleven (11) holes located at the center of each cell will be placed over the mounting plate loaded with eleven (11) cells. Hicorex permanent magnets, 1/4" in diameter, will be dropped inside the holes of the template which will then be removed. The magnets will hold the cells in place against the stainless steel mounting plate.

2.3.4 Test Fixture

The test fixture, as shown in Figure 9 (OCLI Drawing No. TAD-12331), is again designed for testing the center contact cells. Current and voltage probes, electrically isolated, will make contact to the cell. The test fixture has provisions for cooling fluid for temperature control, vacuum hold down, thermocouple, and solenoid to operate the probes. The fixture is capable of testing cells up to 5" in diameter.

3.0 MILESTONE

3.1 The program is behind schedule due to difficulty encountered in developing large area, high efficiency P/N solar cells. A request to change the scope of the contract to allow more time for cell development has been submitted to JPL.

3.1.1 The design of the module has been completed. Modifications as a result of the Design Review Meeting have been incorporated.

3.1.2 Development of high efficiency, P/N cells is continuing. Experiments have been designed to identify the cause of low performance mainly due to low curve fill factors.

3.1.3 Detailed design for the following tooling has been completed. Fabrication has begun.

(a) Back contact soldering machine

(b) Vacuum pick-up

(c) AR coating tooling

(d) Test fixture

3.2 Work Planned for the Next Reporting Period

3.2.1 Continue cell development with increased efforts.

3.2.2 Continue with tooling fabrication.

3.3 A milestone chart is attached.

Revised: 9/13/78
12/22/78

Page 1 of 2

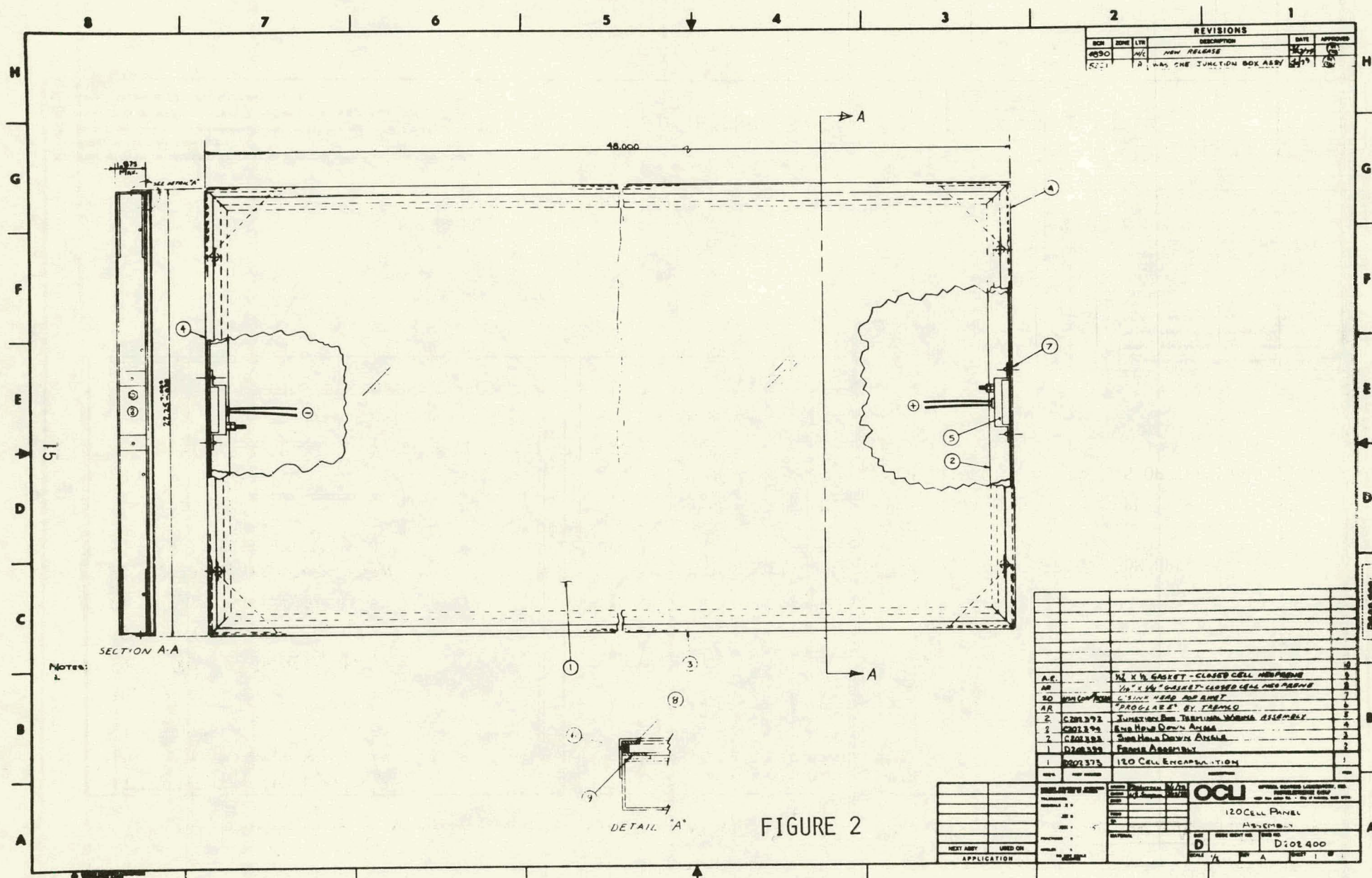
PROGRAM PLAN

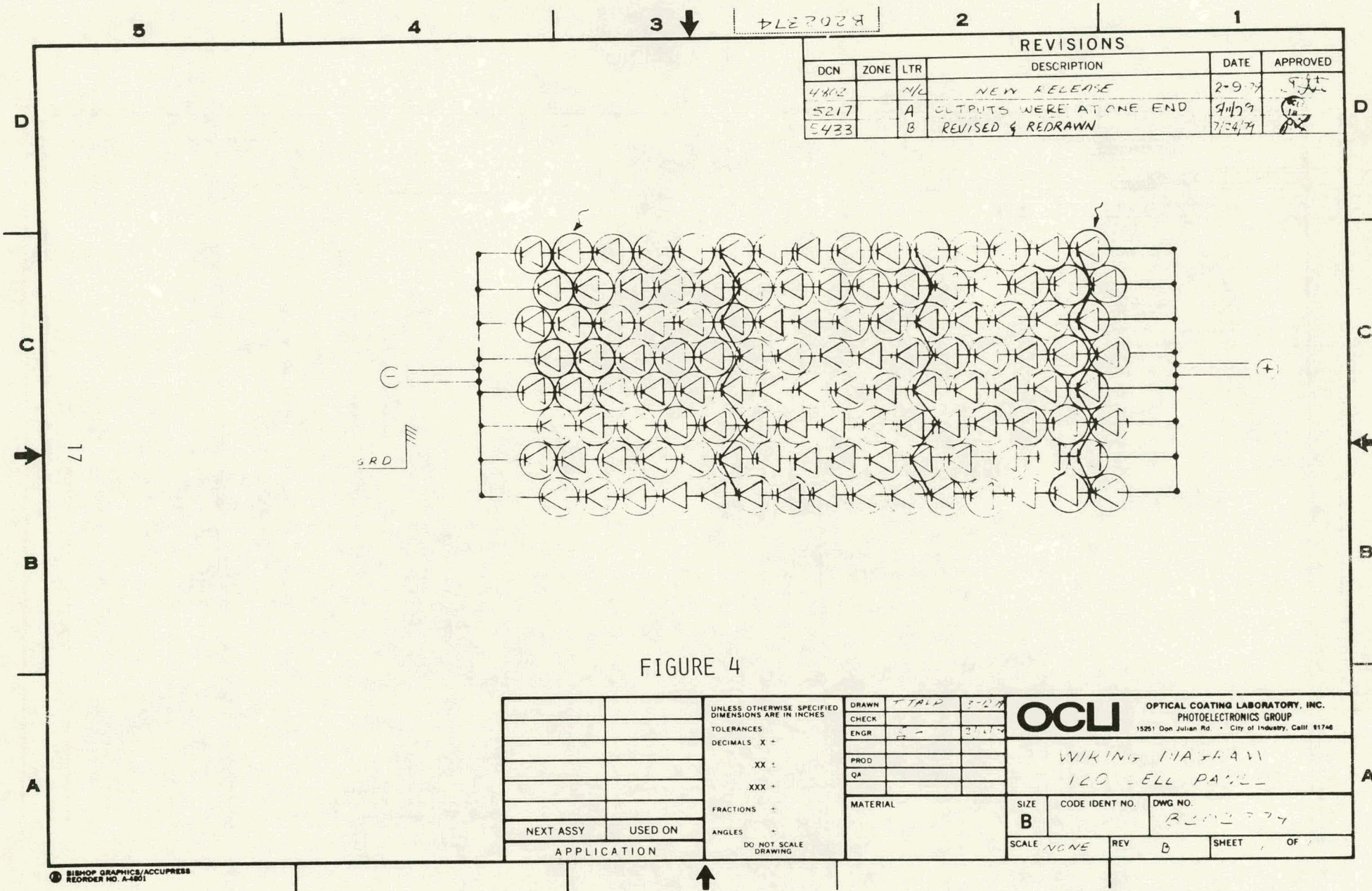
TASK	MONTH									
	DEC	JAN	FEB	MAR	APR	MAY	JUN	JUL	AUG	OCT
1. DESIGN OF HIGH EFFICIENCY SOLAR CELL										
(a) Design of Photomask	■									
Acquisition of Photomask	■									
(b) Design of AR Tooling	■									
Acquisition of AR Tooling	■									
2. DESIGN OF HIGH EFFICIENCY MODULE										
(a) Design of Interconnect	■									
Acquisition of Interconnect	■									
(b) Design of N-Contact Soldering Fixture	■									
Acquisition of N-Contact Soldering Fixture	■									
(c) Design of Module Soldering Fixture	■									
Acquisition of Module Soldering Fixture	■									
(d) Design of Module Laydown Tooling	■									
Acquisition of Module Laydown Tooling	■									
3. MODULE DESIGN REVIEW DATA PACKAGE		▲								
4. MODULE DESIGN REVIEW		▲								
5. RECEIPT OF JPL APPROVAL			▲							
6. FABRICATION AND DELIVERY OF SIX (6) MODULES										
7. TOOLING DESIGN REVIEW DATA PACKAGE					▲					
8. TOOLING DESIGN REVIEW					▲					
9. RECEIPT OF JPL APPROVAL						▲				
10. FABRICATION OF PRODUCTION TOOLING										
11. PREPARATION OF PROCESSING PROCEDURES										
12. FABRICATION OF SOLAR CELLS										
13. FABRICATION OF TWENTY (20) MODULES										
14. PRODUCTION TOOLING AND MANUFACTURING AIDS										▲

13.

PROGRAM PLAN

TASK	MONTH										
	DEC	JAN	FEB	MAR	APR	MAY	JUN	JUL	AUG	SEP	OCT
15. COST DATA FOR 5, 25, 50 kW										Δ	
16. COST DATA PER SAMICS											Δ
17. BASELINE COST ESTIMATE	▲										
18. PROGRAM PLAN	▲										
19. MONTHLY FINANCIAL REPORT	▲		▲	▲	▲	▲	▲	Δ	Δ	Δ	Δ
20. MONTHLY STATUS REPORT	▲		▲		▲	▲		Δ	Δ		
21. QUARTERLY REPORT				▲			▲			Δ	
22. INTERIM TECHNICAL REPORT	2 WEEKS AFTER RECEIPT OF R&D TESTING DATA FROM JPL										
23. FINAL TECHNICAL REPORT											
(a) Draft	2 WEEKS AFTER RECEIPT OF TESTING DATA FROM JPL										
(b) Final	30 DAYS AFTER RECEIPT OF JPL WRITTEN COMMENTS OF THE DRAFT FINAL REPORT										
24. PARTICIPATION IN TECHNICAL REVIEW ACTIVITIES											
(a) Program Review Meetings	AS REQUIRED										
(b) Program Design Review Meetings	AS REQUIRED										
(c) Project Integration Meetings	AS REQUIRED										
(d) Workshops	AS REQUIRED										





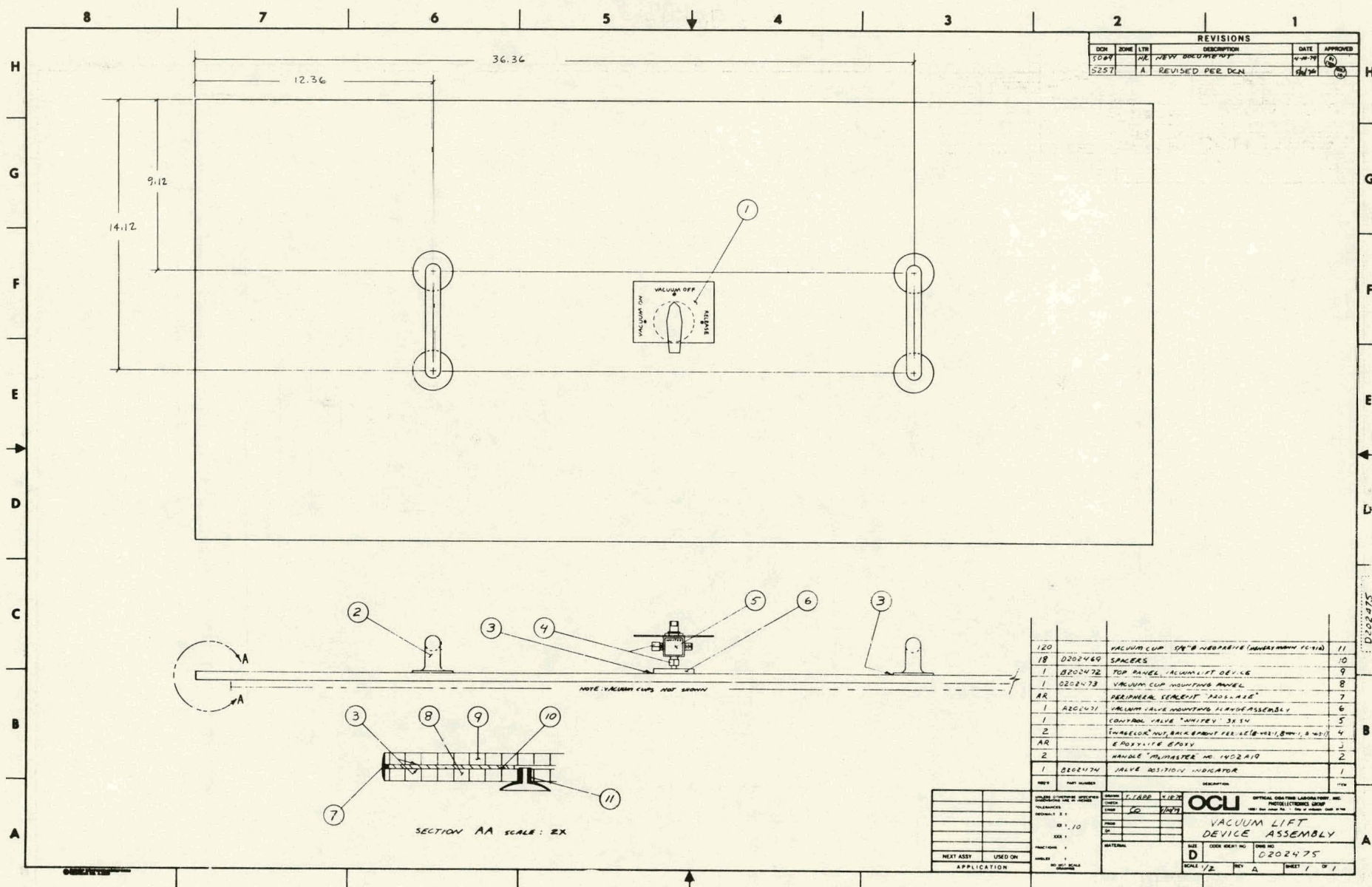


FIGURE 6

24

REVISIONS				
DCN	ZONE	LTR	DESCRIPTION	DATE
5088		N/C	RELEASE	4/1/79

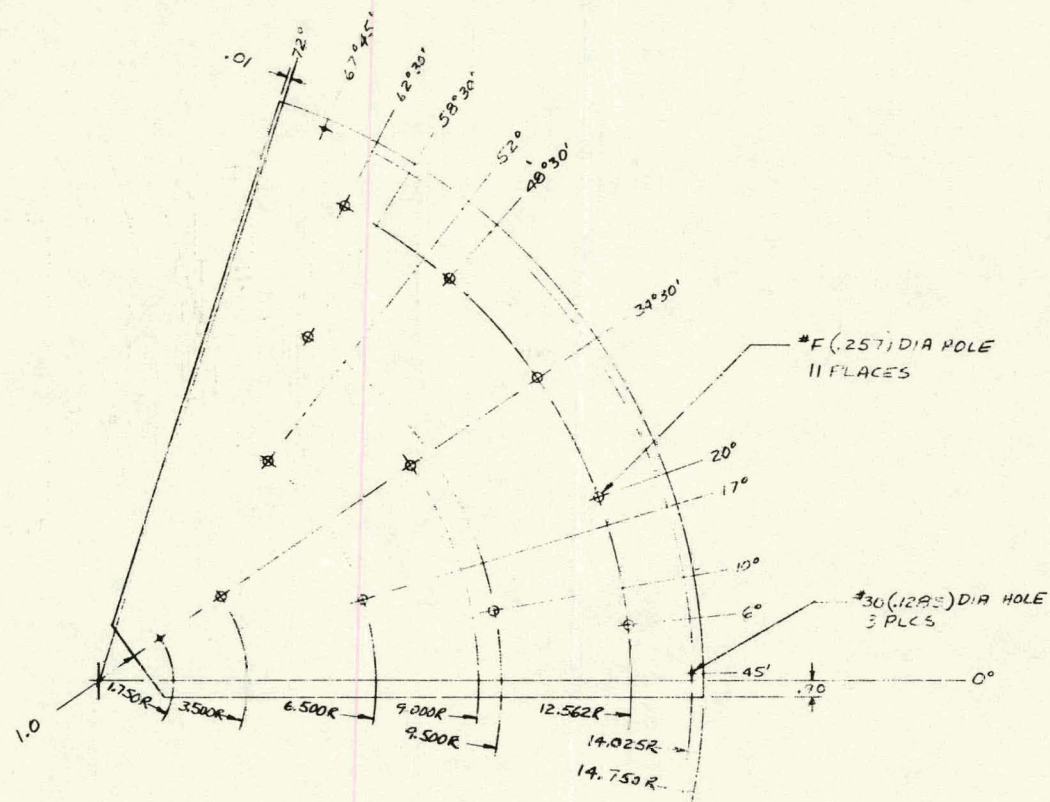


FIGURE 9

REQ'D	PART NUMBER	DESCRIPTION	ITEM
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES		DRAWN: <i>297-64477</i> CHECK: <i>1/1/79</i> ENGR: <i>1/1/79</i> PROD: <i>1/1/79</i> QA: <i>1/1/79</i>	OCL OPTICAL COATING LABORATORY, INC. PHOTOELECTRONICS GROUP 15811 Dune Island Rd. - City of Industry, Calif. 91744
TOLERANCES:		MAGNET LOCATION TEMPLATE	
DECIMALS: X .1		SIZE: C	
XX ± .015		CODE IDENT NO.:	
XXX ± .005		DWG NO. TDC 12333-1	
FRACTIONS: ±		SCALE: 1/2	
ANGLES: ± 1°		REV: N/C	
DO NOT SCALE DRAWING		SHEET: OF	
NEXT ASSY	USED ON	APPLICATION	

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BACK CONTACT SOLDERING MACHINE

<u>Drawing No.</u>	<u>Title</u>
D-202458	X-Y Motion Soldering Device (3 pages)
D-202454	Base Plate
C-202453	Soldering Unit Mounting Plate
C-202452	Side Bar
C-202456	Right Cross Shaft
B-202442	Flux Dispenser Support Yoke
B-202451	Rear Mount Block
B-202447	Actuator Arm Mounting Angle
B-202449	Actuator Arm
B-202466	Cable Bushing Mount
B-202448	Template Alignment Bar
B-202437	Indexed Longitudinal Shaft
B-202443	Longitudinal Shaft Stiffner
B-202438	Longitudinal Shaft
B-202455	Left Cross Shaft
B-202450	Guide Arm
B-202441	Front Mount Block
B-202467	Cable Pulley Mount
A-202445	Cable Support
A-202440	Longitudinal Stop Vlier Mounting Block
A-202457	Hand Retractable Plunger
A-202444	Plunger Mount Extension
A-202439	Shaft Support
A-202446	Flux Dispenser Guide Tube

VACUUM PICK-UP

<u>Drawing No.</u>	<u>Title</u>
D-202475	Vacuum Lift Device Assembly
D-202473	Vacuum Cup Mounting Panel
D-202469	Spacer Details and Location
B-202472	Top Panel Vacuum Lift Device
B-202474	Vacuum Position Indicator
A-202470	Vacuum Valve Mounting Flange
A-202471	Vacuum Valve Mounting Flange Assembly

TEST FIXTURE FOR CENTER CONTACT CELL

<u>Drawing No.</u>	<u>Title</u>
TAD-12331	Terrestrial Solar Cell Test Fixture
TDD-12331-01	Base Plate
TDC-12331-02	Vacuum Base
TDD-12331-03	Cooling Plate
TDB-12331-04	Wiring Detail
TDB-12331-05	Block - Guide Rod
TDB-12331-06	Guide Rod
TDB-12331-07	Slider
TDB-12331-08	Stop
TDB-12331-09	Guide
TDB-12331-10	Spacer
TDB-12331-11	Guide Rod
TDB-12331-12	Locator
TDB-12331-13	Slide Pivot Block
TDB-12331-14	Bearing, Slide-Rear
TDB-12331-15	Bearing, Slide-Rear
TDB-12331-16	Lever
TDC-12331-17	Actuator
TDB-12331-18	Feet, Alignment
TAD-12332	Robe Assembly
TDB-12332-01	Post
TDB-12332-02	Block
TDB-12332-03	Arm

ANTI-REFLECTIVE COATING TOOLING

Drawing No.

Title

TDD-12333

Substrate Plate - MLAR Coating, 852 Evaporator

TDC-12333-01

Magnet Location Template

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13 April 1979