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TA705 DATA RETENTION CHASSIS OPERATING MANUAL

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ABSTRACT

The Data Retention Chassis (DRC) is a data acquisition component based on the Motorola 68000 microprocessor. The purpose of the DRC is to download the correct set-up parameters into sixteen Tektronix 7912 digitizers, to verify that the digitizers retain their settings, and (once the digitizers have triggered) to load that data into the DRC battery back-up CMOS memory. The DRC also has a circuit built into it called the COMMAND LINK. With the help of the TA698 Alternate Common Equipment (ACE), the user employs this link to communicate interactively with the digitizers and the DRC. Another circuit built into the DRC is the data stream multiplexer (DSM) for high-speed data transfers.

ACKNOWLEDGMENTS

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TA705 DATA RETENTION CHASSIS

INTRODUCTION

Purpose

This manual describes the hardware and software of the TA705 Data Retention Chassis (DRC). A physical description and the operating procedures of the TA705 are provided. The TA705 is used:

- To configure the Tektronix 7912AD digitizers
- To collect data from the Tektronix 7912AD digitizers
- To transmit PCM data that is collected after an underground nuclear test is concluded at the Nevada Test Site (NTS). (The data is read, retained internally, and transmitted out of the tunnel before the ground shock can reach the recording equipment.)

System Composition

The DRC system consists of:

- Four identical but independent circuits. (Figure 1 shows the data flow of one of the four circuits used inside the DRC.)
- Support circuitry that interfaces the TEK7912 digitizers with outside recording equipment
- Circuits controlled by a Motorola 68000 microprocessor.
- Processors capable of controlling up to four TEK7912 digitizers. (There are a maximum of sixteen digitizers per DRC chassis.)

Physical Description

The description of the DRC is as follows:

Housing The DRC is housed in an all metal non-corrosive, electrically conductive chassis. The chassis is standard and rack mountable; it is 19 inches wide by 5 1/4 inches high by 26 inches deep. Chassis slides are provided to allow easy access to the internal electronic components.

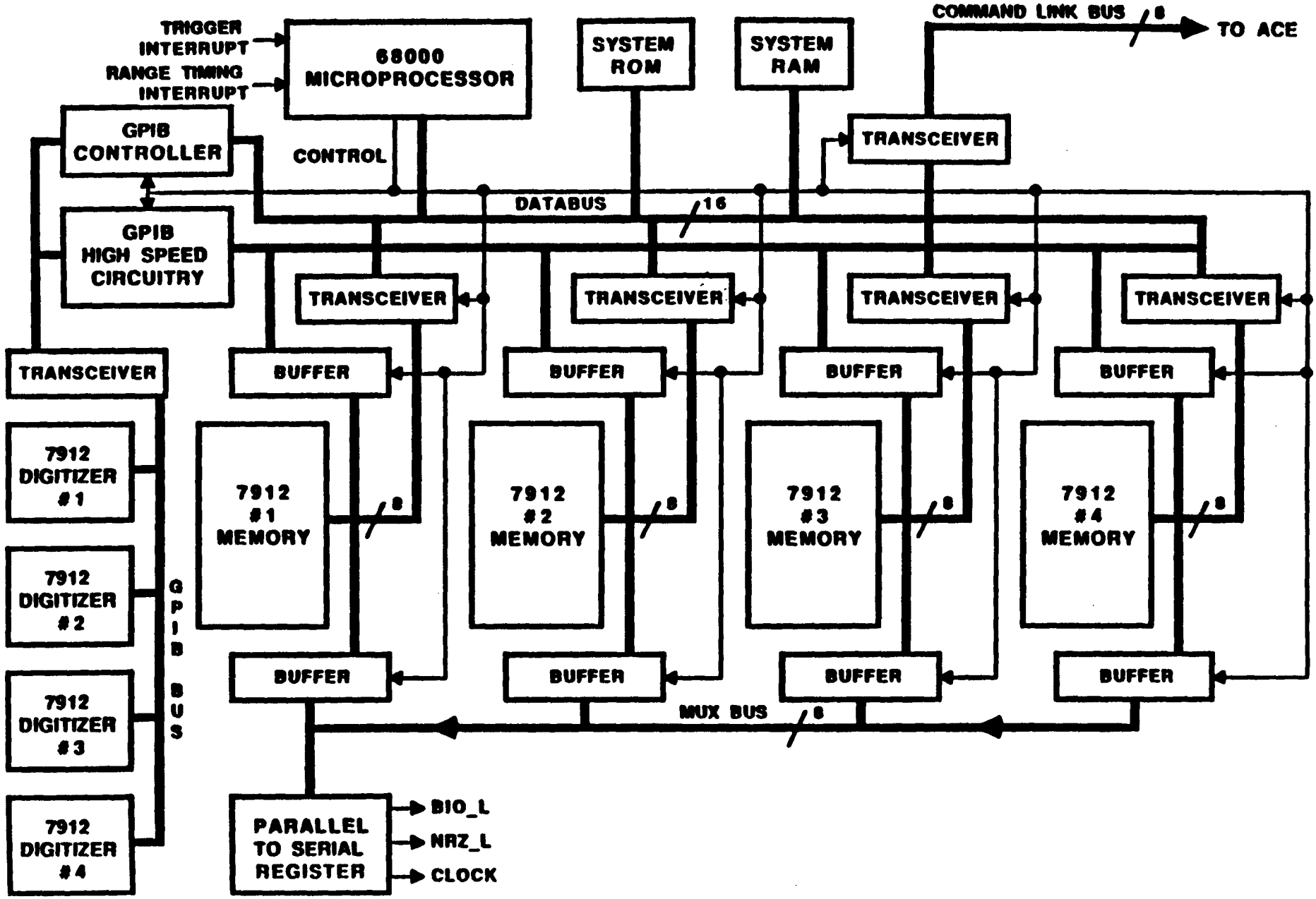


Figure 1. DRC Data Flow in Circuit A

Interface Connections	All normal interface connections are through the rear panel connectors. The connectors labeled SPARE IN/OUT, CMD LINK IN/OUT and DATA LINK IN/OUT are AMP connectors 205843-1 and use male pins, Model Number 66507-9. The connectors labeled GPIB 0,1,2, and 3 are general purpose interface connectors and are specified in the IEEE-488 standards. All other connectors are the standard BNC's female-type connectors. (BNC is for Bayonet, Neill, and Concelman.)
Circuitry	The following circuits are mounted internally on three Augat wire-wrap boards: . internal, integrated logic circuits . input/output circuits . timing circuits. All digital logic operate off +5 V furnished by two power supplies that: . are located in the back of the DRC . operate in parallel.
Cooling	Cooling is provided by a rear panel mounted fan that draws air out of the chassis through slots located on the top and bottom covers near the chassis front panel.
Front Panel	The front panel contains: . locking-type toggle switches, which prevent accidental toggling . switches that control the DRC locally . lamps that signify status and errors . display indicators that signify status

SECTION 2

HARDWARE CONFIGURATION

Description

This section describes how the hardware operates in the DRC. Using Figure 1 will make the information easier to understand.

Independent Circuits

The four independently operating circuits are laid out on two Augat, wire-wrap boards. Each circuit uses half the board.

Board	Description
Board 1, First Half	This half is identified with an [A] on the DRC schematics. All components and signals that communicate with this circuit use [A].
Board 1, Second Half	This half is identified with a [B] on the DRC schematics. All components and signals that communicate with this circuit use [B].
Board 2, First Half	This half is identified with a [C] on the DRC schematics. All components and signals that communicate with this circuit use [C].
Board 2, Second Half	This half is identified with a [D] on the DRC schematics. All components and signals that communicate with this circuit use [D].
Board 3	The other support circuits are laid out on a third Augat, wire-wrap board.

Signals pass between boards through flat ribbon cables which are connected to the board with 26 pin connectors.

THE A,B,C,D Circuits

Each of the four circuits (A,B,C,D) has a:

- 68000 microprocessor
- 16 k x 16 bit static random access memory (RAM)
- 64 k x 16 bit read only memory (ROM)

The Microprocessor

The processor:

- Monitors all the TEK7912 digitizers configuration in a continuous loop.
- Compares the configuration readings with the set-up parameters loaded in the DRC memory.
- If the parameters do not agree, the processor downloads the correct parameters into the proper digitizer.
- The processor will continue in this loop until it receives an interrupt. An interrupt can come from the:
  - timer
  - high-speed GPIB circuit
  - command link
  - range-timing circuit, or
  - trigger circuit.

Memory Types	Description
RAM Memory	. uses CMOS memory chips . is supported by two back-up batteries . is the processor's memory.
ROM Memory	. contains the operating system . contains default settings (These settings are used if the code determines there was a memory loss.)
Digitizer's Memory	. Each TEK7912 digitizer has its own battery-backed CMOS 16 k x 8 bit memory inside the DRC. . After the system has been triggered, the CMOS memory stores the TEK7912 digitizer's: . status . data . configuration.

Storing and Reading Data

Table 1 shows in what order the data is stored. This data and status information is 8724 bytes long and is stored with the most significant information loaded first. In case the multiplexer's serial data stream gets disrupted before all the data has been transmitted, the operator can still plot the data, if the first part was translated out which included the pointers and x-array data.

- The sync, sync complement, sync is loaded in first to identify this as the beginning of a new channel.
- The status information is loaded next and identifies the instrument and channel number. The sync pattern and status is loaded prior to the DRC triggering.
- The data is loaded in next starting with the pointers to be used to interpret the vertical array.
- The X array and Y array are loaded in next followed by a check sum on the data.
- Finally, the configuration of the digitizer is loaded. This is also loaded in prior to the DRC triggering.

Controller Chips and Circuitry

Motorola MC68901

- This is a multifunction peripheral controller chip
- The chip receives, interrupts, and controls in what order the processor will respond to each interrupting signal.
- The chip is equipped with an internal timer the processor uses to time out events that occur on the GPIB bus or the Command Link.

Texas Instruments TI9914

- This is the TI9914 GPIB Controller chip
- The chip communicates with the TEK7912 digitizers
- It loads the configuration

TABLE 1. TEK7912 Data Alignment in DRC Digitizer's Memory

ADDRESS DEC	ADDRESS HEX	OCT	DEF	
7659	BBD6	243	SYNC	PRE-ZERO GENERATED
		134	SYNC COMPLEMENT	
		243	SYNC	
		XXX	STATUS 1	
		XXX	STATUS 2	DRC
		XXX	STATUS 3	
		XXX	STATUS 4	
		XXX	STATUS 5	
7667	BBE6	045	ASCII %	POST ZERO GENERATED
		040	BYTE COUNT (MSB)	
		011	BYTE COUNT (LSB) = 8201	
		WWW	DATA ARRAY POINTER (MSB)	
		WWW	DATA ARRAY POINTER (LSB)	
		XXX	DATA ARRAY POINTER (MSB)	
		XXX	DATA ARRAY POINTER (LSB)	
		YYY	DATA ARRAY POINTER (MSB)	
		YYY	DATA ARRAY POINTER (LSB)	
		ZZZ	DATA ARRAY POINTER (MSB)	
		ZZZ	DATA ARRAY POINTER (LSB)	
7678	BBFC	XXX	X ARRAY DATA#1 (MSB)	
		XXX	X ARRAY DATA#1 (LSB)	
		XXX	X ARRAY DATA#2 (MSB)	
		XXX	X ARRAY DATA#2 (LSB)	7912
		XXX	X ARRAY DATA#512 (MSB)	
		XXX	X ARRAY DATA#512 (LSB)	
8702	C3FC	XXX	Y ARRAY DATA#1 (MSB)	
		XXX	Y ARRAY DATA#1 (LSB)	
		XXX	Y ARRAY DATA#3584 (MSB)	
		XXX	Y ARRAY DATA#3584 (LSB)	
15870	FBFC	ZZZ	CHECK SUM	
		ASCII	;	
15872	FC00	ASCII	SETUP INFORMATION FROM 7912	PRE-ZERO 7912
16383	FFFF	ASCII	SETUP INFORMATION FROM 7912	

. It reads the configuration and the data from the digitizers at low speed.

High Speed GPIB Circuitry

. This circuitry is used to transfer data from the TEK7912 digitizers to the DRC digitizers' CMOS memory

. It transfers the data as fast as the digitizers can transmit it (which is approximately 18 ms) into the DRC digitzer's memory.

Bus Arbitration

The processor:

. controls the data and address bus at all times

. arbitrates who can access the digitizer's memory by enabling or tristating the buffers going to the memories.

. When either the high-speed GPIB circuit or the GPIB controller requests access to one of the memories, the processor:

  . enables the circuits that pertain to that memory

  . sets up the location in memory where the data will be loaded.

This process is necessary because there are four different digitizer memories that are controlled by each processor. The multiplexer circuitry continuously reads the data out of each DRC digitizer's memory. It does not, however, read memory:
. that is being written or read by the processor
. that is being written by the GPIB circuitry.

Trigger and Range Timing

The DRC is capable of receiving:
. Three pulse-type trigger signals
. Four closure-type range timing signals.

When and how the processor collects data and the configuration from the digitizers is based on the arrival of these signals. The closure inputs are connected to range timing unit signals:

. -5 minutes
. -30 seconds
. -1 second
. reset.

The three pulse-type signals are connected to a trigger source, e.g. either fidu or compton. Even though the DRC can receive three different pulse-type signals, each processor must be jumpered to only one pulse signal.

The closure signals are received through the debounce circuitry of the DRC. Each time one of the closure signals is activated or deactivated, its action is stored in a status register and an interrupt is generated.

The trigger circuit expects a transistor-transistor logic (TTL) level pulse terminated in 50 ohms with a minimum width of 6 ns. The pulse (also stored in a status register) will cause an interrupt. The pulse circuit that records the trigger is battery-backed and can only be reset by the processor.

Command Link

Part of the support circuitry includes the Command Link which is used to:

- download, examine, or change either the DRC or the TEK7912 digitizer parameters. (The master data base table set-up parameters are downloaded through this link.)
- upload data and set up parameters from the DRC or the TEK7912 digitizers.

The Command Link is an interactive link that interfaces the DRC to the ACE. The communication between the two devices is accomplished through an eight-bit data bus (the CLD0-CLD7) plus the control signals which are:

- Four function codes: FC0-FC3
- Two address lines: ADR2-ADR3
- One subaddress line: SA0
- One power-on reset line: POR
- One clock line, STROBEA0

The ACE uses these data and control lines to:

- transmit and receive data
- specify which processor or TEK7912 digitizer to communicate with
- interrupt a certain processor
- read the status register of the DRC.

The ACE communicates with the DRC by sending it a certain code which the DRC interprets and executes. The complete set of codes used to communicate be-

tween the two devices are fully explained in Appendix A. Also, see SAND86-1398: Larry W. Ebinger, SANDUS Command System Message and Data Format.

When the ACE communicates with the DRC, the first thing it does is check the status register inside the DRC. It does this by sending the function code for a read status. This register is 8 bits wide. Two of the 8 bits are dedicated to each processor:

- Bits 0 and 1 are for Processor [A]
- Bits 2 and 3 are for Processor [B]
- Bits 4 and 5 are for Processor [C]
- Bits 6 and 7 are for Processor [D].

A low on the lower of the two bits indicates that that particular processor's buffer is empty and ready to receive a byte of data from the ACE. A low on the other bit indicates that that processor's buffer has a byte of data ready for the ACE.

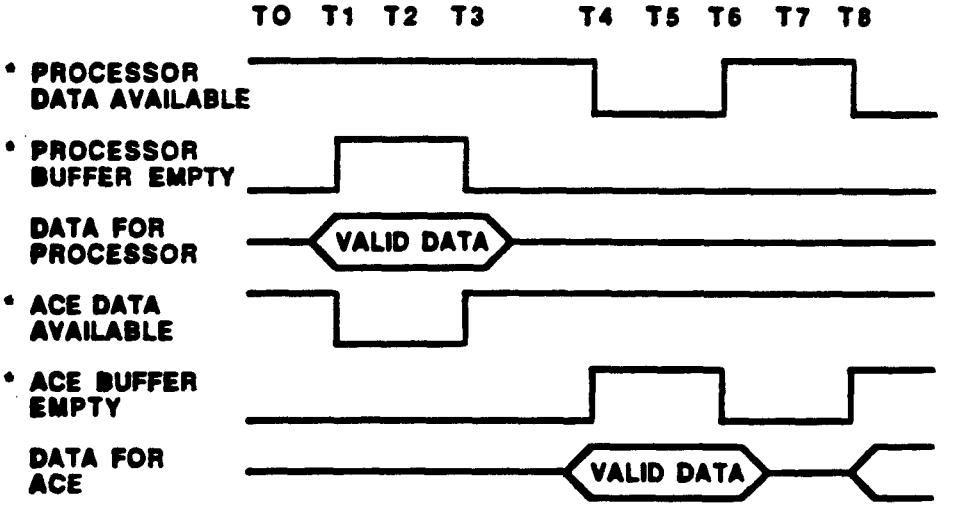
Sequence of Events. Listed below is an explanation of the different stages that are involved in passing data betwen the ACE and one of the processors. Figure 2 also shows this sequence of events graphically.

STAGE	WHO DOES IT	WHAT HAPPENS
At T0	ACE	checks the status register and determines if the processor buffer is empty.
At T1	ACE	writes a byte of code to the buffer and thereby sets the "ACE has data available" flag. This action: . signifies to the processor that data is loaded in its receiver buffer . resets the bit in the status register signaling that the processor's buffer is no longer empty.
	ACE	then sends the codes that will interrupt the processors.
At T2	Processor	answers the interrupt by checking the "ACE has data available" flag.

Stage	Who Does It	What Happens
At T3	Processor	reads the byte of data out of its receiver buffer. This: . resets the "ACE has data available" flag. . sets the processor buffer's empty bit in the status register which lets the ACE know it has read the last byte and is ready to accept another byte.

If more bytes are sent, the procedure is repeated until all the data has been transmitted.

Since the processor knows by interpreting the code that more information is required, it does not have to be interrupted again until the command has stopped and a new command has begun. It will just monitor the "ACE has data available" flag for the next byte or time out.



*active low

Figure 2. Sequence of Events Involved in Passing Data Between ACE and DRC

STAGE	WHO DOES IT	WHAT HAPPENS
At T4	Processor	. has interpreted the data . is required to send information back to the ACE . writes a byte of data to its transmit buffer This action: . sets the bit in the status register "processor has data available" flag signifying that data is available to the ACE. . resets "ACE buffer empty" flag.
At T5	ACE	. reads the status register . finds the bit set in the status register that the processor has data
At T6	ACE	. reads byte of data from the transmit buffer This action: . signifies to the processor that it has read the buffer. . sets "ACE buffer empty" flag. . resets "processor has data" available" flag
At T7	Processor	. checks the ACE buffer empty flag
At T8	Processor	. writes another byte to the transmit buffer . resets the ACE buffer empty flag . resets the bit in the status register "processor data available" . process continues until all required data is transmitted.

Data Stream Multiplexer

Another part of the support circuitry is the Data Stream Multiplexer which reads triggered data directly out of the digitizer's memory without involving the microprocessor. This data is delivered on the PCM serial data stream to the uphole recording equipment.

Data can be outputted through:

- the DRC parallel interface port, or
- the Multiplexer serial stream port.

Settings may be selected in two different ways:

- with the DRC in the **local mode** the settings can be selected with the front panel lever wheel and toggle switches

- with the DRC in the **remote mode** the settings can be selected through the ACE

Multiplexer's Settings on the Front Panel LEDs show:

- the bit rate and format
- the port (either the serial or the parallel port) in which the data is output

ELEMENT	DESCRIPTION
Condition	When data is sent out on the serial port

Circuitry. The multiplexer circuitry is a continuously running circuit that:

- reads each of the sixteen TEK7912 digitizer's memory inside the DRC
- converts the parallel data into serial data
- outputs data in two different ways:
  - a BIO_L type signal
  - a separate clock and NRZ_L type signal.
  - can run at bit rates of:
    - 2.5 Mb/s
    - 5.0 Mb/s
    - 10.0 Mb/s
    - 20.0 Mb/s
- contains four different formats: 1, 2, 3, 4

PROM at Location 3BA12 on Board 3 can be programmed to:

- record the order in which each memory is read
- read one DRC digitizer's memory faster than another DRC digitizer's memory
- exclude certain DRC digitizer's memory.

ELEMENT	DESCRIPTION
Condition	When data is sent out on the parallel interface port
Action	. ACE sends four address lines . lines are decoded by the DRC circuitry which selects one of the 16 digitizer's memories inside the DRC . ACE sends a series of negative data strobes . data is clocked out by the data strobe . ACE reads the data . the rising edge of the pulse . disables the memory . increments the address to the next location in memory . the cycle repeats until all data has been read out of the memory.

Front Panel of the DRC

The Front Panel of the DRC is shown in Figure 3. A description is given below.

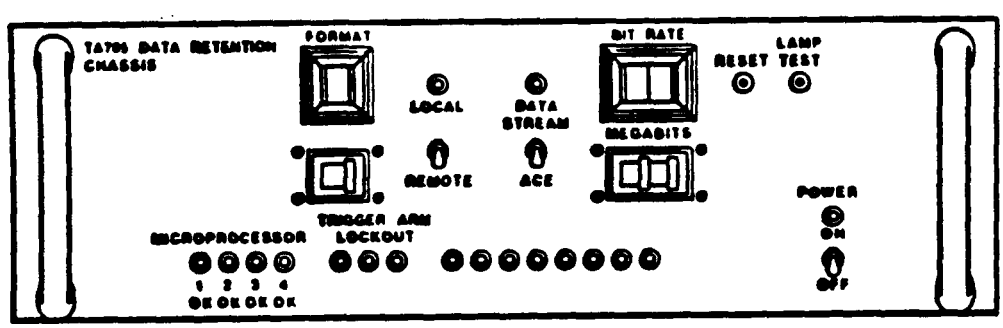


Figure 3. DRC Front Panel

The following actions occur simultaneously:

- The switch labeled "Power" turns on the DRC
- The LED above the switch illuminates
- The power is applied to the DRC circuits
- Four LEDS illuminate to indicate which processors are running:
  - MICROPROCESSOR 1 OK
  - MICROPROCESSOR 2 OK
  - MICROPROCESSOR 3 OK
  - MICROPROCESSOR 4 OK

When one of the following signals is received by the DRC, the appropriate LED is illuminated:

- TRIGGER
- LOCKOUT
- ARM.

The other eight unlabeled warning LEDs work with the MICROPROCESSOR LEDs to signify errors. Going left to right:

Microprocessor	Works With
1	the first two LEDs
2	the second two LEDs
3	the third two LEDs
4	the last two LEDs

If an event occurs while running one of the test options, the microprocessor LED and the warning LEDs will flash on and off until the problem is corrected. The sequence of events is as follows.

The MICROPROCESSOR OK LED will flash on and off.

- If error occurred in the **first memory**, neither warning LED will flash
- If the error occurred in the **second memory**, the lower of the two warning LEDs will flash on and off
- If the error occurred in the **third memory**, the higher of the two warning LEDs will flash on and off
- If the error occurred in the **fourth memory**, both warning LEDs will flash on and off.

PUSH BUTTONS

- The **Reset** push buttom resets all four microprocessors at one time with the test option switch set to one.
- The **Lamp Test** push buttom illuminates all LEDs on the front panel to make sure they are all working

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THREE SWITCHES

- The LOCAL/REMOTE SWITCH
- The ACE/DATA STREAM SWITCH
- The LEVERWHEEL SWITCH

LOCAL/REMOTE SWITCH

WHEN THE SWITCH	THEN
is set to LOCAL	the LED illuminates and the following must be selected from the front panel: . the format . the bit rate . choice between ACE or DATA STREAM Port.
is set to REMOTE	the selections must be sent through the Command Link

LED	Description
FORMAT LED	. specifies which format the multiplexer circuitry is outputting . can be changed with the leverwheel switch located below it
BIT RATE LED	. specifies at which rate the Multiplexer is running . can be changed with the leverwheel switch located below it

ACE/DATA STREAM SWITCH

This switch locally selects whether the DRC data will be:

- outputted in serial through the Data Stream, or
- outputted in parallel through the ACE port.

WHEN THE DATA	THEN
is output through the Data Stream	the LED above the switch is illuminated

The Test Option **LEVERWHEEL SWITCH**:

- is located to the left of the Bit Rate leverwheel switch
- selects twelve different test options (See **Chapter 4** for definition of these options)
- works in conjunction with a microswitch inside the DRC on Board 3

Back Panel of the DRC

Figure 4 shows a diagram of the back panel of the DRC. The pin definition for each of the connectors is labeled in Appendix C.

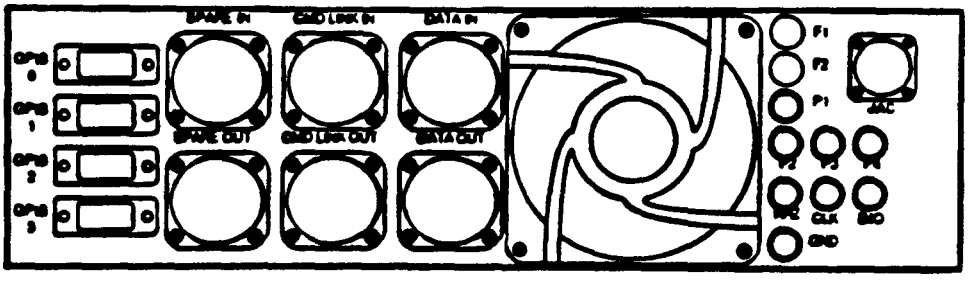


Figure 4. DRC Back Panel

GPIB 0 through GPIB 3 connect the DRC to the TEK7912 digitizers using the standard IEEE-488 cables.

- GPIB 0 communicates with Processor A
- GPIB 1 communicates with Processor B
- GPIB 2 communicates with Processor C
- GPIB 3 communicates with Processor D

CONNECTOR	ACTION
Spare-In	receives the closure-type signals for the range-timing signals
Spare-Out	outputs the status on whether: . lockout has been received . arm has been received . trigger has been received . DRC is in calibration has the connection for the two back-up batteries: . lithium battery . rechargeable battery
CMD Link In	connects the ACE and the DRC command link together
CMD Link Out	connects to a terminator plug or to another DRC

Data In	connects the ACE to the Multiplexer circuitry for parallel data output
Data Out	connects to a terminator plug or to another DRC.

ITEM	PURPOSE
F1/F2 Fuse Holders	Used to fuse the AC power
P1/P2/P3 BNC Connectors	Receive the three-pulse type signals
P4 and BIO_L BNCs	Output the bi-phase signal from the Multiplexer circuitry
Clock BNC	Outputs the clock from the Multiplexer circuitry
NRZ-L	Outputs the data from the Multiplexer circuitry
JAC Connectors	Connect the AC power to DRC

SECTION 3

SOFTWARE CONFIGURATION

Description

This section describes what the software accomplishes inside the DRC. The code was written in 68000 assembly language and was downloaded into two Waferscale WS57C64 and two Intel 27512 proms.

Code

The code operates in two time stages:

Idle Time. During startup or when reset is activated, begins idle time. While running in the idle time loop:

- Check to see if the DRC memory has retained its data
- Verify digitizers are at the correct setting
- Runs commands sent over the Command Link
- Runs any test option selected.

Zero Time. When the DRC receives -30 sec or -1 sec range-timing signals, zero time begins. While running in the zero time loop, the code:

- Disables Command Link
- Verifies that the digitizers are at the correct setting
- Loads digitizers setting in DRC digitizer's memory
- Loads data from digitizers into DRC digitizer's memory once the digitizers and DRC trigger
- Goes into a do-nothing loop.

Major Branches

To help the reader understand the software, this section divides the code into the major branches the code jumps to while running in either the idle-time or the zero-time loop. Figure 5 is a flowchart of the major branches.

- Each branch is described
- The reason the code branched to this section is explained
- Where the code will branch from here

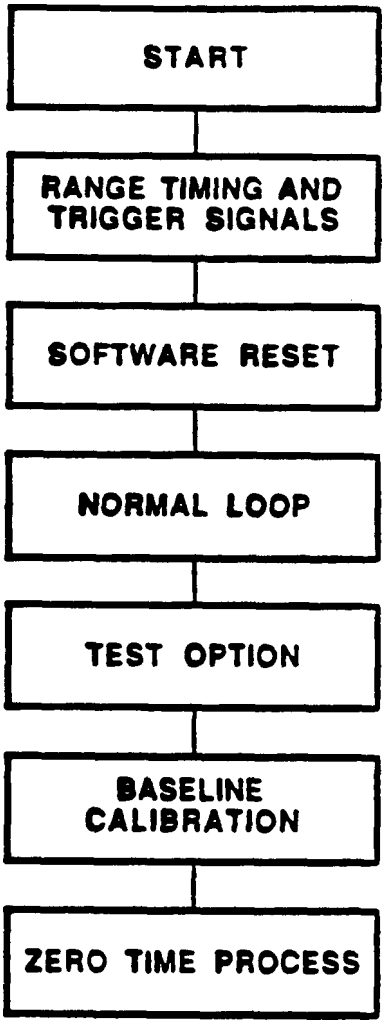


Figure 5. Flowchart of the Major Sections

PART	DESCRIPTION
START ACTION BOX	This is the beginning of the code and is executed: . when power is applied to the microprocessor, or . when a front panel reset button is activated with the test option switch set to one. **The code:** . initializes the variables in the software . loads up the vector table for interrupts and errors

- sends the signals that reset the components in the circuit

- does a memory check for memory retention by checking four different locations for the patterns:

  - 9669
  - A55A
  - 6996
  - 5AA5

  at the:

  - beginning of the memory
  - middle of the memory
  - end of the memory

If any of these locations do not have this exact pattern, the code assumes it does not have the correct data.

EXAMPLE

It is very important that the code know where it is and what events have taken place. If the DRC loses power after the TEK7912 digitizers trigger, once the DRC regains power it must not reset the digitizers for this could cause the TEK7912 digitizers to retrigger and could result in the data getting rewritten with invalid data.

Memory Test Patterns. If these patterns:

- match, the code branches to the trigger and range-timing signals section

- do not match, the processor assumes the worst case: post zero time. This indicates the processor may or may not have collected any of the digitizer's data. The code will:

  - set its registers in their triggered or zero time configuration

  - wait 150 ms. (It waits 150 ms in case it has previously called for zero time data.)

  - write the memory with the correct memory test pattern

  - bring in the default channel numbers

This will give the multiplexer circuit a chance to read out 1 or 2 passes of data. The Code then branches to the trigger and range-timing signals section.

SECTION	DESCRIPTION
RANGE TIMING AND TRIGGER SIGNALS	The code now looks at the register that records the status of the range-timing signals before the interrupt. These signals are the: . -5 min . -30 s . -1 s . Reset. The trigger signal is also reviewed.

External range timing and trigger signals are used to:

- tell the DRC the countdown time
- instruct the DRC when to get set up information from the TEK7912 digitizers
- instruct the DRC when to get data information also from the TEK7912 digitizers.

Listed below are the range timing and trigger signals followed by an explanation of why the system uses these signals.

SIGNAL	ALSO CALLED	DESCRIPTION
-5 min	baseline calibration	TEK7912 digitizers show a tendency to drift after power has been on for some time. A baseline shot 5 minutes before the trigger signal arrives may be used to calibrate the triggered data.
-30 s	initial lockout	is the last time the configuration of the TEK7912 digitizer will be checked before the trigger arrives.

-1 s	final lockout	. backs up the -30 s signal . does not check or load the configuration of the TEK7912s digitizers into the DRC's digitizer's memory
RESET.	The range timing reset signal resets the system.	
TRIGGER.	Following the trigger signal, there is a 16-ms delay that gives the TEK7912 digitizers time to digitize the data.	

Table 2 below:

. lists each timing and trigger signal
. describes the action caused by these signals when the signals are delivered to the DRC.

Table 2. Range Timing and Trigger Signal Results

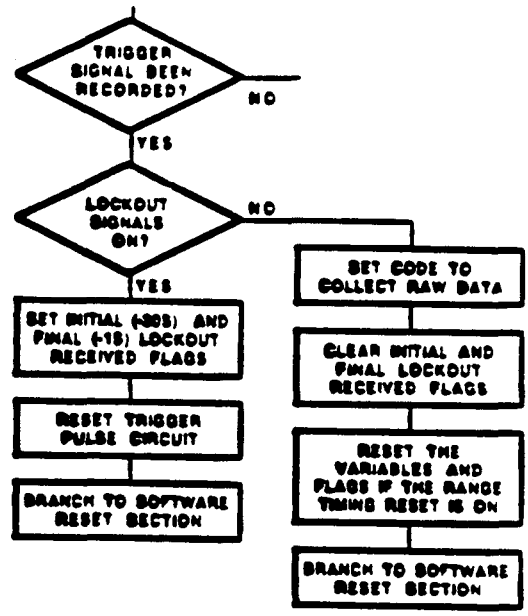
TIMING	REACTION
-5 MINUTES	RESET EACH TEK7912 DIGITIZER WAIT 30 SECONDS SHOOT A BASELINE ON ALL DIGITIZERS SET DIGITIZERS BACK TO CORRECT CONFIGURATION READ OUT AND STORE BASELINE INTO DRC MEMORY
-30 SECONDS	REQUEST CONFIGURATION FROM EACH DIGITIZER LOAD CONFIGURATION INTO DRC MEMORY ATTEMPT TO DOWNLOAD PARAMETERS IF INCORRECT ASK DIGITIZERS TO DIGITIZE DATA AFTER THE TRIGGER
-1 SECOND	BACKUP FOR -30 SECOND SIGNAL HALT DRC FROM DOWNLOADING ANY MORE PARAMETERS ASK DIGITIZERS TO DUMP DATA IF THERE IS NO -30 SECONDS SIGNAL
RESET	RESET THE DRC IF -30 SECONDS AND -1 SECOND SIGNALS ARE DEACTIVATED
TRIGGER	DELAY FOR 16 MS, THEN INPUT RAW DATA FROM TEK7912 DIGITIZERS COMMAND ANY DIGITIZER THAT DID NOT SEND DATA, TO SEND DATA UNTIL THE RANGE TIMING SIGNAL IS DEACTIVATED

Software Status Registers. Since range timing signals play such an important role, their status is recorded in some internal software status registers.

- the registers are tripled in memory
- once registers are called, the code does a comparison between the three registers
- all registers should contain the same values, but if they do not:
  - a vote is taken for 2 out of 3 register values
  - the third register is written to comply with these values
  - if all three registers are different, the code uses the default value
- some registers are static to save the history of the range timing signals
- other registers are dynamic: they are updated as soon as an interrupt takes place.

Trigger Signal Recorded. Figure 6 (a) is a flowchart of the path taken by the code when a triggered signal has been recorded by the DRC

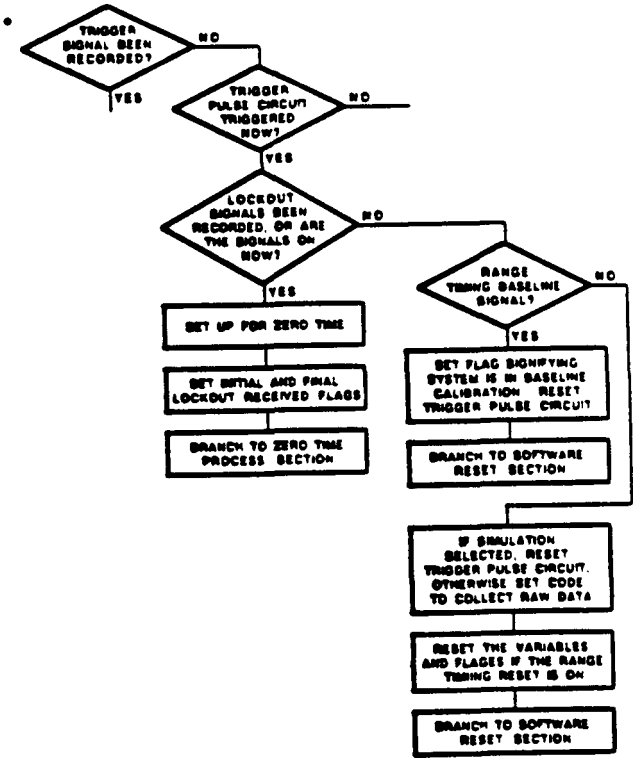
- the code checks the status of the lockout signals to verify whether the initial and final lockout flags need to be set or cleared before branching to the software reset section.
- If there are no lockout signals, the range timing reset signal is checked to see if a reset is being requested.
- Whenever a range timing reset signal is sent and there are no lockout signals, the DRC will initialize its variables and reset its components.



a)

Figure 6. Flowchart Showing Trigger Status
a) Trigger Signal Recorded Earlier

No Trigger Signal Recorded. Figure 6 (b) is a flowchart of the path the code will take if the trigger signal was not recorded earlier, but has just arrived.



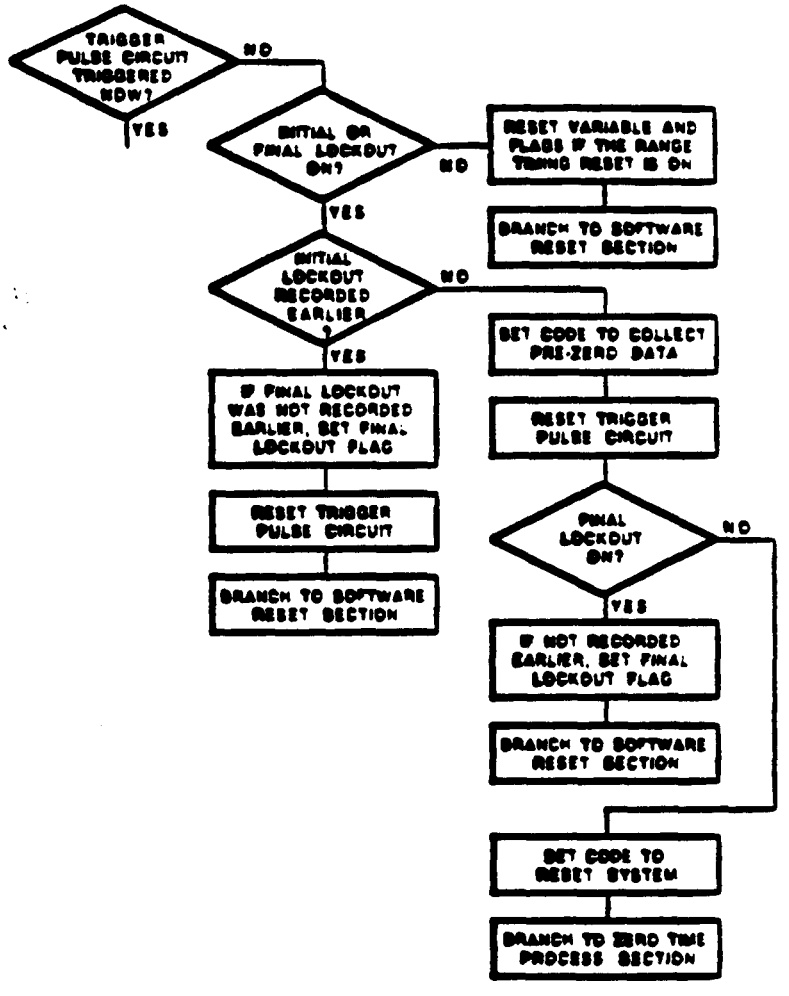
b)

Figure 6 Continued. b) Trigger Just Arrived

If the lockout signals are active, the code:
. sets initial and final lockout flags
. branches to zero time loop to see if it needs to collect data.

If the lockout signals are not active, the code:
. checks to see if baseline calibration is requested
. checks to see if Test Option 3 is selected
. checks to see if range timing reset is active.

No Trigger Pulse Circuit Received. Figure 6 (c) is a flowchart of the path when no trigger signal is received.



c)

Figure 6 continued. c) Trigger Just Arrived

The code will evaluate the state of the lockout signals:

- If the lockout signals are not active and the range timing reset is active, the system will be reset
- If initial lockout is active, the code will be set to collect set-up parameters and data from the TEK7912 digitizers
- If only final lockout is active, the code will be set to collect only the data from the TEK7912 digitizers.

SOFTWARE RESET

Description. This part of the code is entered once the microprocessor receives a range-timing reset from the ACE. Figure 7 is a flowchart for this section of the code.

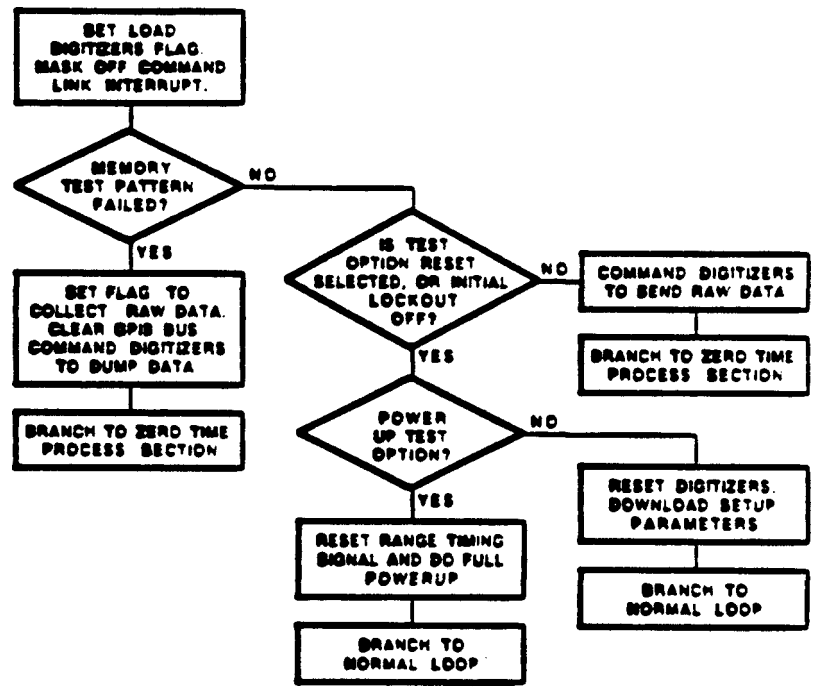


Figure 7. Flowchart of the Software Reset Loop

If the memory test pattern failed, the code will request data.

Data Request. When requesting data, the code sends the commands to the digitizer to digitize and dump raw data.

First time through the code	Not the first time through the code
. Code will download the set-up parameters	. Code will ask for the set-up parameters . Code will try twice to get digitizers to accept commands . If unsuccessful, code will send a device clear to those digitizers that failed . Code will try to send commands the third time before branching to the zero time process section.

If the memory test pattern passes, the code will:

. Check to see if one of the test options is selected which will either:

  . reset the range timing signals, OR
  . reset the TEK7912 digitizers and download the correct set-up parameters

. Check for lockout signals which will command the TEK7912 digitizers to send data.

NORMAL LOOP

Description. This is the main loop when operating in idle mode; the code will stay in this loop until either a reset or the range-timing signals arrive. Figure 8 shows the code will either:

. collect data, OR
. shoot a baseline on each TEK7912 digitizer, OR
. stay in the idle time loop

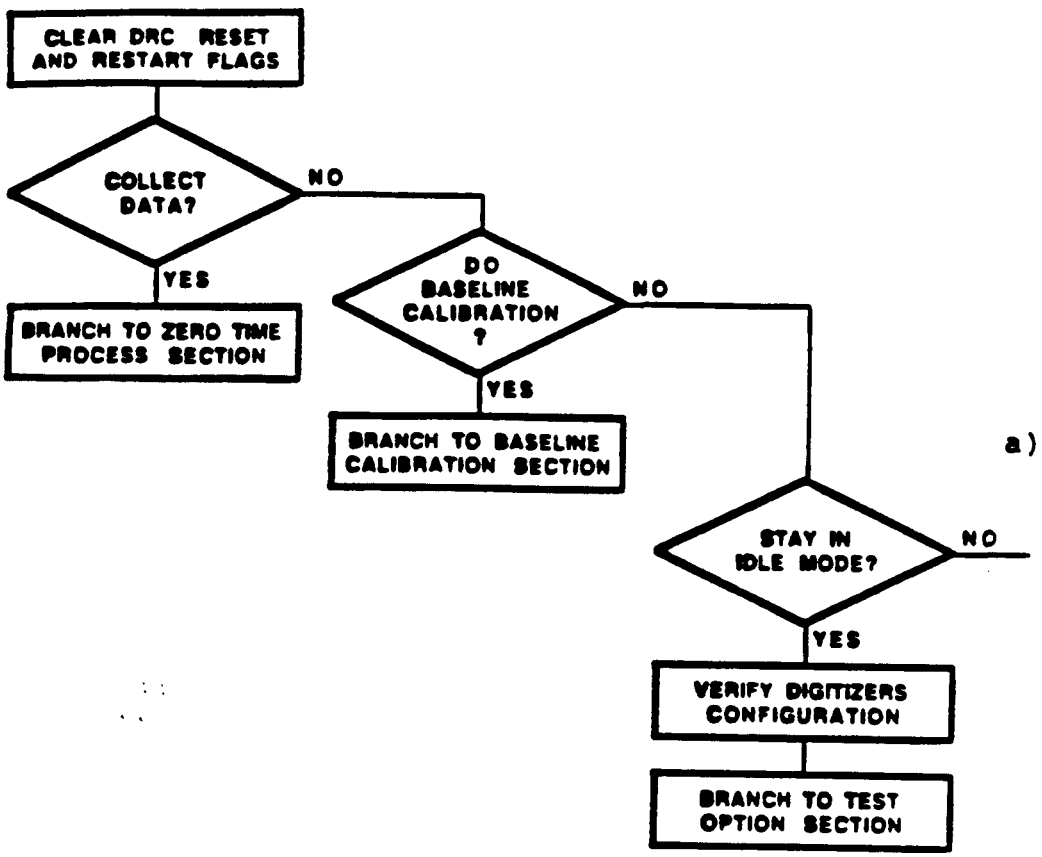


Figure 8. Flowchart of Normal Loop
a) Idle Time Loop

Verify Digitizers Configuration. There are three different options the code would use to configure the TEK7912 digitizers.

1) The code will first use the setup parameters downloaded to it by the command link. These parameters are loaded into the microprocessor RAM memory.

2) If the DRC loses power and the backup battery fails, the code will use the digitizer's setup parameters. The TEK7912 digitizers are equipped with a forget-me-not memory chip that returns the setup parameters the digitizers were at when the power was lost.

3) The code will compare two parameters (the mode digital and the trigger external) to test the digitizer's memory. If these parameters are incorrect, the code will use the setup parameters stored in the DRC ROM memory.

Once the code receives a reset, it will return and repeat Option 2.

Figure 8 (b) is the normal loop section with the code getting ready to branch to the zero time loop.

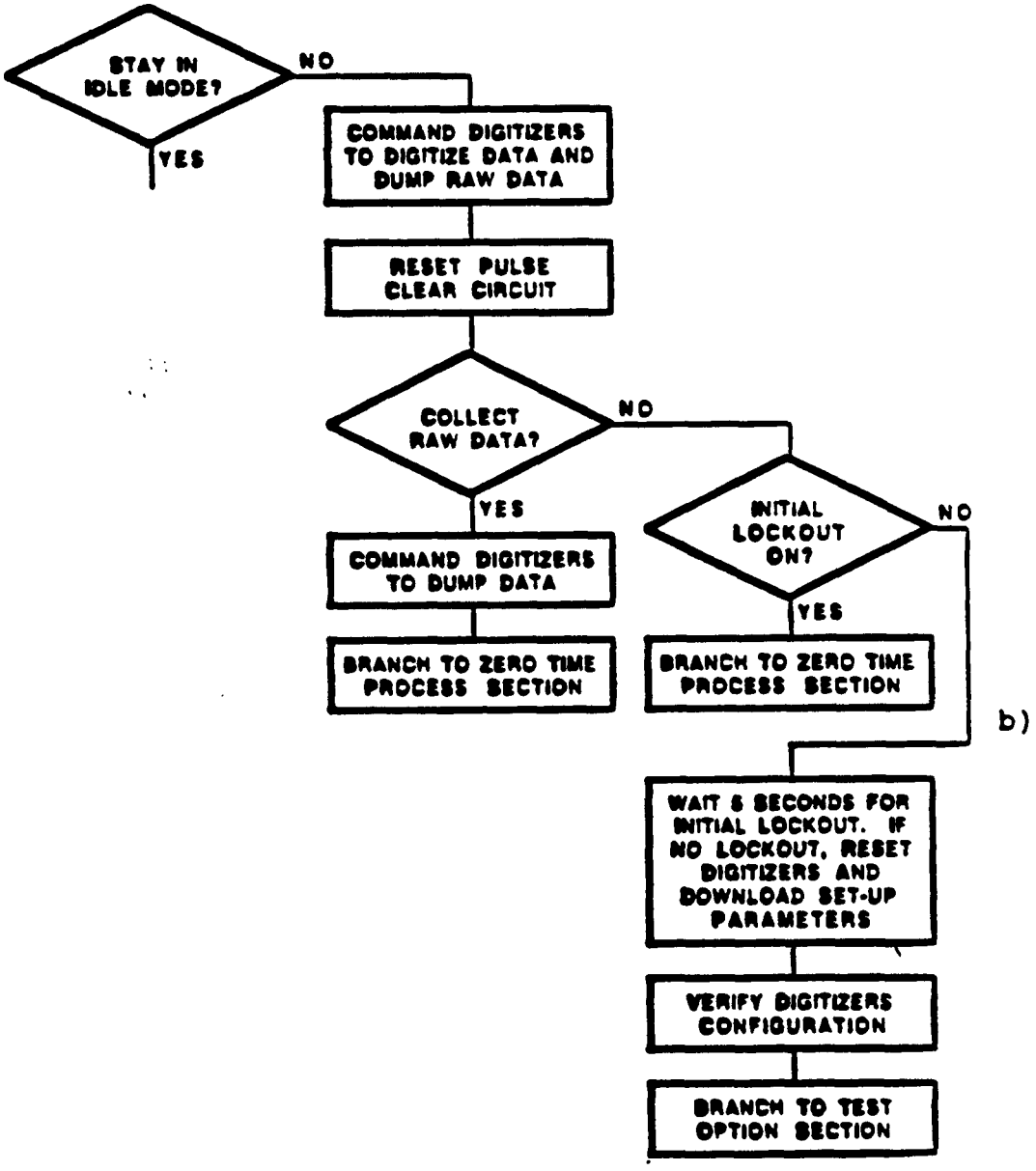


Figure 8 continued. b) Zero Time Loop

The code will go collect data from the TEK7912 digitizer, OR

will wait in a loop for 5 s for:

- the abort flag to be set which resets the DRC
- the initial lockout signals to become active and branch to the zero time loop

After the 5 s timeout, the code:

- sends a device clear to all digitizers
- downloads set-up parameters to each digitizer
- checks for any test options selected
- verifies digitizers' configuration.

TEST OPTION

Figure 9 is a flowchart of the Test Option Code. When the processor runs this section of the code, it examines, then executes any test option selected. If a reset is set by an interrupt or the Command Link, the code branches to the software reset section, otherwise it branches to the normal loop section.

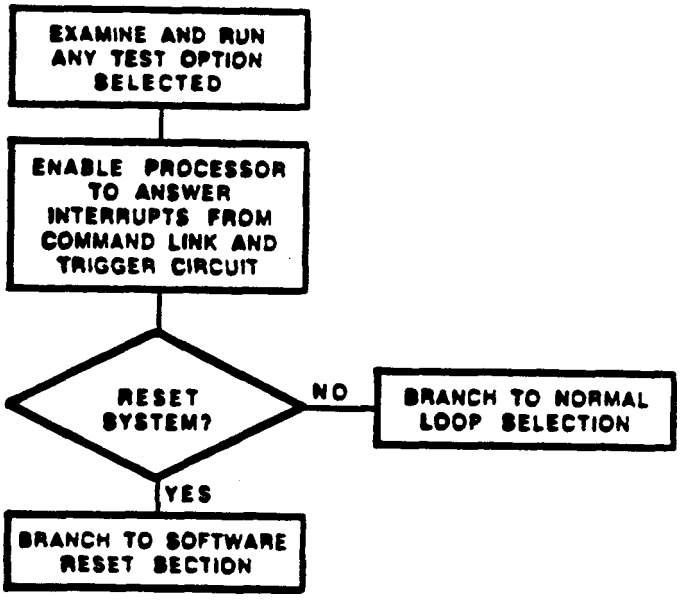


Figure 9. Flowchart of Test Option Code

BASELINE CALIBRATION

When the digitizers have been on for a considerable time, the traces in them sometimes drift. In order to compensate for this, the code will command the digitizers:

- to shoot a baseline
- load that data into its memory for readout 5 min before the trigger comes.

Note: This baseline may then be used to calibrate the actual data.

BASELINE CALIBRATION CODE

Figure 10 shows the path taken to record a baseline in the DRC's memory.

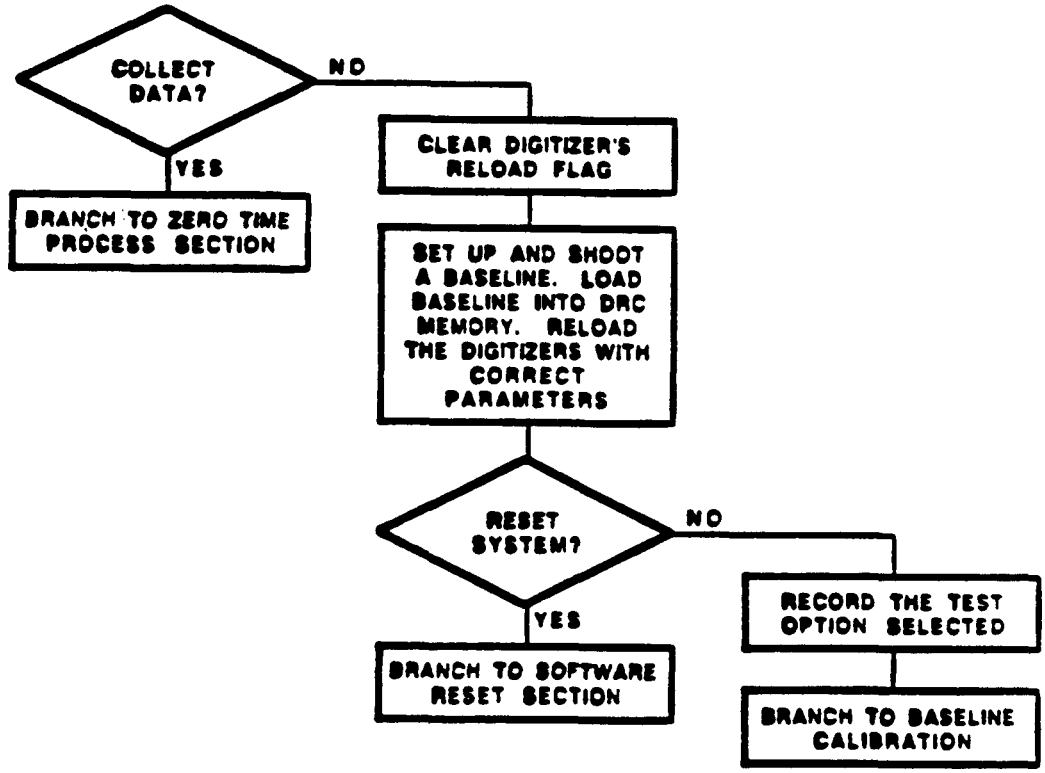


Figure 10 Flowchart of the Baseline Calibration Code

ZERO TIME PROCESS

This part of the code is executed after the microprocessor has received the correct range-timing signals signifying the digitizers have triggered. The zero time process will leave this section only when either:

- a range timing reset signal has been sent and initial and final lockout has been released, OR
- the front panel reset is activated with the test option switch set to Option 1.

Figure 11 is the flowchart for this section. The code will seek to see if:

- it needs to load just the raw data from the digitizers
- load the raw data and the configuration from the digitizers, OR
- if the data has already been collected, the code goes into a "do nothing" loop.

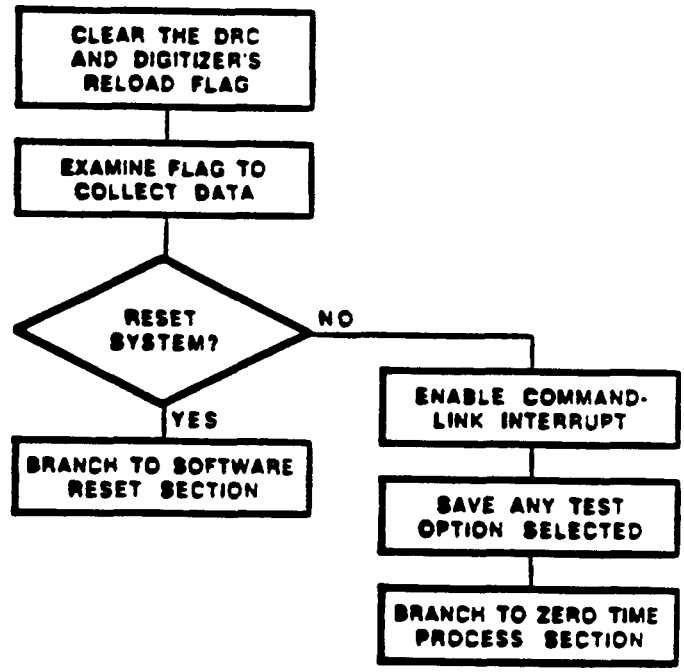


Figure 11. Flowchart of Zero Time Process Section

SECTION 4

OPERATION

DESCRIPTION

This chapter describes the installation, checkout, and basic operating instruction of the DRC. The DRC was designed to operate underground with very little user interaction. However, a simple test must be made to begin with in order to verify that the DRC is operating correctly.

The equipment needed to check out the DRC are:
- an ACE
- the TA703 Range Timing Unit
- a generator that can deliver at least a 5 V and 6 ns pulse
- either a 5 V lithium battery or rechargeable battery
- A Tektronix 1240 Logic Analyzer with a GPIB ROM pack and adapter
- one or more TEK7912 digitizers.

INSTALLATION

The DRC requires two normal blowing 4 amp 125 V fuses. Two fuses are required to handle the two power supplies that were put in for reduncancy; these power supplies are:
- wired in parallel
- connected to two different AC sources.

Status Register Input. Since the same software runs on all microprocessors, the code must have some way of knowing which TEK7912 digitizers it is to address. This is done by reading a status register during initialization. This status register input must be set by wire wrapping the pins.

WIRE WRAPPING THE PINS

1) Connect Pins 8 and 9 of the buffer at 3CG34 to ground. This sets up Circuit [A] to communicate with the digitizers with GPIB addresses 0, 1, 2, or 3
2) Connect Pin 9 of the buffer at 3DG34 to ground. This sets up Circuit [B] to communicate with the digitizers with GPIB addresses of 4, 5, 6, or 7

3) Connect Pin 8 of the buffer at 3EG34 to ground. This sets up Circuit [C] to communicate with the digitizers with GPIB addresses of 10, 11, 12, or 13
4) Leave the buffer at 3FG34 open which sets up Circuit [D] to communicate with addresses of 14, 15, 16, or 17.

Each processor must be connected to one of the following clock speeds:

. 6.25 MHz, OR
. 12.50 MHz.

Table 3 shows how each microprocessor should be wire wrapped to obtain one of the clock speeds.

Table 3. Clock-Speed Selection

Microprocessor	6.25 MHz	12.5 MHz
A	1AB3 to 1AC3	1AB4 to 1AC4
B	1DB3 to 1DC3	1DB4 to 1DC4
C	2AB3 to 2AC3	2AB4 to 2AC4
D	2DB3 to 3DC3	2DB4 to 2DC4

Component Sockets. Finally, a jumper needs to be inserted into an 8-pin component socket to connect the microprocessor to one of the trigger inputs: **P1, P2, or P3:**

. Circuit [A] component socket is located at 3BG42
. Circuit [B] component socket is located at 3BG47
. Circuit [C] component socket is located at 3BG52
. Circuit [D] component socket is located at 3BG57.

To connect to:
. the P1 input, jumper Pin 1 to Pin 8
. the P2 input, jumper Pin 2 to Pin 7
. the P3 input, jumper Pin 3 to Pin 6

Changes. Some format changes might be necessary if all 16 digitizers are not used:

. When the DRC is working on default parameters, it expects four digitizers on each microprocessor
. The DRC will try repeatedly to communicate with any missing digitizers.

Appendix B of this text explains the procedure for changing the software to default the correct number of digitizers.

CHECKOUT PROCEDURES

Below are the proper checkout procedures:

1. Connect the TEK7912 digitizers to the DRC
2. Connect up to 4 TEK7912 digitizers to each of the 4 GPIB connectors on the back of the DRC:

   . Connector GPIB 0 should be connected to the digitizers which have their GPIB addresses set at 0, 1, 2, or 3

   . Connector GPIB 1 should be connected to the digitizers which have their GPIB addresses set at 4, 5, 6, or 7

   . Connector GPIB 2 should be connected to the digitizers which have their GPIB addresses set at 10, 11, 12, or 13

   . Connector GPIB 3 should be connected to the digitizers which have their GPIB addresses set at 14, 15, 16, or 17.

3. Connect the TA703 Range Timing Unit to the SPARE-IN connector of the DRC.*

4. Connect the trigger generator to the BNC trigger input selected, either:
   . P1
   . P2
   . P3.

5. Connect the ACE to the CMD-LNK-IN and J-DATA-IN connectors*

6. Connect the terminator plugs supplied with the unit to the CMD-LNK-OUT and DATA-LNK-OUT connectors

7. Connect the battery to the SPARE-OUT connector*

*NOTE: All pin definitions and connector types for the connectors on the back of the DRC are given in Appendix C.

CONTROLS AND INDICATORS

Turn the DRC power on with the front panel toggle switch.

Should be illuminated	Should not be illuminated
The Microprocessor 1, 2, 3, and 4 OK LEDs	The 8 LEDs to the right
The TRIGGER, LOCKOUT, and ARM LEDs	

Do the following:

. Turn the LOCAL/REMOTE switch to the down position (the LOCAL LED should extinguish)

. Move the switch to the up position (the LED should illuminate)

The DRC is now in local mode; this means some of the DRC selection may be made from the front panel switches.

Do the following:

. Turn the DATA STREAM/ACE switch to the up position (the DATA STREAM/LED should illuminate)

. Move the switch to the down position (the LED should extinguish)

The triggered data is now available to the ACE from the DRC data port.

Do the following:

. Move the FORMAT leverwheel switch through its four positions. (The LED should read: 1, 2, 3, and 4.)

. Move the BIT RATE leverwheel switch through its four positions (The LEDs should read 2.5, 5, 10, and 20 MHz.

Do the following:

. Set the TEST OPTION leverwheel switch (located to the left of the BIT RATE switch) to Position 1 and press the reset button. (The TRIGGER, LOCKOUT, and ARM LEDS should extinguish.)

This resets the range timing countdown time signals and does a full power up.

Table 4 shows the power-up test options that are run when power is first applied, or when the reset button is active while the front panel test option switch is set at one of the positions in the table. These options are run only once.

Table 4. Power-up Test Options

0- NORMAL POWER-UP SEQUENCE
1- RESET COUNTDOWN TIMING SIGNALS AND DO A FULL POWERUP
2- RESERVED
3- SAVE DEFAULT DIGITIZER SETUPS (SAME SETUPS SAVED IF THE INTERNAL MEMORY FORGOT)
4- SAVE DEFAULT DIGITIZER CHANNEL NUMBERS (SAME NUMBERS SAVED IF THE INTERNAL MEMORY FORGOT)
5- RESERVED
6- RESERVED
7- RESERVED

Table 5 shows the normal test options that are run when the DRC is powered up. These options are then selected from the front panel. That option will run repeatedly until another option has been selected.

Table 5. Normal Test Options

0 - SHOT POSITION (CHECKS DIGITIZER'S SETUP CONTINUOUSLY)
1 - SET DIGITIZERS TO LOCAL
2 - SEQUENTIALLY DOWNLOAD SETUP INFORMATION INTO EACH DIGITIZER FROM THE SET-UP PARAMETERS CONTAINED IN THE DRC MEMORY
3 - CONTINUOUSLY ALLOW FOR REPETITIVE RATE SIMULATION. AFTER RECEIVING A TRIGGER, REQUEST THE DIGITIZERS TO DIGITIZE DATA AND DUMP RAW, THEN IT RESETS THE RANGE TIMING SIGNAL AND TRIGGER CIRCUIT AND WAITS FOR ANOTHER TRIGGER
4 - SEQUENTIALLY REQUEST EACH DIGITIZER FOR SET-UP PARAMETERS AND SIGNIFY ANY ERRORS ON THE FRONT PANEL LEDs
5 - SEQUENTIALLY REQUEST EACH DIGITIZER FOR RAW DATA AND SIGNIFY ANY ERRORS ON THE FRONT PANEL LEDs
6 - LOAD AN INCREMENTING PATTERN INTO EACH DIGITIZER'S MEMORY IN THE DRC THROUGH THE GPIB CONTROLLER AND HIGH SPEED GPIB CIRCUITRY. DO A CHECKSUM ON THE DATA AND DISPLAY ANY ERROR ON THE FRONT PANEL LEDs
7 - REQUEST DATA AND SET-UP PARAMETERS FROM THE DIGITIZERS, DO A CHECKSUM ON THE INFORMATION, AND DISPLAY ANY ERRORS ON THE FRONT PANEL LEDs

Table 6 shows special test options. These options are selected with the aid of the front panel test option switch and the microswitch (on Board 3, 3CJ91) turned in the off position.

Table 6. Special Test Options

0 - SHOT POSITION
1 - ENABLE DIGITIZER 1 ONLY
2 - ENABLE DIGITIZER 2 ONLY
3 - ENABLE DIGITIZER 3 ONLY
4 - ENABLE DIGITIZER 4 ONLY
5 - SEQUENTIALLY SELECT EACH READ REGISTER AND STROBE THE CLOCK INPUT. SEQUENTIALLY SELECT EACH WRITE REGISTER AND WRITES AN INCREMENTING COUNT TO THE REGISTER OUTPUT
6 - LOOP INCREMENT PATTERN DIRECTLY INTO SCOPE MEMORY AND DISPLAY ANY ERRORS ON THE FRONT PANEL LEDs
7 - RETURN ALL DIGITIZERS TO ACTIVE STATE. MUST BE RUN AFTER RUNNING SPECIAL OPTIONS 1, 2, 3, OR 4

Running Options

- Run the options in Table 6. After running Options 1-4, run Option 7 to turn on all digitizers

- Run the options in Table 5. Connect the logic analyzer to the GPIB connectors on the back of the DRC to verify the options are running correctly. If a logic analyzer is not available, Options 4-7 will display any errors on the LEDs on the front panel. The interpretation of the flashing LEDs are explained in Section 2 of this manual.

Reading the Data Into the DRC Memory

. Complete the test options,
. Move the test option switch to Position 0
. Send the -5min range timing signal

In about 30 s, the DRC should shoot a baseline for each of the TEK7912 digitizers. The digitizer's configuration are then returned to their normal settings and the data is read into the DRC memory.

. Wait 4.5 min.
. Send the -30 s range timing signal (the LOCKOUT LED should illuminate)

. The DRC will read the scopes' setup parameters and stores them for output with the data
. The DRC commands the digitizers to digitize data and dump raw data.

. Wait 29 s
. Send the -1 s range timing signal (the ARM LED should illuminate)

Do the following:

. Send the trigger signal from the trigger generator (the TRIGGER LED should illuminate). Be sure to trigger the TEK7912 digitizer.

. The DRC delays internal circuitry for 16 ms
. The DRC requests raw data from the TEK7912 digitizers
. About 90 ms after the trigger, the DRC should contain the data from the TEK7912 digitizer.

Do the following:

. Reset the DRC with the TA703 range timing unit
. Run the options in the ACETEST menu to verify that the link between the ACE and the DRC is working.

OPERATING INSTRUCTION

Do the following:

. Verify all the installation has been followed as specified by the preceding section.

. Connect the following to the DRC:
  . TEK7912 digitizers
  . Range Timing Unit
  . ACE.

Do the following:
. Turn on the DRC
. Push the reset button.

The DRC is now ready to receive the range timing signals and to be triggered.

APPENDIX A

Definition of the Command Link Format and Codes

Appendix A describes the Command Link from the ACE to the DRC.

Communicating Bytes to and from the DRC

The DRC contains four processors that may independently (but not simultaneously) receive commands and data. The processors may also be directed to output data to the ACE. Prior to communicating with any processor in the DRC, the ACE should check to see that the desired processor is ready to receive or send a byte. Since each processor has a one-byte transmit buffer and a one-byte receive buffer, it is important to prevent sending a new byte before the old byte has been accepted. A status register has been provided for this purpose.

The Status Register

The status register provides two pieces of information on each processor; Data Available (DAV) and Buffer Empty (BE). To access the status register, the ACE must set the Command Link lines to the following codes, then assert the strobe (N) line.

ACE to DRC Command Link STATUS READ.

	(binary)	(lsb on right)
function code	1110	
address	xxxx	
subaddress	xxx1	

When the status register is read, the bits are interpreted as follows.

D7				BITS				DO	
DAV	BE	DAV	BE	DAV	BE	DAV	BE		
D	D	C	C	B	B	A	A		

DAV When 0, a byte of data is in the buffer. When the ACE reads the data from the buffer, this signal automatically goes to a 1.

BE When 0, indicates that the receive buffer is empty and a byte may be written to the buffer. When a byte is written to the buffer by the ACE, the BE flag goes to a 1.

Writing a Byte to the DRC

Prior to writing data to the DRC, the ACE must check the DRC's status register to ensure that the DRC is ready to receive a byte (BE is 0).

To write a byte to the DRC, the ACE merely places the byte on the data lines, sets the control lines to the state indicated below, and asserts the strobe (N) line.

ACE to DRC Command Link DATA WRITE.

	(binary) (lsb on right)
function code	1101
address	ppcc
subaddress	xxx0

The pp is the desired processor number from the list below.

Processor A	00
Processor B	01
Processor C	10
Processor D	11

And cc is the desired channel number in any given processor's domain.

Channel 0	00
Channel 1	01
Channel 2	10
Channel 3	11

Note that the channel number is not latched into the DRC, but is available to the processors via a standard input port. If the channel number is to be used, the processor must first read the channel number port, and then the actual data byte buffer. This sequence is important because when the data byte buffer is read it automatically clears the BE bit in the status register. The ACE must keep the address lines valid until the processor indicates that it has accepted the data byte (BE will go 0).

Reading a Byte from the DRC

Prior to reading a byte from the DRC, the ACE must check the DRC's status register to ensure that the DRC has a valid byte ready for the ACE (DAV is 0).

To read a byte from the DRC, the ACE sets the control lines to the state indicated below and asserts the strobe (N) line.

ACE to DRC Command Link DATA READ.

	(binary)	(lsb on right)
function code	1110	
address	ppxx	
subaddress	xxx0	

The pp is the desired processor number from the list below.

processor A	00
processor B	01
processor C	10
processor D	11

When the data is read, the DAV flag for the processor read, will be automatically reset to a 1.

Interrupting Processors via the Command Link

The ACE may issue an interrupt to any one of the DRC's processors via the Command Link. An interrupt may be used to indicate to the processor that a communication is about to take place.

To issue an interrupt to the DRC, the ACE sets the control lines to the state indicated below and asserts the strobe (N) line.

ACE to DRC Command Link PROCESSOR INTERRUPT.

	(binary)	(lsb on right)
function code	1100	
address	ppxx	
subaddress	xxxx	

The pp is the desired processor number from the list below.

processor A	00
processor B	01
processor C	10
processor D	11

COMMAND MESSAGE FORMAT

The messages to and from the Command Link shall adhere to the SANDUS command message format except as specified herein.

message byte no.	message changes
1	The capability to send variable length messages has been added. The message length bits are all 1's to indicate a variable length transmission. If the message length is to be variable, the exact length of the message (byte count) shall be provided in bytes 8 and 9 of the header. The exact byte count shall be the actual number of data bytes to be transferred excluding all header and check bytes (LRC). The number of bytes expected to be returned must be in byte positions 10 & 11. The byte positions 8 & 9 contain the number of "good" bytes read from the DRC.
2	no change
3	ELEMENT ADDRESS: DRC channels 0 - 77 (octal) 0 - 17 (octal) is DRC no. 0. 20 - 37 (octal) is DRC no. 1. 40 - 57 (octal) is DRC no. 2. 60 - 77 (octal) is DRC no. 3. The common equipment bit must be set to 1. Each DRC talks to 16 scopes. Bits 0 & 1 identify the channel number; Bits 2 & 3 identify the processor number; and Bits 4 & 5 identify the DRC number.
4	CMD LNK FUNCTION CODE/SUBADDRESS: not used for the DRC.
5	DRC OPERATION CODE: Up to 8 bits in length. Unused msb's must be set to 0.
6	DRC CHANNEL NUMBER: not used. Information now obtained from byte 3.

7	7912 SECONDARY ADDRESS: The lower nibble identifies which unit of the 7912 is to receive/transmit the message. Base = 0, V-amp = 1, Time base = 2. The upper nibble indicates the error status. A 0 indicates normal command termination, 1 to 3 indicate ACE errors, 4 to 7 indicate DRC errors, 8 to 15 indicate 7912 errors. If the upper nibble is not 0, then the returned data bytes contain error messages (if any) and bytes 10 & 11 contain the error message byte count.
8	TX BYTE COUNT 1: The more significant byte of the transmit byte count starting from byte 13 and excluding the checksum (LRC).
9	TX BYTE COUNT 2: The less significant byte of the transmit byte count starting from byte 13 and excluding the checksum (LRC).
10	RX BYTE COUNT 1: The more significant byte of the receive byte count starting from byte 13 and excluding the checksum. The DRC shall respond with a message of exactly this length. If the data to be transferred from the DRC to the ACE is shorter than this length, the DRC shall pad-out the message to achieve the exact length. The actual number of "good" data bytes shall be returned in bytes 8 and 9.
11	RX BYTE COUNT 2: The less significant byte of the receive byte count starting from byte 13 and excluding the checksum. The DRC shall respond with a message of exactly this length. If the data to be transferred from the DRC to the ACE is shorter than this length, the DRC shall pad-out the message to achieve the exact length. The actual number of "good" data bytes shall be returned in bytes 8 and 9.
12	RELATIVE DELAY: The relative delay time between transmission of command message bytes from ACE back to VAX. 0 is for fastest transmission. 1 if the DCSs are in the command link path. 2 don't use.
13	start of data bytes
n	last data byte
n+1	check byte (lrc)

The following is a list of the DRC operation codes and their meaning. The codes are passed in byte 5 of the command header. The codes and their meanings are listed below (in decimal).

OPERATION CODE (byte 5)		
octal	hex	
0	0	NOT USED
1	1	SET-UP WITH ACCEPTANCE OR REJECTION. Indicates that a set-up string is to follow. The string is to be issued to the 7912 "as is". After issuing the string, the DRC shall issue the "SET?" command to the 7912. The string returned from the "SET?" command shall be passed to the ACE "as is". The DRC shall make a copy of the string in a temporary buffer. The DRC will wait until the ACE sends an "ACCEPTANCE" before marking the string as valid. The DRC rejects the string if: 1) A reject is sent. 2) If anything other than an accept is sent.
2	2	SET-UP WITHOUT ACCEPTANCE OR REJECTION. Indicates that a set-up string is to follow. The string is to be issued to the 7912 "as is". No checks on the 7912 will be made. The string is not saved in DRC memory.
3	3	READ DRC SET-UP PARAMETERS. The string in the DRC's parameter set-up area is sent to the ACE via the command link.
4	4	LOAD DRC SET-UP PARAMETERS. The data in the message string is to be copied to the DRC's parameter set-up area.
5	5	QUERY 7912. Indicates that a query string is to follow. The string is to be issued to the 7912 "as is". The DRC shall pass the string returned from the 7912 back to the ACE "as is".
6	6	COMMAND 7912
12	A	START GENERAL CALIBRATION. Indicates that a calibration process should be started on all channels available to this processor.

octal hex

13 B PERFORM CALIBRATION ON 1 CHANNEL.
Indicates that one or more calibration steps are to be performed on the channel specified in the DRC CHANNEL NUMBER (byte 6). Each data byte in the command message shall indicate the calibration step number.

20 10 RESET SINGLE SCOPE.

21 11 INITIALIZE SINGLE SCOPE FROM DRC PARAMETERS.

22 12 DOWNLOAD ALL PARAMETERS TO THE DRC FROM THE SELECTED 7912 SCOPE

24 14 DRC RESET
Resets all internal registers in order to allow the DRC to perform another dry run.

27 17 MASTER RESET
Master reset will return all setups to the DRC's internal default settings. For the master reset to be successful, the following data pattern must also be sent in the message: (byte 13- 132 octal 5A hex) (byte 14- 245 octal A5 hex) (byte-15 74 octal 3C hex) (byte-16 303 octal C3 hex).

35 1d ABORT CURRENT OPERATION.
The current operation being performed by the specified processor shall be terminated.

36 1e ACCEPTANCE.
Indicates that the last string transferred from the DRC to the ACE contains proper set-up information and the string is considered valid.

37 1f REJECTION.
Indicates that the last string transferred from the DRC to the ACE does not contain proper set-up information and the string should be considered invalid. [The DRC will write the last valid string to the 7912 in an attempt to keep the 7912 loaded with valid settings].

50 28 READ 7912 GPIB ADDRESS.

51 29 SET 7912 GPIB ADDRESS.

octal	hex	
144	64	TRANSFER RAW DATA. From TEK7912 to DRC.
156	6e	TRANSFER RAW DATA From DRC to ACE to VAX via Command Link.
170	78	TRANSFER RAW DATA From TEK7912 to ACE to VAX via Command Link.
171	79	TRANSFER RAW DATA From TEK7912 to ACE to VAX via GPIB.
310	c8	DRC ECHO INCOMING MESSAGE. The incoming message is echoed from the DRC "as is". This is primarily a diagnostic aid.
320	d0	ACE ECHO INCOMING MESSAGE. The incoming message is echoed from the ACE "as is". This is primarily a diagnostic aid.
321	d1	ACE FORWARD DATA FROM INCOMING MESSAGE TO GPIB. This is mainly for calibration of instruments via GPIB.
330	d8	READ DRC R/W REGISTER. The DRC R/W status register contents are returned in byte 13 of the command message. This is primarily a diagnostic aid.
360	f0	DRC SELF TEST. The DRC shall perform internal diagnostics and report on its health. The returned message shall indicate the processor's health. A two-byte return message consisting of 55 hex and AA hex shall indicate that no internal errors were detected.
361	f1	EXECUTE INTERNAL CHECKOUT OF DRC

APPENDIX B

Setup of DRC Default Parameters

Appendix B identifies the method that will be used to control which TEK7912 digitizers the DRC will communicate with and what set-up parameters it will use in the default mode.

Guidelines for selecting active Digitizers

The DRC was designed to handle sixteen TEK7912 digitizers, with the four microprocessors handling 4 digitizers each. In certain situations, not all sixteen digitizers are needed. The microprocessors should be programmed to identify which digitizers are not active, otherwise it will spend valuable time trying to communicate with the missing digitizers even if they are not connected to the GPIB bus.

Two files must be edited to implement these changes: the DRC.S and the ASSEMBLY.OBT. After changes are made in the file DRC.S, it must be assembled and linked again. The file ASSEMBLY.OBT is called by the assembler when it assembles DRC.S, therefore, it needs to be changed first before assembling the file DRC.S.

The file ASSEMBLY.OBT will contains four variables: 1) speed, 2) debugflg, 3) lab and 4) fivepack. The variable speed informs the microprocessors of its clock rate, either 6.25 Mhz or 12.5 Mhz. The variable debugflg allows certain test routines to run during the initial checkout of the DRC. The variable lab sets microprocessor 1 to communicate with digitizers at channels 0 thru 3; microprocessor 2 with channels 4 thru 7; microprocessor 3 with channels 10 thru 13; and microprocessor 4 with channels 14 thru 17; or it will set all microprocessors to communicate with digitizers at channels 14 thru 17 only. The variable fivepack is used to identify where the DRC is located in a system of multiple digitizers.

Once ASSEMBLY.OBT has been set up, edit the file DRC.S and proceed to the subroutine called resetchadd. In the file ASSEMBLY.OBT, the variable fivepack was used to identify the location of the DRC; in this routine it will tell the microprocessor what digitizers are located in this rack. When the variable fivepack is set to 0, all sixteen digitizers are active. Other values for fivepack are at the programmer's discretion and must be changed for the situation at hand.

The first thing to determine is where the DRC will be used and with which digitizers it will be communicating. Inside the routine and toward the middle of the code is an instruction which moves -1 into D0. After this instruction, the fivepack is defined. First, find the microprocessor from which you wish to eliminate some digitizers. The variable UPIDNUMBER will contain this information; 0,1,2 and 3 stand for microprocessor numbers 1,2,3 and 4, respectively. The microprocessor can tell if a digitizer is active by examining a location in the memory.

The variables ACTCHREG1, ACTCHREG2, ACTCHREG3 and ACTCHREG4 contain this address for each of the four digitizers. ACTCHREG1 is for digitisers set at channel addresses 0,4,10 or 14; ACTCHREG2 for addreses 1,5,11 or 15; ACTCHREG3 for addresses 2,6,12 or 16; and ACTCHREG4 for addresses 3,7,13 and 17 depending on the microprocessor. To disable a digitizer, a -1 must be written in this location instead of the channel number.

Figure B1 demonstrates how to disable the digitisers at channels 3 and 17 of fivepack 1.

```
          MOVE    #-1,D0          ;GET READY TO DISABLE SOME CHANNELS

++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++

     IF   FIVEPACK=1              ;DIGITIZERS 3 AND 17 IN THIS FIVEPACK
          CMPI.L  #0,UPIDNUMBER   ;SEE IF FIRST PROCESSOR, FOR CHANNEL 3
          BNE     RESETCHADD220   ;IF NOT, SEE IF FOURTH PROCESSOR
          MOVEA.L #ACTCHREG4, A0  ;IF YES, BRING IN CHANNEL 3 ADDRESS
          JSR     CHLOAD          ;CALL THIS ROUTINE TO LOAD CHANNEL 3
                                  ;WITH A DUMMY CHANNEL NUMBER, -1

SETCHADD220 CMPI.L #3,UPIDNUMBER  ;SEE IF FOURTH PROCESSOR, FOR CHANNEL 17
          BNE     RESETCHADD500   ;IF NOT, BRANCH TO END OF ROUTINE
          MOVEA.L #ACTCHREG4, A0  ;IF YES, BRING IN CHANNEL 17 ADDRESS
          JSR     CHLOAD          ;CALL THE ROUTINE TO LOAD CHANNEL 17
                                  ;WITH A DUMMY CHANNEL NUMBER, -1
ENDIF
```

Figure B1. Example for Setting Channels 3 and 17 to Dummy Channel.

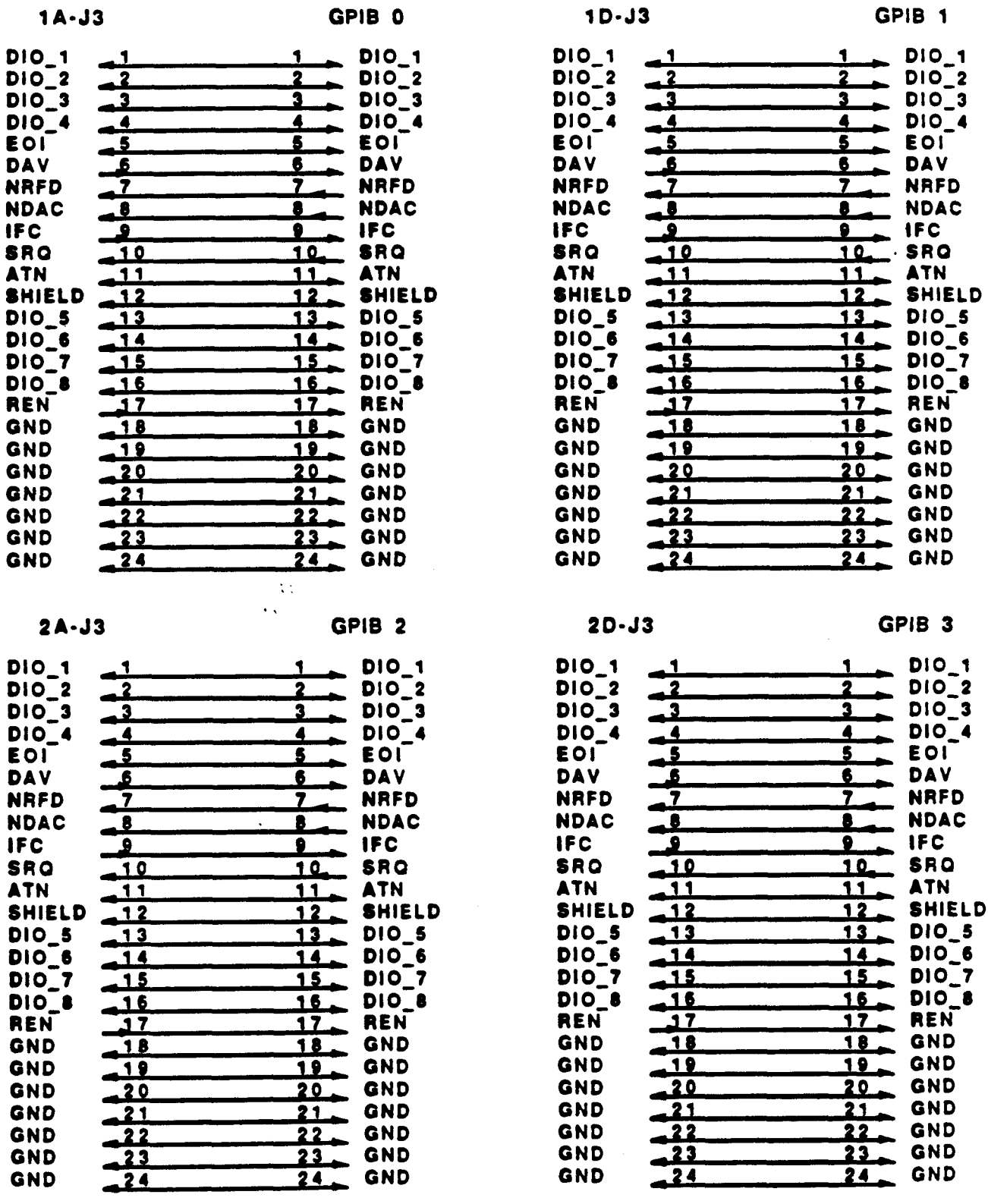
Guideline for Defining Default Parameters

When the memory test pattern fails, the value in the CMOS memory is concluded to be invalid. In this case the DRC will load the digitisers with some default set-up parameters stored in its PROMs. The stored ASCII code setting for different mainframes, vertical plug-ins, and horisontal plug-ins, are located at the end of the DRC.S file.

To set up each digitiser's default setting, edit the file DRC.S and go to the subroutine called resetscsu. Find the right fivepack processor, and digitiser in this code; change the set up by substituting the correct ASCII code for the setting that the digitiser will default to, and assemble the file DRC.S.

APPENDIX C

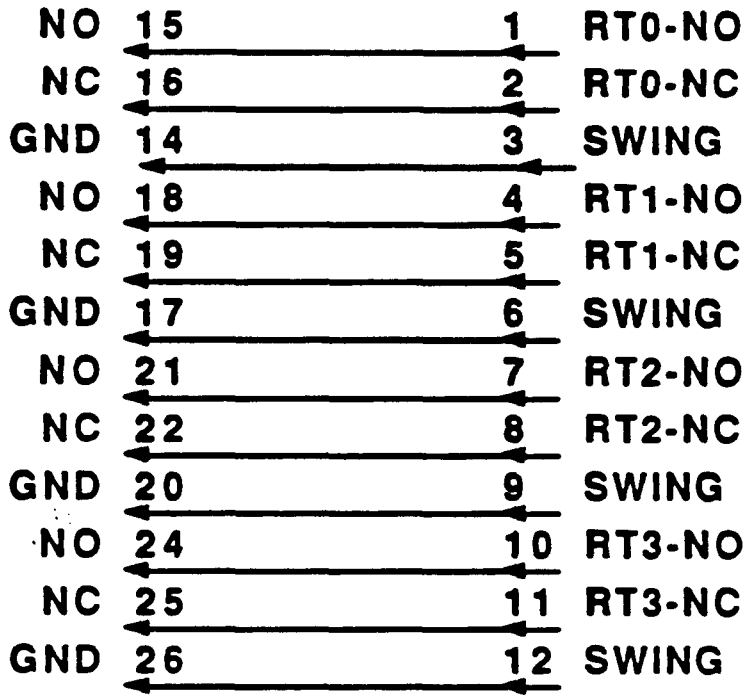
DRC Connector Definition



AMPHENOL 57-40204 CONNECTOR

TA705 Rear Panel Range Time Signals

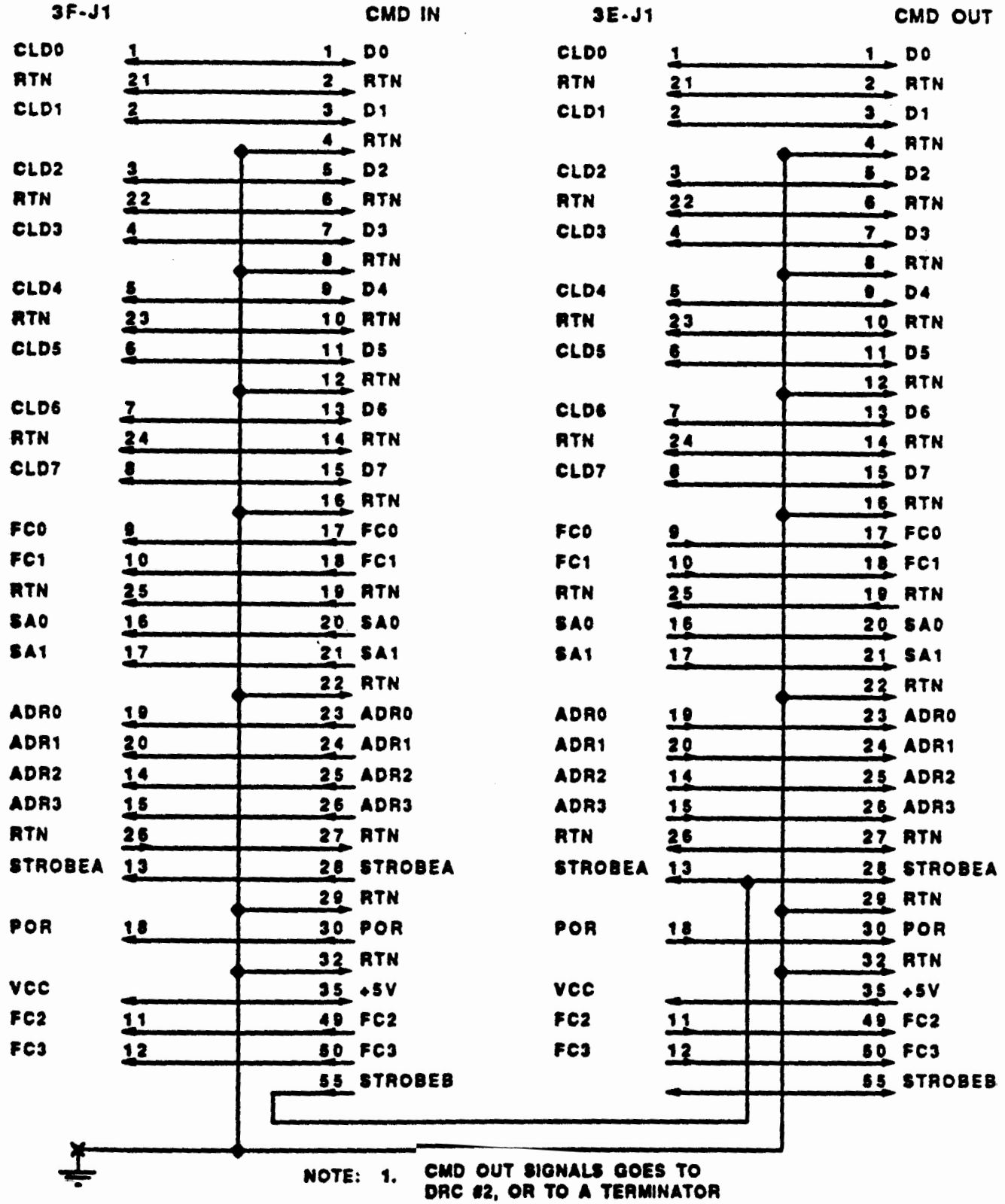
3C-J1



3D-J3

AMP: CONNECTOR 205843-1
PINS 66507-9
CRIMPER 90302-1

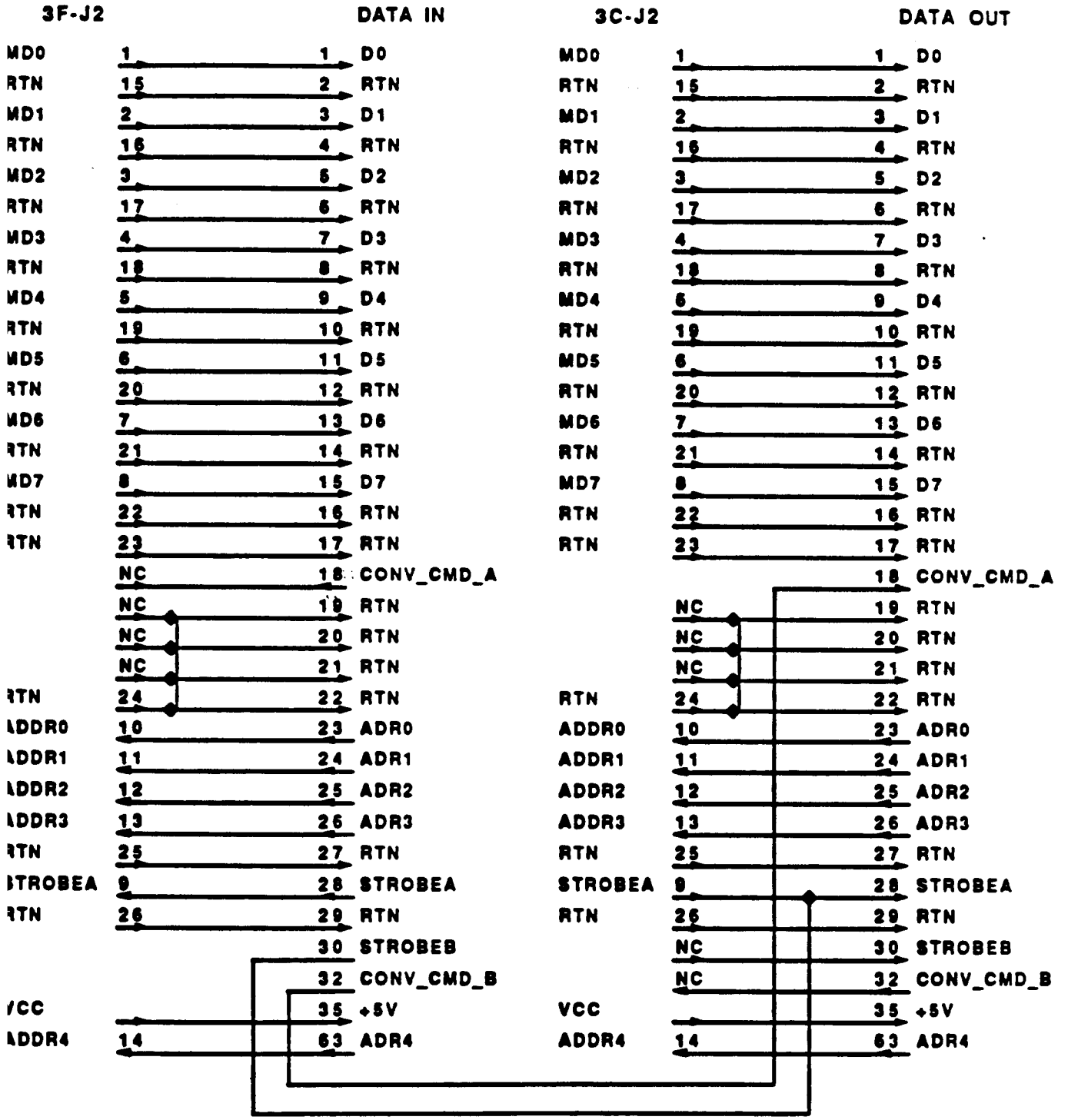
TA705 Rear Panel CMD Link I/O



NOTE: 1. CMD OUT SIGNALS GOES TO DRC #2, OR TO A TERMINATOR

AMP: CONNECTOR 205843-1
PINS 66507-9
CRIMPER 90302-1

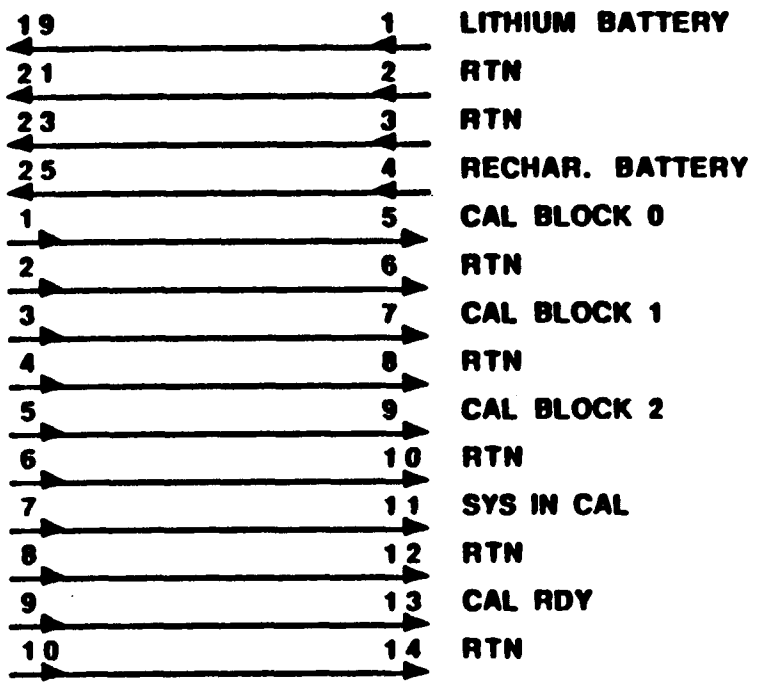
TA705 Rear Data Link I/O



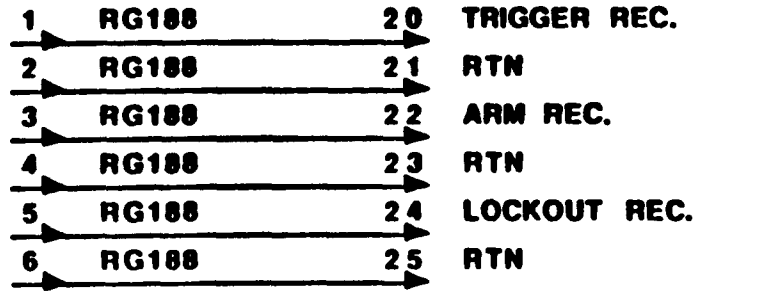
NOTE: DATA OUT SIGNALS GOES TO DRC #2, OR TO A TERMINATOR

AMP: CONNECTOR 205843-1
PINS 66507-9
CRIMPER 90302-1

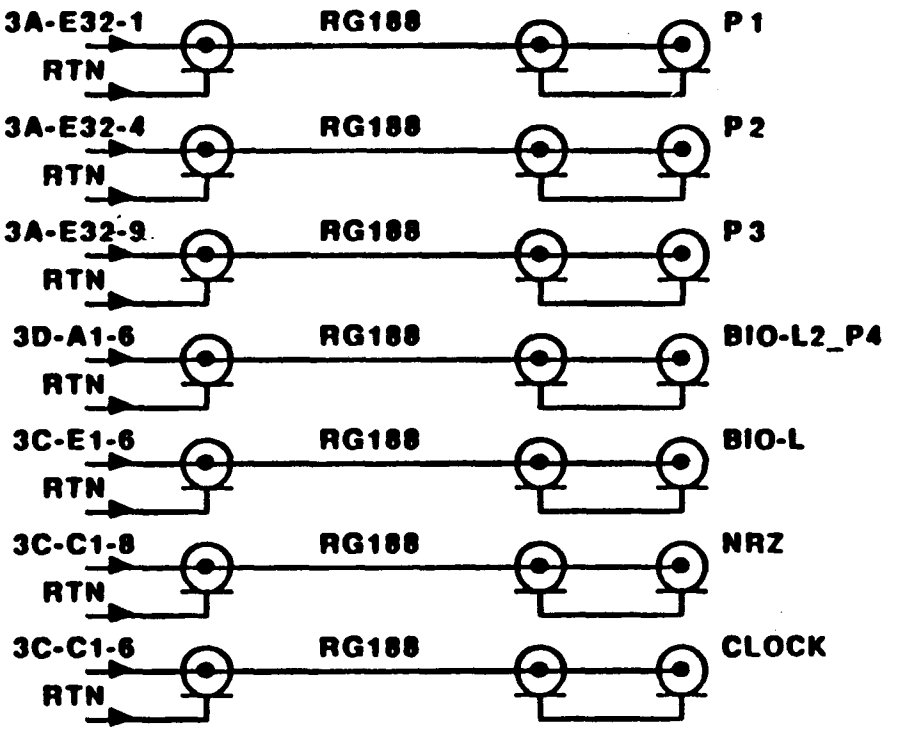
3B-J1 SPARE OUT



3D-J3 SPARE OUT



BNC CONNECTORS



NOTE: 1. PUSH ON PINS AT BOTTOM OF BOARD

AMP: CONNECTOR 205843-1
PINS 66507-9
CRIMPER 90302-1

APPENDIX D

List of Drawings for the TA705 DRC

List of drawings for the TA705 DRC.

Drawing Number	Title
S62715	TA705 DRC Assembly
CK S62715	TA705 DRC Schematics
S76191	TA705 Chassis Modifications
S77997	TA705 Back Panel Spacer

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	8524	J. Wackerly