4.40
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OR. 1036

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PHASE 2 OF THE AUTOMATED ARRAY ASSEMBLY TASK OF THE LOW-COST SILICON SOLAR ARRAY PROJECT

Technical Quarterly Report No. 4, April 1—June 30, 1979

By
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Work Performed Under Contract No. NAS-7-100-954847

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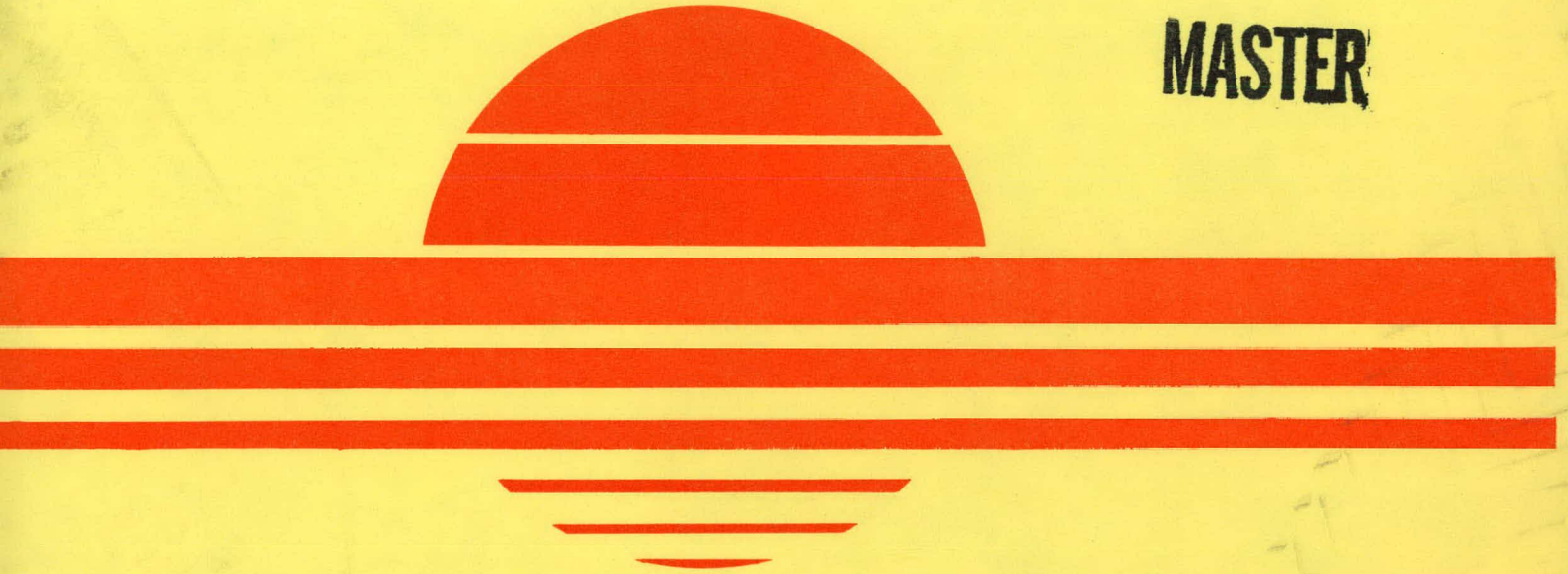
Phoenix, Arizona



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PHASE 2 OF THE AUTOMATED ARRAY ASSEMBLY TASK

OF THE LOW-COST SILICON SOLAR ARRAY PROJECT

TECHNICAL QUARTERLY REPORT NO. 4

1 APRIL 1979 - 30 JUNE 1979

MOTOROLA REPORT NO. 2345/5

JPL CONTRACT NO. 954847

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THE JPL LOW-COST SOLAR ARRAY PROJECT IS SPONSORED BY THE U.S. DEPARTMENT OF ENERGY AND FORMS PART OF THE SOLAR PHOTOVOLTAIC CONVERSION PROGRAM TO INITIATE A MAJOR EFFORT TOWARD THE DEVELOPMENT OF LOW-COST SOLAR ARRAYS. THIS WORK WAS PERFORMED FOR THE JET PROPULSION LABORATORY, CALIFORNIA INSTITUTE OF TECHNOLOGY BY AGREEMENT BETWEEN NASA AND DOE.

PROJECT NO. 2345

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1.0 SUMMARY

Following a substantial delay in funding, this contract was again fully funded in April. This report covers the reduced efforts during the end of 1978 and work initiated in April, 1979.

During this period, all tasks progressed according to scheduled plans. This report highlights the process verification efforts, ion implantation investigations, plasma etching, and cost factors in the metallization processes. Specifically, several items were discussed. Completed modules were delivered to JPL to demonstrate the process sequence. A surface film has been observed on ion implanted wafers which has tentatively been associated with break-down of the vacuum pump oil during implantation. A baseline process for plasma patterning of silicon nitride on a silicon substrate has been specified. In addition, copper has been shown to have strong cost advantages over other metals for a conductor layer; and nickel has been identified as a desirable barrier between copper and silicon.

2.0 INTRODUCTION

There is a high probability that flat plate solar photovoltaic modules will become a major source of electricity generation throughout most of the world, and that the silicon solar cell will be the preferred generating element. In order to provide a realistic framework on which to build an effective program of R&D and demonstration for silicon solar cell modules, a series of objectives has been established to lead to a 1986 goal of 50¢/peak watt. At this price, solar-generated electricity will be able to compete with electric power generated by any other means, provided the solar cell modules are sufficiently reliable (e.g., have a mean life of 20 years).

To reach the 1986 JPL goal will require several advancements: 1) a cheaper source of pure silicon, 2) a much more economical way of transforming the source silicon into large, thin, (essentially) single crystal substrates having a controlled geometry, 3) an economical, large module package that will protect the interconnected solar cells it contains for at least 20 years from degradation caused by exposure to the weather, 4) an automated process sequence that produces high efficiency, reliable, cheap solar cells, tests them, interconnects them, and encapsulates them, and 5) a large market, of the order of 500 Mw/year.

When the JPL/ERDA LSSA Project started, the Motorola Solar Energy R&D Department participated in the Phase I of the Automated Array Assembly Task. The Phase I study identified a few potentially powerful process sequences for silicon solar cell production, and experimentally verified the overall consistency of the process sequence. It concluded that no basic technological innovations were necessary for solar cell fabrication or encapsulation in order to meet the long range LSSA Project goals. Detailed economic analyses

were performed, based on today's technologies, and showed that it should be possible to meet the JPL cost projections for solar panels.

The overall conclusion of the Array Automated Assembly Task, Phase 1, was one of cautious optimism. The present program, for Phase 2, has as its objective the further development of specific process steps (in a particular, powerful process sequence) leading to a completely specified solar cell (and module) production process sequence. This sequence must be capable of a high degree of automation and control. A detailed economic analysis is a major part of the program to ensure that the most cost-effective approach is taken.

During the first part of the Phase II program, feasibility of the process sequence and its individual process steps were confirmed. This, the second part of the Phase II program, is concerned with specification of process control parameters and limits which will allow progress toward automation of the process sequence. The main objective of this contract is sufficient process control limit definition to permit advanced equipment prototypes to be designed for incorporation into an advanced pilot line facility.

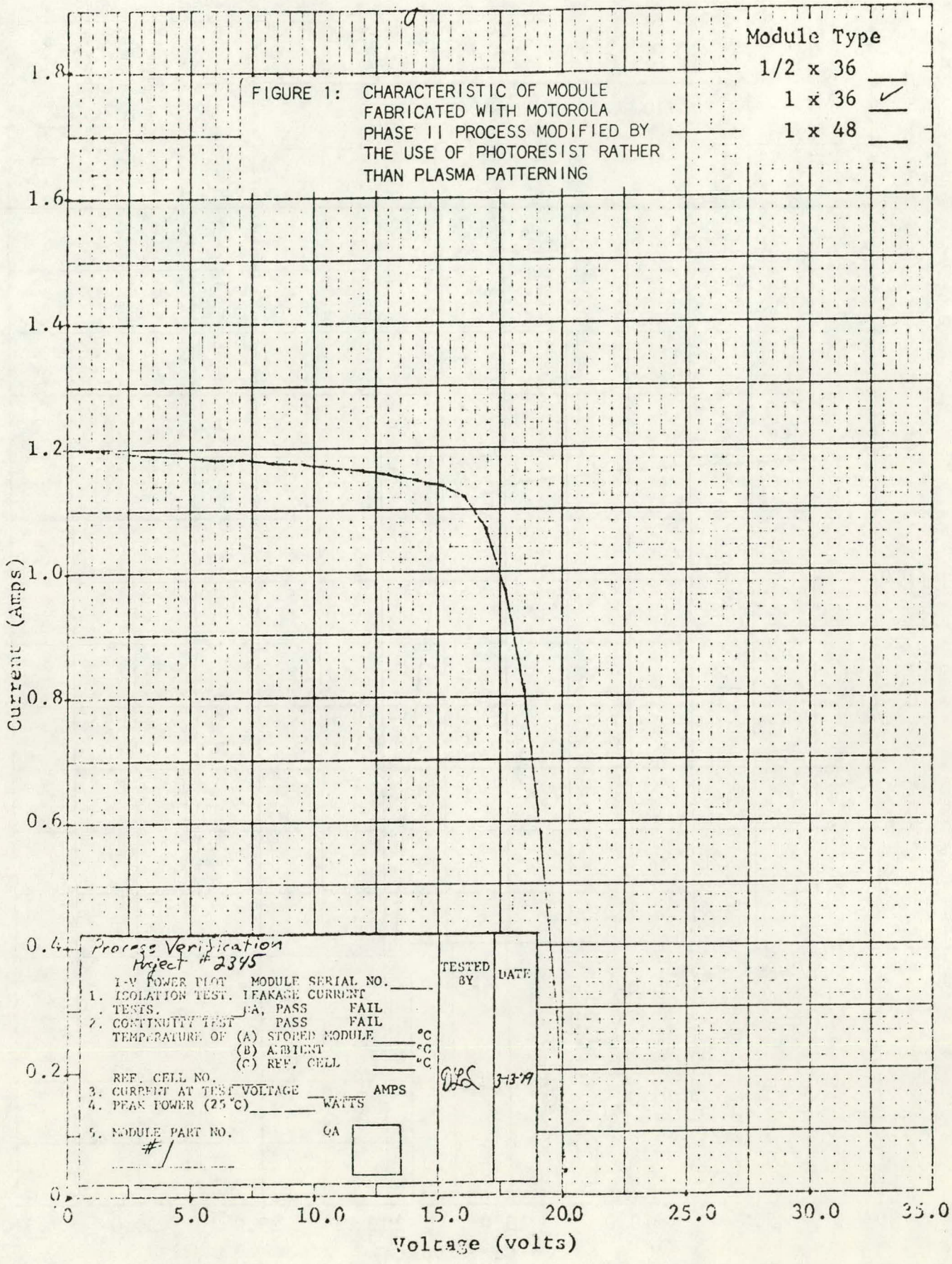
3.0 TECHNICAL DISCUSSION

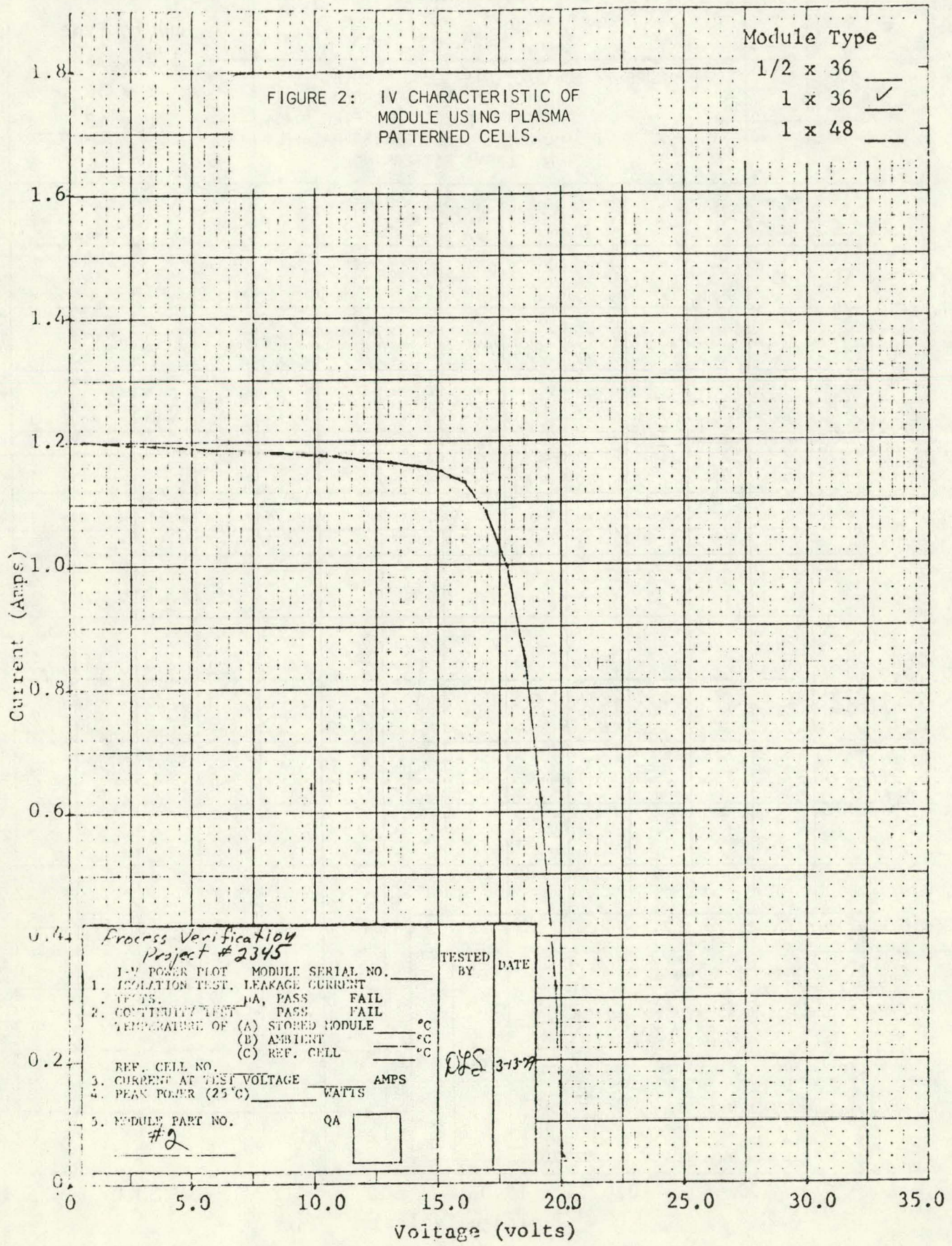
3.1 DEMONSTRATION MODULES

Variations of the Phase II process sequence were used to fabricate two demonstration modules. The modules were of the standard Motorola design with low-iron glass front covers, stainless steel backs, and silicone gel encapsulation. Thirty-six cells were series connected with flexible interconnects for each module. Under pulsed xenon AM1 simulation, the modules delivered a maximum power of approximately 18 watts with open circuit voltage (V_{OC}) of 20 volts and short circuit current (I_{SC}) of 1.2 amps. Characteristic curves for the modules are shown in Figures 1 and 2.

Up to the point of forming the metal contact pattern in the front surface antireflective Si_3N_4 coating, the cells for each module were processed in the same manner. Three inch wafers were first textured on both sides. Then a boron implant was performed on the back surface, followed by a phosphorus implant on the front surface. Both implants were perpendicular to the substrate (zero angle) at an energy of 35 KeV. The boron dose was 3.48×10^{15} cm^{-2} and the phosphorus dose was 1.74×10^{15} cm^{-2}. Since these implants were performed on textured surfaces, the machine doses above correspond to actual doses of 2×10^{15} cm^{-2} and 1×10^{15} cm^{-2}, respectively, on the (111) facets of the textured surface pyramids. This results because of the increased surface area of a textured surface over that of a smooth surface.

After ion implantation, boron and phosphorus electrical activation were achieved during the same 45 minute cycle during which the antireflective layer of silicon nitride (Si_3N_4) was deposited by a low pressure chemical vapor deposition (LPCVD) process at approximately 780°C. This simultaneous implant activation anneal and dielectric deposition cycle has been proven effective.


Module Type
1/2 x 36 ___
1 x 36 ✓
1 x 48 ___
FIGURE 1: CHARACTERISTIC OF MODULE FABRICATED WITH MOTOROLA PHASE II PROCESS MODIFIED BY THE USE OF PHOTORESIST RATHER THAN PLASMA PATTERNING
Current (Amps)
1.8
1.6
1.4
1.2
1.0
0.8
0.6
0.4
0.2
0
0
5.0
10.0
15.0
20.0
25.0
30.0
35.0
Voltage (volts)
Process Verification
Project #2345
I-V POWER PLOT MODULE SERIAL NO. ____
1. ISOLATION TEST. LEAKAGE CURRENT
TESTS. ____ μA, PASS FAIL
2. CONTINUITY TEST PASS FAIL
TEMPERATURE OF (A) STORED MODULE ____ °C
(B) AMBIENT ____ °C
(C) REF. CELL ____ °C
REF. CELL NO. ____
3. CURRENT AT TEST VOLTAGE ____ AMPS
4. PEAK POWER (25°C) ____ WATTS
5. MODULE PART NO. #1
QA
TESTED BY
DATE
3-13-79


Module Type
1/2 x 36 ___
1 x 36 ✓
1 x 48 ___
FIGURE 2: IV CHARACTERISTIC OF MODULE USING PLASMA PATTERNED CELLS.
Current (Amps)
1.8
1.6
1.4
1.2
1.0
0.8
0.6
0.4
0.2
0
0
5.0
10.0
15.0
20.0
25.0
30.0
35.0
Voltage (volts)
Process Verification
Project #2345
I-V POWER PLOT MODULE SERIAL NO.____
1. ISOLATION TEST. LEAKAGE CURRENT
TESTS. ___μA, PASS FAIL
2. CONTINUITY TEST PASS FAIL
TEMPERATURE OF (A) STORED MODULE____°C
(B) AMBIENT ____°C
(C) REF. CELL ____°C
REF. CELL NO.____
3. CURRENT AT TEST VOLTAGE ____ AMPS
4. PEAK POWER (25°C)____ WATTS
5. MODULE PART NO. #2
QA
TESTED BY
DATE
DPS 3-13-79

At this point, the cells used in module 1 were subjected to a photolithographic process to form the desired metal grid pattern in the front surface Si_3N_4 layer. This process requires coating with photoresist and then aligning, exposing, developing, and etching to open the metal contact areas. This is standard "semiconductor" procedure. On the other hand, the cells used in module 2 were patterned using the plasma etch process being developed for Phase II. This process requires simply placing a metal shadow mask over the cell front surface such that the patterned areas to be etched are exposed to the plasma. The entire etching process is accomplished in about three minutes with no expendable materials other than the gas (such as CF_4) used to create the reactive plasma.

All cells were then metal plated and soldered using the palladium-nickel-solder mettalization process. Cells were soldered to the flexible 36-cell interconnects by hand.

3.2 SILICON SURFACE LAYER CONTAMINATION DURING ION IMPLANTATION

It has been noted in the literature (1) that the ion implantation process can, in itself, be a source of surface contamination. Although the process is done in vacuum, residual partial pressures of hydrocarbons from diffusion pump oil can result in polymerized hydrocarbon films because of bombardment by the ion beam. Such films may change the etching properties of the silicon surface and, ultimately, may affect the quality and integrity of metal-semiconductor electrical contacts.

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(1)K. A. Pikar, "Ion Implantation in Silicon", Applied Solid State Science, Volume 5, R. Wolfe, ed., Academic Press, N. Y., 1975.

Ion implantation using large ion beam currents (in the milliamp range) may be especially susceptible to this surface contamination effect. In using the Varian/Extrion model 200-1000 high current machine to form solar cell junction and back surface enhancement layers, an etch resistance phenomenon has been repeatedly observed. Normally, clean silicon surfaces are hydrophobic, and rinse water will immediately run off the surface or will "bead-up" once the native silicon oxide layer has been stripped. However, wafers implanted with high doses in this high current machine will not display this tendency, implying that some surface contamination is present.

Such surface contamination may present production control problems, and a clean silicon surface in the ohmic contact areas is imperative if consistent metal-semiconductor contacts are to be produced. A recent paper in the literature (2) has addressed this problem. It has found that ion-induced carbaceous layers could be removed from the silicon surface by anodic oxidation with subsequent stripping in HF solution. This technique appears to satisfactorily restore the silicon surface cleanliness. (As long as the carbaceous layer and subsequent oxide growth are at most a few hundred Angstroms thick, the properties of the original silicon surface may not be altered significantly.)

We are investigating the use of thermal oxidation or plasma oxidation, followed by oxide stripping, to achieve the same cleaning effect. Oxide layers grown in the range from 250Å to 1000Å thick have been effective in restoring the hydrophobic nature of the silicon surface after stripping that oxide in dilute HF solutions. For a thermal oxide, growth can be accomplished during or after a thermal activation anneal cycle. This can be done in the same furnace tube or in a separate furnace tube. As for a plasma process, the only plasma

---

(2) M. Y. Tsai, et. al., "Study of Surface Contamination Produced During High Dose Ion Implantation," J. Electrochem. Soc.; Sol-St. Sci. and Tech., Vol. 126, No. 1, Jan. 1979, pp 98 - 102.

oxidation cycle considered to date provides about 40Å of SiO_2 at most. Therefore, this cycle must be repeated several times, stripping the oxide after each cycle, to effectively remove the carbonaceous layer.

The fact that a polymerized hydrocarbon film or carbonaceous layer is responsible for the unusual etching/cleaning characteristics of high dose, ion implanted wafers is assumed (but not proven) from the cited reports in the literature and the observation that the oxidation/strip technique sucessfully restores the surface. If this assumption is correct, the best processing response is to eliminate the effect in the first place, rather than to try to cure it afterwards. The possibility of using a different vacuum pump fluid has been suggested (2) and that possibility is being considered. This may substantially reduce the residual hydrocarbon content in the implanter vacuum chambers and may preclude the formation of a harmful carbonaceous layer.

3.3 COMPARISON OF STARTING MATERIALS THROUGH ION IMPLANTATION

A comparison of different ingot-grown starting wafers for ion implanted solar cells has been initiated. Wafers cut from both float zone and Czochralski ingots have been ion implanted and activation annealed for comparison. Early experiments indicated the possibility that float zone material was superior to Czochralski material. Accordingly, a more defined experiment has been performed to study the validity of the early results.

To minimize possible processing variables, bare, smooth, non-texture etched wafers have been utilized for the comparison. While a number of lots have been run, three representative groups are reported here. Each of the three groups consisted of 24 wafers. In each lot, one half (12) of the wafers were float zone wafers purchased from Wacker. These wafers

were utilized as controls for comparison between lots. The other half of each lot was comprised of Czochralski wafers from Wacker, Monsanto, and Motorola, respectively. All substrates were p-type, but various resistivity ranges were utilized.

Wafers were front ion implanted at 35 KeV with phosphorus at a dose of $2 \times 10^{15}/cm^2$. Back surface ion implants of 4×10^{15} boron were also performed. All wafers were then given a furnace activation anneal of 16 minutes at 850°C in a nitrogen ambient, followed by a 120 minute anneal in nitrogen at 550°C.

Open circuit voltage readings were recorded for each wafer under both room (fluorescent) lighting and a tungsten (ELH) simulation of 1-sun. The room light open circuit voltage gives an indication of the cell fill factor -- high values of room light V_{OC} indicate good fill factor. For these wafers, short circuit current readings were implied by measurement of the illuminated cells in reverse saturation. The results of these tests are shown in Table 1 as an average for each half lot.

These measurements indicate that, within experimental variations, all materials give comparable values of 1-sun parameters. A statistical difference is seen for the Czochralski material for room light open circuit voltage. Further processing of these cells through a silicon nitride antireflection coating and pre-metal patterning shows that the variation disappears at this stage of cell fabrication. For all practical purposes, thus, no basic differences have been observed between the various ion implanted materials.

3.4 METALLIZATION AND COST ANALYSIS

At the present time, two techniques for forming metal contacts on solar cells remain potentially viable from both cost and technical considerations: plating and

TABLE 1

COMPARISON OF ION IMPLANTED, SMOOTH-SURFACED MATERIALS

		BEFORE AR			WITH AR
		OPEN CIRCUIT VOLTAGE (VOLTS)		SHORT CIRCUIT CURRENT (milliamps)	OPEN CIRCUIT VOLTAGE (VOLTS)
LOT	MATERIAL	ROOM LIGHT V_{RL}	1-SUN V_{OC}	1-SUN I_{SC}	ROOMLIGHT V_{RL}
SD019	Wacker FZ 1.8 - 3.0 Ω-cm	.308	.564	1050	.391
	Wacker CZ 1.9 - 2.6 Ω-cm	.276	.563	1050	.423
SD020	Wacker FZ 1.8 - 3.0 Ω-cm	.310	.573	1085	.420
	Monsanto CZ 0.2 - 0.5 Ω-cm	.283	.573	1055	.440
SD021	Wacker FZ 1.8 - 3.0 Ω-cm	.338	.579	1115	.432
	Motorola CZ 0.8 - 2.0 Ω-cm	.145	.564	1125	.386

printing (silk screening). The plated metal process has now shown distinct advantages over the printed process.

The Pd_2Si - (Pd) - Ni - solder metallization system for silicon solar cells has been developed at Motorola. This system can be considered the baseline system which all other competing systems must strive to outperform. A full description of the Pd_2Si-(Pd)-Ni-solder metallization is available in DOE/JPL Report Number 954689-78/4, "Metallization of Large Silicon Wafers," Final Report for JPL Contract 954689.

The minimum cost achievable for any metallization system is limited by the cost of component materials. All printed metallization systems which have been satisfactorily utilized with solar cell structures (for contact to the shallow junction areas) are based on silver as the primary conductor. No printable base metal system has been reported to be satisfactory for utilization on solar cells. The Motorola plated metal system, discussed above, utilizes solder as the primary conductor. While solder can be broadly classed as a base-metal, it is relatively expensive. A conductor layer material such as copper would be much cheaper.

Some pertinent properties of potential conductor layer materials are presented in Table 2. Two important observations can be made. First, the conductivities of silver and copper are comparable, while solder is a relatively poor conductor. Second, in order to achieve a given conductivity for any given conductor geometry, 11% more silver, and over 800% more solder, (by weight), would be required compared to copper.

The cost of metals varies significantly as a function of time in a manner determined more by supply and demand factors than by inflation. For the basis of this discussion, the prices for the three metals were identified on March 29, 1979 and are presented in Table 3. On a weight basis, copper is significantly cheaper than solder and less than 1% of the cost of silver.

TABLE 2

COMPARISON OF SELECTED PROPERTIES OF METAL CONDUCTOR LAYERS

	SOLDER (60SN-40PB)	COPPER	SILVER
RESISTIVITY (Micro Ohm-cm)	14.5	1.673	1.59
DENSITY (g/cm^3)	8.53	8.96	10.49
RELATIVE WEIGHT PER UNIT CONDUCTIVITY	8.26	1.0	1.11

TABLE 3

COST* OF CONDUCTOR METALS ON MARCH 29, 1979

	SOLDER** (60SN-40PB)	COPPER	SILVER
COST PER POUND	4.67	1.00	104.22

*BASED ON PURE METAL COMPONENT COSTS

**DOES NOT INCLUDE ALLOY FORMATION COSTS

When the cost per pound of a metal is correlated with the weight requirement for a unit conductivity, the cost of a metal as a conductor can be determined. Utilizing the 3-29-79 prices, solder is about 40 times as expensive as copper, while silver is about 115 times as expensive as copper. On a cost basis, thus, copper is extremely attractive as the primary conductor metal on solar cells.

Copper plating technology exists for metallic surfaces. In the Motorola plated metal system, it appears possible to replace solder with copper. The effect of copper on cell performance and reliability must be examined, however, before substitution can be assured.

3.5 METALLIZATION RELIABILITY

Any solar cell metallization for terrestrial applications must, in addition to being sufficiently economical, provide both excellent electrical performance and ensure reliability under actual operating conditions. Numerous candidates exist which will provide suitable electrical performance, but which fail the reliability criterion. In order to perform reliably, the solar cell metallization must both maintain excellent adherence to the solar cell and, at the same time, not contribute to degradation of the electrical characteristics.

A severe criterion would be that tho only satisfactory adherence test of a metallization system for solar cells is a mechanical pull-test which shows no separation of metal layers and which guarantees that separation of the metal from the cell is accomplished by silicon fracture. (Motorola's palladium silicide-nickel-solder metallization system satisfies this criterion.)

During operation, for a minimum of a 20 year life, the metallization must not contribute to a significant loss in output power from the solar cells. Such a loss could occur either from an increased series resistance, due to such phoenomenona as corrosion or metal migration, or from degradation of the

silicon cell behavior, such as could occur by diffusion of the metal into the silicon. Diffusion of metal into the silicon could cause degradation of minority carrier lifetime in the silicon, decreasing cell efficiency. From all tests performed to date, the Pd_2Si-(Pd)-Ni-solder system appears suitable from these standpoints.

The substitution of copper for solder as the primary conductor layer in the metallization system would result in substantial materials cost savings. Substitutic of copper for solder should have no impact on metal adhesion, but copper can have a degrading effect on cell electrical performance if it accumulates near the p-n junction.

The diffusion of copper in silicon is extremely rapid at low temperatures. While copper present in silicon before device processing can be gettered or precipitated (3), copper penetration following any high temperature processing, such as from cell metallization, can significantly degrade cell efficiency (4).

Diffusion kinetics can generally be described by an Arrhenius type relation,

$$D = D_o e^{-\frac{Q}{RT}}$$

where D is the diffusion coefficient, D_o is the pre-exponential or frequency factor, Q is the activation energy, T is absolute temperature, and R is the gas constant. The penetration of a limited amount of impurity into another species at one temperature can be approximated by a gaussian distribution

$$C = C_o e^{-\frac{x^2}{nDt}}$$

(3) A.M. Salama, "The Effects of Copper and Titanium on Silicon Solar Cells," The Conference Record of the Thirteenth IEEE Photovoltaic Specialists Conference - 1978, p. 496, 1978.

(4) T. Daud and K. M. Koliwad, "Effect of Copper Impurity on Polycrystalline Silicon Solar Cells," Ibid, p. 503.

where C is the concentration of the impurity at distance x, C_o is the surface concentration, D is the diffusion coefficient, t is the time of the diffusion, and n is a constant determined by the diffusion geometry. On the other hand, if the source of impurity is infinite, penetration is described by

$$C = C_o \operatorname{erfc} \frac{x}{\sqrt{nDt}}$$

A measure of impurity penetration for either case can be taken as the distance $\sqrt{Dt}$. Further, at a distance of 10 $\sqrt{Dt}$, vanishingly small amounts of the impurity will be found. A suitable diffusion barrier, thus, has a thickness of at least 10 $\sqrt{Dt}$.

In operation, the solar cell will be subjected only to maximum temperatures near 100°C. Unfortunately, no diffusion data exist for copper in silicon for this temperature range, requiring extrapolation from higher temperature data. Such an extrapolation, however, does not appear unreasonable.

Diffusion of copper in siliocn has been studied for the temperature range of 400°C (5). These data are approximately reproduced in Figure 3 and extrapolated to the lower temperatures of interest. From this figure, diffusion coefficients for copper in silicon in the range of 50°C to 120°C have been determined and are shown in Table 4. These data have been utilized to calculate the distance $\sqrt{Dt}$ for copper in silicon at these temperatures for a time of 20 years, Table 5. These distances are on the order of 1 cm in this time-frame, a distance which virtually ensures copper throughout a silicon solar cell operating for 20 years. Thus, cell degradation is virtually ensured during the required operating life if copper is allowed direct contact to silicon.

(5) R.M. Hall, et. al., Final Report, AFCRL Report 62-533, Contract AF 19 (604)-6623, May, 1962, as quoted in Fundamentals of Silicon Integrated Device Technology, Volume 1, Oxidation, Diffusion, and Epitaxy, Edited by R.M. Burger and R.P. Donovan, p. 235, 1967.

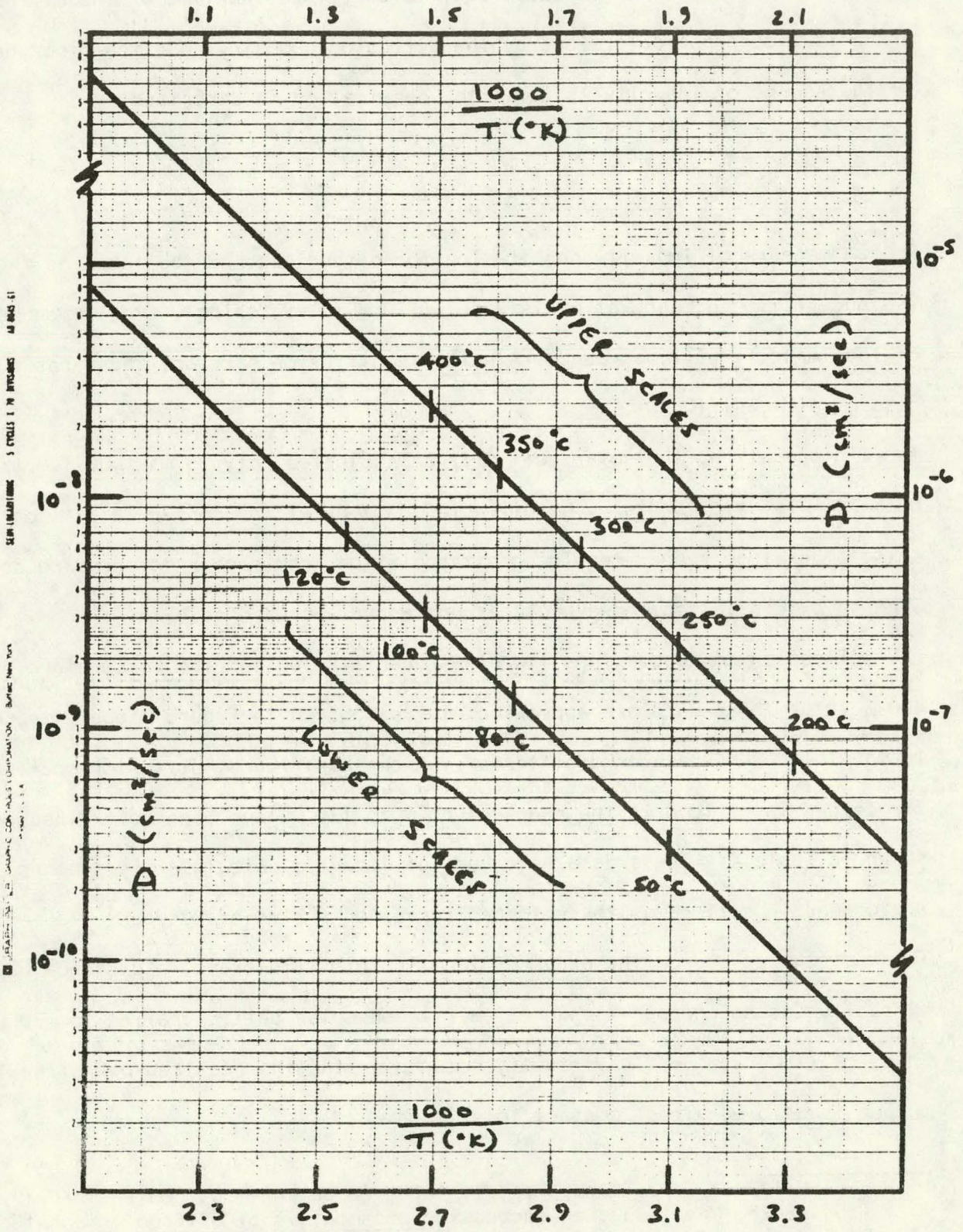


FIGURE 3 EXTRAPOLATION OF DIFFUSION DATA FOR COPPER IN SILICON.

TABLE 4

EXTRAPOLATED DIFFUSION DATA FOR COPPER IN SILICON[5]

TEMPERATURE T (^{o}C)	DIFFUSION COEFFICIENT D (cm^2/sec)
50	3.0×10^{-10}
80	1.35×10^{-9}
100	3.15×10^{-9}
120	6.7×10^{-9}

TABLE 5

PENETRATION OF COPPER IN SILICON FOR A PERIOD OF 20 YEARS

TEMPERATURE T (°C)	DISTANCE $\sqrt{Dt}$ (cm)
50	0.44
80	0.92
100	1.4
120	2.1

It is apparent, thus, that a barrier to copper diffusion into silicon is required to ensure cell reliability. Nickel appears to be ideal for this purpose. Diffusion data for copper and nickel have been compiled (6), and representative data are presented in Table 6. Again, extrapolation of high temperature diffusion data is required. Both copper and nickel exhibit complete mutual solid solubility, and both have face-centered-cubic crystal structures. Extrapolation of diffusion data for face-centered-cubic materials over large temperature ranges has proven satisfactory due to the extreme dominance of diffusion by a single vacancy mechanism in these materials. The extrapolation is primarily dependent upon the accuracy of the high temperature data.

The diffusion data for copper and nickel, shown in Table 6, are reasonably self-consistent. There is, however, sufficient scatter to make precise extrapolations unreliable. Precise diffusion distances are not necessary to determine the suitability of nickel as a diffusion barrier for copper; a general range is satisfactory. Accordingly, typical data, rather than specific high accuracy data, will be utilized.

Typical data for diffusion of copper into nickel and nickel rich alloys of copper and nickel can be approximated from the data in Table 6. For this purpose, values have been chosen as follows:

$$Q = 60 \text{ K cal/g. atom}$$

$$D_o = 1.5 \text{ cm}^2/\text{sec.}$$

Utilizing these numbers, values for diffusion coefficients, D, and diffusion distances, $\sqrt{Dt}$, have been calculated, Table 7. From these calculations, it can be seen that $\sqrt{Dt}$ is vanishingly small at 100°C. If 20 years storage occurred at 300°C, $\sqrt{Dt}$ would be 10^{-7} cm or 10^{-3} micrometer. This means that at 300°C, $10\sqrt{Dt}$ would be only 100 angstroms in 20 years. Nickel is, thus, an

(6) John Askill, Tracer Diffusion Data for Metals, Alloys, and Simple Oxides, 1979.

TABLE 6

REPRESENTATIVE DIFFUSION DATA FOR COPPER AND NICKEL [6]

BULK MATERIAL	DIFFUSING SPECIES	ACTIVATION ENERGY Q (kcal/g.atom)	FREQUENCY FACTOR D_c (cm^2/sec)	TEMPERATURE RANGE (°C)
Copper	Cu^{64}	48.2	0.33	863 - 1057
Copper + 1 wt% Ni	Cu^{64}	48.9	1.86	780 - 890
Copper + 21.5 at % Ni	Cu^{64}	55.3	1.9	863 - 1112
Nickel + 45.4 at % Cu	Cu^{64}	50.3	2.3	985 - 1210
Nickel + 13 at % Cu	Cu^{64}	63.0	1.5	1054 - 1360
Nickel	Cu^{64}	61.3	0.65	850 - 1360
Copper	Ni^{63}	69.2	2.22	900 - 1200
Copper + 21.5 at % Ni	Ni^{63}	49.7	0.063	930 - 1113
Nickel + 45.4 at % Cu	Ni^{63}	60.3	2.3	985 - 1210
Nickel + 13 at % Cu	Ni^{63}	74.9	33	1054 - 1360
Nickel	Ni^{63}	60.5	9.96	1000 - 1400

TABLE 7

CALCULATED DIFFUSION DATA FOR COPPER INTO NICKEL, UTILIZING ASSUMED VALUES OF Q = 60 k cal/g.atom AND D_o = 1.5 cm /sec

T (°C)	D (cm^2/sec)	$\sqrt{Dt}$ (cm)
t = 20 years		
100	7.8×10^{-36}	7×10^{-14}
200	2.2×10^{-28}	3.7×10^{-10}
300	1.6×10^{-23}	1×10^{-7}
t = 30 min		
300	1.6×10^{-23}	1.7×10^{-10}

extremely effective diffusion barrier to copper. If processing interconnection or encapsulation requires times as long as 30 minutes at a temperature near 500°C, the nickel is still an extremely effective barrier. Copper substitution for solder in the Motorola plated metal system appears both technically and economically possible. Experimental efforts are continuing.

3.6 PLASMA ETCHING PROCESSES

A baseline process sequence has been established for the plasma patterning process, and applied to textured surfaces. From this baseline, variations will be performed to improve producibility, reproducibility, and control of the plasma patterning technology. That technology is aimed at selectively and simultaneously etching ohmic contact patterns into the silicon nitride on both sides of a silicon substrate without significantly etching the silicon surface beneath those ohmic areas.

To date, the best pattern definition and selectivity have been achieved by etching in what is referred to as the "reactive ion etching" mode. In this mode, the wafer to be patterned is placed on top of the same electrode to which RF energy is applied. A plasma is struck between that electrode and the surrounding walls of the vacuum chamber, which is at ground potential. The plasma is established at low pressure, less than 0.1 Torr. The RF electrode is capacitively coupled to the RF power supply and will float to a negative DC bias with respect to the plasma potential. This establishes an electric field which can accelerate ions from the plasma to the surface of the wafer supported on the RF electrode. This effect enhances the anisotropy of the plasma etching reaction and helps promote good line definition and mask opening replication without etching beneath the masked areas.

A baseline plasma patterning process sequence is described in the following paragraphs.

A steel shadow mask with openings where the silicon nitride is to be etched away is mechanically aligned to the front surface of a silicon nitride coated solar cell. The cell and mask are placed on a sheet of flat ceramic magnets which serve to hold the steel mask in registration with the cell surface.

The magnetic plate, cell, and mask assembly is positioned in a vacuum chamber on the RF electrode plate. (Plate area is 196 cm^2.) The electrode and chamber are preset at a temperature of 50°C.

The chamber is closed and pumped down to below 0.05 Torr. This requires about 30 seconds.

When pump-down is complete, RF power (100 watts at 13.56 MHz) and etchant gas flow (approximately 1 cm^3/min.) are started simultaneously to generate the plasma. In work to date, a gas mixture of 8% oxygen in Freon 14 (CF_4) has been used. The plasma is maintained for four minutes.

At the completion of the etch cycle, the RF power and etchant gas flow are stopped, the chamber is vented with nitrogen, and the wafer removed.

This process yields excellent replication of the etch mask openings. In fact, due to the nature of the reactive ion plasma and the metal mask, the line openings etched in the silicon nitride are typically a few tenths mil smaller than the line openings in the steel mask. Presently, the masks being used for experiments have approximately 5 mil line openings.

This process can be performed without degrading solar cell electrical characteristics. This has been shown by direct comparison of solar cells whose only difference in processing was the ohmic patterning step. Plasma patterned cells have been compared with those patterned by conventional photolithographic techniques using photoresist to protect against buffered HF etching. Both patterning processes can yield high quality solar cells.

This must imply that even though the CF_4-O_2 gas mixture is capable of etching silicon as well as silicon nitride, any silicon etching which occurs while clearing (patterning) the silicon nitride is not significant.

This implication is confirmed by the etch rate data presented in Figure 4. These data were taken at the same pressure, temperature, and flow rate as given above for the baseline process. Both etch time and RF power were varied. Bare silicon wafers were protected with photoresist so as to expose silicon areas in the shape of a metal grid pattern. After plasma etching, etch depths into the silicon were measured with a mechanical instrument similar to a profilometer. It can be noted that, under these conditions, silicon etch rates at 100 W RF power are small enough so that even for the case of 100% overetching (etching to clear Si_3N_4 in 4 min., then etching Si for an additional 4 min.), only 0.08 μ of silicon surface would be lost. Note that these data imply that the etch rates for SI and for Si_3N_4 are very similar for this particular process. Of course, such a large amount of overetching is not required in the actual process.

Although to date a CF_4 + O_2 mixture has been used satisfactorily, there are other gas mixtures available which promise greater selectivity of etch rates for Si_3N_4 over Si. Two particular gases, CHF_3 and a mixture of SiF_4 + O_2, have been obtained and may prove to be more desirable than CF_4 mixtures for the patterning process. Evaluation of these gases will be reported in the future.

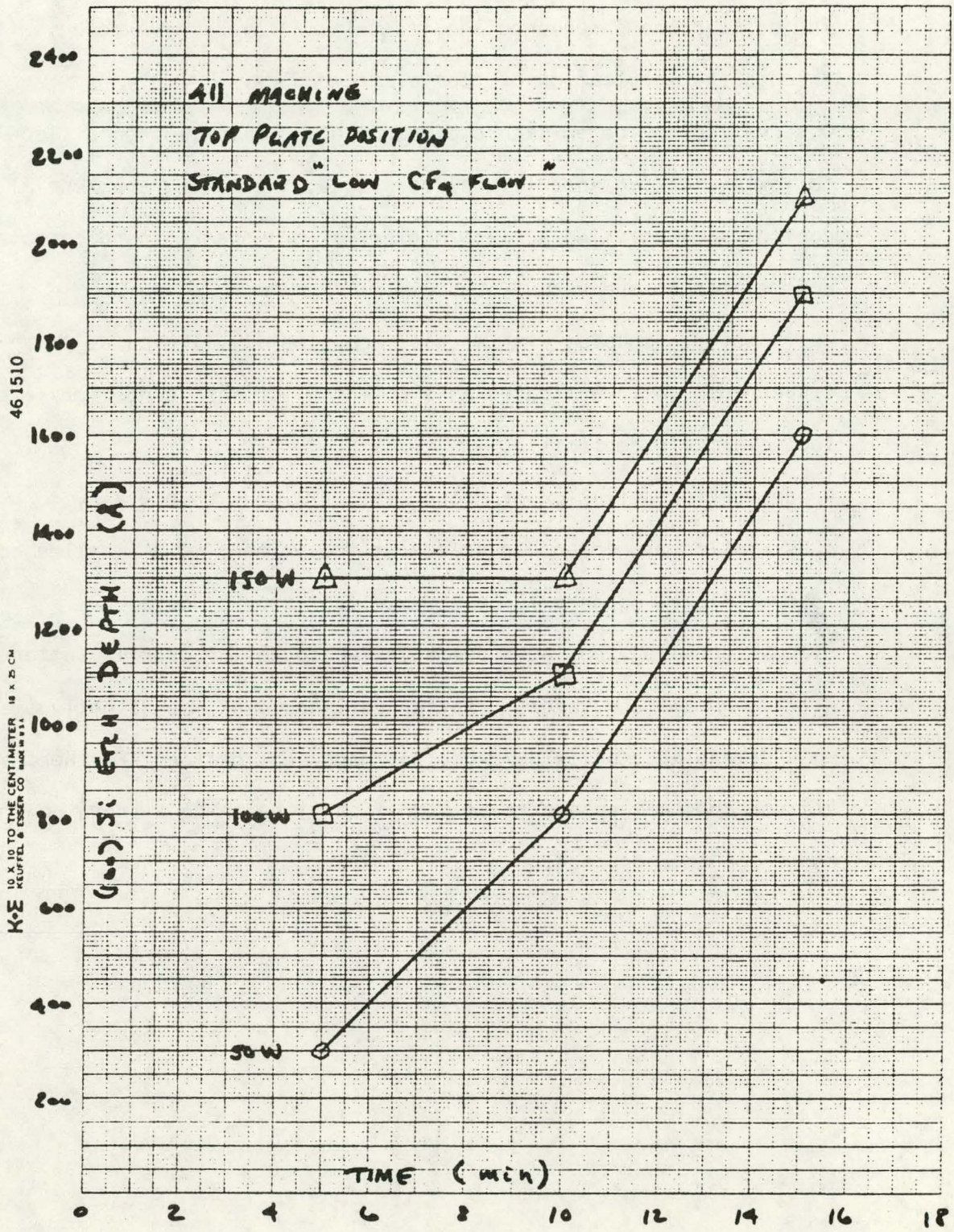


FIGURE 4: SILICON ETCH RATE DATA FOR BASELINE REACTIVE ION ETCHING MODE.

4.0 CONCLUSIONS

Several conclusions can be drawn from the progress during this period.

1. The basic process sequence and its critical steps have been verified through the fabrication of flat plate modules.
2. Observation of the existence of surface contamination on silicon following ion implantation has been made, indicating a potential control problem. The surface contamination appears to be carbonaceous and related to the vacuum pump oil.
3. Cost analysis coupled with process compatability indicates that copper must be investigated as a potential primary conductor layer for solar cell contacts.
4. A barrier for diffusion of copper into silicon is necessary for substitution of copper for solder as the primary metallization conductor layer. Nickel appears to be an excellent barrier metal.
5. Plasma technology has been demonstrated to satisfactorily pattern silicon nitride on silicon wafers. Patterned linewidths are slightly smaller than mask dimensions, allowing excellent mask replication. Further, etching of silicon does not appear to be significant, defining a broad control range for this process.

5.0 RECOMMENDATIONS

No specific recommendations can be made at this time.

6.0 CURRENT PROBLEMS

No current problems have been identified.

7.0 WORK PLAN STATUS

Work is progressing according to plan.

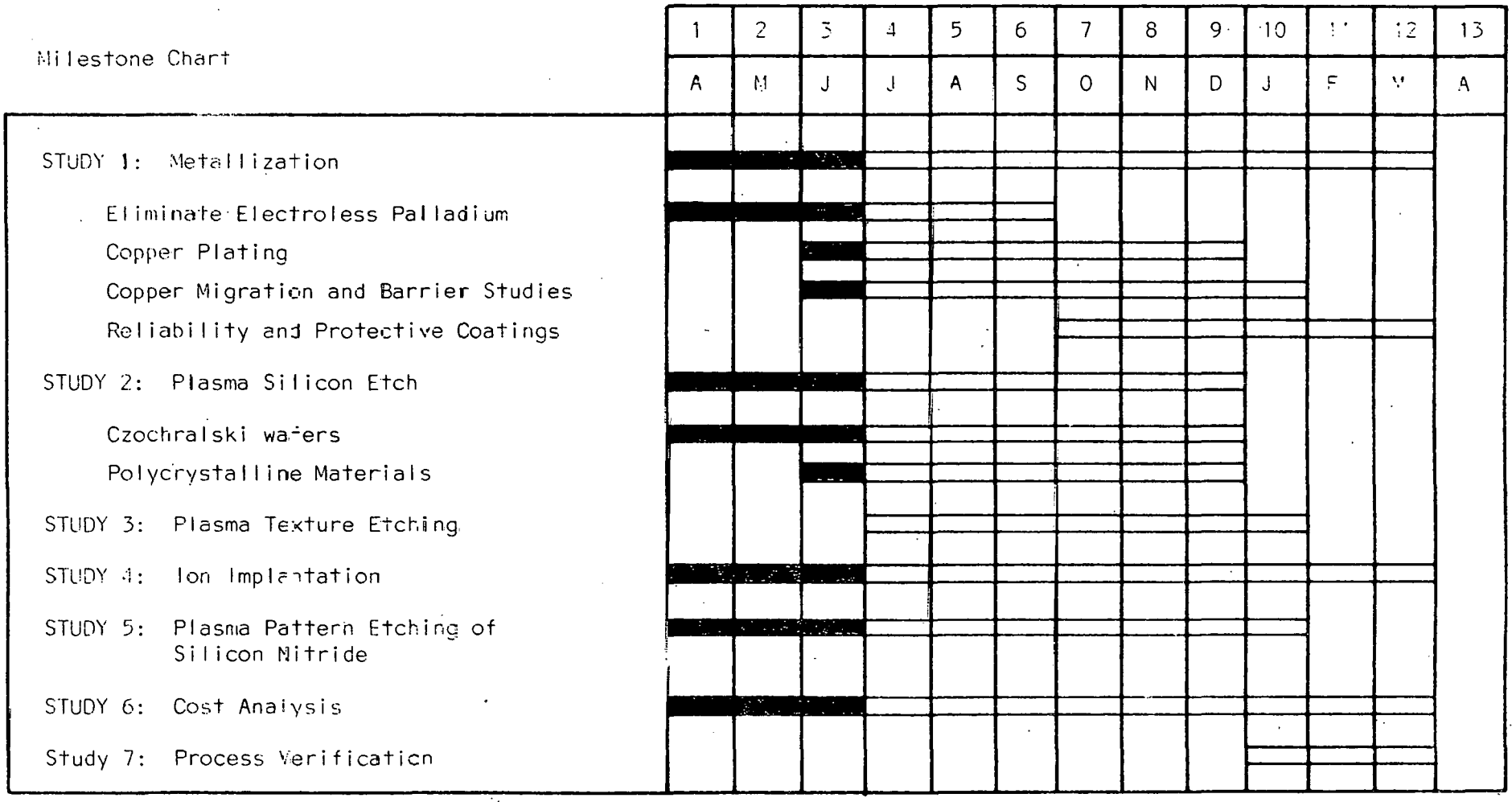
8.0 LIST OF ACTION ITEMS

No items requiring unusual action have come to light during this report period.

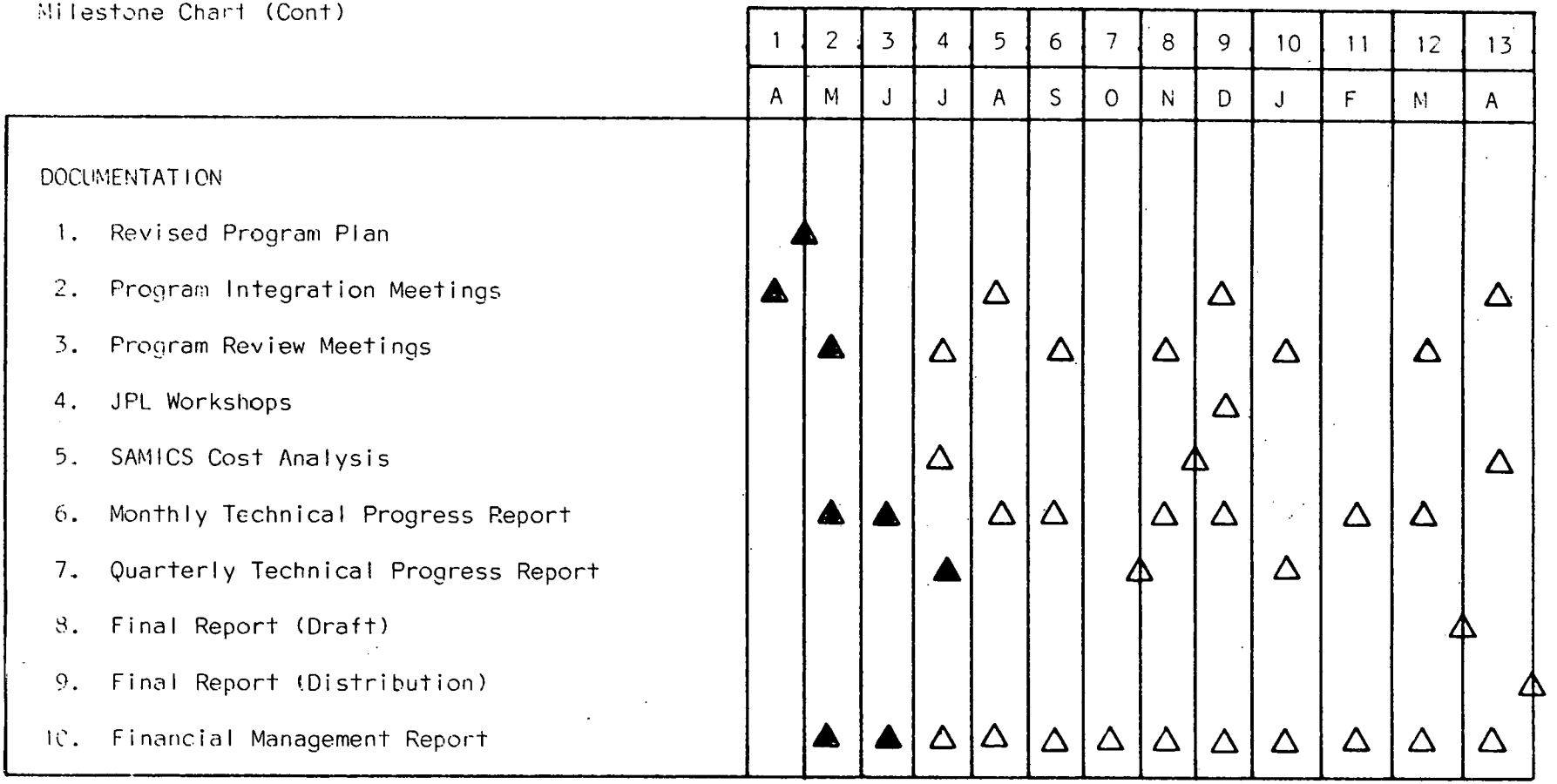
9.0 MILESTONES

Status of program is shown in the Milestone Chart.

Milestone Chart



Milestone Chart (Cont)



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