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THE DATA ACQUISITION SYSTEM FOR SLD*

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ABSTRACT

This paper describes the data acquisition system planned for the SLD detector which is being constructed for use with the SLAC Linear Collider (SLC). An exclusively FASTBUS front-end system is used together with a VAX-based host system. While the volume of data transferred does not challenge the band-width capabilities of FASTBUS, extensive use is made of the parallel processing capabilities allowed by FASTBUS to reduce the data to a size which can be handled by the host system. The low repetition rate of the SLC allows a relatively simple software-based trigger. The principal components and overall architecture of the hardware and software are described.

1. INTRODUCTION

SLD is a large solenoidal detector being constructed for use with the SLAC Linear Collider (SLC), and is expected to begin operation in 1989. The detector will be used to study e^+e^- collisions at energies up to 100 GeV, and is being designed to give 97% of full solid angle coverage with good tracking resolution, particle identification, and electromagnetic and hadronic calorimetry. A schematic cross section of one quadrant of the detector is shown in Fig. 1. The principal elements of the detector include:

- A vertex detector at a radius of 1-3 cm from the beam, consisting of 220 CCD chips, and a total of 50 million pixels with 22 μm spacing.

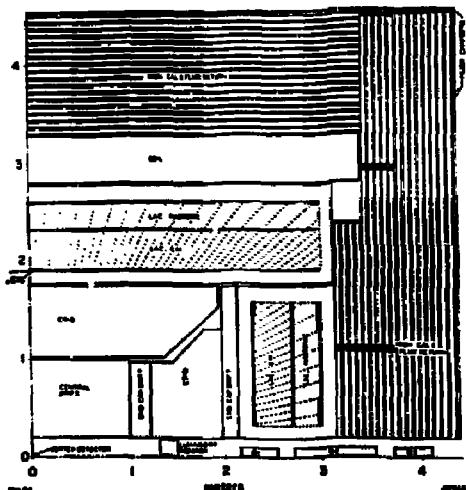


Fig. 1. Cross-section view of one quadrant of the detector.

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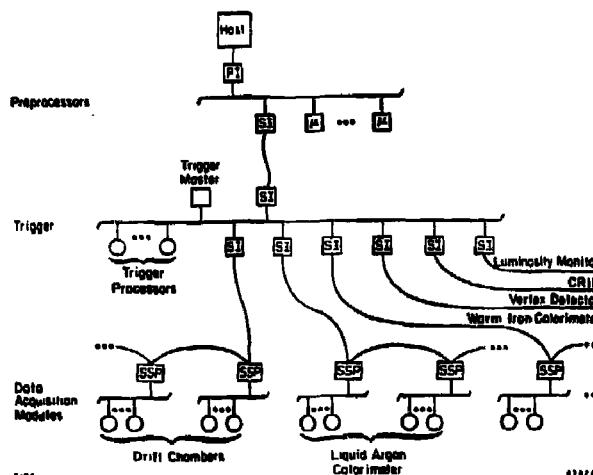


Fig. 2. PASTBUS configuration.

algorithms are changed. This approach significantly reduces the amount of offline processing required and also provides the online analysis, which must operate on a sampling basis, with tags to identify events of interest.

2. THE SLAC SCANNER PROCESSOR¹ (SSP)

The SSP serves the dual functions of acting as a "poor-man's Segment Interconnect" and as a fast processor. It is capable of acting as master (or slave) on either the crate or cable PASTBUS segment. However, it may only be attached to one segment at any one time, and data passed through the SSP must be buffered through its memory (with SSP program intervention).

Characteristics of the processor include:

- A 32-bit integer cpu using 2901C bit-slice technology.
- Emulation of the IBM System/370 instruction set with additional PASTBUS instructions.
- 120 nsec cycle time.
- PASTBUS DS to DK or DK to DS response times of 90 nsec.
- 32 Kword data memory (address lines available up to 128 Kwords).
- 4 Kword program memory (addressable to 16 Kwords).

SLD will rely heavily upon the processing power of the SSPs in the event trigger, event readout, and system calibration.

3. ACQUISITION MODULES

Each of the 220 CCD chips is read out in parallel, with each chip containing 385x578 pixels. Data are clocked out of the CCDs at a rate of 1 pixel per 200 nsec (100 nsec for the pixel shift and 100 nsec for digitization). A flash ADC samples each signal 4 times at 20 nsec intervals for signal averaging and subtracts the resulting sum from that of the previous pixel

for baseline suppression. These digitized signals are passed to a module which, working on several rows of data in a fast memory, applies thresholds and defines clusters of hit pixels. Addresses and pulse heights for these pixels are saved in a PASTBUS readable memory for readout by the SSP.

The drift chambers and Cerenkov Ring Imaging Detectors are read out using a wave form sampling module shown schematically in Fig. 3. Because the full digitization of the drift chamber system requires approximately 30 msec, signals from each wire are first passed through an analog comparator and latched for use by the trigger system between beam crossings. For full digitization, the analog signals are sent to an Analog Memory Unit^{1,4} (AMU). The AMU is a custom VLSI chip containing 256 sample and hold circuits. Two AMU chips are multiplexed together for each wire for a total of 512 samples, and data from a single wire are sampled by the AMUs at 7 nsec intervals (or 50 nsec in the case of the CRIDs), thus storing a complete 512 sample wave form for each wire. Analog data for 64 wires are then multiplexed from the AMUs to a single ADC which digitizes the data at a 1 MHz rate. Pedestal subtractions and gain corrections are then applied to the digitized data. Finally, threshold logic suppresses empty channel data before storing the remaining data in memory. This logic utilizes a look ahead feature in order to save several additional samples before and after the leading and trailing edge thresholds so that the thresholds need not be set exceptionally low.

Signals from the liquid argon calorimeter and the pads of the iron calorimeter are sent to a Calorimeter Data Unit (CDU), which is an analog memory chip similar to the AMU. The CDU is arranged to make 4 time samples of 32 separate input channels. In the SLD application, only 2 samples will be used: one at signal maximum and one just prior to beam crossing in order to measure the signal baseline. To gain dynamic range, each signal is split and measured with two different gains. The preamplifiers and the CDUs will be mounted in the detector in order to minimize cable plant. Analog data from 256 calorimeter channels (with 2 time samples x 2 gains

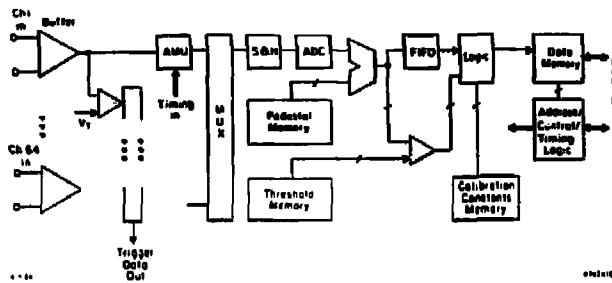


Fig. 3. Wave-form Sampling Module.

for each channel) are multiplexed through a fiber optic link to an ADC on the FASTBUS acquisition board. The ADC digitizes data from the CDUs at a 1 MHz rate, gain selection is made, baseline and gain corrections are applied, and the data are stored in memory. Because the look-ahead feature used by the drift chamber system is more difficult to apply in three dimensions, and because the quantity of data digitized is smaller than in the drift chamber case, suppression of empty channels is not done by the acquisition boards but instead is postponed to the SSP processing stage.

Signals from the iron calorimeter strip readouts are discriminated and latched in shift registers located inside the detector. The latched registers are read out serially at a 2 MHz rate and stored in memory in the FASTBUS acquisition modules. Suppression of empty channel data is performed by the SSP.

4. EVENT TRIGGER

The low 180 Hz repetition rate of the SLC allows a very simple trigger system when compared to those of colliding ring detectors. The required reduction in trigger rate from 180 Hz to 1-2 Hz is much less formidable than on circular machines, and the completely synchronous 5.5 msec between beam crossings allow functions to be performed in software, without introducing dead-time, which would otherwise need to be done with hardware.

Only the drift chamber and liquid argon calorimeter systems are used in the trigger. On the drift chamber acquisition boards, signals from each sense wire are discriminated and latched for each beam crossing. Each layer of the drift chamber system is arranged in cells of eight wires. The 16 latched bits of the 8 wires \times 2 ends/wire of each cell are reduced (using majority coincidence) to a single bit by the SSPs in the acquisition crates. This condensed information is then passed to an SSP at the trigger level which uses the data from all drift chamber crates to identify candidate tracks.

Signals from the calorimeter are completely digitized in approximately 1 μ sec for each beam crossing. The acquisition boards apply pedestal subtraction and gain corrections for each channel and form energy sub-sums in groups of 256 channels. This data is compacted in the acquisition crate SSPs by eliminating groups with energy subsums below threshold. The compacted data is then passed to an SSP at the trigger level which uses data from all calorimeter crates to form an energy trigger.

Within the 5.5 msec between beam crossings, the SSPs make a decision to continue the event readout or to reset the system for the next beam crossing.

5. EVENT READOUT

Event readout at the acquisition crate level proceeds in two phases. Triggered events are fully digitized by the acquisition modules. This process requires approximately 50 msec, and the data acquisition system is dead during this time. The digitized data are buffered into the SSP memory in each crate where further processing is performed. This processing may require several hundred msec to complete. (For example, the drift chamber and CRID wave-form data must be reduced to leading edge time and integrated pulse height, with multi-hit resolution. The typical drift chamber crate will have to reduce approximately 500 such wave-forms per event.) However, if the SSP memory is expanded to 128 kwords, then several events may be buffered in the SSP. During event processing the SSP is interruptible and can process beam-crossing trigger data. Thus additional dead-time is incurred only if the SSP buffer memory fills up. The SSP should easily be capable of buffering at least three events. For a 400 μ s processing time at a 2 Hz trigger rate, this would result in a deadtime of 2% in addition to the 10% deadtime incurred by the acquisition boards themselves.

Processed data from the acquisition level SSPs are passed to a single FASTBUS Micro-VAX at the filter level, which performs further processing on the event as a whole. This processed event data is in turn sent to the host computer where it is logged and further analysed on a sampling basis.

Table 1 shows estimates of the amount of data per event digitized by the acquisition boards, sent to the SSPs, and sent to the host.

6. SYSTEM CALIBRATION

Because each of the time bins of the AMUs must be separately calibrated, the parallel (by crate) processing power available in the SSPs is an important aspect of the calibration system. Each crate contains approximately 600,000 AMU bins, and there are 38 such crates in the system. The time bins are calibrated by applying DC levels to the inputs of the AMUs. Additionally a calibration pulser system will be used in each of the detector subsystems in order to calibrate the individual detector channels through the preamplifiers.

Table 1. Estimates of the amount of data per event digitized by the acquisition boards, passed to the acquisition crate SSP, and passed to the host for detector subsystems.

| Subsystem | Number of Crates | Acq. Boards (Mbytes) | SSP (Kbytes) | Host (Kbytes) |
|---------------|------------------|----------------------|--------------|---------------|
| CCDs | 7 | 50 | 130 | ?? |
| Drift Chamber | 10 | 14 | 500 | 40 |
| GRID | 24 | 32 | 50 | 20 |
| Calorimeter | 5 | 9.1 | 130 | ?? |
| | 46 | 96 | 810 | 100 |

7. HOST PROCESSOR

The host processor system is shown schematically in Fig. 4. Principal elements include:

- The front-end system of Micro-VAX computers previously discussed.
- A VAX 8600 clustered with a VAX 11/780, interfaced to FASTBUS and CAMAC.
- Primary and secondary operator consoles.
- Local and wide-area networking.

Although discussed in a previous section on the FASTBUS acquisition system, the Micro-VAX system may legitimately be considered as part of the host processor system. The software run in the Micro-VAXen is identical to that run for offline analysis (if the filtering algorithms change between the time the data is acquired and the time it is analysed offline). The Micro-VAX runs the same VMS operating system as the primary host computer, and the connection to ethernet allows programs to be run interactively, so that these computers may also be used for diagnostic purposes.

The primary operator consoles consist of a terminal, touch panel, color graphic display, and a Micro-VAX computer connected to the host computer by ethernet. Additionally,

secondary consoles, which are simply graphic terminals, emulate the functions of the primary consoles. These provide an inexpensive and readily available interface to the online system from remote (either within or outside SLAC) as well as local locations.

8. SOFTWARE ARCHITECTURE

The software architecture of the host system is illustrated schematically in Fig. 5. The system consists of a series of processes which constitute a mainline analysis and a set of Solo Control Programs (SCPs) which perform control and display functions and may be custom tailored for application specific purposes.

The mainline analysis tasks run as batch (non-interactive) processes, and perform analyses which, in the absence of infinite computing power, cannot be duplicated by other consumer processes. The processes in Fig. 5 representing the mainline analysis were chosen for purposes of illustration, and bear little resemblance to those which will ultimately be implemented. More important is the network structure required to support such a system. The network structure allows for future offloading of analysis tasks to micro-processor farms, and allows the definition of alternate analysis paths for development or other special purposes. Any process (including the SCPs) may request a subset of event information from any other process subject to event selection criteria. Processes may also append data to an event.

The SCPs use a touch-panel driven system adapted from that developed for the SLC control system.⁵ Any number of SCPs may be running concurrently, and not all SCPs need be identical. Code developed for the touch panel and display system provides well defined separation between "system" and application code, and allows application code to be easily attached to user defined touch panel buttons to provide for custom applications. In addition to having access to histograms and displays accumulated by the mainline analysis processes, the SCP is capable of requesting single event information from these processes, allowing it to perform parasitic

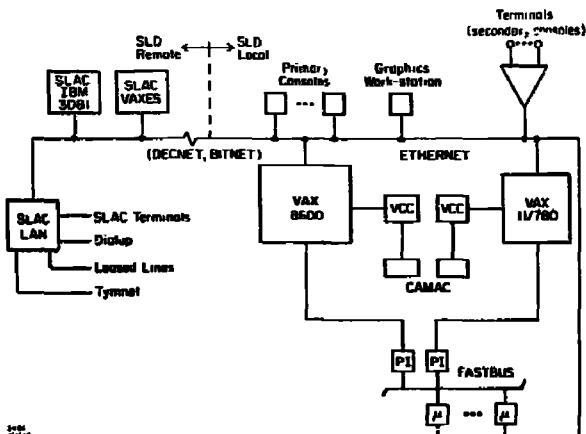


Fig. 4. Host computer configuration.

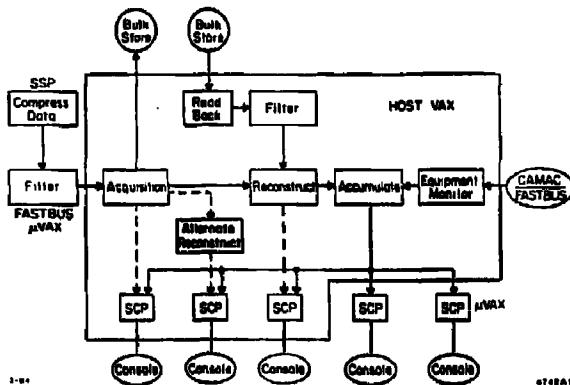


Fig. 5. Host software architecture.

analysis or to histogram standard quantities subject to cuts or selection criteria different from those of the mainline analysis. When used from a primary operator console, the SCP resides in the Micro-VAX rather than the host, resulting in significant cpu savings in the host. The availability of inexpensive and portable secondary consoles allows the development of code by collaborating institutions at remote sites. Such code can then be developed using a uniform control structure and can readily be incorporated into the SLAC-based system.

9. CURRENT STATUS

To date, almost all of the data acquisition system effort has gone into the development of a CAMAC-based system for use in the SLAC test beam facility, where testing of prototype equipment is being carried out. The software developed for this system may rightfully be considered as prototype software expected to evolve into the ultimate SLD operating system. The system uses a VAX 11/780 located at the test beam facility and a VAX 11/780 located in the central laboratory. The two computers communicate through a DECnet link. A single acquisition program runs on the 11/780 which logs data to tape and feeds SCPs which usually run on the 11/780. Provision is also made for a process which analyses PWC data common to all subsystems, although the application code for this process has not yet been installed. Four independent detector subsystems are being tested, resulting in three custom tailored SCPs (the liquid argon and iron calorimeters are analysed together) which run independently of one another. The test beam system has been in operation for slightly more than one year, and the development emphasis is beginning to shift toward FASTBUS development and more formally SLD oriented software.

A standardized FASTBUS workstation is being developed using a Micro-VAX computer and IORFI interface. An IORFI driver for the revised FASTBUS Standard Routines⁶ is nearly complete. A VAX based IBM cross-assembler has been developed for use with SSPs, and an IBM based SSP translator/linker originally developed by the SLAC Mark II group has been adapted for use on the VAX. Work is in progress on a VAX resident symbolic debugger which communicates with the SSP over FASTBUS.

Several prototype CAMAC wave form sampling modules incorporating hybrid chips containing 8 AMUs are currently being bench tested and are expected to be tested under real running conditions within a month. CDU chips have been fabricated and are currently being tested. Design of a hybrid circuit for multiple CDUs is in progress. Production of the first drift chamber FASTBUS board is expected in approximately one year, and the first calorimeter FASTBUS board is expected shortly thereafter.

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