2

SLAC/AP--59

DE88 004818

SLAC/AP-59
AAS Note 28
October 1987
(AP/AAS)

RF PULSE COMPRESSION DEVELOPMENT*

Z. D. FARKAS AND J. N. WEAVER

Stanford Linear Accelerator Center
Stanford University, Stanford, California 94305

Introduction

High-gradient accelerators for future e^+e^- linear colliders will require hundreds of megawatts of RF peak power per meter of accelerating structure.[1] Plots of peak and average power versus frequency[2] are shown in Fig. 1 for a proposed collider[1] with a gradient of 186 MV/m in each accelerator section, which is 1 meter long and has a 0.38 cm radius beam aperture. The average power is the product of the peak power, fill time and pulse repetition frequency. The fill time is the minimum time required to build up the accelerating fields in a section. Figure 1 shows that for this fixed beam aperture the average power decreases and the peak power increases with frequency, suggesting an optimum in the 10 to 15 GHz range. For a frequency of 11.4 GHz (four times the present frequency at SLAC) each section requires an input power of 533 MW peak. Then, as seen in Fig. 2, the relative group velocity is 0.03 and the fill time is 111 ns. This pulse width is considerably narrower than the normal, minimum pulse width of conventional modulators used with high peak power klystrons. Most current high-power microwave amplifier developmental projects at SLAC and elsewhere envision pulse lengths of about 1 μs and fall short of 500 MW peak power as a design goal by at least a factor of 2, with one notable exception which is discussed in more detail in the conclusion of this paper. Thus, RF pulse compression is a promising technique to enhance the usefulness of these amplifiers.

Presently SLAC uses a RF pulse compression system called SLED,[3] which effectively compresses in time a 3.5 μs long, 60 MW klystron pulse into a 0.82 μs long, 160 MW pulse, to match the 0.82 μs fill time of the present 2.856 GHz SLAC accelerator sections. However, SLED has some shortcomings. Its maximum efficiency of 81% can only be reached at a compression ratio of about 3:1, and its efficiency drops off sharply as the compression ratio deviates from 3:1. Also, the compressed pulse power varies with time, which reduces the efficiency when it is used to fill an accelerator section.

*Work supported by the Department of Energy, contract DE AC03 76SF00515.

A new electromagnetic energy compression system, the Binary Energy Compressor (BEC), is being developed at SLAC,* which does not have the same loss mechanisms as SLED. It consists of an arbitrary number of stages. Each stage, a hybrid followed by a delay line, doubles its peak RF input power and halves its input pulse length. Thus, the required RF amplifier peak output power (P_{pk}) to a BEC is lower than the section peak input power (P_{pi}) by a factor of 2^n, and the required RF amplifier pulse is longer than the section fill time by a factor of 2^n, where n is the number of BEC stages and the BEC output pulse width (t_c) is chosen to be the section fill time (t_f) multiplied by $(1-\beta_g)$, a group velocity factor. The actual BEC power multiplication factor (M) is slightly less than 2^n and the compression factor (C_f), which is approximately the ratio of the BEC input pulse length to the compressed pulse length, is slightly greater than 2^n.

The BEC is especially suited to high frequencies, at which the accelerator section fill time is shorter and at which the lengths of the delay lines are reasonable. Also, at high frequencies the nearly lossless TE_{01} mode, in a relatively small diameter, overmoded, circular waveguide, can be used for the delay lines, which are the energy storage elements of a BEC. With low delay line attenuation, M can approach 2^n, and the efficiency of compression (η_{pc}) will be limited mainly by the pulse rise and fall times. The body of this paper 1) discusses the theory and some rules for designing a multistage BEC, including its response to nonstandard phase coding, 2) describes some proof-of-principle experiments with a couple of low power BECs, 3) presents the design parameters for some sample linear collider RF systems that could possibly use a BEC to advantage and 4) outlines in the conclusion some planned R&D efforts. In Appendix I some BEC phase balancing techniques are prescribed, in Appendix II a simple error and stability analysis is presented and in Appendix III a list of symbols used in this paper is given along with their definitions.

BEC Theory of Operation

The theory of BEC operation perhaps can best be understood by looking at a 2 stage and then at a 3-stage BEC, as shown schematically in Figs. 3 and 4, respectively. The high power input and output signals at the various stages of a BEC will be referred to in terms of their phases and power amplitudes, rather than in terms of their phases and voltages. The phase coder modulation waveforms are TTL voltage signals and are referred to in terms of their voltages. In order for a BEC to produce a compressed pulse of width t_c, the two equal, RF input signals to the first hybrid (H_1) must have the relative phases of their associated voltages shifted back and forth between zero and π radians by a phase coder, according to a very specific pattern during a time defined as the BEC

period (t_p). The number of stages in the BEC and the width of the desired output pulses are related to t_p by: $t_p = 2^n t_s$. Furthermore, the RF input power to the phase coder can be pulse modulated so that it consists of a pulse of width (t_k), which must be greater than t_p. By design the delay time (t_{dn}) of the shortest and last delay line of an n-stage BEC is equal to t_s, which alternately is defined as one time bin. Also, each delay line back toward the first is twice as long as the previous one. The first delay line has a delay time (t_{d1}) that is equal to $t_p/2$. Thus, not coincidentally, t_p is the minimum input pulse width required for single pulse BEC operation. Multiple pulse BEC operation, which consists of several, compressed, output pulses for each RF input pulse, can be of great interest and will be discussed further below.

One practical method of generating the phase coding is to use a phase shift keyer (PSK) driven by a TTL signal. The PSK shifts its relative phase length rapidly between 0 and π, as the TTL signal logic changes from 0 to 1. Two PSKs are required for a phase coder. They may be arranged in *series* with one at the input of the power divider and one at the output, as shown in Fig. 3a or with both in *parallel* at the output of the power divider, as shown in Fig. 3b. With the *series* arrangement, the TTL waveform applied to PSK B is the same regardless of the number of BEC stages employed, including a one stage BEC for which PSK A is not required. The *series* format requires simpler coding, and thus was used for the experiments discussed in this paper. The relationship between the two codes is $A = A'$ and $B = A' \oplus B' = |A' - B'|$.

For pulsed BEC operation the phase coder is programmed so that each BEC stage combines its two inputs at the a output during the first half of the pulse and during the second half at the b output. The a output passes through a delay line so that it then coincides in time with the b output. Thus, each stage halves the pulse length and doubles the pulse power. By adding stages and changing the modulation accordingly, this can be repeated with as many stages as desired, subject to switching time and delay line loss limitations.

One method for determining the appropriate phase coding and relative power amplitudes and for adjusting the phases and delay times between stages is a deductive one that uses the following rules at each hybrid or stage. Since by definition the amplitudes, phases and pulse widths are specified at the output, the output is a reasonable place to start and work backwards from.[6] The input power amplitudes to the m^{th} hybrid of a n-stage BEC are denoted by I_{am} and I_{bm} and the output power amplitudes by O_{am} and O_{bm}, where $m = 1, 2, \ldots n$. A minus sign represents a relative phase shift of π radians and no sign represents a relative phase shift of zero.

Rules for BEC operation:

1. Both inputs to H_1, denoted by I_{a1} and I_{b1}, are set equal to unity, but in general can differ in phase by π from one time bin to another time bin during a modulation period.
2. During the last time bin of the modulation period, both outputs from a n-stage BEC are equal in phase and $O_{an} = O_{bn} = MI_{a1} = MI_{b1}$. During the first $(2^n - 1)$ time bins of the same modulation period, O_{an} and O_{bn} are zero.
3. At any stage m, if both equal inputs I_{am} and I_{bm} have the same sign (zero relative phase), all the power exits from output a; hence, $O_{am} = 2I_{am} = 2I_{bm}$ and $O_{bm} = 0$.
4. At any stage m, if both equal inputs I_{am} and I_{bm} have the opposite sign (π relative phase), all the power exits from output b; hence, $O_{bm} = 2I_{am} = 2I_{bm}$ and $O_{am} = 0$.
5. If there is power at only one input to a hybrid, the power at each output is one half of that input power and has the same sign.
6. The sign of either output from a hybrid H_m is the same as that of its a input.
7. O_{a1} is delayed by 2^{n-1} time bins by delay line D_1, O_{a2} is delayed by 2^{n-2} time bins by delay line D_2 and so on until D_n delays O_{an} by only one time bin.
9. If there is no phase coding of the input power, the transmission characteristics of a n-stage BEC are as follows. The BEC is transparent (no power multiplication) if the number of stages is even. The BEC is a combiner (i.e., a doubler at one output) if the number of stages is odd. That translates into $O_{an} = O_{bn} = I_{a1} = I_{b1}$ for n even and $O_{an} = 2I_{a1} = 2I_{b1}$ and $O_{bn} = 0$ for n odd.

The six possible input-output conditions or cases for BEC operation of a hybrid are given in Table 1, which follows from the above rules. The use of these rules, directly and/or by referring to Table 1, is illustrated in Table 2, which lists the PSK phase coding and the phases and the relative power amplitudes at each stage of a 2 stage BEC. It can easily be shown that input power is necessary only during time bins 1 through 4 for a 2 stage BEC for single pulse operation. This type of table is also very helpful in understanding the operation of a particular BEC when the input pulsing and/or phase coding is not standard or is not optimum. Glitches in a pulse, unexpected shortening or lengthening

Table 1 - The input and output phase and relative power amplitude relationships for the m^{th} hybrid of a n-stage BEC at reference planes adjusted for BEC operation. The minus sign indicates a relative phase shift of π radians due to PSK phase coding of the input powers.

Cases	1	2	3	4	5	6
I_{am}	1	1	-1	-1	0	1
I_{bm}	1	-1	1	-1	1	0
O_{am}	2	0	0	-2	1/2	1/2
O_{bm}	0	2	-2	0	1/2	1/2

Table 2 - PSK TTL coding with the resulting phases and power amplitudes in a 2-stage BEC for CW inputs with single-period PSK phase-coding covering time bins 1 through 4. The minus sign indicates a relative phase shift of π radians.

Time Bin	0	1	2	3	4	5	6	7	8
PSK *A* TTL code	0	0	0	0	1	0	0	0	0
PSK *B* TTL code	0	0	0	1	1	0	0	0	0
I_{a1}	1	1	1	1	-1	1	1	1	1
I_{b1}	1	1	1	-1	1	1	1	1	1
O_{a1}	2	2	2	0	0	2	2	2	2
O_{b1}, I_{b2}	0	0	0	2	-2	0	0	0	0
I_{a2}	2	2	2	2	2	0	0	2	2
O_{a2}	1	1	1	1	0	0	0	1	1
O_{b2}, I_{b3}	1	1	1	0	1	0	0	1	1
I_{a3}	1	1	1	1	1	0	0	0	1

of a pulse or unwanted power in some time bins possibly could be traced by constructing such a table with various inputs. The phase coding and relative power amplitudes for a 3 stage BEC (t_1 N_s) are shown in Fig. 4 for pulsed inputs with single-period phase-coding (t_k t_p).

Multiple pulse BEC operation can be achieved with the use of an appropriate phase coder word or modulation period (t_m) equal to an integral number (i) of BEC periods; i.e., t_m it_p. Then, if t_k t_m, t_k will be completely compressed into i output pulses of t_p duration with each pulse spaced apart in time by $(2^n - 1)t_p$. For the limit of a CW RF input, an infinite train of periodic output pulses each of t_p duration is obtained. The phase coder repetition frequency (f_c) is then equal to $1/t_p$, t_m t_p and t_k and f_c lose their meaning. If there is RF input power to the BEC before and after a phase coder modulation period, outputs of various amplitudes occur in time bins other than the last time bin of a BEC period (see rule 2 above). Table 2 shows this as a result of input power during time bins 0 through 8 with bins 1 through 4 coded for 2-stage, single-period, BEC pulse compression. Figure 5 shows the relationships between the pulse periods and the repetition rates for single-period and 2 period phase coding. The next section of this paper shows in some figures and oscillograms very clear examples of this transparent-combiner transmission effect of a BEC on uncoded inputs, as govern by rule 8 above. Also, in Appendix I it is shown how the relative phase shifts between stages can be adjusted for BEC operation by using CW RF signals at the input of the phase coder.

Experiments

Two, low-power BECs were constructed and tested at 11.4 GHz. One used 100 ft and 50 ft WR90 rectangular waveguide delay lines, with 121 and 62 ns time delays, respectively. Because of the high (3 dB/100 ft) attenuation of these delay lines, the first BEC, which was built with them, had a M close to 1 and as such has little usefulness. However, it provided an initial demonstration of the viability of 1-, 2- and 3-stage BEC operation. Also, since the properties of a delay line added to the output of a stage are well understood, the third delay line of Fig. 4 was not necessary to illustrate the theory of operation of a 3 stage BEC. The second experimental BEC used 60 ft long and 30 ft long shorted WC281 circular waveguide delay lines operating in the TE_{01} mode. Special transitions from WC281 to WR90 were employed to connect the delay lines to WR90 3-port circulators, as shown in the circuit of Fig. 6. The theoretical attenuations of the 136 ns and 68 ns delay lines are approximately 0.15 and 0.075 dB, respectively. The measured total attenuation of the two delay lines including transitions and circulators was about 1.5 dB, which begins to be interesting since that translates

into a M of 2.8 for a 2–stage BEC. The circulators of Fig. 6 would not be part of a high-power BEC, but they allowed for a more compact configuration for the initial low-power tests.

Ideal PSK modulation waveforms are shown in Fig. 7 for a 2–stage BEC for the two configurations of Fig. 3. The resulting input power and compressed output power pulses are shown in theoretical form in Fig. 8. Figure 9 is an oscillogram of the outputs of a 2 stage BEC. It shows that a 240 ns portion of the CW input has been compressed into a 60 ns pulse with an amplitude four times greater than the CW amplitude (the vertical scale is not linear), thus confirming the theoretically predicted behavior. Figure 10 is an oscillogram of the PSK modulation waveforms (TTL voltages) for a 2-stage BEC, expanded to show their rise and fall times. The output power pulses for Fig. 9 are shown in Fig. 11, expanded to show their rise and fall times, too. Figure 12 shows 2–stage outputs, superimposed on the same oscillogram, for inputs with and without PSK modulation. With modulation two, compressed, 70 ns long, coincident, output pulses result during the fourth time bin of the four time-bin-long (280 ns) input pulses, which started slightly to the left of the left edge of the oscillogram. Without modulation two, uncompressed, four time-bin-long, output pulses emerge unmultiplied as per rule eight of the previous section. Output *a* (upper set of traces) is delayed three time bins and output *b* (lower set of traces) is delayed two time bins, due to the expected routing through the BEC network. Figure 13 shows the PSK modulation waveforms for 2-period phase-coding of a 2-stage BEC and Fig. 14 shows the resulting output pulses with CW inputs. Figure 15 shows the PSK modulation waveforms for repetitive-period phase-coding of a 2-stage BEC and Fig. 16 shows the resulting output pulses with CW inputs. Thus, CW inputs can be transformed into repetitive output pulses. The horizontal traces superimposed over the pulses of Fig. 16 result from removal of the PSK modulation.

By adding a hybrid to the 2-stage BEC of Fig. 3a and applying 3-stage modulation, a 3–stage-like output results. However, for complete 3–stage operation, output *a* has to be delayed by its pulse length in order to coincide with output *b*, which is what an added D_3 delay line would do. Phase coding for a 3-stage BEC is shown in Fig. 17. The theoretical 3 stage BEC input and output power pulses are shown in Fig. 18. Figure 19 is an oscillogram of the same 3 stage BEC output power pulses with single-period phase-coding of a CW input. It shows that a 280 ns portion (a single modulation period) of the CW input has been compressed into a 35 ns pulse with an amplitude 8 times greater than either CW input, again confirming the theoretically predicted behavior. It is also interesting to note that the portion of the inputs outside the modulation period appear at output *a* with double the amplitude of one input, and there is no output power at output *b*. This is explained by rule 8, which states that a

3-stage BEC is a combiner at the a output for the uncoded portion of the inputs. When the pulse coder pulse repetition rate (f_c) is increased sufficiently, the CW inputs are transformed into repetitive pulses at the outputs. This occurs when $f_c = 1/t_p$ or $f_c = 1/8t_s$ for a 3-stage BEC. The repetitive-period PSK modulation waveforms for a 3-stage BEC are shown in Fig. 20, and the repetitive pulses at the outputs are shown in Fig. 21. Figure 22 shows the outputs when the input is pulsed, but no phase coding is applied.

The PSK modulation waveforms are digital words, which can be generated by using parallel-to-serial shift registers. However, for up to a 3 stage BEC, the waveforms can be generated easily by using a number of laboratory pulse generators. In these experiments the TTL waveforms used to drive the PSKs were generated by three Berkeley Nuclear Corporation 8010 pulse generators.

Some other manifestations of rule 8 and the combiner/transparent nature of uncoded BECs are illustrated by a 3-stage BEC, with 2-stage modulation, which is a quadrupler followed by a combiner. Figure 15 shows repetitive-period, 2-stage phase coding and Fig. 23 shows the resulting output from H_3, which consists of 8 times one input at output a and zero output at output b. Figure 24 shows what happens if the phase coder repetition rate is decreased so that $1/f_c$ is greater than t_p, the BEC period.

Linear Collider RF Systems Incorporating A BEC

Accelerator section parameters for several possible linear collider designs are given in Table 3, along with a listing of the RF peak power needed to produce a given gradient.[8] Table 4 lists the parameters for the BEC's that could be incorporated into the above collider designs in order to decrease the required amplifier peak output power. The BEC parameters are related to the section parameters as follows:

$$P_{pk} \quad \frac{P_{pa}}{M}, \quad t_s \quad t_f(1 \quad \beta_g), \quad t_k \cdot t_p \quad 2^n t_s, \quad P_{ak} \quad P_{pk} t_k f_r$$

$$P_{av} = P_{pa} t_s f_r, \quad \eta_{pc} \quad \frac{M}{G_f}, \quad G_f \geq \frac{t_k}{t_s} = 2^n, \quad t_{dm} \cdot 2^{\ m} t_p - 2^{n\ m} t_s,$$

$$l_{dm}(\mathrm{m}) \cdot 0.3\beta_g t_{dm}(\mathrm{ns}) \quad \left(\frac{2^n \ ^m \cdot \beta_{gd}}{\beta_g}\right) l_s(\mathrm{m}), \quad l_s(\mathrm{m}) \quad 0.3\beta_g t_s(\mathrm{ns}),$$

$$\beta_{gd} \quad \frac{\lambda}{\lambda_{gd}}, \quad A_{dm}(\mathrm{dB}) \quad \frac{0.932 t_{dm}(\mathrm{ns})}{\mathrm{d}^3(\mathrm{in}) f_0^{3/2}(\mathrm{GHz})}.$$

Table 3 – Accelerator section RF parameters for five sample linear collider designs with $f_r = 120$ pps.

Case	f_0	β_g	a	b	l_s	t_f	E_a	P_{ps}/l_s	P_{as}/l_s	P_{ps}	P_{as}
No.	GHz	-	cm	cm	m	ns	MV/m	MW/m	kW/m	MW	kW
1	11.4	.4	1.16	1.54	15	125	21	31.5	0.28	472	4.25
2	11.4	.03	.38	1.07	1	111	186	533	6.9	533	6.91
3	18	.1	.38	0.76	1.8	60	186	700	4.7	1260	8.16
4	30	.1	.21	0.42	1	30	186	430	1.56	430	1.39
5	42	.2	.18	0.3	1	16.6	186	565	.90	565	.90

Table 4 – BEC parameters for the collider designs of Table 3. For these examples, it was assumed that $\eta_{pc} \approx 7/8$ and $C_f = t_k/t_s = t_p/t_s = 2^n$.

Case	n	M	t_s	t_p	P_{pk}	P_{ak}	t_{d1}	β_{gd}	l_{d1}	d	A_{d1}
No.	-	-	ns	ns	MW	kW	ns	-	m	in	dB
1	3	≈7	75	600	67	4.82	300	.893	80	2.81	0.33
2	3	≈7	108	864	76	7.88	432	.893	116	2.81	0.48
3	4	≈14	54	864	90	9.33	432	.959	124	2.81	0.24
4	4	≈14	27	432	31	1.61	216	.947	62	1.5	0.36
5	4	≈14	13.3	213	40	1.02	106	.973	31	1.5	0.11

The symbols are defined in Appendix III. In the first case the present SLC 1.16 cm radius beam aperture and the 21 MV/m gradient are maintained, but the frequency is increased to 11.4 GHz. This quadrupling of the frequency reduces the average power required by a factor of four and reduces the accelerator section cavity radius from 4.13 cm to 1.54 cm. However, for a linear collider design gradient of 186 MV/m, this long section would have an extremely high peak power

requirement and thus be impractical. In the second case, which was proposed by P.B. Wilson,[11] the beam aperture is reduced to 0.38 cm in radius and the section length is shortened. This then results in a 186 MV/m gradient for the about the same peak power as required for the 21 MV/m gradient of case 1. In the third and fourth cases the frequency is increased and consequenly the average power required per meter is further reduced. In the last case the frequency is increased and the aperture is decreased even further, which results in an even further reduction in the average power per meter requirement. Also, the higher the operating frequency of the BEC the shorter the delay lines become, making the BEC mechanical configuration simpler. In all the above designs, a BEC stage can be eliminated by doubling the amplifier peak output power.

Presently, it is not clear which of several high-power X band amplifiers, that are being developed, might best be used with a BEC enhanced RF system. Currently a 5–cavity, 8.6 GHz, conventional-klystron amplifier, designed to put out 30 MW peak, is undergoing tests at SLAC. A 11.43 GHz version may be in the offering soon afterwards. Also, the University of Maryland is developing a high-power gyroklystron in this frequency range.[6]

The gyroklystrons have TE_{01} circular guide outputs and therefore could feed a TE_{01} circular waveguide BEC directly. With or without pulse compression, there is no point in adapting from a TE_{01} circular to a TE_{10} rectangular waveguide and then to a TM_{01} accelerator waveguide. A theoretical design for a transition from a TE_{01} circular waveguide to the TM_{01} circular accelerating guide has been developed.[7] If the distance between an amplifier and an arcelerator section is more than a few meters, then a TE_{01} circular waveguide RF distribution system is recommended, because there is a significant attenuation in rectangular waveguide at high frequencies. For instance, at 18 GHz the attenuation in WR62 rectangular waveguide is 0.15 dB/m as compared to 0.002 dB/m in WC281 circular waveguide.

Another feature of a BEC enhanced RF system, as touched upon earlier in this paper, is its ability to compress a long pulse into a number of shorter pulses, as shown in Figs. 5 and 25. This feature can be used advantageously because in general the klystron pulse rise time is greater than the compressed pulse rise time. For the SLAC 5045 klystron the RF pulse rise time is 1 μs and the 0 to π RF phase transition takes less than 0.1 μs. Thus, it is more efficient to increase the pulse repetition rate by using an amplifier output pulse that is several times longer than t_p, rather than by increasing the number of amplifier pulses. The effective repetition rate (f_{re}) is then increased by a factor of i or $f_{re} = if_r$.

Of course, it is possible to try to develop an amplifier whose peak output power is equal to the peak power required by an accelerator section. Currently, a SLAC–LLL collaboration is experimenting with a relativistic klystron, which has of a conventional, 5–cavity, X–band klystron body and a gun consisting of a megawatt induction linac injector. The gun accelerating voltage is produced by a series of induction modules that are driven by saturable reactor circuits. The resulting ultrashort(approximately 50 ns long), pulsed, multikiloampere beam is passed through focussing coils and on into the klystron body. In general, higher voltages, such as expected for a relativistic klystron, should not necessarily result in abrupt breakdown; however, the fault rate may be greater. Experience will tell at what level fields can exist in the output cavities of a heavily beam-loaded relativistic klystron. If lower than the desired limitations exist on the peak output power of a klystron or other type of microwave amplifier, then perhaps a BEC could step in and boost the level of a longer, lower peak-power pulse as needed. Also, it will be interesting to see what sort of phase and amplitude stability limitations exist with a relativistic klystron with such a short pulse, which is comparable to the klystron cavity filling times. In the end the choice between amplification followed by RF pulse compression and direct amplification should depend on the overall efficiency, the stability, the reliability and the cost of the competing RF systems.

Conclusions and Future Plans

The two low-power tests described above confirmed the basic BEC theory and demonstrated its feasibility with available hardware. The results of an simple analysis of the amplitude and phase sensitivities for a BEC are given in Appendix II, and the lab experiments bore out what the calculations in Appendix II indicate; i.e., that $\pm 10^{\circ}$ phase and $\pm$ 0.2 dB power imbalances make only small differences in the M of a BEC. There was no noticeable difference in the outputs after several days of unattended BEC operation. Concerns about mode conversion losses and resonances in the delay lines due to transition mismatches were not born out in the circular waveguide tests. Circulators were used with the delay lines, because the TE_{01} hybrids which were suitable for high power were still on order. The next step is to build and test a BEC that can operate at high power. A design, which incorporates two WC281 U-bends, straight lengths of WC281 waveguide as delay lines, two WR90 to WC281 transitions, some WR90 elbows and two high-power 3dB hybrids with the a ports in WC281 and the b ports in WR90, is shown in Fig. 26. A definitive test of a high-power BEC must incorporate two high-power microwave amplifiers K_a and K_b, as shown in the same figure.

To simplify the construction of a high-power BEC, the following topics merit investigation in a program of continued BEC development:

1. Loaded TE_{01} delay lines.
2. Two-mode transmission delay lines.
3. Riblet type TE_{01} hybrids for delay lines.
4. Bending of delay lines with tightly coupled cavities.
5. A digital word generator with parallel to serial shift registers to drive the PSKs.

APPENDIX I

Phase Balancing a 2–stage and a 3–stage BEC

For an actual BEC circuit, the phases of the connecting lines between stages must be adjusted properly. For this purpose the fiducial phase shifters, ϕ_0 and ϕ_1 in Fig. 3a, of a 2–stage BEC can be set using the following procedure with a CW RF signal applied to the input of the phase coder:

1. Disconnect input I_{b1}, apply a TTL zero to PSK A and adjust ϕ_1 for zero output at O_{b2}.
2. Reconnect I_{b1} and apply a TTL zero to PSK A and a TTL one to PSK B. Adjust ϕ_0 for zero output at O_{b2}.

The fiducial phase shifters, ϕ_0, ϕ_1 and ϕ_2 in Fig. 4, of a 3–stage BEC can be set using the following procedure with a CW RF signal applied to the input of the phase coder:

1. Apply a TTL zero to both PSK A and PSK B and adjust ϕ_0 (ϕ_0 is inside the phase coder of Fig. 4) for zero output at O_{b1}.
2. Continue with a TTL zero on both PSKs A and B. The setting of ϕ_1 is now of no consequence, since after the above adjustment there is zero input at I_{b2}. Adjust ϕ_2 for zero output at O_{b3}.
3. It remains to set ϕ_1, which can be done either by disconnecting one of the inputs to H_1 or by applying 2 stage modulation, as shown in Fig. 7. In either case adjust ϕ_1 for zero output at O_{b3}.

APPENDIX II

Phase and Amplitude Sensitivities within a BEC

It can be shown that, if the relative phase of the unity amplitude inputs I_a and I_b differ from the properly adjusted BEC phase by $\Delta\theta$ radians then the

output powers are not 2 and zero, but

$$O_a = 2 - (\Delta\theta)^2/2 \quad \text{and} \quad O_b = (\Delta\theta)^2/2. \tag{1}$$

It can also be shown that, if the relative amplitudes of the inputs to a hybrid differ by δ^2, where $\delta = 1 - \sqrt{I_b/I_a}$, then

$$O_a = 2 - \delta^2/4 \quad \text{and} \quad O_b = \delta^2/4. \tag{2}$$

The change in phase length in degrees of phase ($^\circ\phi$) of delay line D_m, as a function of a change in the operating frequency (Δf) and a change in the temperature of the line (ΔT), is given by:

$$\Delta\theta_m(^\circ\phi) = 360 t_{dm}(\text{ns})\Delta f(\text{GHz}) + 360\alpha(^\circ\text{F}^{-1}) f(\text{GHz}) t_{dm}(\text{ns})\Delta T(^\circ\text{F}), \tag{3}$$

where t_{dm} is the delay time of delay line D_m. If $f = 11.4$ GHz, $t_{d1} = 140$ ns (the longest delay line used in the above tests) and α for copper $= 9.4 \times 10^{-6}/^\circ\text{F}$), Eq. (3) becomes:

$$\Delta\theta_1(^\circ\phi) = 50\Delta f(\text{MHz}) + 5.4\Delta T(^\circ\text{F}). \tag{4}$$

Referring back to Eq. (1), a $\Delta\theta$ in D_1 of $\pm$ 5.7°ϕ causes O_a to drop by 1/2%. This implies the following nonstringent conditions: $\Delta f/f \leq 10^{-5}$ or $\Delta T \leq 1.1^\circ$F. However, the requirements on the pulse-to-pulse phase and amplitude stability of the RF into each accelerator section and thus relative to the beam is more stringent. Phase and amplitude detectors at each of the two outputs of each BEC could stabilize those phases and amplitudes via low power attenuators and phase shifters at the amplifier inputs during the appropiate time bins. Thus, some combination of feedback circuits (similar to those required without a BEC) and moderately well-stablized circuit components should easily provide adequate control over the phase and amplitude of the outputs of a BEC supplemented RF system.

APPENDIX III

A List of Symbols and their Definitions

a	the radius of the accelerator section beam aperature (cm)
a	one of the inputs or outputs of the m^{th} BEC hybrid
A_{dm}	the attenuation of the m^{th} delay line of a n-stage BEC, assuming circular waveguide operating in the TE_{01} mode (dB)

α	thermal expansion coefficient (cm-cm^{-1} .° F^{-1})
b	the inside radius of the accelerator section cavities (cm)
b	the other input or output of the m^{th} BEC hybrid
β_g	accelerator section relative group velocity
β_{gd}	delay line relative group velocity
C_f	pulse width compression factor
d	delay line diameter (in)
D_m	the m^{th} RF energy storage delay line
η_{pc}	compression efficiency
E_a	accelerator section accelerating gradient (MV/m)
f_c	phase coder repetition frequency (Hz, pps)
f_o	operating frequency (MHz, GHz)
f_r	RF pulse repetition frequency (Hz, pps)
f_{re}	effective RF pulse repetition frequency for multiple period phase coding (Hz, pps)
H_m	m^{th} BEC hybrid
η_{pc}	compression efficiency
i	number of compressed pulses or BEC periods during a RF pulse
I	BEC hybrid input power amplitude
l_{dm}	length of the m^{th} energy storage delay line (m)
l_s	accelerator section length (m)
λ	free space wavelength (cm)
λ_{gd}	guide wavelength of a delay line (cm)
m	m^{th} BEC stage
M	power amplitude multiplication factor
n	number of BEC stages
O	BEC hybrid output power amplitude
P_{as}	average power into an accelerator section (kW)
P_{ak}	amplifier average power output (kW)
P_{pk}	amplifier peak power output (MW)
P_{ps}	peak power into an accelerator section (MW)
T	temperature (°F)
t_{dm}	time delay of the m^{th} energy storage delay line (ns)
t_f	section fill time (ns)
t_k	klystron pulse width (ns)
t_p	BEC period (ns)
t_s	compressed pulse width (ns)
t_w	phase coder word duration or modulation period (ns)

REFERENCES

1. P. B. Wilson, *"Future e^+e^- Linear Colliders and Beam-Beam Effects,"* SLAC–PUB-3985, May 1986.
2. Z. D. Farkas and P. B. Wilson, *"Comparison of High Group Velocity Accelerating Structures,"* Presented at the Particle Accelerator Conf., Washington, D.C., March 16–19, 1987, SLAC PUB–4088, February 1987.
3. Z. D. Farkas *et al.*, *"SLED: A Method of Doubling SLAC's Energy,"* Proc. of 9th Int. Conf. on High Energy Accelerator, p. 576, May 1976.
4. Z. D. Farkas, *"Binary Peak Power Multiplier and its Application to Linear Accelerator Design,"* IEEE Tran. MTT–34, p. 1036, October 1986.
5. Z. D. Farkas, *"The Role of Group Velocity, Frequency and Aperture in Linear Accelerator Design,"* SLAC AAS–33 September 1987.
6. V. L. Granatstein *et al.*, *"A 30 MW Gyroklystron Amplifier Design for High Energy Linear Accelerators,"* IEEE Transactions Plasma Science, October 1985.
7. Z. D. Farkas, unpublished.

DISCLAIMER

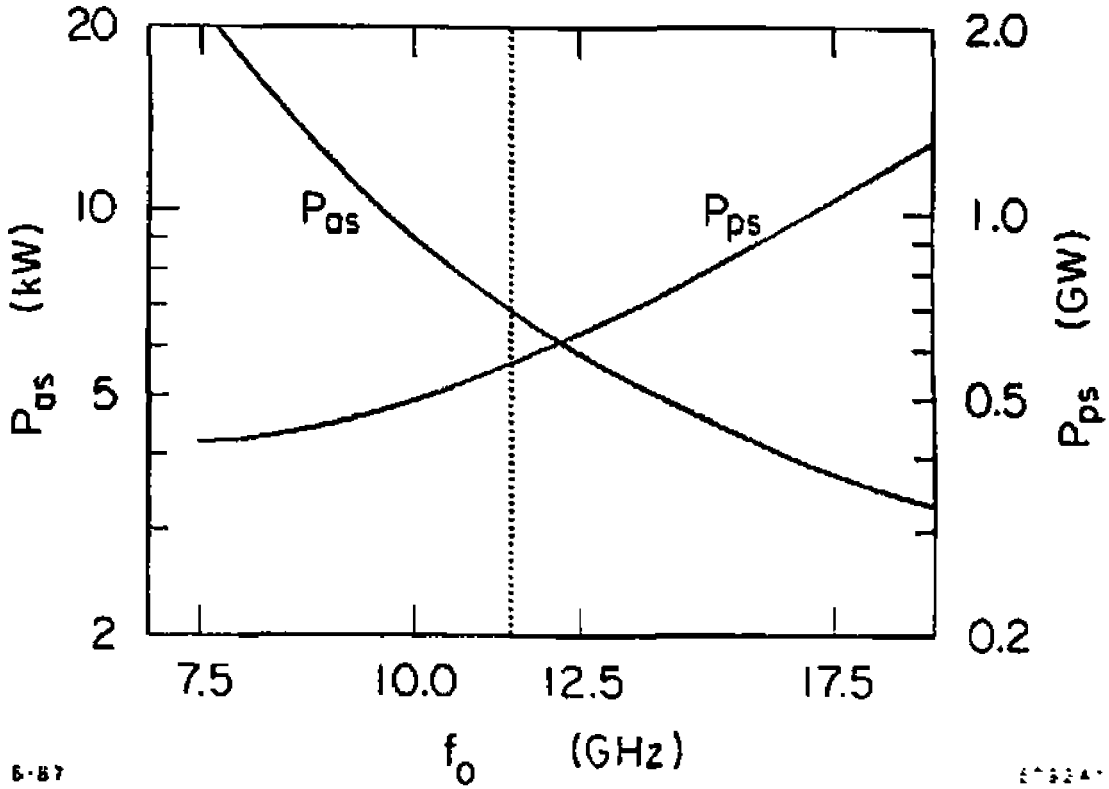


Fig. 1

Linear accelerator section average power (P_a) and peak power (P_p) requirements versus design frequency (f_o). This plot is for a 1 meter long, $2\pi/3$ mode, constant-impedance, disk-loaded structure with a gradient of 186 MV/m, a fixed 0.38 cm radius beam aperture and a cavity radius scaled as a function of frequency. The average power is calculated for a RF pulse repetition rate (f_r) of 120 pps.

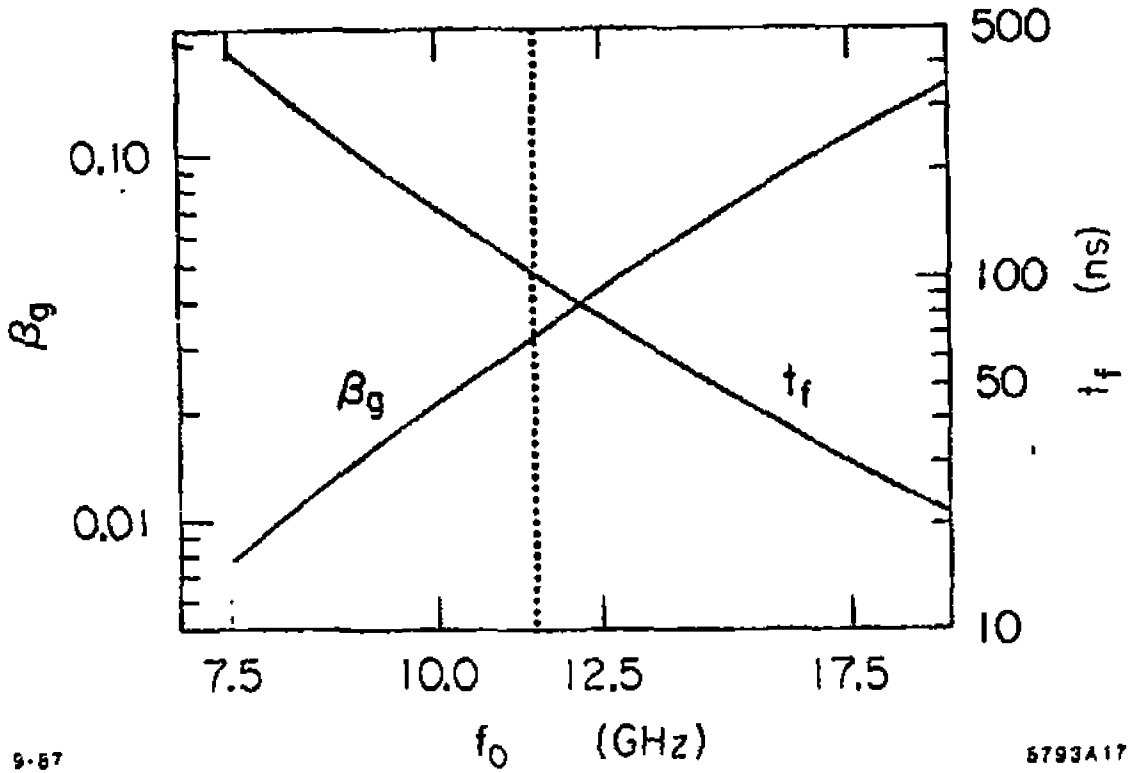
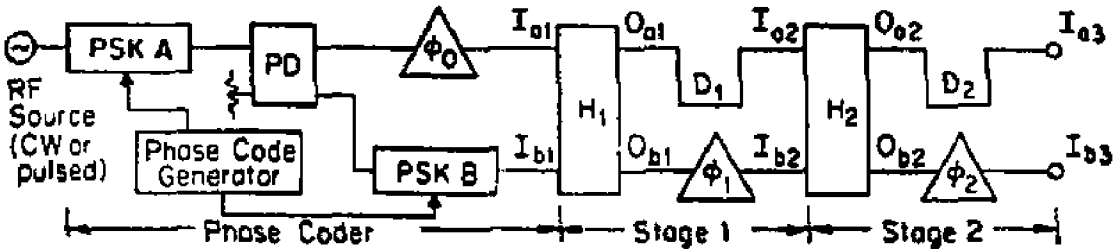
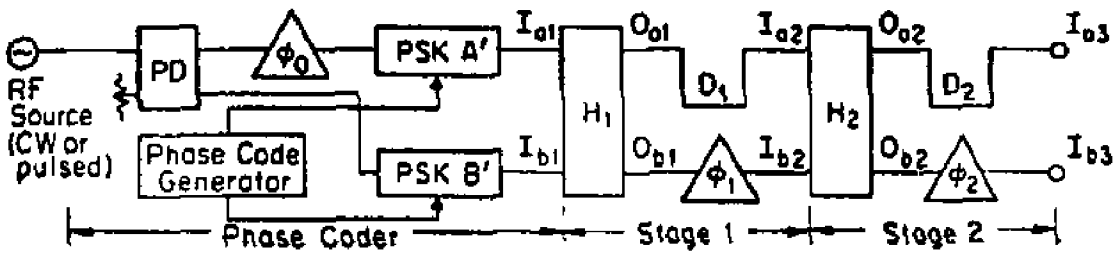


Fig. 2

Accelerator section relative group velocity (β_g) and fili time (t_s) versus design frequency (f_o) for the same design parameter constraints as in Fig. 1.



(a) With a "Series" Connected Phase Coder



6-87 (b) With a "Parallel" Connected Phase Coder 5793A2

Fig. 3

A 2–stage BEC with *series* and *parallel* connected PSKs.

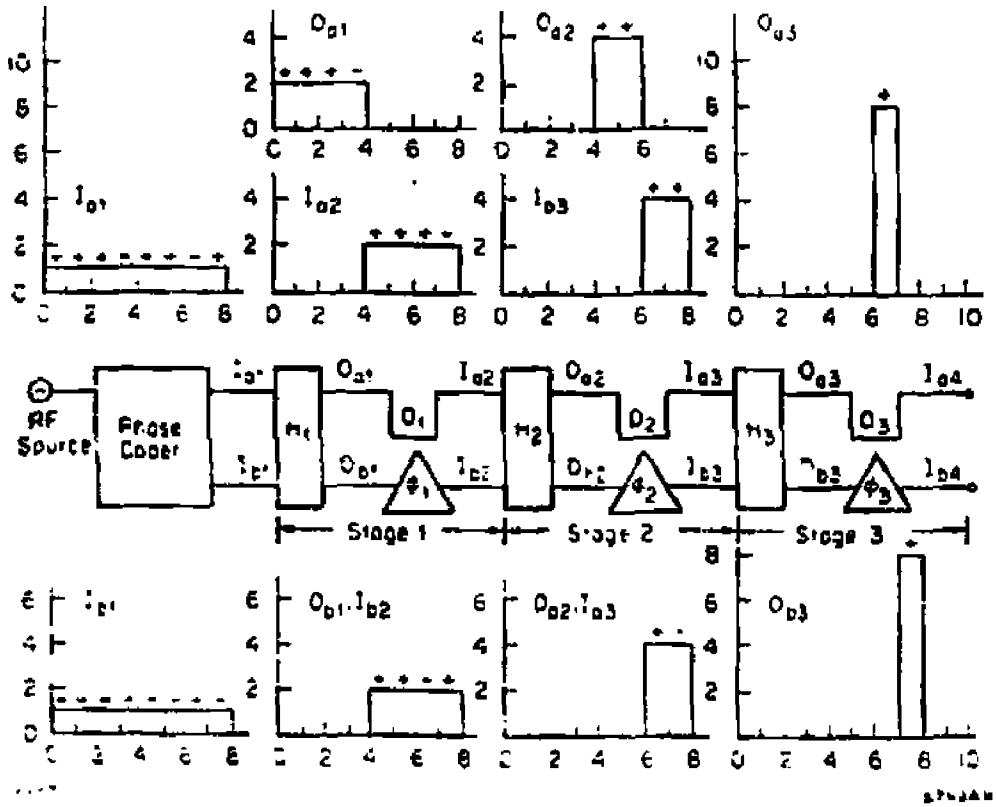
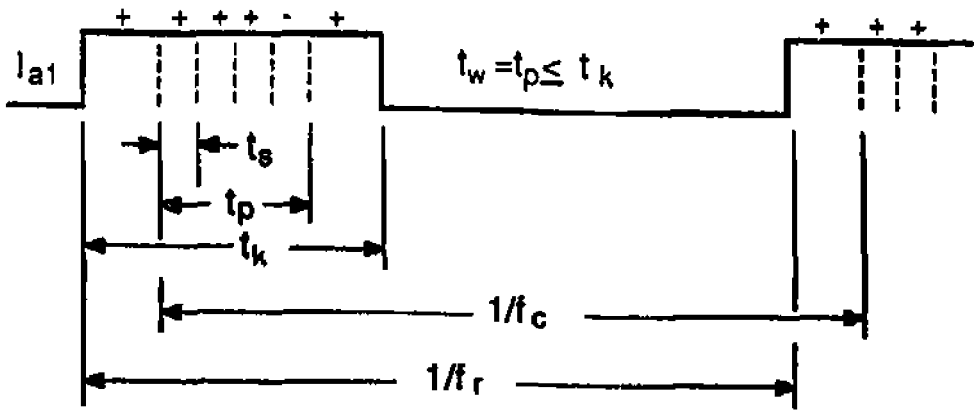
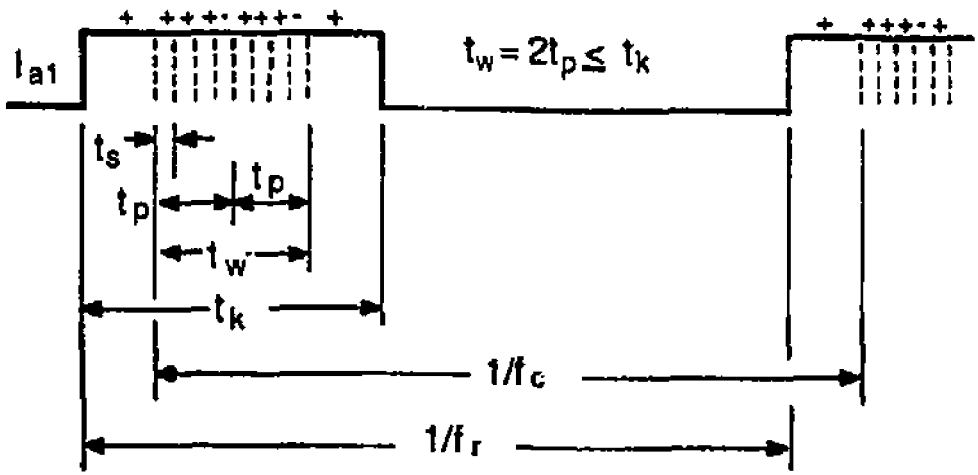


Fig. 4

A 3-stage BEC with its input and output relative phases and power amplitudes. The + and − signs above the amplitudes indicate 0 and π relative RF phase shifts, respectively, due to the phase coder and the circuit paths taken.



(a) Single-period operation.



(b) 2-period operation (i=2).

9-87
5793A18

Fig. 5

The pulsed RF input power amplitude to input *a* of H_1 of a 2-stage BEC, with the phase coding shown for: a) single-period operation and b) 2-period (i = 2) operation. If $f_c = 1/t_w$ and the input signals to the phase coder are CW, the CW inputs are transformed completely into equally spaced output pulses with a repetition frequency of $1/t_p$.

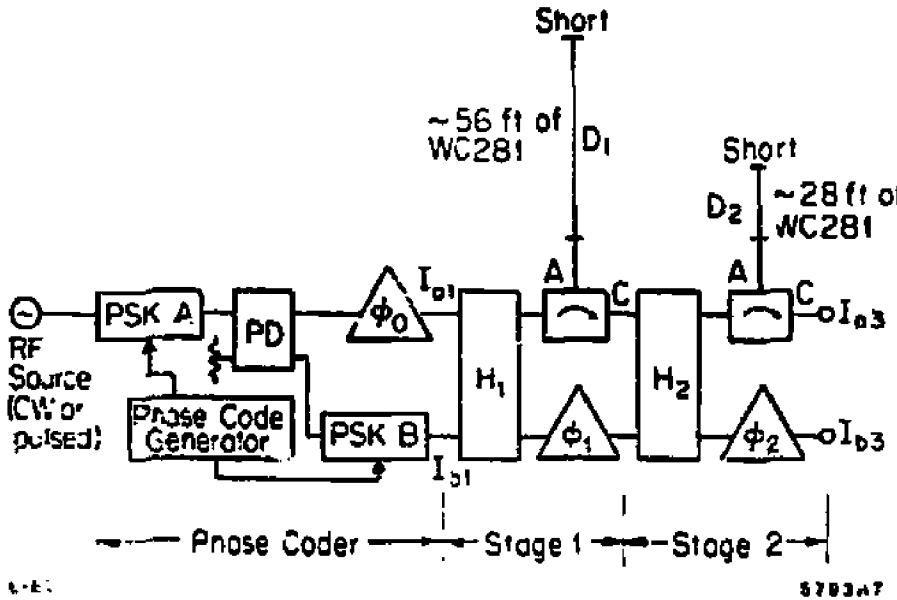


Fig. 6

Schematic of a 2-stage BEC laboratory demonstration set-up using circulators (C) and shorted lengths of WC281 circular waveguide for the two delay lines (D_1 and D_2). An adapter (A) from WR90 to WC281 waveguide was used in order to take advantage of the low loss TE_{01} mode for the long delay lines, while the rest of the components of the stages were in the more common WR90 waveguide.

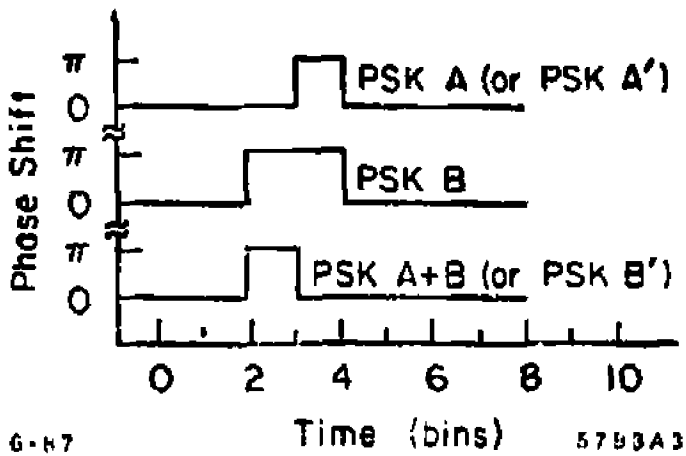


Fig. 7

Phase coding for a 2-stage BEC. PSK A and PSK A & B phase modulate the inputs I_{a1} and I_{b1}, respectively, and are applicable for the configuration of Fig. 3a. PSK A' and PSK B' are applicable for Fig. 3b.

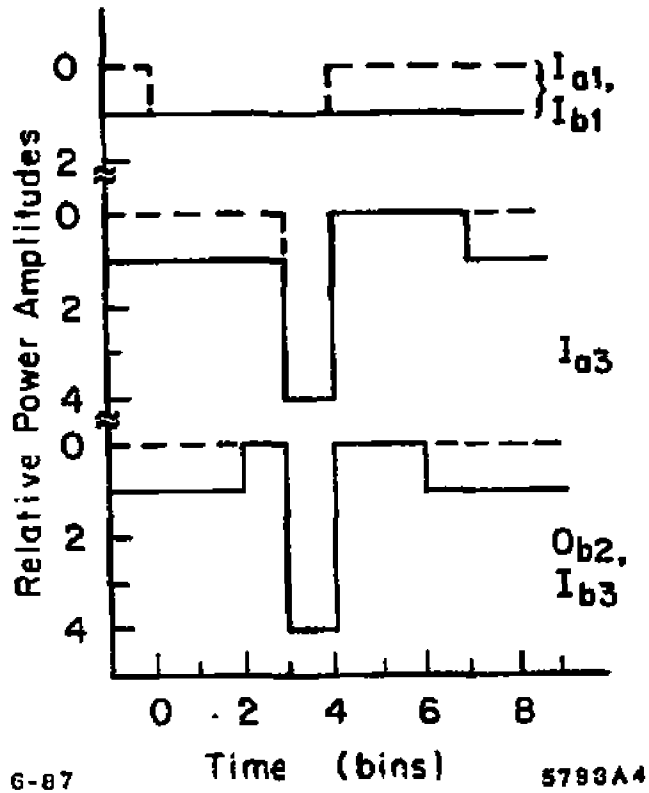


Fig. 8

Theoretical 2-stage BEC input and output powers. The solid lines indicate CW input power and the dashed lines indicate one modulation period for 2-stage BEC operation. The dashed lines follow the solid where only one is shown.

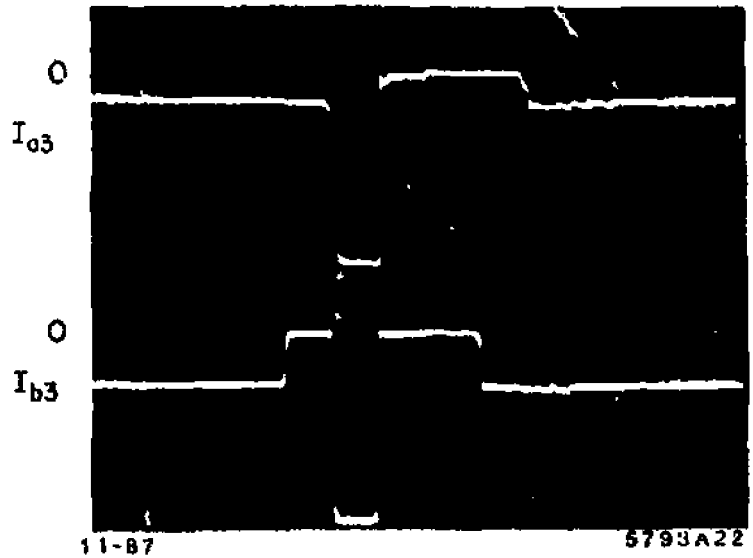


Fig. 9

Oscillogram of the outputs of a 2-stage BEC for CW inputs with single-period phase-coding. Horizontal scale: 100 ns/div.

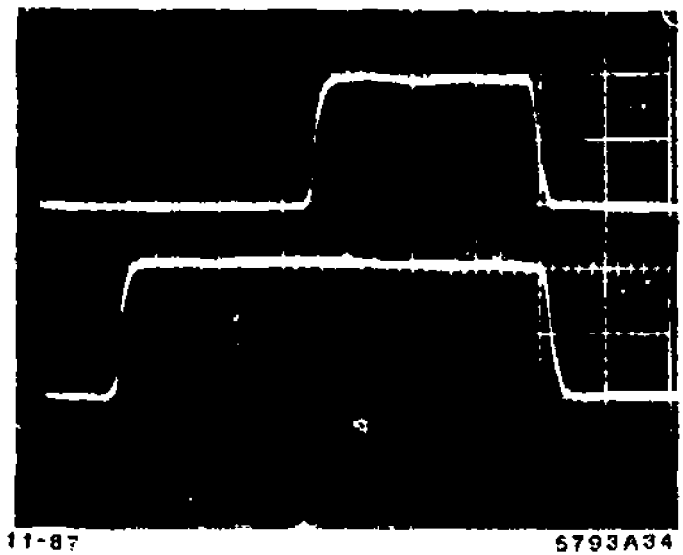


Fig. 10

Oscillogram of the TTL, phase-coding, voltage waveforms to the PSKs of a 2-stage BEC, expanded to show their rise and fall times. Horizontal scale: 20 ns/div.

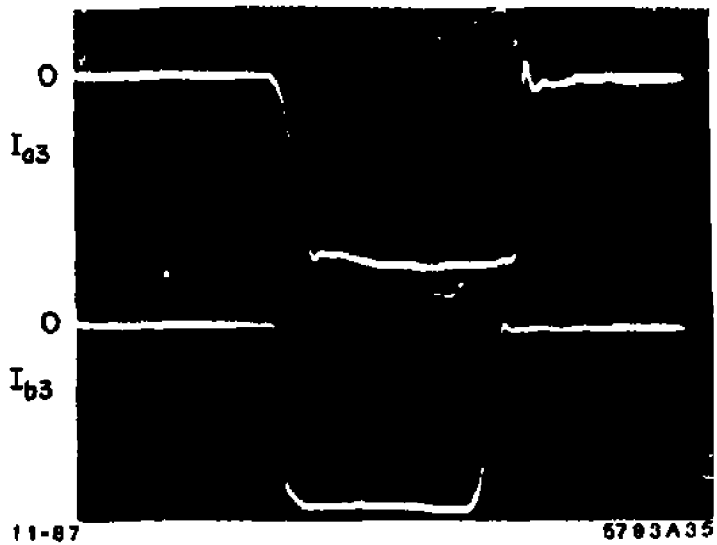


Fig. 11

Oscillogram of the output power pulses of a 2-stage BEC for pulsed inputs with single-period phase-coding, expanded to show the rise and fall times. Horizontal scale: 20 ns/div.

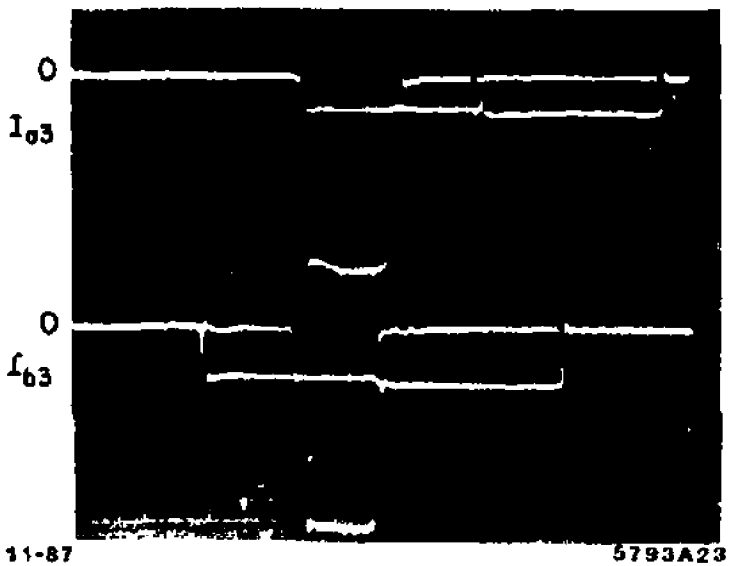


Fig. 12

Oscillogram of superimposed outputs of a 2-stage BEC for pulsed inputs with single-period phase-coding (higher, narrower pulses) and for pulsed inputs without PSK modulation (lower, wider pulses). Horizontal scale: 50 ns/div.

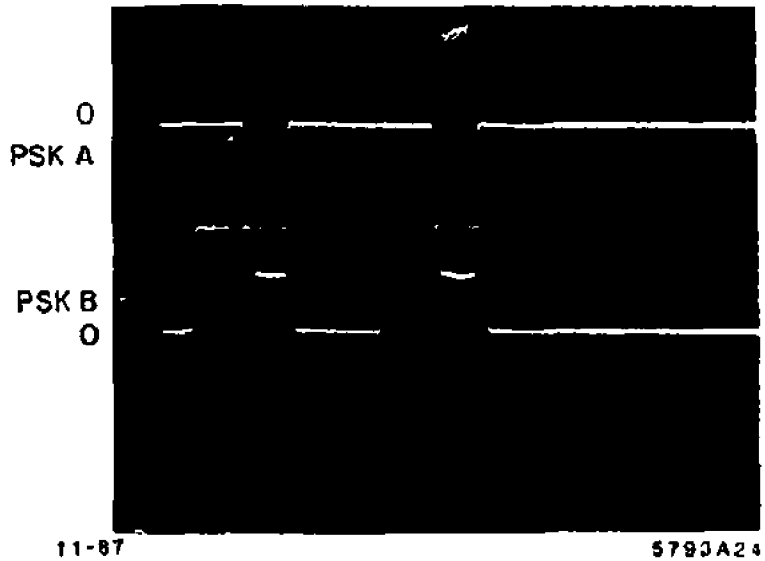


Fig. 13

Oscillogram of the PSK modulation waveforms for a 2-stage BEC for 2-period phase-coding. Horizontal scale: 100 ns/div.

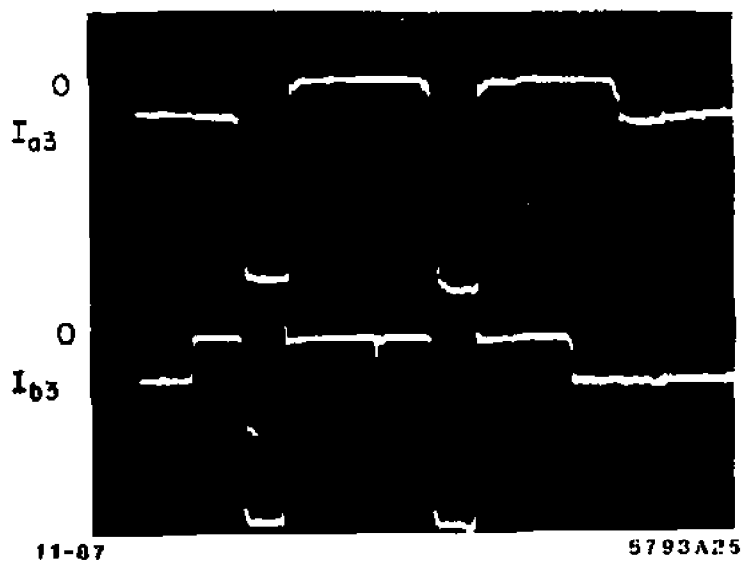


Fig. 14

Oscillogram of the outputs of a 2-stage BEC for CW inputs with 2-period phase-coding. Horizontal scale: 100 ns/div.

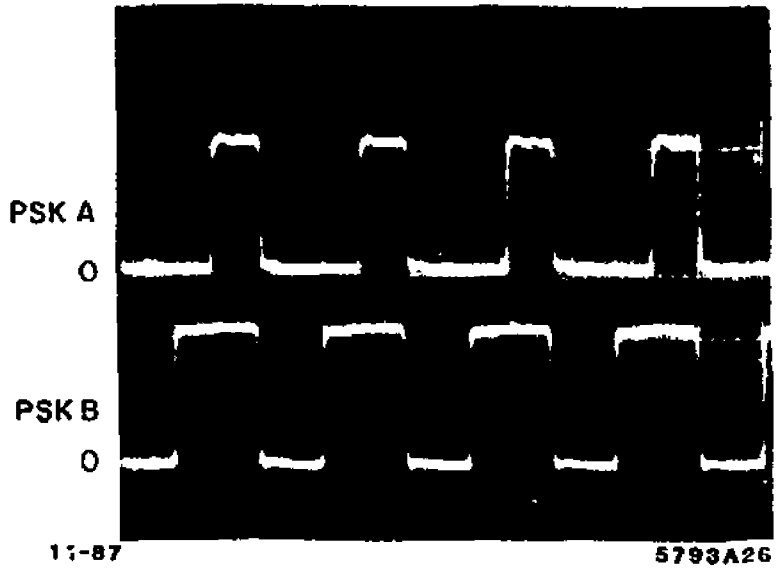


Fig. 15

Oscillogram of the PSK modulation waveforms for a 2-stage BEC for repetitive-period phase-coding. Horizontal scale: 100 ns/div.

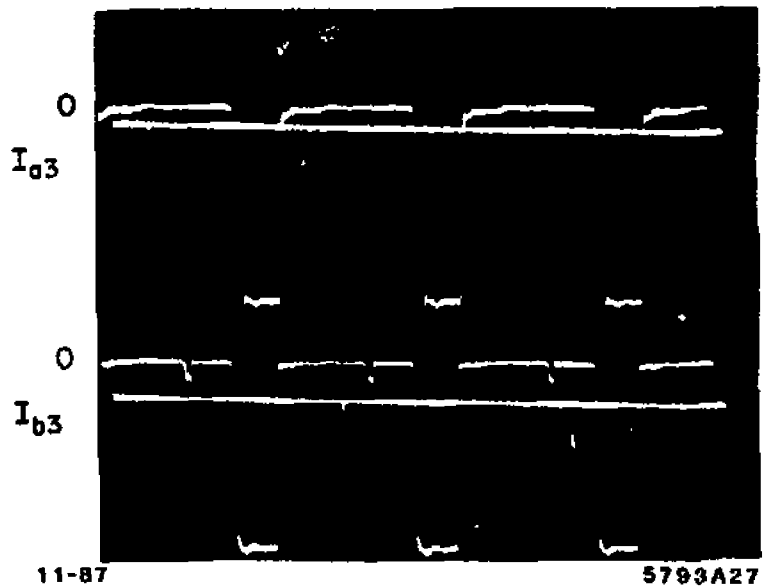


Fig. 16

Oscillogram of the outputs of a 2-stage BEC for CW inputs with repetitive-period phase-coding or no coding (straight horizontal traces). Repetitive-period phase-coding results in the maximum possible repetition rate, which for a 2-stage BEC corresponds to a 25% duty cycle at the output. Horizontal scale: 100 ns/div.

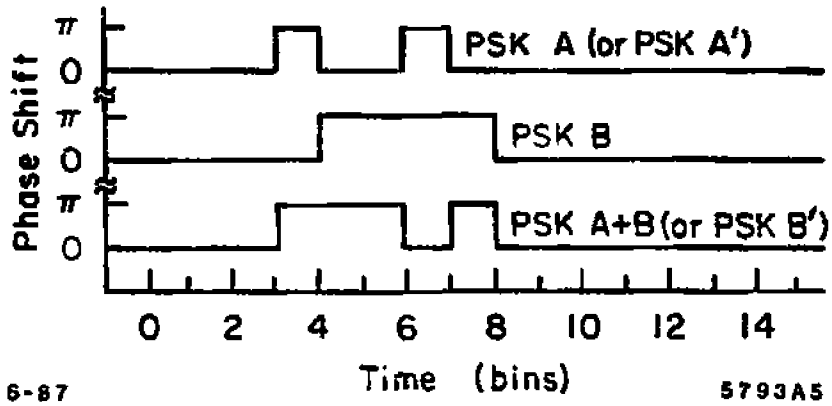


Fig. 17

Phase coding for a 3-stage BEC. PSK A and PSK A & B phase modulate the inputs I_{a1} and I_{b1}, respectively, and are applicable for the configuration of Fig. 3a with the addition of a H_3 and a D_3.

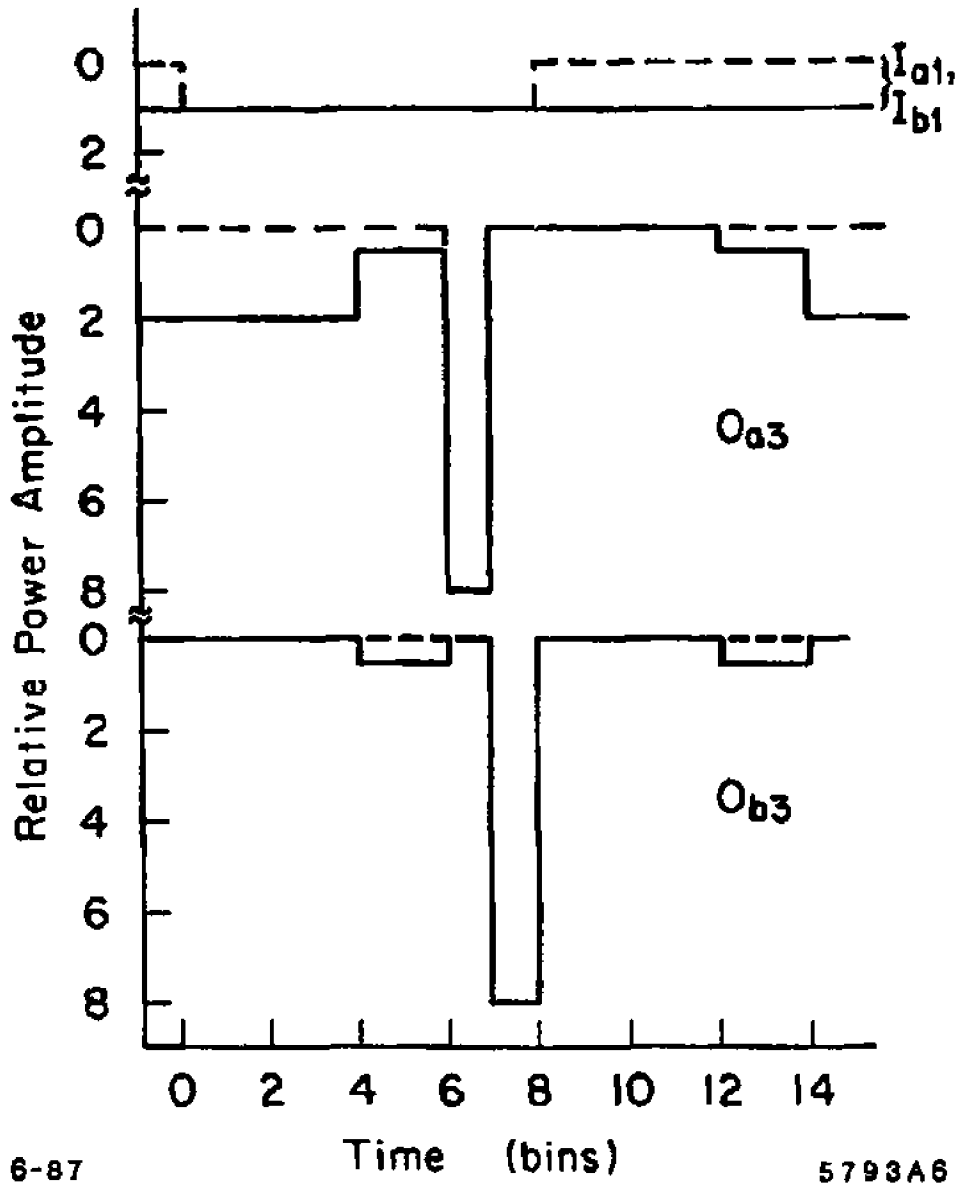


Fig. 18

Theoretical 3-stage BEC (minus a D_3) input and output powers. The solid lines indicate CW input power and the dashed lines indicate one modulation period for 3-stage BEC operation. The dashed lines follow the solid where only one is shown. If a D_3 is added, O_{a3} shifts to the right one time bin.

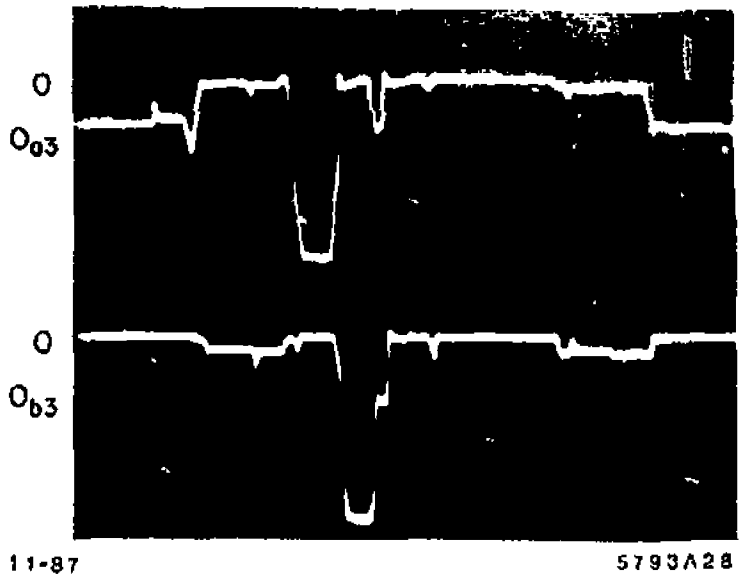


Fig. 19

Oscillogram of the outputs of a 3 stage BEC (minus a D_3) for CW inputs with single-period phase-coding. Horizontal scale: 50 ns/div.

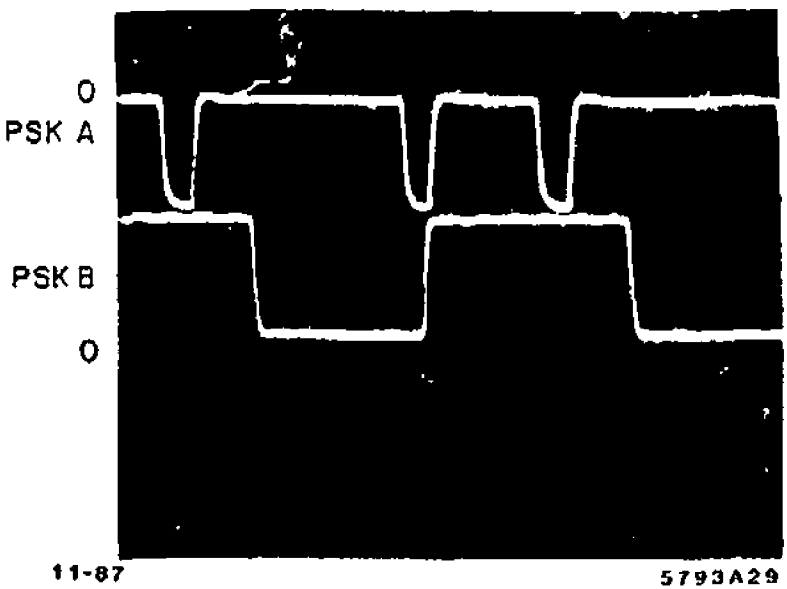


Fig. 20

Oscillogram of the PSK modulation waveforms for a 3-stage BEC for repetitive-period phase-coding. Horizontal scale: 50 ns/div.

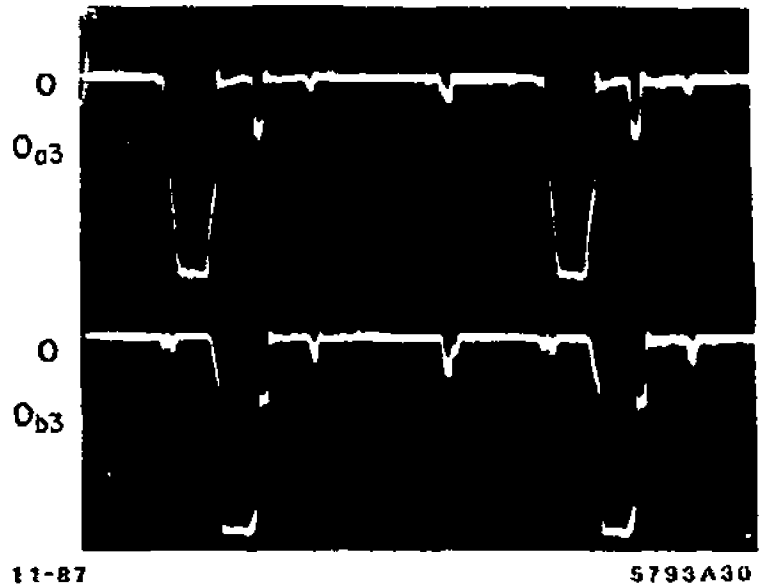


Fig. 21

Oscillogram of the outputs of a 3-stage BEC for CW inputs with repetitive-period phase-coding. Horizontal scale: 50 ns/div.

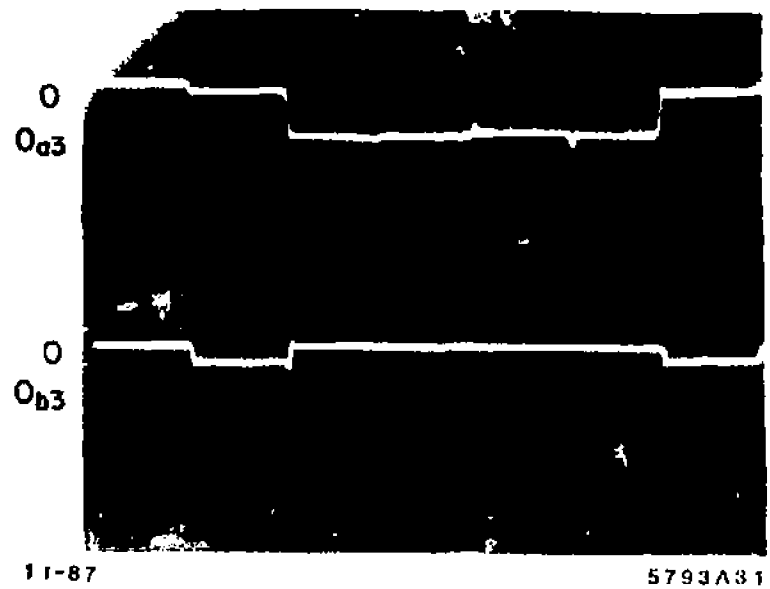


Fig. 22

Oscillogram of the outputs of a 3-stage BEC for pulsed inputs without PSK modulation. Horizontal scale: 50 ns/div.

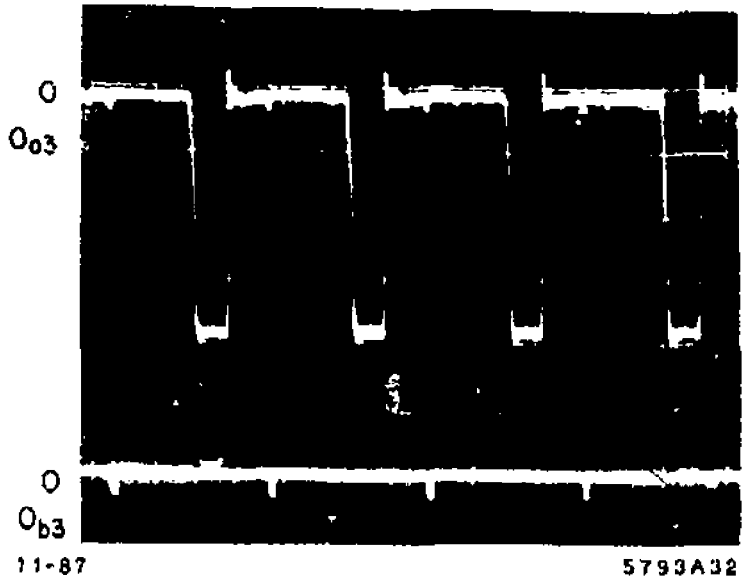


Fig. 23

Oscillogram of the outputs of a 3-stage BEC for CW inputs with 2-stage BEC repetitive-period phase-coding. Horizontal scale: 100 ns/div.

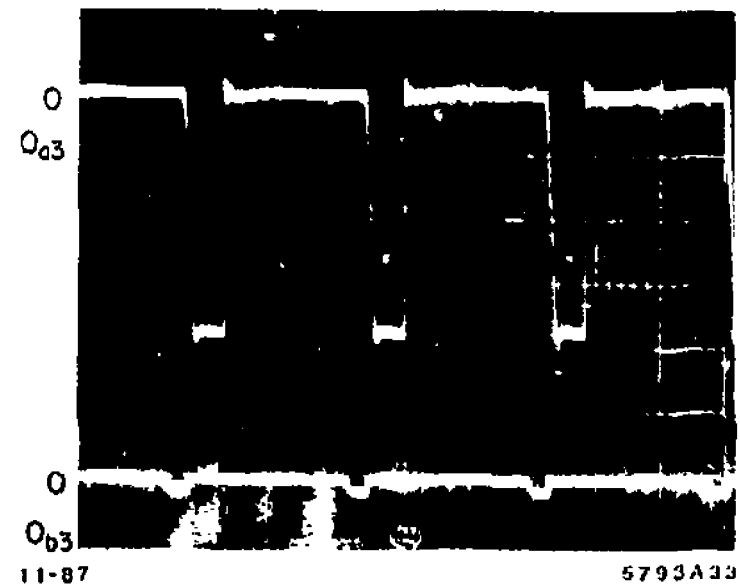


Fig. 24

Oscillogram of the outputs of a 3-stage BEC for CW inputs with 2-stage BEC increased-repetitive-period phase-coding. Horizontal scale: 100 ns/div.

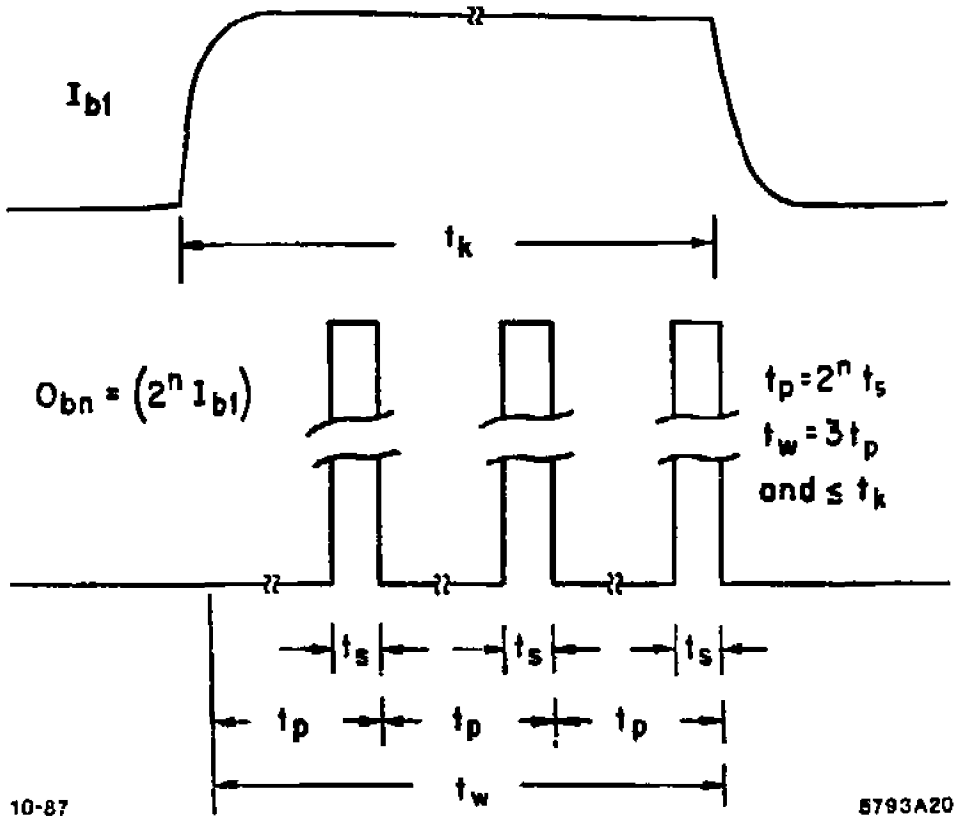


Fig. 25

A klystron output pulse and a 3-period, compressed, pulse train out of a BEC fed by the same klystron output pulse.

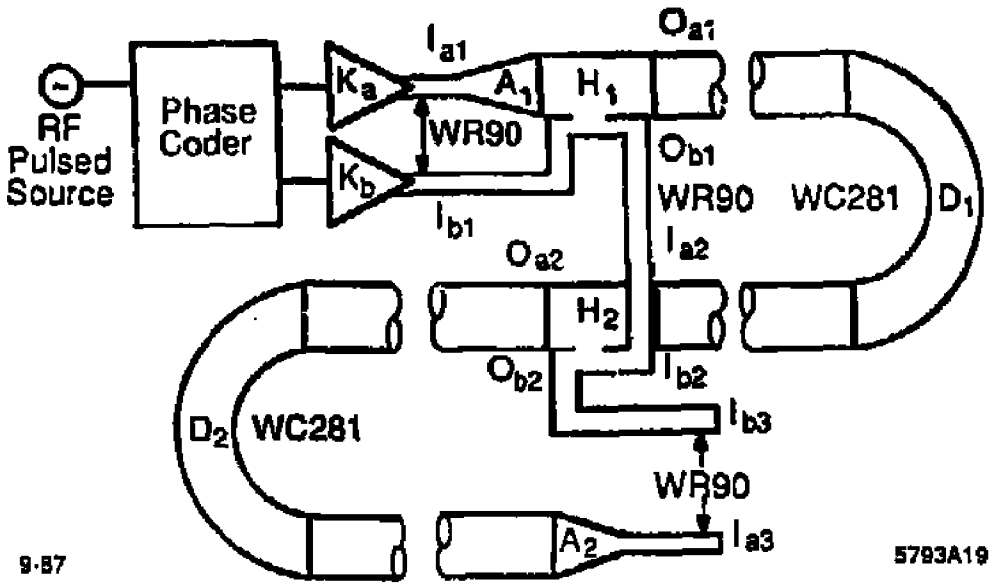


Fig. 26

A high-power, 2-stage BEC.