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DEVELOPMENT OF HIGH EFFICIENCY (14%) SOLAR CELL ARRAY MODULE

Third Quarterly Report for July 15—November 15, 1979

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Work Performed Under Contract No. NAS-7-100-955217

Optical Coating Laboratory, Inc.
Photoelectronics Division
City of Industry, California

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Solar Energy

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THIRD QUARTERLY REPORT

FOR PERIOD COVERING
15 JULY 1979 TO 15 NOVEMBER 1979

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P.A. ILES, S. KHEMTHONG, S. OLAH, W.J. SAMPSON, AND K.S. LING

JPL CONTRACT NO. 955217

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"The JPL Low-Cost Silicon Solar Array Project is sponsored by the U.S. Department of Energy and forms part of the Solar Photovoltaic Conversion Program to initiate a major effect toward the development of low-cost solar arrays. This work was performed for the Jet Propulsion Laboratory, California Institute of Technology by agreement between NASA and DOE."

ABSTRACT

Most effort was concentrated on development of procedures to provide large area (3" diameter) high efficiency (~15.5% AM1, 28°C) P/N solar cells. These efficiencies had been obtained for 2x2 cm area cells, but tests showed that the problem was not reduced silicon quality near the edges of the larger slices. The problems were in optimizing the back-surface field (BSF) process, and its possible interaction with the shallow P+ layer formation. Towards the end of this reporting period a promising process sequence had been identified and is being tested. The module design has been finalized. One hundred and twenty (120) cells will be connected eight (8) in parallel and fifteen (15) in series. The designs and tooling phases have been completed and are awaiting completion of the cells.

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1.0 INTRODUCTION

The goal of the program is to design, fabricate and deliver six (6) high efficiency modules, approximately 2' x 4', with a minimum output of 90 watts at AM1 and 28°C, and with the design goals of 14% overall efficiency. The modules are to use P+/N cells, and most of the effort to date has been to develop procedures to make large area (45.5 cm^2) P+/N cells of adequate efficiency (~15.5% AM1, 28°C). The complementary effort has designed the array layout, and developed tooling for array fabrication, principally for interconnections, white reflecting back surface, back contact soldering machine, AR contact tooling, and assorted tooling for handling and testing, especially for a limited production run.

2.0 TECHNICAL DISCUSSION

2.1 Background

Early work included the possibility that either N+/P or P+/N cells could be used to achieve the array power goals. However, to provide a possible use for N-type silicon should this type be available at low cost in the future, JPL decided that the main emphasis on this contract should be on P+/N cells. There have been some reports in the literature which showed high performance from the P+/N structure (references 1-3). Generally these results were achieved on cells ~4.5 cm^2 area. In 1970, lithium-doped P+/N cells (made by Heliotek or Centralab (1)) achieved 15% AM1, without advantage of some of the later process optimization, including large active area with very fine grids, surface texturing or advanced AR coatings. In 1977, RCA (2) reported cells with 17% AM1, and in 1978 Sandia (3) P/N cells exceeded 17%. In recent

years, apart from some interest in improved concentrator cells using the P+/N structure most effort has been given to N+/P cells. This was understandable, because this configuration is more radiation resistant for space uses, and also is suited to the probable type (P-type) of future low cost silicon sheets. For the latter, the reduced costs will be achieved partly by fewer purification steps, and boron and aluminum (both acceptors) are the most likely dominant impurities which will remain. The experience with high efficiency, large area (45.6 cm^2) N+/P cells led to the choice of a P+NN+ structure, with the N+ processing selected to provide a back surface field (BSF) in addition to a surface N+ layer of increased doping to reduce contact resistance. Again by analogy with earlier work, the target resistivity of the N-silicon was chosen as ~10 ohm-cm, this higher resistivity giving the chance of high Voc (from the BSF) along with enhanced Isc from the higher starting minority carrier diffusion length, and also enhancement of the diffusion length by the BSF.

2.2 Comparison of N/P and P/N Configurations

Theoretically, there is no reason why either of the two configurations N/P or P/N should have higher efficiency. They both use silicon of equivalent quality, and consideration of the main photovoltaic properties confirms this evidence.

Jsc - Depends mainly on diffusion length, and in theory and practice, both N and P silicon can have high values. The other factors (reflectance, diffused layer quality) are similar. This equivalent of Jsc is seen in the similarity between the spectral response areas (Figure 1) for good quality cells of each type.

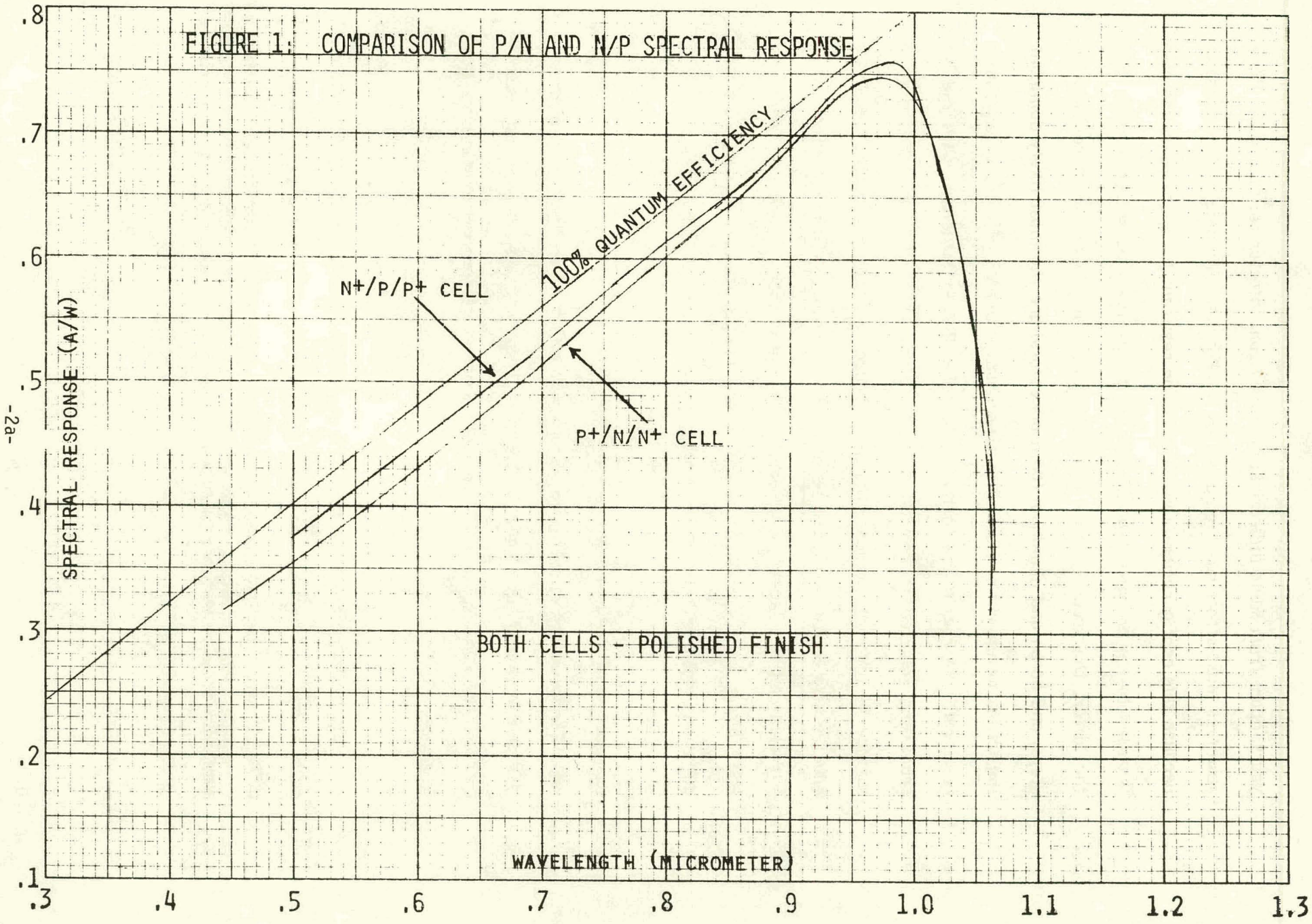


FIGURE 1: COMPARISON OF P/N AND N/P SPECTRAL RESPONSE
SPECTRAL RESPONSE (A/W)
WAVELENGTH (MICROMETER)
100% QUANTUM EFFICIENCY
N+/P/P+ CELL
P+/N/N+ CELL
BOTH CELLS - POLISHED FINISH
.8
.7
.6
.5
.4
.3
.2
.1
.3
.4
.5
.6
.7
.8
.9
1.0
1.1
1.2
1.3

Voc - With or without BSF, Voc values for equivalent bulk-doping levels are close (in theory, Voc for the P/N structure is slightly greater than that for N/P cells).

CFF - This is determined mainly by the series and shunt resistances, and these can be optimized in similar fashion for both structures. Thus Pmax which is given by the product Isc . Voc . CFF is equivalent, as is the efficiency. Figure 2 shows I-V curves (at AM0) for good cells of the two types.

2.3 Choice of Process Sequence

By analogy with earlier work, also with current high efficiency N/P cells the BSF option was chosen. The similarities in process sequences can be seen in Tables 1 and 2 which show the flow charts for N+/P cells of either BSF or P+ option, compared to that for P+/N cell.

2.4 Cell Design

The array design called for the use of 3" diameter (45.6 cm^2 area) cells. This cell size follows current solar cell array practice, and allows the use of standard wafer handling and processing equipment, and current cell technology. However, this choice imposed some limitation on the processes used, and increased the difficulty of achieving high efficiency. The grid contact design for the cell (with a center contact for interconnection) is suitable for sheet resistances ~100 ohm/square, and is shown in Figure 3.

2.5 Choice of Silicon

It was decided to use in-house Czochralski N-ingots of 3" diameter. Outside purchased-ingots, especially when float-zone refined often have

FIGURE 2

AMO I-V CURVES FOR P/N AND N/P CELLS

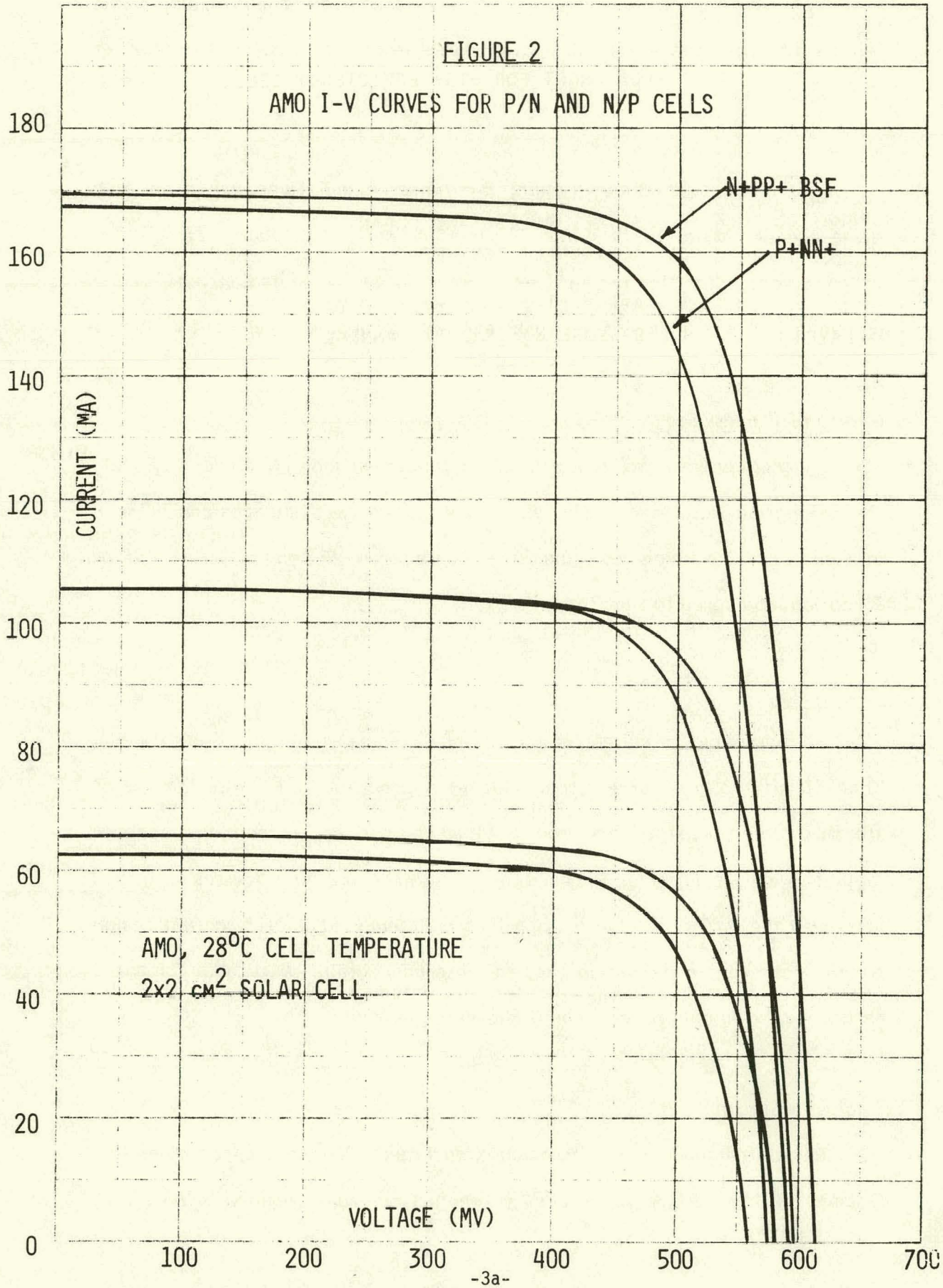


TABLE 1

FLOW CHART FOR HIGH EFFICIENCY CELLS

$N^+ P^+ P$

SILICON PREPARATION	1. GROW INGOT, P-TYPE	BSF 7-14 OHM-CM	P+ 1-3 OHM-CM
	2. SLICE, POLISH AND CLEAN		
	2A. (OPTIONAL) TEXTURE		
N^+ LAYER	3. APPLY DIFFUSION MASK TO BACK		
	4. DIFFUSE N^+ (FRONT), ANNEAL		
	5. HF CLEAN		
P^+ LAYER		BSF	P+
	6.	SCREEN PRINT ALUMINUM ON BACK	6. EVAPORATE ALUMINUM
	7.	BAKE	7. HEAT TREAT
	8.	ALLOY ALUMINUM (P+)	8. REMOVE EXCESS ALUMINUM
	9.	REMOVE EXCESS ALUMINUM AND CLEAN	9. CLEAN
CONTACTS	10. FRONT CONTACT MASK (PHOTORESIST)		
	11. EVAPORATE FRONT CONTACT (TITANIUM-PALLADIUM-SILVER)		
	12. EVAPORATE BACK CONTACT (ALUMINUM, TITANIUM-PALLADIUM-SILVER)		
	13. CONTACT BUILD-UP (OPTIONAL)		
COATING	14. CUT TO SIZE, CLEAN (IF REQUIRED)		
	15. EVAPORATE AR COATING		
	16. SINTER (CONTACTS, COATING)		
	17. MECHANICAL INSPECTION		
	18. ELECTRICAL TEST		

TABLE 2

FLOW CHART FOR HIGH EFFICIENCY CELLS

P^+ N N^+

		BSF	N^+
SILICON PREPARATION	1. GROW INGOT, N-TYPE	7-14 OHM-CM	1-3 OHM-CM
	2. SLICE, POLISH AND CLEAN		
	2A. (OPTIONAL) TEXTURE		
N^+ LAYER	3. APPLY DIFFUSION MASK TO FRONT		
	4. DIFFUSE N^+ (BACK), ANNEAL		
	5. HF CLEAN		
P^+ LAYER	6. APPLY DIFFUSION MASK TO BACK		
	7. DIFFUSE P^+, TACK-ON $\pm$ DRIVE-IN + ANNEAL		
	8. HF CLEAN		
CONTACTS	9. EVAPORATE BACK CONTACT (ALUMINUM, TITANIUM-PALLADIUM-SILVER)		
	10. FRONT CONTACT MASK (PHOTORESIST)		
	11. EVAPORATE FRONT CONTACT (TITANIUM-PALLADIUM-SILVER)		
	12. CONTACT BUILD-UP (OPTIONAL)		
COATING	13. CUT TO SIZE, CLEAN (OPTIONAL)		
	14. EVAPORATE AR COATING		
	15. SINTER		
	16. MECHANICAL INSPECTION		
	17. ELECTRICAL TEST		

APPLICATION		REVISIONS				
NEXT ASSY	USED ON	LTR	DCN	DESCRIPTION	DATE	APPROVED
		N/C	4574	NEW	1/27/78	

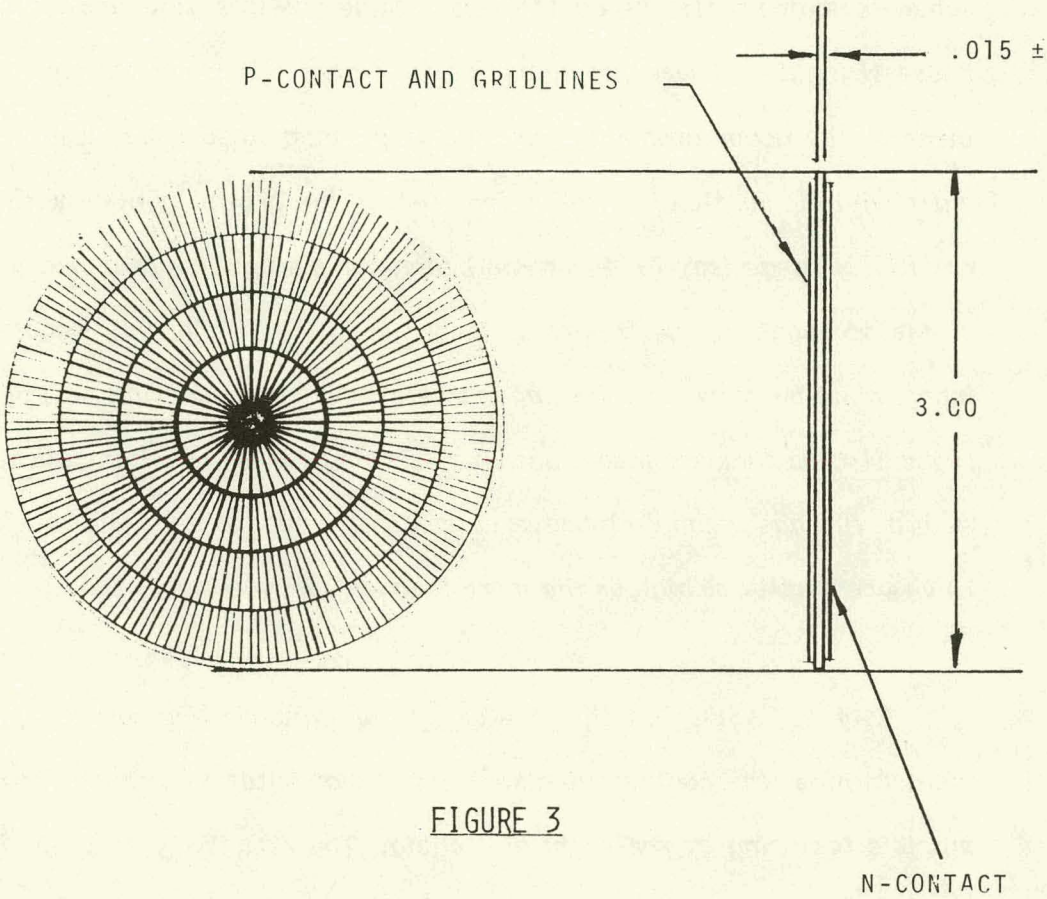


FIGURE 3

1.0 P-CONTACT OF .25 DIAMETER IS AT CENTER OF CELL

2.0 BOTH CONTACT-METALS ARE VACUUM DEPOSITED TITANIUM-PALLADIUM-SILVER

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES DECIMALS .X ± .XX ± .010 .XXX ± FRACTIONS ± ANGLES ± DO NOT SCALE DRAWING	DRAWN S. Khemthong 11/27/78 CHECK ENGR S. Khemthong 11/27/78 PROD QA	OCLI OPTICAL COATING LABORATORY, INC. PHOTOELECTRONICS GROUP 15251 Don Julian Rd. • City of Industry, Calif. 91746	
		HIGH EFFICIENCY 3" TERRESTRIAL CELL	
MATERIAL SILICON SOLAR TERRESTRIAL CELL		SIZE A	CODE IDENT NO.	DWG NO. A-202337
		SCALE NONE	REV N/C	SHEET 1 OF 1

slightly better quality than routine Czochralski crystals but this quality is not easily specified (or guaranteed), and the world wide shortage of silicon often increases the buying price severely, or stretches the delivery to prevent schedules being met. We could foresee some possible problems when using in-house N-ingots. These problems are first that the lower segregation coefficient of the donor atoms (phosphorus as planned for use but also arsenic and antimony) means that a smaller fraction of the grown ingot is within a given resistivity range (say 7-14 ohm-cm) than for similar ingots doped with boron, whose segregation coefficient is larger (~1.0). In addition, because the N-ingots must be grown in the same growers used for production runs of P-ingots, fewer N-type runs are made, and the "learning curve" which includes intagibles such as furnace clean up by several successive runs is not followed far enough to ensure quality as high as the more frequent P-type ingots.

Even so, ASEC felt that the quality of in-house N-ingots would be sufficient to meet the contract goals. The (100) orientation was used, to allow for possible texturing by preferential etching. The resistivity goal was 7-14 ohm-cm, although much of the material to date has had resistivity 20 ohm-cm.

2.6 Surface Finish

This N-ingots are sliced to 3" diameter wafers, and chemically polished to remove work damage, and to provide a smooth surface for good line definition, and more important to allow a good quality, shallow PN junction to be formed. Later tests showed that slightly increased overall output could be obtained by use of textured surfaces. In addition the texturing of the front surface only, provided an easy identification of front and back surfaces to prevent probing, or the addition of flats to the slices.

2.7 BSF Formation

We selected a phosphorus N+ diffusion to provide a suitable BSF on the N-silicon. The front surface was masked with SiO_2 to confine the N+ diffusion to the back surface. The goal is to provide a highly doped N+ layer to the back surface and to extend this layer sufficiently deep into the silicon to provide an effective BSF, giving carrier collection increase by preventing back surface recombination, and also an associated Voc increase. The specification of BS Fields even for N+/PP+ cells is still empirical, in that several methods can be successful often with varying effectiveness. Although the understanding of BSF requirements is increasing, with the chance of specific design specifications in the future, all of the development work on this contract, and probably the cell fabrication for the arrays will have been performed in this empirical phase. For this reason, we included several intentional variations of the N+ process step to seek the best method.

The N+ step cannot be viewed as a separate entity. For one thing, the N+ diffusion can possibly decrease the original silicon quality (especially the diffusion length) by the combination of the heating and cooling cycles, and the substitutional introduction of high densities of phosphorus, which is slightly mismatched in size with the replaced silicon atoms. On the other hand, with care, the use of some N+ diffusions, especially the $POCl_3$ process selected for use here, can provide some gettering of impurities, with increased diffusion length or even the chance of improved PN junction quality. In addition the front PN junction is provided by a later P+ diffusion, and the heat treatment (heating and cooling) needed for this step can interact with the effectiveness of the N+ layer (the best empirical diffusion cycles for both P+ and N+ are performed at comparable low temperatures ($875\text{-}900^{o}$)).

Thus several tests of different heating and cooling cycles, and of reversed order of performance were included in the tests described below. One test described below evaluated the use of ion implantation to provide either the N+ layer, the P+ layer or both layers on the same slice. We used the ion implantation and annealing procedures felt to be the best available from this method, but found the overall cell quality slightly lower than the all-diffused methods. For this reason, and to minimize additional delays caused by trying to optimize a process not performed in-house at ASEC, we retained the all-diffused structure.

For high quality N+PP+ BSF cells, the use of aluminum paste screened-on and alloyed has provided the best BSF cells to date (better than typical all-diffused or ion implanted). However, we did not have time in the present program to search for an equivalent alloy method to give the required N+ BSF.

Anticipating the conclusions reached at the end of this report, despite many empirical variations, we feel that the combination of the silicon used, and the best N+ and P+ diffusion provided a fairly good BSF. Even better BSF's would be possible with improved silicon quality.

In the production run, we plan to use some lower resistivity silicon (~2 ohm-cm) with P+ layer, to reduce the need to optimize the BSF process.

2.8 PN Junction Formation

Previous experience showed that the development of a reliable P+ diffusion step was essential to provide high efficiency, large area P+/N cells.

There are three boron sources which have given good cells, namely boron trichloride (BCl_3), diborane (B_2H_6) and boron nitride (BN).

Based on experience with photosensors and also diffused P+ layers in N+PP+ cells, we selected the BN method for use in this contract. The method uses BN discs, with surfaces conditioned, to provide a good B_2O_3 source for vapor transport to the N wafers held close to the BN discs. The 3" cells are held in a quartz boat with retaining areas, and some tests were run (rotating slices and re-diffusing) to ensure that there were no areas near the edge which were imperfectly diffused. As usual for high output solar cell diffusions, the requirements of very shallow junctions (~0.3 μm) and high sheet impurity concentrations raise the possibility of variable junction quality. In addition we required that the diffused layer be uniform across the whole slice surface. The cycle we chose gave good PN junctions although we selected a low temperature (to minimize process interactions) and this often gave a slightly higher sheet resistance than required for the grid designs selected (goal was 50-80 ohm/square, often had 100-150 ohm/square). The higher sheet resistance values, in addition to increasing the losses from lateral current flow to the grid lines, also tended to reduce PN junction quality slightly (by shunting). We also used a mask layer on the N+ layer to prevent P+ doping of this layer. In summary, the P+ diffusion step gave fairly repeatable results, with PN junction (and cell) performance adequate to meet the contract goals. Later tests showed that new large area BN discs were needed to give good total slice area uniformity.

2.9 Back Contact

After the two diffusion steps, the slices are cleaned to remove the diffusion glasses or mask layers, and then additionally cleaned to prepare the surfaces for contact application. We used the Ti-Pd-Ag contact system currently considered to be the best available, for reduced contact resistance, low grid line resistance, minimum interaction with the N+ and P+ regions and for probable long field life.

To obtain additional output from reflection and absorption of longer wavelengths (0.9-1.1 μm) which are not completely absorbed on passing through the silicon slice, we included a back surface reflector (BSR) layer, in this case using aluminum which has high reflectance in the near infrared, and which also is compatible with the Ti-Pd-Ag system. For the P+NN+ structure, there is additional caution needed when including this step, because Al when heated above 500°C can provide a P+ layer, which can give an adverse Schottky barrier on the N+ surface. However, in order to preserve the high infrared reflectance the Al should not be heated even above 400°C. Thus the sinter cycle used to improve contact coating adhesion and to minimize resistance between the contact metals and the silicon was set at 400°C -15 minutes.

2.10 Front Contact

The grid pattern selected for the P+NN+ cells (Figure 3) is designed to give low resistive losses for sheet resistances up to 90 ohm/square. Although in the array the eventual mesh interconnect to the center area will involve an additional shadow loss of ~1.5%, past experience with high efficiency 3"

diameter N+/P cells has shown that the increased CFF using the pattern selected can offset this additional shadow loss.

The grid pattern is formed by photolithography; which allows the use of narrow lines, with some cross lines (see Figure 3). To increase CFF, the silver layer evaporated on the silicon can be built up by electroplating. The silver layer on the front (and the back) can be directly interconnected by use of solder-coated copper mesh.

2.11 AR Coating

When the silicon surface is polished, the use of a multilayer AR coating (in this case TiOx plus Al_2O_3) can provide low reflectance over the cell response range. The coating layers are designed to provide good optical matching with the encapsulating materials, to retain low reflectance in the array. When the surface is textured, already the silicon reflectance is reduced, and the choice of the AR coating becomes less critical. However, we have retained the use of the MLAR on the textured surface, thus providing minimum reflectance. The resultant increase in cell current by using textured surface is ~1-2% above that of a polished surface with the MLAR coating.

2.12 Sintering

As described above, a sinter step, is used to increase adhesion of both contacts and coating. In addition this heat treatment can reduce ultraviolet absorption in the coating, and can also reduce contact resistance. As mentioned, heating at $400^{o}C$ for 15 minutes was found to be adequate to perform these functions, and also to retain the high reflectance of the Al layer at the back contact, and to minimize any interaction of the Al and the N+ layer.

2.13 Electrical Test

All cells made were tested at AM1, 28°C, using JPL standard cells to calibrate the AM1 simulator. In addition some AM0 measurements were made on smaller area cells (4 cm^2) to provide additional information on the detailed photovoltaic properties.

It is planned to supply a number of typical P+NN+ cells to JPL, to serve as transfer standards, to check the array output measurements. This discussion has explained the choice of process step. The next section will survey the many tests run to decide on the optimum sequence. To focus attention on the contract goals, Table 3 shows the array and cell goals needed.

2.14 Tests Not Pursued Further

Use of Ion Implantation to Provide P+ Layer

Spire Corporation implanted B^{11} to form a P+ layer; the BSF was formed either by N+ diffusion (at ASEC) or by P^{31} implantation (at Spire). The best state-of-the-art values for ion energy and fluence were used (10-25 Kev, 2.5-5x$10^{15}/cm^2$) along with the best combined furnace annealing cycles. The best results (see Table 4) were obtained with the higher energy, higher fluence B^{11} implant, and the N+ diffused layer. However, the results did not show any advantage over all-diffused cells. Because further iterative tests between the two companies would be time-consuming, this option was discontinued for the present program.

Use of Hydrogen Injection During BN Diffusion

Literature reports suggested that improved consistency could be obtained with BN sources if hydrogen was injected with the other transport gases.

TABLE 3

ARRAY AND CELL GOALS

MINIMUM (90W ARRAY)

TOTAL MODULE AREA =	6890 cm^2
PACKING FACTOR =	79%
CELL OUTPUT REQUIRED =	0.701 W
(ASSUMING 7% REFLECTANCE GAIN)	
CELL EFFICIENCY =	15.4% ←
MDOULE EFFICIENCY =	13.1%

14% MODULE

MODULE OUTPUT =	96.4 W
CELL OUTPUT =	0.751 W
CELL EFFICIENCY =	16.5% ←

TABLE 4

ION IMPLANTATION TESTS, AM1 (45.6 cm^2)

TEST	BSF	P+	NO. CELLS	AVERAGE				BEST
				V_{OC}	J_{SC}	CFF	EFF.	EFF.
1. (A)	N+ DIFFUSED	B^{11} IMPLANT $2.5x10^{15}$ 10 KEV	10	558	33.1	.68	12.5	13.2
2. (B)	N+ DIFFUSED	B^{11} IMPLANT $5x10^{15}$ 25 KEV	10	570	33.6	.72	13.9	15.0
3. (A)	P^{31} IMPLANT	B^{11} IMPLANT $2.5x10^{15}$ 10 KEV	10	549	30.4	.65	11.0	11.4

(A) ANNEAL (850-30) + (500-60)

(B) ANNEALED DURING N+ DIFFUSION

Two tests were made, where a small amount of hydrogen (4% by volume) was added to the $N_2 + O_2$ gases during the boron diffusion at 900°C. In test #1, the wafers were given a drive-in cycle in $H_2 + O_2$ atmosphere at 900°C for 25 minutes; in test #2, the drive-in time was 10 minutes. These tests did not show promise, and further tests with hydrogen injection were not pursued, particularly since the tests involved interaction with production diffusion furnaces, the only available equipment for boron diffusion of 3" wafers.

2.15 *Tests Resulting in 4 cm^2 Area Cells*

Table 5 summarizes effects of variations in the processes on the properties of 328 cells. The range of "average" parameters for each test is given, with a "best" column showing the potential of the particular sequences. Both the N+ and P+ schedules were varied over small ranges of temperature, times and cooling rates. There was not much difference in this range, and some combinations showed good promise.

In test B, the effect of the BSF can be seen. This also illustrates the danger in using higher resistivity silicon if the BSF process does not give the expected enhancement.

Several attempts at reversing the order of the P+ and BSF processes (i.e. performing the shallow P+ diffusion first) Tests C did not show any advantage over the order given in Table 2. Tests D selected the most promising schedules from the series of tests A, and confirmed that they could give good efficiency cells.

TABLE 5

4 cm^2 CELLS, AM1 READINGS

TEST	NO. CELLS	AVERAGE V_{OC} (mV)	AVERAGE J_{SC} (mA/cm^2)	AVERAGE CFF	AVERAGE EFF. (%)	BEST EFF. (%)
(A) VARIOUS N+, P+ SCHEDULES (SMALL RANGE)	96	500-596	34.0-36.6	.68-.75	14.2-16.5	15.1-16.6
(B) TEST OF BSF						
NO BSF	36	520	34.6	.67	12.2	12.9
+ BSF	70	585	36.6	.73	15.6	16.5
% IMPROVEMENT		12.5	5	9	28	
(C) REVERSED SEQUENCE (VARIOUS N+, P+ SCHEDULES)	102	555-575	35.9-36.6	.71-.74	14.2-15.4	14.5-15.6
(D) SELECTED N+, P+ SCHEDULES	24	588	37	.73	15.9	16.3

TOTAL 328

2.16 *Tests Resulting in 45.6 cm^2 Area Cells*

To provide realistic cell efficiencies, 258 cells of 45.6 cm^2 area were fabricated in a series of tests shown in Table 6. Tests E, F and J repeated tests A and D above. Tests G, I and K varied the BN procedures, where careful annealing after diffusion gave slight improvement. Test H showed that when the other processes were effective, a textured surface can give slight improvement over the results from polished surface. Test L was a limited "extended" run (~100 cells), with direct comparison of textured and polished cells with the "best" process sequence. The results illustrated again the advantge of the textured surface (13.8% versus 12.8%), but overall gave disappointing results. The fault was traced to inadequate BN diffusion, and it was necessary to order new large area BN discs for the production run. Figure 4 shows the histogram distribution of efficiencies for the two surface finish groups.

2.17 *Conclusions*

The process sequences selected showed promise, but the consistency was not as good as expected. Several reasons were probable causes, including

(a) Sometimes the BN discs did not produce a sufficiently well-diffused layer all across the 3" slices. This led to the possibility of shunted cells, and for reasons not well understood, reduced output of cells which were not seriously shunted by reducing the effectiveness of the BSF process. One reason may be the inability of the boron diffusion process to provide sufficient gettering to increase minority carrier diffusion length.

(b) There were a few cases where some cell shunting was observed; this was probably leakage of impurities through the protective masks used on the opposite face from that being diffused.

TABLE 6

45.6 cm^2 CELLS, AM1

TEST	NO. CELLS	AVERAGE V_{OC}	AVERAGE J_{SC}	AVERAGE CFF	AVERAGE EFF.	BEST EFF.
(E) LIKE (A)	8	590	34.0	.75	15.2	15.6
(F) LIKE (D)	24	560	34.6	.63*	12.2	13.5
(G) TO REDUCE $R_{\square}$						
HIGHER BN TEMPERATURE	46	570-588	32.4-33.9	.70-.72	13.3-13.9	13.6-14.6
(H) TEXTURED CELLS (VARY ANNEAL)						
SLOW PULL (BN)	8	496	33.0	.62	10.0	10.6
SHUT OFF (BN)	9	583	37.8	.71	15.7	16.2
(I) POLISHED (VARY ANNEAL)						
SLOW PULL (BN)	10	525	30.5	.71	11.4	11.9
SHUT OFF (BN)	10	577	33.6	.72	14.1	15.2
BN SLOW PULL, ROTATE, REPEAT	10	556	33.6	.72	13.6	14.0
(J) SLIGHT N+, P+ MODIFICATION (POLISHED)	15	584	35.3	.73	15.1	15.6
(K) ANNEAL AFTER P+ (POLISHED)						
NO ANNEAL	5	564	34.0	.71	13.6	13.9
+ ANNEAL	14	566	34.5	.72	14.2	15.0
(L) EXTENDED RUN						
POLISHED	44	550	34.6	.67	12.8	14.3
TEXTURED	65	535	35.5	.70	13.8	14.7

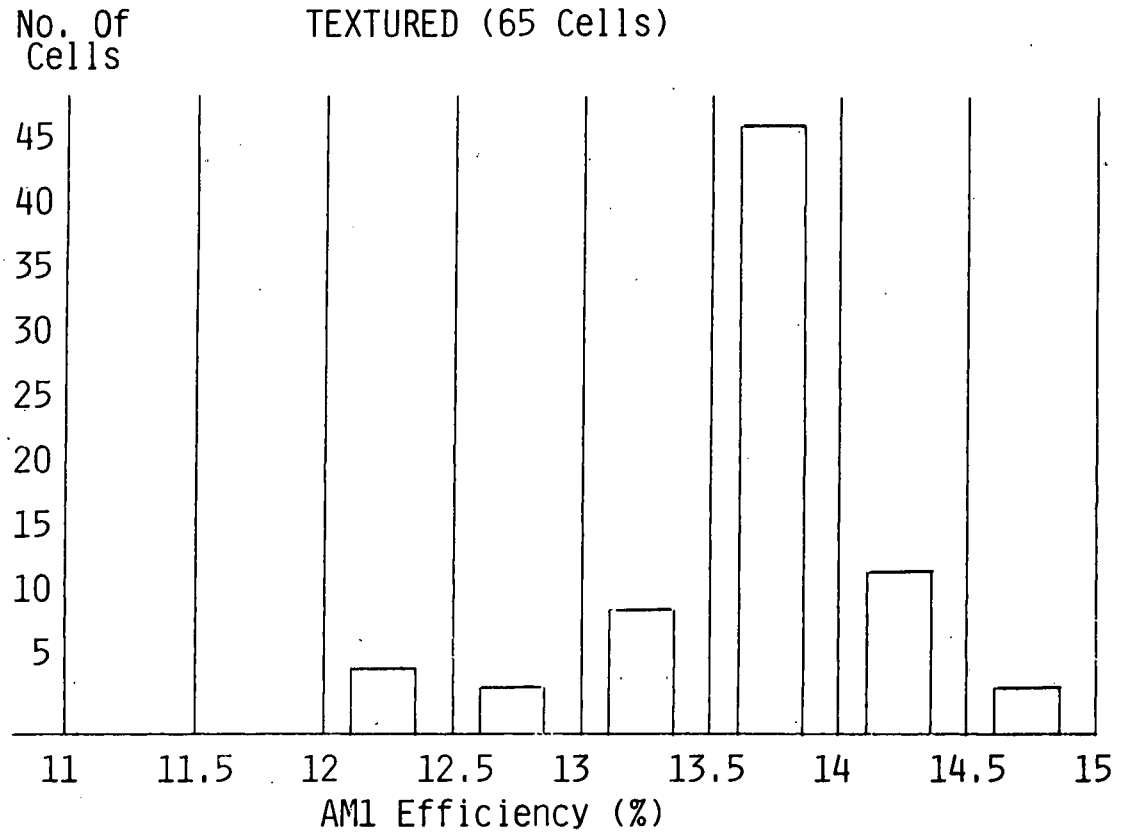
TOTAL 258

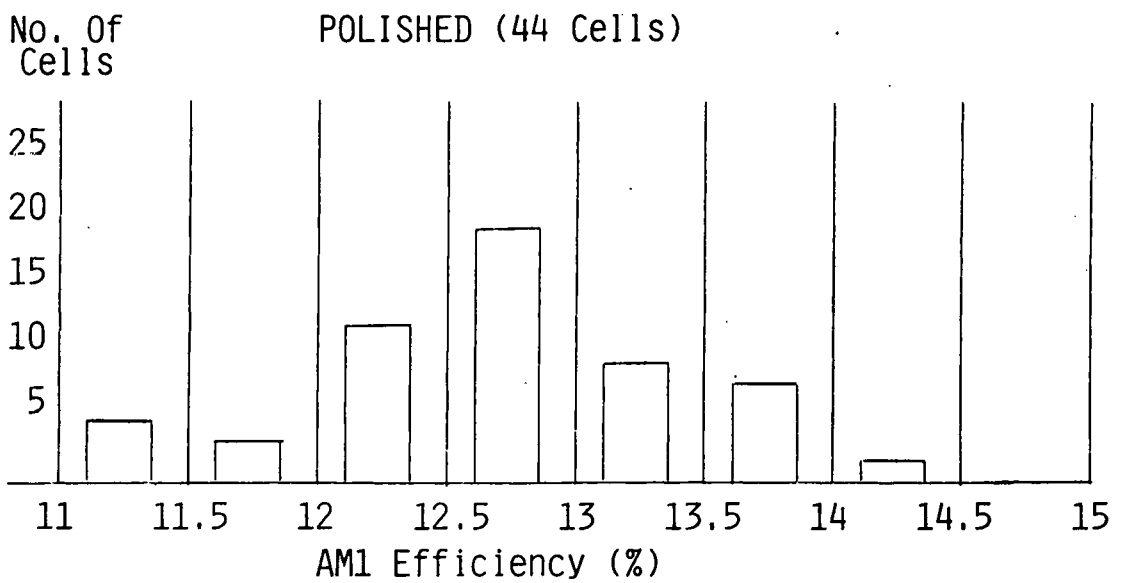
*SEVERELY SHUNTED. TRIMMED EDGES - NO IMPROVEMENT.

FIGURE 4

EXTENDED RUN

HISTOGRAM DISTRIBUTION OF AM1 EFFICIENCY (at 450 mV)





(c) *Mostly high resistivity (~20 ohm-cm) silicon was available and used. In combination with (a), this could lead to serious reduction in output if the BSF process was not fully effective. A careful resistivity check (identical processing with 3 ranges 7-10, 11-13, 13-20 ohm-cm is planned).*

(d) *Early work on textured surfaces often showed up to 5% improvement in Jsc, accompanied by slight reduction in Voc and CFF. With careful processing, about 4% net improvement in efficiency could be obtained.*

(e) *To minimize array losses, tooling was tested to mask the center contact thoroughly during the AR coating step. This ensured that increased resistance was not caused during the interconnection soldering.*

(f) *The "frozen" process chosen for the deliverable arrays is considered promising for exceeding the minimum array needs.*

(g) *A brief test is scheduled to evaluate the use of lower resistivity (~2 ohm-cm) silicon with an N+ layer. This design may not have ultimate output as high as the BSF design, but also has reduced sensitivity to the process parameters, also the lower resistivity range silicon can be grown more repeatably.*

(h) *On examining the better results achieved, in cell efficiency, and in the separate highest values for Jsc, Voc and CFF, we conclude that with further fine-tuning, P+/N cells can be made with at least as high output as the best N+/P cells*

3.0 ARRAY DETAILS

3.1 Production Tooling

All have been completed.

3.2 Hardware

Module components such as Sunadex glass, aluminum frame, junction boxes, terminals, etc., are all in house.

4.0 MILESTONE

4.1 The milestone chart is attached.

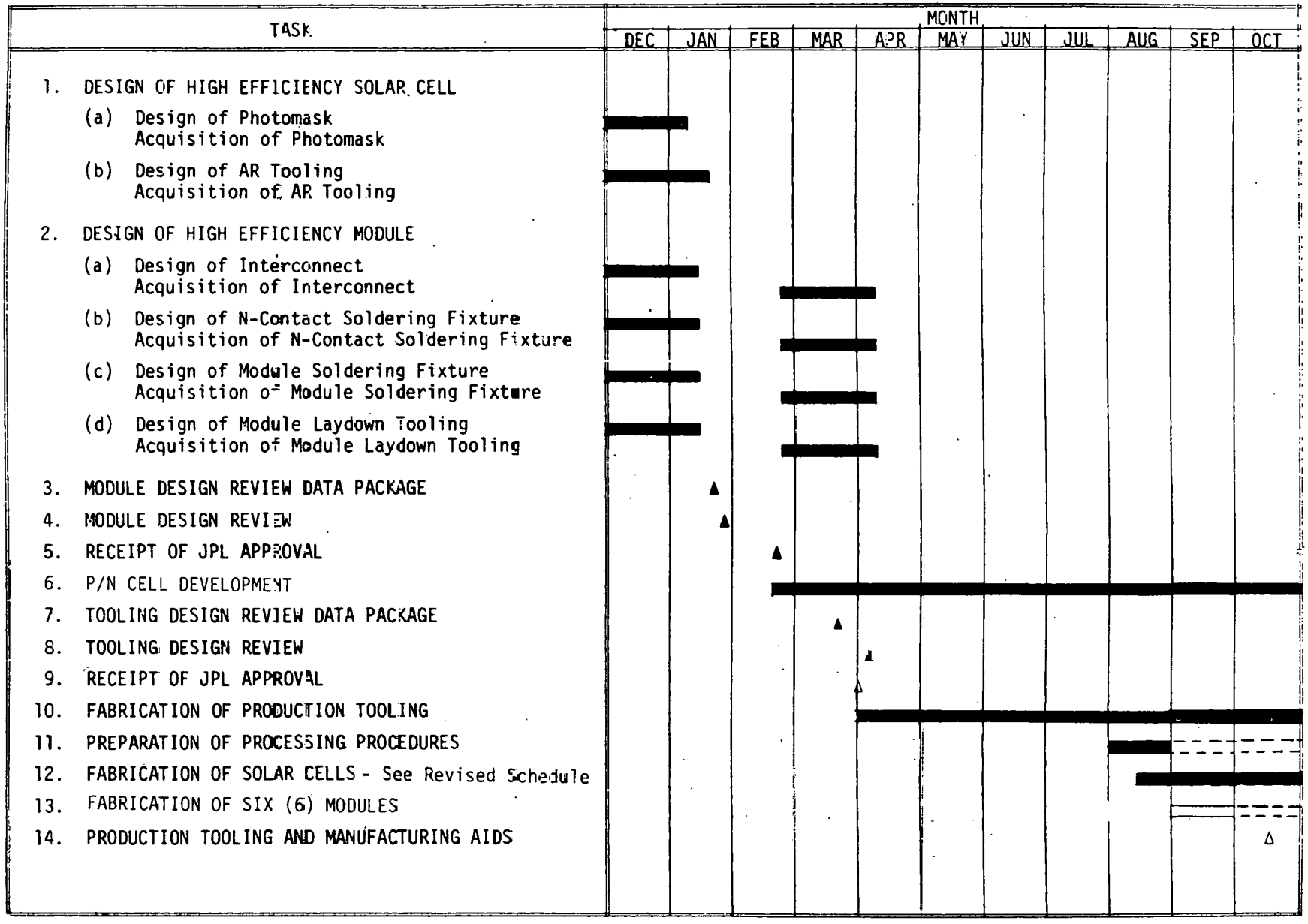
4.2 A revised schedule is attached.

5.0 REFERENCES

1. Various work under JPL Lithium Program (unpublished).
2. "P/N High Efficiency Silicon Solar Cells", M.S. Bae and R.V. D'Aiello, Appl. Phys. Lettr, 31, No. 4, 1977, p. 265.
3. "High Efficiency P+NN+ Back-Surface-Field Silicon Solar Cells", J.G. Fossum and E.L. Burgess, Appl. Phys. Lettr, 33, No. 3, 1978, p. 238.

9/18/78
Revised: 12/22/78

PROGRAM PLAN



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PROGRAM PLAN

TASK	MONTH										
	DEC	JAN	FEB	MAR	APR	MAY	JUN	JUL	AUG	SEP	OCT
15. COST DATA FOR 5, 25, 50 KW										△	
16. COST DATA PER SAMICS											△
17. BASELINE COST ESTIMATE	▲										
18. PROGRAM PLAN	▲										
19. MONTHLY FINANCIAL REPORT		▲		▲	▲	▲	▲	▲	▲	▲	▲
20. MONTHLY STATUS REPORT		▲		▲	▲	▲		▲	▲		
21. QUARTERLY REPORT					▲		▲			△	
22. INTERIM TECHNICAL REPORT	2 WEEKS AFTER RECEIPT OF R&D TESTING DATA FROM JPL										
23. FINAL TECHNICAL REPORT											
(a) Draft	2 WEEKS AFTER RECEIPT OF TESTING DATA FROM JPL										
(b) Final	30 DAYS AFTER RECEIPT OF JPL WRITTEN COMMENTS OF THE DRAFT FINAL REPORT										
24. PARTICIPATION IN TECHNICAL REVIEW ACTIVITIES											
(a) Program Review Meetings	AS REQUIRED										
(b) Program Design Review Meetings	AS REQUIRED										
(c) Project Integration Meetings	AS REQUIRED				▲						
(d) Workshops	AS REQUIRED										

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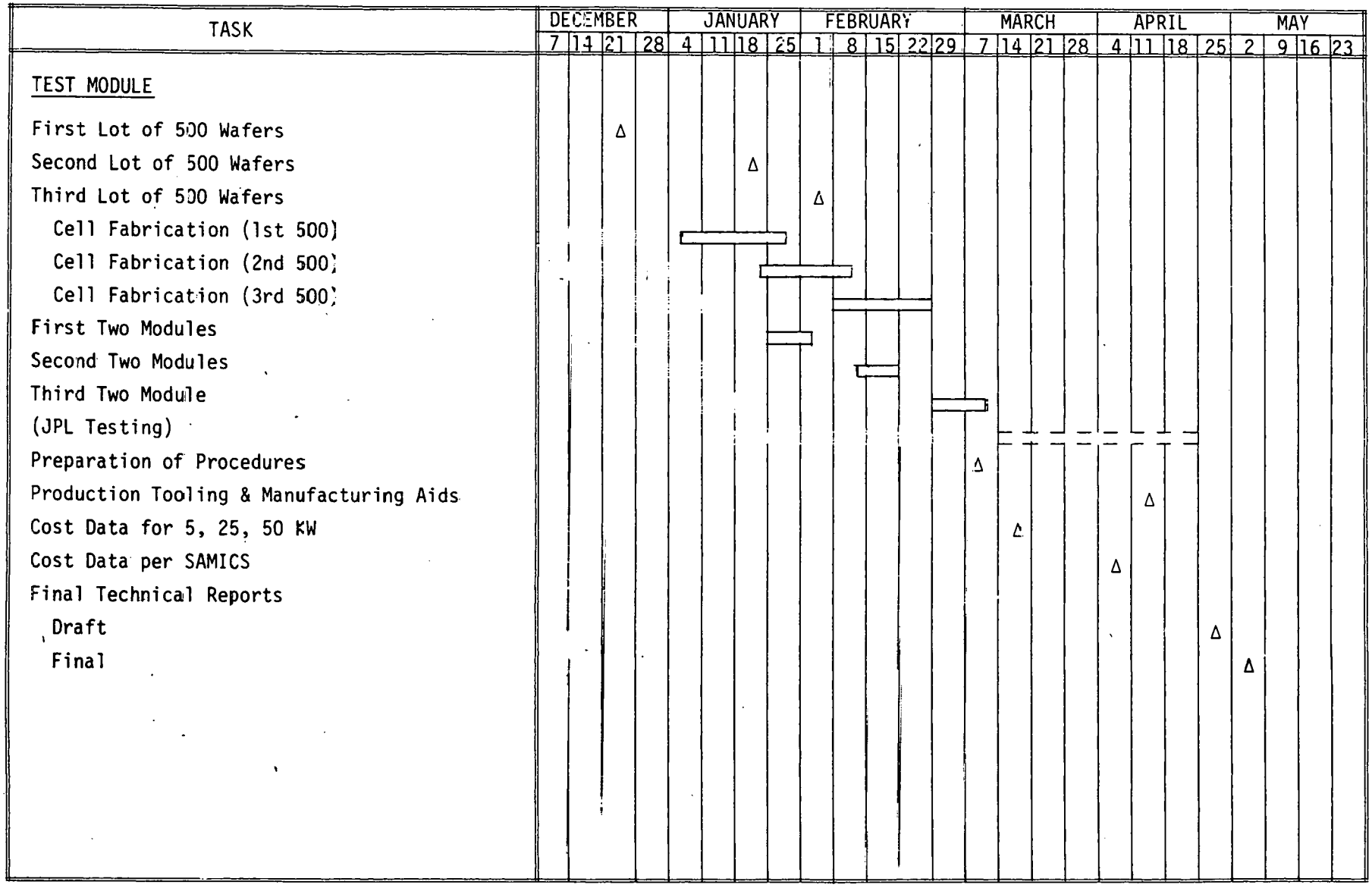
REVISED SCHEDULE

JPL CONTRACT NO. 955217



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29 November 79