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Design Analysis of Advanced Photovoltaic Technologies

A Subcontract Report

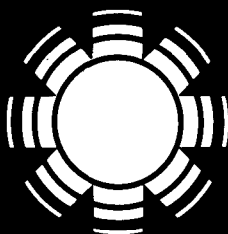
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**Prepared under Subcontract Nos. XF-1-1228-1
and XG-1-1064-1**



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Solar Energy Research Institute

A Division of Midwest Research Institute

1617 Cole Boulevard
Golden, Colorado 80401

Operated for the
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PREFACE

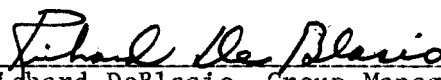
This document describes the work performed between June 1981 and April 1982 by BDM Corporation, Albuquerque, New Mexico, under SERI subcontracts No. XF-1-1228-1 ("Design Analysis of Advanced Photovoltaic Technologies") and No. XG-1-1064-1 ("Module Optimization Methodology for Advanced Photovoltaic Cells and Devices"). The SERI subcontract administrator was Margaret Lemke, technical monitor was Laxmi Mrig, and task manager was Richard DeBlasio.

The objective of this document is to combine two interrelated subcontract reports that address design and optimization methodologies for advanced photovoltaic cells and devices as related to module and system application designs. Four advanced photovoltaic material cells--polycrystalline silicon, amorphous silicon, CdS/CuInSe₂, and gallium arsenide--were evaluated for conceptual modeling and analysis with regard to residential and central station system design applications. In addition, a module optimization methodology is described in Appendix B along with the computer code PVMOC (Photovoltaic Module Optimization Code), to assist PV module designers using advanced PV material cells in evaluating the performance and cost of alternate designs.

When these studies were performed, available technical information on advanced PV cell parameters was utilized, and reasonable assumptions were made in performing the design analyses when data were not available. As advances in cell research evolve these parameters will likely change and therefore should be re-examined, and current information regarding assumptions utilized should be obtained when employing the design techniques provided in this document.



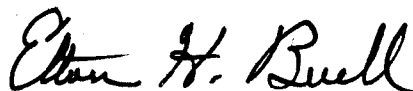
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SECTION 1.0

EXECUTIVE SUMMARY

1.1 OVERVIEW OF STUDY

The purpose of the Design Analysis of Advanced PV Technologies study is to provide guidelines and a methodology for channeling the development of advanced PV technologies along paths which will produce modules capable of being integrated into practical system applications. The program approach was to develop a methodology for designing and analyzing systems from advanced PV technologies, to exercise the methodology for selected advanced technologies, and then to generalize the results into guidelines for technology development and system design evaluation. Mature technologies were selected which have a high probability of achieving DOE/SERI advanced technology goals.

An overview of the program is shown in Figure 1-1. The program began with the selection of the advanced photovoltaic technologies to be evaluated. Next, detailed data was acquired describing the characteristics of the photovoltaic material to be evaluated. Conceptual designs of both the modules and systems were developed and the model implementation on PV-TAP [1] and SOLCEL II [2] followed the design process. The module conceptual designs were accomplished using the Module Optimization Methodology [3]. Detailed evaluation of the performance, cost, reliability, and safety of the photovoltaic technology and system was performed using PV-TAP and SOLCEL II and analysis and design guidelines were developed. The installation of PV-TAP at SERI was accomplished at the outset of the program and was used to support modeling and analysis in this program.

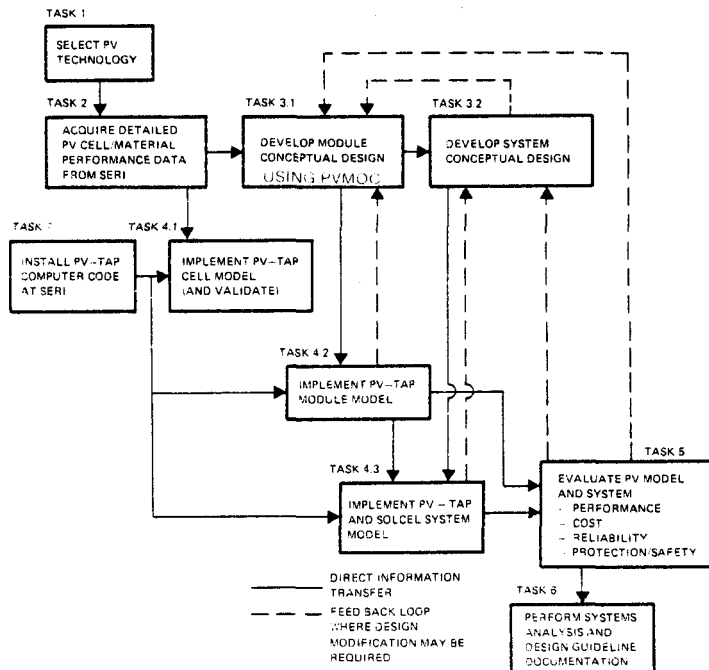


Figure 1-1. OVERVIEW OF PROGRAM

1.2 CONCLUSIONS AND RECOMMENDATIONS

The conclusions and recommendations presented here were derived from design and analysis on specific polycrystalline silicon, amorphous silicon, cadmium sulfide, and gallium arsenide technologies, and apply specifically to these technologies. Where appropriate, however, the conclusions and recommendations have been generalized to all advanced PV technologies. For each conclusion or recommendation, subsections of this report which contain supporting discussions are listed in parentheses. Detailed discussions of results and conclusions are contained in Section 5.0.

1.2.1 Cell Characteristics (2.1, 3.1.3.1, 5.2.1.1, 5.2.1.4)

Before a practical module can be developed for a particular advanced technology, a large number of cell characteristics (electrical, thermal, mechanical, etc.) must be known. Most of these are not yet available for the PV cell technologies assessed. Of particular interest to module electrical design is reverse bias susceptibility of cells (5.2.1.4). This information is not available for any of the cells assessed. Reverse breakdown voltage, maximum allowable temperature, failure mechanisms, and probability of failure must all be determined by analysis and test to determine bypass diode requirements and feasibility of paralleling cells.

1.2.2 Cell Fill Factor Considerations (5.2.1.1)

The cell technology should have a good fill factor (≥ 0.7), and a high voltage ratio ($V_{MPC}/V_{OCC} > 0.8$) to facilitate interface of the array with the input voltage limits of the DC-AC inverter.

A very high current ratio ($J_{MPC}/J_{SCC} > 0.92$) is not desirable because this increases power dissipation in reverse bias if shadowing should occur and a very high fill factor ($FF > 0.8$) is also not desirable because this reduces module efficiency under parameter variation conditions.

Therefore, a low series resistance is more desirable than a high shunt resistance (although a low shunt resistance should also be avoided because it reduces efficiency).

1.2.3 Current to Voltage Ratio (5.2.1.2)

The ratio of peak power current to peak power voltage should be as low as possible ($I_{MPC}/V_{MPC} \sim 5 \text{ A/V}$ for $80\text{-}100 \text{ cm}^2$ single crystal silicon) to reduce the width and thickness required for module metallization and conductor runs, and to improve modularity in residential applications and improve tolerance to photocurrent variations by increased paralleling. Modularity is enhanced by reducing the power of the subarray so that the array can be sized to fit

the residential roof area. The subarray is composed of modules connected in series to develop the voltage needed to interface with the DC-AC inverter. Higher voltage and lower current produces lower subarray power. But high current to voltage ratio increases subarray power.

High current to voltage ratio also decreases the amount of paralleling which can be accomplished in a module. Paralleling of cells or series strings of cells improves tolerance to photocurrent variations because summing the photocurrents of parallel groups produces tighter distributions. In a module of given area and voltage, however, high current and low voltage in cells means more series connections and less paralleling. If, on the other hand, the module voltage is lowered to increase paralleling, the lower voltage module degrades subarray modularity.

The ideal module for residential applications is about 2.5 ft. x 4 ft. with peak power at 20 V and 4.4 A if module open circuit voltage is limited to 30 V. If the 30 V limit can be exceeded, 4 ft. x 6 ft. modules with 50 V and 4.4 A may be preferred. If four cells are required in parallel in the module, cell current should be no greater than 1.1 A; if five cells are required, cell current should be 0.88 A; etc. The net result, therefore, of high current to voltage ratio is a reduction in the maximum allowable cell area.

1.2.4 Voltage-Temperature Characteristics (5.2.1.3)

The array operating voltage will assume a range of values corresponding to ambient temperature changes at the application locale. This array voltage range must be matched to the inverter input voltage limits. The interface is often difficult for single crystal silicon which has a fractional voltage variation with temperature ($\Delta V/\Delta T$) of about 0.0035-0.004/°C. Therefore, a lower value than this would be more desirable.

1.2.5 Limiting Cell Area (5.2.1.5)

Practical limits should be placed on cell area once a technology is capable of producing large area cells ($> 25 \text{ cm}^2$), to prevent excessive metallization and conductor run requirements, to preserve subarray modularity, and to improve performance and reliability by reducing the effects of nonuniformities in cell processing and permitting more paralleling in the module.

High cell aspect ratio (long length and short width) should also be avoided as this might also result in excessive metallization requirements and processing reliability problems due to the long length dimension.

1.2.6 System Applications (5.2.1.6)

As previously discussed, high voltage modules are more desirable than low voltage modules from performance considerations. High voltage modules ($V_{MPC} \geq 20$ V), however, may present a safety hazard in residential applications due to homeowner or unskilled personnel handling. CPS applications, on the other hand, should utilize large area (32 ft² or 3 m²) and high voltage (≥ 100 V) modules due to high inverter voltages (1000-2000 V) and more skilled personnel involved in handling and maintenance.

It is recommended that initial module development for advanced technologies be oriented toward residential applications with smaller area (4-8 ft²) lower voltage (≤ 20 V) modules, since these modules will experience fewer problems with voltage isolation, factory assembly, handling, etc. and because there exists significant experience with residential applications.

1.2.7 Specific Technology Conclusions

A comparison of the technologies analyzed in this study with single crystal silicon is contained in Table 1-1. The comparisons were made for the considerations discussed in the previous sections. Five different technologies were considered in this study: one polycrystalline silicon, one amorphous silicon, one cadmium sulfide, and two gallium arsenide processes. The polycrystalline silicon technology studied is the ribbon-to-ribbon (RTR) recrystallization process developed by Motorola [4] in which thin microcrystalline silicon is melted using either a laser or an electron beam and allowed to recrystallize into large grain poly-silicon. The amorphous silicon technology uses a P-I-N deposition process developed by RCA [5], which produces integrated series-connected cells on a glass superstrate. A thin transparent conducting oxide is used as an electrode between the glass and the amorphous silicon cell. The cadmium sulfide technology is a copper-ternary heterojunction of P-type CuInSe₂ with N-type CdS developed by Boeing [6]. The process envisions ribbons of CdS/CuInSe₂ cells on a flexible substrate [7]. One of the gallium arsenide technologies utilizes the "CLEFT" process being developed at MIT [8]. Thin homojunction GaAs cells are grown on reusable GaAs substrates, bonded to a glass superstrate and separated from the GaAs substrate with a cleaving wedge. The other GaAs technology uses AlGaAs/GaAs cascaded cells similar to those reported by Research Triangle Institute [9]. The goal envisioned results in 500 x concentrating cells with 30 percent efficiency at 50°C and at least 20 percent efficiency at 100°C [10].

Many of the values shown in Table 1-1 for the advanced technologies were postulated from technology goals and projections. The actual values for state-of-the-art cells and cells of the future may differ significantly. The ratio I_{MPC}/V_{MPC} will vary with cell area. Desirable values for this ratio and for maximum cell area will vary with specific cell characteristics, with process constraints, and with module design for specific applications. The

Table 1-1. COMPARISON OF CELL CHARACTERISTICS

CHARACTERISTICS ⁽¹⁾	Poly-Si RTR	A-Si Integrated	CdS/CuInSe ²	GaAs CLEFT	GaAs/AlGaAs (500x)	Prefer	Crystal Si
CELL CHARACTERIZATION	← ADDITIONAL CHARACTERIZATION REQUIRED →						WELL-KNOWN
V_{MPC}/V_{OCC}	0.83	0.80	0.71	0.86	0.87	>0.8	0.80-0.83
J_{MPC}/J_{SCC}	0.92	0.86	0.92	0.96	0.88	<0.92	0.90-0.94
FILL FACTOR	0.77	0.69	0.65	0.82	0.77	0.77-0.80	0.74-0.77
$I_{MPC}V_{MPC}(A/V)/\text{Prefer}^{(2)}$	3.9-4.2/ <2.9	0.43-0.47/ <0.86	5.1-6.2/ <3.7	2.7-2.9/ <0.75	N/A ⁽³⁾	Technology ⁽⁵⁾ Dependent	4.5-5.5
$\Delta f_V/\Delta T (^{\circ}\text{C}^{-1})$	0.0037	0.0018	0.0048	0.0033	0.0064 ⁽⁴⁾	<c-Si	0.0037-0.004
CELL AREA MAXIMUM USED (cm ²)/ Prefer ⁽²⁾	96/ <64	25/ 25	50/ <31	100/ <26	1.27	Technology ⁽⁵⁾ Dependent	80-100
ASPECT RATIO	~2.7	>4.0 ⁽⁶⁾	~1.3	1.0	1.0	Avoid Large Values	1.0

(1) VALUES FOR ADVANCED TECHNOLOGIES ARE POSTULATED FROM GOALS — ACTUAL CELL VALUES MAY DIFFER SIGNIFICANTLY

(2) CONSIDERATION APPLIES TO RESIDENTIAL APPLICATIONS ONLY.

(3) CHARACTERISTIC NOT CRITICAL FOR CONCENTRATOR DESIGN.

(4) VALUE POSTULATED FROM WORST CASE EFFICIENCY VARIATION — ACTUAL MAY BE MUCH LESS.

(5) MAXIMUM AREA DESIRABLE IS DEPENDENT ON CELL CHARACTERISTICS, PROCESS CONSTRAINTS APPLICATION — MAY VARY SIGNIFICANTLY FROM VALUES SPECIFIED.

(6) HIGH ASPECT RATIO DUE TO WIDTH LIMITATION ON CELL.

amorphous silicon cell technology is width-limited to less than 2.4 cm due to high resistance of the transparent electrode (conducting oxide).

1.2.8 Conclusions Derived from Design and Analysis Results

A detailed discussion of analysis results and conclusions is contained in Section 5.1 and summarized below.

- The high series resistance of the CdS/CuInSe₂ cell results in lower module efficiency at 1.0 sun than at 0.5 suns (10.0 percent versus 10.7 percent).
- Power loss in arrays due to variation of photocurrent (I_p) from cell-to-cell (photocurrent mismatch losses), are nearly linear up to ± 20 percent I_p distribution, but become non-linear beyond this ($P_{LOSS} = 6.5-11.5$ percent at ± 20 percent I_p but $P_{LOSS} \sim 20-32.5$ percent at ± 50 percent I_p).
- Although tolerance to I_p distributions cannot be quantified at this time, certain qualitative assessments can be made. Tolerance to I_p distribution is enhanced most by paralleling of cells. Connecting cells in series first before cross-strapping, increases power loss. High cell fill factor also reduces tolerance to I_p distribution.
- Tolerance to hot spot heating conditions is improved by using small bypass group size. Heating is increased by high shunt resistance.
- SOLCEL II analyses of annual energy production require technology dependent parameters which cannot easily be obtained for all advanced technologies. As a result, valid results cannot always be obtained for advanced technology systems. It is recommended that modifications discussed in Section 5.1.4.2 be made to SOLCEL II to permit accurate modeling of advanced technologies.
- Economic analyses were based on technology cost goals and typical cost parameters; therefore, all technologies appear to have comparable worth although, in fact, they do not. In some cases, cost data did not exist and in other cases was not made available from proprietary or other considerations. The economic methodology provides a valuable tool used in conjunction with the complete design and analysis procedure. Additional economic analyses should be performed if sufficient data can be made available.

1.2.9 Recommendations for Future Efforts

The following recommendations for future work have been generated based on the conclusions presented above.

- SOLCEL II should be modified so that it can be applied more easily to advanced PV technologies as discussed in Section 5.1.4.2.
- Additional characterization of advanced technology cells should be undertaken. Specifically, reverse breakdown voltages, maximum allowable temperatures, and voltage variations with temperature should be determined.
- Additional module designs should be performed based on latest cell characteristics data and projections. The effects of designing modules at nominal operating cell temperature (NOCT) instead of at 25-28°C should be assessed using the full module and system design methodology.
- Realistic economic analyses should be performed for the systems based on best technology data and projections, if available.
- A study should be undertaken to quantify the dependence of photocurrent distribution tolerance on cell characteristics and interconnections.
- Module design trade-offs should be investigated for selected technologies to determine optimum designs under various constraint conditions such as high or low voltage, different maximum allowable reverse biases, and different size constraints. Residential applications should be investigated first followed by commercial/industrial and central power applications later.
- Guidelines for determination of optimum cell area based on system application considerations should be developed for each advanced technology.

1.3 TASK SUMMARIES

1.3.1 Data Collection and Technology Selection

Data were collected for the photovoltaic technology material listed in Table 1-2. The data, which served as inputs to the photovoltaic module and array designs and analyses, included photovoltaic cell electrical, mechanical, optical, thermal, and chemical properties, as well as geometric

considerations. For the cases in which different processes were used in a technology, the process which yielded the maximum efficiency was used for that technology. For this purpose, amorphous silicon, polycrystalline silicon, gallium arsenide flat plate and gallium arsenide concentrator are all considered to be separate technologies. However, the efficiencies of cells made by $\text{Cu}_2\text{S}/\text{Cd}_{1-x}\text{Zn}_x\text{S}$ and $\text{CuInSe}_2/\text{CdS}$ processes were compared, and $\text{CuInSe}_2/\text{CdS}$ was chosen as the technology for the cadmium sulfide material based on its higher efficiency and unusual I-V characteristics (high current/low voltage.)

Table 1-2. ADVANCED PV MATERIALS INCLUDED FOR DATA COLLECTION

<u>PRINCIPAL MATERIAL</u>	<u>VARIANT TECHNOLOGIES</u>
• Silicon	• Amorphous Silicon (a-Si)
• Gallium Arsenide	• Polycrystalline Silicon (p-Si)
• Cadmium Sulfide	• Flat Plate (thin-film)
	• Concentrator
	• $\text{Cu}_2\text{S}/\text{Cd}_{1-x}\text{Zn}_x\text{S}$
	• $\text{CuInSe}_2/\text{CdS}$

1.3.2 Module and System Conceptual Designs

1.3.2.1 Overview Of Designs

Conceptual designs of photovoltaic (PV) modules and systems were developed for a select set of advanced PV technologies. The four advanced technologies chosen were amorphous silicon, polycrystalline silicon, $\text{CdS}/\text{CuInSe}_2$ and gallium arsenide. These technologies are currently in the R&D laboratory development stage. Therefore, the work performed in this effort builds upon engineering judgment and projection of potentially feasible methods in which the current cell technology might be extended into modules that could, in turn, be integrated into a larger power generating array.

The modules were designed using the module optimization methodology [3]. A brief description of the methodology and its application to each technology has been included. The details of the module optimization methodology are included as Appendix B. The eight modules presented in this report have been

developed as examples of that methodology. Because of the developmental nature of the cell technologies, neither BDM nor SERI suggest that any future manufactured module will resemble the conceptual designs presented in this document.

An overview of the system conceptual design methodology is presented in Figure 1-2. The first step in this process is the identification of the cell characteristics, for each technology, which satisfy SERI technology goals, including the current, voltage, and power output at rated conditions. To obtain these characteristics, existing data (most notably cell I-V curves) must be enhanced in a technology-consistent manner to satisfy the technology goals if they have not yet been achieved.

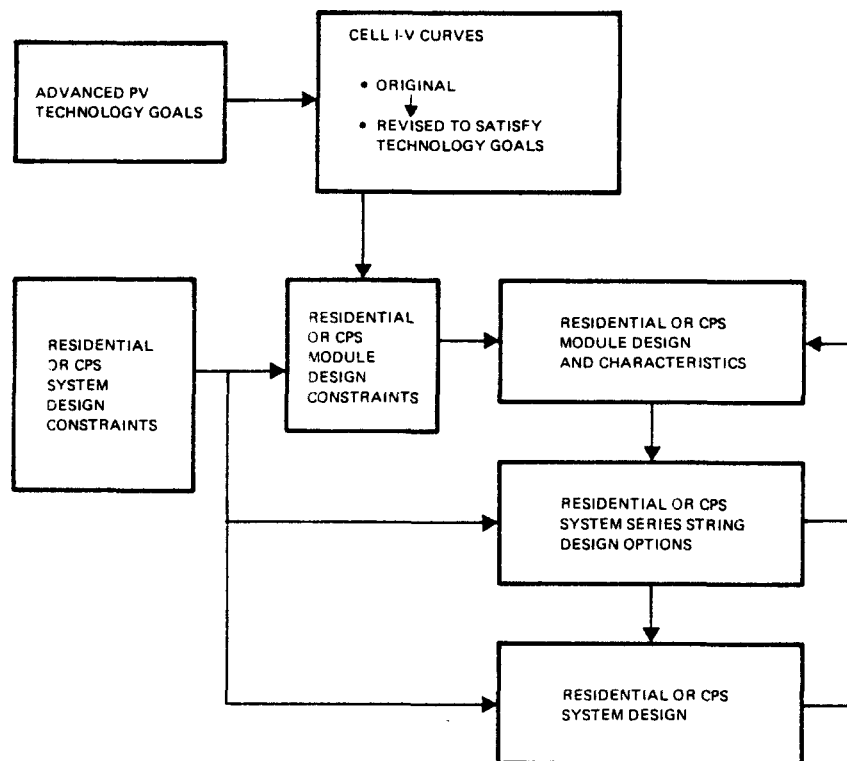


Figure 1-2. MODULE AND SYSTEM DESIGN PROCESS

The next step is to identify module and system design constraints based on practical system applications. The residential and central power station (CPS) PV systems have been selected in order to bound the range of possible applications. The system design constraints include system power level, nominal DC voltage, and DC voltage limits. The system application also implies certain module constraints such as module size and voltage as in the case of residential roof-support spacing. The particular technology characteristics also provide module design constraints such as maximum cell size

and cell-to-cell spacing. The PV module for each technology and application is designed using the module optimization methodology based on the module design constraints.

Based on the module voltage as a function of temperature, and on the array voltage and power constraints, the optimum series-string of modules is determined. First, the DC voltage and AC power windows, as a function of expected temperature, are obtained for various numbers of series-connected modules. The option which is most closely divisible into the desired system output power, in addition to providing the optimum voltage window, is chosen for the system series-string design. The full system is then obtained by paralleling series strings until the desired power is obtained.

Complete discussions of the design methodology, the system applications chosen, the generic power system designs, and the module and system design constraints are presented in Section 3.1. The residential module and system designs for each technology and application are presented and discussed in Sections 3.2 through 3.5. Section 3.2 contains the polycrystalline silicon residential and CPS designs; Section 3.3 contains the amorphous silicon designs; Section 3.4 contains the CdS/CuInSe₂ designs; and Section 3.5 contains the gallium arsenide designs.

1.3.2.2 Summary Of Designs

Module and system designs for residential and CPS applications were developed for the four technologies. Two residential arrays were designed for each technology—one for a 4 kW system, and one for an 8 kW system. One CPS array was designed for each technology. The CPS systems are 50 MW each.

The final design parameters for each technology are summarized in Tables 1-3 and 1-4. Characteristics of current-technology, single-crystal silicon modules and systems are included in the tables for comparison.

Both the residential and the CPS designs are based on the same polycrystalline silicon technology; namely, the ribbon-to-ribbon (RTR) recrystallization process developed by Motorola [4]. The module and system designs follow the steps previously illustrated in Figure 1-2. The complete design process for polycrystalline silicon is discussed in detail in Section 3.2. The cell technology goals are discussed in Section 3.2.1. Module and system design constraints applicable to all technologies are discussed in Section 3.1. Module constraints derived from cell or module manufacturing processes are described in Sections 3.2.2 and 3.2.3.

Table 1-3. SUMMARY OF MODULE CHARACTERISTICS

CHARACTERISTICS	POLY-Si		AMORPHOUS Si		CdS/CuInSe ₂		GaAs		CRYSTALLINE SILICON				
	RES	CPS	RES	CPS	RES	CPS	RES	CPS	RESIDENTIAL			CPS	
PROCESS	RTR		INTEGRATED ON GLASS		FLEXIBLE RIBBON		CLEFT	MULTI-JUNCTION CASCADED	CZOCHELSKI INGOT		SEMI-CRYST. CAST INGOT	DENDRITIC WEB	CZOCHELSKI INGOT
TYPE	FLAT PLATE		FLAT PLATE		FLAT PLATE		FLAT PLATE	(500X) CONCENTRATING	FLAT PLATE REF. [11]	FLATE PLATE [12]	FLATE PLATE REF. [13]	FLAT PLATE [14, 15]	100 x CONC. [14, 15]
CELL PARAMETERS													
V _{MPC} (V) @ 25°C	0.5V		0.73		0.30		0.833	1.30 (100°C)	0.48	0.46	0.40	~0.5	~ 0.48 (71°C)
J _{MPC} (mA/cm ²)	23.0		13.7		36.0		24.0	7730	~25	~28	25	~28	35 mA. cm ² -SUN
η _C (%)	11.5		10.0		10.8		20.0	20.1	~12	~13	~10	14.2	~ 17
SERIES LENGTH (cm)	5.78	5.78	1.96	1.64	5.79	5.79	9.75	1.27 CELL DIAMETER	10 cm SQUARE	10 cm DIAMETER	9.5 cm SQUARE	~ 3.2	2.5 cm SQUARE
PARALLEL LENGTH (cm)	14.68	15.82	11.81	13.92	7.77	7.32	9.50	28.4 LENS (SQUARE)				9.8	
MODULE CHARACTERISTICS								POINT FOCUS FRESNEL					POINT FOCUS FRESNEL
SERIES LENGTH (cm)	120.7	120.7	29.9	29.9	120.7	120.7	120.7	236.7 ⁽¹⁾ (7.77 FT.)	120.0	120	120	132	~330 ⁽²⁾ (10.8 FT.)
PARALLEL LENGTH (cm)	120.7	241.3	120.7	120.7	81.1	241.3	40.4	294.8 ⁽¹⁾ (9.67 FT.)	34.0	30.5	~60	132	~1300 ⁽²⁾ (42.7 FT.)
BYPASS GROUP (CELLS)	10	10	7	7	10	10	6	4	33	35	6	NOT KNOWN	14
PARALLELING (STRINGS)	4	3	10	2	4	4	2	2	1	1	6	12	1
SERIES CELLS	40	100	14	70	50	160	24	40	33	35	12	40	840
V _{MPM} (V)	20.0	50.0	10.22	51.1	15.0	48.0	20.0	52.0 (100°C)	15.8	16.1	4.5	20	420 (71°C)
I _{MPM} (A)	7.8	6.31	3.17	0.624	6.47	6.10	4.45	19.6	2.53	2.3	13.36	8.9	11
P _M (W)	156	315.5	32.4	31.9	97.1	293.0	89.0	1018 ⁽¹⁾	40.0	37.0	60.1	178.8	4600 ⁽²⁾
PACKING FACTOR	0.933	0.943	0.90	0.886	0.921	0.932	0.913	0.726 LENS	~0.81	~0.75	0.92	0.9	NOT KNOWN
η _M (%)	10.73	10.84	9.0	8.86	9.95	10.07	18.26	14.59	9.8	10.1	9.2	12.2	12.8

(1) TWO MODULES PER PEDESTAL

(2) ONE "MODULE" PER PEDESTAL

Table 1-4. SUMMARY OF SYSTEM CHARACTERISTICS

CHARACTERISTICS	POLY Si		AMORPHOUS Si		CdS/CuInSe ₂		GaAs		CRYSTALLINE SILICON 4 kW [11]
	4 kW	8 kW	4 kW	8 kW	4 kW	8 kW	4 kW	8 kW	
RESIDENTIAL SYSTEMS									
SERIES MODULES	10	10	20	20	13	13	10	10	13
PARALLEL STRINGS	3	6	7	14	4	8	5	10	9
VOLTAGE (V)	200	200	204.4	204.4	195	195	200	200	195
DC POWER (kW)	4.68	9.36	4.54	9.07	5.05	10.09	4.45	8.90	4.68
AC POWER (kW)	4.10	8.20	3.98	7.95	4.42	8.85	3.90	7.80	4.10
CPS SUBSYSTEMS ⁽¹⁾							POINT - FOCUS FRESNEL		DENDRITIC WEB [14, 15] POINT - FOCUS FRESNEL [14, 15]
SERIES MODULES	20		20		21		20		100 2
PARALLEL STRINGS	366		3585		371		112		405 550
VOLTAGE (V)	1000		1020		1008		1040		~ 2.000 ⁽²⁾ ~ 2.000 ⁽²⁾
DC POWER (MW)	2.284		2.282		2.283		2.281		~ 5.6 ~ 5.6
AC POWER (MW)	2.002		2.000		2.001		1.999		5.0 5.0

(1) ADVANCED TECHNOLOGIES — 25 SUBSYSTEMS = 50 MW SYSTEM
CRYSTALLINE SILICON — 20 SUBSYSTEMS = 100 MW SYSTEM

(2) BOTH SYSTEMS BY MARTIN MARIETTA
OTHER SYSTEMS [26, 27, 28] USE 1000-1200 V

The amorphous silicon designs for each application are based on a deposition process, used by RCA, which produces integrated, series-connected cells on a glass superstrate [5]. Detailed discussion of the amorphous silicon designs is contained in Section 3.3.

The same copper-ternary technology was used for both cadmium sulfide applications. The process envisioned produces ribbons of CdS/CuInSe₂ cells on a flexible substrate [6, 7]. The design steps are discussed in detail in Section 3.4.

Two gallium arsenide technologies were considered. The residential design utilizes the CLEFT process, being developed at MIT, which grows homojunction cells on reusable substrates which are then bonded to glass and cleaved from the substrate [8]. All the previously mentioned systems are non-concentrating. The GaAs CPS application, however, is a concentrating system using a 500X point-focus fresnel lens design with 1.27 cm diameter, multi-junction

cascaded cells similar to those reported by RTI [9, 10]. The designs for each of these GaAs processes are discussed in detail in Section 3.5.

Tables 1-3 and 1-4 summarize the module and system designs for all technologies and applications. For the CPS systems, only the characteristics of the 2 MW subsystems are listed. In each case, the AC outputs of 25 subsystems are paralleled to produce the 50 MW systems.

The differences in the cell and module sizes seen in Table 1-3 are due in part to process constraints which are explained in the subsequent chapters. In general, it was felt that CPS modules could be made larger and produce higher voltages than residential modules could, due to better installation and maintenance controls in a CPS application. Thus, CPS modules are approximately 50 V at maximum power compared with a maximum of 20 V for residential modules.

Tables 1-3 and 1-4 also provide characteristics of state-of-the-art single crystal silicon modules and systems for comparison [11-15]. The single crystal silicon modules and systems listed are typical of the current technology but are not exhaustive, in that at least 10 manufacturers produce flat plate modules which can be used for residential or CPS applications, and several manufacturers produce concentrating systems which can be used for CPS applications. Present day concentrating systems are not considered viable for residential applications.

The first two crystalline silicon residential modules consist of three rows of cells, all connected in series with one bypass diode. Each of these manufacturers offers the option of a 5 V module with 11 cells in series in a row with three rows in parallel and one bypass diode. The module with square cells also may be obtained with all cells in series but with three bypass diodes, one across every 11 cells. This version was used in the 4 kW BDM residential application [11] summarized in Table 1-4 since it contains better reverse bias protection.

The 4.6 kW module referenced for the crystalline silicon concentrating application is designated an "array" by the manufacturer, whereas a 14 cell subassembly is designated a "module." The term "module" is used to represent all the cells and lens enclosed by a single frame. In our GaAs advanced technology CPS design, this consists of one 8 ft. x 10 ft. concentrating assembly with two assemblies per pedestal; in the crystalline silicon design, however, each 14-cell subassembly contains a frame so that there are 64 of these framed modules on one pedestal which we have listed in the array instead of the module.

1.3.3 Conceptual Design Analysis

1.3.3.1 Evaluation Plan

Based on the conceptual designs of modules and systems developed for advanced PV technologies, PV-TAP and SOLCEL II models were developed and validated. Module and system cost/performance evaluations were performed based on these models. The evaluation plan is diagrammed in Figure 1-11. Analyses performed using PV-TAP assessed the output variation with insolation and temperature extremes and the power loss with cell-to-cell photocurrent (IP) variation. PV-TAP analyses also addressed cell reliability by quantifying the cell heating due to shadow-induced reverse bias.

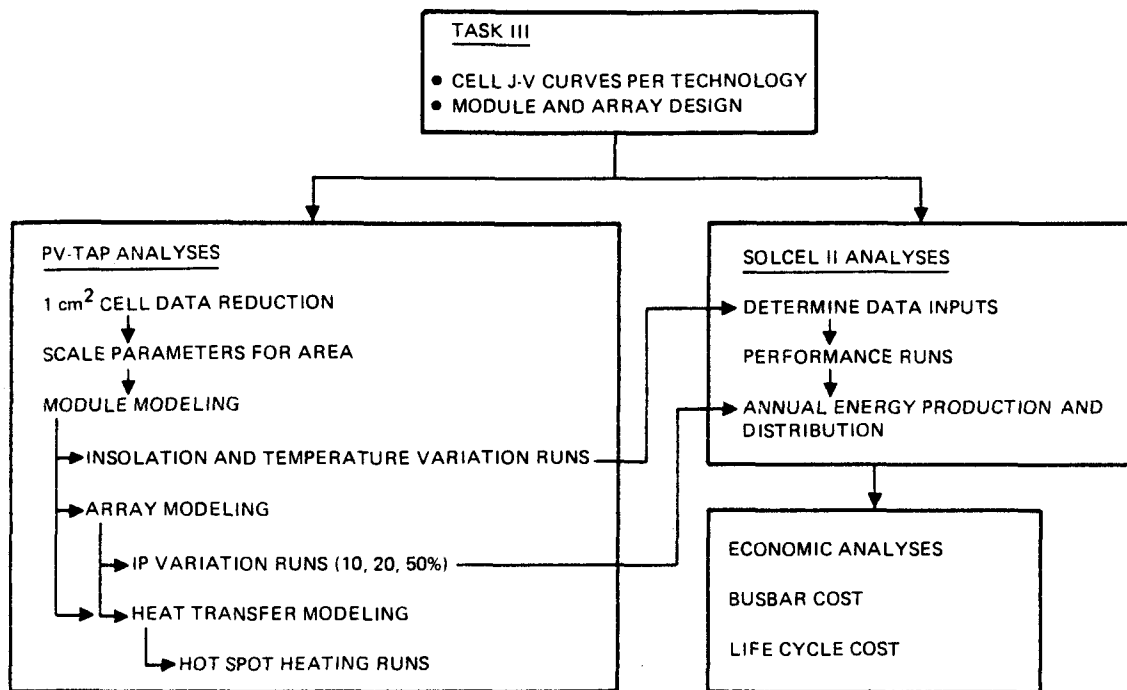


Figure 1-3. EVALUATION FLOW CHART FOR EACH ADVANCED PV SYSTEM APPLICATION

The evaluation plan also includes assessment of system annual performance using SOLCEL II and system economic analyses using the SOLCEL II Life Cycle Costing methodology. In addition to data from the module and systems designs, the SOLCEL II analyses also require that module current and voltage values at extremes of temperature and insolation be obtained from the PV-TAP analyses. The SOLCEL II analyses report the annual DC energy production, the AC energy delivered to the load, the AC backup energy required and the AC energy wasted or sold to the utility. The SOLCEL II performance results are scaled based on the PV-TAP IP variation analyses results.

The economic analysis uses the Life Cycle Cost (LCC) methodology incorporated in the SOLCEL II model. The SOLCEL II model has been expanded to include the financial benefits associated with selling excess energy back to the electric utility. Published cost projections for PV modules and Balance of System (BOS) costs have been used to project the LCC of each of the Advanced PV Systems. These cost projections include: system peak output proportional costs; array area proportional costs; and array FOB costs/Wp. The implication of this analytical approach is that PV module efficiency is the determining factor for relative system cost effectiveness. Levelized cost projections have been made for total system costs, cost per kWh of electricity generated by the PV system, and the break-even cost of conventional energy.

1.3.3.2 Overview Of Modeling

In order to perform computer analyses on PV systems, the cells, modules and arrays must be modeled in terms compatible with computer codes used and then the models must be validated to ensure compliance with expected system operation and to quantify the accuracy of the models. PV-TAP runs were made to validate the models by comparing the results with the specifications for the cells, modules, and systems developed. First, the postulated 1 cm² cell data were reduced using the data reduction capability of PV-TAP which determines the Ebers-Moll parameters required for PV cell modeling from I-V curve data. The PV cell data reduction verification for 1 cm² cells for each technology is shown as the first part of Table 1-5.

Next, the cell parameters were scaled to the areas of the cells used in each of the modules and the modules were then modeled using PV-TAP. A summary of the module modeling verification is also shown in Table 1-5, for each technology and system design. Each array design was also modeled and verified as shown in the last section of Table 1-5.

1.3.3.3 Overview Of Analysis Results

The analyses performed of the modules and systems designed:

- Demonstrate the variation in the output of modules due to variation in insolation and in cell temperature;
- Determine the effect of variations in the short circuit currents of the cells in an array;
- Demonstrate that shadowing of one cell in an array will not result in excessive heating of that cell;
- Demonstrate the effectiveness of the designs over an annual period of time;
- Determine the cost of these designs.

Table 1-5. MODELING AND VERIFICATION SUMMARY

DATA REDUCTION SUMMARY FOR 1 CM ² CELLS								
	POLYCRYSTALLINE SILICON		AMORPHOUS SILICON		CdS/CuInSe ₂		GaAs FLATE PLATE CONC	
ACCURACY (PERCENT DEVIATION) FOR V _{OC} FOR I _{MPC}	0.0% 0.09%		0.0% 0.2%		0.9% 0.5%		0.2% 0.1% 0.02% 0.8%	
MODULE MODELING AND VERIFICATION SUMMARY								
	POLYCRYSTALLINE SILICON RES CPS		AMORPHOUS SILICON RES CPS		CdS/CuInSe ₂ RES CPS		GaAs RES CPS	
V _{OC} (V) (CALC/DESIGN)	24.0/24.0	60.0/60.0	12.74/12.74	63.7/63.7	21.4/21.2	68.5/67.8	23.3/23.3	60.0/60.0
V _{MP} (V) (CALC/DESIGN)	19.98/20.0	49.94/50.0	10.03/10.22	50.2/51.1	15.2/15.0	48.4/48.0	19.99/20.0	49.2/50.0
P _M (W) (CALC/DESIGN)	156.5/156.0	315.7/315.5	32.48/32.42	32.06/31.89	97.55/97.05	294.7/293.0	88.8/89.0	1007/1013
POWER DEVIATION	0.3%	0.06%	0.2%	0.5%	0.5%	0.6%	0.2%	0.6%
ARRAY MODELING AND VERIFICATION SUMMARY								
V _{OC} (V) (CALC/DESIGN)	240.0/240.0	1200/1200	254.8/254.8	1274/1274	2783.3/275.6	1438/1491	233.2/233	1200/1200
V _{MP} (V) (CALC/DESIGN)	199.8/200.0	997/1000	202.3/204.4	1005/1020	197.0/195	1086/1075	199.9/200	985/1000
P _M (kW) (CALC/DESIGN)*	4.698/4.680	2286/2284	4.55/4.54	229/2282	5.07/5.05	2292/2282	4.44/4.45	2257/2269
POWER DEVIATION	0.4%	0.09%	0.2%	0.7%	0.4%	0.4%	0.2%	0.5%

*POWERS LISTED FOR CPS APPLICATIONS ARE FOR 2 MW SUBSYSTEMS

The first three of these were performed with PV-TAP; the annual performances were simulated with SOLCEL II, and the costs were obtained using an expanded SOLCEL II LCC methodology.

The maximum power that can be supplied by a photovoltaic module will be altered by variations in insolation and temperature. To demonstrate these effects the temperature was kept constant while three variations in insolation were simulated with PV-TAP. Next, the insolation was kept constant while three different temperatures were used. The results of these analyses are summarized in Table 1-6. It is seen that an order of magnitude of variation in insolation can result in a difference of more than a factor of 10 in the output power of a module. Variations in temperature can result in a difference of 30 percent in the output power. Unlike the other technologies, the CdS results indicate a higher efficiency at .5 suns than at 1.0 sun. This is due to the high series resistance of these cells, which reduces the voltage output at higher insolutions.

Short-circuit current (or photocurrent, I_p) of cells tend to vary from cell to cell. This variation will degrade the performance of an array. The greater the variation in the photocurrent, the more the net array output is degraded. This fact is illustrated in Figure 1-12, in which the variations in cell short-circuit currents are assumed to be Gaussian. The abscissa of the graph is the percent of variation of the 3σ three standard deviation points of the distribution from the nominal value. The ordinate shows the percent of array output power degradation.

The modules were specifically designed so that if one cell of a bypass group were shadowed, excessive heating of the cell would not occur and thus would not damage the cell. To verify this design constraint, PV-TAP was used to simulate the situation in which one cell of an entire array is shadowed. PV-TAP was used to calculate the temperature of the cell as a function of the amount of shadowing. As shown in Table 1-7, the maximum temperature rise was in no case excessive. More detailed discussions are included in sections 4.1.2.4 and 5.1.3.

The annual variation in array performance due to hourly changes in insolation and weather was simulated with SOLCEL II. Typical insolation and weather data for Albuquerque, New Mexico, were used in this analysis. The results are shown in Table 1-8. Of the total annual AC energy produced by the residential systems the GaAs production is the lowest by more than 10 percent. There is no apparent reason for this discrepancy since the GaAs system, though half the area of the others, has twice the efficiency. Nor is the efficiency variation with temperature significantly different from the others. The problem may be in the specification of the device-dependent parameters as discussed in section 5.1.4. It is recommended that SOLCEL II be modified to alleviate this problem and the analyses be redone. A similar problem exists with the CPS analyses in which a different SOLCEL II methodology was required for the GaAs analysis when obviously spurious results were obtained due to the device-dependent parameter specifications.

Table 1-6. INSOLATION AND TEMPERATURE RESULTS, OUTPUT POWER (W)

TECHNOLOGY:	POLY SI		aSi		CdS		GaAs
APPLICATION:	RES	CPS	RES	CPS	RES	CPS	RES
INSOLATION	(W)	(W)	(W)	(W)	(W)	(W)	(W)
.1 SUN	11.33	22.86	1.976	1.952	9.615	29.04	8.223
.5 SUN	73.98	149.1	14.58	14.40	52.08	157.2	44.09
1.0 SUN	156.5	315.7	32.48	32.06	97.55	294.7	88.81
TEMPERATURE							
15°C	163.0	328.6	33.16	32.73	104.4	315.1	91.96
25°C	156.5	315.7	32.48	32.06	97.55	294.7	88.81
75°C	123.7	249.0	28.84	28.67	63.76	192.4	72.45

TECHNOLOGY:	GaAs
APPLICATION:	CPS
INSOLATION	(W)
50 SUNS	82.11
250 SUNS	476.3
500 SUNS	1007
CELL TEMPERATURE	
50°C	1568
100°C	1007
120°C	781.9

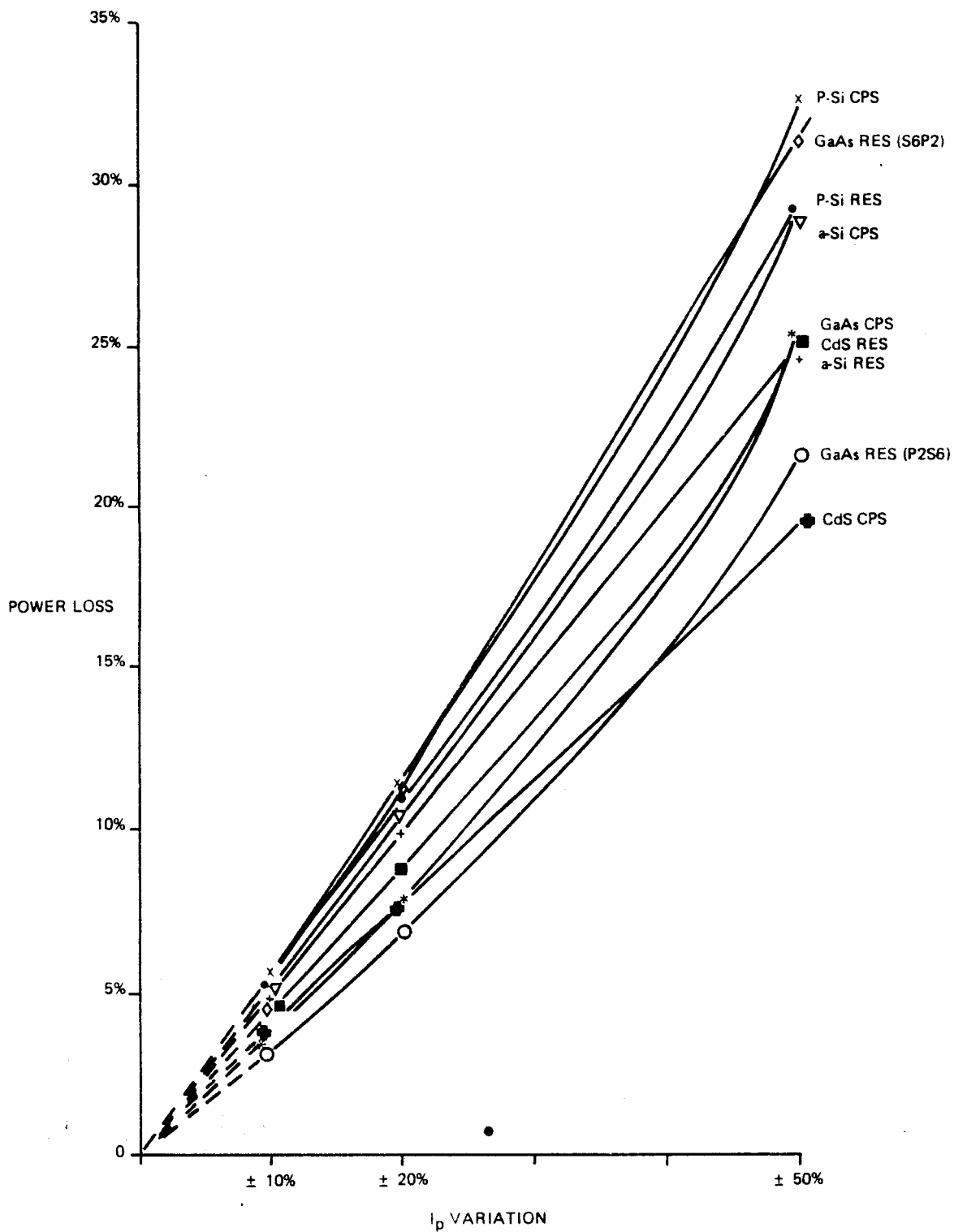


Figure 1-4. POWER LOSS DUE TO I_p VARIATION

Table 1-7. HOT SPOT HEATING RESULTS SUMMARY

	POLY-SILICON		A - SILICON		CdS/CuInSe ₂		GaAs	
	RES	CPS	RES	CPS	RES	CPS	RES	CPS
MAX. TEMP. ALLOWABLE (°C)	100	100	80	80	122	122	100	<u>@ 500x</u> 212
MAX. TEMP. OBTAINED (°C)	71	74	61	61	72	69	74	177
TEMP. MARGIN (°C)	29	26	19	19	50	53	26	35

Table 1-8. SOLCEL II RESULTS SUMMARY

ANNUAL ENERGY DISTRIBUTION kWh	RESIDENTIAL 4 kW ARRAY			
	POLY-Si	a-Si	CdS/CuInSe ₂	GaAs
TOTAL AVAILABLE INSOLATION	135,384	155,985	157,668	75,525
TOTAL INSOLATION RECEIVED	103,705	119,486	120,775	57,853
PRODUCED DC ENERGY	10,775	10,968	10,938	9,681
AC ENERGY SUPPLIED TO LOAD	2,494	2,489	2,581	2,414
UTILITY ENERGY TO THE LOAD	4,121	4,126	4,034	4,201
LOAD DEMAND	6,616	6,616	6,616	6,616
ENERGY SOLD TO UTILITY	5,338	5,481	5,412	4,584
TOTAL AC ENERGY PRODUCED	7,832	7,970	7,993	6,998
10 PERCENT VARIATION IN PHOTOCURRENT	7,410	7,577	7,647	6,782
20 PERCENT VARIATION IN PHOTOCURRENT	6,978	7,173	7,286	6,519
50 PERCENT VARIATION IN PHOTOCURRENT	5,522	5,978	5,979	5,500

ANNUAL ENERGY DISTRIBUTION MWh	CPS 2.2 MW ARRAY			
	POLY-Si	a-Si	CdS/CuInSe ₂	GaAs
TOTAL AVAILABLE INSOLATION	65,345	79,887	70,319	40,844
TOTAL INSOLATION RECEIVED	50,055	61,194	53,865	40,844
PRODUCED DC ENERGY	5,261	5,532	4,946	6,686
AC ENERGY SUPPLIED TO LOAD	4,494	4,730	4,211	5,775
SYSTEM PARASITICS*				33
TOTAL AC ENERGY PRODUCED	4,494	4,730	4,211	5,775
10 PERCENT VARIATION IN PHOTOCURRENT	4,244	4,487	4,048	5,562
20 PERCENT VARIATION IN PHOTOCURRENT	3,982	4,238	3,889	5,322
50 PERCENT VARIATION IN PHOTOCURRENT	3,033	3,349	3,390	4,297

*PARASITE POWER REQUIRED FOR TRACKING, COOLING, ETC. FOR CONCENTRATING SYSTEM

The AC energies produced under photocurrent variation conditions were obtained by factoring the total AC energies by the results of the PV-TAP photocurrent variations analysis for each system.

An economic analysis for each technology of the photovoltaic designs was also performed. The results are displayed in Tables 1-9a and 1-9b. All four technologies within a given application category (residential or central powered appear to have equal worth because insufficient data or projections were available to perform accurate cost analyses. Instead, the economic analyses were performed, with generalized cost goals, to demonstrate the methodology and to provide a baseline for future comparisons.

Although no definitive results or basis for technology comparisons were obtained from the SOLCEL II or economic analyses, the examples provided a demonstration of the methodology and exposed the need for revisions to the SOLCEL II code and for generation and/or promulgation of more detailed cost data for advanced PV technologies.

1.3.4 Assessments and Guidelines

The results of the conceptual design analyses were assessed to provide recommendations and guidelines for advanced PV technology development and analysis. An overview of the assessment and guideline development format is shown in Figure 1-13. Based on the conceptual designs and the cost/performance analyses performed on them, the results were analyzed and the implications of the results on the design and analysis procedures were assessed. These assessments are included in Section 5.1. Following this design and analysis assessment, the characteristics of each technology were assessed and guidelines were developed for advanced PV technologies in general and also for the specific technologies considered in this study. These technology guidelines are presented in Section 5.2. Finally, the recommendations for design and analysis procedures, contained throughout Sections 5.1 and 5.2, were compiled and summarized into guidelines for design and analysis in Section 5.3.

In the assessment of results and procedures, the results were shown to be consistent with theory. Trends in the results were noted and comparisons between applications were made where appropriate. The impact of design and analysis procedures was discussed and recommendations for improvements in the procedures were presented where appropriate.

In the technology assessments and guidelines, desirable and undesirable characteristics were discussed, first in general, then for each technology as appropriate. Discussion of advanced PV technology data which are required but are not yet available was included and characteristics which require improvement were discussed for each technology.

**Table 1-9a. ECONOMICS RESULTS SUMMARY: RESIDENTIAL
SYSTEMS PARAMETERS AND COSTS**

PARAMETER	PV TECHNOLOGY			
	p - Si	a - Si	CdS/CuInSe ₂	GaAs
ARRAY SIZE (M ²)	43.7	50.4	50.8	24.4
PEAK OUTPUT (kWp AC)	4.1	4.0	4.4	3.9
ANNUAL OUTPUT (kWh AC)	7832	7970	7993	6999
ANNUAL RESIDENTIAL LOAD (kWh AC)	6615	6615	6615	6615
ANNUAL OUTPUT TO LOAD (kWh AC)	2494	2489	2581	2415
BACK UP ENERGY (kWh AC)	4121	4126	4034	4200
OUTPUT PROPORTIONAL COST (\$)	3690	3582	3978	3510
AREA PROPORTIONAL COST (\$)	3494	4033	4068	1949
PV ARRAY COST (\$)	15867	15403	17105	15093
SYSTEM PRESENT VALUE (\$)	27107	26980	29234	24991
ANNUAL LIFE CYCLE COST (\$)	3184	3169	3434	2935

Table 1-9b. ECONOMIC RESULTS SUMMARY: CPS SYSTEMS PARAMETERS AND COSTS

PARAMETER	PV TECHNOLOGY			
	p - Si	a - Si	CdS/CuInSe ₂	GaAs
ARRAY SIZE (M ²)	21,095	25,789	22,701	15,629
PEAK OUTPUT (kWp AC)	1,954	1,954	1,946	2,270
ANNUAL OUTPUT (kWH x 1000 AC)	4,494	4,730	4,211	5,775
OUTPUT PROPORTIONAL COST (\$)	781,600	781,600	778,400	908,000
AREA PROPORTIONAL COST (\$)	1,413,400	1,727,900	1,521,000	1,047,100
PV ARRAY COST (\$)	1,875,800	1,875,800	1,868,200	2,179,200
ANNUAL REQUIRED REVENUE (\$/Y)	516,400	556,300	528,600	524,400
PRODUCTION COST (\$/kWH)	0.115	0.118	0.126	0.091

The design and analysis procedures used in this study are considered to form a basic set of guidelines for module and system design and analysis. Procedural cautions and special recommendations were presented along with suggestions for variations or improvements in the design and analysis procedures.

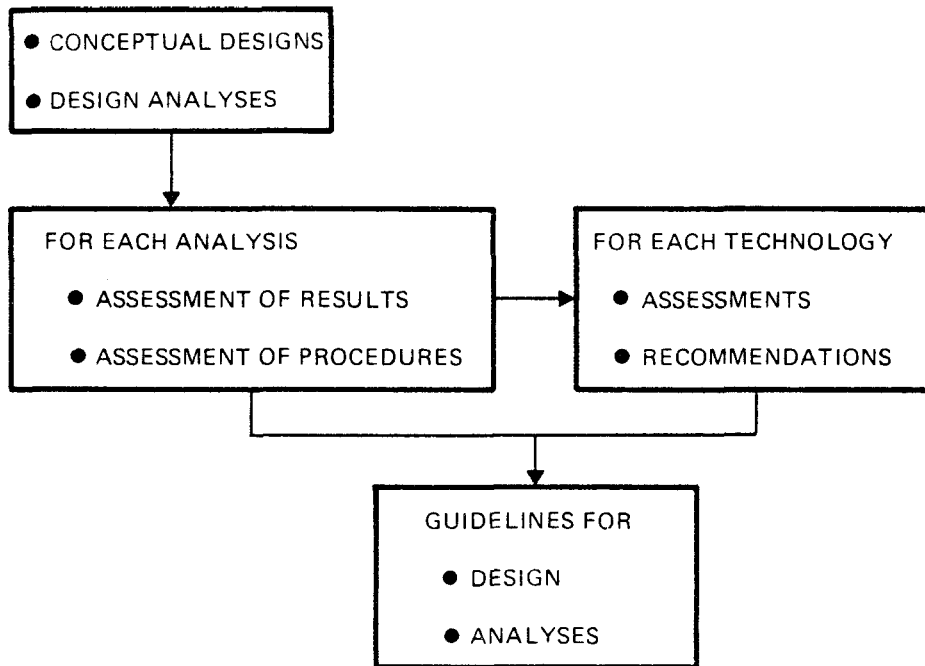


Figure 1-5. DIAGRAM OF DESIGN AND ANALYSIS ASSESSMENT AND GUIDELINES

1.3.5 PV-TAP Installation

The Photovoltaic Transient Analysis Program (PV-TAP), has been installed on the SERI CDC 720 computer system. PV-TAP is a nonlinear circuit and network analysis code capable of handling both electrical and thermal analyses on systems ranging from single PV cells to megawatt arrays. Reference 1 of this document contains the user's manual and a guide to the use of the photovoltaic elements. It is assumed that the user is familiar with the SERI operating system. The PV-TAP code is accessed on the SERI system by the use of the job control cards listed in Table 1-10. The program is run by attaching a problem file which describes the electrical or thermal network and solution controls to the job control cards and submitting the combination as a batch job. The output is returned in 132 character per line format. Therefore, a long format output terminal such as a line printer or Deckwriter must be used.

Table 1-10. PV-TAP JOB CONTROL CARDS

/BAT
/ATTACH,PV1
/GET,INFILE
/REWIND,INFILE
/PV1,INFILE,OUTFILE
/REWIND,OUTFILE
/HEADING,OUT.NAME
/COPY,OUTFILE,OUT
/ROUTE,OUT,DC=PR

SECTION 2.0

DATA COLLECTION AND TECHNOLOGY SELECTION

Data were collected for advanced PV materials mutually agreed upon by SERI and BDM. The data was used to assist in the selection of technology processes for which module and system designs would be performed and to obtain sufficient cell characteristics to permit performing these designs. This section presents the results of the data collection effort. Section 2.1 describes the data resources and collection process used for the project. Section 2.2 describes the data selection criteria and presents data selected for input to the conceptual design process.

Table 2-1. ADVANCED PV MATERIALS INCLUDED FOR DATA COLLECTION

PRINCIPAL MATERIAL	VARIANT TECHNOLOGIES
• Silicon	• Amorphous Silicon (a-Si)
	• Polycrystalline Silicon (p-Si)
• Gallium Arsenide	• Flat Plate (thin-film)
	• Concentrator
• Cadmium Sulfide	• $\text{Cu}_2\text{S}/\text{Cd}_{1-x}\text{Zn}_x\text{S}$
	• $\text{CuInSe}_2/\text{CdS}$

2.1 DATA RESOURCES AND DATA COLLECTION

The four primary data resources used for data collection were SERI, recent PV conference proceedings, manufacturers and researchers under contract to DOE, and manufacturers and researchers not under contract to DOE. In general, whereas DOE contractors were responsive to a request for information, non-DOE contractors were not responsive.

Information was collected for all of the advanced PV materials listed in Table 2-1. A list of desirable PV cell data was developed and is included in Table 2-2. The list is comprehensive and most of the data were not available from any sources, indicating that much additional characterization is required before practical, reliable modules for commercial use can be built from these technologies. A compilation of electrical data were obtained from SERI [16]. Additional information and data were obtained from discussions with SERI Technology experts [7,10,17].

Table 2-2. PV CELL DATA REQUESTED

- ELECTRICAL PROPERTIES
 - I-V Characteristics (vs. ambient temperature, cell temperature and insolation)
 - Efficiency (vs. temperature and insolation)
 - Reverse Breakdown Voltage
 - Shunt Resistance or dark reverse I-V curve
- MECHANICAL PROPERTIES
 - Modulus of Elasticity
 - Shear Modulus
 - Density
 - Poisson's Ratio
 - Tensile Strength
 - Fatigue Stress vs. Number of Cycles (SN diagrams)
 - Shear Strength
- OPTICAL PROPERTIES
 - Reflectivity
 - Absorptance
 - Long Wavelength Emissivity
- THERMAL PROPERTIES
 - Thermal Conductivity
 - side-to-side and front-to-back if different
 - Maximum Allowable Temperature
 - Thermal Expansion Coefficient
 - Specific Heat
- CHEMICAL PROPERTIES
 - Environmental Stability
 - Compatibility with Encapsulants
- GEOMETRIC CONSIDERATIONS
 - Dimensions
 - Maximum and Minimum Cell Size
 - Cell Shapes

Individual papers presented at recent PV conferences and meetings and current reports and articles were reviewed and categorized. The principal sources are included in the reference section of this report [18,19,20,21] .

Principal investigators of PV manufacturing and research organizations were contacted by telephone to request current information for specific technologies. A letter request which included the list of cell data requirements in Table 2-2 was sent following the telephone call. A list of organizations and investigators contacted is presented in Table 2-3. Although the degree of response varied, some information was obtained from all of these organizations.

Table 2-3. ORGANIZATIONS RESPONSIVE TO REQUEST FOR INFORMATION

TECHNOLOGY	ORGANIZATION	INVESTIGATOR
<u>Silicon</u>		
a-Si	Exxon RCA SAI	Dr. Ted Moustakas Dr. Dave Carlson Dr. Yudi Gupta
p-Si	Motorola Honeywell RCA	Dr. Kaluri Sarma Dr. Paul Chapman Dr. Art Firester
<u>GaAs</u>		
Flat Plate	SMU	Dr. Shirley Chu
Concentrator	Varian	Dr. Peter Borden
<u>CdS</u>		
CuInSe ₂ /CdS	Boeing	Dr. R. A. Mickelsen
Cu ₂ S/(CdS/Zn)S	Institute of Energy Conversion	Dr. John Meakin

2.2 TECHNOLOGY SELECTIONS

Data were collected for each of the technologies previously identified. For each technology, the process which has produced sample cells with the highest reported efficiency was selected over competitive processes with lower efficiency cells. Where competitive process data were unavailable, the most current identified data were chosen. In case a conflict appeared between SERI "M & E Lab" data and reported data, SERI data were chosen.

The technology processes chosen for module design are listed in Table 2-4 [4,5,6,8, and 9] . The most current I-V curves available for each technology are presented in Figures 2-1 through 2-5 [4,22,23,24 and 10] . No I-V curves were available for the GaAs concentrator process; rather, the data were postulated based on discussions with J. Benner, SERI [10] . Additional description of the technologies as well as cell characteristics are contained in the conceptual designs in sections 3.2 through 3.5.

Table 2-4. TECHNOLOGY PROCESSES SELECTED FOR MODULE DESIGN

TECHNOLOGY	PROCESS	DEVELOPER
POLYCRYSTALLINE SILICON	RIBBON-TO-RIBBON (RTR) RECRYSTALLIZATION	MOTOROLA
AMORPHOUS SILICON	INTEGRATED, SERIES-CONNECTED PIN ON GLASS SUPERSTRATE	RCA
CADMIUM SULFIDE	CdS/CuInSe ₂	BOEING
GALLIUM ARSENIDE FLAT PLATE	HOMOJUNCTION CELLS CLEAVED FROM REUSABLE SUBSTRATES (CLEFT PROCESS)	MIT
CONCENTRATOR	MULTI-JUNCTION, CASCADED AlGaAs/GaAs	RTI

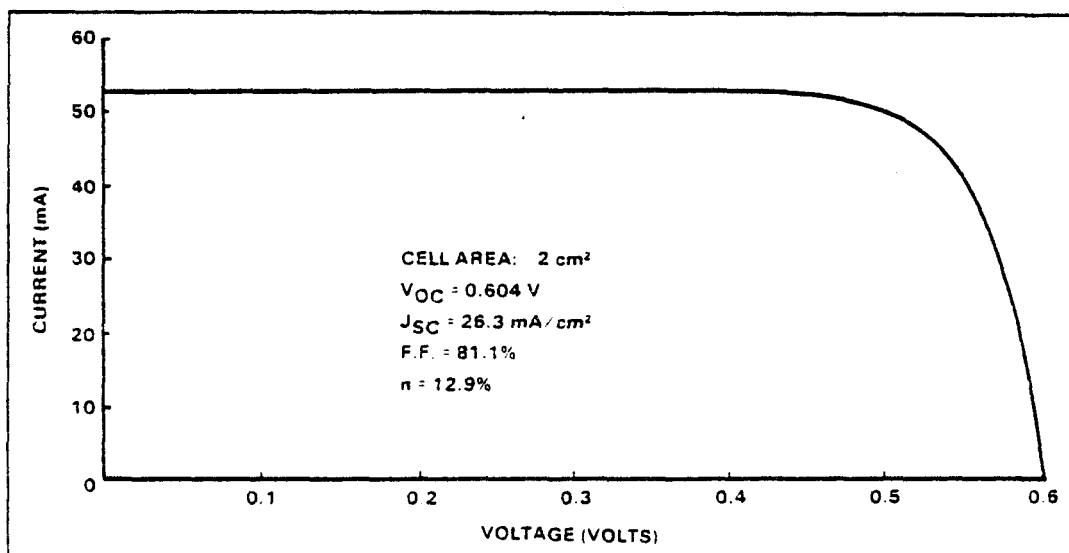


Figure 2-1. POLYCRYSTALLINE SILICON I-V CURVE

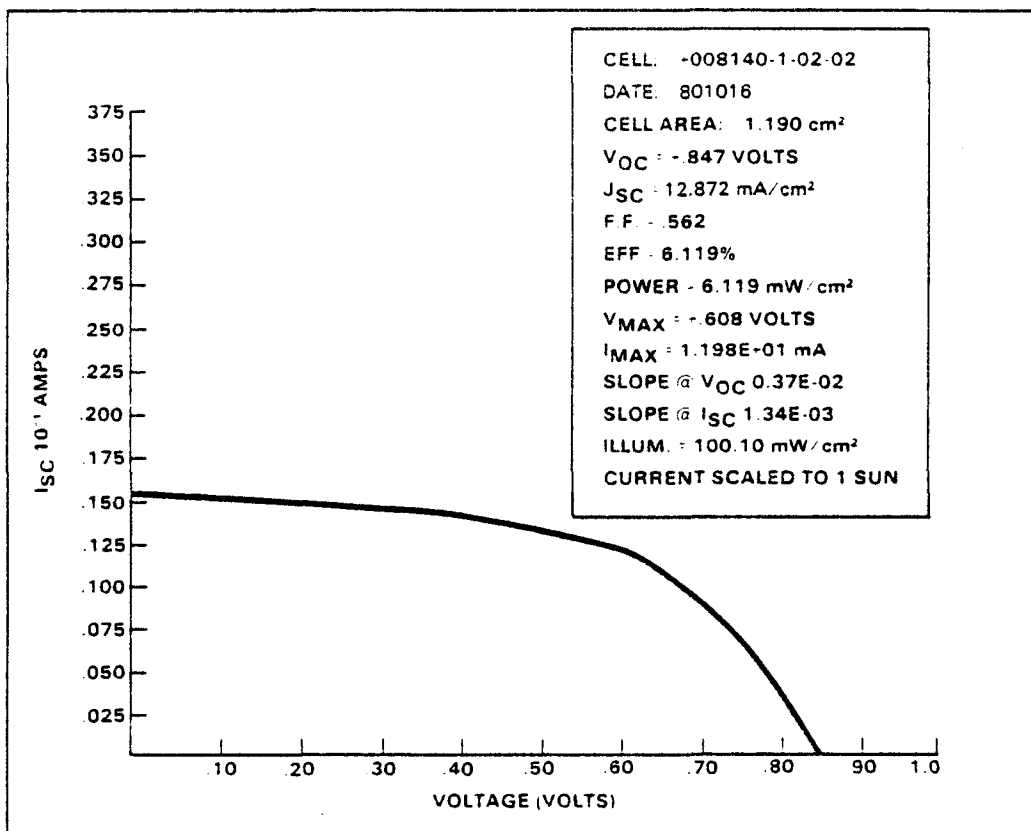


Figure 2-2. AMORPHOUS SILICON I-V CURVE

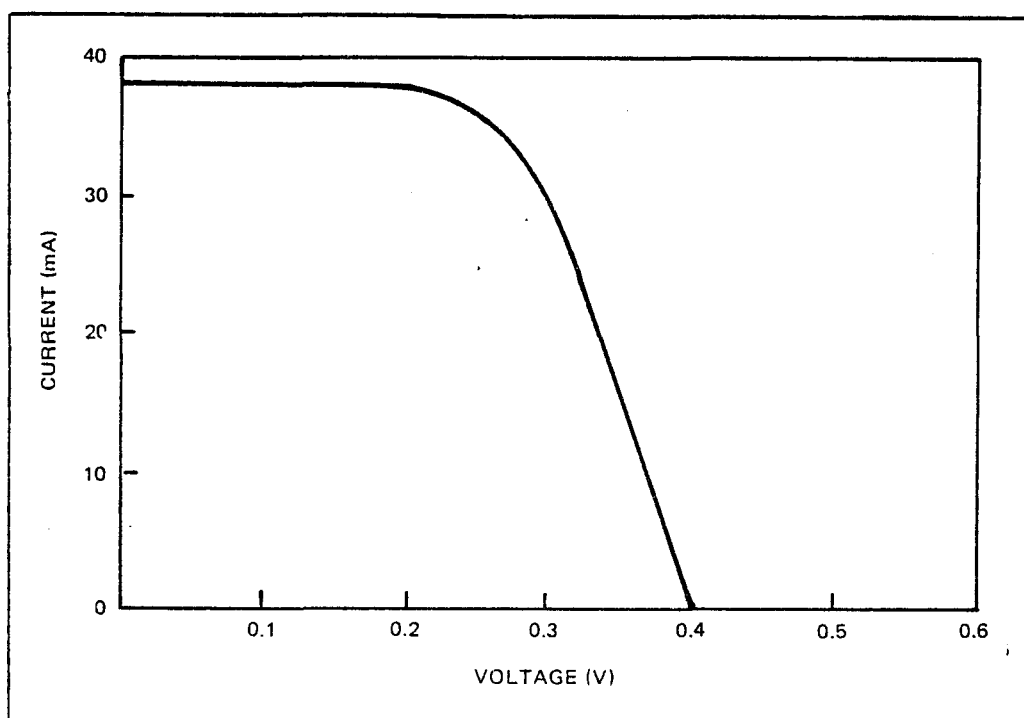


Figure 2-3. CADMIUM SULFIDE I-V CURVE (CdS/CuInSe₂)

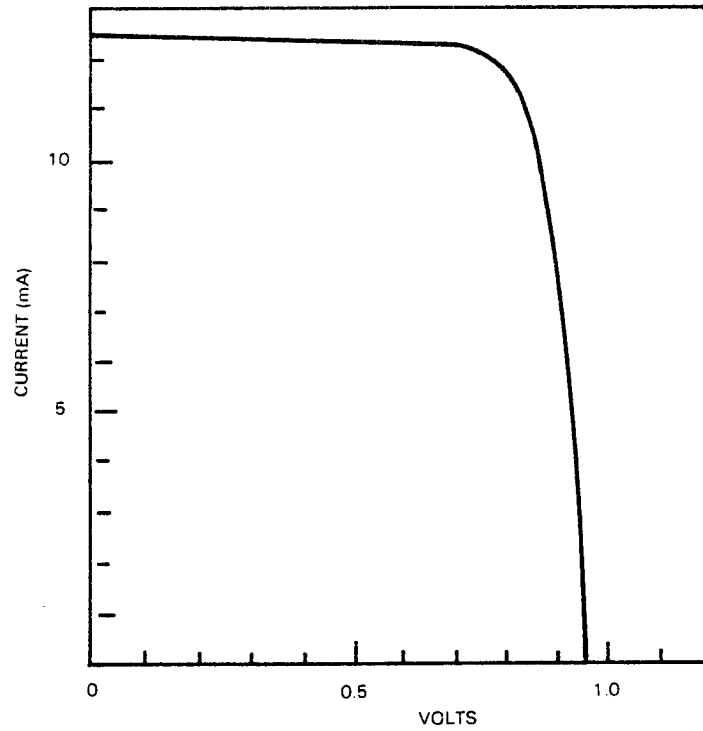


Figure 2-4. GaAs SHALLOW HOMOJUNCTION CELL I-V CURVE

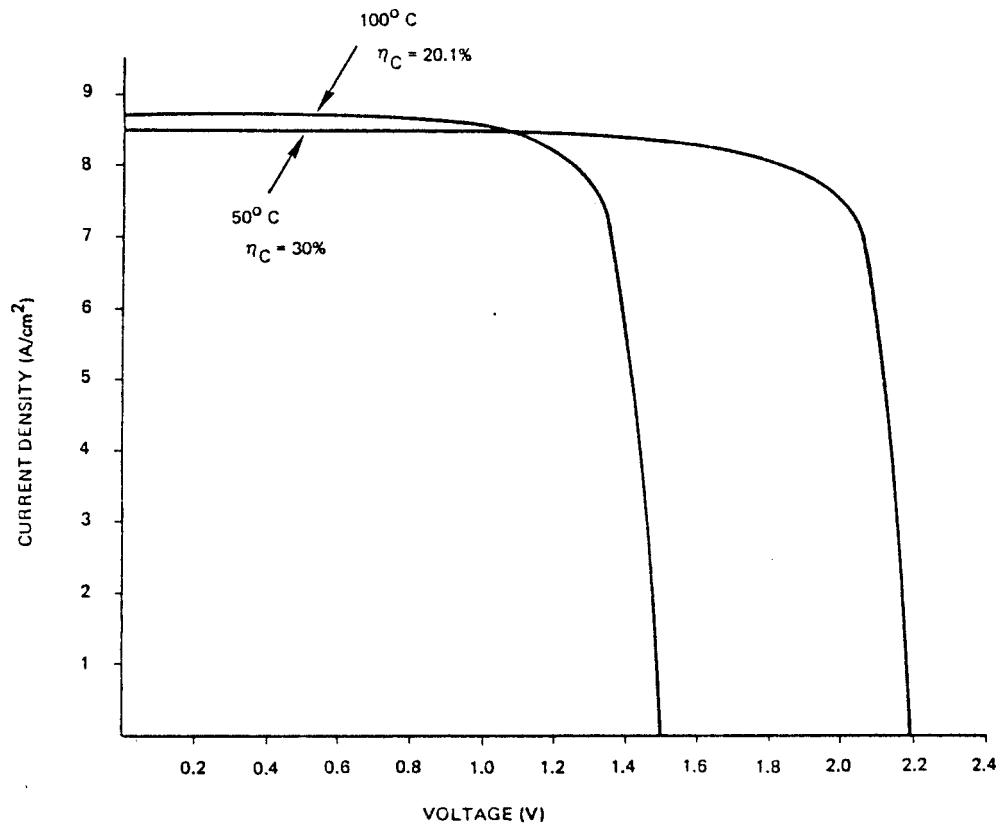


Figure 2-5. POSTULATED GaAs MULTI-JUNCTION CELL J-V CURVES

SECTION 3.0

MODULE AND SYSTEM CONCEPTUAL DESIGNS

Conceptual designs of modules and systems were developed for each of the technology processes selected in section 2.0. The design approach and generic system descriptions for residential and central power station (CPS) applications are presented in section 3.1. Sections 3.2 through 3.5 present the conceptual design development for each of the technologies.

3.1 DESIGN METHODOLOGY APPROACH

An overview of the module and system conceptual design methodology is presented in Figure 3-1. The first step in this process is the identification of the cell characteristics for each technology which satisfy SERI technology goals. These characteristics include the current, voltage and power output at rated conditions. Once the basic technologies to be utilized were defined and specific processes for each technology selected, IV curves were obtained. These IV curves were revised if needed to satisfy SERI technology goals prior to development of conceptual module and system designs. The nature and characteristics of the technology and process were considered in revising the IV curves so that the revisions were performed in a technology-consistent manner. This was the first step in the module and system design process illustrated in Figure 3-1.

The next step was to define system design constraints. First generic systems were selected and specific system characteristics defined. The system design constraints thus obtained not only serve as inputs to develop systems from module designs, but also are used in conjunction with the cell parameters to define module design constraints. The system design constraints include system power level, nominal DC voltage, and DC voltage limits. The module constraints obtained from the system constraints include module size and voltage. In the case of residential roof-mounted applications, for example, module lengths should correspond to standard roof support spacing. Those module design constraints obtained from the particular cell technology characteristics include maximum cell size and cell-to-cell spacing. The PV module for each technology and application is designed using the module optimization methodology [3]. See Appendix B for details of the methodology.

Module voltage and power characteristics as a function of temperature are next determined and used with the array voltage and power constraints to determine the optimum series string of modules. First the DC voltage and AC power windows as a function of expected temperature are obtained for various numbers of series-connected modules. The option which is most closely divisible into the desired system output power, in addition to providing the optimum voltage window, is chosen for the system series string design. The full system is then obtained by paralleling series strings until the desired power is obtained.

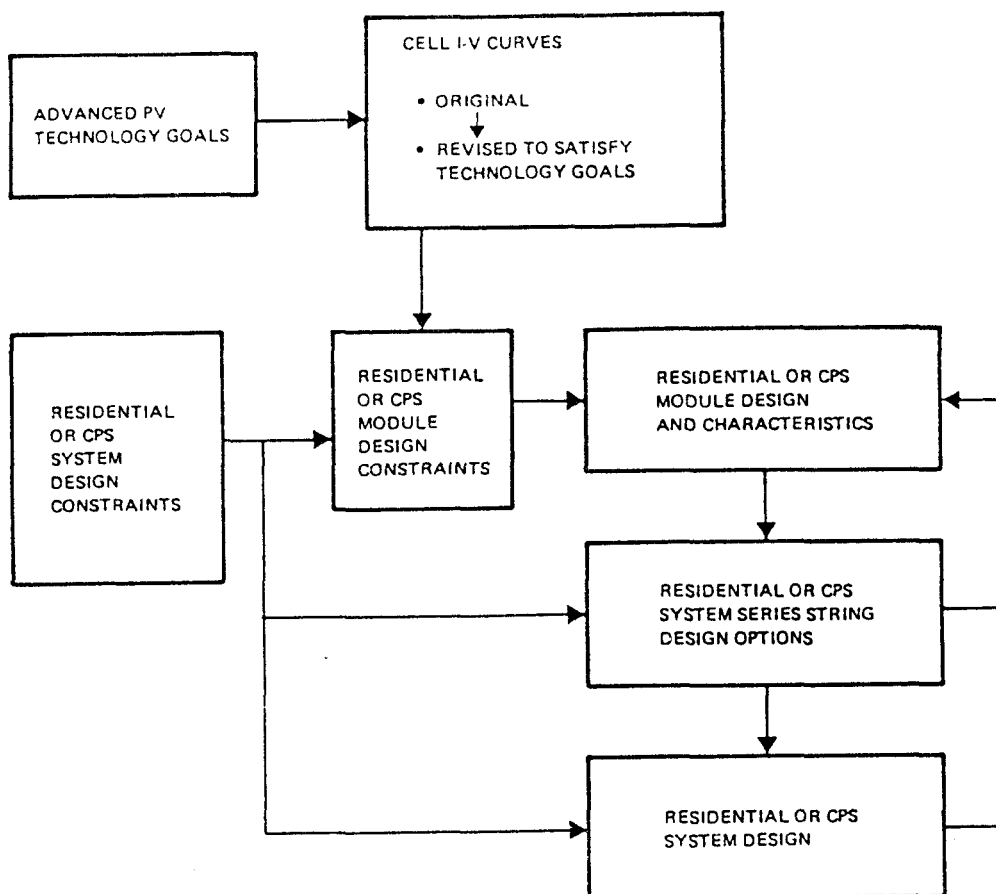


Figure 3-1. MODULE AND SYSTEM DESIGN PROCESS

In section 3.1.1 the selection of the generic systems is discussed, and block diagrams of the generic systems are presented. In section 3.1.2 the system and module constraints required to exercise the design methodologies are presented and discussed. Section 3.1.3 describes both the module electrical design methodology and the array design methodology.

3.1.1 Selection of System Applications

Generic PV systems are classified into three categories: residential, intermediate load and central power station. Residential systems produce power up to 10 kW. Intermediate load applications range in power from 10 to 500 kW, and CPS applications are greater than 500 kW. The residential and CPS system applications have been selected for design and analysis in order to bound the ranges of possible applications. Studies performed by Sandia Laboratories [25] have shown that residential systems are most economical in the 4 to 8 kW range when operated in an interactive mode with public utility. Therefore, residential designs were performed at 4 and 8 kW. In a series of studies, [26, 27, 28] CPS conceptual designs were performed for Sandia Labs. The

critical power in a CPS design is not the total plant power but the power handled by each inverter. For ease of design and analysis the smallest inverter design from the studies (2 MW) was used for our CPS subsystem design. The full system is then obtained by paralleling 25 inverter outputs to obtain a nominal 50 MW system. A matrix listing the technologies and processes used for the residential and CPS designs is contained in Table 3-1.

Table 3-1. TECHNOLOGY APPLICATIONS MATRIX

Technology	Process	System Type	
		Residential	CPS
Polycrystalline Silicon (Flat Plate)	RTR Recrystallization	4 kW/8 kW	50 MW
Amorphous Silicon (Flat Plate)	Integrated Series-Connected Cells Deposited on Glass	4 kW/8 kW	50 MW
Cadmium Sulfide (Flat Plate)	CdS/CuInSe ₂ Ribbon	4 kW/8 kW	50 MW
Gallium Arsenide (Flat Plate)	Shallow, Homojunction Cells Grown on Reusable Substrates (CLEFT)	4 kW/8 kW	--
Gallium Arsenide (Concentrating)	Multi-junction, Cascaded Cells with 500 x Point- Focus Fresnel	--	50 MW

A block diagram of a typical residential PV system [11], which can be used in conjunction with any of the listed technologies, is shown in Figure 3-2. The layout and interconnections are typical of most applications in which the PV power system is paralleled and interactive with public utility. The roof-mounted array contains blocking diodes on each string either on the roof or in a separate junction box on the wall outside the power conditioning room, such as the maintenance and safety enclosure (M&S) shown in the diagram. The M&S enclosure also contains fuses, monitoring jacks, and disconnect and shorting switches plus varistors for lightning protection. The individual DC conductors from each row of the array are usually not connected on the roof but are brought down to the maintenance and safety closure and interconnected beyond the monitor points. Each individual conductor can be broken for maintenance on a single row. Inside the house, in the power conditioning room a DC disconnect switch is encountered before the DC is connected to the inverter. This provides positive safety in the event that the inverter should require maintenance.

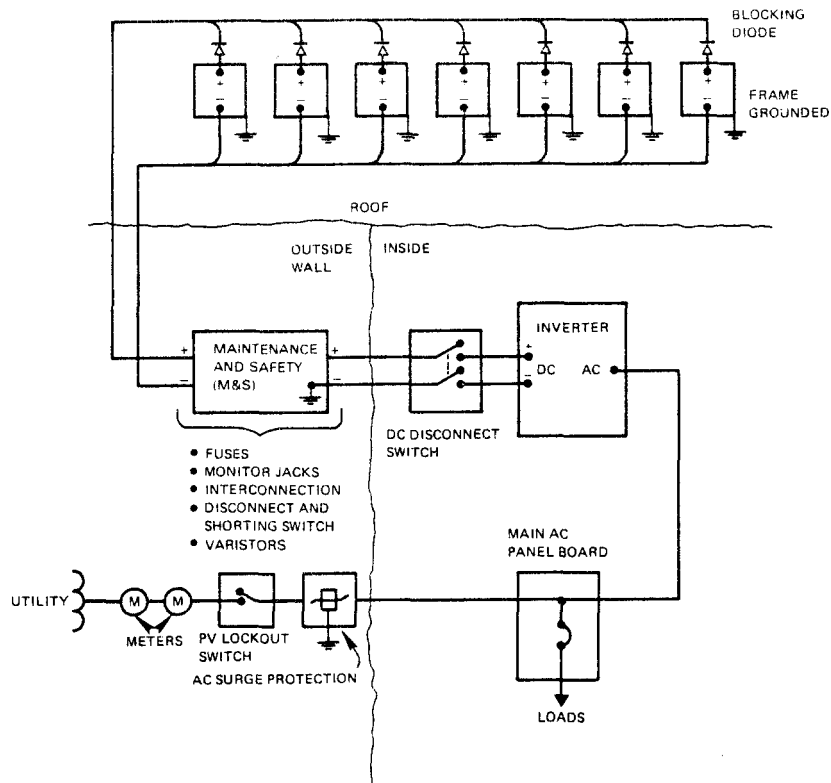


**Figure 3-2. 4 kW POLYCRYSTALLINE SILICON
RESIDENTIAL PV SYSTEM BLOCK DIAGRAM [11]**

Residential inverters can be obtained in 2 kW steps. The inverter is sized to handle the highest expected power from the array. For a 4 kW AC system, the array must be rated to deliver at least 4.6 kW DC. Under cold temperature, high insolation conditions, the array power may reach close to 6 kW DC under optimum conditions. Therefore, a 6 kW inverter would be used. Voltage input windows for residential inverters are typically 160-250 V.

The inverter AC is tied to the utility line in the main AC panel board before routing to the loads. At the utility service entrance, a PV lockout switch is provided for the utility line to ensure positive disconnect from the PV power system in the case of utility maintenance. AC surge protection is also provided and may be included as part of the PV lockout switch. Two utility meters are placed on the utility line to monitor the power in and the power out of the building.

All residential PV power systems contain basically the same components and functions. Therefore, all residential arrays designed for advanced PV applications in this study will interface with the same power conditioning system.

A typical residential control system and protection scheme is enumerated in Table 3-2. As previously discussed, the system contains manual controls in the form of both DC and AC disconnects and monitoring jacks. The system also contains automatic controls, usually in the inverter. The inverter AC output is tied and synchronizes with utility. The inverter will automatically dis-

Table 3-2. PV RESIDENTIAL CONTROL SYSTEM

- Manual Control
 - Monitor and Break Each String
 - DC Disconnect Switch
 - AC Disconnect Switch
 - Circuit Breaker on Inverter Output
- Automatic (Inverter Controlled)
 - AC, Tied and Synchronized to Utility, Feeds Power to load or utility based on load demand
 - Turns on automatically when array power exceeds inverter tare power
 - Disconnects automatically
 1. Array power less than tare power
 2. Array power or voltage too high or too low
 3. Loss of utility tie
 4. Utility voltage or frequency out of range
 5. Ground fault detected
- Fuses, Varistors and Breakers for Surge Protection

connect if the utility power shows anomalous behavior such as out of frequency or loss of utility tie. The inverter will also disconnect from the PV array if the array power or voltage is too high, or the power is less than the inverter no load power.

A block diagram of a typical CPS application is shown in Figure 3-3 [26, 27, 28]. Since only a few conceptual designs have been performed, no prototypes exist at present. The power conditioning system is therefore not as well-defined as in the case of residential applications. In general, however, certain characteristics are seen to be common to all systems. Subarrays of several megawatts will interface with a single inverter to produce an AC output which will be transformed to high voltage and paralleled with other inverter outputs to produce hundreds of megawatts of power at voltages of hundreds of kilovolts. The nominal input to the inverter is limited to approximately 1,000-2,000 V to prevent excessive voltage isolation requirements in the PV modules. The inverter AC will be stepped up to the 30-70 kV range either in the inverter or in a separate transformer. The array may be center grounded to limit voltage on either side of ground. Blocking diodes are required on both the positive and negative lines. At the inverter station, disconnect switches, monitor jacks and surge protection are required - much as in the case of the residential system.

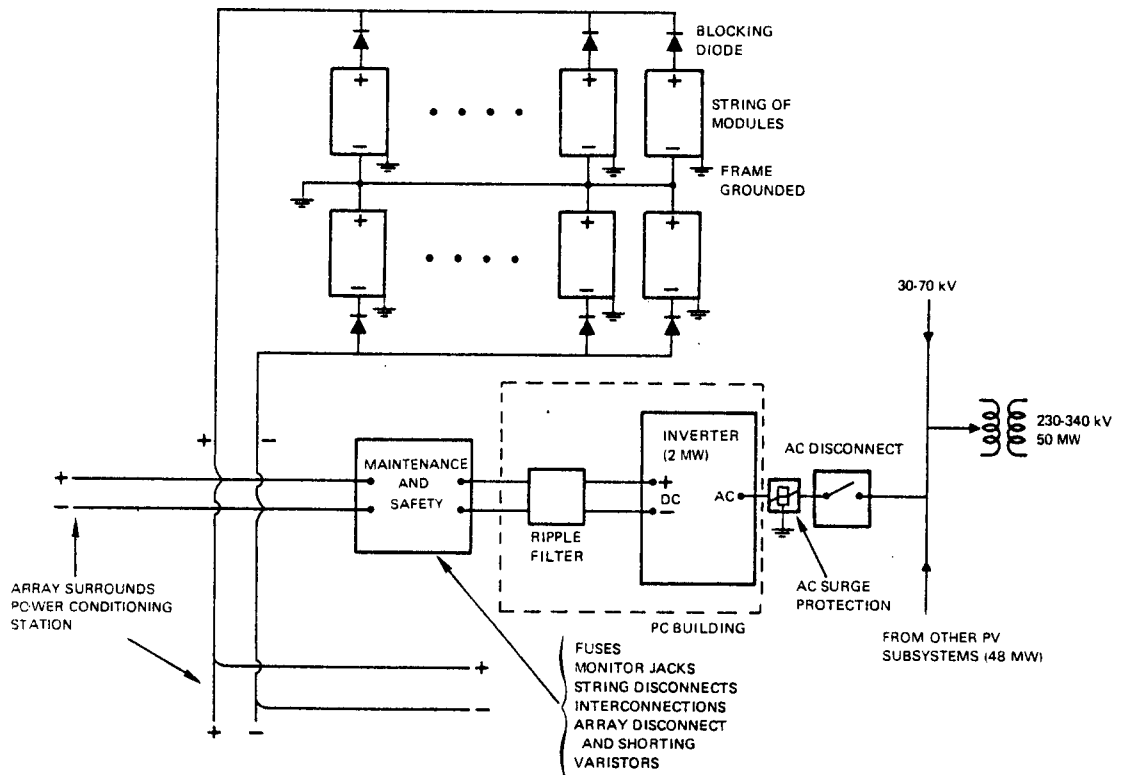


Figure 3-3. TYPICAL CPS PV SYSTEM BLOCK DIAGRAM

A control system for the CPS inverter substation is shown in Table 3-3. Most of the control functions are similar to those used in residential applications. However, the subsystem may contain the capability for control from a remote location, such as a central control station.

Table 3-3. PV CPS CONTROL SYSTEM

- Manual Control
 - Monitor and Break Each String
 - DC Disconnect
 - AC Disconnect
 - Breakers on Inverter Input and Output
 - Operator Control from Remote Location
- Automatic (Inverter Controlled)
 - AC Tied and Synchronized to Utility
 - Turns on automatically when array power exceeds inverter tare power
 - Disconnects automatically
 1. Array power less than tare power
 2. Array power or voltage too high
 3. Loss of utility tie
 4. Utility voltage current or frequency out of range
 5. Ground fault detected
- Fuses, varistors, and blocking diodes for surge protection

3.1.2 System and Module Design Constraints

Based on the generic systems and block diagrams discussed in the previous section, the system design constraints shown in Table 3-4 were obtained for the residential applications. Two designs were produced, one with a minimum 4 kW AC power, the other with a minimum 8 kW AC power. The voltage at peak power has the range of 160 to 250 V. The combined efficiency of all power conditioning components is specified at 0.8765. The components and efficiencies which contribute to this overall efficiency are: cell mismatch efficiency of 0.98, wiring loss efficiency of 0.98, peak power tracking efficiency of 0.995, blocking diode efficiency of 0.997, and inverter efficiency of 0.92. The CPS applications have a minimum system AC power of 50 MW. The peak power voltage has a range of 800 to 1300 V DC with a nominal voltage of 1000 V. The combined efficiency of power conditioning components is the same as for residential applications, 0.8765.

Module design constraints were based on the system constraints, studies performed for residential and CPS applications, and the cell parameters for a particular technology. In this section, the design constraints which apply to all advanced technologies for residential and then for CPS modules are listed and discussed. Module design constraints for each application which are dependent on the particular cell technology will be listed and discussed in each technology section.

The design constraints which apply to all residential module designs are listed in Table 3-5. The maximum module open circuit voltage and maximum module peak power voltage are provided for personnel safety [29]. The acceptable module peak power voltages permit the use of modules either singly or in combination for battery charging applications and are all nearly divisible into the nominal 200 V system DC voltage [30]. Because reverse breakdown voltages and reverse bias stress susceptibility of advanced PV technologies are not well defined, the maximum allowable reverse cell voltage was specified by default as -6.7 V because this would produce a cell temperature of approximately 100°C [31] in a typical single crystal silicon module under worst case reverse bias conditions.

Because residential modules are usually mounted on roofs with 16, 24, 32, or 48-inch framing dimensions and because they require handling by one or two workmen using ladders, it is generally felt that the maximum acceptable module dimensions should be approximately 4 ft. x 4 ft. For these designs the maximum module dimensions were specified as 47.5 in. to allow for manufacturing tolerances and spacing during roof assembly. (Although metric units are considered more acceptable for technical studies, dimensions in this report have been provided in English units as well as metric to be more consistent with construction industry practices.) The spacing between the cells and the edge of the module is specified as 3/8 in. This will permit conductor runs along the edge of the module and sufficient distance to prevent shadowing due to the lip of the module frame. The amorphous silicon and gallium arsenide residential modules have smaller maximum module dimen-

Table 3-4. RESIDENTIAL AND CPS SYSTEMS DESIGN CONSTRAINTS

Constraint		Residential	CPS
System AC Power			
P_S (AC)		4 kW and 8 kW	50 MW
Peak Power Voltage nominal	V_{MPS}	200 V nominal	1000 V
Range		160-250 V	800-1300 V
Efficiency of Power Components			
η_{PC}		0.8765	0.8765

**Table 3-5. DESIGN CONSTRAINTS APPLIED TO
ALL RESIDENTIAL MODULE DESIGNS**

- Maximum Open Circuit Module Voltage at Low Temperature

$$V_{OCM}(\text{Max}) = 30V @ - 20^{\circ} C$$

- Maximum Module Peak Power Voltage

$$V_{MPM}(\text{Max}) = 20V$$

- Acceptable Module Peak Power Voltages

$$V_{MPM} = 5, 7.5, 10, 15, \text{ or } 20V$$

- Maximum Allowable Reverse Cell Voltage

$$V_{RMAX} = -6.7V$$

- Maximum Module Dimensions*

$$\text{Dim (Max)} = 47.5 \text{ in.} \times 47.5 \text{ in. (120.65 cm)}$$

- Edge Spacing

$$\Delta_{SE} = 3/8 \text{ in. (0.9525 cm)}$$

- Parallel Redundancy Desirable

Prevents bypass activation due to single cell shadowing,
single interconnect breaking or single cell cracking.

- * Amorphous Silicon - 11.75 in. X 47.5 in. (29.85 cm x 120.65 cm)
Ga As - 23.5 in. X 47.5 in. (59.69 cm x 120.65 cm)

sions due to technology process constraints [17, 8]. These are discussed in the amorphous silicon and gallium arsenide sections. Paralleling of cells or strings of cells is desirable to increase the module output and prevent bypass diode activation due to single cell shadowing, single interconnect breaking, or single cell cracking. Paralleling in the module was accomplished only after module and cell size constraints and module voltage constraints were satisfied and sufficient space was still available for paralleling.

The same types of constraints apply to the CPS module designs; however, the constraint values have been changed as indicated in Table 3-6. In general, CPS modules can be made larger and produce higher voltages than residential modules due to better installation and maintenance controls in a CPS application. Thus, the maximum open circuit module voltage has been specified as 150 V and the maximum module peak power voltage is 100 V. Acceptable module peak power voltages are 50 and 100 V which are both divisible into 1000 V nominal CPS system voltage. Maximum allowable reverse cell voltage is again -6.7 V due to lack of definition of reverse bias stress susceptibility.

The module dimensions have been changed to approximately 4 ft. x 8 ft. The amorphous silicon module size constraints, however, are still limited to 1 ft. x 4 ft. due to the postulated technology constraints, and the gallium arsenide concentrator design has an 8 ft. x 12 ft. size constraint based on the technique of mounting the module on a tracking pedestal. It is felt that two such modules could be mounted, one on either side of the center pedestal. The edge spacing remains at 3/8 in. for the flat plate applications; however, the gallium arsenide CPS concentrator application will require 1 in. edge spacing to permit use of a larger frame. Parallel redundancy is required for cracked cells and broken interconnects; however, cell shadowing is not considered to be a serious consideration for CPS applications.

Additional constraints on module designs which are based on particular cell technology will be discussed in each of the technology design sections.

3.1.3 Module and System Design Methodologies

3.1.3.1 Overview of Module Electrical Design Methodology

The electrical methodology [3] was developed to assist the module designer or analyst in determining the optimum physical layout and electrical connection of cells, within a module, for a given cell technology and application.

For all cases, the cell technology is represented by a J-V curve (current density versus voltage) or the key electrical parameters, V_{OC} , J_{SC} , V_{MPC} and J_{MPC} (open circuit cell voltage, short circuit current density, and voltage and current density at the maximum power point, respectively). The cell production process has been previously defined, and the cell character-

**Table 3-6. DESIGN CONSTRAINTS APPLIED TO
ALL CPS MODULE DESIGNS**

- Maximum Open Circuit Module Voltage at Low Temperature

$$V_{OCM}(\text{Max}) = 150V @ - 20^{\circ}C$$

- Maximum Module Peak Power Voltage

$$V_{MPM}(\text{Max}) = 100V$$

- Acceptable Module Peak Power Voltage

$$V_{MPM} = 50V \text{ or } 100V$$

- Maximum Allowable Reverse Cell Voltage

$$V_{RMAX} = -6.7V$$

- Maximum Module Dimensions*

$$\text{Dim (Max)} = 47.5 \text{ in.} \times 95.0 \text{ in.} (120.65 \text{ cm} \times 241.3 \text{ cm})$$

- Edge Spacing⁺

$$\Delta_{SE} = 3/8 \text{ in.} (0.9525 \text{ cm})$$

- Parallel Redundancy Desirable

- For cracked cells and broken interconnects
- Not for Cell Shadowing

* Amorphous Silicon - 11.75 in. X 47.5 in. (29.85 cm x 120.65 cm)
 Ga As - 95.0 in X 143.0 in. (241.3 cm x 363.22 cm)
 + Ga As - 1.0 in. (2.54 cm)

ristics such as material resistivities and thickness, metallization grid patterns, and breakdown voltage do not vary. The cell characteristics which are determined in the module design are the cell dimensions. It is assumed that the manufacturer is capable of producing optimum metallization grid patterns on the cell for any cell dimensions that might be obtained. Cell efficiency is held constant during the calculations. If the cell dimensions obtained are smaller than expected, permitting a higher efficiency, the user may repeat the methodology with an updated efficiency. Table 3-7 lists the cell parameters and module conductor parameters required by the methodology.

The primary objective of the methodology is to produce a module with specific peak power voltage, V_{MPM} , and reverse bias protection using bypass diodes. Other design objectives such as desired module dimensions or cell area are considered secondary. The flow-charted algorithms and computer code are designed to satisfy this objective. The algorithm can be easily altered, however, to satisfy other objectives when using the methodology in hand analysis.

As indicated in Figure 3-4, the design starts with the cell J-V curve. Although efficiency may vary with cell area, the J-V curve is obtained from characteristics at the approximate or maximum cell area anticipated. The parameters thus obtained from this standardized curve can be easily scaled once the final cell area is determined.

The methodology proceeds, as shown in the second box, by providing cell specifications such as maximum allowable cell temperature and cell reverse breakdown voltage, and module design specifications such as peak power voltage and maximum open circuit voltage, for use as design constraints. Additional constraints are then derived, based on these initial constraints. The constraints and specifications used in this general constraint segment are listed in Table 3-8.

The user may specify a series of acceptable module voltages (V_{MPM} 's). The methodology attempts to design a module to the maximum voltage specified (V_{MPMAX}) but will use a lower voltage if a design cannot be obtained at the highest voltage. The module design must not exceed the maximum allowable open circuit voltage (V_{OCMAX}) for a particular application at the lowest expected cell temperature (T_L). Spacings from end cells to edges of the module (Δ_{SE} 's) and between cells (Δ_S 's) in both the series and parallel directions are specified by the user.

Table 3-7. REQUIRED CELL AND CONDUCTOR PARAMETERS

- J_{SCC} , V_{OCC} , J_{MPC} , V_{MPC} ,
 - From J-V curve at standard insolation and single temperature
- $\Delta V/\Delta T$ (Open Circuit Voltage Temperature Coefficient)
 - From V-T curve
 - From J-V curves at 2 temperatures
- Reverse Bias Stress Parameters
 - V_B (Breakdown Voltage)
 - From reverse I-V curve
 - $\Delta T/\Delta S$ (Temperature Coefficient for Insolation Power) and
 - $\Delta T/\Delta P$ (Temperature Coefficient for Power Dissipation)
 - From thermal analysis of laminations
 - From typical module data
- N_{ACI} (Number of Across-the-Cell or Redundant Interconnects)
 - If applicable-from cell technology
- Resistance Limited Technologies
 - R (Sheet Resistivity of Worst Current Carrier in Cell)
 - P_{FL} (Fractional Power Loss Allowable in Current Carrier)
 - From manufacturer
- Module Metalization and Conductor Requirements
 - ρ (Resistivity of Current Carriers in Module)
 - P_F (Fractional Power Loss Allowable in Module Conductors)
 - From handbook or manufacturer

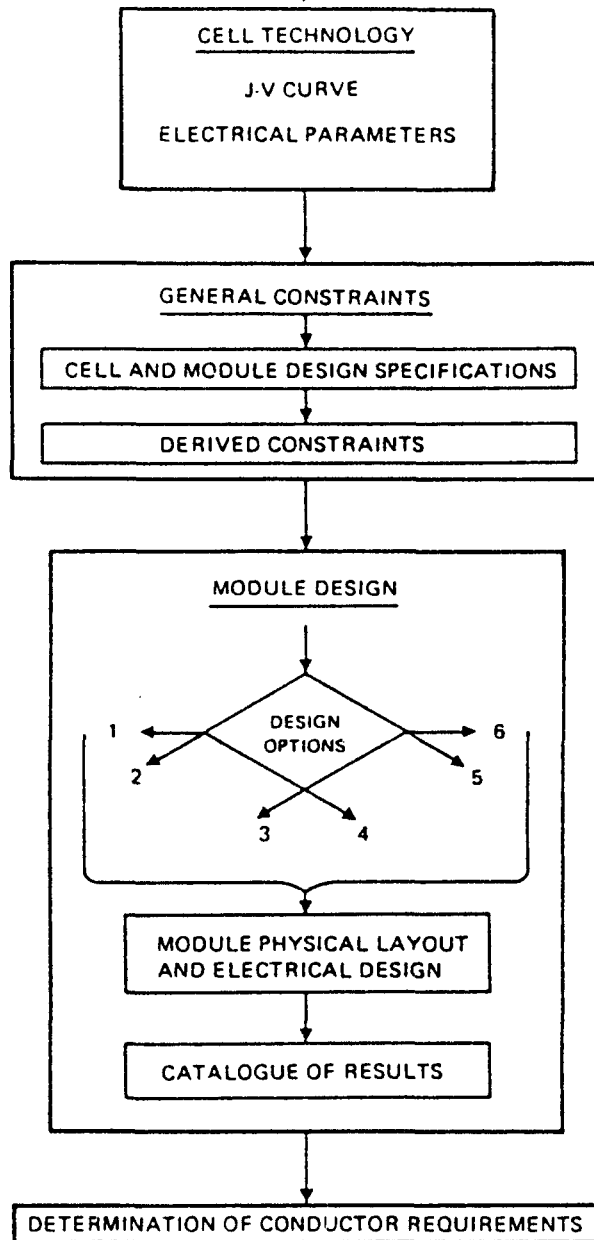


Figure 3-4. OVERVIEW OF ELECTRICAL METHODOLOGY

Table 3-8. GENERAL DESIGN CONSTRAINTS

Constraint and Symbol	Type*
Acceptable Module Peak Power Voltages (V_{MPM} 's)	S
Maximum Module Open Circuit Voltage (V_{OCMAX})	S
Lowest Cell Temperature Expected in Application (T_L)	S
Cell-to-Edge and Cell-to-Cell Spacings (Δ_{SE} and Δ_S)	S
Maximum Reverse Cell Voltage Allowable (V_{RMAX})	S/D
Maximum Cell Temperature in Reverse Bias (T_{CMAX})	S
Maximum Number of Cells in Bypass Group (N_{BPMAX})	D
Maximum Number of Bypass Groups in Series (N_{GMAX})	D
Maximum Number of Cells in Series in Module (N_{BGMAX})	D
Minimum Number of Parallel Segments Required for Redundancy (N_{MMIN})	D

*S = Value Specified

D = Value Derived

In order to determine the maximum number of cells allowable in a bypass group (N_{BPMAX}) for reverse bias protection, the user may input maximum allowable cell temperature in reverse bias (T_{CMAX}) or maximum reverse voltage allowable (V_{RMAX}), or V_{RMAX} may be calculated from T_{CMAX} and various cell parameters. The maximum number of bypass groups in series (N_{GMAX}) and the maximum number of cells in series in the module (N_{BGMAX}), which is $N_{BPMAX} \times N_{GMAX}$, are determined from V_{MPMAX} and V_{OCMAX} .

The minimum number of parallel segments required for redundancy (N_{MMIN}) addresses the case of individual cell shadowing or broken interconnects. If N_{MMIN} or more cells or bypass groups are paralleled in the module, the bypass group will not become reverse-biased under these conditions but will continue to produce power, albeit at a reduced level.

Following the determination of all general constraints, the methodology permits the user to design the module through any one of six options. The design options are specified in terms of cell and module dimensional con-

straints. The options are numbered, as in Table 3-9, in order of decreasing packing fraction which would normally be obtained from each option. Thus, in most cases, designing a module with maximum cell area and maximum module dimensions constraints will produce a design with higher packing fraction than specifying fixed-cell dimensions and maximum module dimensions. Although additional constraint combinations could be postulated, they would tend to produce low packing fractions, or would be contradictory or contain too many variables.

Table 3-9. MODULE DESIGN OPTIONS

IN ORDER OF DECREASING PACKING FRACTION, DIMENSIONAL CONSTRAINTS GIVEN ARE:

- 1) MAXIMUM CELL AREA AND MAXIMUM MODULE DIMENSIONS
- 2) NUMBER AND DIMENSIONS OF CELLS
- 3) FIXED CELL AND MAXIMUM MODULE DIMENSIONS
- 4) MAXIMUM CELL WIDTH AND AREA AND FIXED MODULE DIMENSIONS
- 5) MAXIMUM CELL AREA AND FIXED MODULE DIMENSIONS
- 6) MAXIMUM CELL DIMENSIONS AND FIXED MODULE DIMENSIONS

Design option number 4 is a special case which considers a cell technology that is resistance-limited. In this situation, one of the current carriers in the cell has a sufficiently high resistivity to produce significant power losses if the length in the direction of current is not constrained. This is characteristic of many integrated technologies and technologies in which metallization grids cannot be used.

Although the various module design option algorithms perform different calculations, they all result in a module design in which the physical layout of the cells in the module, the actual cell and module dimensions, the series and parallel interconnections, and the module conductor requirements are specified. The bypass group design (N_{bp}) and number of bypass groups in series (N_G) may also be modified in the process. The results of the design process, including all physical and electrical characteristics, are listed at the end of the design process.

3.1.3.2 Array Design Methodology

The array design methodology is diagrammed in Figure 3-5. It starts with a completed module design such as obtained from the module design methodology described in the previous section. It also requires the cell temperature

dependence parameters which specify the change in open circuit voltage with temperature and short circuit current with temperature. Using this information the module voltage and power are calculated at cell temperatures typical of those expected in actual operation. Series strings of modules are then postulated and the voltage windows, as a function of the same temperatures as used in the module calculations, are determined. These voltage windows are compared with the system voltage range constraint. For the same series string options, the AC power windows as a function of temperature are also calculated. The AC power window for the string is determined by multiplying the DC power by the efficiency of the combined power conditioning components, 0.8765.

The full array design is obtained by selecting the series string option which satisfies both the voltage window and is divisible into the minimum AC system power constraint. If the system voltage or power constraints cannot be satisfied by any series string and paralleling options, the module must be redesigned.

The techniques for the array design methodology can be easily implemented on a minicomputer as was done for this project. The results of the HP 85 simulation are shown in each section under the system design.

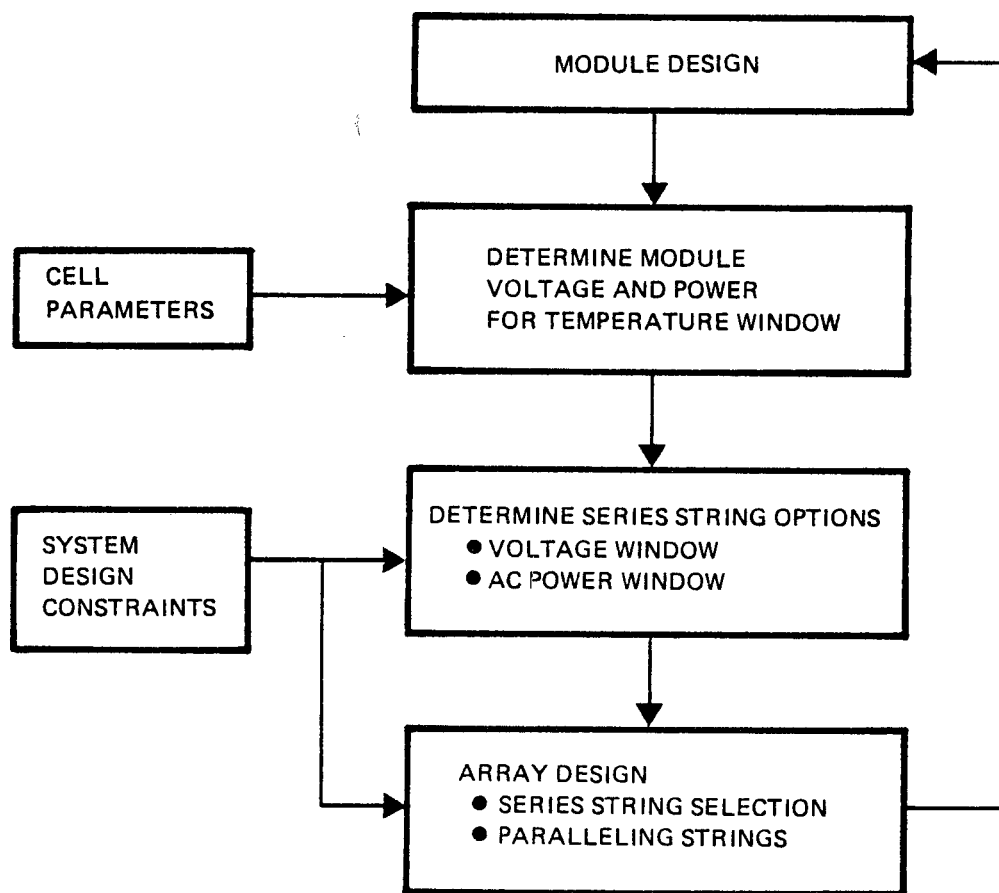


Figure 3-5. ARRAY DESIGN METHODOLOGY

3.2 POLYCRYSTALLINE SILICON CONCEPTUAL DESIGNS

The polycrystalline silicon system designs were developed using the design approach previously discussed in section 3.1 based on the module and system design methodologies discussed in section 3.1.3.

3.2.1 Cell Parameters

The polycrystalline silicon residential and CPS designs are both based on the ribbon-to-ribbon recrystallization (RTR) process developed by Motorola [4]. An IV curve obtained from the paper by Sarma is shown as the upper curve in Figure 3-6. This curve is described in the paper as "one of the best." The average efficiency for the process was quoted as 11.5 percent, therefore, the lower curve was obtained based on the 11.5 percent efficiency. This curve was obtained by lowering the short circuit and the fill factor while preserving the open circuit voltage at 0.6 V. Normalizing this curve for a one-square-centimeter cell, the parameters listed in Table 3-10 were obtained. The voltage at peak power is 0.5 V and the current density at peak power is 23 mA/cm². The voltage and current variations with temperature are typical of silicon technology. The current variation with temperature is expressed as a fractional variation and would be multiplied by the actual cell current to determine the current variation with temperature. The cell contains three across-the-cell interconnects to provide redundancy in the case of cracked

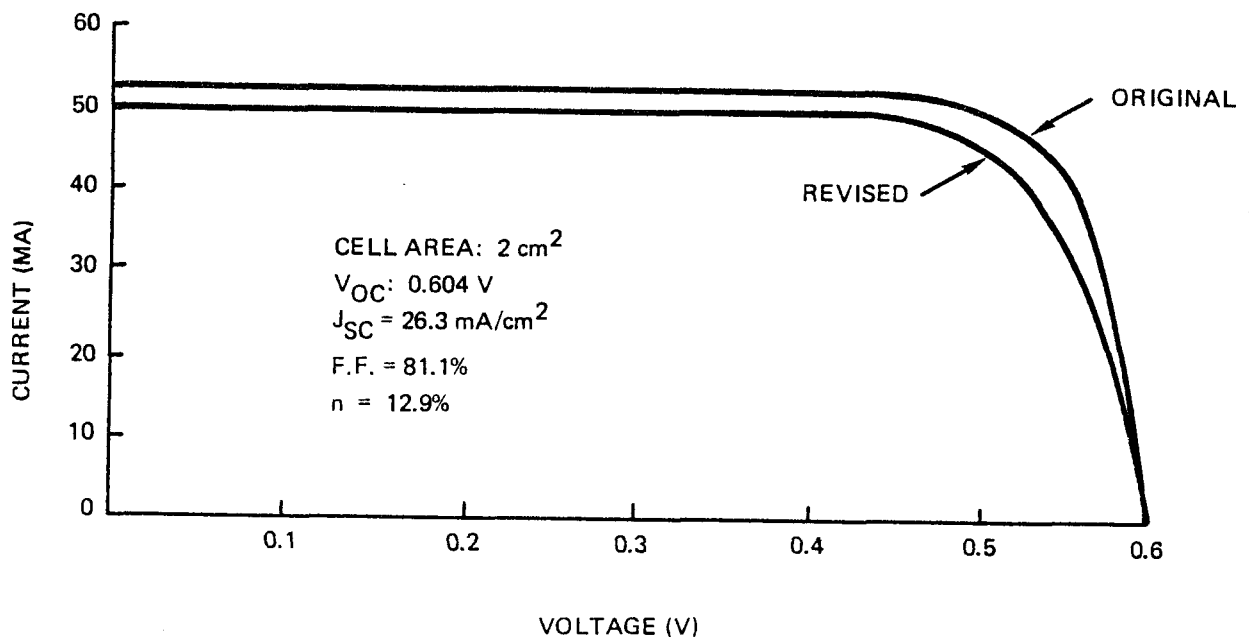


Figure 3-6. POLYCRYSTALLINE SILICON I-V CURVE

Table 3-10. POLYCRYSTALLINE SILICON CELL PARAMETERS

V_{OCC}	=	0.60V
V_{MPC}	=	0.50V
J_{SCC}	=	25.0mA/cm ²
J_{MPC}	=	23.0mA/cm ²
FF	=	0.767
P_C	=	11.5mW/cm ²
η_C	=	11.5 percent
$\Delta V/\Delta T$	=	-2.2mV/°C
$\Delta f_I/\Delta T$	=	0.00061/°C
N_{ACI}	=	3 Across-the-Cell (Redundant) Interconnects

cells or broken interconnects. These redundant interconnects are useful in reducing the number of parallel strings or cells required to satisfy parallel redundancy constraints.

3.2.2 Polycrystalline Silicon Residential Designs

3.2.2.1 Residential Module Designs

The design constraints which apply to all residential module designs were discussed in section 3.1.2 and are reproduced here in Table 3-11 for the reader's convenience. Table 3-12 presents the module design constraints which apply specifically to polycrystalline silicon residential modules. (Although metric units are considered more acceptable for technical studies, dimensions in this report have been provided in English units as well as metric to be more consistent with construction industry practices.) The maximum cell length in the series direction - which corresponds also to the width of the silicon ribbon - and the maximum cell length in the parallel direction were specified as 6.0 cm and 16.0 cm, respectively, based on telephone communication with K. Sarma of Motorola [32]. The 1/16 in. interior spacing between cells is consistent with spacing requirements for cell assembly in modules in which voltage differentials are within 50 V [33]. The maximum number of cells in a bypass group was determined from the maximum

**Table 3-11. DESIGN CONSTRAINTS APPLIED TO
ALL RESIDENTIAL MODULE DESIGNS**

- Maximum Open Circuit Module Voltage at Low Temperature

$$V_{OCM}(\text{Max}) = 30\text{V @ } -20^{\circ}\text{C}$$

- Maximum Module Peak Power Voltage

$$V_{MPM}(\text{Max}) = 20\text{V}$$

- Acceptable Module Peak Power Voltages

$$V_{MPM} = 5, 7.5, 10, 15, \text{ or } 20\text{V}$$

- Maximum Allowable Reverse Cell Voltage

$$V_{RMAX} = -6.7\text{V}$$

- Maximum Module Dimensions*

$$\text{Dim (Max)} = 47.5 \text{ in. X } 47.5 \text{ in. (120.65 cm)}$$

- Edge Spacing

$$\Delta_{SE} = 3/8 \text{ in. (0.9525 cm)}$$

- Parallel Redundancy Desirable

Prevents bypass activation due to single cell shadowing,
single interconnect breaking or single cell cracking.

* Amorphous Silicon - 11.75 in. X 47.5 in. (29.85 cm x 120.65 cm)
Ga As - 23.5 in. X 47.5 in. (59.69 cm x 120.65 cm)

**Table 3-12. POLYCRYSTALLINE SILICON DESIGN CONSTRAINTS
FOR RESIDENTIAL MODULES**

- Maximum Cell Length in Series Direction (Ribbon Width)

$$L_{CS} = 6.0\text{cm}$$

- Maximum Cell Length in Parallel Direction

$$L_{CP} = 16.0\text{cm}$$

- Interior Spacing

$$\Delta_{SI} = 1/16 \text{ in. (0.15 cm)}$$

- Maximum Number of Cells in Bypass Group

$$N_{BPMAX} = 11 \text{ cells}$$

- Minimum Number of Cells or Strings in Parallel

$$N_{MMIN} = 3 \text{ for cracked cell or broken interconnect}$$

allowable reverse cell voltage of -6.7 V (previously specified in Table 3-11). The equation used to obtain $N_{BP\text{MAX}}$ is:

$$N_{BP\text{MAX}} = 1 - \frac{V_{R\text{MAX}} + V_{FD}}{V_{OCC}} \quad \text{Eq.(3-1)}$$

where V_{FD} = forward voltage of bypass diode. The parallel redundancy constraint of three cells or strings in parallel was obtained from the relationship between the cell short-circuit current and peak-power current, and the number of across-the-cell interconnects, by the equation:

$$N_{M\text{MIN}} = \frac{J_{SCC}}{2N_{ACI} (J_{SCC} - J_{MPC})} \quad \text{Eq.(3-2)}$$

Using the module electrical design optimization methodology discussed in section 3.1.3.1, with design option 6 to produce a module with fixed dimensions, the polycrystalline silicon residential module design characteristics listed in Table 3-13 were obtained. The cell dimensions of 5.78 cm for the series length and 14.68 cm for the parallel length are slightly less than the maximum cell dimensions of 6.0 cm and 16.0 cm, respectively. Using the cell series length of 5.78 cm, 20 cells can fit exactly in the 47.5 inch module dimension; therefore, $N_{BP\text{MAX}}$ was specified as 10 cells and two bypass groups fit exactly in the module dimension.

As illustrated in the polycrystalline silicon residential module diagrams in Figure 3-7, the maximum allowable module voltage of 20 V was obtained by snaking the series group back in the opposite direction, so that 40 cells are connected in series. The parallel length of the module was then capable of accepting four strings in parallel for each bypass group. Thus, 20 cells are arranged in the series direction in the module, while eight cells are arranged in the parallel direction in the module.

The packing factor obtained for the module is 0.933. The module electrical parameters are also listed in Table 3-13. The overall module efficiency, which is obtained by multiplying the cell efficiency of 11.5 percent by the packing factor, is 10.7 percent.

3.2.2.2 Residential System Designs

Following the system design methodology discussed in section 3.1.3.2, module voltage and power were determined at various cell temperatures characteristic of typical operations. The results are shown in Table 3-14, using $-0.0022 \text{ V/}^\circ\text{C}$ and $0.0013 \text{ A/}^\circ\text{C}$ as the voltage and current variations with

Table 3-13. POLYCRYSTALLINE SILICON RESIDENTIAL
MODULE DESIGN

- Cell Dimensions

- $L_{CS} \times L_{CP} = 2.28 \text{ in.} \times 5.78 \text{ in.} = 13.18 \text{ in.}^2$
 $5.78 \text{ cm} \times 14.68 \text{ cm} = 84.9 \text{ cm}^2$

- Bypass Group and Parallel Redundancy

- $N_{BP} = 10 \text{ cells}$
 - $N_M = 4 \text{ strings}$

- Module Dimensions and Layout

- $L_{MS} \times L_{MP} = 47.5 \text{ in.} \times 47.5 \text{ in.} (120.65 \text{ cm})$
 - 20 in. S-direction X 8 in. P-direction
 - Packing Factor = 0.933

- Module Electrical

- 40 series X 4 parallel
 - $V_{OCM} = 24.0V$, $V_{MPM} = 20.0V$
 - $I_{SCM} = 8.5A$, $I_{MPM} = 7.8A$
 - $P_M = 156W$, $\eta_M = 10.7 \text{ percent}$

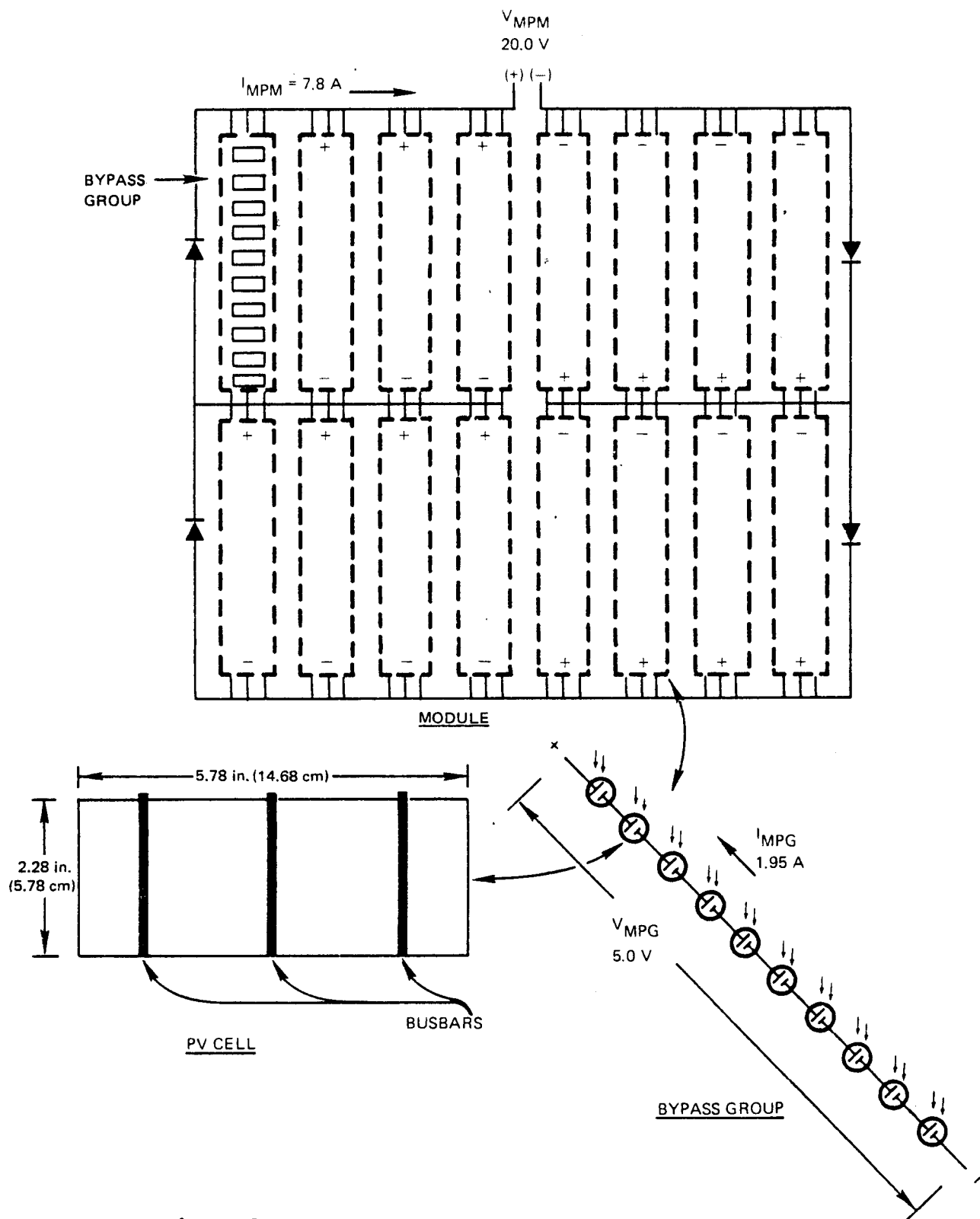


Figure 3-7. POLYCRYSTALLINE SILICON RESIDENTIAL MODULE

temperature. The increase in cell temperature above ambient, (TCELL-TAMB) due to insolation, is shown in the table as 25°C. The ambient conditions are listed in the first and second column. SOC stands for Standard Operating Conditions. The third column contains the associated cell temperatures. The calculated voltages, currents and powers are shown in the remaining columns. NOCT/1000 stands for Nominal Operating Cell Temperature at 1000 W/m².

Based on the residential module data as a function of the temperature window, the DC voltages shown in Table 3-15 were obtained for the series string options of 9, 10, and 11 modules, respectively. At rated conditions of 25°C cell temperature, the 10-module option produces a voltage at peak power of 200 V and an open-circuit voltage of 240 V. This option also produces an acceptable peak power voltage variation with temperature.

The AC power window for each of the series-string options is shown in Table 3-16. The powers were obtained by multiplying the DC power of the series string by the overall power conditioning efficiency of 0.8765. It can be seen that the 10-module option produces a power at 25°C, which is approximately divisible into 4 kW - the minimum AC power constraint for the residential system. Thus, three of these strings could be paralleled to obtain the 4-kW residential system and six strings could be paralleled to obtain the 8-kW system.

The 4-kW and 8-kW polycrystalline silicon residential array schematics are illustrated in Figure 3-8. Ten modules are connected in series to obtain the nominal 200 V desired. In one case, three subarrays are connected in parallel to obtain a DC power of 4.68 kW. The AC power is then 4.10 kW. For the other case, six subarrays are connected in parallel to obtain a DC power of 9.36 kW. The AC power is then 8.20 kW.

3.2.3 Polycrystalline Silicon CPS Designs

3.2.3.1 CPS Module Design

The design constraints which apply to all CPS module designs were previously discussed in section 3.1.2 and are reproduced here in Table 3-17 for the reader's convenience. Table 3-18 lists the CPS module constraints which apply specifically to the polycrystalline silicon technology. These constraints are the same as those previously discussed for the polycrystalline silicon residential modules.

Using the module optimization methodology discussed in section 3.1.3.1, the CPS module characteristics presented in Table 3-19 were obtained. Design option 6 was used to produce the module with the fixed dimensions of 47.5 in. x 95.0 in. The series and parallel lengths of the cells are 5.78 cm x 15.82 cm, respectively. With the cell series length of 5.78 cm, 20 cells could be placed in the module dimension of 47.5 in.; thus, the bypass group

Table 3-14. POLYCRYSTALLINE SILICON RESIDENTIAL MODULE DATA

MODULE ANALYSIS WORK SHEET...P-SI...20 VOLT RESIDENTIAL

```

VOC DELTA  -.0022
W/T--U/C
UMAX DELT  -.0022
W/T--U/C
ISC DELTA   .0013
W/T--A/C
IMAX DELT   .0013
W/T--A/C
NO OF CEL   40
IN SERIES
NO OF CEL   4
IN //
TCELL-TAM   25
AT 1 SUN
    
```

CONDITION	TAMB DEG-C	TCELL DEG-C	VOC VOLTS	ISC AMPS	UMAX VOLTS	IMAX AMPS	PMAX WATTS
LOW TEMP	-10	15	24.88	8.448	20.88	7.748	161.7782
RATED CON	25	25	24	8.5	20	7.8	156
S.O.C. NOCT/1000	20	45	22.24	8.604	18.24	7.904	144.1690
T=30C/86F	30	55	21.36	8.656	17.36	7.956	138.1162
T=40/104F	40	65	20.48	8.708	16.48	8.008	131.9718
T=50/122F	50	75	19.6	8.76	15.6	8.06	125.736

Table 3-15. POLYCRYSTALLINE SILICON RESIDENTIAL SUBARRAY DC VOLTAGE WINDOW

PV STRING VOLTAGE

* TEMP AMB CELL	NO MODS= 9		NO MODS= 10		NO MODS= 11	
	UMAX	UOC	UMAX	UOC	UMAX	UOC
TAMB -10 TCELL 15	187.92	223.92	208.8	248.8	229.68	273.68
0 25	180	216	200	240	220	264
20 45	164.16	200.16	182.4	222.4	200.64	244.64
30 55	156.24	192.24	173.6	213.6	190.96	234.96
40 65	148.32	184.32	164.8	204.8	181.28	225.28
50 75	140.4	176.4	156	196	171.6	215.6

*TEMPERATURE IS IN °C

**Table 3-16. POLYCRYSTALLINE SILICON RESIDENTIAL SUBARRAY AC POWER OUTPUT
WITH PARASITIC LOSS**

*PV STRING POWER... $POW=PMOD*NMOD*NALL$

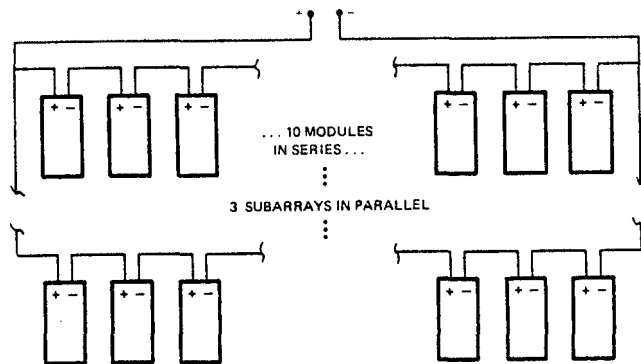
NMIS= .98MISMATCH
 NWIR= .98WIRE LOSS
 NPPT= .995PK POW TR.
 NBDID= .997BLK DIODE
 NPCO= .92POW COND
 NALL= .8765127OVERALL

	TEMP	NO MODS=	NO MODS=	NO MODS=
	AMB	9	10	11
	CELL			
TAMB	-10	1276.206	1418.007	1559.808
TCELL	15			
	0	1230.624	1367.360	1504.096
	25			
	20	1137.293	1263.659	1390.025
	45			
	30	1089.545	1210.606	1331.666
	55			
	40	1041.075	1156.750	1272.425
	65			
	50	991.8828	1102.092	1212.301
	75			

*POWER IS IN WATTS

4 kW ... POLYCRYSTALLINE SILICON ... 20 VOLT MODULE

RESIDENTIAL ARRAY SCHEMATIC

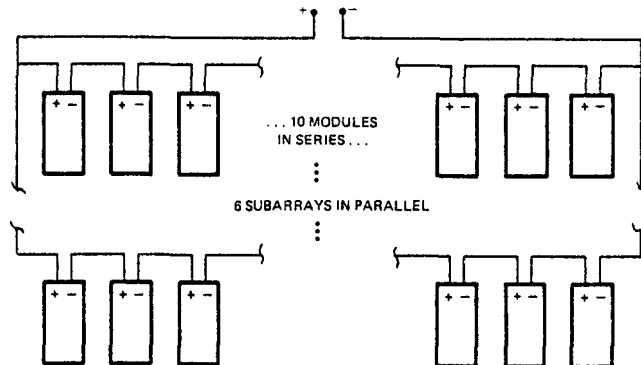


ARRAY SPECIFICATIONS

AT RATED CONDITIONS: INSOLATION = 1000 WATTS/m²; T_{CELL} = 25°C
MODULE: 40 SERIES x 4 PARALLEL P-SI CELLS
 POWER = 20 VOLTS x 7.8 AMP = 156 WATTS
SUBARRAY: 10 MODULES IN SERIES
 SUBARRAY POWER = 1560 WATTS
ARRAY: 3 SUBARRAYS IN PARALLEL
 D.C. POWER = 4.68 kW
 A.C. POWER = 4.10 kW

8 kW ... POLYCRYSTALLINE SILICON ... 20 VOLT MODULE

RESIDENTIAL ARRAY SCHEMATIC



ARRAY SPECIFICATIONS

AT RATED CONDITIONS: INSOLATION = 1000 WATTS/m²; T_{CELL} = 25°C
MODULE: 40 SERIES x 4 PARALLEL P-SI CELLS
 POWER = 20 VOLTS x 7.8 AMP = 156 WATTS
SUBARRAY: 10 MODULES IN SERIES
 SUBARRAY POWER = 1560 WATTS
ARRAY: 6 SUBARRAYS IN PARALLEL
 D.C. POWER = 9.36 kW
 A.C. POWER = 8.2 kW

Figure 3-8. SCHEMATICS AND SPECIFICATIONS FOR 4 kW and 8 kW POLYCRYSTALLINE SILICON ARRAYS

**Table 3-17 DESIGN CONSTRAINTS APPLIED TO
ALL CPS MODULE DESIGNS**

- Maximum Open Circuit Module Voltage at Low Temperature

$$V_{OCM}(\text{Max}) = 150\text{V} @ - 20^{\circ}\text{C}$$

- Maximum Module Peak Power Voltage

$$V_{MPM}(\text{Max}) = 100\text{V}$$

- Acceptable Module Peak Power Voltage

$$V_{MPM} = 50\text{V or } 100\text{V}$$

- Maximum Allowable Reverse Cell Voltage

$$V_{RMAX} = -6.7\text{V}$$

- Maximum Module Dimensions*

$$\text{Dim (Max)} = 47.5 \text{ in. X } 95.0 \text{ in. (120.65 cm x 241.3 cm)}$$

- Edge Spacing⁺

$$\Delta_{SE} = 3/8 \text{ in. (0.9525 cm)}$$

- Parallel Redundancy Desirable

- For cracked cells and broken interconnects
- Not for Cell Shadowing

- * Amorphous Silicon - 11.75 in. X 47.5 in. (29.85 cm x 120.65 cm)
- Ga As - 95.0 in. X 143.0 in. (241.3 cm x 363.22 cm)
- + Ga As - 1.0 in. (2.54 cm)

**Table 3-18. POLYCRYSTALLINE SILICON DESIGN
CONSTRAINTS FOR CPS MODULES**

- Maximum Cell Length in Series Direction (Ribbon Width)

$$L_{CS} = 6.0\text{cm}$$

- Maximum Cell Length in Parallel Direction

$$L_{CP} = 16.0\text{cm}$$

- Interior Spacing

$$\Delta_{SI} = 1/16 \text{ in. (0.159 cm)}$$

- Maximum Number of Cells in Bypass Group

$$N_{BPMAX} = 11 \text{ cells}$$

- Minimum Number of Cells or Strings in Parallel

$$N_{MMIN} = 3 \text{ for cracked cell or broken interconnect}$$

Table 3-19. POLYCRYSTALLINE SILICON CPS MODULE DESIGN

- Cell Dimensions
 - $L_{CS} \times L_{CP} = 2.28 \text{ in.} \times 6.23 \text{ in.} = 14.20 \text{ in.}^2$
 $5.78 \text{ cm} \times 15.82 \text{ cm} = 91.4 \text{ cm}^2$
- Bypass Group and Parallel Redundancy
 - $N_{BP} = 10 \text{ cells}$
 - $N_M = 3 \text{ strings}$
- Module Dimensions and Layout
 - $L_{MS} \times L_{MP} = 47.5 \text{ in.} \times 95.0 \text{ in.} (120.65 \text{ cm} \times 241.3 \text{ cm})$
 - 20 in. S-direction $\times$ 15 in. P-direction
 - Packing Factor = 0.943
- Module Electrical
 - 100 series $\times$ 3 parallel
 - $V_{OCM} = 60.0V$, $V_{MPM} = 50.0V$
 - $I_{SCM} = 6.86A$, $I_{MPM} = 6.31A$
 - $P_M = 315.5W$, $\eta_M = 10.84 \text{ percent}$

was specified as 10 cells with two bypass groups in the series direction. The bypass groups could then be snaked up and down five times to obtain the desirable peak power voltage of 50 V as illustrated in the polycrystalline CPS module diagrams in Figure 3-9. The module parallel length of 95.0 in. was sufficient to contain 15 cells with 5.82 cm parallel cell lengths; thus, each bypass group could be paralleled three times to satisfy the parallel redundancy constraints.

The module packing factor obtained is 0.943. The module electrical parameters are also listed in Table 3-19. The module efficiency, which is obtained by multiplying the cell efficiency of 11.5 percent by the packing factor, is 10.84 percent.

3.2.3.2 CPS System Design

Following the system design methodology discussed in section 3.1.3.2, the voltage and power of the module as a function of expected cell temperatures are presented in Table 3-20, using voltage variation with temperature of $-0.0022\text{V}/^{\circ}\text{C}$ and current variation with temperature of $0.0014\text{ A}/^{\circ}\text{C}$. The increase in cell temperature above ambient due to insolation is 25°C .

Table 3-21 lists the DC voltage variations with temperature for series string options of 19, 20, and 21 modules, respectively. The 20-module option matches the nominal system voltage constraint of 1000 V at 25°C . The voltage variations for the 20-module option also satisfy the voltage window constraint of 800 to 1300 V DC. The AC power variations with temperature are presented in Table 3-22. The 20-module string produces an AC power of 5531 W at 25°C . This option can be paralleled 362 times to obtain the minimum subarray AC power of 2.0 MW.

In Figure 3-10, the 50-MW polycrystalline silicon CPS array is shown to consist of 25 subarrays of 2 MW each connected in parallel. Each 2MW subarray consists of 20 modules connected in series to obtain a nominal 1,000 V and 362 series strings connected in parallel to produce 2.28 MW of DC power. With the power conditioning component efficiency of 0.8765, the AC power thus produced is 2.00 MW.

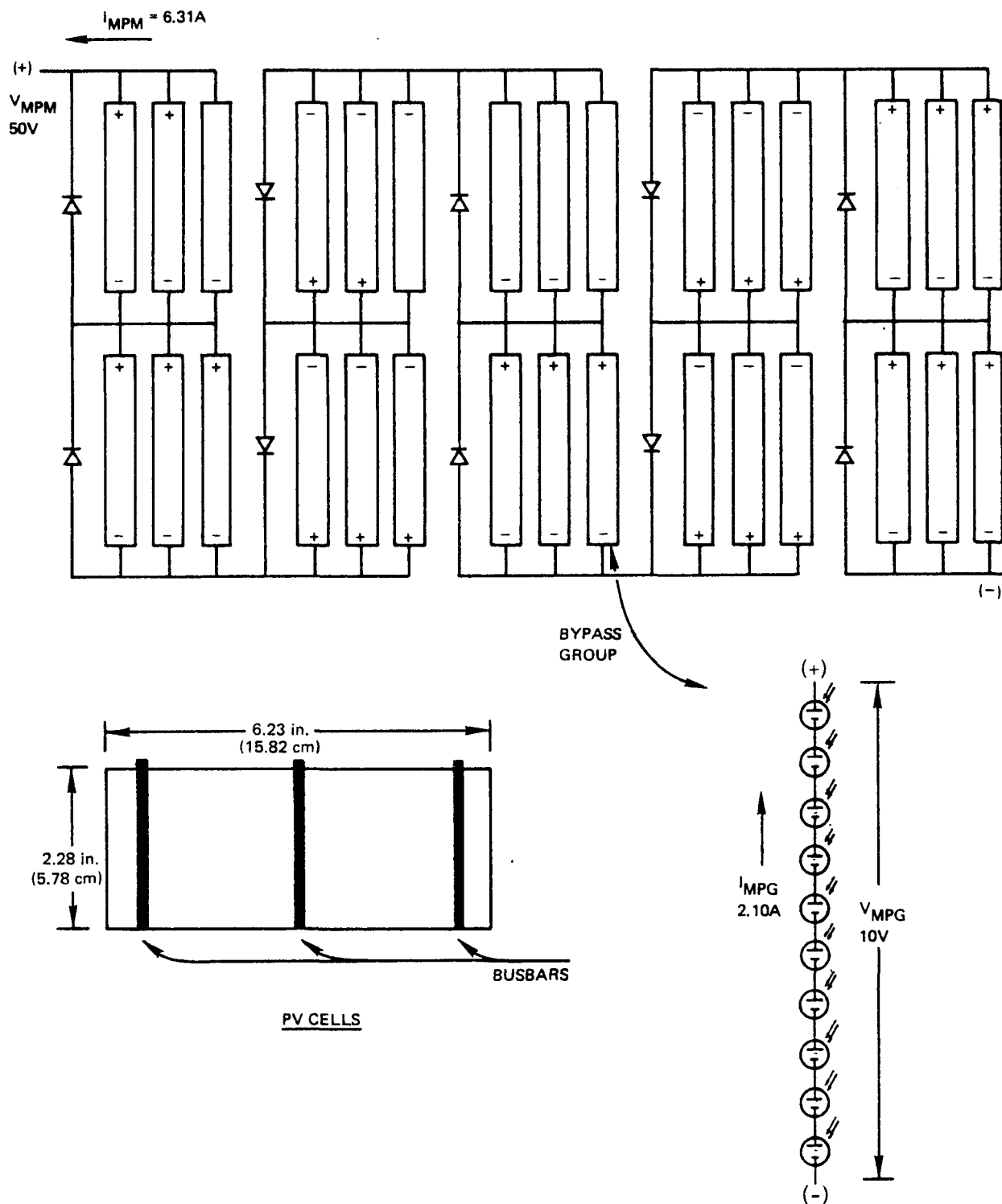


Figure 3-9. POLYCRYSTALLINE SILICON CPS MODULE

Table 3-20. POLYCRYSTALLINE SILICON CPS MODULE DATA

 MODULE ANALYSIS WORK SHEET...P-SI...50 VOLT CENTRAL POWER STATION

VOC DELTA -.0022
 W/T--U/C
 VMAX DELT -.0022
 W/T--U/C
 ISC DELTA .0014
 W/T--A/C
 IMAX DELT .0014
 W/T--A/C
 NO OF CEL 100
 IN SERIES
 NO OF CEL 3
 IN //
 TCELL-TAM 25
 AT 1 SUN

CONDITION	TAMB DEG-C	TCELL DEG-C	VOC VOLTS	ISC AMPS	VMAX VOLTS	IMAX AMPS	PMAX WATTS
LOW TEMP	-10	15	62.2	6.818	52.2	6.268	327.1896
RATED CON	0	25	60	6.86	50	6.31	315.5
S.O.C. NOCT/1000	20	45	55.6	6.944	45.6	6.394	291.5664
T=30C/86F	30	55	53.4	6.986	43.4	6.436	279.3224
T=40/104F	40	65	51.2	7.028	41.2	6.478	266.8936
T=50/122F	50	75	49	7.07	39	6.52	254.28

Table 3-21. POLYCRYSTALLINE SILICON CPS STRING DC VOLTAGE WINDOW

PV STRING VOLTAGE							
* TEMP AMB CELL	NO MODS= 19		NO MODS= 20		NO MODS= 21		
	UMAX	VOC	UMAX	VOC	UMAX	VOC	
TAMB -10 TCELL 15	991.8	1181.8	1044	1244	1096.2	1306.2	
0 25	950	1140	1000	1200	1050	1260	
20 45	866.4	1056.4	912	1112	957.6	1167.6	
30 55	824.6	1014.6	868	1068	911.4	1121.4	
40 65	782.8	972.8	824	1024	865.2	1075.2	
50 75	741	931	780	980	819	1029	

*TEMPERATURE IS IN °C

Table 3-22. POLYCRYSTALLINE SILICON CPS STRING AC POWER OUTPUT WITH PARASITIC LOSSES

* PU STRING POWER... $POW = PMOD * NMOD * NALL$			

NMIS=	.98	MISMATCH	
NWIR=	.98	WIRE LOSS	
NPPT=	.995	PK POW TR	
NBDID=	.997	BLK DIODE	
NPCS=	.92	POW COND	
NALL=	.8765127	OVERALL	

TEMP	NO MODS=	NO MODS=	NO MODS=
AMB	19	20	21
CELL			

TAMB	-10 5448.931	5735.717	6022.503
TCELL	15		

	0 5254.255	5530.795	5807.335
	25		

	20 4855.671	5111.233	5386.795
	45		

	30 4651.763	4896.593	5141.422
	55		

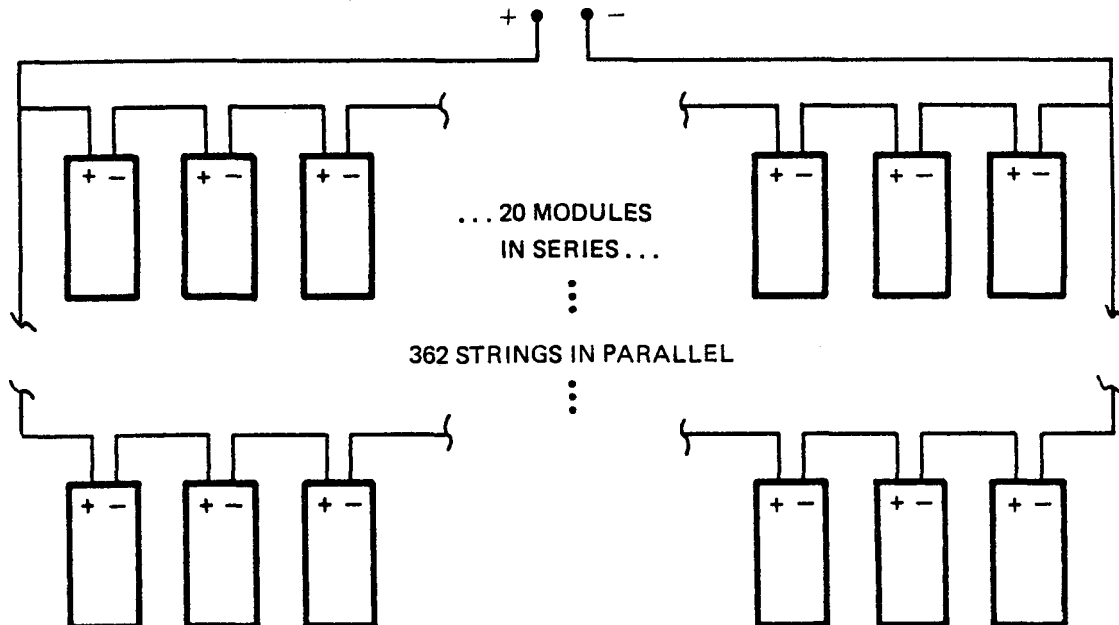
	40 4444.777	4678.713	4912.648
	65		

	50 4234.713	4457.593	4680.473
	75		

*POWER IS IN WATTS

50 MW ... POLYCRYSTALLINE SILICON ... 50 VOLT MODULE

CENTRAL POWER STATION 2 MW SUBARRAY SCHEMATIC



ARRAY SPECIFICATIONS

AT RATED CONDITIONS: INSOLATION = 1000 WATTS/m²; T_{CELL} = 25°C

MODULE: 100 SERIES x 3 PARALLEL P-SI CELLS

POWER = 50 VOLTS x 6.31 AMP = 315.5 WATTS

STRING: 20 MODULES IN SERIES

STRING POWER = 6.31 kW

SUBARRAY: 362 STRINGS IN PARALLEL

D.C. POWER = 2.28 MW

A.C. POWER = 2.00 MW

CENTRAL POWER STATION ARRAY: 25 SUBARRAYS IN PARALLEL

A.C. POWER = 50 MW

Figure 3-10. SCHEMATIC AND SPECIFICATIONS FOR 50 MW P-SI CPS ARRAY

3.3 AMORPHOUS SILICON CONCEPTUAL DESIGNS

The amorphous silicon system designs were developed using the design approach previously discussed in section 3.1 based on the module and system design methodologies discussed in section 3.1.3.

3.3.1 Cell Parameters

The amorphous silicon residential and CPS designs are both based on the deposition process used by RCA, which produces integrated, series-connected cells on a glass superstrate [5]. An IV curve obtained from SERI files [22] is shown as the lower curve in Figure 3-11. This curve represents a cell efficiency of 6.12 percent. Since the goal for amorphous silicon is 10 percent, the upper curve was postulated. It contains higher short-circuit current, fill factor, and open-circuit voltage. The curve is consistent with expected upper limits for amorphous silicon [34]. By normalizing this curve for a 1 cm^2 cell, the parameters in Table 3-23 were obtained.

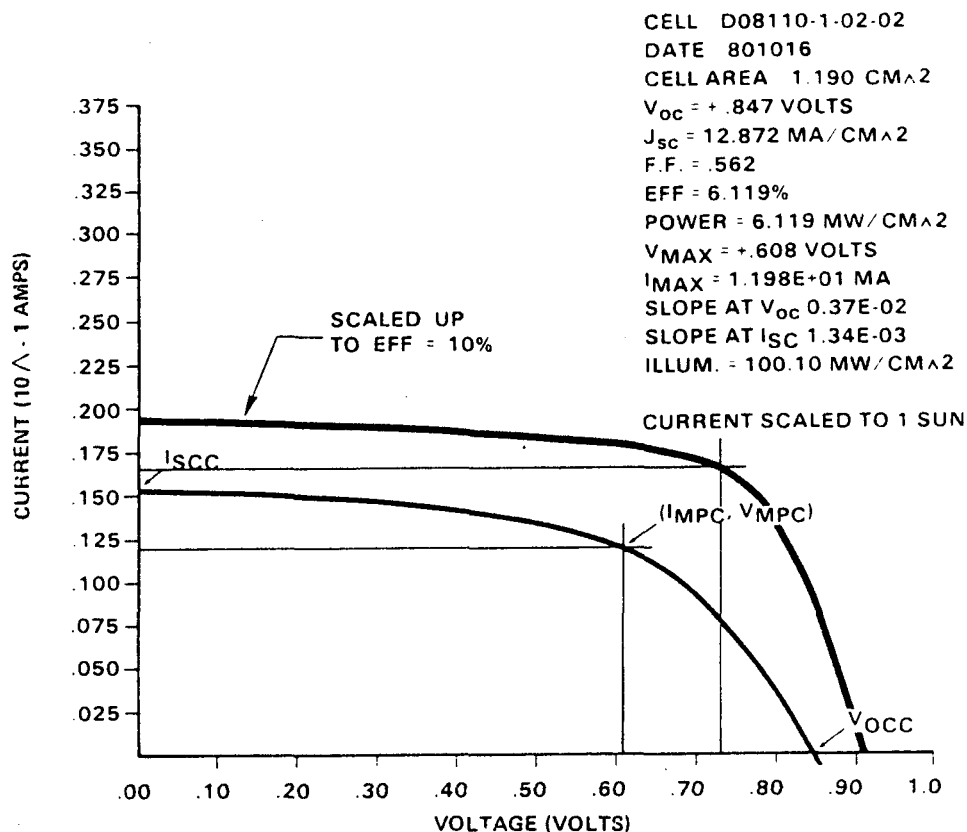


Figure 3-11. AMORPHOUS SILICON CELL I-V CURVE

The voltage at peak power is 0.73 V and the current density at peak power is 13.7 mA/cm². The voltage variation with temperature was obtained from telephone communication with RCA [35]. The current variation with temperature is expressed as a fractional variation, and would be multiplied by the actual cell current to determine the current variation with temperature. The value is the same as that used for polycrystalline silicon, since no other data were available. The technology is resistance-limited by the transparent conducting oxide (TCO), which is deposited between the glass and the cell, and must carry the current generated by the cell. The sheet resistivity of the TCO is 1.0 Ω /SQ based on expected future improvements [17].

Table 3-23. AMORPHOUS SILICON CELL PARAMETERS

V_{OCC}	= 0.91V
V_{MPC}	= 0.73V
J_{SCC}	= 16mA/cm ²
J_{MPC}	= 13.7mA/cm ²
FF	= 0.687
P_C	= 10mW/cm ²
η_C	= 10.0 percent
$\Delta V/\Delta T$	= -1.6mV/ ^o C
$\Delta f_I/\Delta T$	= 0.00061/ ^o C
$R_{\square TCO}$	= 1.0 Ω / $\square$

3.3.2 Amorphous Silicon Residential Designs

3.3.2.1 Residential Module Designs

The design constraints which apply to all residential module designs were discussed in section 3.1.2 and are reproduced here in Table 3-24 for the reader's convenience. Table 3-25 presents the module design constraints which apply specifically to amorphous silicon residential modules. The module dimensions of 1 ft. x 4 ft. were considered to be the approximate limits of the deposition technology.

Table 3-24. DESIGN CONSTRAINTS APPLIED TO
ALL RESIDENTIAL MODULE DESIGNS

- Maximum Open Circuit Module Voltage at Low Temperature

$$V_{OCM}^{(Max)} = 30V @ - 20^{\circ} C$$

- Maximum Module Peak Power Voltage

$$V_{MPM}^{(Max)} = 20V$$

- Acceptable Module Peak Power Voltages

$$V_{MPM} = 5, 7.5, 10, 15, \text{ or } 20V$$

- Maximum Allowable Reverse Cell Voltage

$$V_{RMAX} = -6.7V$$

- Maximum Module Dimensions*

$$Dim (Max) = 47.5 \text{ in. X } 47.5 \text{ in. (120.65 cm)}$$

- Edge Spacing

$$\Delta_{SE} = 3/8 \text{ in. (0.9525 cm)}$$

- Parallel Redundancy Desirable

Prevents bypass activation due to single cell shadowing,
single interconnect breaking or single cell cracking.

* Amorphous Silicon - 11.75 in. X 47.5 in. (29.85 cm x 120.65 cm)
Ga As - 23.5 in. X 47.5 in. (59.69 cm x 120.65 cm)

**Table 3-25. AMORPHOUS SILICON DESIGN CONSTRAINTS
FOR RESIDENTIAL MODULES**

- Maximum Module Dimensions

$$\text{Dim (Max)} = 11.75 \text{ in.} \times 47.5 \text{ in.} \text{ (29.85 cm} \times \text{120.65 cm)}$$

- Maximum Cell Area

$$A_{\text{CMAX}} = 25.0 \text{ cm}^2$$

- Power Loss in TCO

$$f_{\text{TCO}} = P_{\text{TCO}}/P_{\text{C}} = 0.05 \rightarrow L_{\text{CSMAX}} = 0.953 \text{ in.} \text{ (2.42 cm)}$$

- Interior Spacing

- between positive ends of series strings in parallel = 1/4 in. (0.635 cm)

- between negative ends of series strings in parallel = 1/8 in. (0.3175 cm)

- between positive and negative ends of series strings in series =
3/16 in. (0.476 cm)

- between cells in parallel direction = 1/32 in. (0.0794 cm)

- Maximum Number of Cells in Bypass Group

$$N_{\text{BPMAX}} = 7 \text{ cells}$$

- Minimum Number of Cells or Strings in Parallel

$$N_{\text{MMIN}} = 7$$

The maximum cell length in the series direction is determined in the Module Optimization Methodology from a maximum acceptable power loss in the TCO (f_{TCO}) of 5 percent. The equation used in the calculation was:

$$L_{CSMAX} = \sqrt{\frac{3f_{TCO} V_{OCC} FF}{R_{\square} J_{SCC}}} \quad \text{Eq. (3-3)}$$

The interior spacings between cells are consistent with the spacings required for stand-off and metallization for this process. The maximum number of cells in a bypass group was determined from the maximum allowable reverse cell voltage of -6.7 V, which was previously specified in Table 3-24. The equation used to obtain N_{BPMAX} is:

$$N_{BPMAX} = 1 - \frac{V_{RMAX} + V_{FD}}{V_{OCC}} \quad \text{Eq. (3-1)}$$

where V_{FD} = forward voltage of bypass diode. The parallel redundancy constraint of seven cells or strings in parallel was obtained from the relationship between the cell short circuit current and peak power current by the equation

$$N_{MMIN} = \frac{J_{SCC}}{J_{SCC} - J_{MPC}} \quad \text{Eq. (3-4)}$$

Using the module optimization methodology discussed in section 3.1.3.1 with design option 4 to produce a module with fixed dimensions, the amorphous silicon residential module design characteristics listed in Table 3-26 were obtained. The cell series length of 0.77 in. is slightly less than the maximum cell series length of 0.953 in. The cell area of 23.1 cm² is slightly less than the maximum cell area of 25 cm². Using the cell series length of 0.77 in., 14 cells can fit exactly in the 11.75 in. module dimension; therefore, N_{BPMAX} was specified as seven cells and two bypass groups fit exactly in the module dimension.

As illustrated in the amorphous silicon residential module diagrams in Figure 3-12, the maximum allowable module voltage of 20 V was not obtained. Rather, the two bypass groups were paralleled ten times to satisfy the parallel redundancy constraints and allow location of both positive and negative terminals on the same end of the module, thus requiring only one junction box. The parallel length of the module was then capable of accepting 10 strings in parallel for each bypass group. Thus, 14 cells are arranged in a series direction in the module while 10 cells are arranged in the parallel direction in the module.

Table 3-26. AMORPHOUS SILICON RESIDENTIAL MODULE DESIGN

- Cell Dimension

- $L_{CS} \times L_{CP} = 0.77 \text{ in.} \times 4.65 \text{ in.} = 3.58 \text{ in.}^2 = 23.1 \text{ cm}^2$

- Bypass Group and Parallel Redundancy

- $N_{BP} = 7 \text{ cells}$

- $N_M = 10 \text{ strings}$

- Module Dimensions and Layout

- $L_{MS} \times L_{MP} = 11.75 \text{ in.} \times 47.5 \text{ in.} (29.85 \text{ cm} \times 120.65 \text{ cm})$

- 14 cells in Series X 10 Parallel

- Packing Factor = 0.90

- Module Electrical

- $V_{OCM} = 12.74V$, $V_{MPM} = 10.22V$

- $I_{SCM} = 3.70A$, $I_{MPM} = 3.17A$

- $P_M = 32.42W$, $\eta_M = 9.0 \text{ percent}$

The packing factor obtained for the module is 0.90. The module electrical parameters are also listed in Table 3-26. The overall module efficiency which is obtained by multiplying the cell efficiency of 10 percent by the packing factor, is 9.0 percent.

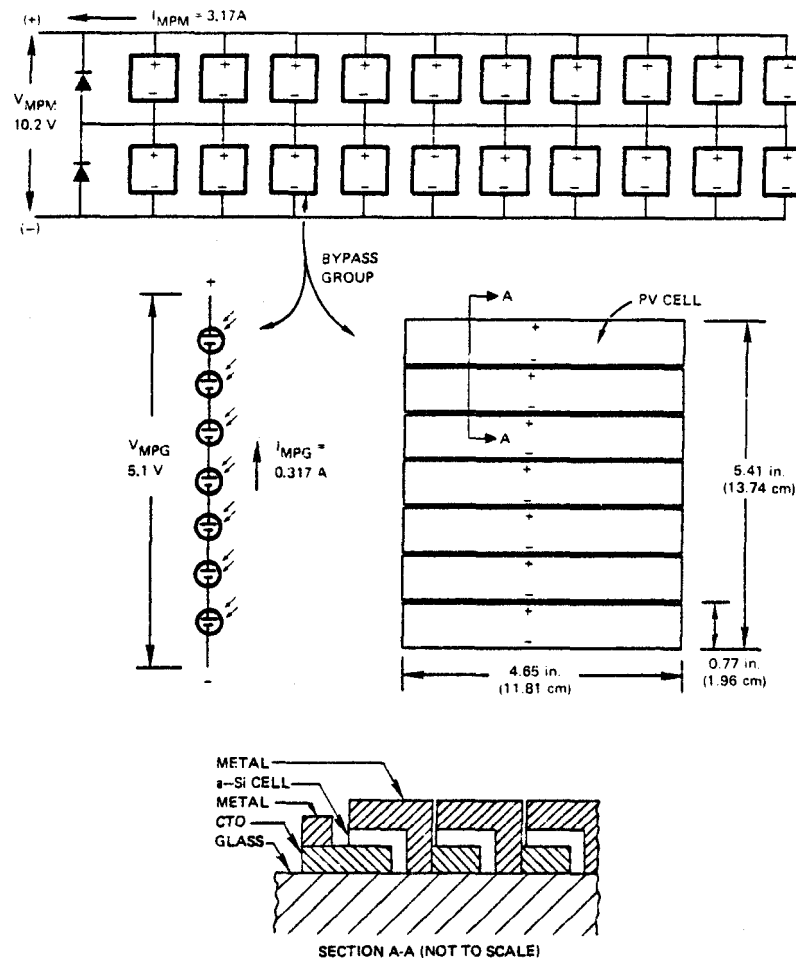


Figure 3-12. AMORPHOUS SILICON RESIDENTIAL MODULE

3.3.2.2 Residential System Designs

Following the system design methodology discussed in section 3.1.3.2, module voltage and power were determined at various cell temperatures characteristic of typical operations. The results are shown in Table 3-27, using $-0.0016\text{V}/^{\circ}\text{C}$ and $.00023\text{ A}/^{\circ}\text{C}$ as the voltage and current variations with temperature. The increase in cell temperature above ambient due to insolation is shown in the table as 25°C .

Based on the residential module data as a function of the temperature window, the DC voltages shown in Table 3-28 were obtained for the series string options of 19, 20, and 21 modules, respectively. At rated conditions of 25°C cell temperature, the 20-module option produces a voltage at peak power of 204 V and an open circuit voltage of 225 V. This option also produces an acceptable peak power voltage variation with temperature.

Table 3-27. AMORPHOUS SILICON RESIDENTIAL MODULE DATA

MODULE ANALYSIS WORK SHEET....A-SI..TEN VOLT RESIDENTIAL

VOC DELTA -.0016
 W/T--V/C
 VMAX DELT -.0016
 W/T--V/C
 ISC DELTA .00023
 W/T--A/C
 IMAX DELT .00023
 W/T--A/C
 NO OF CEL 14
 IN SERIES
 NO OF CEL 10
 IN //
 TCELL-TAM 25
 AT 1 SUN

CONDITION	TAMB DEG-C	TCELL DEG-C	VOC VOLTS	ISC AMPS	VMAX VOLTS	IMAX AMPS	PMAX WATTS
LOW TEMP	-10	15	12.964	3.677	10.444	3.147	32.86727
RATED CON	0	25	12.74	3.7	10.22	3.17	32.3974
S.O.C. NOCT/1000	20	45	12.292	3.746	9.772	3.216	31.42675
T=30C/86F	30	55	12.068	3.769	9.548	3.239	30.92597
T=40/104F	40	65	11.844	3.792	9.324	3.262	30.41489
T=50/122F	50	75	11.62	3.815	9.1	3.285	29.8935

Table 3-28. AMORPHOUS SILICON RESIDENTIAL SUBARRAY DC VOLTAGE WINDOW

PV STRING VOLTAGE							
*TEMP AMB CELL	NO MODS= 19		NO MODS= 20		NO MODS= 21		
	UMAX	VOC	UMAX	VOC	UMAX	VOC	
TAMB -10 TCELL 15	198.436	246.316	208.88	259.28	219.324	272.244	
0 25	194.18	242.06	204.4	254.8	214.62	267.54	
20 45	185.668	233.548	195.44	245.84	205.212	258.132	
30 55	181.412	229.292	190.96	241.36	200.508	253.428	
40 65	177.156	225.036	186.48	236.88	195.804	248.724	
50 75	172.9	220.78	182	232.4	191.1	244.02	

*TEMPERATURE IS IN °C

The AC power window for each of the series string options is shown in Table 3-29. The powers were obtained by multiplying the DC power of the series string by the overall power conditioning efficiency of 0.8765. It can be seen that the 20-module option produces a power at 25°C which is approximately one-seventh of 4 kW, the minimum AC power constraint for the residential system. Thus, seven of these strings could be paralleled to obtain the 4 kW residential system and 14 strings could be paralleled to obtain the 8 kW system.

The 4 kW and 8 kW amorphous silicon residential array schematics are illustrated in Figure 3-13. Twenty modules are connected in series to approximate the nominal 200 V desired. In one case, seven subarrays are connected in parallel to obtain a DC power of 4.54 kW. The AC power is then 3.98 kW. For the other case, 14 subarrays are connected in parallel to obtain a DC power of 9.07 kW. The AC power is then 7.95 kW.

3.3.3 Amorphous Silicon CPS Designs

3.3.3.1 CPS Module Design

The design constraints which apply to all CPS module designs were previously discussed in section 3.1.2 and are repeated here in Table 3-30 for the reader's convenience. Table 3-31 lists the CPS module constraints which apply specifically to the amorphous silicon technology. These constraints are the same as those previously discussed for the amorphous silicon residential modules.

Using the module optimization methodology discussed in section 3.1.3.1, the CPS module characteristics presented in Table 3-32 were obtained. Design option 4 was used to produce the module with the fixed dimensions of 11.75 in. x 47.5 in. The series and parallel lengths of the cells are 0.644 in. x 5.48 in., respectively. With the cell series length of 0.644 in., 70 cells could be placed in the module dimension of 47.5 in.; thus, the bypass group was specified as 7 cells with ten bypass groups in the series direction to approximate the desirable peak power voltage of 50 V as illustrated in the amorphous silicon CPS module diagrams in Figure 3-14. The module parallel length of 11.75 in. was sufficient to contain only 2 cells with 5.48 in. parallel cell lengths; thus, the parallel redundancy constraint could not be satisfied. This indicates that high voltage modules cannot be satisfactorily designed with small areas (4 ft.²). For this amorphous silicon technology, the area must be 3.5 times larger to satisfy all constraints at 50V. If the cell could be made with two across-the-cell interconnects, however, the parallel redundancy constraints would be satisfied by this design.

The module packing factor obtained is 0.886. The module efficiency which is obtained by multiplying the cell efficiency of 10.0 percent by the packing factor, is 8.86 percent.

Table 3-29. AMORPHOUS SILICON RESIDENTIAL SUBARRAY AC POWER OUTPUT WITH PARASITIC LOSS

* PV STRING POWER... $POW=PMOD*NMOD*NALL$

NMIS= .98MISMATCH
 NWIR= .98WIRE LOSS
 NPPT= .995PK POW TR
 NBDIO= .997BLK DIODE
 NPCO= .92POW COND
 NALL= .8765127OVERALL

	TEMP NO MODS=	NO MODS=	NO MODS=
	AMB 19	20	21
CELL			
TAMB -10	547.3630	576.1716	604.9801
TCELL 15			
0	539.5379	567.9347	596.3314
25			
20	523.3730	550.9190	578.4649
45			
30	515.0331	542.1402	569.2472
55			
40	506.5217	533.1807	559.8398
65			
50	497.8386	524.0407	550.2427
75			

*POWER IS IN WATTS

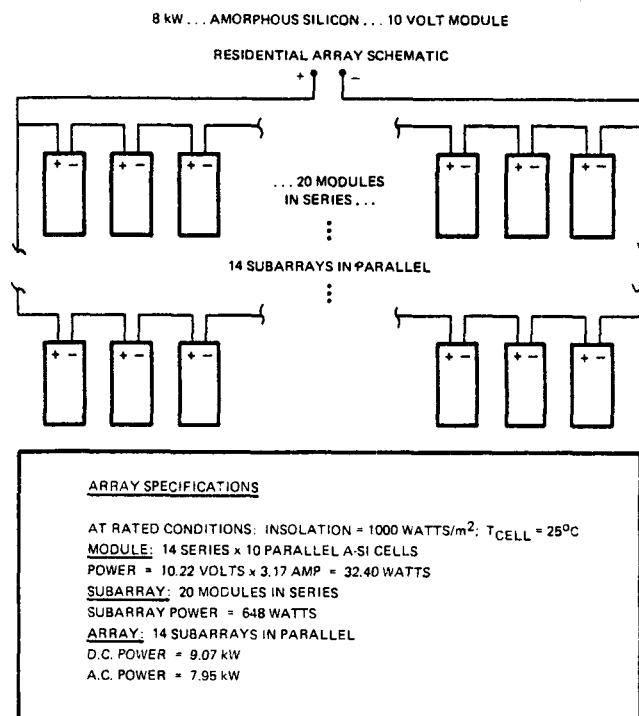
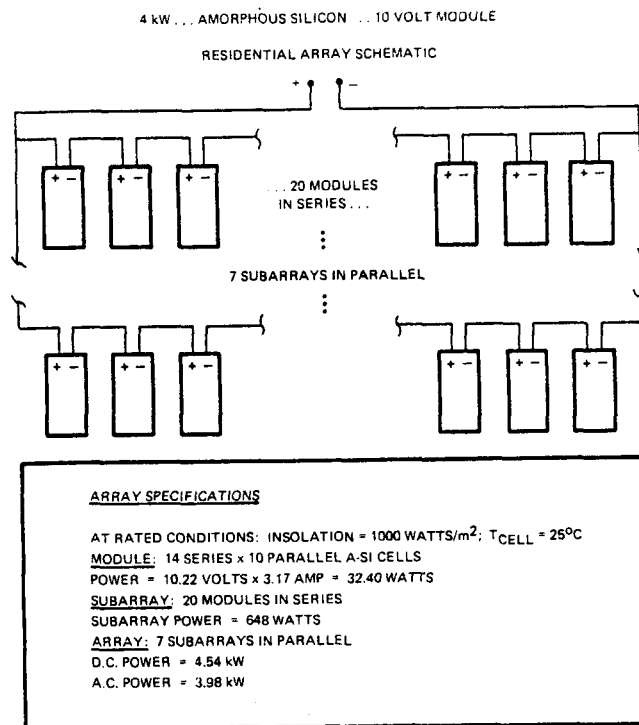


Figure 3-13. SCHEMATICS AND SPECIFICATIONS FOR 4 kW and 8 kW AMORPHOUS SILICON ARRAYS

**Table 3-30. DESIGN CONSTRAINTS APPLIED TO
ALL CPS MODULE DESIGNS**

- Maximum Open Circuit Module Voltage at Low Temperature

$$V_{OCM}(\text{Max}) = 150V @ - 20^{\circ}C$$

- Maximum Module Peak Power Voltage

$$V_{MPM}(\text{Max}) = 100V$$

- Acceptable Module Peak Power Voltage

$$V_{MPM} = 50V \text{ or } 100V$$

- Maximum Allowable Reverse Cell Voltage

$$V_{RMAX} = -6.7V$$

- Maximum Module Dimensions*

$$\text{Dim (Max)} = 47.5 \text{ in X } 95.0 \text{ in (120.65 cm x 241.3 cm)}$$

- Edge Spacing⁺

$$\Delta_{SE} = 3/8 \text{ in (0.9525 cm)}$$

- Parallel Redundancy Desirable

- For cracked cells and broken interconnects
- Not for Cell Shadowing

- * Amorphous Silicon - 11.75 in X 47.5 in (29.85 cm x 120.65 cm)
- Ga As - 95.0 in X 143.0 in (241.3 cm x 363.2 cm)
- + Ga As - 1.0 in (2.54 cm)

Table 3-31. AMORPHOUS SILICON DESIGN CONSTRAINTS
FOR CPS MODULES

- Maximum Module Dimensions

$$\text{Dim (Max)} = 11.75 \text{ in} \times 47.5 \text{ in} \text{ (29.85 cm} \times \text{120.65 cm)}$$

- Maximum Cell Area

$$A_{\text{CMAX}} = 25.0 \text{ cm}^2$$

- Power Loss in TCO

$$f_{\text{TCO}} = P_{\text{TCO}}/P_{\text{C}} = 0.05 \Rightarrow L_{\text{CSMAX}} = 0.953 \text{ in} \text{ (2.42 cm)}$$

- Interior Spacing

- between positive ends of series strings in parallel = 1/4 in (0.635 cm)

- between negative ends of series strings in parallel = 1/8 in (0.3175 cm)

- between positive and negative ends of series strings in series = 3/16 in (0.476 cm)

- between cells in parallel direction = 1/32 in (0.0794 cm)

- Maximum Number of Cells in Bypass Group

$$N_{\text{BPMAX}} = 7 \text{ cells}$$

- Minimum Number of Cells or Strings in Parallel

$$N_{\text{MMIN}} = 7$$

Table 3-32. AMORPHOUS SILICON CPS MODULE DESIGN

- Cell Dimension

- $L_{CS} \times L_{CP} = 0.644 \text{ in} \times 5.48 \text{ in} = 3.53 \text{ in}^2 (22.77 \text{ cm}^2)$

- Bypass Group and Parallel Redundancy

- $N_{BP} = 7 \text{ cells}$

- $N_M = 2 \text{ strings (Parallel Redundancy not satisfied)}$

- Module Dimensions and Layout

- $L_{MS} \times L_{MP} = 11.75 \text{ in} \times 47.5 \text{ in} (29.85 \text{ cm} \times 120.65 \text{ cm})$

- 70 cells in Series X 2 Parallel

- Packing Factor = 0.886

- Module Electrical

- $V_{OCM} = 63.7V$, $V_{MPM} = 51.1V$

- $I_{SCM} = 0.729A$, $I_{MPM} = 0.624A$

- $P_M = 31.89W$, $\eta_M = 8.86 \text{ percent}$

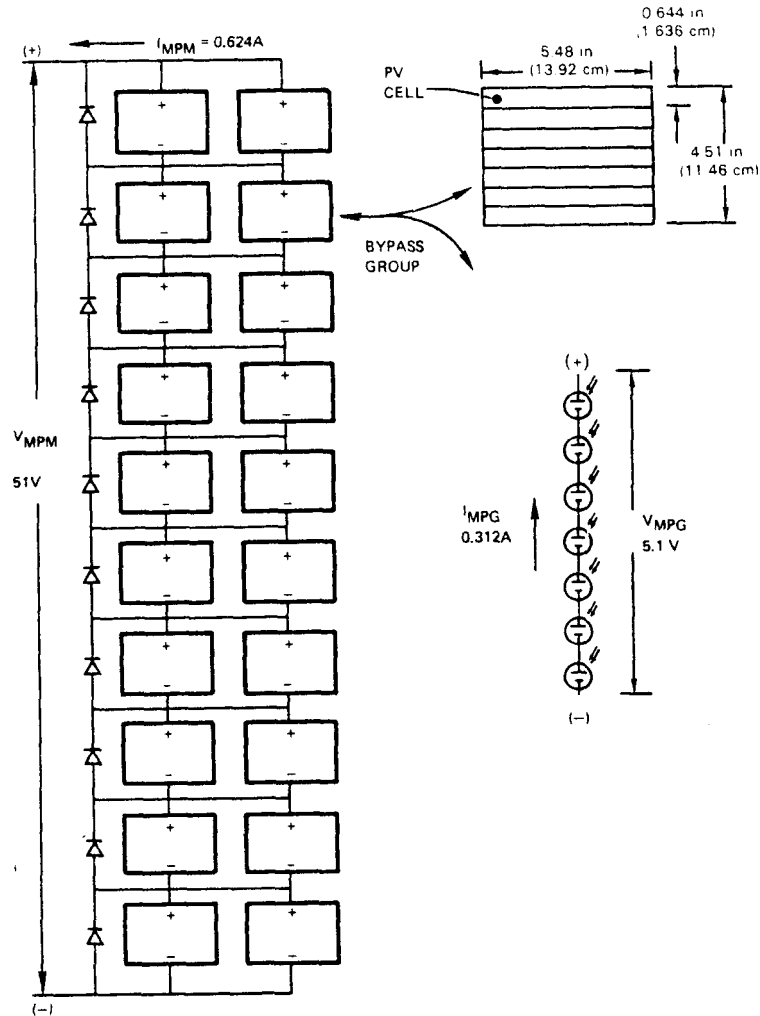


Figure 3-14. AMORPHOUS SILICON CPS MODULE

3.3.3.2 CPS System Design

Following the system design methodology discussed in section 3.1.3.2, the voltage and power of the module as a function of expected cell temperatures are presented in Table 3-33, using voltage variation with temperature of $-.0016 \text{ V}/^\circ\text{C}$ and current variation with temperature of $.00022 \text{ A}/^\circ\text{C}$. The increase in cell temperature above ambient due to insolation is 25°C .

Table 3-34 lists the DC voltage variations with temperature for series string options of 19, 20, and 21 modules, respectively. The 20-module option approximates the nominal system voltage constraint of 1000 V at 25°C . The voltage variations for the 20-module option also satisfy the voltage window constraint of 800 to 1300 V DC. The AC power variations with temperature are presented in Table 3-35. The 20-module string produces an AC power of 558 W at 25°C . This option can be paralleled 3585 times to obtain the minimum subarray AC power of 2.0 MW.

In Figure 3-15, the 50 MW amorphous silicon CPS array is shown to consist of 25 subarrays of 2 MW each connected in parallel. Each 2 MW subarray consists

Table 3-33. AMORPHOUS SILICON CPS MODULE DATA

 MODULE ANALYSIS WORK SHEET....A-SI..51 VOLT CENTRAL POWER STATION

VOC DELTA -.0016
 W/T--U/C
 UMAX DELT -.0016
 W/T--U/C
 ISC DELTA .00022
 W/T--A/C
 IMAX DELT .00022
 W/T--A/C
 NO OF CEL 70
 IN SERIES
 NO OF CEL 2
 IN //
 TCELL-TAM 25
 AT 1 SUN

CONDITION	TAMB DEG-C	TCELL DEG-C	VOC VOLTS	ISC AMPS	UMAX VOLTS	IMAX AMPS	PMAX WATTS
LOW TEMP	-10	15	64.82	.7246	52.12	.6196	32.29355
RATED CON	0	25	63.7	.729	51	.624	31.824
S.O.C. NOCT/1000	20	45	61.46	.7378	48.76	.6328	30.85533
T=30C/86F	30	55	60.34	.7422	47.64	.6372	30.35621
T=40/104F	40	65	59.22	.7466	46.52	.6416	29.84723
T=50/122F	50	75	58.1	.751	45.4	.646	29.3284

Table 3-34. AMORPHOUS SILICON CPS STRING DC VOLTAGE WINDOW

PV STRING VOLTAGE							
* TEMP AMP CELL		NO MODS= 19		NO MODS= 20		NO MODS= 21	
		VMAX	VOC	VMAX	VOC	VMAX	VOC
TAMB	-10	990.28	1231.58	1042.4	1296.4	1094.52	1361.22
TCELL	15						
	0	969	1210.3	1020	1274	1071	1337.7
	25						
	20	926.44	1167.74	975.2	1229.2	1023.96	1290.66
	45						
	30	905.16	1146.46	952.8	1206.8	1000.44	1267.14
	55						
	40	883.88	1125.18	930.4	1184.4	976.92	1243.62
	65						
	50	862.6	1103.9	908	1162	953.4	1220.1
	75						

* TEMPERATURE IS IN °C

Table 3-35. AMORPHOUS SILICON CPS STRING AC POWER OUTPUT WITH PARASITIC LOSSES

* PV STRING POWER... $POW=PMOD*NMOD*NALL$

NMIS= .98MISMATCH
 NWIR= .98WIRE LOSS
 NPPT= .995PK POW TR
 NBDID= .997BLK DIODE
 NPCSC= .92POW COND
 NALL= .8765127OVERALL

	TEMP	NO MODS=	NO MODS=	NO MODS=
	AMB	19	20	21
	CELL			
TAMB	-10	537.8085	566.1142	594.4199
TCELL	15			
	0	529.9887	557.8828	585.7769
	25			
	20	513.8567	540.9017	567.9468
	45			
	30	505.5444	532.1520	558.7596
	55			
	40	497.0681	523.2296	549.3910
	65			
	50	488.4276	514.1343	539.8410
	75			

*POWER IS IN WATTS

of 20 modules connected in series to obtain a nominal 1000 V and 3585 series strings connected in parallel to produce 2.28 MW of DC power. With the power conditioning component efficiency of 0.8765, the AC power thus produced is 2.00 MW.

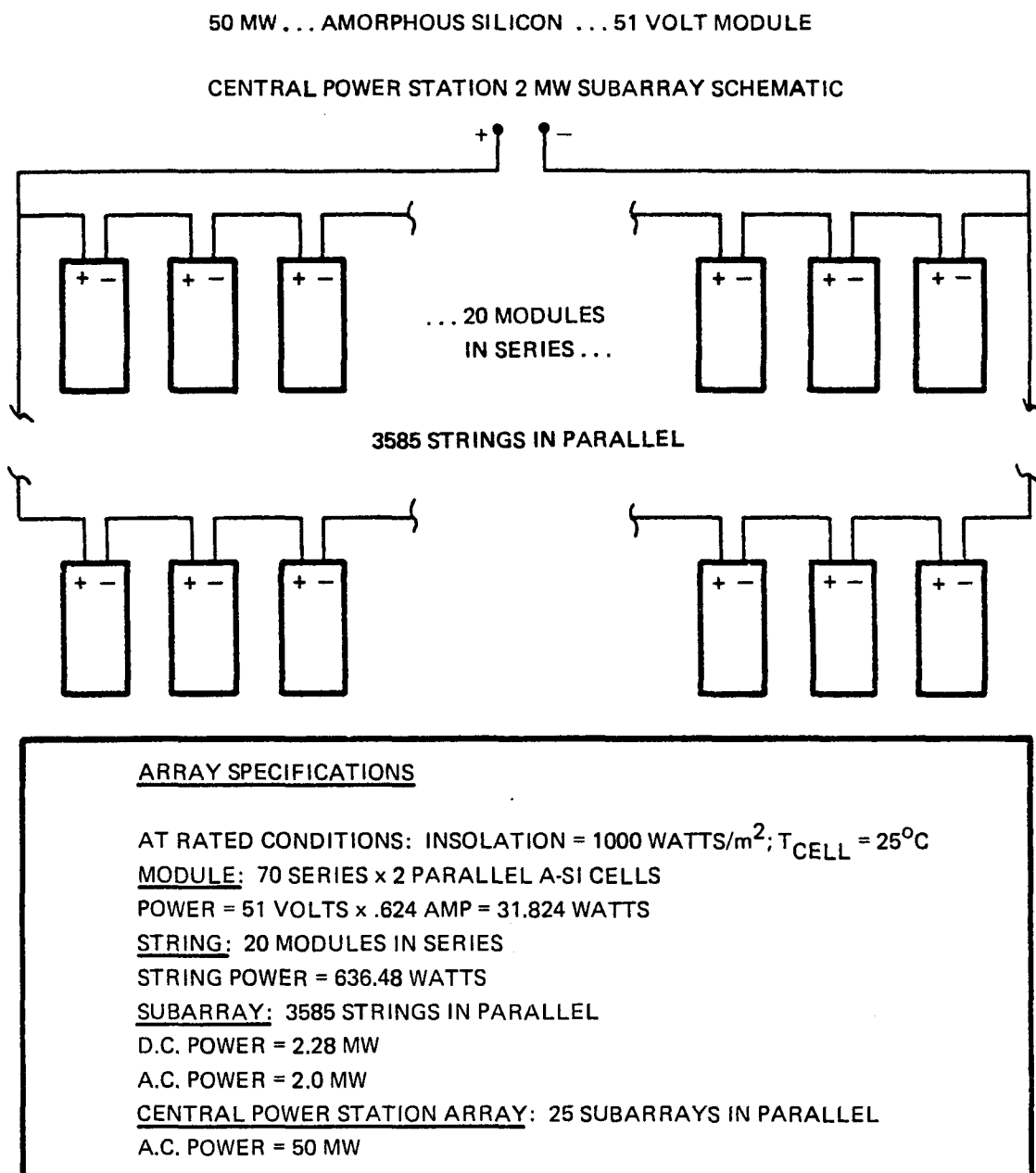


Figure 3-15. SCHEMATIC AND SPECIFICATIONS FOR 50 MW A-SI CPS ARRAY

3.4 CdS/CuInSe₂ CONCEPTUAL DESIGNS

The CdS/CuInSe₂ system designs were developed using the design approach previously discussed in section 3.1 based on the module and system design methodologies discussed in section 3.1.3.

3.4.1 Cell Parameters

The CdS/CuInSe₂ residential and CPS designs are both based on the technology developed by Boeing [6]. The process envisioned produces ribbons of cells on a flexible substrate [7]. The lower efficiency I-V curve seen in Figure 3-16 was reported at a SERI conference [23].

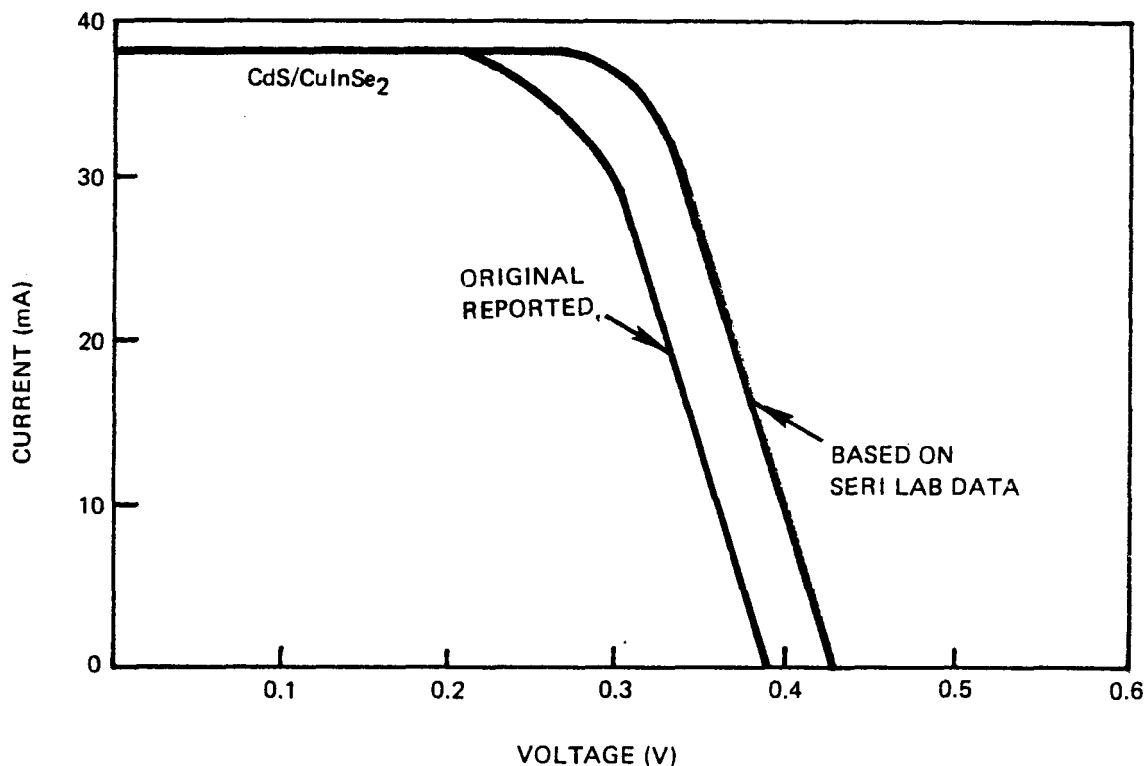


Figure 3-16. CdS/CuInSe₂ I-V CURVE

The higher efficiency curve was obtained from unpublished SERI laboratory data [16] and represents the best performance obtained to date on CdS/CuInSe₂ cells. Normalizing this curve for a one square centimeter cell, the parameters listed in Table 3-36 were obtained. The voltage at peak power is 0.3 V and the current density at peak power is 36 mA/cm². The voltage variation with temperature was obtained from unpublished data supplied by Boeing [36]. The current variation with temperature is expressed as a fractional variation

and would be multiplied by the actual cell current to determine the current variation with temperature. The value is the same as that used for polycrystalline silicon since no other data were available. The cell contains two across-the-cell interconnects to provide redundancy in the case of cracked cells or broken interconnects. These redundant interconnects are useful in reducing the number of parallel strings or cells required to satisfy parallel redundancy constraints.

Table 3-36. CdS/CuInSe₂ CELL PARAMETERS

V_{OCC}	= 0.424V
V_{MPC}	= 0.30V
J_{SCC}	= 39.0 mA/cm ²
J_{MPC}	= 36.0 mA/cm ²
FF	= 0.646
P_C	= 10.8 mW/cm ²
η_C	= 10.8 percent
$\Delta V/\Delta T$	= -2.0 mV/°C
$\Delta f_I/\Delta T$	= 0.00061/°C
N_{ACI}	= 2

3.4.2 CdS/CuInSe₂ Residential Designs

3.4.2.1 Residential Module Designs

The design constraints which apply to all residential module designs were discussed in section 3.1.2 and are reproduced here in Table 3-37 for the reader's convenience. Table 3-38 presents the module design constraints which apply specifically to CdS/CuInSe₂ residential modules. The maximum cell area of 8 in.² (~50 cm²) is felt to be a reasonable goal for this technology [7]. In order to obtain an approximately square cell, the maximum cell length in the series direction, which corresponds to the width of the ribbon, is specified as 2.5 in. The 1/16 in. interior spacing between cells is consistent with spacing requirements for cell assembly in modules in which

**Table 3-37. DESIGN CONSTRAINTS APPLIED TO
ALL RESIDENTIAL MODULE DESIGNS**

- Maximum Open Circuit Module Voltage at Low Temperature

$$V_{OCM}(\text{Max}) = 30\text{V @ } -20^{\circ}\text{C}$$

- Maximum Module Peak Power Voltage

$$V_{MPM}(\text{Max}) = 20\text{V}$$

- Acceptable Module Peak Power Voltages

$$V_{MPM} = 5, 7.5, 10, 15, \text{ or } 20\text{V}$$

- Maximum Allowable Reverse Cell Voltage

$$V_{RMAX} = -6.7\text{V}$$

- Maximum Module Dimensions*

$$\text{Dim (Max)} = 47.5 \text{ in. X } 47.5 \text{ in. (120.65 cm)}$$

- Edge Spacing

$$\Delta_{SE} = 3/8 \text{ in. (0.9525 cm)}$$

- Parallel Redundancy Desirable

Prevents bypass activation due to single cell shadowing,
single interconnect breaking or single cell cracking.

* Amorphous Silicon - 11.75 in. X 47.5 in. (29.85 cm x 120.65 cm)
Ga As - 23.5 in. X 47.5 in. (59.69 cm x 120.65 cm)

Table 3-38. CdS/CuInSe₂ DESIGN CONSTRAINTS FOR RESIDENTIAL MODULES

- Maximum Cell Length in Series Direction (Ribbon Width)

$$L_{\text{CSMAX}} = 2.5 \text{ in. (6.35 cm)}$$

- Maximum Cell Area

$$A_{\text{CMAX}} = 8 \text{ in.}^2 (51.6 \text{ cm}^2)$$

- Interior Spacing

$$\Delta_{\text{SI}} = 1/16 \text{ in. (0.159 cm)}$$

- Maximum Number of Cells in Bypass Group

$$N_{\text{BPMAX}} = 15 \text{ cells}$$

- Minimum Number of Cells or Strings in Parallel

$$N_{\text{MMIN}} = 4 \text{ for cracked cell or broken interconnect}$$

voltage differentials are within 50 V [33]. The maximum number of cells in a bypass group (15 cells) was determined from the maximum allowable reverse cell voltage of -6.7 V previously specified in Table 3-37. The equation used to obtain N_{BPMAX} is:

$$N_{BPMAX} = 1 - \frac{V_{RMAX} + V_{FD}}{V_{OCC}} \quad \text{Eq. (3-1)}$$

where V_{FD} = forward voltage of bypass diode. The parallel redundancy constraint of four cells or strings in parallel was obtained from the relationship between the cell short circuit current and peak power current and the number of across-the-cell interconnects by the equation

$$N_{MMIN} = \frac{J_{SCC}}{2N_{ACI} (J_{SCC} - J_{MPC})} \quad \text{Eq. (3-2)}$$

Using the module electrical optimization methodology discussed in section 3.1.3.1 with design option 6 to produce a module with fixed dimensions, the residential module design characteristics listed in Table 3-39 were obtained. The cell dimensions of 2.28 in. for the series length and 6.98 in.² for the area are slightly less than the maximum cell length and area of 2.5 in. and 8 in.², respectively. Using the cell series length of 2.28 in., 20 cells can fit exactly in the 47.5 in. module dimension; therefore, N_{BPMAX} was specified as 10 cells and two bypass groups fit exactly in the module dimension.

As illustrated in the module diagrams in Figure 3-17, the maximum allowable module voltage of 20 V was not obtained because the bypass group voltage of 3.0 V does not divide evenly into 20 V. Instead, the allowable voltage of 15 V from Table 3-37 was used. Because the design required an odd number of bypass groups, the series strings could not be snaked evenly. The final design, therefore, deviated from the module electrical design methodology in that the paralleling for the middle bypass group was split into two sections with interconnection wires running under the cells (dashed lines). The parallel length of the module was capable of accepting 15 cells; therefore, each bypass group contains six parallel strings. In the final layout, 20 cells are arranged in a series direction in the module while 15 cells are arranged in the parallel direction in the module.

The packing factor obtained for the module is 0.926. The module electrical parameters are also listed in Table 3-39. The overall module efficiency which is obtained by multiplying the cell efficiency of 10.8 percent by the packing factor, is 10.0 percent.

Table 3-39. CdS/CuInSe₂ RESIDENTIAL
MODULE DESIGN - OPTION 1

- Cell Dimensions

$$L_{CS} \times L_{CP} = 2.28 \text{ in.} \times 3.06 \text{ in.} = 6.98 \text{ in.}^2 (45.03 \text{ cm}^2)$$

- Bypass Group and Parallel Redundancy

- $N_{BP} = 10 \text{ cells}$

- $N_M = 6 \text{ strings}$

- Module Dimensions and Layout

- $L_{MS} \times L_{MP} = 47.5 \text{ in.} \times 47.5 \text{ in.} (120.65 \text{ cm})$

- 20 in. S-direction $\times$ 15 in. P-direction

- Packing Factor = 0.926

- Module Electrical

- 50 Series $\times$ 6 Parallel

- $V_{OCM} = 21.2V$, $V_{MPM} = 15.0V$

- $I_{SCM} = 10.625A$, $I_{MPM} = 9.71A$

- $P_M = 145.6W$, $\eta_M = 10.0 \text{ percent}$

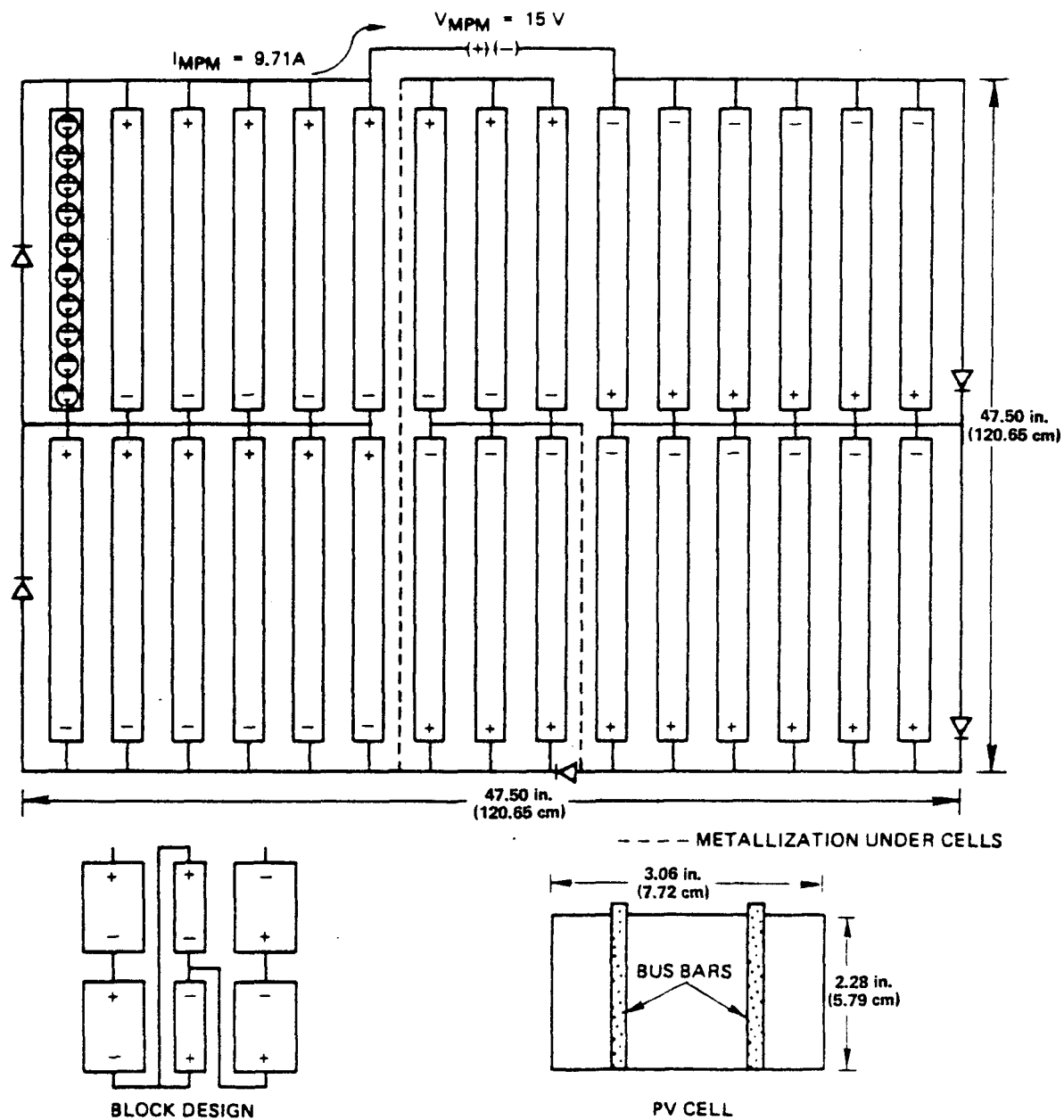


Figure 3-17. CdS/CuInSe₂ RESIDENTIAL MODULE (OPTION 1)

3.4.2.2 Residential System Designs

Following the system design methodology discussed in section 3.1.3.2, module voltage and power were determined at various cell temperatures characteristic of typical operations. The results are shown in Table 3-40, using $-.002 \text{ V}/^{\circ}\text{C}$ and $.0011 \text{ A}/^{\circ}\text{C}$ as the voltage and current variations with temperature. The increase in cell temperature above ambient due to insolation is shown in the table as 25°C .

Based on the residential module data as a function of the temperature window, the DC voltages shown in Table 3-41 were obtained for the series string options of 12, 13, and 14 modules, respectively. At rated conditions of 25°C cell temperature, the 13-module option produces a voltage at peak power of almost 200 V and an open circuit voltage of 275 V. None of the options produce an acceptable peak power voltage variation with temperature because of the high $\Delta V/\Delta T$ for the specified V_{MPC} and because the ratio of V_{OCC} to V_{MPC} is also high.

The AC power window for each of the series string options is shown in Table 3-42. The powers were obtained by multiplying the DC power of the series string by the overall power conditioning efficiency of 0.8765. It can be seen that none of the module options produces a power at 25°C which is approximately divisible into 4 kW, the minimum AC power constraint for the residential system; thus, three strings of the 13-module option could be paralleled to obtain a 4.98 kW residential system or two strings could be paralleled to obtain a 3.32 kW system.

The 3 kW and 5 kW residential array schematics are illustrated in Figure 3-18. Thirteen modules are connected in series to approximate the nominal 200 V desired. In one case, two subarrays are connected in parallel to obtain a DC power of 3.79 kW. The AC power is then 3.32 kW. For the other case, three subarrays are connected in parallel to obtain a DC power of 5.68 kW. The AC power is then 4.98 kW.

3.4.2.3 Module and System Redesign

Since 4 kW and 8 kW arrays could not be obtained with the $\text{CdS}/\text{CuInSe}_2$ module shown in Figure 3-17, the module was redesigned. The power to voltage ratio was too large in the original module, resulting in an AC power of 1.66 kW for the required string of modules. Therefore, the redesign was accomplished by reducing the power of the module while preserving the voltage at 15 V. The simplest approach was to subtract parallel strings from each bypass group. Since the center bypass group was split into two sections, an even number of strings had to be subtracted. The option 2 module listed in Table 3-43 and illustrated in Figure 3-19 was obtained by subtracting two strings from each bypass group.

Table 3-40. CdS/CuInSe₂ RESIDENTIAL MODULE DATA (OPTION 1 MODULE)

MODULE ANALYSIS WORK SHEET...CU IN SE2..15 V RESIDENTIAL

VOC DELTA -.002
 W/T--V/C
VMAX DELT -.002
 W/T--V/C
ISC DELTA .0011
 W/T--A/C
IMAX DELT .0011
 W/T--A/C
NO OF CEL 50
IN SERIES
NO OF CEL 6
 IN //
TCELL-TAM 25
 AT 1 SUN

CONDITION	TAMB DEG-C	TCELL DEG-C	VOC VOLTS	ISC AMPS	VMAX VOLTS	IMAX AMPS	PMAX WATTS
LOW TEMP	-10	15	22.2	10.559	16	9.644	154.304
RATED CON	0	25	21.2	10.625	15	9.71	145.65
S.O.C. NOCT/1000	20	45	19.2	10.757	13	9.842	127.946
T=30C/86F	30	55	18.2	10.823	12	9.908	118.896
T=40/104F	40	65	17.2	10.889	11	9.974	109.714
T=50/122F	50	75	16.2	10.955	10	10.04	100.4

Table 3-41. CdS/CuInSe₂ RESIDENTIAL SUBARRAY DC VOLTAGE WINDOW (OPTION 1 MODULE)

PV STRING VOLTAGE						
* TEMP AMP CELL	NO MODS= 12		NO MODS= 13		NO MODS= 14	
	UMAX	VOC	UMAX	VOC	UMAX	VOC
TAMB -10 TCELL 15	192	266.4	208	288.6	224	310.8
0 25	180	254.4	195	275.6	210	296.8
20 45	156	230.4	169	249.6	182	268.8
30 55	144	218.4	156	236.6	168	254.8
40 65	132	206.4	143	223.6	154	240.8
50 75	120	194.4	130	210.6	140	226.8

*TEMPERATURE IS IN °C

Table 3-42. CdS/CuInSe₂ RESIDENTIAL SUBARRAY AC POWER OUTPUT WITH
PARASITIC LOSS (OPTION 1 MODULE)

* PU STRING POWER...POW=PMOD*NMOD*NALL

NMIS=	.98	MISMATCH		
NWIR=	.98	WIRE LOSS		
NPPT=	.995	PK POW TR		
NBDID=	.997	BLK DIODE		
NPCS=	.92	POW COND		
NALL=	.8765127	OVERALL		
TEMP	NO MODS=	NO MODS=	NO MODS=	
AMB	12	13	14	
CELL				
TAMB	-10	1622.993	1758.242	1893.492
TCELL	15			
	0	1531.969	1659.633	1787.297
	25			
	20	1345.756	1457.902	1570.048
	45			
	30	1250.566	1354.780	1458.994
	55			
	40	1153.989	1250.154	1346.320
	65			
	50	1056.023	1144.024	1232.026
	75			

*POWER IS IN WATTS

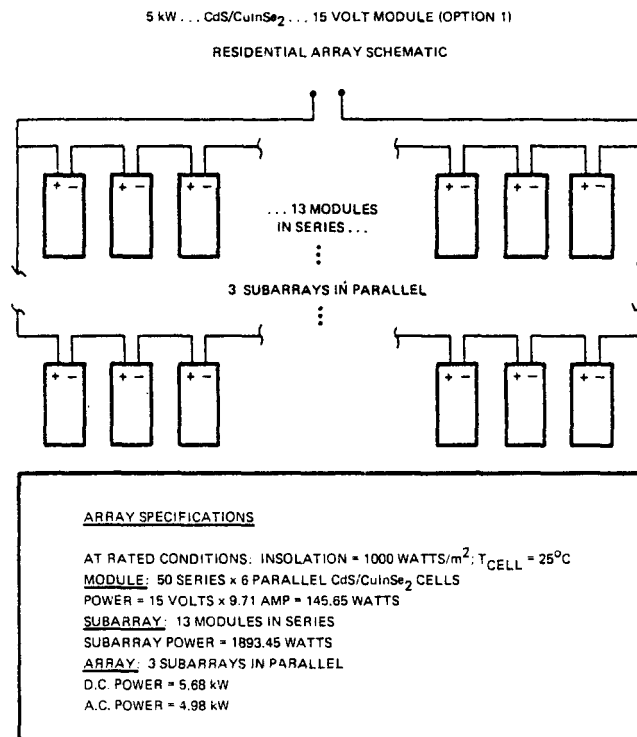
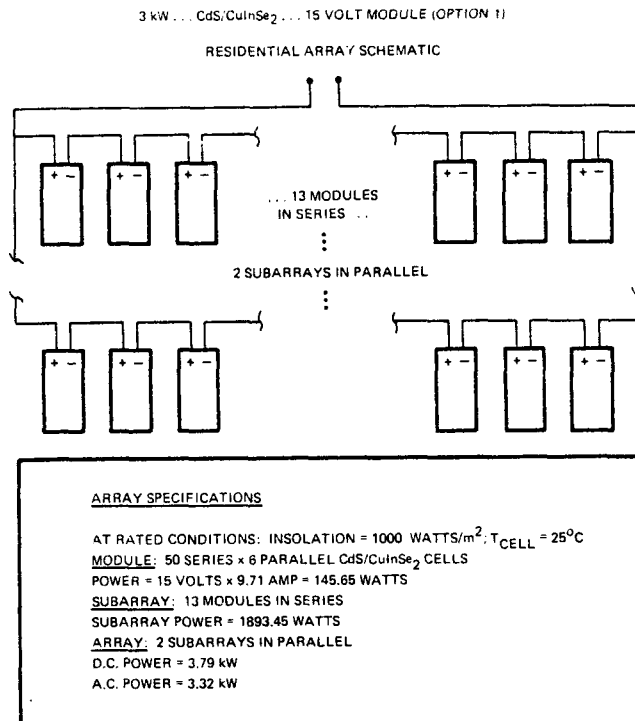


Figure 3-18. SCHEMATICS AND SPECIFICATIONS FOR 3 kW and 5 kW CdS/CuInSe₂ ARRAYS (OPTION 1 MODULE)

Table 3-43. CdS/CuInSe₂ RESIDENTIAL MODULE DESIGN - OPTION 2

- Cell Dimensions

$$L_{CS} \times L_{CP} = 2.28 \text{ in.} \times 3.06 \text{ in.} = 6.98 \text{ in.}^2 (45.03 \text{ cm}^2)$$

- Bypass Group and Parallel Redundancy

- $N_{BP} = 10 \text{ cells}$

- $N_M = 4 \text{ strings}$

- Module Dimensions and Layout

- $L_{MS} \times L_{MP} = 47.5 \text{ in.} \times 31.91 \text{ in.} (120.65 \text{ cm} \times 81.05 \text{ cm})$

- 20 in. S-direction X 10 in. P-direction

- Packing Factor = 0.921

- Module Electrical

- 50 Series X 4 Parallel

- $V_{OCM} = 21.2V$, $V_{MPM} = 15.0V$

- $I_{SCM} = 7.08A$, $I_{MPM} = 6.47A$

- $P_M = 97.05W$, $\eta_M = 9.95 \text{ percent}$

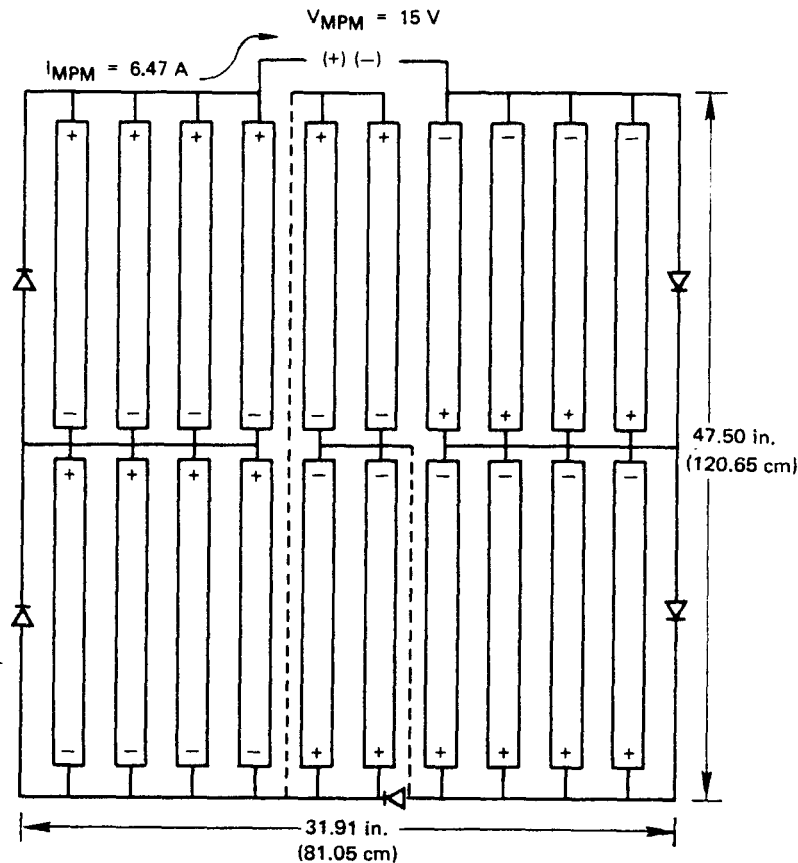


Figure 3-19. CdS/CuInSe₂ RESIDENTIAL MODULE (OPTION 2)

The resulting module parallel length was then 31.9 in. with 10 cells arranged in the parallel direction. This reduced the module power from 145.0 W for the original to 97.05 W for option 2. With four strings for each bypass group, parallel redundancy is still satisfied.

Other options could have been chosen. For example, the module parallel length could have been chosen as 3 ft. or 2 ft. and the module could have been completely redesigned. The solution chosen, however, was the simplest option and preserved the 4 ft. series length. The parallel length of 31.9 in. is not critical since the roof mounting need only be accomplished based on one dimension. In fact, many currently available residential modules have widths that are not multiples of one foot.

The system design process was then repeated for the option 2 module. The module voltage and power versus temperature are shown in Table 3-44. Based on this data, the voltage and AC power windows for module string options of 12, 13, and 14 modules were determined (Tables 3-45 and 3-46). Once again, the 13-module option was chosen. In this case, however, it is nearly divisible into 4 kW. Therefore, four of these strings could be paralleled to approximate the 4 kW residential system and eight strings could be paralleled for the 8 kW system.

Table 3-44. CdS/CuInSe₂ RESIDENTIAL MODULE DATA (OPTION 2 MODULE)

MODULE ANALYSIS WORK SHEET...CU IN SE2..15 V RESIDENTIAL							
VOC DELTA	-.002						
W/T--U/C							
VMAX DELT	-.002						
W/T--U/C							
ISC DELTA	.0011						
W/T--A/C							
IMAX DELT	.0011						
W/T--A/C							
NO OF CEL	50						
IN SERIES							
NO OF CEL	4						
IN //							
TCELL-TAM	25						
AT 1 SUN							
CONDITION	TAMB DEG-C	TCELL DEG-C	VOC VOLTS	ISC AMPS	VMAX VOLTS	IMAX AMPS	PMAX WATTS
LOW TEMP	-10	15	22.2	7.041	16	6.426	102.816
RATED CON	0	25	21.2	7.085	15	6.47	97.05
S.O.C. NOCT/1000	20	45	19.2	7.173	13	6.558	85.254
T=30C/86F	30	55	18.2	7.217	12	6.602	79.224
T=40/104F	40	65	17.2	7.261	11	6.646	73.106
T=50/122F	50	75	16.2	7.305	10	6.69	66.9

Table 3-45. CdS/CuInSe₂ RESIDENTIAL SUBARRAY DC VOLTAGE WINDOW (OPTION 2 MODULE)

PV STRING VOLTAGE							
* TEMP AMB CELL	NO MODS= 12		NO MODS= 13		NO MODS= 14		
	U _{MAX}	U _{OC}	U _{MAX}	U _{OC}	U _{MAX}	U _{OC}	
TAMB -10 TCELL 15	192	266.4	208	288.6	224	310.8	
0 25	180	254.4	195	275.6	210	296.8	
20 45	156	230.4	169	249.6	182	268.8	
30 55	144	218.4	156	236.6	168	254.8	
40 65	132	206.4	143	223.6	154	240.8	
50 75	120	194.4	130	210.6	140	226.8	

*TEMPERATURE IS IN °C

Table 3-46. CdS/CuInSe₂ RESIDENTIAL SUBARRAY AC POWER OUTPUT
WITH PARASITIC LOSS (OPTION 2 MODULE)

* PV STRING POWER... $POW=PMOD*NMOD*NALL$

NMIS= .98MISMATCH
NWIR= .98WIRE LOSS
NPPT= .995PK POW TR
NBDID= .997BLK DIODE
NPCS= .92POW COND
NALL= .8765127OVERALL

	TEMP NO MODS=	NO MODS=	NO MODS=
	AMB 12	13	14
CELL			
TAMB -10	1081.434	1171.554	1261.673
TCELL 15			
0	1020.787	1105.852	1190.918
25			
20	896.7146	971.4408	1046.167
45			
30	833.2901	902.7310	972.1718
55			
40	768.9401	833.0184	897.0967
65			
50	703.6644	762.3031	820.9418
75			

*POWER IS IN WATTS

The final 4 kW and 8 kW CdS/CuInSe₂ residential array schematics are illustrated in Figure 3-20. Thirteen modules are connected in series to approximate the nominal 200 V desired. In one case, four subarrays are connected in parallel to obtain a DC power of 5.05 kW. The AC power is then 4.42 kW. For the other case, eight subarrays are connected in parallel to obtain a DC power of 10.09 kW. The AC power is then 8.85 kW.

3.4.3 CdS/CuInSe₂ CPS Designs

3.4.3.1 CPS Module Design

The design constraints which apply to all CPS module designs were previously discussed in section 3.1.2 and are repeated here in Table 3-47 for the reader's convenience. Table 3-48 lists the CPS module constraints which apply specifically to the CdS/CuInSe₂ technology. These constraints are the same as those previously discussed for the CdS/CuInSe₂ residential modules.

Using the module optimization methodology discussed in section 3.1.3.1 the CPS module characteristics presented in Table 3-49 were obtained. Design option 6 was used to produce the module with the fixed dimensions of 47.5 in. x 95.0 in. The series and parallel lengths of the cells are 2.28 in. x 2.88 in., respectively. With the cell series length of 2.28 in., 20 cells could be placed in the module dimension of 47.5 in.; thus, the bypass group was specified as 10 cells with two bypass groups connected in parallel in the series direction. The bypass groups could then be snaked up and down 16 times to obtain the desirable peak power voltage of approximately 50 V as illustrated in the CPS module diagrams in Figure 3-21. The module parallel length of 95.0 in. was sufficient to contain 32 cells with 2.88 in. parallel cell lengths. Thus, each bypass group could be paralleled four times to satisfy the parallel redundancy constraints. The layout and interconnections shown in Figure 3-21 indicate paralleling of bypass group strings in the series direction. The submodule at the lower left contains two bypass groups. Each bypass group consists of 10 cells in series by four strings in parallel. Positive terminals of the submodule are at top and bottom on the left side while negative terminals are at top and bottom on the right. The module is then composed of eight of these submodules connected in series in the parallel module direction.

The module packing factor obtained is 0.932. The module efficiency which is obtained by multiplying the cell efficiency of 10.8 percent by the packing factor, is 10.1 percent.

3.4.3.2 CPS System Design

Following the system design methodology discussed in section 3.1.3.2, the voltage and power of the module as a function of expected cell temperatures are presented in Table 3-50, using voltage variation with temperature of

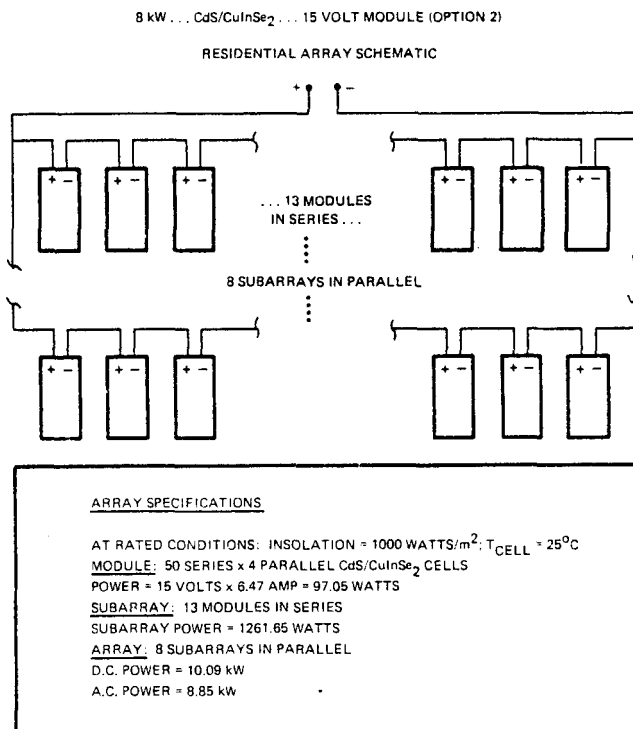
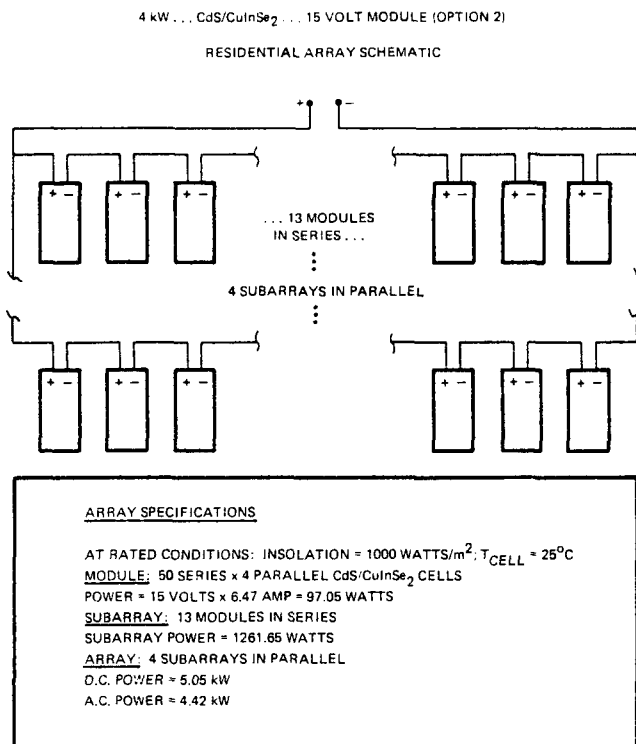


Figure 3-20. SCHEMATICS AND SPECIFICATIONS FOR 4 kW and 8 kW CdS/CuInSe₂ ARRAYS (OPTION 2 MODULE)

Table 3-47. DESIGN CONSTRAINTS APPLIED TO
ALL CPS MODULE DESIGNS

- Maximum Open Circuit Module Voltage at Low Temperature

$$V_{OCM}(\text{Max}) = 150V @ - 20^{\circ}C$$

- Maximum Module Peak Power Voltage

$$V_{MPM}(\text{Max}) = 100V$$

- Acceptable Module Peak Power Voltage

$$V_{MPM} = 50V \text{ or } 100V$$

- Maximum Allowable Reverse Cell Voltage

$$V_{RMAX} = -6.7V$$

- Maximum Module Dimensions*

$$\text{Dim (Max)} = 47.5 \text{ in. X } 95.0 \text{ in. (120.65 cm x 241.3 cm)}$$

- Edge Spacing⁺

$$\Delta_{SE} = 3/8 \text{ in. (0.9525 cm)}$$

- Parallel Redundancy Desirable

- For cracked cells and broken interconnects
- Not for Cell Shadowing

- * Amorphous Silicon - 11.75 in. X 47.5 in. (29.85 cm x 120.65 cm)
- Ga As - 95.0 in. X 143.0 in. (241.3 cm x 363.2 cm)
- + Ga As - 1.0 in. (2.54 cm)

**Table 3-48. CdS/CuInSe₂ DESIGN CONSTRAINTS FOR
CPS MODULES**

- Maximum Cell Length in Series Direction (Ribbon Width)

$$L_{\text{CSMAX}} = 2.5 \text{ in. (6.35 cm)}$$

- Maximum Cell Area

$$A_{\text{CMAX}} = 8 \text{ in.}^2 \text{ (51.6 cm}^2\text{)}$$

- Interior Spacing

$$\Delta_{\text{SI}} = 1/16 \text{ in. (0.159 cm)}$$

- Maximum Number of Cells in Bypass Group

$$N_{\text{BPMAX}} = 15 \text{ cells}$$

- Minimum Number of Cells or Strings in Parallel

$$N_{\text{MMIN}} = 4 \text{ for cracked cell or broken interconnect}$$

Table 3-49. CdS/CuInSe₂ CPS MODULE DESIGN

- Cell Dimensions

$$L_{CS} \times L_{CP} = 2.28 \text{ in.} \times 2.88 \text{ in.} = 6.57 \text{ in.}^2 (42.39 \text{ cm}^2)$$

- Bypass Group and Parallel Redundancy

- $N_{BP} = 10 \text{ cells}$

- $N_M = 4 \text{ strings}$

- Module Dimensions and Layout

- $L_{MS} \times L_{MP} = 47.5 \text{ in.} \times 95.0 \text{ in.} (120.65 \text{ cm} \times 241.3 \text{ cm})$

- 20 in. S-direction x 32 in. P-direction

- Packing Factor = 0.932

- Module Electrical

- 160 Series X 4 Parallel

- $V_{OCM} = 67.8V$, $V_{MPM} = 48.0V$

- $I_{SCM} = 6.68A$, $I_{MPM} = 6.10A$

- $P_M = 293.0W$, $\eta_m = 10.1 \text{ percent}$

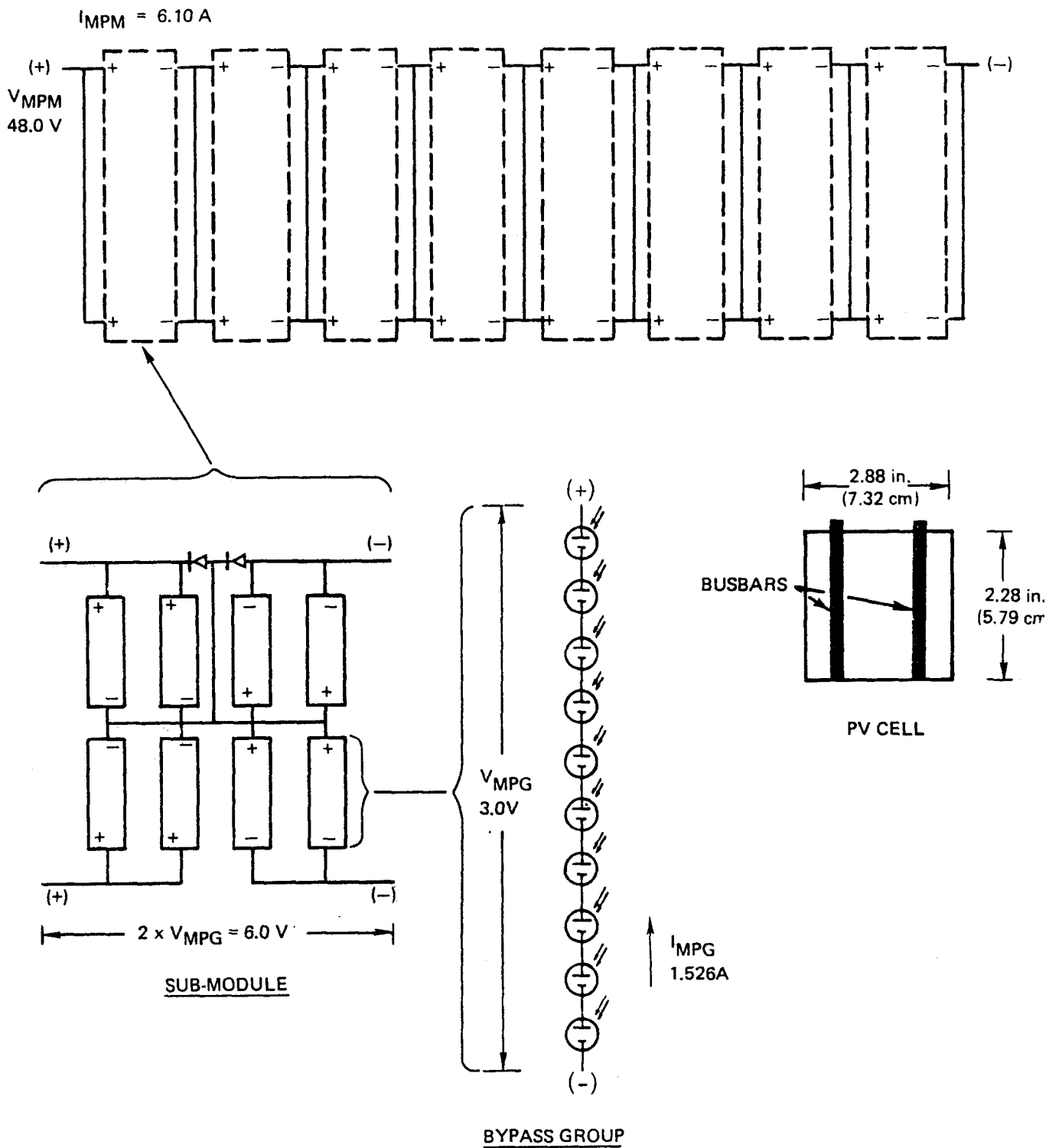


Figure 3-21. CdS/CuInSe₂ CPS MODULE

Table 3-50. CdS/CuInSe₂ CPS MODULE DATA

MODULE ANALYSIS WORK SHEET...CU IN SE2..48 VOLT CENTRAL POWER STATION							
VOC DELTA	-.002						
W/T--U/C							
VMAX DELT	-.002						
W/T--U/C							
ISC DELTA	.001						
W/T--A/C							
IMAX DELT	.001						
W/T--A/C							
NO OF CEL	160						
IN SERIES							
NO OF CEL	4						
IN //							
TCELL-TAM	25						
AT 1 SUN							
CONDITION	TAMB DEG-C	TCELL DEG-C	VOC VOLTS	ISC AMPS	VMAX VOLTS	IMAX AMPS	PMAX WATTS
LOW TEMP	-10	15	71	6.64	51.2	6.064	310.4768
RATED CON	0	25	67.8	6.68	48	6.104	292.992
S.O.C. NOCT/1000	20	45	61.4	6.76	41.6	6.184	257.2544
T=30C/86F	30	55	58.2	6.8	38.4	6.224	239.0016
T=40/104F	40	65	55	6.84	35.2	6.264	220.4928
T=50/122F	50	75	51.8	6.88	32	6.304	201.728

-0.002 V/°C and current variation with temperature of 0.0010 A/°C. The increase in cell temperature above ambient due to insolation is 25°C.

Table 3-51 lists the DC voltage variations with temperature for series string options of 20, 21, and 22 modules, respectively. The 21-module option approximates the nominal system voltage constraint of 1000 V at 25°C. None of the module options satisfy the voltage window constraint of 800 to 1300 V DC because of the high $\Delta V/\Delta T$ for the specified V_{MPC} and because the ratio of V_{OCC} to V_{MPC} is also high. The AC power variations with temperature are presented in Table 3-52. The 21-string module produces an AC power of 5393 W at 25°C. This option can be paralleled 371 times to obtain the minimum subarray AC power of 2.00 MW.

In Figure 3-22, the 50 MW CdS/CuInSe₂ CPS array is shown to consist of 25 subarrays of 2 MW each connected in parallel. Each 2 MW subarray consists of 21 modules connected in series to approximate a nominal 1000 V and 371 series strings connected in parallel to produce 2.28 MW of DC power. With the power conditioning component efficiency of 0.8765, the AC power thus produced is 2.00 MW.

Table 3-51. CdS/CuInSe₂ CPS DC VOLTAGE WINDOW

PU STRING VOLTAGE

* TEMP AMB CELL	NO MODS= 20		NO MODS= 21		NO MODS= 22	
	UMAX	VOC	UMAX	VOC	UMAX	VOC
TAMB -10 TCELL 15	1024	1420	1075.2	1491	1126.4	1562
0 25	960	1356	1008	1423.8	1056	1491.6
20 45	832	1228	873.6	1289.4	915.2	1350.8
30 55	768	1164	806.4	1222.2	844.8	1280.4
40 65	704	1100	739.2	1155	774.4	1210
50 75	640	1036	672	1087.8	704	1139.6

*TEMPERATURE IS IN °C

Table 3-52. CdS/CuInSe₂ CPS STRING AC POWER OUTPUT WITH PARASITIC LOSSES

* PV STRING POWER...POW=PMOD*NMOD*NALL

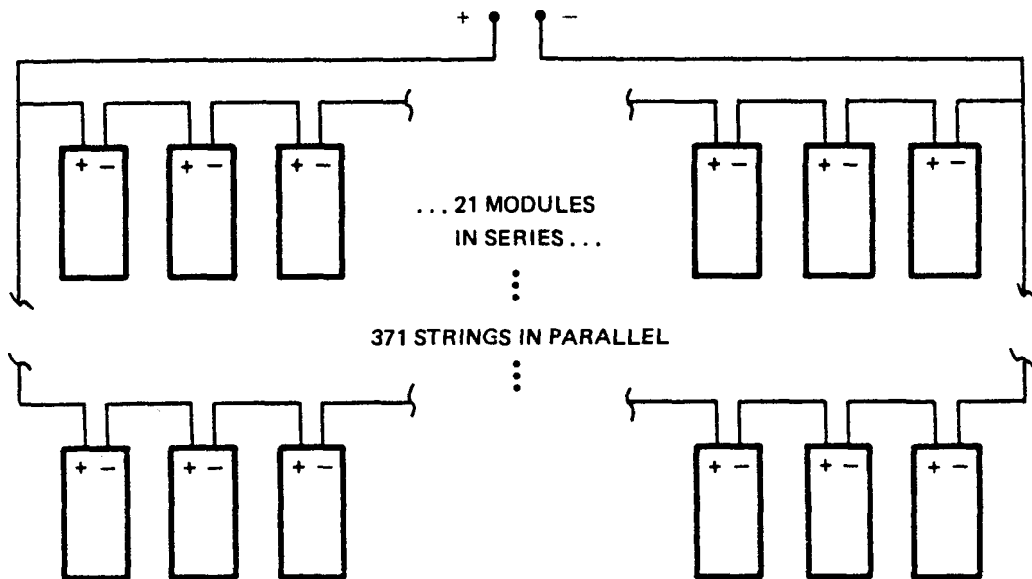
NMIS= .98MISMATCH
 NWIR= .98WIRE LOSS
 NPPT= .995PK POW TR
 NBDID= .997BLK DIODE
 NPCB= .92POW COND
 NALL= .8765127OVERALL

	TEMP	NO MODS=	NO MODS=	NO MODS=
	AMB	20	21	22
	CELL			
TAMB	-10	5442.737	5714.874	5987.011
TCELL	15			
	0	5136.224	5393.035	5649.847
	25			
	20	4509.735	4735.222	4960.709
	45			
	30	4189.759	4399.247	4608.735
	55			
	40	3865.295	4058.560	4251.824
	65			
	50	3536.343	3713.160	3889.977
	75			

*POWER IS IN WATTS

50 MW ... CdS/CuInSe₂ ... 48 VOLT MODULE

CENTRAL POWER STATION 2 MW SUBARRAY SCHEMATIC



ARRAY SPECIFICATIONS

AT RATED CONDITIONS: INSOLATION = 1000 WATTS/m²; T_{CELL} = 25°C

MODULE: 160 SERIES x 4 PARALLEL CdS/CuInSe₂ CELLS

POWER = 48 VOLTS x 6.104 AMP = 292.99 WATTS

STRING: 21 MODULES IN SERIES

STRING POWER = 6.15 kW

SUBARRAY: 371 STRINGS IN PARALLEL

D.C. POWER = 2.28 MW

A.C. POWER = 2.00 MW

CENTRAL POWER STATION ARRAY: 25 SUBARRAYS IN PARALLEL

A.C. POWER = 50 MW

Figure 3-22. SCHEMATIC AND SPECIFICATIONS FOR 50 MW CdS/CuInSe₂ CPS ARRAY

3.5 GALLIUM ARSENIDE CONCEPTUAL DESIGNS

The Gallium Arsenide (GaAs) system designs were developed using the design approach previously discussed in section 3.1 based on the module and system design methodologies discussed in section 3.1.3. The format is slightly different than that used in the sections for the other technologies since a different technology process is used for the CPS than that used for the residential designs.

3.5.1 GaAs Residential Designs

3.5.1.1 Cell Parameters

The GaAs residential designs are based on the CLEFT process, being developed at MIT, which grows homojunction cells on reusable substrates [8]. An I-V curve, which satisfies the 20 percent efficiency goal for GaAs, (Figure 3-23) was obtained from SERI files [24]. Normalizing this curve for a one-square-centimeter cell, the parameters listed in Table 3-53 were obtained. The voltage at peak power is 0.833 V and the current density at peak power is 24 mA/cm². The voltage variation with temperature was obtained from efficiency versus temperature data reported for similar type cells [37], using the same current variation with temperature as used for all technologies in these designs.

The current variation with temperature is expressed as a fractional variation and would be multiplied by the actual cell current to determine the current variation with temperature. The cell contains two across-the-cell interconnects to provide redundancy in the case of cracked cells or broken interconnects. These redundant interconnects are useful in reducing the number of parallel strings or cells required to satisfy parallel redundancy constraints.

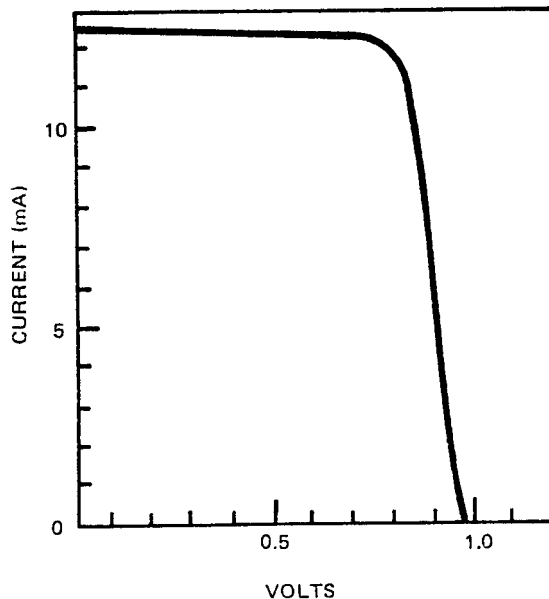


Figure 3-23. GaAs SHALLOW HOMOJUNCTION CELL I-V CURVE

Table 3-53. GaAs CELL PARAMETERS FOR RESIDENTIAL MODULES

V_{OCC}	=	0.97V
V_{MPC}	=	0.833V
J_{SCC}	=	25.0mA/cm ²
J_{MPC}	=	24.0mA/cm ²
FF	=	0.824
P_C	=	20.0mW/cm ²
η_C	=	20 percent
$\Delta V/\Delta T$	=	-3.2mV/°C
$\Delta f_I/\Delta T$	=	0.00061/°C
N_{ACI}	=	2

3.5.1.2 Residential Module Designs

The design constraints which apply to all residential module designs were discussed in section 3.1.2 and are reproduced here in Table 3-54 for the reader's convenience. Table 3-55 presents the module design constraints which apply specifically to GaAs residential modules. The maximum module dimensions of 2 ft. x 4ft. are those postulated by MIT [8]. The maximum cell area of 16 in.² (~100 cm²) represents a goal expressed by J. Benner of SERI [10]. The 1/16 in. interior spacing between cells is consistent with spacing requirements for cell assembly in modules in which voltage differentials are within 50 V [33]. The maximum number of cells in a bypass group was determined from the maximum allowable reverse cell voltage of -6.7 V (previously specified in Table 3-54). The equation used to obtain N_{BPMAX} is:

$$N_{BPMAX} = 1 - \frac{V_{RMAX} + V_{FD}}{V_{OCC}} \quad \text{Eq. (3-1)}$$

where V_{FD} = forward voltage of bypass diode. The parallel redundancy constraint of seven cells or strings in parallel was obtained from the relationship between the cell short-circuit current and peak-power current, and the number of across-the-cell interconnects, by the equation:

**Table 3-54. DESIGN CONSTRAINTS APPLIED TO
ALL RESIDENTIAL MODULE DESIGNS**

- Maximum Open Circuit Module Voltage at Low Temperature

$$V_{OCM}(\text{Max}) = 30V @ - 20^{\circ} C$$

- Maximum Module Peak Power Voltage

$$V_{MPM}(\text{Max}) = 20V$$

- Acceptable Module Peak Power Voltages

$$V_{MPM} = 5, 7.5, 10, 15, \text{ or } 20V$$

- Maximum Allowable Reverse Cell Voltage

$$V_{RMAX} = -6.7V$$

- Maximum Module Dimensions*

$$\text{Dim (Max)} = 47.5 \text{ in X } 47.5 \text{ in (120.65 cm)}$$

- Edge Spacing

$$\Delta_{SE} = 3/8 \text{ in (0.925 cm)}$$

- Parallel Redundancy Desirable

Prevents bypass activation due to single cell shadowing,
single interconnect breaking or single cell cracking.

- * Amorphous Silicon - 11.75 in X 47.5 in (29.85 cm x 20.65 cm)
Ga As - 23.5 in X 47.5 in (59.69 cm x 120.65 cm)

Table 3-55. GaAs DESIGN CONSTRAINTS FOR RESIDENTIAL MODULES

- Maximum Module Dimensions
Dim(Max) = 23.5in X 47.5 in (59.69 cm x 120.65 cm)
- Maximum Cell Area
 $A_{\text{CMAX}} = 16 \text{ in}^2 (103.2 \text{ cm}^2)$
- Interior Spacing
 $\Delta_{\text{SI}} = 1/16 \text{ in } (0.159 \text{ cm})$
- Maximum Number of Cells in Bypass Group
 $N_{\text{BPMAX}} = 7 \text{ cells}$
- Minimum Number of Cells or Strings in Parallel
 $N_{\text{MMIN}} = 7 \text{ for cracked cell or broken interconnect}$

$$N_{\text{MMIN}} = \frac{J_{\text{SCC}}}{2N_{\text{ACI}} (J_{\text{SCC}} - J_{\text{MPC}})} \quad \text{Eq. (3-2)}$$

Using the module electrical design optimization methodology discussed in section 3.1.3.1, with design option 5 to produce a module with fixed dimensions, the GaAs residential module design characteristics listed in Table 3-56 were obtained. The cell dimensions are nearly square and the cell area of 14.36 in.² is slightly less than the 16 in.² maximum.

Using the cell series length of 3.84 in., 12 cells can fit exactly in the 47.5 in. module dimension; therefore, N_{BPMAX} was specified as 6 cells and two bypass groups fit exactly in the module dimension.

As illustrated in the GaAs residential module diagrams in Figure 3-24, the maximum allowable module voltage of 20 V was obtained by snaking the series group back in the opposite direction, so that 24 cells are connected in series. The parallel length of the module was then capable of accepting three cells in parallel for each series cell. Thus, 12 cells are arranged in the series direction in the module, while six cells are arranged in the parallel direction in the module. Since the parallel redundancy constraint is seven cells, this constraint could not be satisfied.

As seen in the PV cell diagram at the lower left in Figure 3-24, the redundant interconnects run in the parallel direction. It was felt that with this process, it would be easier to make parallel interconnections for initial cell connections and to make all series connections along the sides of the module, as shown in the interconnection layout, although J. C. Fan in a telephone communication indicated this was not required [38].

Table 3-56. GaAs RESIDENTIAL MODULE - DESIGN OPTION 1

- Cell Dimensions
 - $L_{CS} \times L_{CP} = 3.84\text{in} \times 3.74\text{ in} = 14.36\text{in}^2 \text{ (92.65 cm}^2\text{)}$
- Bypass Group and Parallel Redundancy
 - $N_{BP} = 6$ cells
 - $N_M = 3$ cells (Parallel Redundancy not satisfied)
- Module Dimensions
 - $L_{MS} \times L_{MP} = 47.5\text{in} \times 23.5\text{in} \text{ (120.65 cm x 59.69 cm)}$
 - 12 in S-direction X 6 in P-direction
 - Packing Factor = 0.926
- Module Electrical
 - 24 Series X 3 Parallel
 - $V_{OCM} = 23.3\text{V}$, $V_{MPM} = 20.0\text{V}$
 - $I_{SCM} = 6.95\text{A}$, $I_{MPM} = 6.67\text{A}$
 - $P_M = 133.2\text{W}$, $\eta_M = 18.52$ percent

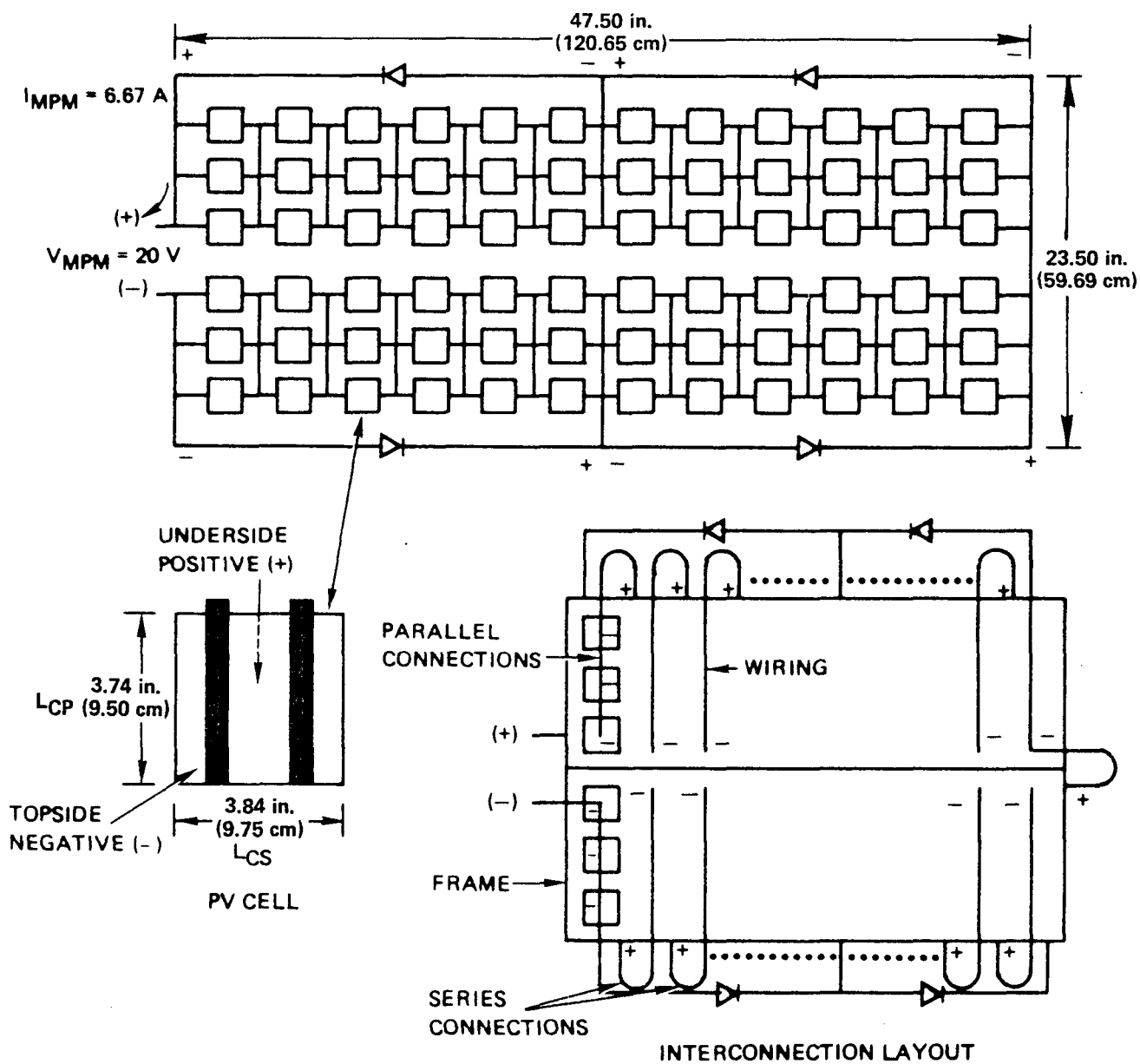


Figure 3-24. GaAs RESIDENTIAL MODULE (OPTION 1)

The packing factor obtained for the module is 0.926. The module electrical parameters are also listed in Table 3-56. The overall module efficiency, which is obtained by multiplying the cell efficiency of 20.0 percent by the packing factor, is 18.52 percent.

3.5.1.3 Residential System Designs

Following the system design methodology discussed in section 3.1.3.2, module voltage and power were determined at various cell temperatures characteristic of typical operations. The results are shown in Table 3-57, using $-.0032 \text{ V}/^{\circ}\text{C}$ and $0.0014 \text{ A}/^{\circ}\text{C}$ as the voltage and current variations with temperature. The increase in cell temperature above ambient, due to insolation, is shown in the table as 25°C .

Table 3-57. GaAs RESIDENTIAL MODULE DATA (OPTION 1 MODULE)

MODULE ANALYSIS WORK SHEET...GA AS..FLAT PLATE 20 VOLT RESIDENTIAL.							
VOC DELTA	-.0032						
W/T--V/C							
UMAX DELT	-.0032						
W/T--V/C							
ISC DELTA	.0014						
W/T--A/C							
IMAX DELT	.0014						
W/T--A/C							
NO OF CEL	24						
IN SERIES							
NO OF CEL	3						
IN //							
TCELL-TAM	25						
AT 1 SUN							

CONDITION	TAMB DEG-C	TCELL DEG-C	VOC VOLTS	ISC AMPS	UMAX VOLTS	IMAX AMPS	PMAX WATTS
LOW TEMP	-10	15	24.068	6.908	20.768	6.658	138.2733
RATED CON	0	25	23.3	6.95	20	6.7	134
S.O.C. NOCT/1000	20	45	21.764	7.034	18.464	6.784	125.2598
T=30C/86F	30	55	20.996	7.076	17.696	6.826	120.7929
T=40/104F	40	65	20.228	7.118	16.928	6.868	116.2615
T=50/122F	50	75	19.46	7.16	16.16	6.91	111.6656

Based on the residential module data as a function of the temperature window, the DC voltages shown in Table 3-58 were obtained for the series string options of 9, 10, and 11 modules, respectively. At rated conditions of 25°C cell temperature, the 10-module option produces a voltage at peak power of 200 V and an open-circuit voltage of 233 V. This option also produces an acceptable peak power voltage variation with temperature.

The AC power window for each of the series-string options is shown in Table 3-59. The powers were obtained by multiplying the DC power of the series string by the overall power conditioning efficiency of 0.8765. It can be seen that none of the module options produces a power at 25°C, which is approximately divisible into 4 kW - the minimum AC power constraint for the residential system. Thus, three strings of the 10-module option could be paralleled to obtain a 3.52 kW residential system or four strings could be paralleled to obtain a 4.70 kW system.

The 3 kW and 5 kW residential array schematics are illustrated in Figure 3-25. Ten modules are connected in series to obtain the nominal 200 V desired. In one case, three subarrays are connected in parallel to obtain a DC power of 4.02 kW. The AC power is then 3.52 kW. For the other case, four subarrays are connected in parallel to obtain a DC power of 5.36 kW. The AC power is then 4.70 kW.

3.5.1.4 Module And System Redesign

Since 4 kW and 8 kW arrays could not be obtained with the GaAs module shown in Figure 3-24, the module was redesigned. The power to voltage ratio, though not excessively large in the original module, resulted in an AC power for the required string of modules which could not be multiplied to obtain 4 kW. Therefore, the redesign was accomplished by reducing the power of the module while preserving the voltage at 20V. The simplest approach was to subtract parallel cells. The option 2 module listed in Table 3-60 and illustrated in Figure 3-26 was obtained by reducing the parallel cells from three to two. The resulting module parallel length was then 15.9 in. with 4 cells arranged in the parallel direction. This reduced the module power from 133.2 W for the original to 89.0 W for option 2.

Other options could have been chosen. For example, the module parallel length could have been chosen as 1 ft. and the module could have been completely redesigned. The solution chosen, however, was the simplest option and preserved the 4 ft. series length. The parallel length of 15.9 in. is not critical since the roof mounting need only be accomplished based on one dimension. In fact, many currently available residential modules have widths that are not multiples of one foot.

**Table 3-58. GaAs RESIDENTIAL SUBARRAY DC VOLTAGE
WINDOW (OPTION 1 MODULE)**

PV STRING VOLTAGE							
* TEMP AMB CELL		NO MODS= 9		NO MODS= 10		NO MODS= 11	
		VHAX	VOC	VHAX	VOC	VHAX	VOC
TAMB	-10	196.912	216.612	207.68	240.69	228.448	264.748
TCELL	15						
	0	180	209.7	200	233	220	256.3
	25						
	20	186.176	195.876	184.64	217.64	203.104	239.404
	45						
	30	159.264	188.964	176.96	209.96	194.656	230.956
	55						
	40	152.352	182.052	169.28	202.28	186.208	222.508
	65						
	50	145.44	175.14	161.6	194.6	177.76	214.06
	75						

*TEMPERATURE IS IN °C

**Table 3-59. GaAs RESIDENTIAL SUBARRAY AC POWER OUTPUT
WITH PARASITIC LOSS (OPTION 1 MODULE)**

* PU STRING POWER...POW=PMOD*NMOD*NALL

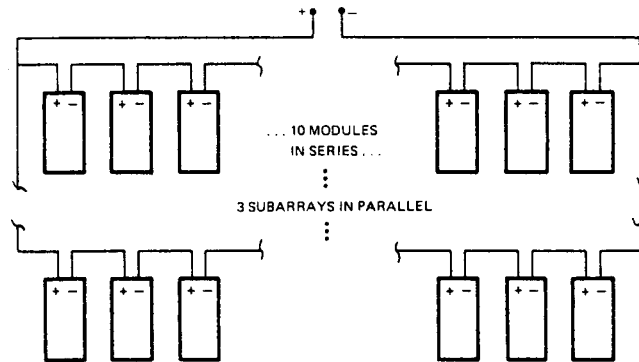
NMIS=	.98	MISMATCH
NWIR=	.98	WIRE LOSS
NPPT=	.995	PK POW TR
NBDID=	.997	BLK DIODE
NPCS=	.92	POW COND
NALL=	.8765127	OVERALL

	TEMP	NO MODS=	NO MODS=	NO MODS=
	AMB	9	10	11
	CELL			
TAMB	-10	1090.785	1211.983	1333.182
TCELL	15			
	0	1057.074	1174.527	1291.980
	25			
	20	988.1261	1097.918	1207.710
	45			
	30	952.8886	1058.765	1164.642
	55			
	40	917.1422	1019.047	1120.952
	65			
	50	880.8869	978.7632	1076.639
	75			

*POWER IS IN WATTS

3 kW ... GA AS ... 20 VOLT (FLAT PLATE) MODULE (OPTION 1)

RESIDENTIAL ARRAY SCHEMATIC

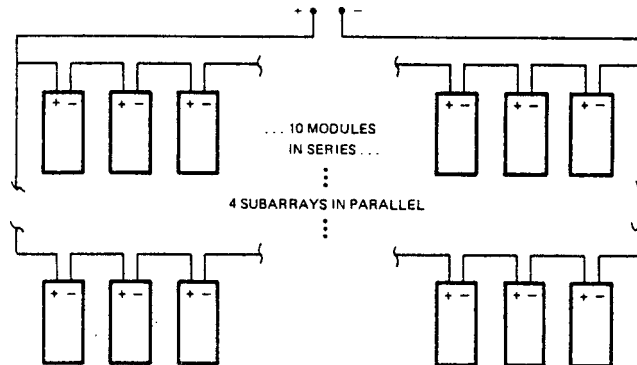


ARRAY SPECIFICATIONS

AT RATED CONDITIONS: INSOLATION = 1000 WATTS/m²; T_{CELL} = 25 °C
MODULE: 24 SERIES x 3 PARALLEL GA AS CELLS
 POWER = 20 VOLTS x 6.7 AMP = 134 WATTS
SUBARRAY: 10 MODULES IN SERIES
 SUBARRAY POWER = 1340 WATTS
ARRAY: 3 SUBARRAYS IN PARALLEL
 D.C. POWER = 4.02 kW
 A.C. POWER = 3.52 kW

5 kW ... GA AS ... 20 VOLT (FLAT PLATE) MODULE (OPTION 1)

RESIDENTIAL ARRAY SCHEMATIC



ARRAY SPECIFICATIONS

AT RATED CONDITIONS: INSOLATION = 1000 WATTS/m²; T_{CELL} = 25 °C
MODULE: 24 SERIES x 3 PARALLEL GA AS CELLS
 POWER = 20 VOLTS x 6.7 AMP = 134 WATTS
SUBARRAY: 10 MODULES IN SERIES
 SUBARRAY POWER = 1340 WATTS
ARRAY: 4 SUBARRAYS IN PARALLEL
 D.C. POWER = 5.36 kW
 A.C. POWER = 4.70 kW

Figure 3-25. SCHEMATICS AND SPECIFICATIONS FOR 3 kW AND 5 kW GaAs ARRAYS (OPTION 1 MODULE)

Table 3-60. GaAs RESIDENTIAL MODULES - DESIGN OPTION 2

- Cell Dimensions

$$L_{CS} \times L_{CP} = 3.84 \text{ in.} \times 3.74 \text{ in.} = 14.36 \text{ in.}^2 (92.64 \text{ cm}^2)$$

- Bypass Group and Parallel Redundancy

- $N_{BP} = 6 \text{ cells}$

- $N_M = 2 \text{ cells}$ (Parallel Redundancy not satisfied)

- Module Dimensions

- $L_{MS} \times L_{MP} = 47.5 \text{ in.} \times 15.9 \text{ in.}$ (120.65 cm x 40.39 cm)

- 12 in. S-direction X 4 in. P-direction

- Packing Factor = 0.913

- Module Electrical

- 24 Series X 2 Parallel

- $V_{OCM} = 23.3V$, $V_{MPM} = 20.0V$

- $I_{SCM} = 4.63A$, $I_{MPM} = 4.45A$

- $P_M = 89.0W$, $\eta_M = 18.26 \text{ percent}$

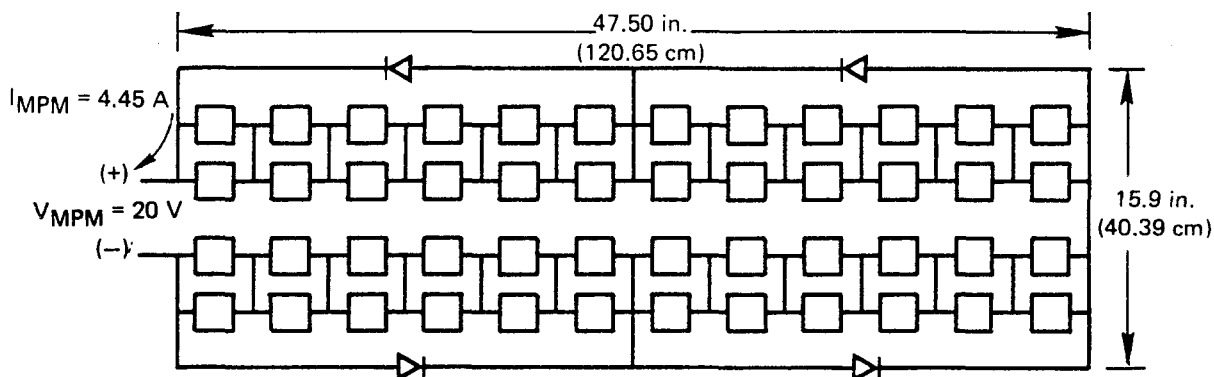


Figure 3-26. GaAs RESIDENTIAL MODULE (OPTION 2)

The system design process was then repeated for the option 2 module. The module voltage and power versus temperature are shown in Table 3-61. Based on this data, the voltage and AC power windows for module string options of 9, 10 and 11 modules were determined (Tables 3-62 and 3-63). Once again, the 10-module option was chosen. In this case, however, it is nearly divisible into 4 kW. Therefore, five of these strings could be paralleled to approximate the 4 kW residential system and ten strings could be paralleled for the 8 kW system.

The 4 kW and 8 kW GaAs residential array schematics are illustrated in Figure 3-27. Ten modules are connected in series to obtain the nominal 200 V desired. In one case, five subarrays are connected in parallel to obtain a DC power of 4.45 kW. The AC power is then 3.90 kW. For the other case, ten subarrays are connected in parallel to obtain a DC power of 8.90 kW. The AC power is then 7.80 kW.

3.5.2 GaAs CPS System Design

3.5.2.1 Cell Parameters

The GaAs CPS application uses multi-junction cascaded cells similar to those reported by Research Triangle Institute (RTI) [9]. The J-V curves, postulated to satisfy SERI GaAs efficiency goals, (Figure 3-28) are based on information obtained from J. Benner of SERI [10]. The efficiency variation with temperature is speculative, since data is lacking at this time, and may be overly conservative. The cell parameters used for the CPS module design are listed in Table 3-64. The design was performed at a nominal operating temperature of 100°C. The peak power voltage is 1.3 V and the peak power current density is 7.73 A/cm² at 500X concentration. The rate of change of voltage with temperature was obtained from the efficiency variation and is given as -14 mV per degree C. The fractional change in current with tempera-

Table 3-61. GaAs RESIDENTIAL MODULE DATA (OPTION 2 MODULE)

MODULE ANALYSIS WORK SHEET...GA AS..FLAT PLATE 20 VOLT RESIDENTIAL							
UOC DELTA	- .0032						
W/T--U/C							
UMAX DELT	- .0032						
W/T--U/C							
ISC DELTA	.0014						
W/T--A/C							
IMAX DELT	.0014						
W/T--A/C							
NO OF CEL	24						
IN SERIES							
NO OF CEL	2						
IN //							
TCELL-TAM	25						
AT 1 SUN							
CONDITION	TAMB DEG-C	TCELL DEG-C	UOC VOLTS	ISC AMPS	UMAX VOLTS	IMAX AMPS	PMAX WATTS
LOW TEMP	-10	15	24.068	4.602	20.768	4.422	91.83610
RATED CON	0	25	23.3	4.63	20	4.45	89
S.O.C. NOCT/1000	20	45	21.764	4.686	18.464	4.506	83.19878
T=30C/86F	30	55	20.996	4.714	17.696	4.534	80.23366
T=40/104F	40	65	20.228	4.742	16.928	4.562	77.22554
T=50/122F	50	75	19.46	4.77	16.16	4.59	74.1744

Table 3-62. GaAs RESIDENTIAL SUBARRAY DC VOLTAGE WINDOW (OPTION 2 MODULE)

PV STRING VOLTAGE							
• TEMP AMS CELL	NO MODS= 9		NO MODS= 10		NO MODS= 11		
	UMAX	VOC	UMAX	VOC	UMAX	VOC	
TAMB -10 TCELL 15	186.912	216.612	207.68	240.68	228.448	264.748	
0 25	180	209.7	200	233	220	256.3	
20 45	166.176	195.876	184.64	217.64	203.104	239.404	
30 55	159.264	188.964	176.96	209.96	194.656	230.956	
40 65	152.352	182.052	169.28	202.28	186.208	222.508	
50 75	145.44	175.14	161.6	194.6	177.76	214.06	

*TEMPERATURE IS IN °C

**Table 3-63. GaAs RESIDENTIAL SUBARRAY AC POWER OUTPUT
WITH PARASITIC LOSS (OPTION 2 MODULE)**

* PV STRING POWER... $P_{OW} = P_{MOD} * N_{MOD} * N_{ALL}$

NMIS= .98MISMATCH NWIR= .98WIRE LOSS NPPT= .995PK POW TR NBODI= .997BLK DIODE NPCO= .92POW COND NALL= .8765127OVERALL			

	TEMP NO MODS=	NO MODS=	NO MODS=
	AMB 9	10	11
	CELL		

TAMB -10	724.4595	804.9551	885.4506
TCELL 15			

0	702.0867	780.0963	858.1059
25			

20	656.3231	729.2479	802.1727
45			

30	632.9324	703.2583	773.5841
55			

40	609.2025	676.8916	744.5808
65			

50	585.1332	650.1480	715.1628
75			

*POWER IS IN WATTS

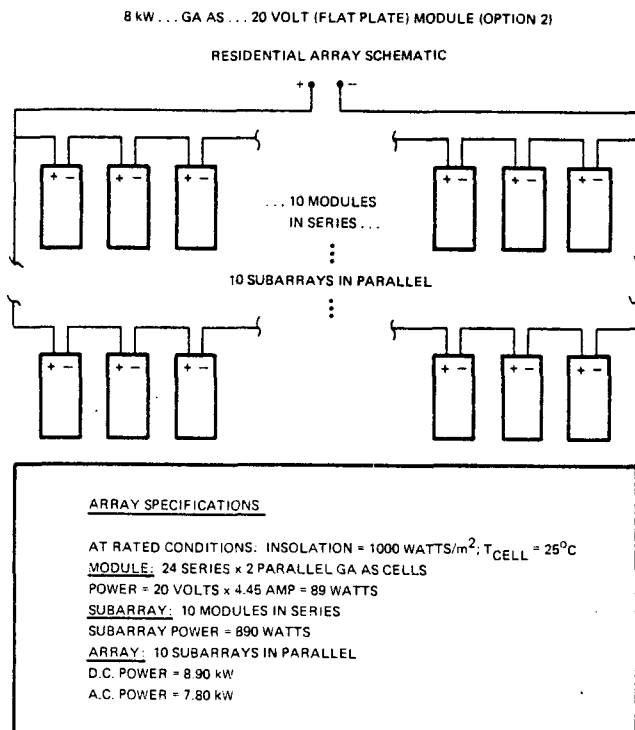
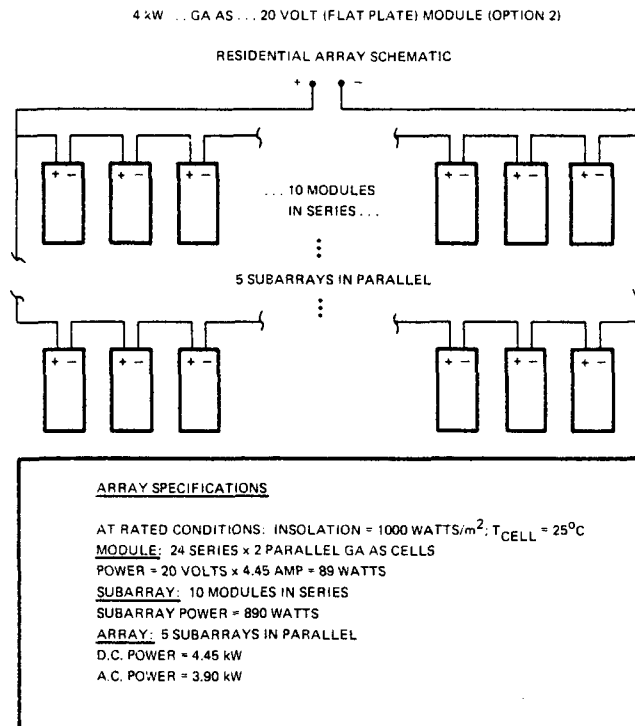


Figure 3-27. SCHEMATICS AND SPECIFICATIONS FOR 4 kW AND 8 kW GaAs ARRAYS (OPTION 2 MODULE)

ture is the same as that used for all other technologies, since data was not available for this parameter.

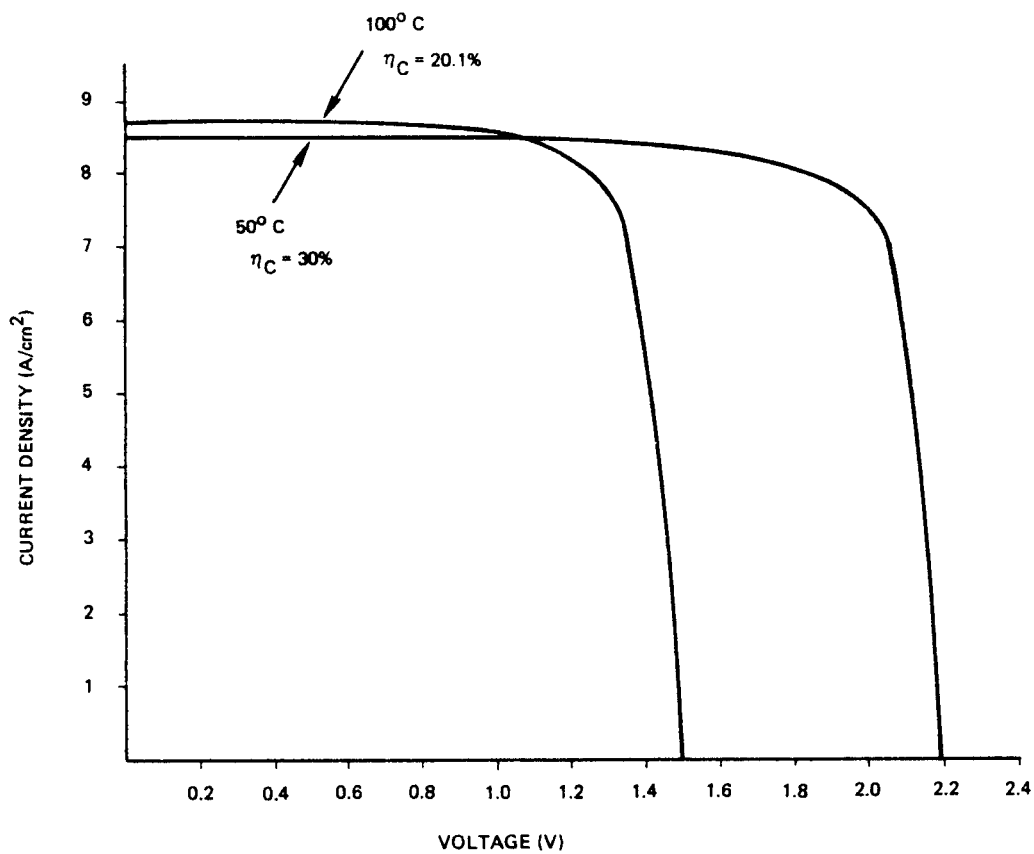


Figure 3-28. POSTULATED GaAs MULTI-JUNCTION CELL J-V CURVES

Table 3-64. GaAs CELL PARAMETERS FOR CPS MODULES

Temperature	<u>50 °C</u>	<u>100 °C</u>
$V_{OCC} =$	2.2V	1.5V
$V_{MPC} =$	2.0V	1.3V
$J_{SCC} =$	8.5A/cm ²	8.76A/cm ²
$J_{MPC} =$	7.5A/cm ²	7.73A/cm ²
FF =	0.802	0.765
$P_C =$	15W/cm ²	10.05W/cm ²
$\eta_c =$	30 percent	20.1 percent
$\Delta V / \Delta T =$	-14mV/°C	
$\Delta F_I / \Delta T =$	0.00061/°C	

3.5.2.2 CPS Module Design

The design constraints which apply to all CPS module designs were discussed in section 3.1.2 and are reproduced here in Table 3-65 for the reader's convenience. Table 3-66 presents the module design constraints which apply specifically to the GaAs CPS design. The GaAs CPS design is specified as a point-focus Fresnel lens system with 500X concentration. The maximum module dimensions are approximately 8 ft. x 12 ft. The cell dimension is specified as 0.5 in. The edge and interior spacing apply not to the cell, but to the Fresnel lens which covers the cell. The edge spacing of 1' in. applies specifically to the frame around the module. The interior spacing of 1/4 in. was designed to allow for the width of lens holders and stiffeners.

The maximum number of cells in a bypass group is five cells, based on the maximum allowable reverse cell voltage of -6.7 V. The minimum number of cells or strings in parallel is nine, based on the relationship between the short-circuit current density and the peak-power current density for cells without across-the-cell interconnects. This equation is

$$N_{MMIN} = \frac{J_{SCC}}{J_{SCC} - J_{MPC}} \quad \text{Eq. (3-4)}$$

Table 3-65. DESIGN CONSTRAINTS APPLIED TO
ALL CPS MODULE DESIGNS

- Maximum Open Circuit Module Voltage at Low Temperature

$$V_{OCM}(\text{Max}) = 150V @ - 20^{\circ}C$$

- Maximum Module Peak Power Voltage

$$V_{MPM}(\text{Max}) = 100V$$

- Acceptable Module Peak Power Voltage

$$V_{MPM} = 50V \text{ or } 100V$$

- Maximum Allowable Reverse Cell Voltage

$$V_{RMAX} = -6.7V$$

- Maximum Module Dimensions*

$$\text{Dim (Max)} = 47.5 \text{ in. X } 95.0 \text{ in. (120.65 cm x 241.3 cm)}$$

- Edge Spacing⁺

$$\Delta_{SE} = 3/8 \text{ in. (0.9525 cm)}$$

- Parallel Redundancy Desirable

- For cracked cells and broken interconnects
- Not for Cell Shadowing

- * Amorphous Silicon - 11.75 in. X 47.5 in. (29.85 cm x 120.65 cm)
- Ga As - 95.0 in. X 143.0 in. (241.3 cm x 363.2 cm)
- + Ga As - 1.0 in. (2.54 cm)

Table 3-66. GaAs DESIGN CONSTRAINTS FOR CPS MODULES

- Point Focus Fresnel Lens Design
- Maximum Module Dimensions
Dim(Max) = 95.0 in. X 143.0 in. (241.3 cm x 363.2 cm)
- Cell Diameter
 $D_C = 0.5$ in. (1.27 cm)
- Concentration
CR = 500X
- Edge Spacing
 $\Delta_{SE} = 1.0$ in. (2.54 cm)
- Interior Spacing
 $\Delta_{SI} = 1/4$ in. (0.635 cm)
- Maximum Number of Cells in Bypass Group
 $N_{BPMAX} = 5$ cells
- Minimum Number of Cells or Strings in Parallel
 $N_{MMIN} = 9$ cells

The GaAs CPS module characteristics at 100°C obtained using the module electrical design optimization methodology are listed in Table 3-67. To obtain 500X concentration with a cell diameter of 0.5 in., a circular lens of 11.18 in. may be used. The Fresnel lens design postulated here uses square lenses; thus, the dimensions of the square lens are specified as 11.18 in. for each side. The module dimensions are based on the lens arrangement rather than on the cell arrangement. With 11.18 in. lens series length, eight lenses can be arranged in the series direction to produce a module series length of 93.19 in., which is within the maximum module series length constraint of 95 in. Therefore, the bypass group is specified as four cells, which is within the maximum bypass group constraint of five cells. Two bypass groups are placed in series in the series direction, as illustrated in Figure 3-29, which diagrams the GaAs CPS module design. The series connection of cells is snaked five times to obtain a nominal 52 V at peak power. Because the lens parallel length is fixed at 11.18 in., only two cells can be paralleled in each bypass group without exceeding the maximum module parallel length of 143 in. Therefore, 10 lenses are arranged in the parallel module direction, resulting in a parallel module length of 116.05 in.

The packing factor of 0.726 was obtained by multiplying the cell area by the concentration ratio and by the number of cells in the module and dividing by the total module area. Therefore, the use of circular cells is the main contributing factor to the low packing factor of 0.726 since, for a conservative concentration design, only the circular portion of each lens is considered to contribute to the concentration. The module efficiency of 14.59 percent is then obtained by multiplying the cell efficiency by the packing factor.

3.5.2.3 CPS System Design

Following the system design methodology discussed in section 3.1.3.2, the voltage and power of the module as a function of expected cell temperatures are presented in Table 3-68, using voltage variation with temperature of $-0.014\text{V}/^\circ\text{C}$ and current variation with temperature of $.00519\text{ A}/^\circ\text{C}$. The nominal cell temperature is 100°C.

Table 3-69 lists the DC voltage variations with temperature for series string options of 19, 20, and 21 modules, respectively. The 20-module option matches the nominal system voltage constraint of 1000 V at 25°C. None of the module options satisfy the voltage window constraint of 800 to 1300 V DC because of the high $\Delta V/\Delta T$ specified. As previously mentioned, however, this value is highly speculative and may be overly conservative. The AC power variations with temperature are presented in Table 3-70. The 20-module string produces an AC power of 17.85 kW at 100°C. This option can be paralleled 112 times to obtain the minimum subarray AC power of 2.0 MW.

Table 3-67. GaAs CPS MODULE DESIGN AT 100°C

- Fresnel Lens Dimensions

$$L_{CS} \times L_{CP} = 11.18 \text{ in.} \times 11.18 \text{ in.} = 125.0 \text{ in.}^2 \text{ (80.65 cm)}$$

- Bypass Group and Parallel Redundancy

- $N_{BP} = 4 \text{ cells}$

- $N_M = 2 \text{ cells}$ (Parallel Redundancy not required)

- Module Dimensions

- $L_{MS} \times L_{MP} = 93.19 \text{ in.} \times 116.05 \text{ in.}$ (236.7 cm x 294.8 cm)

- 8 in. S-direction x 10 in. P-direction

- Packing Factor = 0.726

- Module Electrical

- 40 Series X 2 Parallel

- $V_{OCM} = 60.0V$, $V_{MPM} = 52.V$

- $I_{SCM} = 22.2A$, $I_{MPM} = 19.58A$

- $P_M = 1018.2W$, $\eta_M = 14.59 \text{ percent}$

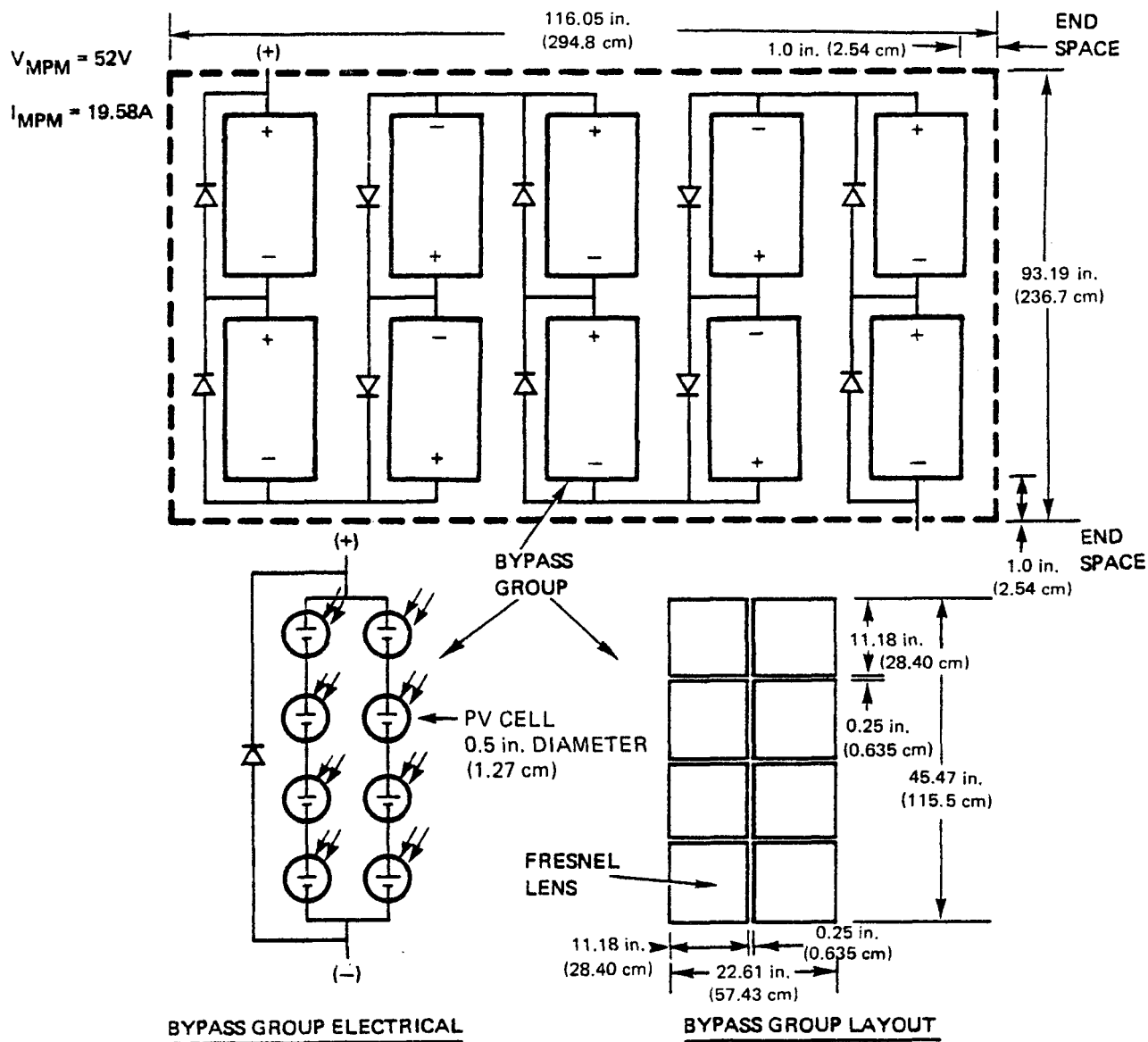


Figure 3-29. GaAs 500X CPS MODULE

Table 3-68. GaAs CPS MODULE DATA

MODULE ANALYSIS WORK SHEET...GA AS..CONCENTRATOR CENTRAL POWER STATION

VOC DELTA -.014
 W/T--U/C
UMAX DELT -.014
 W/T--U/C
ISC DELTA .00519
 W/T--A/C
IMAX DELT .00519
 W/T--A/C
NO OF CEL 40
IN SERIES
NO OF CEL 2
 IN //

CONDITION	TCELL DEG-C	VOC VOLTS	ISC AMPS	UMAX VOLTS	IMAX AMPS	PMAX WATTS
LOW TEMP	50	88	21.691	80	19.061	1524.88
- 20 %	80	71.2	21.9924	63.2	19.3724	1224.336
RATED CON	100	60	22.2	52	19.58	1018.16
+ 20 %	120	48.8	22.4076	40.8	19.7876	807.3341

Table 3-69. GaAs CPS STRING DC VOLTAGE WINDOW

PV STRING VOLTAGE						
* TEMP	NO MODS= 19		NO MODS= 20		NO MODS= 21	
CELL	UMAX	UOC	UMAX	UOC	UMAX	UOC
50	1520	1672	1600	1760	1680	1848
80	1200.8	1352.8	1264	1424	1327.2	1495.2
100	988	1140	1040	1200	1092	1260
120	775.2	927.2	816	976	856.8	1024.8

*TEMPERATURE IS IN °C

**Table 3-70. GaAs CPS STRING AC POWER OUTPUT
WITH PARASITIC LOSSES**

 • PV STRING POWER... $POW = PMOD * NMOD * NALL$

NMIS= .98MISMATCH
 NMIR= .98WIRE LOSS
 NPPT= .995PK POW TR
 NBDIO= .997BLK DIODE
 NPCO= .92POW COND
 NALL= .8765127OVERALL

	TEMP NO MODS= 19	NO MODS= 20	NO MODS= 21
CELL			
50	25394.98	26731.53	28068.11
80	20389.77	21462.92	22536.06
100	16958.17	17848.60	18741.03
120	13445.13	14152.77	14880.41

*POWER IS IN WATTS

In Figure 3-30, the 50 MW GaAs concentrating CPS array is shown to consist of 25 subarrays of 2 MW each connected in parallel. Each 2 MW subarray consists of 20 modules connected in series to obtain a nominal 1,000 V and 112 series strings connected in parallel. There are two modules per pedestal; therefore, the 2 MW subarray contains 1120 pedestals. The subarray will produce 2.28 MW of DC power. With the power conditioning component efficiency of 0.8765, the AC power thus produced is 2.00 MW.

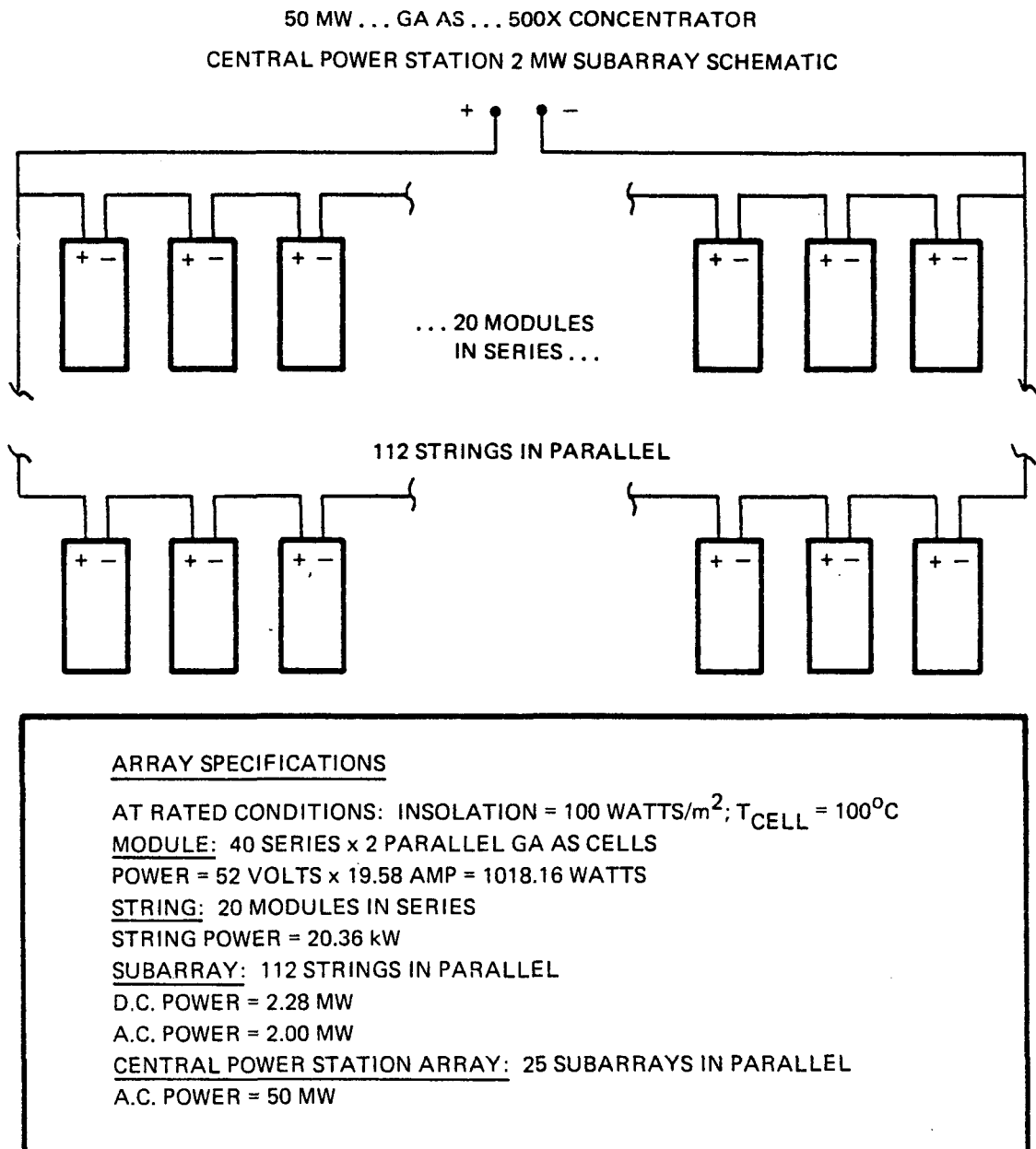


Figure 3-30. SCHEMATIC AND SPECIFICATIONS FOR 50 MW GaAs CENTRAL POWER STATION



SECTION 4.0

CONCEPTUAL DESIGN ANALYSIS

Based on the conceptual designs of modules and systems developed for advanced PV technologies, PV-TAP and SOLCEL II models were developed and validated. Module and system cost/performance evaluations were performed based on these models. The evaluation plan is diagrammed in figure 4-1. Analyses performed using PV-TAP assessed the output variation with insolation and temperature extremes and the power loss with cell-to-cell photocurrent (IP) variation. PV-TAP analyses also addressed cell reliability by quantifying the cell heating due to shadow-induced reverse bias.

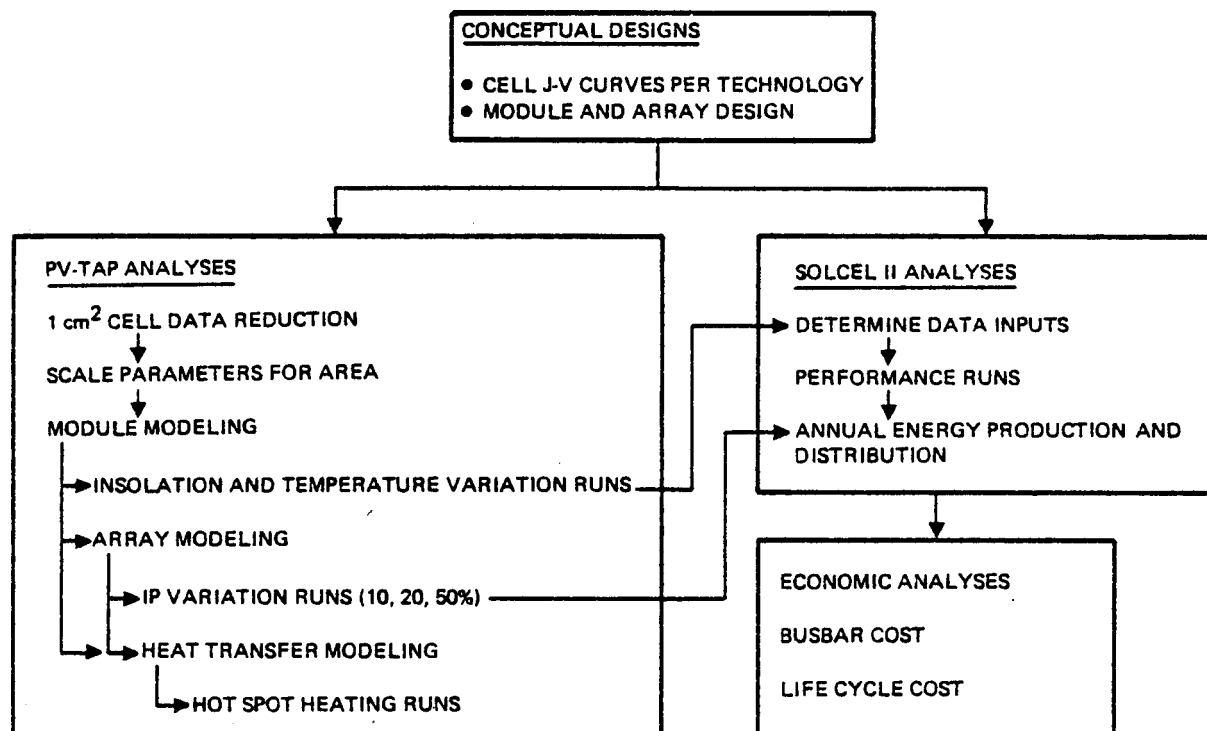


Figure 4-1. EVALUATION FLOW CHART FOR EACH ADVANCED PV SYSTEM APPLICATION

The evaluation plan also includes assessment of system annual performance using SOLCEL II and system economic analyses using the SOLCEL II Life Cycle Costing methodology. In addition to data from the module and systems designs, the SOLCEL II analyses also require that module current and voltage values at extremes of temperature and insolation be obtained from the AC

energy wasted or sold to the utility. The SOLCEL II performance results are scaled based on the PV-TAP IP variation analyses results.

The economic analysis used the Life Cycle Cost (LCC) methodology incorporated in the SOLCEL II model. The SOLCEL II model has been expanded to include the financial benefits associated with selling excess energy back to the electric utility. Published cost projections for PV modules and Balance of System (BOS) costs have been used to project the LCC of each of the Advanced PV Systems. These cost projections include: system peak output proportional costs; array area proportional costs; and array FOB costs/pW. The implication of this analytical approach is that PV module efficiency is the determining factor for relative system cost effectiveness. Levelized cost projections have been made for total system costs, cost per kWh of electricity generated by the PV system, and the break-even cost of conventional energy.

The PV-TAP analyses for each technology application are presented in Section 4.1. In performing computer analyses, the problem must first be formulated (or modeled) in the language of the computer code input format. Then, the models must be validated by comparison with data to ensure the correctness of the modeling and to determine the accuracy (or deviation from the data) of the calculations. The PV-TAP modeling procedures are discussed in Section 4.1.1; then, the results of the model validation and a cataloguing of inputs for each technology are presented in Section 4.1.2; finally, the results of the PV-TAP analyses are presented and discussed in Section 4.1.3. The SOLCEL II analyses are presented in Section 4.2. First, the SOLCEL II modeling and validation is discussed (Section 4.2.1); then, the inputs for each technology are catalogued (Section 4.2.2); finally, the results are presented and discussed (Section 4.2.3). The economic analyses are presented and discussed in Section 4.3. First, the input parameters are presented (Section 4.3.1); then, the methodology and results of the residential analyses are presented (Section 4.3.2); finally, the methodology and results of the CPS analyses are presented (Section 4.3.3).

4.1 PV-TAP ANALYSES

PV-TAP is an electrical circuit analysis code developed by BDM to simulate the electrical performance of photovoltaic cells, modules, and arrays. It is very flexible and can be used to perform many different types of analyses, e.g., analysis of the effects of statistical variations in cell short-circuit currents on the electrical output of arrays, and verification that temperature increases in a shadowed cell are not excessive.

4.1.1 Modeling and Validation Procedures

Figure 4-2 diagrams the PV-TAP modeling and validation process. First, the postulated 1 cm² cell data was reduced using the data reduction feature in

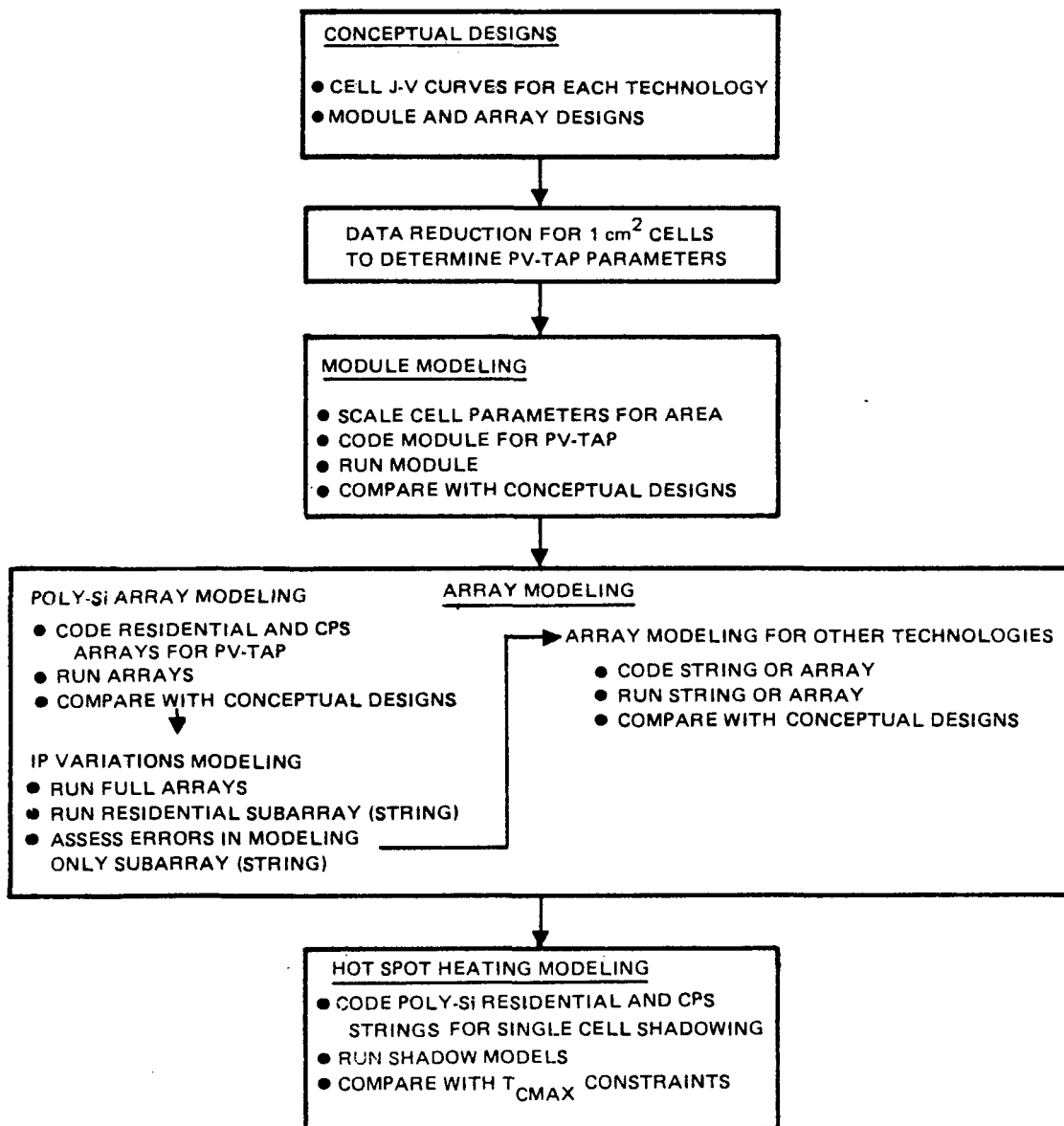


Figure 4-2. FLOW CHART FOR PV-TAP MODELING

PV-TAP [39] which determines the Ebers-Moll parameters required for PV cell modeling from I-V curve data. The data reduction is discussed in Section 4.1.1.1 which also contains an explanation of PV-TAP format and code features.

Next, the cell parameters were scaled to the areas of the cells used in each of the modules and the modules were modeled on PV-TAP. Rather than specify each cell in the module individually, the PV aggregate model was used to specify an entire bypass group with its parallel strings as a single element. It is preferable not to aggregate beyond the bypass level because the action of the bypass diode will be lost. The module models were run and the results compared with the designs. The module modeling is discussed in Section 4.1.1.2.

The array modeling involved several steps. The residential and CPS arrays for the polycrystalline silicon technology were modeled and run. Photocurrent variations were run on the residential array and on a single string to assess the errors which might be introduced because the CPS array could not be modeled in its entirety in a single run. Because the systems for the other technologies will be built up in the same way, the polycrystalline array system will serve for modeling validation. Photocurrent variation modeling on the polycrystalline CPS array was also demonstrated. Finally, the arrays for the other technologies were modeled and run on PV-TAP. The array modeling is discussed in Section 4.1.1.3.

The last PV-TAP modeling performed was hot spot heating due to shadowing of a single cell. This modeling was demonstrated using the polycrystalline residential and CPS series strings with one cell specified independently for shadowing. The format for the modeling is discussed in Section 4.1.1.4.

4.1.1.1 PV Cell Data Reduction

The inputs required to run the data reduction feature in PV-TAP and the outputs obtained from it are listed in Table 4-1. The minimum set of inputs required are the cell short circuit current (ISC), the shunt conductance (G) (inverse of shunt resistance), the cell temperature (TEMP) and I-V curve point pairs. The voltage and current temperature coefficients (DVDT and DIDT) may also be input to obtain more accurate temperature modeling than that obtained from the code default conditions. The cell photocurrent (IP) is not used for data reduction but is required if an I-V curve obtained from the resultant parameters is to be plotted. Weighting factors may be placed on each of the point pairs to assign more importance to selected points on the I-V curve.

The program calculates the temperature independent saturation current constant (IS), the emission constant or ideality factor (M), the series resistance (RS), and the saturation current temperature parameters (P and ALPHA). The program also provides a comparison of calculated currents with

the currents from the input data. The user also has the option to perform a state solution run which will generate an I-V curve from the cell parameters. These cell data reduction features are illustrated in the following tables and figure for a polycrystalline silicon PV cell.

Table 4-1. PV CELL DATA REDUCTION INPUTS/OUTPUTS

INPUTS

- Short Circuit Current - ISC
- Shunt Conductance - G
- Cell Temperature - TEMP
- Cell Photocurrent - IP
- Voltage-Temperature Coefficient - DVDT
- Current-Temperature Coefficient - DIDT
- I-V Point Pairs - V, I, Wt.

OUTPUTS

- Saturation Current Constant - IS
- Emission Constant - M
- Series Resistance - RS
- Exponent of Temperature - P
- Temperature Coefficient - ALPHA
- Comparison of Currents at Input Voltages

A listing of the PV-TAP input for the polycrystalline silicon cell data reduction is shown in Table 4-2. The PV-TAP inputs are in the form of an outline so that subordinate data is indented as seen in the table entries in lines 25-30. In line 3, the PV cell is given the device name "PSIO1". The model number within PV-TAP for a PV cell is 11. Data reduction is performed under the "LIBRARY" entry (lines 3-14) by specifying voltage-current point-pairs following the "DATA DC" line, which keys the data reduction process. The recommended (though not mandatory) set of units for PV-TAP is volts, milliamps, kilohms, degrees Kelvin, etc. Weighting factors of 1.0 and .1 were placed on the points to assign more importance to the peak power point and the open circuit voltage. In addition to performing data reduction, the "LIBRARY" entry is also used for inputting fixed parameters for devices as illustrated in lines 15-18 for a bypass diode.

The inputs in lines 19 through 35 produce a state solution which calculates the current and voltage of the cell from short circuit to open circuit load conditions by varying the load resistance (R1L). The PV cell is

Table 4-2. POLYCRYSTALLINE SILICON CELL DATA REDUCTION INPUT LISTING

```

1      * 1CM SQUARE POLY-SI CELL
2      LIBRARY
3          PV PSIO1 11
4              G 1
5              IP 25.0
6              TEMP 298
7              ISC 25.0
8              DVDT -.0022
9              DIDT 1.53E-2
10             DATA DC
11                 .45 24.1 .1
12                 .5 23 1
13                 .55 17.3 .1
14                 .6 0.0 1
15             D BPD1 1
16                 RB 1E-4
17                 IS 8.24E-6
18                 TH 20.
19     PVA1 1 0 S T P PSIO1 0,0,0,0,0,S1
20     VIS S 0 1.0
21     VIT T 0 298
22     DIBP 0 1 BPD1
23     R1L 1 0 .08
24     X1=TABLE1(V(R1L))
25     TABLE1
26         0.0 25.0
27         .45 24.1
28         .50 23.0
29         .55 17.3
30         .6 0.0
31     STATE1
32         R1L 1E-6 1E-5 1E-4 1E-3$
32     1E-2 (9) 2E-2 (20) 3E-2 (7) 1E-1 1 10 100
33         PRINT V(R1L) I(R1L) X1 P(R1L) N(1)
34         PLOT X1 I(R1L) VS V(R1L)
35     END

```

specified in line 19. It is connected between node 1 and 0 and receives insolation and temperature through nodes S and T, respectively. P is the power dissipation output node. The cell parameters are obtained from the PSI01 device. The first four zeros indicate no parasitic impedance and the last zero indicates no parameter distribution. The S1 designation indicates a single cell rather than a combination of cells.

The insolation and temperature are input by specifying voltage sources of 1.0 suns and 298°K, respectively. Specifying the insolation between nodes S and 0 connects this voltage source to the S node of the PV cell; the same is done for the T nodes. A bypass diode (line 22) is connected across the PV cell. It has no effect on this run, however. RLL is the load resistance which has an initial value of 0.08 k Ω . The table (X1) in lines 24-30 is a repeat of the input data and is used to plot the original data.

The STATE1 entry prefaces the state solution run controls. RLL is swept from short circuit to open circuit conditions to produce a full set of I-V values. An overlay of the input data with calculated I-V values will be produced by the plotrequest in line 34. Note that the dollar sign (\$) is used as a line continuation symbol so that line 32 actually consists of two lines.

Table 4-3 presents the PV-TAP listings of current comparisons at the input voltages and the final cell parameters resulting from the data reduction. The calculated current at the peak power voltage (0.5V) is within 0.09 percent of the original current.

All the parameters assigned to device PSI01 are listed. Default values are assigned to those parameters not calculated or specified in the device library entry. ISC, TEMP, DVDT, and DIDT are not listed because they are not PV cell model parameters but are only used for data reduction. IS is the temperature-independent saturation current. The saturation current at 298°K determined from IS, P, and ALPHA is 2.18E-5 mA.

The parameters calculated from data reduction are followed by goodness-of-fit data in parentheses. These values assess the ability of the parameters to match all the input point-pairs. Note that the deviations on IS and RS are greater than the parameter values indicating that the I-V curve postulated through the VOCC, JSCG, and VMPC-JMPC points in Section 3.2.1 (Figure 3-6) did not closely match the exponential model. In spite of the large values in the goodness-of-fit data, the curves in the PV-TAP comparison plot for the polycrystalline silicon cell shown in Figure 4-3 compare well. But the comparison is actually better than shown since the Xs are plotted from a table which uses linear interpolation between table values. The open circuit voltage is the same as in the data (0.60V) and, as stated above, the peak power current is within 0.09 percent of the data.

The plot shown in Figure 4-3 results from the state solution run controls. The Xs represent the original data from X1 = TABLE1 and the Is are the calculated currents. The x-axis is labeled from 0.0 to 0.6V across the load

**Table 4-3. POLYCRYSTALLINE SILICON CELL CURRENT COMPARISON
AND PARAMETER LISTING**

DATA REDUCTION TYPE DC FOR PSIO1

TERMINAL VOLTAGE	CURRENT	
	EXPERIMENTAL	CALCULATED

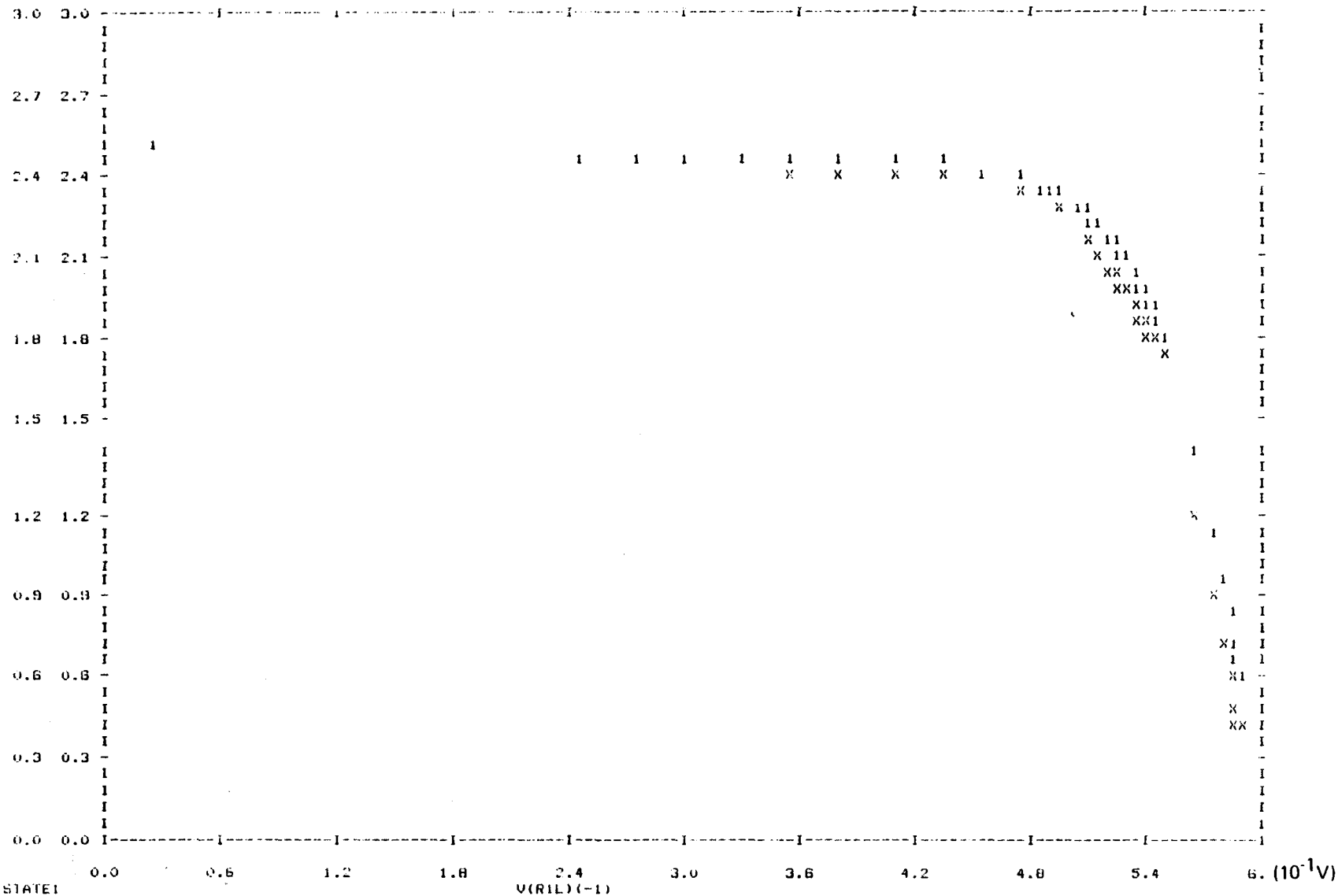
.4500E+00	.2410E+02	.2421E+02
.5000E+00	.2300E+02	.2298E+02
.5500E+00	.1730E+02	.1786E+02
.6000E+00	0.	-.1562E-01

1

LIBRARY VALUES AFTER COMPLETION OF DATA REDUCTION

TYPE	PREFIX	MODEL	
PSIO1	PV	11	PHOTOVOLTAIC CELL
G	1.000000+000		
IS	8.757990+002	(9.25+003)	
M	1.271214+000	(3.09-001)	
VZ	1.100000+000		
N	5.000000-001		
C	1.500000+006		
W	2.000000-005		
A	1.500000+001		
VB	-3.500000+001		
B	1.000000+000		
RS	4.015096-004	(9.41-004)	
IP	2.500000+001		
KSC	4.500000+003		
T	5.000000+004		
CS	0.000000+000		
CST	0.000000+000		
CT	0.000000+000		
CTT	0.000000+000		
P	2.359949+000	(5.74-001)	
SR	1.000000+000		
TR	2.980000+002		
ETA	1.000000+000		
GK	1.160000+004		
ALPHA	1.054840+004	(2.68+003)	

X1 I(R1L)
(10¹ mA)



STATE1
* 1CM SQUARE POLY-SI CELL
VARIABLE
X1(+1)
I(R1L)(+1)

Figure 4-3. POLYCRYSTALLINE SILICON CELL DATA REDUCTION I-V PLOT

resistor (R1L). The y-axis scales are 0.0 to 30 mA for each. The y-axis variables are listed by the program in the lower left of the figure.

The PV-TAP plotting routine produces a value for each variable at each voltage obtained. Therefore, there should be as many Xs as 1s. The lack of Xs at some of the voltages which display 1s indicates that the values are nearly identical so that PV-TAP can not discriminate them and plots only the higher symbol, the 1.

4.1.1.2 Module Modeling

The schematic shown in Figure 4-4 illustrates the principles of the module and array modeling exemplified by the polycrystalline silicon residential application. The module modeling is shown in the module inset. The array modeling principles will be discussed in Section 4.1.1.3. Table 4-4 lists the features of the input format for module modeling. For all applications a bypass group is specified by a single PV aggregate model. The designation S10P4 indicates 10 cells connected in series with four of these series strings connected in parallel. A bypass diode is placed across each bypass group. Insolation and temperature inputs to the PV aggregate models are accomplished with voltage sources and an I-V curve for the module is produced by varying the load resistance across the module.

Table 4-4. MODULE MODELING AND VERIFICATION FORMAT

SAME FOR ALL MODULES

- Bypass group specified by PV Aggregate model
- Bypass diode across each bypass group
- Insolation and temperature input to aggregate with voltage sources
- Module I-V curve produced by varying load resistance in DC state solution

VARIES WITH APPLICATION

- Series/parallel interconnection of cells in bypass group
- Number of bypass groups (N_G) connected in series
- Cell parameter values
- Insolation = 1 Sun for flat plate
= 500 Suns for concentrator
- Cell Temperature = 298°K (25°) for flat plate
= 373°K (100°C) for concentrator

For each different module the number of cells connected in series and parallel in a bypass group and the number of bypass groups connected in

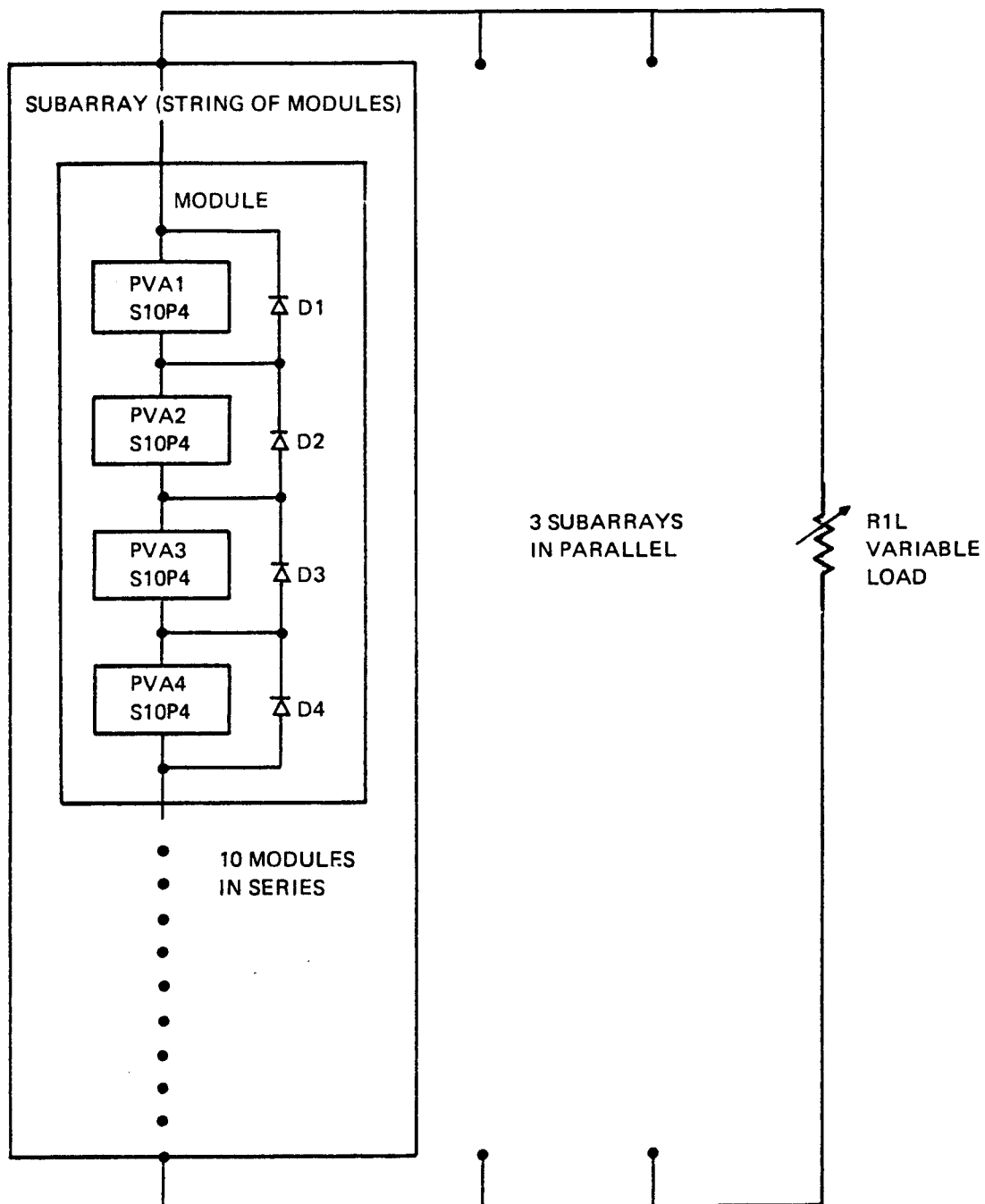


Figure 4-4. MODULE AND ARRAY MODEL FOR POLYCRYSTALLINE SILICON RESIDENTIAL APPLICATION

series in the module will be different. The cell parameter values will vary from module to module depending on the cell technology and the area of the cell. Standard insolation for modeling flat plate modules is 1 sun and for the concentrator application is 500 suns. The flat plate modules are modeled at 298°K which corresponds to 25°C and the concentrator module is modeled at 373°K corresponding to 100°C. The effects on the output power due to variations in temperature or insolation on the entire module can be evaluated by substituting different values as inputs to the PV model.

The PV-TAP model listing of the polycrystalline silicon residential module is shown in Table 4-5. The area-dependent parameters have been scaled for the 85.1 cm² cell area. The parameter, CT, represents the dependence of the short circuit current on temperature. It is the fractional change in current, $\Delta I_T/\Delta T$, listed in Section 3.2.1

The module is defined in lines 16 through 26. PVA1 through PVA4 are PV aggregate cells. The entry "S10P4" indicates 10 cells connected in series by 4 series strings connected in parallel. The first four zeros indicate that wiring and parasitic impedances are not desired. The last zero represents the distribution entry. The zero indicates that all parameters in the 40 cell aggregate are identical. If a distribution is desired for a parameter, a distribution entry called "AGGREGATION" is included somewhere in the input at the column one level and the number of the distribution is entered in the PV aggregate model in place of the zero. An example of an aggregation entry is shown below.

```
AGGREGATION2
      IP GAUSS 1.92E3
```

In this example, the aggregation entry is identified by the number 2 and the IP distribution is gaussian with a lower 3-sigma value of 1.92E3 mA. The nominal value is 2.13E3 mA determined by the library entry on line 9.

In lines 27 and 28, one module is connected to a load resistor which will be swept through the values in line 30. Note the use of the dollar sign (\$) as a line continuation symbol for lines 30 and 31. Line 32 will produce I-V and power curves on the same plot as illustrated in Figure 4-5. The open circuit voltage is the same as in the conceptual design (24.0V). The peak power is 156.5W compared with 156W in the design.

4.1.1.3 Array Modeling

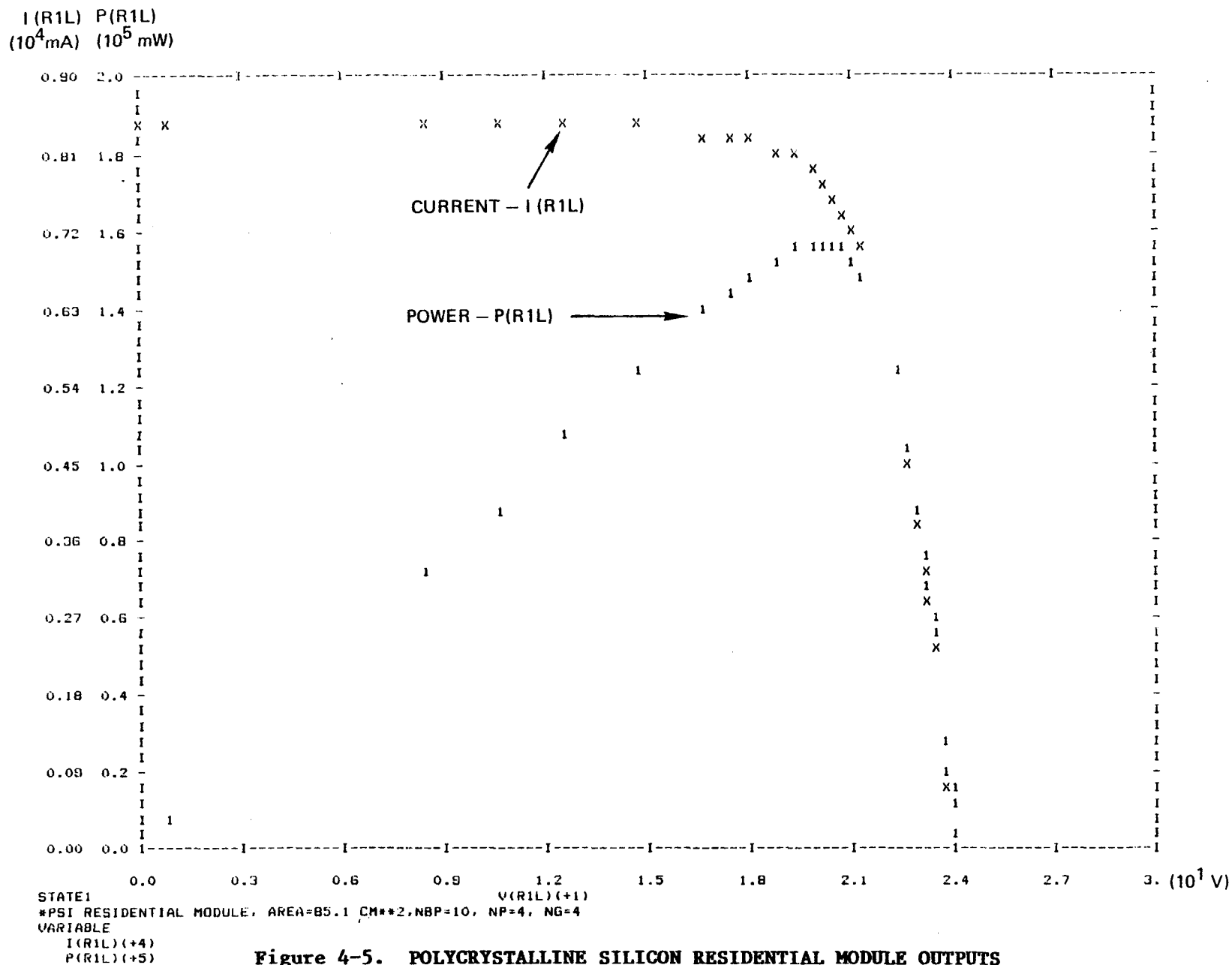
Referring back to Figure 4-4, the array model can be seen to be a logical extension of the module model. In general, modules are connected in series to form a series string of the desired voltage. Then series strings are connected in parallel to obtain the desired array power. In the case of the polycrystalline silicon residential application, ten modules are connected in series to form the series string and three strings or subarrays are connected

Table 4-5. POLYCRYSTALLINE SILICON RESIDENTIAL MODULE COMPUTER MODEL

```

1  *PSI RESIDENTIAL MODULE, AREA=85.1 CM**2,NBP=10, NP=4, NG=4
2  LIBRARY
3      PV PSI01 11
4          M 1.271214
5          P 2.359949
6          ALPHA 1.05484E4
7          CT .00061
8          G 85.1
9          IP 2.13E3
10         IS 7.45E4
11         RS 4.72E-6
12     D BPD1 1
13         RB 1E-4
14         IS 8.24E-6
15         TH 20.
16     DEFINE MODULE POS NEG 0
17         PVA1 POS 1 S T P1 PSI01 0,0,0,0,0,S10P4
18         PVA2 1 2 S T P2 PSI01 0,0,0,0,0,S10P4
19         PVA3 2 3 S T P3 PSI01 0,0,0,0,0,S10P4
20         PVA4 3 NEG S T P4 PSI01 0,0,0,0,0,S10P4
21         D1BP 1 POS BPD1
22         D2BP 2 1 BPD1
23         D3BP 3 2 BPD1
24         D4BP NEG 3 BPD1
25         VIS S 0 1.0
26         VIT T 0 298
27     MODULE1 1 0 0
28     R1L 1 0 .08
29     STATE1
30         R1L 1E-6 1E-5 1E-4 1E-3$
31         (4) 2E-3 (10) 3E-3 (7) 1E-2$
32         (4) 5E-2 1E-1 1 10 100
33         PRINT V(R1L) I(R1L) P(R1L)$
34     V(MODULE1.PVA1) V(MODULE1.PVA2) V(MODULE1.PVA3) V(MODULE1.PVA4)
35     PLOT I(R1L) P(R1L) VS V(R1L)
36     END

```



in parallel to form the full array. The model is run by placing a load resistance across the array and varying it to produce an I-V curve.

The short circuit current will vary for different cells of the same size and technology. These variations can be modeled statistically with PV-TAP. After the type of distribution is given, an actual distribution is calculated on the basis of parameters supplied. Then PV-TAP randomly assigns a cell short-circuit current to each cell, based on the distribution calculated. The calculation of the electrical performance of an array then proceeds as usual. For this analysis, a Gaussian distribution was chosen. A number representing the short circuit current that is the third standard deviation from the mean (either higher or lower than the mean) is needed by PV-TAP to determine the distribution. The mean of the distribution is the nominal value used in the cases with identical cells.

The full polycrystalline silicon residential array was easily run on the SERI computer. However, the CPS array exceeded the core limits of the small core memory on the SERI computer. Therefore, the CPS array was modeled as a single string with a parallel segment designation. This designation permits PV-TAP to simply multiply the current and power of the string by the number of strings in parallel. This is illustrated in Table 4-6 which contains the input listing for the polycrystalline silicon CPS array. A string of 20 series connected modules is defined as a model called SUB in lines 39 through 59. In line 60 one model SUB is replicated 362 times by the parallel segment designator in the parentheses.

Although the paralleling technique will produce an exact solution for the case of identical cells, it introduces an error into the calculation of the array characteristics under photocurrent variation conditions. Although each cell in the series string will have a different photocurrent value, all 362 strings will have the same resultant aggregate photocurrent. This is contrasted with the exact solution for the residential application which contains only three series strings. Since each of these three strings, however, is specified as a separate SUB element, each of the strings will have a different aggregate photocurrent. To assess the errors introduced by this modeling technique, the polycrystalline silicon residential array was run for photocurrent variations with both the full array and with the string with parallel segment designator. The results of this modeling are presented in the PV-TAP array modeling results in Section 4.1.2.3. Based on this error assessment the remaining array applications were modeled using the parallel segment designator.

4.1.1.4 Hot Spot Heating

Hot spot heating can be satisfactorily modeled with a series string of modules rather than the full array. The worst hot spot heating occurs when a single cell in a string is partially shadowed so that it is not only heated due to reverse bias but also due to incident sunlight. A schematic illus-

Table 4-6. POLYCRYSTALLINE SILICON CPS 2MW SUBARRAY COMPUTER MODEL

```

1      * CPS PSI SUBARRAY
2      LIBRARY
3      PD PSI01 11
4          M 1.271214
5          P 2.38554E
6          ALPHA 1.05404E4
7          CT .00081
8          G 91.5
9          IP 2.29E3
10         IS 8.01E4
11         RS 4.39E-6
12     D BPD1 1
13         RB 1E-4
14         IS 8.24E-6
15         TH 20.
16     DEFINE MODULE POS NEG 0
17         PVA1 POS 1 S T P1 PSI01 0.0.0.0.0.S10P3
18         PVA2 1 2 S T P2 PSI01 0.0.0.0.0.S10P3
19         PVA3 2 3 S T P3 PSI01 0.0.0.0.0.S10P3
20         PVA4 3 4 S T P4 PSI01 0.0.0.0.0.S10P3
21         PVA5 4 5 S T P5 PSI01 0.0.0.0.0.S10P3
22         PVA6 5 6 S T P6 PSI01 0.0.0.0.0.S10P3
23         PVA7 6 7 S T P7 PSI01 0.0.0.0.0.S10P3
24         PVA8 7 8 S T P8 PSI01 0.0.0.0.0.S10P3
25         PVA9 8 9 S T P9 PSI01 0.0.0.0.0.S10P3
26         PVA10 9 NEG S T P10 PSI01 0.0.0.0.0.S10P3
27         D18P 1 POS BPD1
28         D28P 2 1 BPD1
29         D38P 3 2 BPD1
30         D48P 4 3 BPD1
31         D58P 5 4 BPD1
32         D68P 6 5 BPD1
33         D78P 7 6 BPD1
34         D88P 8 7 BPD1
35         D98P 9 8 BPD1
36         D108P NEG 9 BPD1
37         V1S S 0 1.0
38         V1T T 0 298
39     DEFINE SUB A B 0
40         MODULE1 A 1 0
41         MODULE2 1 2 0
42         MODULE3 2 3 0
43         MODULE4 3 4 0
44         MODULE5 4 5 0
45         MODULE6 5 6 0
46         MODULE7 6 7 0
47         MODULE8 7 8 0
48         MODULE9 8 9 0
49         MODULE10 9 10 0
50         MODULE11 10 11 0
51         MODULE12 11 12 0
52         MODULE13 12 13 0
53         MODULE14 13 14 0
54         MODULE15 14 15 0
55         MODULE16 15 16 0
56         MODULE17 16 17 0
57         MODULE18 17 18 0
58         MODULE19 18 19 0
59         MODULE20 19 20 0
60     SUB1 (3G2) 1 0 0
61     R1L 1 0 .08
62     STATE1
63         R1L 1E-6 1E-5 1E-4 (12) 4E-4 (20) 5E-4*
64         (20) 1E-3 (9) 1E-2 1E-1 1 10 100
65     PRINT MODULE1 (R1L) PERIOD

```

trating the principles of the hot spot heating modeling is detailed in Figure 4-6. A polycrystalline silicon residential application is used as an example in this figure. The string of modules was represented by five aggregate PV cells. The formulas for the sequences specified for PVA1 through PVA5 are given in Table 4-7 for all technologies and applications except for GaAs residential. Here, a is the number of modules in the series string of an array of a specific technology and application, b is the number of cells in a bypass group within a module, c is the number of such groups in parallel, and d is the number of such parallel combinations in series in the module.

The formulas specify that for PVA1 there are b cells in series first, then c such groups in parallel, then (a-1)d such parallel sets in series. The reason for this is that one cell of one module must be specified differently than all the other cells of that module and all other modules. Thus, one module of the string must be modeled differently, hence the a-1 term is PVA1. PVA2, PVA3, PVA4, and PVA5 are used to describe the final module. PVA2 describes all except one of the series sets of parallel strings. All of these have identical cells. This results in the d-1 term in PVA2. Of the remaining set, all except one of the parallel strings are identical. The one containing the cell to be shadowed is different, thus the c-1 term for PVA3. Now there is one bypass group left. All of the cells except one are not shadowed, resulting in the b-1 term in PVA4. The single shadowed cell is thus described as simply one cell in series in PVA5.

Table 4-7. FORMULAS FOR THE DETERMINATION OF SEQUENCES USED TO SPECIFY AGGREGATE PV CELLS TO PV-TAP FOR THE HOT-SPOT HEATING RUNS (EXCEPT FOR GaAs RESIDENTIAL APPLICATIONS)

PVA1	$Sb P_c S(a-1) \times d$
PVA2	$Sb P_c S(d-1)$
PVA3	$Sb P (c-1)$
PVA4	$S(b-1)$
PVA5	$S1$

The gallium arsenide residential module series string can be explained by an identical reasoning, except that cells are first connected in parallel before being connected in series in a bypass group; hence, the specifications begin with P instead of S for PVA1 through PVA3.

Returning to the polycrystalline silicon residential application in Figure 4-6, all the modules but one are combined into the single element, PVA1. In this case, nine modules are combined into PVA1. Each of the nine modules contains four bypass groups connected in series; thus, the designation S36.

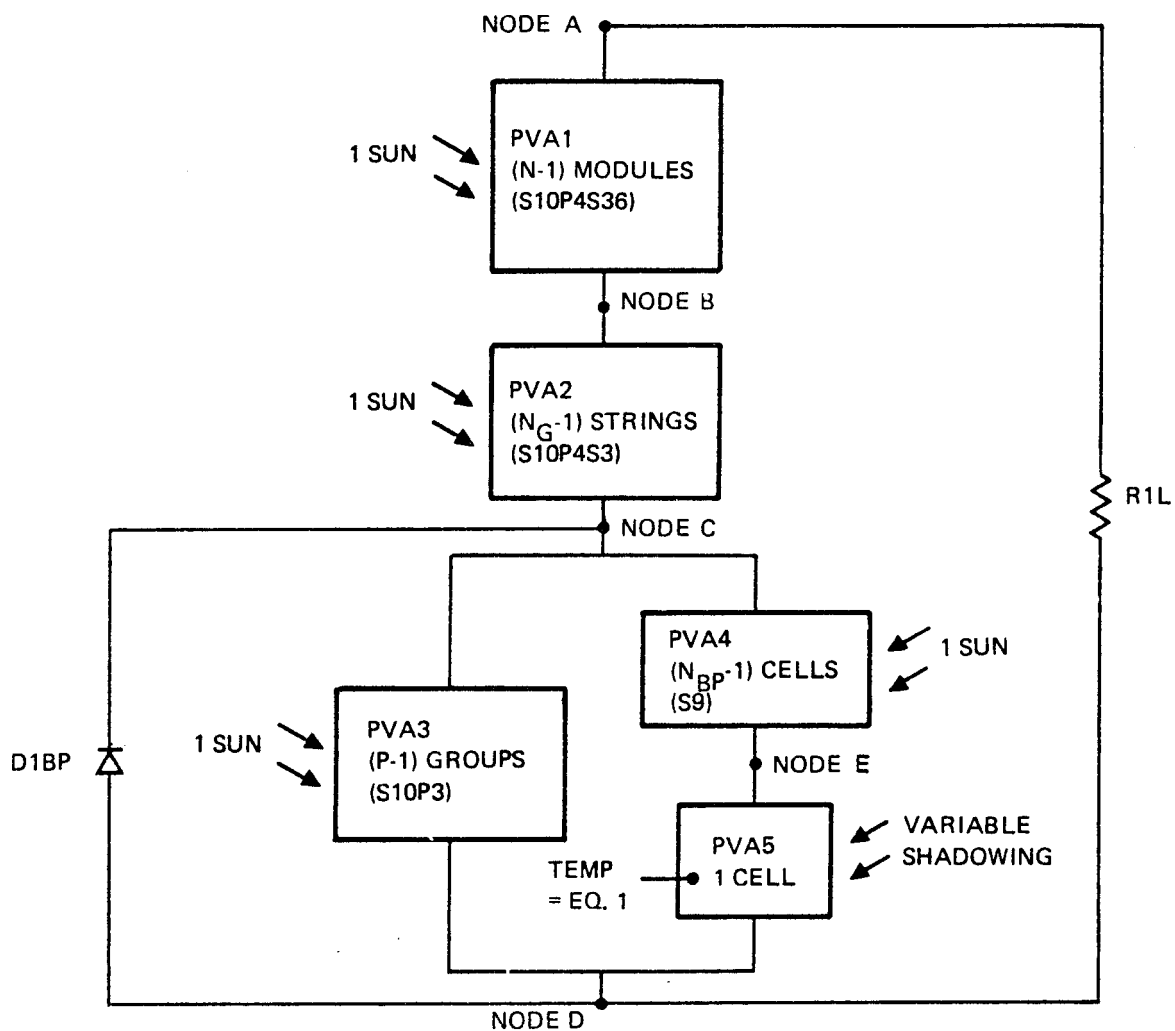


Figure 4-6. SCHEMATIC OF HOT SPOT HEATING MODEL FOR POLYCRYSTALLINE SILICON RESIDENTIAL APPLICATION

The remaining module is broken up into four elements. PVA2 contains all but one of the series connected bypass groups. The remaining bypass group is broken up among PVA3, PVA4, and PVA5. PVA3 contains all but one of the parallel strings in the bypass group. The remaining string in the bypass group is divided among PVA4 and PVA5. PVA4 contains all but one cell. The remaining cell, PVA5, is the one which is shadowed. The temperature of the cell is given by Equation 4-1.

$$T_C - T_A = (\Delta T / \Delta S) S A_C - (\Delta T / \Delta P) I_{PV} V_{PV} \quad \text{Eq. (4-1)}$$

where

T_A	= ambient temperature ($^{\circ}\text{C}$ or $^{\circ}\text{K}$)
$\Delta T / \Delta S$	= temperature coefficient for insolation power ($^{\circ}\text{C}/\text{mW}$)
$\Delta T / \Delta P$	= temperature coefficient for electric power ($^{\circ}\text{C}/\text{mW}$)
S	= insolation (mW/cm^2)
A_C	= cell area (cm^2)
I_{PV}	= cell current (mA)
V_{PV}	= cell voltage (V)

The input listing for the polycrystalline silicon residential hot spot heating application is contained in Table 4-8. The five aggregate cells are shown in lines 16 through 20. Line 21 connects the bypass diode across the module composed of PVA3, PVA4, and PVA5. V2T is the temperature input to the shadowed cell. It has the form of Equation 4-1 and is input to the cell at node T2. The value 8510 represents the multiplication of the cell area (85.1 cm^2) by the standard insolation ($100 \text{ mW}/\text{cm}^2$). The variable V(V2S) is the actual insolation on the shadowed cell. V2S is set up in line 27 with node S2 connected to the S2 node of PVA5. V2S will be varied from 1 sun to 0.4 suns as specified in line 32 to simulate the variable shadowing on the cell. Returning to line 22, P1 and P2 represent the temperature coefficients for insolation and electrical power, respectively. The values are given in lines 23 and 24. I(PVA5) and V(PVA5) are the current and voltage of the cell. Under reverse bias conditions, V(PVA5) will be negative; thus, this term will add to the first term and to the ambient temperature which is specified as 293°K .

In STATE2 (lines 39 through 46) the load resistance is set to a low value to simulate the short circuit current condition which is the worst operating condition for cell heating. The insolation on the cell represented by V2S is decreased from 1.0 to 0.4 suns and various temperatures and parameters are printed and plotted. The most significant values obtained are the temperature at node T2 and the voltage across PVA5. These are specified for plotting in lines 43 and 44 versus X2. X2 was defined in line 30 as 1 minus the insolation on the cell; thus, it represents the degree of shadowing on the cell.

**Table 4-8. POLYCRYSTALLINE SILICON RESIDENTIAL APPLICATION
HOT SPOT HEATING MODEL**

ONE-2 NETWORK ANALYSIS PROGRAM RELEASE 9.1 FTM

01/27/82 17.02.03.

```

0 0000000001111111112222222222333333333344444444445555555555666666666677777777778
  12345678901234567890123456789012345678901234567890123456789012345678901234567890
  * PSI HOT-SPOT HEATING: STRING OF TEN RESIDENTIAL MODULES
  LIBRARY
  1  BV PSI01 11
  2
  3    M 1.271214
  4    P 2.359949
  5
  6    ALPHA 1.05484E4
  7    CT .00061
  8    G 95.1
  9    IP 2.13E3
 10    IS 7.45E4
 11    RS 4.72E-6
 12    D BPD1 1
 13    RB 1E-4
 14    IS 8.24E-6
 15    TH 20.
 16  PVA1 A E S T P1 PSI01 0.0,0.0,0.0,S10P4S36
 17  PVA2 B C S T P2 PSI01 0.0,0.0,0.0,S10P4S3
 18  PVA3 C D S T P3 PSI01 0.0,0.0,0.0,S10P3
 19  PVA4 C E S T P4 PSI01 0.0,0.0,0.0,S9
 20  PVA5 E D S2 T2 P5 PSI01 0.0,0.0,0.0,S1
 21  B1BP D C BPD1
 22  V2T T2 0 9510*V(V2S)*P1-I(PVA5)*V(PVA5)*P2+293
 23  P1 3.5E-3
 24  P2 3E-3
 25  X1=I(PVA5)*V(PVA5)
 26  V1S S 0 1.0
 27  V2S S2 0 1.0

 28  V1T T 0 320
 29  R1L A D .023
 30  X2=1-V2S
 31  STATE1
 32    V2S 1.0 (72) 0.04
 33    *R1L .020
 34    PRINT X2 N(T2) V(PVA5) I(PVA5) X1 V(PVA4) I(PVA3) V(PVA3)
 35    PLOT N(T2) VS X2
 36    PLOT V(PVA5) VS X2
 37    PLOT I(PVA5) VS X2
 38    PLOT X1 VS X2
 39  STATE2
 40    V2S 1.0 (72) 0.04
 41    *R1L 2.5E-5
 42    PRINT X2 N(T2) V(PVA5) I(PVA5) X1 V(PVA4) I(PVA3) V(PVA3)
 43    PLOT N(T2) VS X2
 44    PLOT V(PVA5) VS X2
 45    PLOT I(PVA5) VS X2
 46    PLOT X1 VS X2
 47  END

```

The plots of the temperature and voltage of the cell are contained in Figures 4-7 and 4-8. The maximum temperature of 344°K (71°C) occurs at approximately 25 percent shadowing and at a reverse bias of 4.7 volts.

4.1.2 Model Validation and Inputs for Specific Applications

This section discusses the results of the modeling effort, including the results of modeling runs performed and determination of input values for the cost/performance evaluation.

4.1.2.1 PV Cell Data Reduction

The data reduction runs performed on 1 cm², unit area cells for each PV technology are summarized in Table 4-9. First, the input parameter values for each technology are specified. Then, the PV cell parameters calculated by the data reduction are presented. Finally, the accuracy of the data reduction process is specified in terms of percent deviation from input values. Since, in most cases, the I-V curves were postulated or projected from existing data, the currents and voltages input do not represent real data. Therefore, the data will not exactly match the PV cell model and some deviation will be seen between the input data and current-voltage values obtained from the calculated parameters. As can be seen, however, the deviations are generally small--all less than 1 percent. In most cases, however, weighting factors had to be placed on the input I-V points to assist the program in matching the critical points--the peak power point and the open circuit voltage. Thus, for the polycrystalline silicon cell data reduction, weighting values of 1.0 were placed on these points while weighting values of 0.1 were placed on the other two points. Notice that the CdS/CuInSe₂ cell data reduction did not require weighting values.

Some additional difficulty was encountered in performing the data reduction for the amorphous silicon cell. The I-V curve for this cell was projected to represent an efficiency of 10 percent starting with experimental data from a 6 percent efficient cell. The I-V curve appears to exhibit a large series resistance effect; yet, the actual shape of the curve caused the data reduction program to calculate a series resistance less than 1 mΩ. Therefore, the series resistance shown (50 mΩ) was input as a fixed value and not actually calculated so that the parameter values obtained would be more realistic. None of the other four data reductions performed required this technique. In general, problems in data reduction will not result if well-behaved, measured data are used; however, if any parameters such as series resistance are already known, inputting these as fixed values will always facilitate the data reduction process.

The input data for the GaAs concentrator cell data reduction represents a departure from cell parameters listed for this cell in Section 3.5.2.1. Data reductions performed on the original data indicated that the ratio of peak

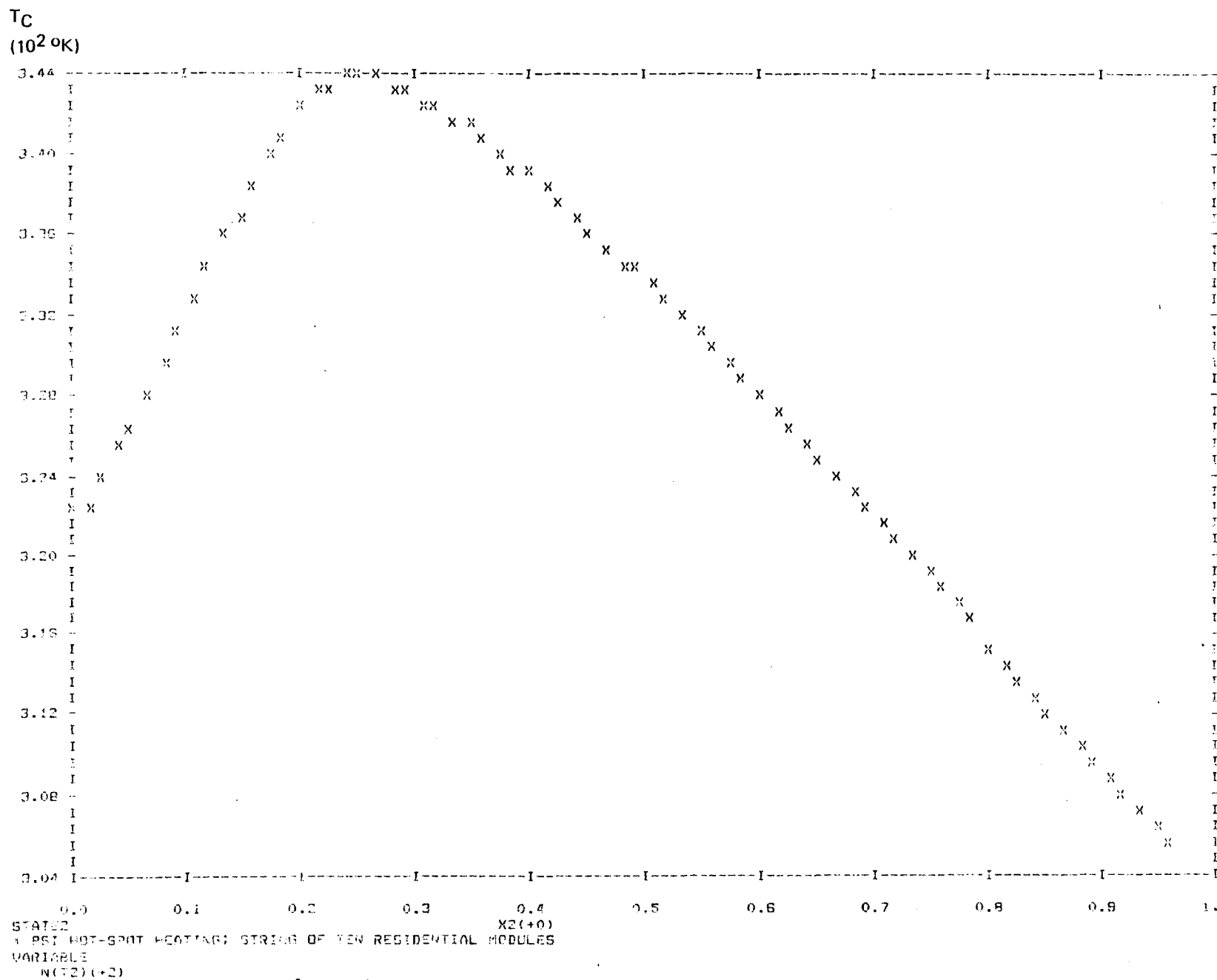


**Figure 4-7. POLYCRYSTALLINE SILICON RESIDENTIAL CELL TEMPERATURE
VERSUS DEGREE OF SHADOWING**

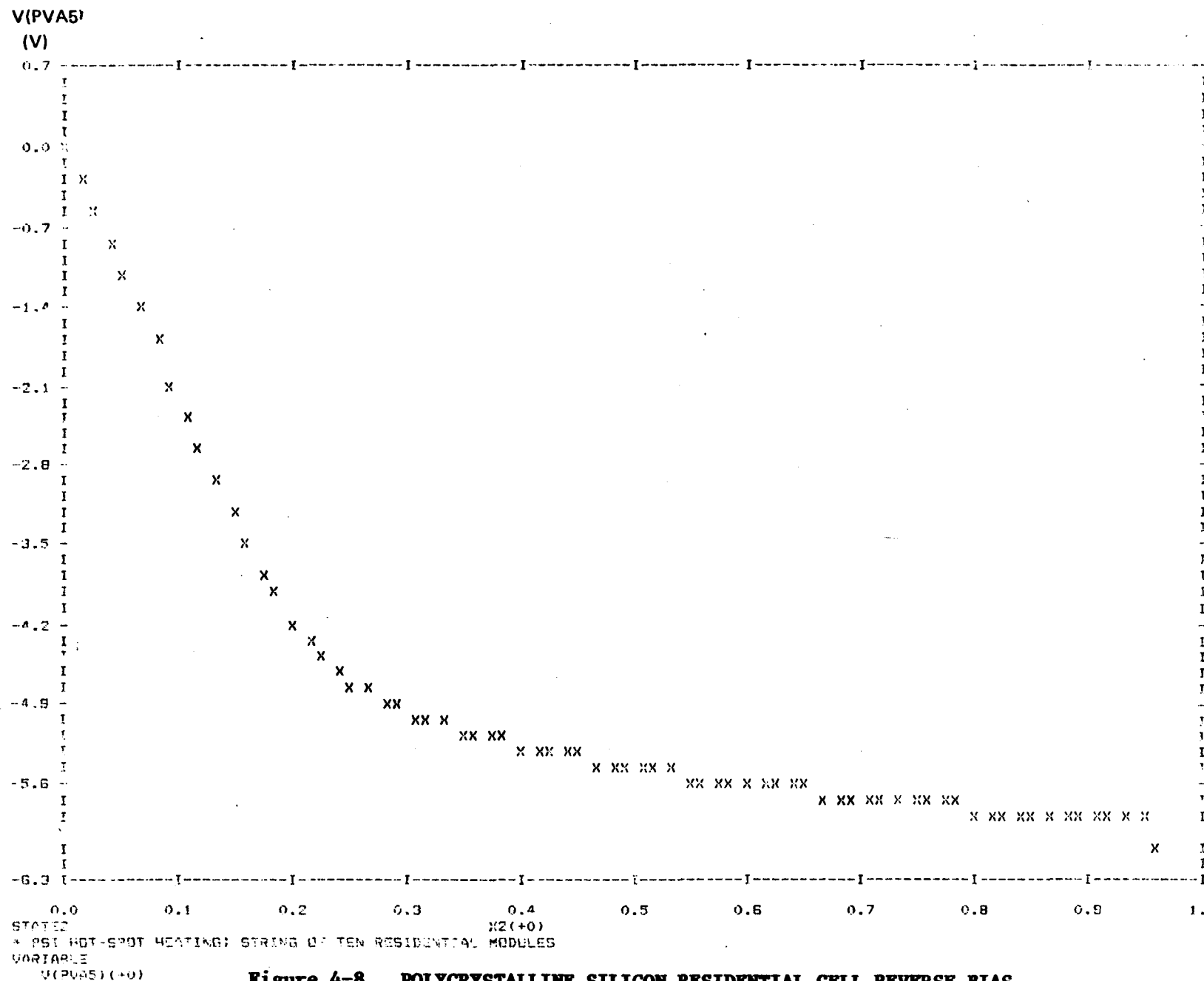


**Figure 4-8. POLYCRYSTALLINE SILICON RESIDENTIAL CELL REVERSE BIAS
VERSUS DEGREE OF SHADOWING**

Table 4-9. DATA REDUCTION SUMMARY FOR 1 CM² CELLS

	POLYCRYSTALLINE SILICON	AMORPHOUS SILICON	CdS/CuInSe ₂	GaAs FLAT PLATE	GaAs CONCENTRATOR
INPUTS ISC (mA) G (mmho) TEMP (°K) IP (mA) DVDT (V/°C) DIDT (I/°C) V, I, Wt (V, mA, —)	25.0 1.0 298 25.0 -0.0022 15.3E-3 0.45, 24.1, 0.1 0.50, 23.0, 1.0 0.55, 17.3, 0.1 0.60, 0.0, 1.0	16.0 0.5 298 16.0 -0.0016 9.76E-3 0.70, 14.4, 0.1 0.73, 13.7, 1.0 0.75, 13.25, 0.1 0.91, 0.0, 1.0	39.4 1.0 298 39.4 -0.002 23.8E-3 0.24, 38.9, — 0.30, 36.0, — 0.36, 24.5, — 0.424, 0.0, —	25.0 0.1 298 25.0 -0.0032 15.3E-3 0.833, 24.0, 1.0 0.88, 20.9, 0.1 0.90, 17.2, 0.1 0.97, 0.0, 1.0	8760 0.1 373 17.52 -0.014 5.2 1.2, 8250, 0.1 1.25, 8000, 1.0 1.3, 7600, 0.1 1.5, 0.0, 1.0
OUTPUTS IS (mA/°K ^P) M (-) RS (K) P (-) ALPHA (°K)	8.758E2 1.271 4.015E-4 2.360 1.0548E4	5.098 3.332 5.0E-5 0.900 4.3644E3	8.120E3 0.7982 2.057E-3 3.7585 1.4195E4	1.967E7 1.209 1.538E-3 2.4805 1.7579E4	1.126E23 3.190 1.0E-6 0.9404 2.3944E4
ACCURACY (PERCENT DEVIATION) FOR V _{OC} FOR I _{MPC}	0.0% 0.09%	0.0% 0.2%	0.9% 0.5%	0.2% 0.1%	0.02% 0.8%

power voltage to open circuit voltage was too high. The resultant series resistance obtained was less than 1 m Ω and the peak power obtained occurred near 1.25 V instead of 1.3 V. It should be remembered that the GaAs concentrator cell data was postulated and does not represent actual I-V data. Therefore, the peak power point was moved to 8.0 A at 1.25 V. This results in a module with peak power voltage of 50.0 V instead of 52.0 V and peak power current of 20.6 A instead of 19.58 A. The module power is 1,013 W instead of 1,018 W. These changes have also been reflected in the module and array modeling summaries in the subsequent sections of this report.

4.1.2.2 Module Modeling

The results of the module modeling runs are contained in Table 4-10. The inputs shown in the table are of the type previously discussed in Table 4-4 as those which vary with the particular application. The interconnection of cells in the bypass group is shown first. The interconnection scheme is read from left to right; thus, for the polycrystalline silicon residential module, 10 cells are first connected in series; then, four of these 10-cell strings are connected in parallel. N_G specifies the number of bypass groups connected in series in the module. Note that the GaAs residential module represents a divergence from the other modules in that cells are first connected in parallel, and then six of the two-cell parallel groupings are connected in series to form the bypass group.

The cell parameters shown have been scaled by the actual cell areas used in the modules. The area dependent parameters are IP, G, IS and RS. The IP, G and IS values obtained from the data reduction are multiplied by the cell area to obtain the parameters shown in this table. On the other hand, RS is divided by the cell area. The other parameters are independent of area.

Table 4-10 also lists critical outputs obtained from the module modeling runs. For each module, the open circuit voltage, the voltage at maximum power, and maximum power obtained are catalogued. The values for these points obtained from the design process are listed to the right of each slash. For the GaAs CPS application the design values were changed due to the changes discussed in the cell data reduction in Section 4.1.2.1. The deviations of the calculated power from the design point, which are mostly due to the deviations resulting from the cell data reduction process, are all less than 1 percent.

Analyses of the effects of insolation and temperature variations were done separately. The inputs for these variations are shown in Table 4-11. To simulate these effects the temperature is kept constant while three variations in insolation are simulated with PV-TAP. Next, the insolation is kept constant while three different temperatures are used.

Table 4-10. MODULE MODELING AND VERIFICATION SUMMARY

INPUTS	POLYCRYSTALLINE SILICON		AMORPHOUS SILICON		CdS/CuInSe ₂		GaAs	
	RES	CPS	RES	CPS	RES	CPS	RES	CPS
BYPASS GROUP	S10P4	S10P3	S7P10	S7P2	S10P4	S10P4	P2S6	S4P2
N _G	4	10	2	10	5	16	4	10
A _C (cm ²)	85.1	91.5	23.1	22.8	44.9	42.4	92.64	1.27
CELL PARAMETERS								
IP (mA/SUN)	2.13E3	2.29E3	370	365	1.77E3	1.67E3	2.316E3	22.20
G (mmho)	85.1	91.5	11.6	11.4	44.9	42.4	9.264	0.127
IS (mA/°K ^P)	7.45E4	8.01E4	118.0	116.0	3.65E5	3.44E5	1.822E9	1.427E23
M (-)	1.271	1.271	3.332	3.332	0.7982	0.7982	1.209	3.190
RS (K)	4.72E-6	4.39E-6	2.16E-6	2.19E-6	4.58E-5	4.85E-5	1.66E-5	7.89E-7
P (-)	2.3599	2.3599	0.900	0.900	3.7585	3.7585	2.4805	0.9404
ALPHA (°K)	1.0548E4	1.0548E4	4.3644E3	4.3644E3	1.4195E4	1.4195E4	1.7579E4	2.3944E4
CT (°K ⁻¹)	0.00061	0.00061	0.00061	0.00061	0.00061	0.00061	0.00061	0.00061
OUTPUTS								
V _{OC} (V) (CALC/DESIGN)	24.0/24.0	60.0/60.0	12.74/12.74	63.7/63.7	21.4/21.2	68.5/67.8	23.3/23.3	60.0/60.0
V _{MP} (V) (CALC/DESIGN)	19.98/20.0	49.94/50.0	10.03/10.22	50.2/51.1	15.2/15.0	48.4/48.0	19.99/20.0	49.2/50.0
P _M (W) (CALC/DESIGN)	156.5/156.0	315.7/315.5	32.48/32.42	32.06/31.89	97.55/97.05	294.7/293.0	88.8/89.0	1007/1013
POWER DEVIATION	0.3%	0.06%	0.2%	0.5%	0.5%	0.6%	0.2%	0.6%

Table 4-11. INSOLATION AND TEMPERATURE VARIATION PV-TAP INPUTS

- a) **FOR CENTRAL POWER AND RESIDENTIAL APPLICATIONS OF POLY-SI,
A-SI, CdS, AND FOR RESIDENTIAL APPLICATIONS OF GaAs**

INSOLATION (SUNS)	TEMPERATURE (°C)
0.1	25
0.5	25
1.0	25
1.0	15
1.0	25
1.0	75

- b) **FOR CENTRAL POWER APPLICATIONS OF GaAs**

INSOLATION (SUNS)	TEMPERATURE (°C)
50	100
250	100
500	100
500	50
500	100
500	120

4.1.2.3 Array Modeling

The results of the array modeling runs are summarized in Table 4-12. The array models are formed by connecting module models in series to produce strings of modules. The values shown for the number of modules in a string and the number of parallel strings in the array were obtained from the array designs. The results of the array modeling runs are summarized in the same manner as were the results of the module modeling runs. As expected, the deviations of the calculated power from the power postulated in the designs are all less than 1 percent.

In modeling the arrays, the polycrystalline silicon residential array was modeled first. A string of modules was specified as a sub-array model as shown previously in Figure 4-4: then, three subarray models were connected in parallel to model the full array. When this technique was attempted in modeling the polycrystalline silicon CPS array, the core limits of the SERI computer were exceeded. Therefore, the CPS array was modeled as a single string of modules with a parallel segment designator of 362 as previously discussed in Section 4.1.1.3. The two modeling techniques will produce identical results for the case of identical cells. Under cell photocurrent variation conditions, however, the use of the parallel segment designator will cause all 362 strings to have the same aggregate photocurrent as opposed to the case of the residential array modeling in which the three strings will each have a different aggregate photocurrent. In order to assess the errors produced by using the parallel segment designator, the residential array was run with this same technique. The results of the modeling assessment are summarized in Table 4-13. Runs were made with cell photocurrent distributions of ± 10 percent and ± 50 percent. The array power obtained using identical cells is shown in the first line. The second line compares the array power obtained from the string model with the power obtained using the full array. The losses in array power due to the cell photocurrent variations from the case of identical cells are shown in the third line. The differences in power loss between the string model and the full array model are shown in the fourth line. For the 10 percent cell distribution the difference in power loss is 0; for the 50 percent cell distribution the difference in power loss is only 1.3 percent out of about 30 percent which is within the accuracy of the aggregation modeling [41].

Table 4-12. ARRAY MODELING AND VERIFICATION

	POLYCRYSTALLINE SILICON		AMORPHOUS SILICON		CdS/CuInSe ₂		GaAs	
	RES	CPS	RES	CPS	RES	CPS	RES	CPS
INPUTS								
STRING OF MODULES	10	20	20	20	13	21	10	20
PARALLEL STRINGS	3	362	7	3585	4	371	5	112
OUTPUTS								
V _{OC} (V) (CALC/DESIGN)	240.0/240.0	1200/1200	254.8/254.8	1274/1274	2783.3/275.6	1438/1491	233.2/233	1200/1200
V _{MP} (V) (CALC/DESIGN)	199.8/200.0	997/1000	202.3/204.4	1005/1020	197.0/195	1086/1075	199.9/200	985/1000
P _M (kW) (CALC/DESIGN)*	4.698/4.680	2286/2284	4.55/4.54	2297/2282	5.07/5.05	2292/2282	4.44/4.45	2257/2269
POWER DEVIATION	0.4%	0.09%	0.2%	0.7%	0.4%	0.4%	0.2%	0.5%

*POWERS LISTED FOR CPS APPLICATIONS ARE FOR 2 MW SUBSYSTEMS

Table 4-13. ASSESSMENT OF ERRORS PRODUCED BY MODELING ONLY ONE STRING OF MODULES INSTEAD OF FULL ARRAY

	CELL IP DISTRIBUTION	
	$\pm 10\%$	$\pm 50\%$
$P_M(W)$ (Identical cells)	4698	4698
$P_M(W)$ (String/Full Array)	4445.3/4445.1	3253.7/3313.6
Power Loss (%) (String/Full Array)	5.39/5.39	30.8/29.5
Difference in Power Loss (%)	0.0	1.3
Module IP Data		
IP (Average) (A)	8.125A	6.729A
3σ - IP(A)	8.215A	7.281A
IP Distribution (%)	± 1.1	$\pm 8.2\%$

In order to assist in understanding the effects of the modeling, an additional state solution was obtained in each of the string runs which assessed the photocurrent variations of the modules. A load resistance was placed across each of the ten modules in the module string and was set to a low resistance value to obtain the short circuit current of each module. The short circuit current is a good approximation of the photocurrent. The average value of the ten module photocurrents for the 10 percent cell distribution case was 8.125 A with a 3σ photocurrent of 8.215 A. This represents a 3σ variation of ± 1.1 percent. For the 50 percent cell distribution case, the module photocurrent variation is ± 8.2 percent. Thus, the distributions of photocurrents in the modules are much tighter than the cell photocurrent distributions. The photocurrent distributions for the strings of modules would be further tightened with the result that very little loss is seen in paralleling strings. Based on this modeling assessment, the other seven arrays were modeled with the parallel segment designator technique. The percentage that the 3σ point varied from the mean was chosen to be the same for all technologies. The actual currents supplied on this basis are listed in Table 4-14, in which the lower 3σ points representing the specified percentage variation from the mean are given.

This procedure was performed for the array designs for each technology and application except for the CdS central power array. The procedure for this application of the CdS technology is outlined in Figure 4-9. It was found that since PV-TAP ran with difficulty on the small core memory of the SERI computer that not enough core was available to model an entire CdS CPS series string. The reason for this is the relatively low voltage of this cell, which

Table 4-14. SUMMARY OF PHOTOCURRENT VARIATION MODELING

	POLYCRYSTALLINE SILICON		AMORPHOUS SILICON		CdS/CuInSe ₂		GaAs	
	RES	CPS	RES	CPS	RES	CPS	RES	CPS
NOMINAL IP	2.13A	2.29A	370mA	365mA	1.77A	1.67A	2.316A	22.2mA
3σ IP -- + 10%	1.917A	2.061A	333mA	328.5mA	1.593A	1.503A	2.084A	19.98mA
+ 20%	1.704A	1.832A	296mA	292mA	1.416A	1.336A	1.853A	17.76mA
+ 50%	1.065A	1.145A	185mA	182.5mA	0.885A	0.835A	1.158A	11.1mA

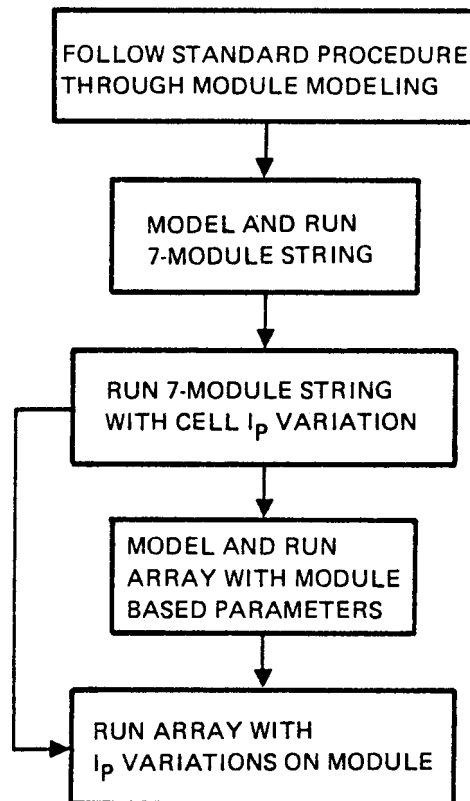


Figure 4-9. ARRAY MODELING FOR CdS/CuInSe₂ CPS APPLICATION

resulted in significantly more cells connected in series to yield the desired module voltage. It was thus modeled in two steps. Instead of modeling the full 21 modules in the CPS string, a string module was composed of seven modules as shown in Figure 4-9. A second run was then made to represent the full string by replacing the cell parameters with modules parameters. Thus, each module was modeled as a single cell. The short circuit current variations in the results of the module runs were analyzed to obtain the mean and the 3 σ points for the cells used to represent the modules. Thus, the second set of runs (which represented the modules as cells) formed the results for this case.

In order to demonstrate photocurrent variation modeling, both the residential and CPS polycrystalline silicon arrays were analyzed for 10 percent and 50 percent cell photocurrent variation. The results of the modeling demonstration are included in Table 4-15. The residential run is the same as previously shown for the full array model in Table 4-13. Table 4-15, however, contains more detailed results and also contains the CPS results. The table first summarizes the cell photocurrent, open circuit voltage, peak power voltage and peak power of each array for the case of identical cells. Then, the results of the 10 percent and 50 percent Gaussian photocurrent distributions are summarized. First, the photocurrents at the 3 σ points are shown. Next, the open circuit voltage obtained and the deviation from the open circuit voltage with identical cells are listed. The same type of results are included for the peak power voltage and the peak power. A negative value on the percent deviation indicates a decrease in voltage or power. The losses in power for the 10 percent cell photocurrent distribution case are about the same (5.5 percent) for the residential and CPS applications. For the case of the 50 percent cell photocurrent distribution, the difference in the power loss between the CPS and residential applications is still only 3 percent.

4.1.2.4 Hot Spot Heating Modeling

The purpose of the hot spot heating analysis is to examine the resulting temperature rise in a single cell due to shadowing of that cell. The shadowed cell is in a module in a series string of modules. The modeling for this condition was previously discussed in Section 4.1.1.4. Table 4-16a summarizes the cell interconnections for each of the five PV aggregate elements previously described in Figure 4-6, and the temperature coefficients for each application. The temperature coefficients were obtained for each technology by constraining the cell temperature in normal operation to 50°C for flat plate technologies and 100°C for the concentrator technology and specifying the ratio of $\Delta T/\Delta S$ to $\Delta T/\Delta P$ to be the same as that for the polycrystalline technology. The sequences described in Table 4-16a result from the values of Table 4-16b applied to the formulas in Table 4-7. PVA5 will receive variable shadowing to assess the maximum cell temperature which can be obtained, the reverse bias corresponding to this cell temperature and the degree of shadowing at which these values were obtained. The results are dependent mainly on the size of the bypass group and the shunt resistance and area of the cells.

Table 4-15. PHOTOCURRENT VARIATION MODELING USING POLYCRYSTALLINE SILICON

	RESIDENTIAL	CPS
IDENTICAL CELLS		
Photocurrent (IP)	2.13A	2.29A
$V_{OC}(V)$	240	1200
$V_{MP}(V)$	199.8	997
$P_M(kW)$	4.698	2286
+ 10% GAUSSIAN IP		
IP - 3σ Points	1.917A, 2.343A	2.06A, 2.52A
$V_{OC}(V)$ /Deviation	239.3/-0.29%	1197/-0.25%
$V_{MP}(V)$ /Deviation	199.5/-0.15%	997/0.0%
$P_M(kW)$ /Deviation	4.445/-5.4%	2159/-5.6%
+ 50% GAUSSIAN IP		
IP - 3σ Points	1.065A, 3.195A	1.145A, 3.435A
$V_{OC}(V)$ /Deviation	236.1/-1.6%	1180/-1.7%
$V_{MP}(V)$ /Deviation	203.5/+1.9%	1020/+2.3%
$P_M(kW)$ /Deviation	3.314/-29.5%	1542/-32.5%

Table 4-16a. SUMMARY OF HOT SPOT HEATING INPUTS

	POLYCRYSTALLINE SILICON		AMORPHOUS SILICON		CdS/CuInSe ₂		GaAs	
	RES	CPS	RES	CPS	RES	CPS	RES	CPS
PVA1	S10P4S36	S10P3S190	S7P10S38	S7P2S190	S10P4S60	S10P4S320	P2S216	S4P2S190
PVA2	S10P4S3	S10P3S9	S7P10	S7P2S9	S10P4S4	S10P4S15	P2S18	S4P2S9
PVA3	S10P3	S10P2	S7P9	S7	S10P3	S10P3	P2S5	S4
PVA4	S9	S9	S6	S6	S9	S9	S1	S3
PVA5	S1	S1	S1	S1	S1	S1	S1	S1
$\frac{\Delta T(^{\circ}C)}{\Delta S(mW)}$	3.5E-3	3.5E-3	13.4E-3	13.4E-3	6.47E-3	6.47E-3	3.26E-3	1.26E-3
$\frac{\Delta T(^{\circ}C)}{\Delta P(mW)}$	3E-3	3E-3	11.5E-3	11.5E-3	5.54E-3	5.54E-3	2.78E-3	1.079E-3

Table 4-16b. STRING MODELING FOR HOT-SPOT HEATING RESULTS

	PSI		ASI		CdS		GaAs
	RES	CPS	RES	CPS	RES	CPS	CPS
a	10	20	20	20	13	21	20
b	10	10	7	7	10	10	4
c	4	3	2	4	4	4	2
d	4	10	2	10	5	16	10

Table 4-17 summarizes the results of hot spot heating runs performed on polycrystalline silicon residential and CPS applications. The bypass group size is the same for each application. The reverse bias and the degree of shadowing at which the maximum cell temperature is obtained is approximately the same for both applications because the shunt resistances of each case are sufficiently close that the effect of the difference is negligible. The cell temperature is more strongly dependent on cell area; therefore, the cell temperatures are different for the two cases. The larger cell area for the CPS cell produces a higher cell temperature. The cell temperatures are significantly lower than the maximum cell temperature of 100°C which was used for the module designs. There are two reasons for this difference. First, the bypass group design equations used in the design phase were conservative in that the maximum allowable cell area was used and the cell was considered to be fully illuminated in the equation so that the allowable reverse voltage was conservative. The calculations performed resulted in a maximum bypass group size of 11 cells. The second reason for the lower cell temperature is the fact that the final module design resulted in a bypass group of only 10 cells rather than the maximum allowable of 11 cells.

Table 4-17. HOT SPOT HEATING MODELING USING POLYCRYSTALLINE SILICON

	RESIDENTIAL	CPS
Bypass Group	10	10
Worst Case Shadowing		
T_C (°C)	70.7	74.1
V_R (V)	-4.7	-4.6
f_{SH} (%)	25.3	25.3

4.1.3 Conceptual Design Performance Evaluation

The objective of this part of Section 4.0 is to present the results of the module insolation and temperature variations (Section 4.1.3.1), array photocurrent variations (Section 4.1.3.2), and hot spot heating (Section 4.1.3.3) for each technology application.

4.1.3.1 Insolation and Temperature Variations

The I-V curves for the specific module design for each technology and application were generated for each temperature and insolation listed in

Table 4-11, and the maximum output power was selected from a listing of the I-V curve. The maximum output electrical power for each technology and application are shown in Table 4-18a. It is seen that if only half of the design insolation for the modules is present, the resulting power is decreased by slightly more than one-half, except in the case of the CdS technologies, in which the resulting power is slightly greater than half of the power that the modules were as designed to produce. In all the cases, when the insolation was one-tenth the insolation that the modules were designed for, the output power was less than a tenth of the output power that the module was designed to produce.

In the temperature variations, it is seen that a lower operating temperature for the cells in a module would result in greater power output. However, it is assumed in the design that since the cells are not cooled actively, their temperature will be at least 15°C. As demonstrated in the hot-spot heating analysis, the temperature will not change significantly due to conditions such as shadowing. Additionally, the changes in output power for the various temperatures postulated do not reflect the drastic changes resulting from variations in insolation. Thus, the output power will not vary excessively over a reasonable range of operating temperatures.

The short circuit current and open circuit voltage for each technology and application are shown in Table 4-18b. The short circuit currents and open circuit voltages obtained from these PV-TAP runs were used to more accurately model the inputs to SOLCEL II than could be accomplished using simple, hand-calculation techniques.

4.1.3.2 Photocurrent Variations

The resulting output power of the arrays and their percentage variations from the nominal output power due to the different cell short circuit current variations are shown in Table 4-19. Figure 4-10 is a plot of the information found in the table. Although the variations are not linear, the percent power loss does not exceed 35 percent even in the worst situation, in which case the 3σ point varies 50 percent from the nominal value. The curves shown in Figure 4-10 should not be considered authoritative for any specific technology and application involved, since the designs were done on the basis of estimations of several parameters. They do, however, reflect general trends, which are true for all of the technologies. Most of the technologies and applications had resulting power losses which were fairly similar up to 20 percent variations in short circuit currents. In this case, no power loss exceeded 12 percent, and at 10 percent variation, the power loss was less than 6 percent. Thus, variations in cell short-circuit current tend to be smoothed out when the cells are arranged into an array.

Table 4-18a. INSOLATION AND TEMPERATURE RESULTS, OUTPUT POWER (W)

TECHNOLOGY:	POLY SI		aSI		CdS		GaAs
APPLICATION:	RES	CPS	RES	CPS	RES	CPS	RES
INSOLATION							
.1 SUN	11.33	22.86	1.976	1.952	9.615	29.04	8.223
.5 SUN	73.98	149.1	14.58	14.40	52.08	157.2	44.09
1.0 SUN	156.5	315.7	32.48	32.06	97.55	294.7	88.81
TEMPERATURE							
15°C	163.0	328.6	33.16	32.73	104.4	315.1	91.96
25°C	156.5	315.7	32.48	32.06	97.55	294.7	88.81
75°C	123.7	249.0	28.84	28.67	63.76	192.4	72.45

TECHNOLOGY:	GaAs
APPLICATION:	CPS
INSOLATION	
50 SUNS	82.11
250 SUNS	476.3
500 SUNS	1007
TEMPERATURE	
50°C	1568
100°C	1007
120°C	781.9

Table 4-18b. **INSOLATION AND TEMPERATURE RESULTS, SHORT CIRCUIT CURRENT AND OPEN CIRCUIT VOLTAGE**

TECHNOLOGY	POLY-SILICON		A-SILICON		CdS/CuInSe ₂		GaAs
APPLICATION	RES	CPS	RES	CPS	RES	CPS	RES
INSOLATION	(A) / (V)	(A) / (V)	(A) / (V)	(mA) / (V)	(A) / (V)	(A) / (V)	(A) / (V)
0.1 SUN	0.85/20.7	0.68/51.8	0.37/9.72	73.0/48.6	0.71/19.0	0.67/60.7	0.46/21.6
0.5 SUN	4.26/23.1	3.43/57.7	1.85/11.9	365./59.4	3.53/20.7	3.33/66.2	2.32/22.8
1.0 SUN	8.52/24.0	6.87/60.0	3.70/12.7	730./63.7	7.07/21.4	6.67/68.5	4.63/23.3
TEMPERATURE							
15°C	8.46/24.8	6.83/62.1	3.68/12.9	726./64.7	7.02/22.4	6.63/71.8	4.60/24.1
25°C	8.52/24.0	6.87/60.0	3.70/12.7	730./63.7	7.07/21.4	6.67/68.5	4.63/23.3
75°C	8.78/19.8	7.08/49.4	3.81/11.8	752./58.9	7.28/16.1	6.87/51.7	4.77/19.5

TECHNOLOGY	GaAs
APPLICATION	CPS
INSOLATION	(A) / (V)
50 SUNS	2.22/50.6
250 SUNS	11.1/57.2
500 SUNS	22.2/60.0
TEMPERATURE	
50°C	21.5/87.6
100°C	22.2/60.0
120°C	22.5/48.9

Table 4-19. PHOTOCURRENT DISTRIBUTION RESULTS, ARRAY/SUBARRAY POWER OUTPUT (W) AND PERCENT POWER LOSS FROM NOMINAL

TECHNOLOGY:	POLY SI		aSi		CdS		GaAs		
APPLICATION:	RES	CPS	RES	CPS	RES	CPS	RES (P2S6)	RES (S6P2)	CPS
3 σ - % FROM AVG. 0	4.698 kW	2.286 MW	4.546 kW	2.297 MW	5.075 kW	2.292 MW	4.441 kW	4.441 kW	2.257 MW
10	4.445 kW 5.39%	2.159 MW 5.56%	4.322 kW 4.93%	2.181 MW 5.13%	4.855 kW 4.33%	2.203 MW 3.88%	4.304 kW 3.08%	4.245 kW 4.41%	2.174 MW 3.68%
20	4.184 kW 10.9%	2.026 MW 11.4%	4.096 kW 10.0%	2.059 MW 10.4%	4.626 kW 8.85%	2.117 MW 7.64%	4.137 kW 6.85%	3.934 kW 11.4%	2.080 MW 7.84%
50	3.314 kW 29.5%	1.542 MW 32.5%	3.410 kW 25.0%	1.627 MW 29.2%	3.794 kW 25.2%	1.844 MW 19.5%	3.492 kW 21.4%	3.051 kW 31.3%	1.680 MW 25.6%

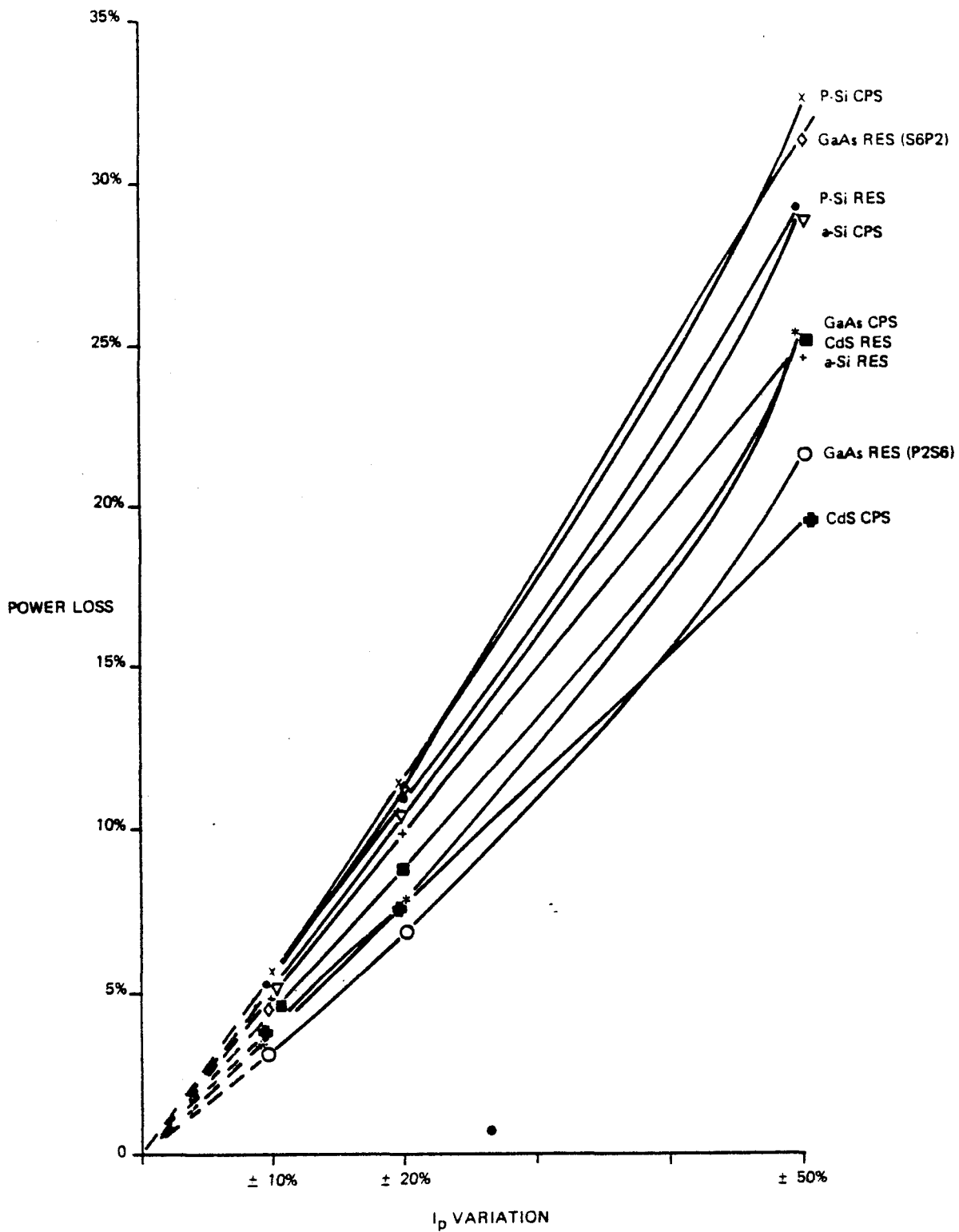


Figure 4-10. POWER LOSS DUE TO I_p VARIATION

4.1.3.3 Hot Spot Heating

The results of the hot spot heating runs are displayed in Table 4-20. It is obvious that in no case was the temperature increase of a shadowed cell in excess of the allowable temperature increase of the cell (50°C for p-si, 30°C for a-si, 72°C for CdS, 50°C for GaAs flat plate and 92°C for GaAs concentrator). In every case the results are worst-case because the series string of modules provides the most current to drive the shadowed cell into reverse bias and because the string modules were short-circuited. This trend is observed throughout the various technologies and applications. As in the case of photocurrent results, these should not be taken authoritatively for any technology or application specifically, since the I-V curves, upon which all of the analyses depend, were generated with best estimations of the parameters involved for each technology.

Table 4-20. HOT-SPOT HEATING SUMMARY, MAXIMUM TEMPERATURE RISE ABOVE SHORT CIRCUIT TEMPERATURES

TECHNOLOGY:	PSI		ASI		CdS		GaAs	
APPLICATION:	RES	CPS	RES	CPS	RES	CPS	RES	CPS
MAX TEMP. °C	71	74	61	61	72	69	74	177
DESIGN TEMP. °C	50	52	51	51	49	47	50	120
DIFFERENCE °C	21	22	10	10	23	22	24	57

4.2 SOLCEL II ANALYSES

4.2.1 SOLCEL II Modeling and Validation Procedure

Figure 4-11 diagrams the SOLCEL II modeling process. The polycrystalline silicon residential application was used to demonstrate SOLCEL II modeling. The voltage and current variations with temperature from the conceptual design calculations were also used for the SOLCEL II modeling inputs. The residential array was modeled by determining the required PV inputs and the inverter and load characteristics. The SOLCEL II run was made using weather data for Albuquerque from the SOLMET library and hourly load data for a typical home in Albuquerque. In addition to the listing of the annual energy distribution which is the standard output provided by SOLCEL II, additional

plots were made to demonstrate the ability to generate non-standard outputs from SOLCEL II. The array power and load demand for the first day of each season and histograms of the array power and load demand for the whole year were plotted for this modeling application.

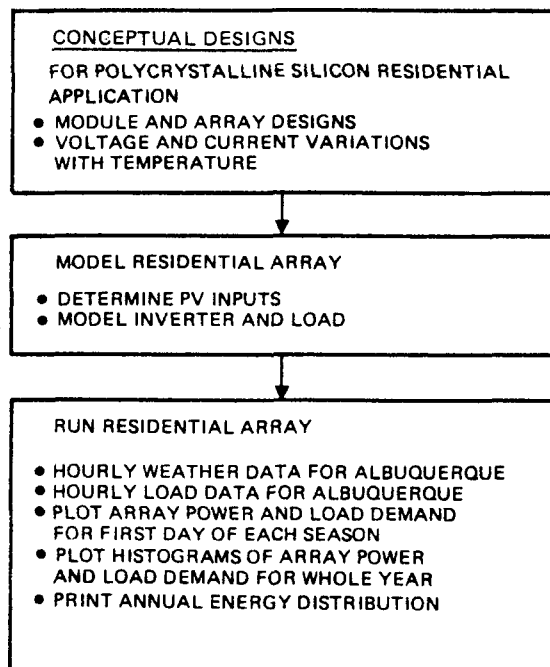


Figure 4-11. FLOW CHART FOR SOLCEL II MODELING

The inputs required to run SOLCEL II are contained in Table 4-21. The program requires that the array location and tilt angle, the load on the array, and typical weather data be supplied in addition to the array parameters. The weather data is supplied by SOLMET typical meteorological year data for a given location. The load data is also specified as typical hourly data for a given type of residence such as a gas heated or an all electric home. The power conditioning information required refers to the DC to AC inverter. The rated power of the inverter and the efficiency at full load are input. The program also requires the maximum allowable power into the inverter and the minimum (no load or tare) power. These are the powers levels at which the inverter will shut down.

The cell parameters required by SOLCEL II are determined by the code from current and voltage values input by the user. Short circuit current and open circuit voltage values are input at high and low insolation and temperatures. Of course, the high and low insolation and temperature values must also be input. The series resistance of the cell is also input by the user. This value is calculated by the user from two voltages points corresponding to the same junction current on I-V curves of different insolation. The method is described in reference 4.

The program also requires the device dependent constants (A_0 and E_{G0}). These constants are used by SOLCEL II in the determination of the cell saturation current. A_0 is a saturation current coefficient and E_G represents the band gap energy. Although these values are different for the various advanced PV technologies, these values cannot easily be obtained from cell current-voltage relationships. Therefore, the default values contained in the SOLCEL II program will be used for these parameters. The error in accuracy introduced by using default parameters is not expected to be significant since these constants will mainly affect the current-voltage values as a function of temperature, which have been bounded by using values at high and low temperatures.

The cell area is not a required input parameter; however, it is required in order to put the short circuit current and series resistance values in the proper format. These parameters are specified as unit area values; therefore, the short circuit current is specified in A/m^2 and the series resistance is specified $\Omega\text{-m}^2$.

The module dimensions, the packing factor of the module, and the number of modules in the array are also required to complete the array specification. These are input to SOLCEL II as two parameters, the total module area in the array and the module packing factor. SOLCEL II requires a number of additional inputs which are not shown in Table 4-21. These include the type of collector (flat plate, etc.), module cooling parameters (which may often be specified by default values) and energy storage characteristics. A complete discussion of input requirements and characteristics is contained in the SOLCEL II users manual [2].

The SOLCEL II inputs used to demonstrate the modeling with the polycrystalline silicon residential application are listed in Table 4-22. The array was located at 35° north latitude and tilted at 35° south from the horizontal. Electric load data for a typical gas heated home in Albuquerque was chosen from the available data base because this more nearly approximates the reduced electrical demand of a passive solar, energy efficient, all electric residence of the future than the data from existing all electrical residences. The residential systems are designed to convert the array dc into utility compatible ac power to operate in parallel with the public utility. Since SOLCEL II is not designed to handle electricity sold to the utility, any excess energy produced is cataloged by SOLCEL II as wasted energy. To assess the effect of utility purchase of residential PV electri-

city, the user can multiply the excess energy by the average inverter efficiency and an appropriate selling price. The dc to ac inverter specified in the design process is a 6-kW solid state inverter with maximum efficiency at full load of 90 percent. The tare power is 160 W and the maximum dc power which the inverter will accept before shutdown is 6.6 kW.

Table 4-21. SOLCEL II INPUT REQUIREMENTS

- Latitude and Tilt Angle
- Load and Weather (SOLMET TMY) Data
- Inverter Data
 - Rated Power
 - Efficiency at Full Load
 - Maximum and Minimum (Tare) Powers
- Low and High Insolations
- Low and High Temperatures
- Cell Parameters
 - Short Circuit Current and Open Circuit Voltage Matrix (at Low and High Insolations and Temperatures)
 - Series Resistance (R_s)
 - Device Constants (A_0 and E_{G0})
 - Cell Area
- Module and Array Parameters
 - Module Dimensions and Packing Factor
 - Number of Modules in Array

The matrix of short circuit current and open circuit voltage values used in this modeling demonstration are also contained in the table. The two superscript designations on I_{SC} and V_{OC} refer to insolation and temperature respectively. Thus, I_{SC}^{HL} indicates the short-circuit current at high insolation and low temperature. In the actual SOLCEL II runs on the various applications, the low insolation value will be 0.1 sun instead of 0.5 sun used for this modeling demonstration. The short circuit currents and series resistance are cell unit-area values.

Table 4-22. SOLCEL II INPUTS FOR MODELING OF POLYCRYSTALLINE SILICON RESIDENTIAL APPLICATION

- Latitude and Tilt Angle - 35°N and 35°
- Load Data - Albuquerque Gas Heated Home
- Power Conditioning
 - 6 kW DC-AC Inverter
 - Turn-off at 6.6kW DC
 - Efficiency = 90% at Full Load
 - Tare Power = 160W
- Insolation and Temperature Limits

$S_L = 0.5 \text{ Sun}; S_H = 1.0 \text{ Sun}$

$T_L = 15^\circ\text{C}; T_H = 75^\circ\text{C}$
- $*I_{SC}^{LL} = 124.4 \text{ A/m}^2, V_{OC}^{LL} = 0.599 \text{ V}$
 $I_{SC}^{HL} = 248.8 \text{ A/m}^2, V_{OC}^{HL} = 0.655 \text{ V}$
 $I_{SC}^{LH} = 129.5 \text{ A/m}^2, V_{OC}^{LH} = 0.466 \text{ V}$
 $I_{SH}^{HH} = 259.0 \text{ A/m}^2, V_{OC}^{HH} = 0.49 \text{ V}$
- $R_S = 4.0\text{E-}5 \Omega\text{-m}^2$
- $A_{CELL} = 85.1\text{E-}4 \text{ m}^2$
- Packing Factor = 0.933
- Module Dimensions = 1.207m x 1.207m; Number of Modules = 30

*Note: First Superscript = Insolation
 Second Superscript = Temperature

The annual energy distribution obtained from the SOLCEL II run is contained in Table 4-23. The total DC energy produced by the array was 11,156 kW-hrs. The array satisfies 2,540 kW-hrs of the load demand of 6,616 kW-hrs. The rest of the load demand is supplied by the utility. The energy sold to the public utility company would be that listed as "WASTED ARRAY ENERGY (DC)".

Both the array dc power and the ac load demand for each hour of the day are plotted in Figures 4-12 through 4-15 for March 21, June 20, September 20, and December 20, respectively. Histograms assessing the occurrence of load demand levels and array dc power levels are shown in Figures 4-16 and 4-17, respectively. These histograms illustrate the value of selling power to utility since the array has higher occurrence of high power levels than the load demand. Without utility purchase, most of the array energy would be wasted. These plots are not standard output of SOLCEL II, but were generated to illustrate the type of creative plotting which can be done by adding plotting routines to SOLCEL II.

4.2.2 SOLCEL II Specific Application Modeling

The inputs used for the SOLCEL II analyses which are common to all eight advanced PV technology applications are summarized in Table 4-24. These are in the form previously presented in Table 4-21. The values shown in Table 4-24 are also similar to those presented for the polycrystalline silicon residential modeling demonstration run in Table 4-22. However, some differences can be found. The load for the CPS applications is the utility grid which is being fed by the CPS array. The CPS inverter has a rated power of 2.2 MW. The efficiency is 87.65 percent for the remaining runs as opposed to 90 percent for the modeling demonstration run. This efficiency was obtained by incorporating all the power conditioning efficiencies discussed in Section 3.0 into the inverter efficiency model. The tare power and the maximum power are presented here as percentages of the rated power; however, these represent the same numbers as previously used for the 6 kW application.

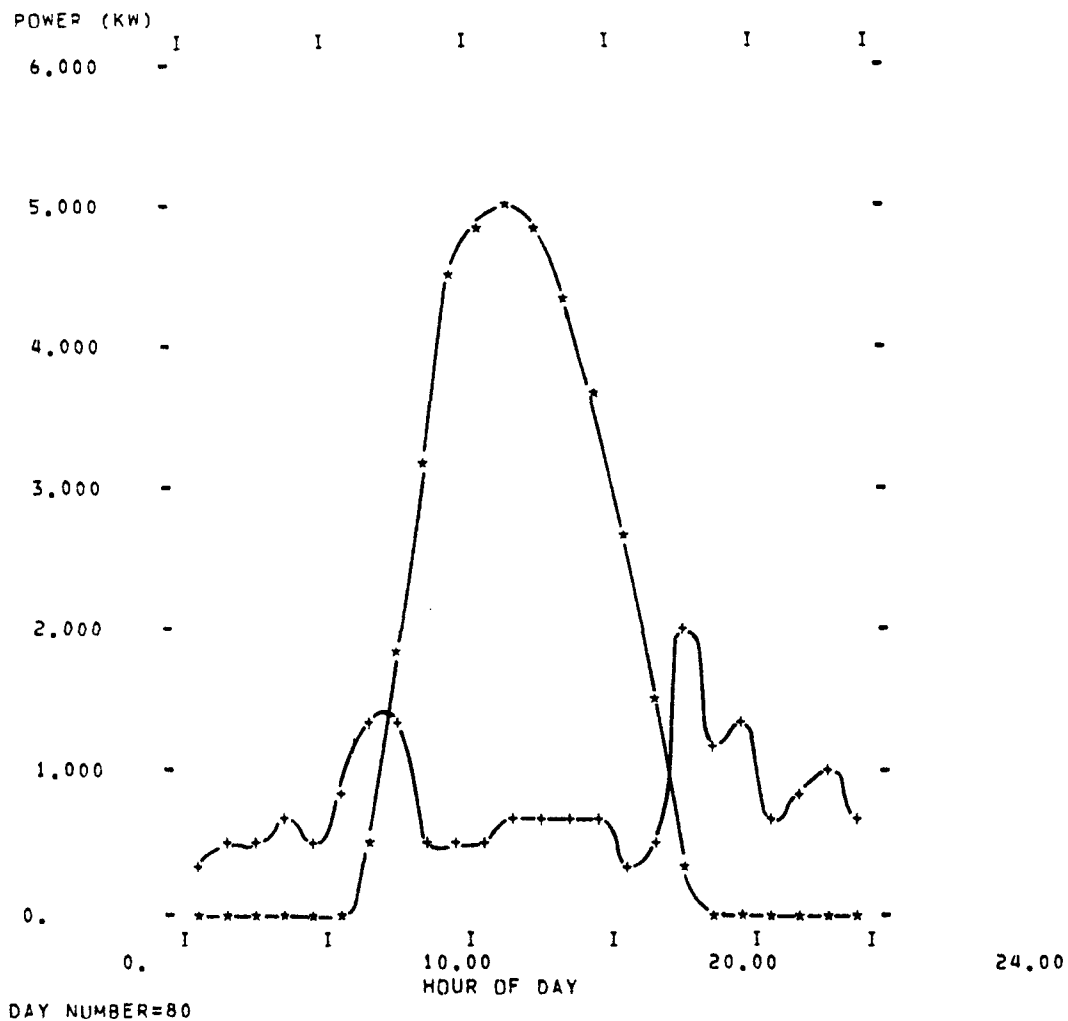
The low insolation value has been changed from the 0.5 sun value used in the demonstration run to 0.1 suns in order to more clearly bound the PV cell data. High and low insolation and temperature values are also presented in this table for the concentrator application.

Additional inputs required by SOLCEL II which vary with technology and cell area are summarized in Table 4-25. The numbers and symbols listed along the left column correspond to those used in the SOLCEL II user's manual [2] and are provided to assist the reader in understanding the inputs. For the flat plate applications, both residential and CPS, the short circuit current and open circuit voltage matrix versus insolation and temperature were determined from PV-TAP insolation and temperature variation analyses to more accurately model the inputs to SOLCEL II than could be accomplished using the simple, hand-calculation techniques in the conceptual design phase. The series resistances were determined from the insolation variation analyses. On the

**Table 4-23. SOLCEL II OUTPUT LISTING FOR POLYCRYSTALLINE
SILICON RESIDENTIAL ARRAY**

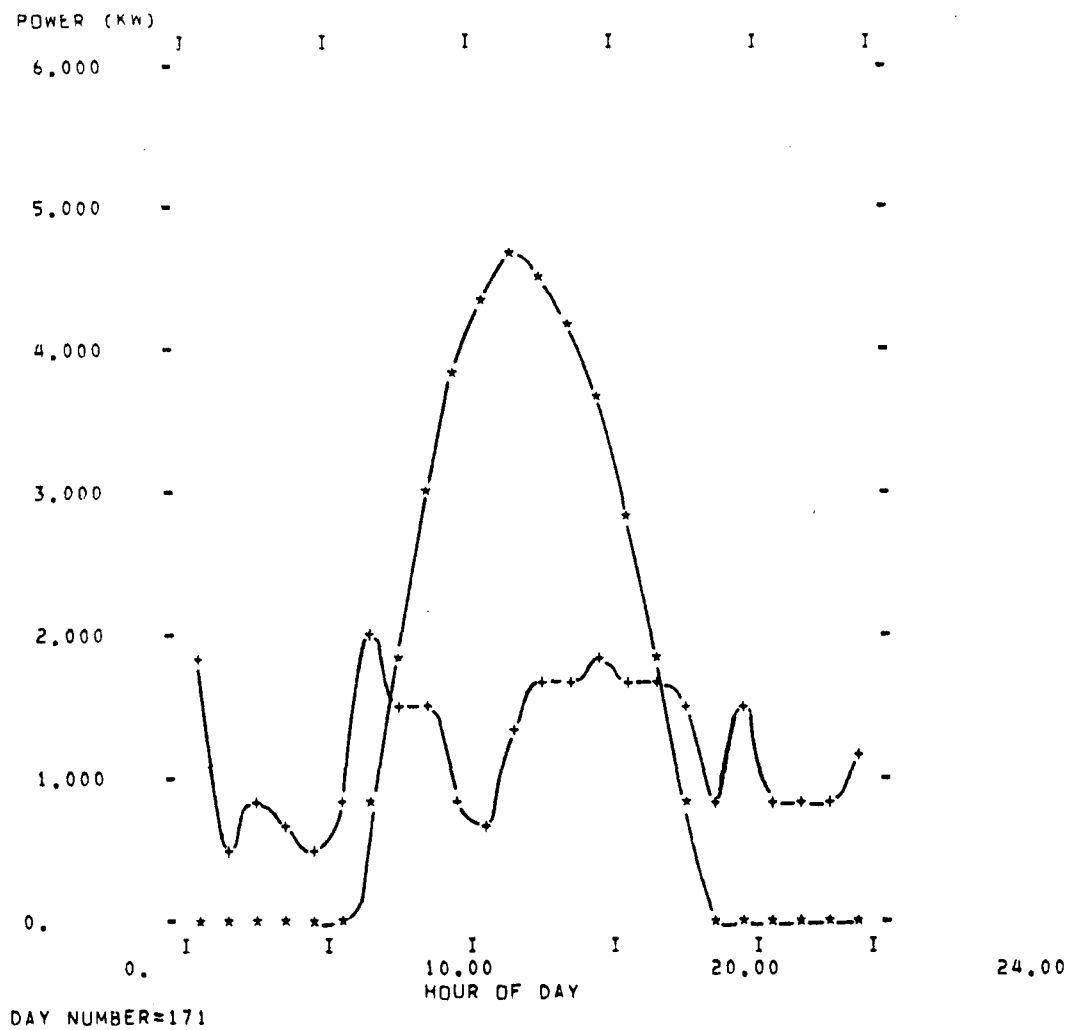
ANNUAL ENERGY DISTRIBUTION	TOTAL KW-HRS
-----	-----
TOTAL AVAILABLE INSOLATION	135346.75
TOTAL INSOLATION RECEIVED	103990.29
TOTAL ARRAY ENERGY(DC)	11155.98
ARRAY ENERGY(AC) TO LOAD	2540.32
BATTERY ENERGY(AC) TO LOAD	0.00
BACK-UP ENERGY(AC) TO LOAD	4075.48
LOAD DEMAND	6615.80
SYSTEM INTERNAL ENERGY	0.00
BATTERY CHARGING ENERGY	0.00
BATTERY DISCHARGING ENERGY	0.00
WASTED ARRAY ENERGY(DC)	7745.28

INVERTER WAS TURNED OFF 0 TIMES BECAUSE OF OVERLOAD GT 10 PERCENT



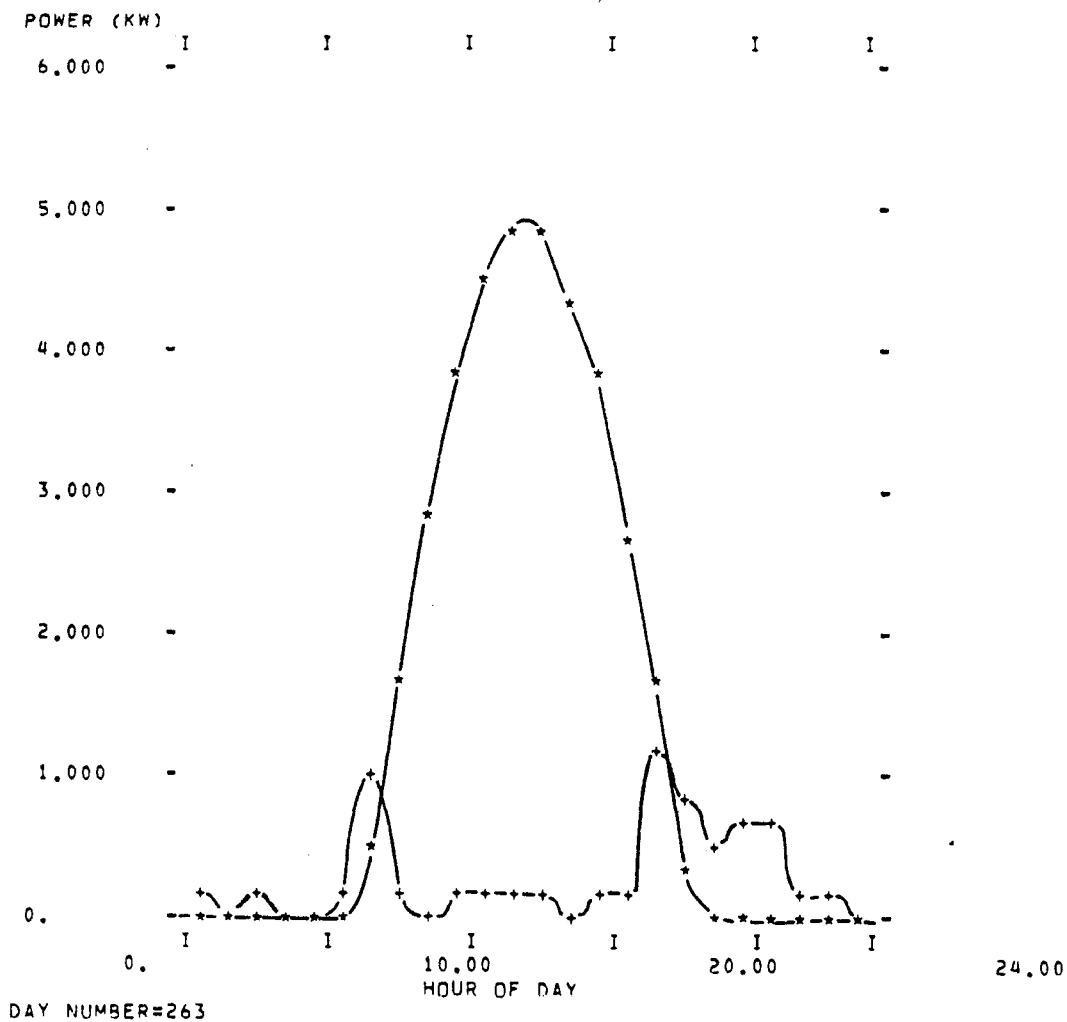
LEGEND: * = DATA POINT FOR PV SYSTEM OUTPUT
+ = DATA POINT FOR RESIDENTIAL LOAD

Figure 4-12. ARRAY POWER AND LOAD DEMAND FOR 21 MARCH



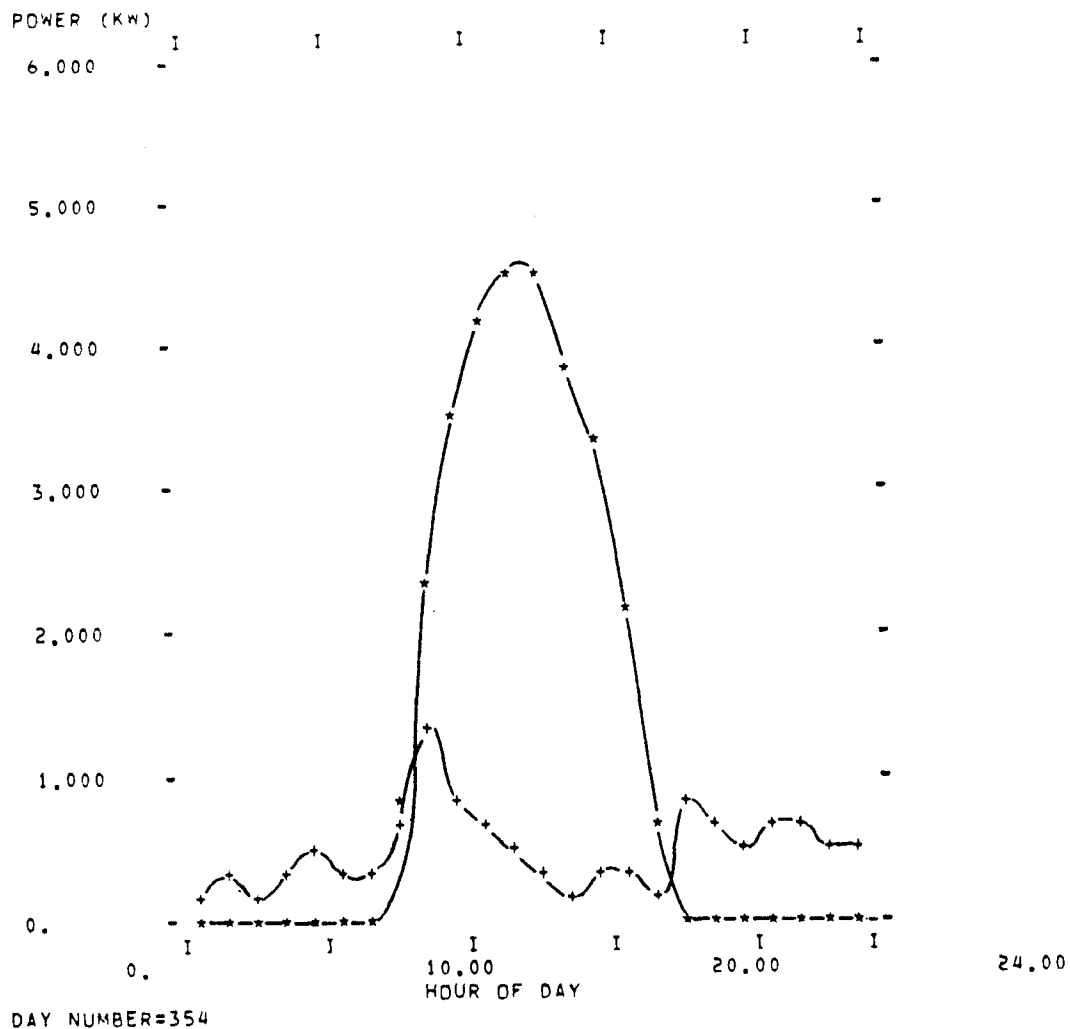
LEGEND: * = DATA POINT FOR PV SYSTEM OUTPUT
 + = DATA POINT FOR RESIDENTIAL LOAD

Figure 4-13. ARRAY POWER AND LOAD DEMAND FOR 20 JUNE



LEGEND: * - DATA POINT FOR PV SYSTEM OUTPUT
 + - DATA POINT FOR RESIDENTIAL LOAD

Figure 4-14. ARRAY POWER AND LOAD DEMAND FOR 20 SEPTEMBER



LEGEND: * = DATA POINT FOR PV SYSTEM OUTPUT
 + = DATA POINT FOR RESIDENTIAL LOAD

Figure 4-15. ARRAY POWER AND LOAD DEMAND FOR 20 DECEMBER

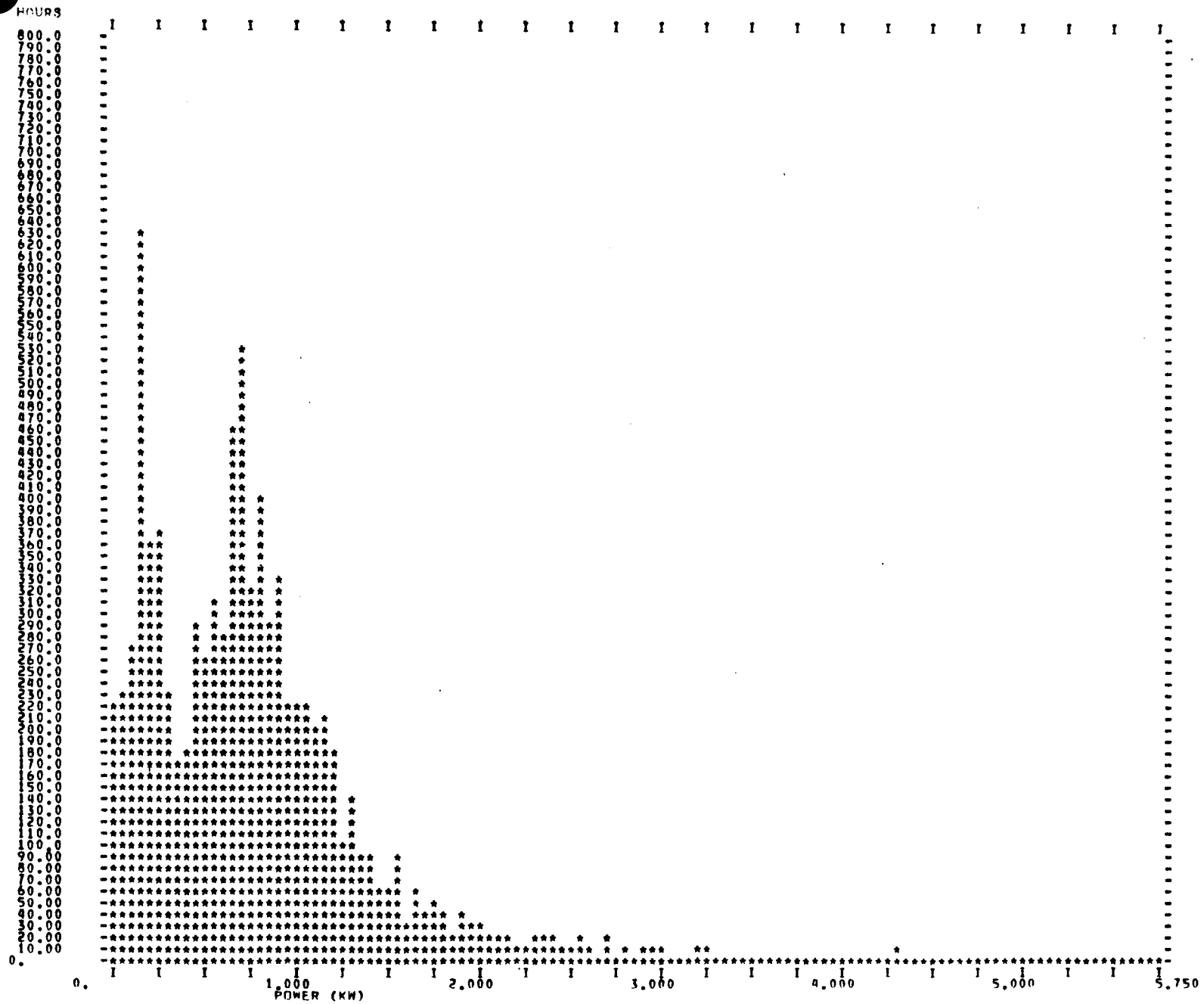


Figure 4-16. HISTOGRAM OF HOURLY OCCURRENCE OF LOAD POWER DEMAND

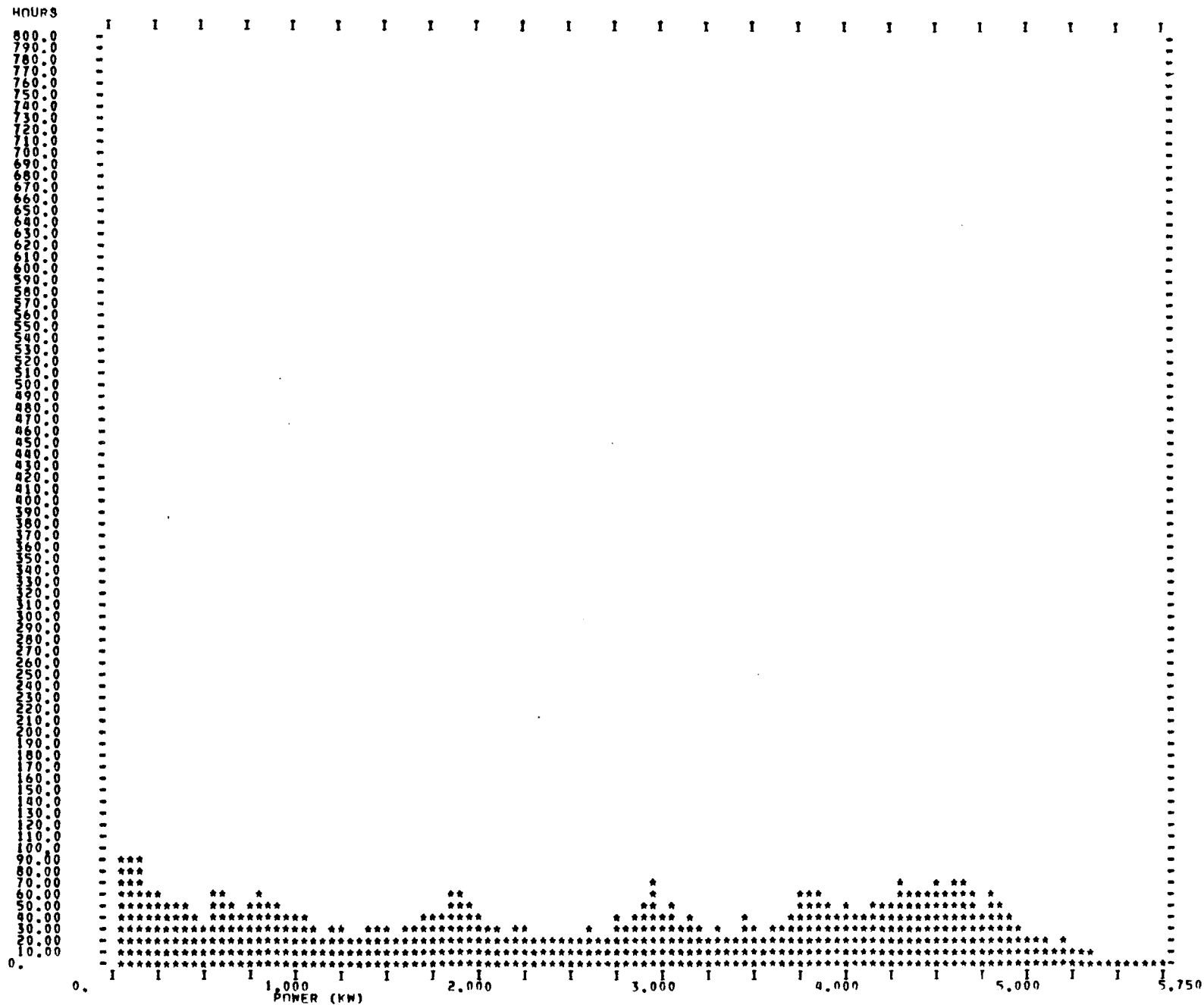


Figure 4-17. HISTOGRAM OF HOURLY OCCURENCE OF ARRAY OUTPUT POWER

**Table 4-24. SOLCEL II INPUT REQUIREMENTS FOR
ADVANCED PV TECHNOLOGIES**

SAME FOR ALL APPLICATIONS

- LATITUDE (35°N) AND TILT ANGLE (35°)
- RESIDENTIAL LOAD DATA (ALBUQUERQUE GAS HEATED HOME);
CPS LOAD (UTILITY GRID)
- INVERTER – 6 kW RESIDENTIAL OR 2.2 MW CPS
 - EFFICIENCY – 87.65% AT FULL LOAD
 - TARE POWER – 2.67% OF RATED POWER
 - MAXIMUM POWER – 10% ABOVE RATED POWER
- A_0 , E_{GO} – DEFAULT VALUES
- LOW AND HIGH INSOLATION
 - 0.1 AND 1.0 SUN FOR FLAT PLATE
 - 50 AND 500 SUN FOR CONCENTRATOR
- LOW AND HIGH TEMPERATURE
 - 15°C AND 75°C FOR FLAT PLATE
 - 50°C AND 120°C FOR CONCENTRATOR

Table 4-25. SOLCEL II INPUTS SUMMARY

SOLCEL II	DEFINITION	POLY-Si		a - Si		CdS/CuInSe ₂		GaAs	
		RES	CPS	RES	CPS	RES	CPS	RES	CPS
3	LOW INSO	100	100	100	100	100	100	100	
4	HIGH INSO	1000	1000	1000	1000	1000	1000	1000	
5	LOW TEMP	15	15	15	15	15	15	15	
6	HIGH TEMP	75	75	75	75	75	75	75	
7	I _{LI} LT	24.86	24.89	15.92	15.93	38.99	39.09	24.85	
8	I _{HI} LT	248.6	248.9	159.20	159.3	389.9	390.9	248.5	
9	I _{LI} HT	25.79	25.81	16.51	16.51	40.42	40.51	25.75	
10	I _{HI} HT	257.9	258.10	165.10	165.1	404.2	405.1	257.54	
11	V _{LI} LT	.540	.54	.71	.71	.401	.401	.931	
12	V _{HI} LT	.621	.621	.923	.923	.449	.449	1.00	
13	V _{LI} HT	.408	.408	.614	.614	.269	.269	.739	
14	V _{HI} HT	.494	.494	.842	.842	.323	.323	.815	
15	SERIES RESISTOR	4E-5	4E-5	5.3E-6	5.3E-6	2.05E-4	2.05E-4	1.6E-4	
PVTT		6E3	2.2E6	6E3	2.2E6	6E3	2.2E6	6E3	2.2E6
CL		1.207	1.207	1.207	1.207	1.207	1.207	1.207	2.367
CW		36.21	17477.36	41.72	21366.6	42.17	18807.47	20.2	6602.8
PACFAC		.933	.943	.90	.886	.921	.932	.913	.726
CONRA		1	1	1	1	1	1	1	500
ARLENS									.08065
ARSINK									1.267E-4
CTP									.1
TFI									300
TFO									400
ICTYPE		2	2	2	2	2	2	2	8
IECON		1	4	1	4	1	4	1	4
EFFC		.115	.115	.10	.10	.108	.108	.20	.4452
EPVEFM		1	1	1	1	1	1	1	4
COEF									.0066

other hand, the SOLCEL II analysis of the concentrator application used the efficiency versus temperature methodology option in SOLCEL II because problems were encountered with extreme deviation in the device constant (K_{pgv}) calculated by SOLCEL II, as part of the saturation current coefficient. This may have been caused by the use of default values for A_0 and E_{G0} . The efficiencies at 50°C and 120°C were obtained from the PV-TAP temperature variation analysis.

The flat plate runs used default values for the module heat transfer parameters and produced acceptable results in all cases. The concentrator application, however, required specification of non-default heat transfer parameters for a fully-tracking collector. These parameters are also listed in Table 4-25.

4.2.3 SOLCEL II Performance Evaluation

Table 4-26 summarizes the results of the SOLCEL II analyses. For the residential applications, the annual totals are presented for total available insolation, total insolation received by the array (sun is usually not normal to array surface), total array dc energy produced, total ac energy supplied to the load, backup energy (from utility) required by the load, total load demand, and the energy sold to the utility. For the CPS applications, all ac energy is supplied to the load which is the utility grid. The concentrator application also includes system parasitics. The table also includes the array ac energy which might be produced under photocurrent variation conditions. This was obtained for the residential systems by adding the ac energy supplied to the load to the ac energy supplied to the utility and then, multiplying this by the results of the PV-TAP photocurrent variations analyses for cell photocurrent variations of + 10, + 20 and + 50 percent. For the CPS systems, however, the ac energy supplied to the load was used as the baseline since all energy produced is supplied to the load.

4.3 ECONOMIC ANALYSIS

The economic analysis is comprised of two elements, a Life Cycle Cost (LCC) developed for the 4 KW residential systems, and a required revenue developed for the 50 MW Central Power Station (CPS) systems. Section 4.3.1 presents the standard costs and financial parameters used throughout the remainder of the section. Section 4.3.2 consists of discussion of the LCC methodology used for the analysis of the residential systems and the different technology array characteristics and LCCs. Section 4.3.3 contains a discussion of the required revenue methodology used for analysis of the CPS systems and presents the different technology array parameters and required revenues. An assessment of the economic analysis results and procedures is presented in section 5.1.5.

Table 4-26. SOLCEL II RESULTS SUMMARY

ANNUAL ENERGY DISTRIBUTION (kWh)	RESIDENTIAL 4 kW ARRAY			
	POLY-Si	a-Si	CdS/CuInSe ₂	GaAs
TOTAL AVAILABLE INSOLATION	135,384 kWh	155,985	157,668	75,525
TOTAL INSOLATION RECEIVED	103,705	119,486	120,775	57,853
PRODUCED DC ENERGY	10,775	10,968	10,938	9,681
AC ENERGY SUPPLIED TO LOAD	2,494	2,489	2,581	2,414
UTILITY ENERGY TO THE LOAD	4,121	4,126	4,034	4,201
LOAD DEMAND	6,616	6,616	6,616	6,616
ENERGY SOLD TO UTILITY	5,338	5,481	5,412	4,584
TOTAL AC ENERGY PRODUCED	7,832	7,970	7,993	6,998
10 PERCENT VARIATION IN PHOTOCURRENT	7,410	7,577	7,647	6,782
20 PERCENT VARIATION IN PHOTOCURRENT	6,978	7,173	7,286	6,519
50 PERCENT VARIATION IN PHOTOCURRENT	5,522	5,978	5,979	5,500

ANNUAL ENERGY DISTRIBUTION MWh	CPS 2.2 MW ARRAY			
	POLY-Si	a-Si	CdS/CuInSe ₂	GaAs
TOTAL AVAILABLE INSOLATION	65,345 MWh	79,887	70,319	40,844
TOTAL INSOLATION RECEIVED	50,055	61,194	53,865	40,844
PRODUCED DC ENERGY	5,261	5,532	4,946	6,686
AC ENERGY SUPPLIED TO LOAD	4,494	4,730	4,211	5,775
SYSTEM PARISITICS				33
TOTAL AC ENERGY PRODUCED	4,494	4,730	4,211	5,775
10 PERCENT VARIATION IN PHOTOCURRENT	4,244	4,487	4,048	5,562
20 PERCENT VARIATION IN PHOTOCURRENT	3,982	4,238	3,889	5,322
50 PERCENT VARIATION IN PHOTOCURRENT	3,033	3,349	3,390	4,297

4.3.1 Standard Costs and Financial Parameters

Since real cost data are not available for the technologies studied, published cost projections are used to determine the installed array cost for each PV technology [42, 43, 44, 45]. These cost projections include system peak output (ac) proportional costs, array area proportional costs, and PV module costs/ W_p . The implication of this analytical approach is that PV module efficiency will be the determining factor of relative system cost effectiveness. The costs are differentiated by type of system and year of first system installation. The proportional costs used for this study, displayed in Table 4-27, are the same for all technologies.

Typical financial parameters are used for the economic analysis of each generic type of PV system. These parameters are displayed in Table 4-28. Most of the parameters are self-explanatory.

The base year is the cost year, 1981. The start-up year is the first year that these costs are projected to be reasonable cost estimates. The 1981 dollar costs are used for the initial start-up year costs. SOYD stands for "Sum of the Years Depreciation."

4.3.2 Residential System Economic Analysis

The LCC methodology used for analysis of the advanced PV residential systems is based upon a discounted cash flow algorithm as developed by A. M. Perino [46] and modified by E. R. Hoover [2]. The Hoover modifications have been incorporated in the Sandia National Labs SOLCEL II PV system computer model. This methodology has been further modified by BDM to account for energy sold back to the electric utility. The buy-back rate used for this study is 0.5.

Input parameters and costs and the resulting residential LCC's are presented in Table 4-29a. Two LCC's are given for each technology, Present Value and annual cost. The Present Value is the sum of all system life cash flows discounted back to the time of system startup. The annual LCC is the self-amortizing annual cost of the system Present Value.

4.3.3 CPS System Economic Analysis

The required revenue methodology used for analysis of the CPS systems is based upon a discounted cash flow algorithm developed by W. C. Dickinson and K. C. Brown [47]. This algorithm determines the annual revenue required to amortize the discounted system costs over the life of the PV system. This annual cost, when divided by the system annual electrical output yields the production cost of electricity.

Input parameters and costs and the resulting CPS required revenues are presented in Table 4-29b.

Table 4-27. ECONOMIC INPUTS: STANDARD COST ELEMENTS

COST ELEMENT	PV SYSTEM	
	RESIDENTIAL (1986)	CENTRAL POWER STATION (1989)
1. OUTPUT PROPORTIONAL COSTS (\$/kWp)		
ENGINEERING	320	200
BUILDINGS	80	70
POWER CONDITIONING	500	130
TOTAL	\$900/kWp	\$400/kWp
2. AREA PROPORTIONAL COSTS (\$/M ²)		
STRUCTURE	42	35
CIVIL WORK	18	15
ELECTRICAL	20	11
LAND	—	6
TOTAL	\$80/M ²	\$67/M ²
3. ARRAY COST	\$ 3.87/Wp	\$ 0.96/Wp

Table 4-28. FINANCIAL AND SYSTEM PARAMETERS

	RESIDENTIAL (4 kW)	CPS (50 MW)
DISCOUNT RATE	.10	.10
LOAN INTEREST RATE	.12	.12
DOWN PAYMENT (%)	.2	.2
INCOME TAX RATE	.3	.5
GENERAL INFLATION RATE	.09	.09
ELECTRICAL ESCALATION RATE	.10	—
INVESTMENT TAX CREDIT	—	.15
SOLAR TAX CREDIT	.40	.25
UTILITY BUY BACK RATE	.5	—
O&M RATE	.02	.015
PROPERTY TAX/INSURANCE	.02	.02
SALVAGE VALUE	.1	.1
ELECTRICITY COST	.067/kWH	—
BASE YEAR	1981	1981
START UP YEAR	1986	1989
SYSTEM LIFE	20 Y	20 Y
LOAN LIFE	5 Y	20 Y
ACCOUNTING LIFE	—	7 Y
DEPRECIATION METHOD	—	SOYD

**Table 4-29a. ECONOMIC RESULTS SUMMARY: RESIDENTIAL
SYSTEMS PARAMETERS AND COSTS**

PARAMETER	PV TECHNOLOGY			
	p - Si	a - Si	CdS/CuInSe ₂	Ga/As
ARRAY SIZE (M ²)	43.7	50.4	50.8	24.4
PEAK OUTPUT (kWp AC)	4.1	4.0	4.4	3.9
ANNUAL OUTPUT (kWh AC)	7832	7970	7993	6999
ANNUAL RESIDENTIAL LOAD (kWh AC)	6615	6615	6615	6615
ANNUAL OUTPUT TO LOAD (kWh AC)	2494	2489	2581	2415
BACK UP ENERGY (kWh AC)	4121	4126	4034	4200
OUTPUT PROPORTIONAL COST (\$)	3690	3582	3978	3510
AREA PROPORTIONAL COST (\$)	3494	4033	4068	1949
PV ARRAY COST (\$)	15867	15403	17105	15093
SYSTEM PRESENT VALUE (\$)	27107	26980	29234	24991
ANNUAL LCC (\$)	3184	3169	3434	2935

**Table 4-29b. ECONOMIC RESULTS SUMMARY: CPS SYSTEMS
PARAMETERS AND COSTS**

PARAMETER	PV TECHNOLOGY			
	p - Si	a - Si	CdS/CuInSe ₂	GaAs
ARRAY SIZE (M ²)	21,095	25,789	22,701	15,629
PEAK OUTPUT (kWp AC)	1,954	1,954	1,946	2,270
ANNUAL OUTPUT (kWH x 1000 AC)	4,494	4,730	4,211	5,775
OUTPUT PROPORTIONAL COST (\$)	781,600	781,600	778,400	908,000
AREA PROPORTIONAL COST (\$)	1,413,400	1,727,900	1,521,000	1,047,100
PV ARRAY COST (\$)	1,875,800	1,875,800	1,868,200	2,179,200
ANNUAL REQUIRED REVENUE (\$/Y)	516,400	556,300	528,600	524,400
PRODUCTION COST (\$/kWH)	0.115	0.118	0.126	0.091



SECTION 5.0

DESIGN AND ANALYSIS ASSESSMENTS AND GUIDELINES

The results of the conceptual design analyses were assessed to provide recommendations and guidelines for advanced PV technology development and analysis. An overview of the assessment and guideline development format is shown in Figure 5-1. Based on the conceptual designs and the cost/performance analyses performed on them, the results were analyzed and the implications of the results on the design and analysis procedures were assessed. These assessments are included in Section 5.1. Following this design and analysis assessment, the characteristics of each technology were assessed and guidelines were developed for advanced PV technologies in general and also for the specific technologies considered in this study. These technology guidelines are presented in Section 5.2. Finally, the recommendations for design and analysis procedures, contained throughout Sections 5.1 and 5.2, were compiled and summarized into guidelines for design and analyses in Section 5.3.

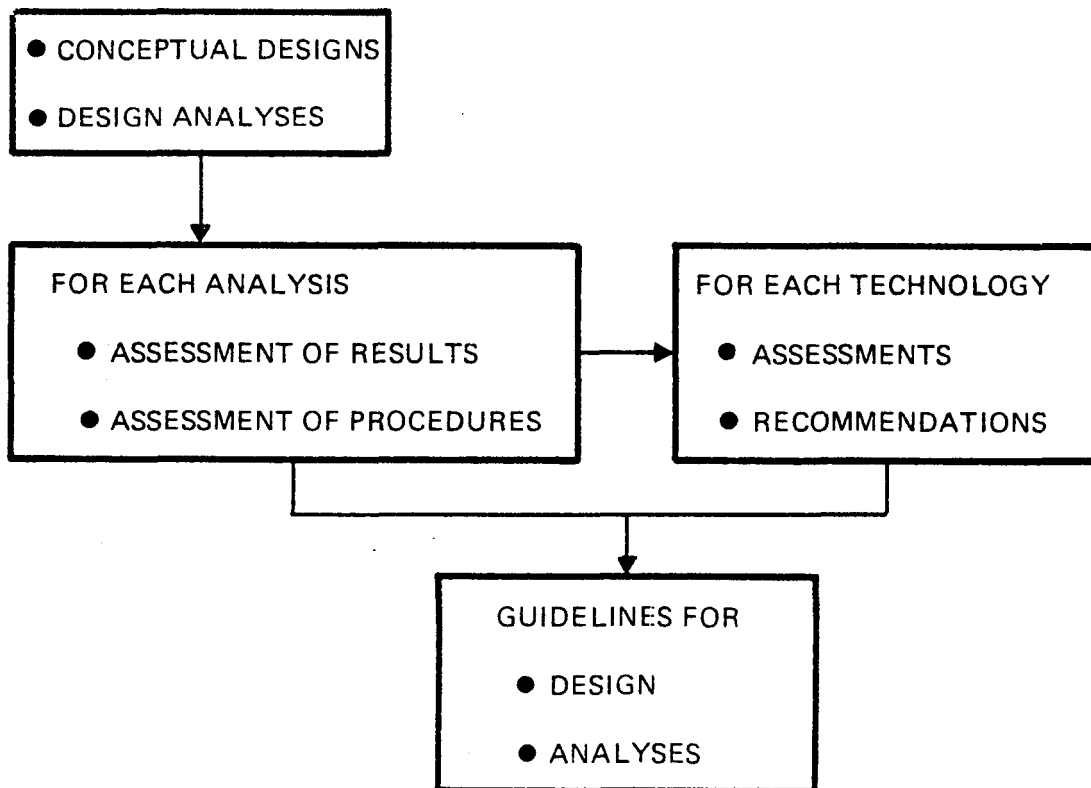


Figure 5-1. DIAGRAM OF DESIGN AND ANALYSIS ASSESSMENT AND GUIDELINES

5.1 ASSESSMENTS OF RESULTS AND PROCEDURES

The results are shown to be consistent with theory. Trends in the results are noted and comparisons between applications are made where appropriate. The impact of design and analysis procedures is discussed and recommendations for improvements in the procedures are presented where appropriate.

5.1.1 Insolation and Temperature Variations

Analyses of the effects of insolation and temperature variations were performed for each technology using the PV-TAP computer program. The analyses were performed to more accurately quantify the current, voltage and power produced by the modules at extremes of insolation and temperature than were obtained in the conceptual design process from simplified equations. The results can also be used as inputs to SOLCEL II analyses of annual energy distribution. To obtain the powers, currents and voltages for each array the module values need only be factored by the number of modules in series and parallel within the array.

5.1.1.1 Assessment of Results

The output powers obtained from the analyses for each application are summarized in Table 5-1; the short circuit currents and open circuit voltages obtained are summarized in Table 5-2. In general, the values matched the nominal values from the conceptual designs, but the variations at the temperature extremes exceed those obtained from the simplified equations used in the conceptual design process. As might be expected, the output power is not linear with insolation. The increasing slope (superlinearity) of the power with insolation seen in most of the applications is a combination of the linear response of the short circuit current with insolation and the logarithmic response of the open circuit voltage with insolation. An exception to this trend is seen in the CdS/CuInSe₂ applications, in which the power has a decreasing slope (sublinear) between 0.5 sun and 1.0 sun. This is caused by the high series resistance for this technology which reduces the output voltage at high insolation. Therefore, the CdS module efficiencies are higher at 0.5 suns than at 1.0 sun.

5.1.1.2 Assessment of Procedures

The analysis for the effects of insolation and temperature variations was simple to formulate and perform. Two families of characteristics were obtained for each application. First, the temperature was set at the nominal design temperature (25°C for flat plate and 100°C for concentrators) and the insolation was varied in steps from 1/10 the design

Table 5-1. INSOLATION AND TEMPERATURE RESULTS, OUTPUT POWER (W)

TECHNOLOGY:	POLY SI		aSI		CdS		GaAs
APPLICATION:	RES	CPS	RES	CPS	RES	CPS	RES
INSOLATION	(W)	(W)	(W)	(W)	(W)	(W)	(W)
.1 SUN	11.33	22.86	1.976	1.952	9.615	29.04	8.223
.5 SUN	73.98	149.1	14.58	14.40	52.08	157.2	44.09
1.0 SUN	156.5	315.7	32.48	32.06	97.55	294.7	88.81
TEMPERATURE							
15°C	163.0	328.6	33.16	32.73	104.4	315.1	91.96
25°C	156.5	315.7	32.48	32.06	97.55	294.7	88.81
75°C	123.7	249.0	28.84	28.67	63.76	192.4	72.45

TECHNOLOGY:	GaAs
APPLICATION:	CPS
INSOLATION	(W)
50 SUNS	82.11
250 SUNS	476.3
500 SUNS	1007
TEMPERATURE	
50°C	1568
100°C	1007
120°C	781.9

Table 5-2. INSOLATION AND TEMPERATURE RESULTS, SHORT CIRCUIT CURRENT AND OPEN CIRCUIT VOLTAGE

TECHNOLOGY	POLY-SILICON		A-SILICON		CdS/CuInSe ₂		GaAs
APPLICATION	RES	CPS	RES	CPS	RES	CPS	RES
INSOLATION	(A) / (V)	(A) / (V)	(A) / (V)	(mA) / (V)	(A) / (V)	(A) / (V)	(A) / (V)
0.1 SUN	0.85/20.7	0.68/51.8	0.37/9.72	73.0/48.6	0.71/19.0	0.67/60.7	0.46/21.6
0.5 SUN	4.26/23.1	3.43/57.7	1.85/11.9	365./59.4	3.53/20.7	3.33/66.2	2.32/22.8
1.0 SUN	8.52/24.0	6.87/60.0	3.70/12.7	730./63.7	7.07/21.4	6.67/68.5	4.63/23.3
TEMPERATURE							
15°C	8.46/24.8	6.83/62.1	3.68/12.9	726./64.7	7.02/22.4	6.63/71.8	4.60/24.1
25°C	8.52/24.0	6.87/60.0	3.70/12.7	730./63.7	7.07/21.4	6.67/68.5	4.63/23.3
75°C	8.78/19.8	7.08/49.4	3.81/11.8	752./58.9	7.28/16.1	6.87/51.7	4.77/19.5

TECHNOLOGY	GaAs
APPLICATION	CPS
INSOLATION	(A) / (V)
50 SUNS	2.22/50.6
250 SUNS	11.1/57.2
500 SUNS	22.2/60.0
TEMPERATURE	
50°C	21.5/87.6
100°C	22.2/60.0
120°C	22.5/48.9

insolation up to the full design insolation. Then, the insolation was held constant at the design insolation (1.0 sun for flat plate and 500 sun for concentrator) and the temperature was varied in steps from the lower limits to the upper limits specified in the conceptual designs. Since no PV-TAP calculations were performed which combined the low temperature and low insolation limits, the short circuit current and open circuit voltage values for these conditions were obtained for the SOLCEL II runs from hand calculations based on the low insolation and design temperature results. Therefore, some inaccuracy was introduced into the SOLCEL II analyses. Analyses performed in the future should be formulated to ensure obtaining these values from PV-TAP runs.

5.1.2 Photocurrent Variations

Analyses were performed to assess the reduction in output power resulting from cell to cell variations in photocurrent generation. The analyses were performed using the PV-TAP computer program. Since no data exists at present on photocurrent variations in advanced PV technologies, the analyses were performed as parametric studies. The analyses were performed with Gaussian distributions on the cell photocurrents. The upper and lower three sigma (3σ) points of the distributions were specified as 10, 20 and 50 percent from the nominal value. The results provide an assessment of the actual power which might be obtained from an advanced PV technology application since the cell to cell variation in photocurrent is the most critical parameter which prevents the array from producing the output power expected. The results of photocurrent variation analyses can also be used to factor the annual energy production obtained from SOLCEL II analyses to obtain a more realistic assessment of annual ac energy produced.

5.1.2.1 Assessment of Results

The photocurrent distribution results are summarized in Table 5-3 in terms of array power output and percent power loss from the nominal case for all 8 technology applications. In addition, the results of a parametric study on interconnection variation are also presented for the gallium arsenide residential application. In the module developed for this application, individual cells are first connected in parallel before cells are connected in series to form a bypass group, in opposition to the other modules in which cells are first connected in series to form bypass groups with paralleling performed only at the group level. The P2S6 designation shown in parentheses indicates an interconnection scheme with two cells in parallel, then six of these groups in series. The interconnection variation consisted of connecting six cells in series first to form the bypass group with two bypass groups in parallel in an interconnection technique similar to that used for all other modules. It can be seen clearly that connecting cells in parallel increases the

**Table 5-3. PHOTOCURRENT DISTRIBUTION RESULTS, ARRAY/SUBARRAY
POWER OUTPUT (W) AND PERCENT POWER LOSS FROM NOMINAL**

TECHNOLOGY	POLY SI		aSi		CdS		GaAs		
APPLICATION	RES	CPS	RES	CPS	RES	CPS	RES (P2S6)	RES (S6P2)	CPS
30 - % FROM AVG. 0	4.698 kW	2.286 MW	4.546 kW	2.297 MW	5.075 kW	2.292 MW	4.441 kW	4.441 kW	2.257 MW
10	4.445 kW 5.39%	2.159 MW 5.56%	4.322 kW 4.93%	2.181 MW 5.13%	4.855 kW 4.33%	2.203 MW 3.88%	4.304 kW 3.08%	4.245 kW 4.41%	2.174 MW 3.68%
20	4.184 kW 10.9%	2.026 MW 11.4%	4.096 kW 10.0%	2.059 MW 10.4%	4.626 kW 8.85%	2.117 MW 7.64%	4.137 kW 6.85%	3.934 kW 11.4%	2.080 MW 7.84%
50	3.314 kW 29.5%	1.542 MW 32.5%	3.410 kW 25.0%	1.627 MW 29.2%	3.794 kW 25.2%	1.844 MW 19.5%	3.492 kW 21.4%	3.051 kW 31.3%	1.680 MW 25.6%

Table 5-4. ASSESSMENT OF FACTORS AFFECTING PHOTOCURRENT VARIATION RESPONSES

VALUE/RANKING	POLY-SILICON		A-SILICON		CdS/CuInSe ₂		GaAs		
	RES	CPS	RES	CPS	RES	CPS	RES (S6P2)	RES (P2S6)	CPS
BYPASS GROUP SIZE	10/4*	10 / 4	7 / 3	7 / 3	10 / 4	10 / 4	6 / 2	6 / 2	4 / 1
PARALLELING IN MODULE	4 / 2	3 / 3	10 / 1	2 / 4	4 / 2	4 / 2	2 / 4	2 / 4	2 / 4
FILL FACTOR	0.77 / 3	0.77 / 3	0.69 / 2	0.69 / 2	0.65 / 1	0.65 / 1	0.82 / 4	0.82 / 4	0.77 / 3
PARALLELING CELL	NO / 2	NO / 2	NO / 2	NO / 2	NO / 2	NO / 2	NO / 2	YES / 1	NO / 2
TOTAL WEIGHT	<u>11</u>	<u>12</u>	<u>8</u>	<u>11</u>	<u>9</u>	<u>9</u>	<u>12</u>	<u>11</u>	<u>10</u>

*WITHIN A CATEGORY, TECHNOLOGIES ARE RANK ORDERED ACCORDING TO TOLERANCE TO PHOTOCURRENT VARIATIONS, THEREFORE, 1 REPRESENTS THE HIGHEST TOLERANCE

tolerance to photocurrent variations in that, for all three cases (10, 20 and 50 percent variation), the power loss is lower than for the opposite interconnection scheme. Extreme care should be exercised, however, in performing parallel cell connections if the technology process has a high probability of producing shorted or low resistance cells or cells prone to shorting failures. If cells are connected in parallel, shorting of cells will result in greater power loss since one cell will short out all others connected in parallel with it. Therefore, several cells up to a full bypass group should be connected in series before any paralleling is done.

Although it is difficult to make definitive comparisons between technologies and applications due to the many variables affecting photocurrent variation effects from one technology application to the next, some general trends can be seen and conclusions can be made based on careful assessment. In Table 5-4, four of the most critical characteristics affecting photocurrent variations are assessed for each application. The last characteristic listed (paralleling cells) has already been discussed. The other characteristics consist of the number of cells connected in series in a bypass group, the paralleling of bypass groups within the module, and the cell fill factor. The cell fill factor can be used as a measure of the tolerance or lack of tolerance of the cell peak power to variations in the operating point which might be produced by photocurrent variations. Both the actual value of each characteristic and the ranking of that characteristic among those of the other applications is presented in the table. The value producing the greatest tolerance to photocurrent variations is ranked number one, with other values within that characteristic group receiving higher numbers as the tolerance decreases. Therefore, the sum of the rankings for each applications results in a total weight for each application such that the lowest weight should produce the lowest power loss.

In Table 5-5, the applications are arranged by decreasing power loss for each of the 10, 20 and 50 percent photocurrent variation cases. In each column the application is listed first followed by the power loss for that application and finally the weight obtained from the previous table. In each case, the gallium arsenide residential application with the P2S6 interconnection scheme is at or near the bottom of the chart indicating very low power loss. This verifies the high significance of paralleling at the cell level for increased photocurrent variation tolerance. Therefore, the rankings for this characteristic could be additionally weighted to acknowledge this significance.

Considering the other eight application cases which all use the same interconnection technique, the weights are seen not to align in the same decreasing order as the power loss percentages. This is especially true for the 10 percent photocurrent variation case, in which other factors such as total number of cells, series and shunt resistances and total number of bypass groups connected in series might also be affecting the

Table 5-5. ARRANGEMENT OF APPLICATIONS BY DECREASING POWER LOSS

PHOTOCURRENT VARIATION	$\pm 10\%$			$\pm 20\%$			$\pm 50\%$		
APPLICATION - POWER LOSS (%) - WEIGHT	POLY-SI	CPS	- 5.5 - 12	POLY-SI	CPS	- 11.4 - 12	POLY-SI	CPS	- 32.5 - 12
	POLY-SI	RES	- 5.39 - 11	GaAs	RES (S6P2)	- 11.4 - 12	GaAs	RES (S6P2)	- 31.3 - 12
	A-SI	CPS	- 5.13 - 11	POLY-SI	RES	- 10.9 - 11	POLY-SI	RES	- 29.5 - 11
	A-SI	RES	- 4.93 - 8	A-SI	CPS	- 10.4 - 11	A-SI	CPS	- 29.2 - 11
	GaAs	RES (S6P2)	- 4.41 - 12	A-SI	RES	- 10.0 - 8	GaAs	CPS	- 25.6 - 10
	CdS	RES	- 4.33 - 9	CdS	RES	- 8.9 - 9	CdS	RES	- 25.2 - 9
	CdS	CPS	- 3.88 - 9	GaAs	CPS	- 7.8 - 10	A-SI	RES	- 25.0 - 8
	GaAs	CPS	- 3.68 - 10	CdS	CPS	- 7.6 - 9	GaAs	RES (P2S6)	- 21.4 - 11
	GaAs	RES (P2S6)	- 3.08 - 11	GaAs	RES (P2S6)	- 6.9 - 11	CdS	CPS	- 19.5 - 9

ranking. In going from the 10 percent to the 20 percent to the 50 percent case, the arrangement of applications changes such that the higher weighted applications rise to the top of the chart. Thus, it might be postulated that the higher photocurrent distributions accentuate the effects of those critical parameters used in the ranking process.

In each of the cases, the CdS CPS application produces lower losses than would be expected from its weighting of 9. This may be due to the different modeling technique required for this application than was used for all others. Since a full 21 module string could not be modeled in a single run due to the memory limits of the computer, a 7 module string was run with cell parameters and cell photocurrent distributions; then, the full module string was run based on module parameters and module photocurrent distributions. It might well be that the 7 modules used to obtain the statistical module photocurrent distributions did not represent a sufficiently large sample to produce an accurate statistical distribution especially for the large (50 percent) photocurrent variation case. Therefore, the results for this application may be optimistic, especially for the 50 percent photocurrent variation case. It might be more reasonable to expect the CdS CPS application to produce power losses more consistent with the CdS residential application.

Due to the proximity of the residential and CPS applications for polycrystalline silicon and likewise for amorphous silicon and cadmium sulfide in the 10 percent column, it would appear that the total number of cells connected in series has little effect at low photocurrent distributions compared with the degree of paralleling within the module which in the polycrystalline and amorphous silicon cases is greater for the residential applications and for which the cadmium sulfide case is the same for each application. For the 50 percent column, however, polycrystalline and amorphous silicon CPS applications produce much greater power losses than their residential counterparts. This may be due to the higher probability of producing low photocurrents with a larger statistical sample. The gallium arsenide residential and CPS applications cannot be directly compared since they represent different gallium arsenide technologies and radically different designs. Note that the numbers of cells in a bypass group for the other technologies are the same for residential and CPS applications.

5.1.2.2 Assessment of Procedures

The procedures utilized in the photocurrent variation analyses are for the most part straightforward. The nominal cell photocurrent was the same as that used for the cell photocurrent in the module modeling. The 3σ points for each case in this parametric study represent photocurrents which are 10, 20 and 50 percent, respectively, from the nominal value. PV-TAP chooses the actual cell photocurrent values from a Gaussian distribution produced by a random number generator. Individual elements

in the computer simulation represent bypass groups modeled using the PV aggregate model in PV-TAP.

When aggregation is performed beyond the bypass group level, so that more than one bypass group is represented within a single element, the effect of paralleling at the bypass group level is lost. Therefore, if the full series string of modules cannot be modeled in this detail due to computer core limitations, a two-step technique, as was used for the cadmium sulfide CPS application, is necessary to model first the detailed situation within the module, and then to model the full string based on the module results. Some inaccuracies, however, may be introduced if the number of modules used to obtain the module photocurrent distribution is not sufficiently large. This may have been the case in the cadmium sulfide CPS application analysis performed. It is recommended that the maximum number of modules which can be simulated within the memory limits of the computer be input to obtain the best statistical distribution. This may be costly and time consuming, however, because it may require making several runs increasing or decreasing the number of modules connected in series until the memory limits of the computer are fully utilized. This could not be done under the present study due to time and computer cost constraints.

5.1.3 Hot Spot Heating

Hot spot heating refers to the heating of an individual cell in a module due to shadowing of that cell. The highest temperature occurs when the shadowed cell is only partially shadowed so that heating is due not only to reverse bias but also to incident sunlight. The analysis determines whether the cell temperature will remain below the maximum specified as a constraint in the module design methodology and how much temperature margin will exist.

5.1.3.1 Assessment of Results

The analysis results are presented from a different point of view in Table 5-6 than were presented in section 4.2. The maximum cell temperature obtained for each case is compared with the maximum temperature allowable based on the module design constraints. For the module designs, the maximum reverse bias was specified as -6.7V because this was consistent with worst case cell heating to 100°C for the polycrystalline silicon technology. Although all flat plate modules were designed to operate at 50°C under normal operating conditions, the different photocurrent generation for each technology results in a different maximum cell temperature at -6.7V for each technology. A similar condition exists for the gallium arsenide CPS concentrator application except that the nominal design temperature is 100°C. The maximum allowable temperatures listed in Table 5-6, therefore, do not represent real technology

Table 5-6. ASSESSMENT OF HOT SPOT HEATING RESULTS

	POLY-SILICON		A - SILICON		CdS/CuInSe ₂		GaAs	
	RES	CPS	RES	CPS	RES	CPS	RES	CPS
MAX. TEMP. ALLOWABLE (°C)	100	100	80	80	122	122	100	$\frac{500 \times}{212}$
MAX. TEMP. OBTAINED (°C)	71	74	61	61	72	69	74	177
TEMP. MARGIN (°C)	29	26	19	19	50	53	26	35
$A_{C\text{MAX}}/A_C$ (cm ²)	96/85.1	96/91.5	25/23.1	25/22.8	51.6/44.9	51.6/42.4	103/92.6	1.27/1.27
$N_{BP\text{MAX}}/N_{BP}$	11/10	11/10	7/7	7/7	15/10	15/10	7/6	5/4
$V_{R\text{MAX}}/V_R$ (V)	-6.7/-4.7	-6.7/-4.65	-6.7/-4.3	-6.7/-4.3	-6.7/-3.0	-6.7/-3.0	-6.7/-4.4	-6.7/-3.9
f_{SH} (%) AT MAX. TEMP.	25.3	25.3	20.0	20.0	14.7	14.7	9.3	4.0
R_{SH} (Ω)	11.7	10.9	87.6	87.6	22.3	23.6	108	7.9k
I_{SC} (A) AT FULL INSOLATION	2.13	2.29	0.370	0.365	1.77	1.67	2.32	11.1
f_{SH} (%) ONSET	18.9	18.6	13.3	13.4	7.6	7.6	1.8	0.004

dependent constraints. Such data was not available for any of the technologies. The maximum allowable temperatures of 100 to 120°C are consistent, however, with maximum temperatures for single crystal silicon modules. The gallium arsenide CPS maximum temperature allowable, on the other hand, is greater than normal solder melting temperatures; therefore, a lower reverse bias constraint should be used if the array is to operate at 100°C. It can thus be implied that array operating temperatures of 100°C may require very conservative bypass group design to prevent solder failures under shadowing and/or short circuit current conditions.

The third line in Table 5-6 is the temperature margin for each application obtained by subtracting the temperature obtained from the PV-TAP run from the allowable temperature. This margin varies from 19°C to 53°C depending on the particular application. The rest of the chart is used to assess the causes for this margin.

It should be remembered that in the module conceptual design process, a conservative equation was used for the bypass diode design. In the equation, the maximum cell area (A_{CMAX}) was used and the maximum reverse voltage of -6.7V was represented by the sum of the open circuit voltages of the unshadowed cells to obtain a maximum bypass group size (N_{BPMAX}). In the final module design, the cell areas were usually less than A_{CMAX} and the bypass group size was often less than N_{BPMAX} . The actual reverse bias at the worst case shadowing is usually more representative of the peak power voltage than the open circuit voltage of the unshadowed cells as illustrated in the table by the difference between V_{RMAX} and the V_R obtained. In addition, the maximum temperature in the design calculation was conservatively considered to occur at full illumination. In the PV-TAP results, however, it can be seen that the degree of shadowing which produced the maximum temperature varied with application from 4 percent to approximately 25 percent. The percent shadowing obtained from the PV-TAP analyses is consistent with the onset shadowing percentage which could be calculated from the simple equation shown below.

$$f_{SH}(ONSET) = \frac{(V_R/R_{SH})}{I_{SCC}} \quad \text{Eq.(5-1)}$$

The onset percentage is obtained when the current through the shunt resistance of the shadowed cell produces a reverse bias of V_R . The onset shadow percentage is then representative of a minimum decrease in illumination required from the full illumination short circuit current (I_{SCC}). The actual percent shadow at maximum cell temperature is, in all cases, a few percent higher than the onset percentage.

5.1.3.2 Assessment of Procedures

The equation used for the bypass group design in the module design process is very conservative as explained in the previous section. Some of this conservatism can be eliminated if the peak power voltage of the unshadowed cells is used in place of the open circuit voltage in the equation. The onset shadow percentage could also be used in the bypass design equation with V_R represented by the combined peak power voltages of the unshadowed cells. These modifications would reduce the margin between the maximum allowable temperature and the temperature obtained from the PV-TAP calculations. These modifications should be made with care, however, because much of the margin seen in the table is due to reducing the cell area and the bypass group size below the maximum specified in the design. If these reductions are not present, the design margin could be lost entirely, especially since the PV-TAP analyses represent a worst case operating condition of module short circuit as opposed to the design calculations which were performed at module peak power. The designer and/or analyst must be careful to ensure that some temperature margin does exist. It can be seen also that if the shunt resistance (R_{SH}) is large as in the gallium arsenide CPS application, the maximum temperature occurs with very little shadowing (4.0 percent in this case) so that the cell is almost fully illuminated.

Both the design and the PV-TAP analyses were performed with ambient temperature of 20°C. In flat plate applications, however, the cell temperature is approximately linear with ambient temperature. Since the ambient temperature could be as high as 40°C in many locations, the 19°C margin as seen in the amorphous silicon applications could be reduced to zero. Therefore, the analyst should perform the PV-TAP analyses and perhaps even the bypass group design, at the maximum ambient temperature which could be expected at the location of the system application. Performing the bypass group design at high ambient temperature would result in small bypass group size.

5.1.4 Annual Energy Distribution Using SOLCEL II

The SOLCEL II computer code was used to perform calculations of the annual dc energy produced and the ac energy distribution for each application. The SOLCEL II code does not contain the capability to sell energy to public utility; therefore, for the residential applications the energy produced in excess of the residential load requirements, was listed as wasted energy. In an actual utility interactive system, this wasted energy would, in fact, be sold to the utility. For the CPS applications, all the energy produced is supplied to the electric utility grid. The results of the SOLCEL II analyses were also used as inputs to the economic analyses which will be discussed in section 5.1.5. The total ac power produced in each SOLCEL II analysis was also factored by the PV-TAP outputs from the photocurrent variation analyses to assess the

actual annual energy which might be produced in a real array with photocurrent variations.

5.1.4.1 Assessment of Results

The results of the SOLCEL II analyses for both residential and CPS applications are summarized in Table 5-7. For the residential analyses, the energy listed by SOLCEL II as wasted energy has been specified in this table as energy sold to utility. The total ac energy produced for the residential applications is the sum of the ac energy supplied to the load and the energy sold to utility. The total ac energy produced has been reduced by the typical power losses obtained from the PV-TAP analyses for 10, 20 and 50 percent variation in cell photocurrent.

Since all the energy produced in the CPS application is supplied to the electric utility grid, the load demand and energy sold to utility categories do not apply to the CPS applications. For the gallium arsenide CPS application system parasitics have been included because the concentrating array is considered to be tracking and actively cooled. The gallium arsenide systems for both residential and CPS applications display much lower available insolation and insolation received than the other technologies because the gallium arsenide technologies contain 20 percent efficient cells compared with efficiencies of 10 to 11.5 percent for the other technologies.

The reader is cautioned against comparing technologies based on these SOLCEL II results because many of the parameters used to obtain the system designs were estimated or projected to meet technology goals. Comparison of the CPS applications is further confounded by the fact that a different SOLCEL II methodology was used for the gallium arsenide concentrator application than for the other CPS applications. The difference in procedure is fully discussed in the next section. In addition, the temperature dependence of the gallium arsenide cell parameters was based on speculative efficiency versus temperature data which may be overly conservative; therefore, the annual energy production may be different than that calculated if the temperature dependence of the efficiency should prove to be lower. These examples, however, provide a demonstration of the SOLCEL II methodology and have exposed the need for revisions to the SOLCEL II code (discussed below) for better application to advanced PV technologies.

5.1.4.2 Assessment of Procedures

As indicated in Table 5-8, all flat plate applications use the SOLCEL II methodology in which short circuit currents and open circuit voltages are input at high and low insolation and temperature. This data along with the series resistance input produces a detailed PV cell model within

Table 5-7. SOLCEL II RESULTS SUMMARY

ANNUAL ENERGY DISTRIBUTION kWh	RESIDENTIAL 4 kW ARRAY			
	POLY-Si	a-Si	CdS/CuInSe ₂	GaAs
TOTAL AVAILABLE INSOLATION	135,384	155,985	157,668	75,525
TOTAL INSOLATION RECEIVED	103,705	119,486	120,775	57,853
PRODUCED DC ENERGY	10,775	10,968	10,938	9,681
AC ENERGY SUPPLIED TO LOAD	2,494	2,489	2,581	2,414
UTILITY ENERGY TO THE LOAD	4,121	4,126	4,034	4,201
LOAD DEMAND	6,616	6,616	6,616	6,616
ENERGY SOLD TO UTILITY	5,338	5,481	5,412	4,584
TOTAL AC ENERGY PRODUCED	7,832	7,970	7,993	6,998
10 PERCENT VARIATION IN PHOTOCURRENT	7,410	7,577	7,647	6,782
20 PERCENT VARIATION IN PHOTOCURRENT	6,978	7,173	7,286	6,519
50 PERCENT VARIATION IN PHOTOCURRENT	5,522	5,978	5,979	5,500

ANNUAL ENERGY DISTRIBUTION MWh	CPS 2.2 MW ARRAY			
	POLY-Si	a-Si	CdS/CuInSe ₂	GaAs
TOTAL AVAILABLE INSOLATION	65,345	79,887	70,319	40,844
TOTAL INSOLATION RECEIVED	50,055	61,194	53,865	40,844
PRODUCED DC ENERGY	5,261	5,532	4,946	6,686
AC ENERGY SUPPLIED TO LOAD	4,494	4,730	4,211	5,775
SYSTEM PARISITICS				33
TOTAL AC ENERGY PRODUCED	4,494	4,730	4,211	5,775
10 PERCENT VARIATION IN PHOTOCURRENT	4,244	4,487	4,048	5,562
20 PERCENT VARIATION IN PHOTOCURRENT	3,982	4,238	3,889	5,322
50 PERCENT VARIATION IN PHOTOCURRENT	3,033	3,349	3,390	4,297

Table 5-8. SOLCEL II INPUTS SUMMARY

SOLCEL	DEFINITION	POLY-Si		a - Si		CdS/CuInSe ₂		GaAs	
		RES	CPS	RES	CPS	RES	CPS	RES	CPS
3	LOW INSO	100	100	100	100	100	100	100	
4	HIGH INSO	1000	1000	1000	1000	1000	1000	1000	
5	LOW TEMP	15	15	15	15	15	15	15	
6	HIGH TEMP	75	75	75	75	75	75	75	
7	I _L LT	24.86	24.89	15.92	15.93	38.99	39.09	24.85	
8	I _H LT	248.6	248.9	159.20	159.3	389.9	390.9	248.5	
9	I _L HT	25.79	25.81	16.51	16.51	40.42	40.51	25.75	
10	I _H HT	257.9	258.10	165.10	165.1	404.2	405.1	257.54	
11	V _L LT	.540	.54	.71	.71	.401	.401	.931	
12	V _H LT	.621	.621	.923	.923	.449	.449	1.00	
13	V _L HT	.408	.408	.614	.614	.269	.269	.739	
14	V _H HT	.494	.494	.842	.842	.323	.323	.815	
15	SERIES RESISTOR	4E-5	4E-5	5.3E-6	5.3E-6	2.05E-4	2.05E-4	1.6E-4	
PVTT		6E3	2.2E6	6E3	2.2E6	6E3	2.2E6	6E3	2.2E6
CL		1.207	1.207	1.207	1.207	1.207	1.207	1.207	2.367
CW		36.21	17477.36	41.72	21366.6	42.17	18807.47	20.2	6602.8
PACFAC		.933	.943	.90	.886	.921	.932	.913	.726
CONRA		1	1	1	1	1	1	1	500
ARLENS									.08065
ARSINK									1.267E-4
CTP									.1
TFI									300
TFO									400
ICTYPE		2	2	2	2	2	2	2	8
IECON		1	4	1	4	1	4	1	4
EFFC		.115	.115	.10	.10	.108	.108	.20	.4452
IPVEFM		1	1	1	1	1	1	1	4
COEF									.0066

SOLCEL II. SOLCEL II produces a matrix of output power versus insolation and temperature. This formulation also requires device dependent parameters (A_0 and E_{G0}) be input by the user. These parameters vary with cell technology and cannot be calculated from current-voltage relationships. Therefore, default values in the code were used for all applications. The default parameters apply specifically to single crystal silicon technology; therefore, application of these parameters to other technologies produces questionable results. Since current-voltage data is input at extremes of illumination and temperature, the loss in accuracy should not be significant. If more accurate results are to be obtained for advanced PV technologies, however, either these parameters must be obtained for various PV technologies or the SOLCEL II code must be modified to permit use of parameters which can be obtained from current-voltage data in place of these parameters. A similar PV cell model is used in PV-TAP in which similar parameters are obtained from actual current-voltage data as a function of temperature.

The same technique was attempted for the gallium arsenide CPS concentrator application. Large deviations were obtained, however, in the SOLCEL II calculation of internal parameters as a result of the use of these default parameters. The resultant parameters produced inconsistent results in that the average module efficiency was much lower than should have been obtained from the 20 percent cell efficiency. A different SOLCEL II methodology was therefore used for the calculation of annual energy distribution for the gallium arsenide CPS concentrator application.

The efficiency versus temperature methodology described in the SOLCEL II documentation was used. This is a simple method which does not use a detailed PV cell model, but instead factors the efficiency based on efficiency versus temperature data. The efficiency must be specified to SOLCEL II at 28°C. Since the gallium arsenide concentrator operates at 100°C with 20 percent efficiency, the efficiency specified at 28°C becomes 44.5 percent. As previously discussed, the efficiency versus temperature specification for the gallium arsenide CPS cells is highly speculative and may be overly conservative. On the other hand, the methodology uses a linear approximation for the power variation with insolation based on the full illumination efficiency input. For a detailed PV cell model, however, the reduction in output with reduced illumination is not linear, but rather superlinear so that, if the insolation is reduced by 50 percent, the output power should be reduced by more than 50 percent.

Based on these considerations, it can readily be seen that if comparisons are to be made between technologies, the same SOLCEL II methodology should be used for all calculations. The detailed PV cell model formulation may not be necessary for performing comparisons. As long as the formulation is the same for each technology, comparisons can be valid. However, if detailed energy distribution information is to be obtained

from realistic cell and system parameter inputs, the more accurate SOLCEL II methodology should be used. As previously discussed, however, modifications may be required to the SOLCEL II code in order to use this formulation for advanced PV technology.

The parameter, E_{GO} , is used in an exponential. It represents the band gap constant of the material. The user could ignore the physical definition of this parameter and determine the parameter from current-voltage versus temperature data. The term, A_0 , is related to the saturation current and is multiplied by a device constant calculated by SOLCEL II in order to obtain the saturation current. This method of formulation makes it difficult for the user to obtain A_0 and E_{GO} from current-voltage versus temperature data. If A_0 and the device constant (K_{DEV}) calculated by SOLCEL II are combined into one parameter which is calculated by the user, these parameters will be similar to those used in PV-TAP and can be specified fully by the user.

The total AC energy produced was factored by the typical power losses obtained from the PV-TAP analyses for 10, 20, and 50 percent variation in cell photocurrent. The energy distributed to the load and that sold to utility could not be factored, however, because the photocurrent losses occur on the DC side of the inverter and will affect the energy distribution. The ideal method of factoring in the photocurrent losses would be to input them as reduced current and voltage inputs to SOLCEL II. This would, however, involve a separate SOLCEL II run for each photocurrent variation condition instead of the single run used here.

5.1.5 Economic Analysis

5.1.5.1 Assessment of Results

The economic analysis determines the Life Cycle Cost (LCC) for residential systems and the Required Revenue for CPS systems. Since costs are classified as area proportional ($\$/m^2$) and output proportional ($\$/Wp$) and since the cost coefficients are the same within a given application (residential or CPS), the implication is that PV module efficiency is the determining factor of relative cost effectiveness. The equality of coefficients even applies to the actual PV module costs since projected costs are used ($\$3.87/Wp$ in 1986 and $\$0.96/Wp$ in 1989). Thus, it can be seen in Tables 5-9a and 5-9b that the GaAs systems have the lowest LCC and Production Cost because they have the highest output density (Wp/m^2).

Although these examples are useful for demonstrating the methodology used and studying the effects of system input parameters on LCC and Production Cost, the results should not be used to compare technologies at this time since the technology designs are highly speculative and cost projections were used for module price. It is assumed, for example, that GaAs at 20

**Table 5-9a. ECONOMIC RESULTS SUMMARY: RESIDENTIAL
SYSTEMS PARAMETERS AND COSTS**

PARAMETER	PV TECHNOLOGY			
	p - Si	a - Si	CdS/CuInSe ₂	Ga/As
ARRAY SIZE (M ²)	43.7	50.4	50.8	24.4
PEAK OUTPUT (kWp AC)	4.1	4.0	4.4	3.9
ANNUAL OUTPUT (kWH AC)	7832	7970	7993	6999
ANNUAL RESIDENTIAL LOAD (kWH AC)	6615	6615	6615	6615
ANNUAL OUTPUT TO LOAD (kWH AC)	2494	2489	2581	2415
BACK UP ENERGY (kWH AC)	4121	4126	4034	4200
OUTPUT PROPORTIONAL COST (\$)	3690	3582	3978	3510
AREA PROPORTIONAL COST (\$)	3494	4033	4068	1949
PV ARRAY COST (\$)	15867	15403	17105	15093
SYSTEM PRESENT VALUE (\$)	27107	26980	29234	24991
ANNUAL LIFE CYCLE COST (\$)	3184	3169	3434	2935

**Table 5-9b. ECONOMIC RESULTS SUMMARY: CPS SYSTEMS
PARAMETERS AND COSTS**

PARAMETER	PV TECHNOLOGY			
	p-Si	a-Si	CdS/CuInSe ₂	GaAs
ARRAY SIZE (M ²)	21,095	25,789	22,701	15,629
PEAK OUTPUT (kWp AC)	1,954	1,954	1,946	2,270
ANNUAL OUTPUT (kWH x 1000 AC)	4,494	4,730	4,211	5,775
OUTPUT PROPORTIONAL COST (\$)	781,600	781,600	778,400	908,000
AREA PROPORTIONAL COST (\$)	1,413,400	1,727,900	1,521,000	1,047,100
PV ARRAY COST (\$)	1,875,800	1,875,800	1,868,200	2,179,200
ANNUAL REQUIRED REVENUE (\$/Y)	516,400	556,300	528,600	524,400
PRODUCTION COST (\$/kWH)	0.115	0.118	0.126	0.091

percent efficiency will cost the same as amorphous silicon at 10 percent efficiency. On the other hand, it cannot be determined at this time whether GaAs cells can be made which are sufficiently thin and/or have high enough efficiency to offset the high cost of the gallium arsenide material. Neither can it be determined at this time if amorphous silicon will ever achieve efficiencies of 10 percent over a practical cell size or if 10 percent efficiency is really required. In addition, since SOLCEL II outputs are used as inputs to the economic analyses, the different SOLCEL II methodology required for the GaAs application from that used for the other applications, as discussed in section 5.1.4, further confounds accurate comparison of economic results.

5.1.5.2 Assessment of Procedures

The procedures used in the economic analysis are partially discussed in Section 4.2 and are discussed in detail in other references presented [2,3,46,47]. The technique is straightforward but the results are dependent on the validity of the input parameters which are often estimates or projections. The results are also highly dependent on the results of the SOLCEL II analyses which are used as inputs to the economic analyses. Therefore, care must be taken in formulating the SOLCEL II analyses and the effects of parameter changes must be understood.

In the case of the GaAs application, a different SOLCEL II analysis methodology was used than for the other technologies, as discussed in section 5.1.4. Since the SOLCEL II methodology was different, the economic analysis also contains the added variable and technology comparisons are even more ill-advised. If technology comparisons are to be made in the future based on more accurate cost and efficiency data, the same SOLCEL II methodology should be used for each technology to eliminate this variable.

5.2 TECHNOLOGY ASSESSMENTS AND GUIDELINES

In this section, assessments of the various technologies are performed based on conceptual design and analysis experience gained during the study. General guidelines which apply to all technologies are also formulated and applied to specific technologies where appropriate. Discussions are included on desirable and undesirable cell characteristics, necessary technology data which are not available, and characteristics which require improvement for each technology.

5.2.1 Guidelines for all Technologies

5.2.1.1 Cell Fill Factor Considerations

The quality of the cell parameters for a particular technology as represented by the cell current-voltage (I-V) curve is very important in the quest for a practical, efficient and reliable module. Not only should the cell efficiency be high (>10 percent for most technologies; >20 percent for GaAs), but the fill factor must have certain desirable characteristics. A high fill factor not only improves the cell efficiency but also improves the interface of the PV array with the DC-AC inverter voltage window. The fill factor can be viewed as being comprised of two terms, the ratio of peak power voltage to open circuit voltage (V_{MPC}/V_{OCC}) and the ratio of peak power current to short circuit current (I_{MPC}/I_{SCC}). If the voltage ratio is low, an array whose peak power voltage variation with temperature is matched to the inverter voltage window may force the inverter to occasionally turn off or prevent it from turning on due to over-voltage associated with the high open circuit voltage.

A low voltage ratio in the fill factor may also prevent the attainment of a desirable peak power voltage in a module design due to personnel safety hazard. A module, for example, could not be designed for 20 V at peak power because the open circuit voltage at low temperature could exceed a maximum safe voltage such as 30 V specified by JPL [29] for residential modules.

On the other hand, a high current ratio in the fill factor is less desirable. Although it improves cell efficiency, it causes higher power dissipation and heating under shadowing conditions. The cell will attain near maximum reverse bias while still almost fully illuminated. Therefore, more bypass protection is required.

It should also be noted that although a high fill factor improves individual cell efficiency, it does not necessarily improve module efficiency. A high fill factor reduces the tolerance of the cell power to variations in the operating point such as will occur due to cell-to-cell variations in photocurrent generation. Since the current at peak power will be different for each cell, the cells connected in series will operate at different voltages. If the fill factor is high, the power curve will have a sharp peak so that the power decreases significantly for short excursions from the peak power point. Thus, a valid argument can be made for limiting the fill factor by limiting the shunt resistance of the cell. This may also reduce the cost of cell processing by relaxing some processing constraints.

5.2.1.2 Current to Voltage Ratio

It should also be noted that a high efficiency due to a high maximum power current is less desirable than a high efficiency produced by a high maximum power voltage. The high voltage requires fewer cells in series to attain desirable module voltages and therefore, permits more paral-

leling of cells or bypass groups for increased tolerance to photocurrent variations. Paralleling of cells or bypass groups with high ratios of maximum power current to voltage, by comparison, produces modules which require higher metallization widths and thicknesses especially for large area modules which could have long conductor runs.

A high current to voltage ratio also adversely affects the modularity which is desirable in residential systems. Residential inverters are produced in 2 KW steps. Although this modularity could be changed in future inverters, residential systems will not exceed 10 KW and may be most economical between 4 and 8 KW. For an 8 KW inverter, however, the PV array should be sized at about 7 KW to prevent shutdown of the inverter due to excessive input power under high insolation, low temperature conditions as might be experienced for tilted arrays in late winter. These conditions could produce power increases of up to 25 percent so that the array power would be about 8.75 KW. An 8 KW inverter would be expected to shut down at about 10 percent above rated power or 8.8 KW for an 8 KW inverter.

The PV array, however, is usually composed of strings of series-connected modules which are in turn connected in parallel. The modules are connected in series to interface with the inverter voltage window. Thus, the string can be viewed as a basic array building block. If the current to voltage ratio of the cell is large, then the power to voltage ratio of a large area module will also be large assuming the module open circuit voltage is limited to less than 30 V. It may then be difficult to obtain both the array power and voltage desired for interface with the inverter. A string power of 850-880 W is most desirable for modularity because this would produce ideal array powers for interfacing with inverters sized in 1KW steps, but is possible only for higher voltage modules (15-20 V) of relatively small size (<2.5 ft. x 4 ft.) which then would not contain the desired degree of paralleling. An alternate modularity power range would be 1700-1760 W.

The ideal modules for residential applications would then have peak power currents of 4.4A so that a 200 V series string of modules would produce 880 W or 8.8A for a 1760 W string. Since it is also desirable to parallel 3 or 4 cells in a module, the cell current should be about 1.1-1.5A for the small modules and 2.2-2.9A for the large modules. If the 30V limit can be exceeded, however, a 50V, 4.4A 4 ft. x 6 ft. module would be ideal.

5.2.1.3 Voltage-Temperature Characteristics

The rate of change of cell voltage with temperature is also a critical characteristic for interface of series strings of modules with inverters. The variation in string voltage over the expected range of temperatures

for the location of the array must be within the voltage window of the inverter which has acceptable limits of about ± 20 percent from the nominal voltage. This design interface is already difficult for single crystal silicon modules which have an open circuit voltage variation $(\Delta V/\Delta T)$ of about $-2.2 \text{ mV}/^\circ\text{C}$. If this variation is expressed as a fractional quantity $((\Delta V/\Delta T)/V_{\text{OCC}})$, the criteria can be applied to other technologies. Thus, the advanced PV technology should have a fractional variation

$$(\Delta f_V/\Delta T)_{\text{Adv.}} \leq \left[(\Delta V/\Delta T)/V_{\text{OCC}} \right] \text{ si} \quad \text{Eq. (5-2)}$$

$$\leq \frac{-2.2 \text{ mV}/^\circ\text{C}}{600 \text{ mV}}$$

$$\leq 0.0037/^\circ\text{C}$$

This will produce string voltage variations for most practical temperature limits in real applications of about ± 20 percent from the nominal voltage.

5.2.1.4 Reverse Breakdown and Maximum Temperature

The reverse breakdown voltage of the cell and the maximum allowable temperature of a cell in a module are critical parameters in module design. They are used as constraints in the determination of the maximum number of cells permitted in a bypass group. The higher the values of these parameters, the greater the number of cells permitted in a bypass group and conversely the fewer bypass diodes required. If, in fact, only one bypass diode is required for a module, it can be placed across the terminals rather than requiring integration into the module. This is usually only possible for low voltage modules ($\leq 10 \text{ V}$).

At present, the reverse bias and temperature stress susceptibilities of advanced PV technology cells have not been quantified. Thus, the breakdown voltages, the maximum allowable temperatures and the failure mechanisms and characteristics (short, open, resistance change, etc.) must be determined first from tests on cells and eventually from tests on modules for any advanced technology as it approaches technical readiness.

Since reverse breakdown can occur over small areas of the junction, all reverse power dissipation could be confined to this same small area. The power dissipation is proportional to the cell current through its area dependence. Therefore, large area cells could have higher susceptibility than smaller area cells. From this consideration, it is obvious that tests must be made for the maximum cell area which might be used in a module design and that only testing will provide realistic data on reverse bias susceptibility.

5.2.1.5 Limiting Cell Area

As discussed in the previous section, larger area cells are generally more susceptible to reverse bias failure. It may, therefore, be advisable to place limits on the maximum desirable cell area for a particular technology based on reverse bias tests. This may not be practical for most advanced technologies at this time due to the relative infancy of many of the technologies; however, it may be appropriate for any technology once it is capable of producing high efficiency over a large area ($\geq 25 \text{ cm}^2$).

Additional reasons for limiting cell area are:

- . To prevent excessive metallization or conductor requirements due to high current to voltage ratio as discussed in section 5.2.1.2.
- . To prevent excessive power to voltage ratio which results in reduced modularity and more difficult inverter power interface as also discussed in Section 5.2.1.2.
- . To reduce effects of nonuniformities in cell which can reduce efficiency and reliability and increase the impact of cell failures (especially shorting).

Many of these considerations apply not only to cell area but also to high cell aspect-ratio (long length and short width) since this implies controlling the cell process over a long dimension and may also require long metallization runs.

5.2.1.6 System Applications

Since the residential and intermediate application sectors are better defined than the CPS sector and have produced operational experience, initial module development should be tailored toward these applications, while CPS module development by manufacturers should await better CPS systems definitions.

In general, however, modules for CPS applications could be larger ($\geq 4 \text{ ft.} \times 8 \text{ ft.}$) than modules for residential application ($2 \text{ ft.} \times 4 \text{ ft.}$, $4 \text{ ft.} \times 4 \text{ ft.}$, $2.5 \text{ ft.} \times 8 \text{ ft.}$, etc.) because they will be ground-mounted rather than roof-mounted and because more careful handling and maintenance will be available. This latter argument can also be used along with strict access control and personnel training to justify high voltage modules for CPS applications ($\geq 100 \text{ V}$). In fact, the higher voltage will be required if the module area is increased in order to prevent excessive conductor run requirements in the modules. It should be noted, however, that module series string modularity is not a consideration in CPS array designs since the array power will be so high that hundreds of strings will be required.

5.2.2 Guidelines for Specific Technologies

The cautions and concerns expressed in this section do not imply that a technology is not feasible but that careful consideration be given to these design issues.

5.2.2.1 Polycrystalline Silicon

The polycrystalline silicon technology process used in the conceptual designs and analyses in this study was the ribbon-to-ribbon (RTR) recrystallization process developed by Motorola [4]. The I-V characteristics are similar to single crystal silicon, and modules built from these cells should have similar electrical characteristics as single crystal silicon modules. Since the cells are made from ribbons, however, they will not be circular but square or rectangular. Therefore, the considerations on aspect ratio (Section 5.2.1.5) will apply to these cells. The cell area could also be very large ($> 100 \text{ cm}^2$); therefore, area dependent considerations apply as in Sections 5.2.1.2, 5.2.1.4, and 5.2.1.5.

Redundant, across-the-cell interconnects can be used with this technology to reduce the output power loss in the event of a cracked cell or a broken interconnection.

5.2.2.2 Amorphous Silicon

The amorphous silicon conceptual designs and analyses in this study are based on a deposition process used by RCA which produces integrated, series-connected cells on a glass superstrate [5]. The cells are limited in the series direction by the resistivity of the transparent, conducting oxide (TCO) to less than 1.0 in. wide; therefore, the caution on aspect ratio (Section 5.2.1.5) applies to this technology. The high probability of pinholes in amorphous silicon further supports the case against long lengths as well as large areas. In addition, paralleling at the cell level is not recommended for high occurrence of shorting or low resistance cells.

The amorphous silicon technology, in general, is so thin that metallization and conductor run requirements for large area modules may result in compatibility problems with the process. In addition, interconnection metallizations between cells, especially where paralleling occurs, must be sufficiently large to handle large excess current; for example, when shadowing causes cell groups to be bypassed, the metallization between cell groups may be required to carry the full current along its length rather than being distributed across its width. This is especially true for low voltage (5-10 V) modules with significant paralleling which increases the total module current. The designs performed also assumed that the module size was limited to a maximum of 1 ft. x 4 ft. by the deposition process. If larger area modules can be made, the metallization, conductor and bypass diode design integrations become even more critical.

It should be noted that the fractional voltage versus temperature coefficient postulated for this technology is low:

$$\Delta f_V / \Delta T = \frac{1.6 \text{ mV}/^{\circ}\text{C}}{910 \text{ mV}} = 0.0018/^{\circ}\text{C} \quad \text{Eq. (5-3)}$$

which will facilitate the interface with the inverter voltage window.

5.2.2.3 CdS/CuInSe₂

The cadmium sulfide process envisioned for this design and analysis study produces ribbons of CdS/CuInSe₂ cells on a flexible substrate [6, 7]. The I-V curves for CdS/CuInSe₂ cells produced by Boeing indicate a low voltage ratio in the fill factor, a problem discussed in Section 5.2.1.1. Therefore, compatibility with inverter voltage windows may be difficult and development of residential modules with peak power voltage > 15 V may not be feasible. The voltage ratio can be increased by improving the series resistance of the cell. The fractional voltage versus temperature coefficient postulated

$$\Delta f_V / \Delta T = \frac{2 \text{ mV}/^{\circ}\text{C}}{420 \text{ mV}} = 0.0048/^{\circ}\text{C} \quad \text{Eq. (5-4)}$$

is larger than 0.0037/^oC criteria presented in Section 5.2.1.3, which also implies an interface compatibility problem with the inverter voltage window. This can be improved slightly if the voltage of the cell can be increased, but the interface with the inverter voltage window will still be a difficult design problem.

The photocurrent generation for this technology is the highest reported for any PV cell technology. If this high current cannot be balanced by high voltage generation, the high current to voltage ratio will produce problems such as discussed in Section 5.2.1.2. In the residential conceptual design performed, the size of the module had to be reduced to provide the modularity necessary to obtain the desired array power.

The low peak power voltage of the cell (0.3 V) requires that many cells be connected in series to obtain desirable module voltages. The high photocurrent implies that cell area should be limited to prevent excessive current to voltage ratio. The combination of small cell area and many series connections results in a tradeoff between low packing factor for many small cells or low photocurrent variation tolerance due to low paralleling for larger cells. The photocurrent variation tolerance can be improved by reducing the bypass group size below the maximum allowable, but this will result in increased bypass diode costs.

Redundant, across-the-cell interconnects can be used with this technology to reduce the output loss in the event of a cracked cell or a broken interconnection.

5.2.2.4 GaAs Flat Plate Cells

The GaAs residential design and analysis is based on the CLEFT process developed at MIT which grows homojunction cells on reusable substrates [8]. The module size was limited to 2 ft. x 4 ft. in accordance with the postulated module size in the reference. If a larger size module is possible, it would permit more paralleling to increase photocurrent variation tolerance but would decrease the modularity of the module series string. This was already a problem in the conceptual design in which the size of the module had to be decreased to obtain the desired array power. On the other hand, the photocurrent variation tolerance was already the best of the various conceptual designs due to paralleling of individual cells rather than at the bypass group level. Therefore, the present module size is ideal unless the voltage can be increased to about 50V. In that case, a 4 ft. x 4 ft. module would be better.

Because of the higher cell efficiency (20 percent) with the same photocurrent generation (25 mA/cm²) as for polycrystalline silicon, the power to voltage ratio is actually lower than for polycrystalline silicon. The polycrystalline silicon module string, however, had just the right power to produce the desired array power. Therefore, another option for the GaAs module might have been to increase the module size if this is consistent with process capabilities. Since the current to voltage ratio for GaAs cells is lower than for the same area polycrystalline silicon cells, the metallization and module conductor requirements should not be a problem.

The fractional voltage variation with temperature:

$$\Delta f_V / \Delta T = \frac{3.2 \text{ mV}/^\circ\text{C}}{970 \text{ mV}} = 0.0033/^\circ\text{C} \quad \text{Eq. (5-5)}$$

is better than the criteria (0.0037/°C) established in Section 5.2.1.3. In addition, redundant, across-the-cells interconnects can also be used with this technology. The cell postulated in the design had two such interconnects, but three or four might be better.

5.2.2.5 GaAs Concentrator Cells

The GaAs CPS design and analysis in this study used 0.5 in diameter, multi-junction, cascaded cells similar to those reported by RTI [9,10] in a 500X point-focus Fresnel lens design. A detailed focusing accuracy and profile analysis were not performed; rather, the concentration was assumed to be supplied by the circular portion of a square Fresnel lens. Thus, the packing factor was reduced by the ratio of the circular to square area. Other designs with improvement in packing factor could obviously be postulated.

The cell efficiency loss with temperature was postulated to be a worst case value. From a cell efficiency of 30 percent at 50°C, the efficiency drops to 20 percent at 100°C. This results in a voltage variation with temperature of 14mV/°C or a fractional variation of:

$$\Delta f_V / \Delta T = \frac{14 \text{ mV/}^\circ\text{C}}{2200 \text{ mV}} = 0.0064/^\circ\text{C}. \quad \text{Eq. (5-6)}$$

This is extremely high compared with the criteria established in Section 5.2.1.3 and causes severe problems with the inverter voltage window interface. The value is, as already noted however, very conservative and should probably be much lower.

The array was postulated as operating at 100°C cell temperature. The efficiency would be improved greatly by operating at a lower temperature. In addition, the hot spot cell heating due to reverse bias caused by shadowing or dust accumulation could result in cell temperatures near the melting point of solder if the array is operated at 100°C.

Because of the high concentration, the cell current is very high (11.1 A at short circuit). This should not produce any problems with conductor runs, however, since the cells are spaced far apart and only the lenses are tightly packed, nor would there be problems with bypass diode design integration.

5.3 DESIGN AND ANALYSIS GUIDELINES

Previous sections 5.1 and 5.2 presented assessments of the analysis results and procedures and technology assessments and recommendations. Detailed design and analysis procedures were presented in previous sections 3.0 and 4.0 of this report. This section compiles the recommendations for improvements to these design and analysis procedures and the cautions for the proper implementation of the procedures which are contained throughout sections 5.1 and 5.2.

5.3.1 Design Guidelines

The conceptual design procedures presented in section 3.0 can serve as effective guidelines for module and array design. Some additional recommendations and guidelines are provided here. Module and array designs performed using postulated data are at best hypothetical. Before any concrete designs can be produced, real measured data must be available. In the conceptual designs performed, for example, breakdown voltages, maximum allowable temperature and voltage-temperature coefficients were not known. The list of parameters contained in Table 5-10 is the minimum set required to perform module design. Additional constraints must also be supplied. These include such conditions as maximum cell area, cell-to-cell spacings required, module dimensions and voltage desired, among others. These constraints were discussed briefly in

Table 5-10. REQUIRED CELL AND CONDUCTOR PARAMETERS

- J_{SCC} , V_{OCC} , J_{MPC} , V_{MPC} , FFC
 - From J-V curve at standard insolation and single temperature
- $\Delta V/\Delta T$ (Open Circuit Voltage Temperature Coefficient)
 - From V-T curve
 - From J-V curves at 2 temperatures
- Reverse Bias Stress Parameters
 - V_B (Breakdown Voltage)
 - From reverse I-V curve
 - $\Delta T/\Delta S$ (Temperature Coefficient for Insolation Power) and
 - $\Delta T/\Delta P$ (Temperature Coefficient for Power Dissipation)
 - From thermal analysis of laminations
 - From typical module data
- N_{ACI} (Number of Across-the-Cell or Redundant Interconnects)
 - If applicable-from cell technology
- Resistance Limited Technologies
 - R (Sheet Resistivity of Worst Current Carrier in Cell)
 - P_{FL} (Fractional Power Loss Allowable in Current Carrier)
 - From manufacturer
- Module Metalization and conductor Requirements
 - ρ (Resistivity of Current Carriers in Module)
 - P_F (Fractional Power Loss Allowable in Module Conductors)
 - From handbook or manufacturer

section 3.0 and are covered in detail in the module optimization methodology report [3].

The designs performed must consider realistic applications and must be responsive to the requirements of these applications; for example, for residential applications, spacing of roof supports and limitation on voltages for personnel safety must be considered. In addition, the array voltage over a realistic range of temperatures must be compatible with the voltage window of the inverter used to interface with the utility and the load or of the regulator used for DC applications.

The only improvement recommended for the design procedures concerns determination of the maximum number of cells which can be connected in series in a bypass group (N_{BPMAX}). The equation

$$N_{BPMAX} = 1 - \frac{V_{RMAX} + V_{FD}}{V_{OCC}}, \quad \text{Eq. (5-7)}$$

in which V_{FD} is the forward voltage drop of the bypass diode, applies well when V_{RMAX} is used to represent the breakdown voltage of the cell, but is overly conservative when V_{RMAX} represents the voltage at which the maximum cell temperature in reverse bias is attained. For this condition, V_{OCC} should be replaced by V_{MPC} :

$$N_{BPMAX} = 1 - \frac{V_{RMAX} + V_{FD}}{V_{MPC}} \quad \text{Eq. (5-8)}$$

In addition, the equation used to obtain V_{RMAX} from the temperature constraint can be modified. The present equation is

$$V_{RTMAX} = \frac{(\Delta T / \Delta S) A_{CMAX} S_0 - (T_{CMAX} - T_A)}{(\Delta T / \Delta P) I_{MPC}} \quad \text{Eq. (5-9)}$$

In this equation, $\Delta T / \Delta S$ and $\Delta T / \Delta P$ are temperature coefficients, T_{CMAX} is the maximum allowable temperature of a cell, A_{CMAX} is its maximum area, and T_A is the ambient temperature. This equation is conservative since the cell area is usually less than A_{CMAX} and the cell is partially shadowed when its maximum temperature is reached. Thus, the illumination on the cell is less than S_0 , which is the full insolation of the cell. If the maximum shunt resistance of the cell is known, S_0 can be replaced by

$$S = \left[1 - \frac{(V_{RTMAX}/R_{SH})}{I_{SCC}} \right] S_0, \quad \text{Eq.(5-10)}$$

in which R_{SH} is the cell shunt resistance, and the resulting equation solved for V_{RTMAX} .

$$V_{RTMAX} = \frac{(\Delta T / \Delta S) A_{CMAX} S_0 - (T_{CMAX} - T_A)}{(\Delta T / \Delta P) I_{MPC} + \frac{(\Delta T / \Delta S) A_{CMAX} S_0}{R_{SH} I_{SCC}}} \quad \text{Eq.(5-11)}$$

Since most of the conservatism has been removed from the equation, the calculation should be made at the highest ambient temperature (T_A) which could be expected in a realistic application (40-45°C) to ensure that the bypass group is not underdesigned and some margin exists.

5.3.2 Analysis Guidelines

The analyses performed on the conceptual designs in this study represent a basic set which should be performed for all systems. Additional types of analyses could be postulated which may be useful for some applications to obtain certain useful information. Additional analyses could include:

- Cabling, interconnection and switchgear losses for use as inputs to the design or the SOLCEL II analyses;
- Lightning analyses to determine the effectiveness of the protection designs;
- Switching transients from the switchgear or transients fed to the DC line from the inverter;
- Effects on output power of individual cell failure or statistical distributions of cell failures;
- Effects of recurring shadows on power output.

Depending on the complexity of the analysis formulation, these analyses could be performed either by hand or with PV-TAP. In most applications, hand analyses would be satisfactory for most of these. The analysis of the effects on output of statistical distributions of cell failures should be performed on PV-TAP if the percentage of failures could produce more than one per module. However, this would be more appropriate as a study than as a design tool.

The analysis of the effects of recurring shadows can be performed by hand to obtain rough estimates or with PV-TAP to obtain exact results. In either case, however, this analysis would be performed for a particular array at a selected site and would not apply to site-independent design.

The next paragraphs summarize recommendations for improvements and cautions in the analysis formulations previously presented in various other sections of this report. It should be remembered in each case that the results of any analysis are no more valid than the data used as inputs. The most accurate model will not produce accurate results based on estimated data.

If the series string of modules must be broken to model the array due to computer memory limitations, the largest number of modules which the computer can accept should be used to obtain the statistical distribution of module photocurrents. Next, the accuracy of the modeling should be determined by running the same number of modules in a string using the module-based parameters and photocurrent distribution, and comparing this with the cell-based results. Finally, the full series string of modules should be run with the module-based parameters.

For the hot spot heating analysis, the array should be run under short circuit conditions with the unshadowed cells operating at the short circuit temperature and an ambient temperature of 40-45°C to ensure that some temperature margin exists under worst case conditions. If the maximum cell temperature is exceeded, the impact must be assessed and the module design might require revision. If the margin is large, the module design could also be revised if a valid, less expensive design can be found.

In performing the SOLCEL II analysis, the PV input option which uses the detailed PV cell model is recommended. This formulation, however, requires technology dependent device parameters for accurate temperature dependence modeling. If these parameters cannot be determined accurately, the analyst might consider using the simpler efficiency versus temperature option in SOLCEL II. In performing comparative assessments, either methodology is valid but the methodology used must be the same for all analyses if comparisons are to be made.

The analyst could also consider modeling the SOLCEL II technology dependent parameters based on current-voltage versus temperature data. This technique is discussed in Section 5.1.4.2. The analyst is advised to study the PV cell model in SOLCEL II [2] carefully before attempting this technique.

The photocurrent variation effects were factored into the SOLCEL II output of the total annual AC energy produced. It is felt, however, that factoring the energy distributed to the load and that sold to the utility would be stretching the credibility of this simplified approximation. The analyst, who wishes to determine this energy distribution under photocurrent variation conditions, should consider factoring the SOLCEL II short circuit current and open circuit input values instead. This would, however, require making

SOLCEL II runs for each photocurrent variation condition instead of simply factoring the output of one run.

The economic analysis procedures outlined in section 4.0 and discussed in the references [2,3,46,47] are straightforward and can be applied to any system. Inputs consist of area dependent costs and power dependent costs, with the areas obtained from the module and system design and the output power determined from the SOLCEL II analysis. In the analyses performed in this study, most of the costs were estimated. If realistic life cycle costs are to be obtained, realistic cost data must first be obtained.

SECTION 6.0

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APPENDIX A
ADDITIONAL PV-TAP MODELING RUNS



AMORPHOUS SILICON CELL DATA REDUCTION INPUT LISTING

```

1      * 1CM SQUARE A-SI CELL
2      LIBRARY
3      PV ASIO1 11
4          G .5
5          IF 16
6          TEMP 298
7          ISC 16
8          DUDT -.0016
9          DIDT 9.76E-3
10         RS 5E-5
11         DATA DC RS
12             .7 14.4 .1
13             .73 13.7 1.0
14             .75 13.25 .1
15             .91 0.0 1.0
16
17         D BPD1 1
18             RB 1E-4
19             IS 8.24E-6
20             TH 20.
21
22     PVA1 1 0 5 T P ASIO1 0.0,0.0,0.0,S1
23     VIS S 0 1.0
24     VIT T 0 298
25     D1BP 0 1 BPD1
26     R1L 1 0 .08
27     X1=TABLE1(V(R1L))
28     TABLE1
29         0.0 16.0
30         .6 15.0
31         .7 14.4
32         .73 13.7
33         .75 13.25
34         .80 11.8
35         .91 0.0
36
37     STATE1
38         R1L 1E-6 1E-5 1E-4 1E-3 1E-2$
39         (4) 5E-2 (20) 6E-2 (4) 1E-1 1 10 100
40         PRINT V(R1L) I(R1L) X1 P(R1L) N(1)
41         PLOT X1 I(R1L) P(R1L) VS V(R1L)
42
43     END

```

AMORPHOUS SILICON CELL CURRENT
COMPARISON AND PARAMETER LISTING

DATA REDUCTION TYPE DC FOR ASI01

TERMINAL VOLTAGE	CURRENT	
	EXPERIMENTAL	CALCULATED

.7000E+00	.1440E+02	.1430E+02
.7300E+00	.1370E+02	.1372E+02
.7500E+00	.1325E+02	.1321E+02
.9100E+00	0.	-.1186E-01

1
LIBRARY VALUES AFTER COMPLETION OF DATA REDUCTION

TYPE	PREFIX	MODEL	
ASI01	PV	11	PHOTOVOLTAIC CELL
G	5.000000-001		
IS	5.098310+000		(1.38+000)
M	3.331877+000		(4.98-002)
VZ	1.100000+000		
N	5.000000-001		
C	1.500000+006		
W	2.000000-005		
A	1.500000+001		
VB	-3.500000+001		
B	1.000000+000		
RS	5.000000-005		
IP	1.600000-001		
KSC	4.500000-003		
T	5.000000+004		
CS	0.000000+000		
CST	0.000000+000		
CT	0.000000+000		
CTT	0.000000+000		
P	9.003934-001		(1.35-002)
SR	1.000000+000		
TR	2.980000+002		
ETA	1.000000+000		
GA	1.150000+004		
ALPHA	4.394357+003		(5.40+001)

CdS/CuInSe₂ CELL DATA REDUCTION INPUT LISTING

```

1      * 1CM CADMIUM SULFIDE CELL
2      LIBRARY
3          PV CDS01 11
4              G 1
5              IP 39.4
6              TEMP 298
7              ISC 39.4
8              DVDI -.002
9              DIDT 23.8E-3
10             DATA DC
11                 .24 38.9
12                 .3 36
13                 .36 24.5
14                 .424 0.0
15             D BPD1 1
16                 RB 1E-4
17                 IS 8.24E-6
18                 TH 20.
19     PVA1 1 0 S T P CDS01 0.0,0.0,0.0,S1
20     V1S S 0 1.0
21     V1T T 0 298
22     D1BP 0 1 BPD1
23     R1L 1 0 .08
24     X1=TABLE1(V(R1L))
25     TABLE1
26         0.0 39.4
27         .24 38.9
28         .3 36
29         .36 24.5
30         .424 0.0
31     STATE1
32         R1L 1E-6 2E-4 (9) 1E-3 (40) .01 (20)$
33         .05 (40) .1 (9) 1 10 100
34         PRINT V(R1L) I(R1L) X1 P(R1L) N(1)
35         PLOT X1 I(R1L) VS V(R1L)
36     END

```

CdS/CuInSe₂ CELL CURRENT COMPARISON AND PARAMETER LISTING

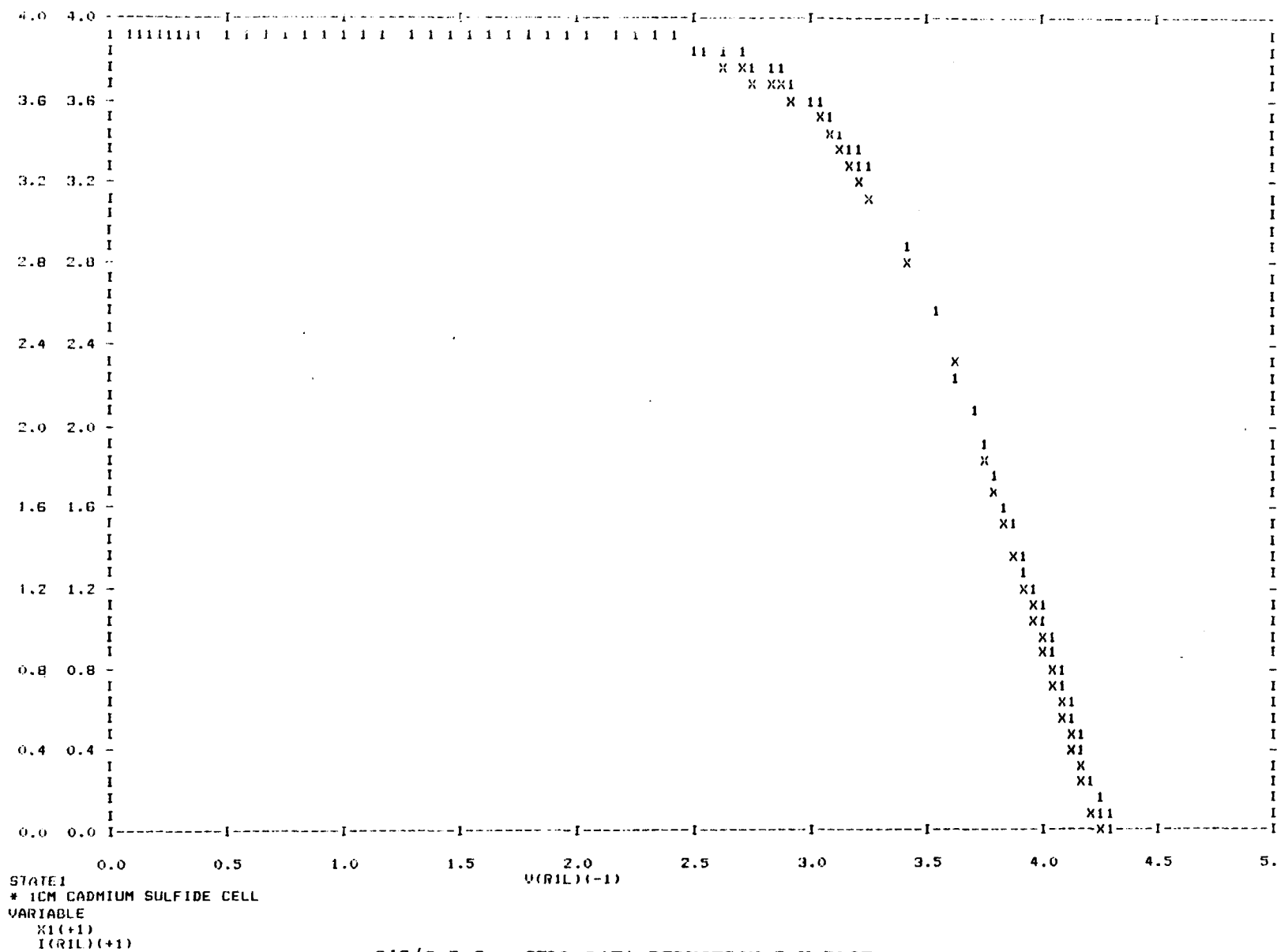
DATA REDUCTION TYPE DC FOR CDS01

TERMINAL VOLTAGE	CURRENT	
	EXPERIMENTAL	CALCULATED

.2400E+00	.3890E+02	.3888E+02
.3000E+00	.3600E+02	.3619E+02
.3600E+00	.2450E+02	.2377E+02
.4240E+00	0.	.1616E+01

1
LIBRARY VALUES AFTER COMPLETION OF DATA REDUCTION

TYPE	PREFIX	MODEL
CDS01	PV	11 PHOTOVOLTAIC CELL
G	1.000000+000	
IS	8.120212+003	(3.81+004)
M	7.981908-001	(6.73-002)
VZ	1.100000+000	
N	5.000000-001	
C	1.500000+006	
W	2.000000-005	
A	1.500000+001	
VB	-3.500000+001	
B	1.000000+000	
RS	2.057276-003	(1.64-004)
IP	3.940000+001	
KSC	4.500000+003	
T	5.000000+004	
CS	0.000000+000	
CST	0.000000+000	
CT	0.000000+000	
CTT	0.000000+000	
P	3.758500+000	(3.17-001)
SR	1.000000+000	
TR	2.980000+002	
ETA	1.000000+000	
GK	1.160000+004	
ALPHA	1.419492+004	(1.18+003)



GaAs FLAT PLATE CELL DATA REDUCTION INPUT LISTING

```

1      * 1CM SQUARE GALLIUM ARSENIDE FLAT PLATE CELL
2      LIBRARY
3          PV GAS01 11
4              G .1
5              TEMP 298
6              DEDT 25.0032
7              DIDD 15.3E-3
8              DATA DC
9                  .833 24.0 1.0
10                 .88 20.0 .1
11                 .90 17.2 .1
12                 .97 0.0 1.0
13
14      D BPD1 1
15          RB 1E-4
16          IS 8.24E-6
17          TH 20.
18
19      PVA1 1 0 S T P GAS01 0,0,0,0,0,S1
20      VIS S 0 1.0
21      VIT T 0 298
22      DIBP 0 1 BPD1
23      R1L 1 0 .08
24      X1=TABLE1(V(R1L))
25      TABLE1
26          0.0 25.0
27          .7 24.6
28          .8 24.2
29          .83 24.0
30          .88 20.0
31          .90 17.2
32          .97 0.0
33      STATE1
34          R1L 1E-6 2E-4 (9) 1E-3 (40) .01 (20)$
34          .05 (40) .1 (9) 1 10 100
35          PRINT V(R1L) I(R1L) X1 P(R1L) N(1)
36          PLOT X1 I(R1L) VS V(R1L)
37      END

```

GaAs FLAT PLATE CELL CURRENT
COMPARISON AND PARAMETER LISTING

DATA REDUCTION TYPE DC FOR GAS01

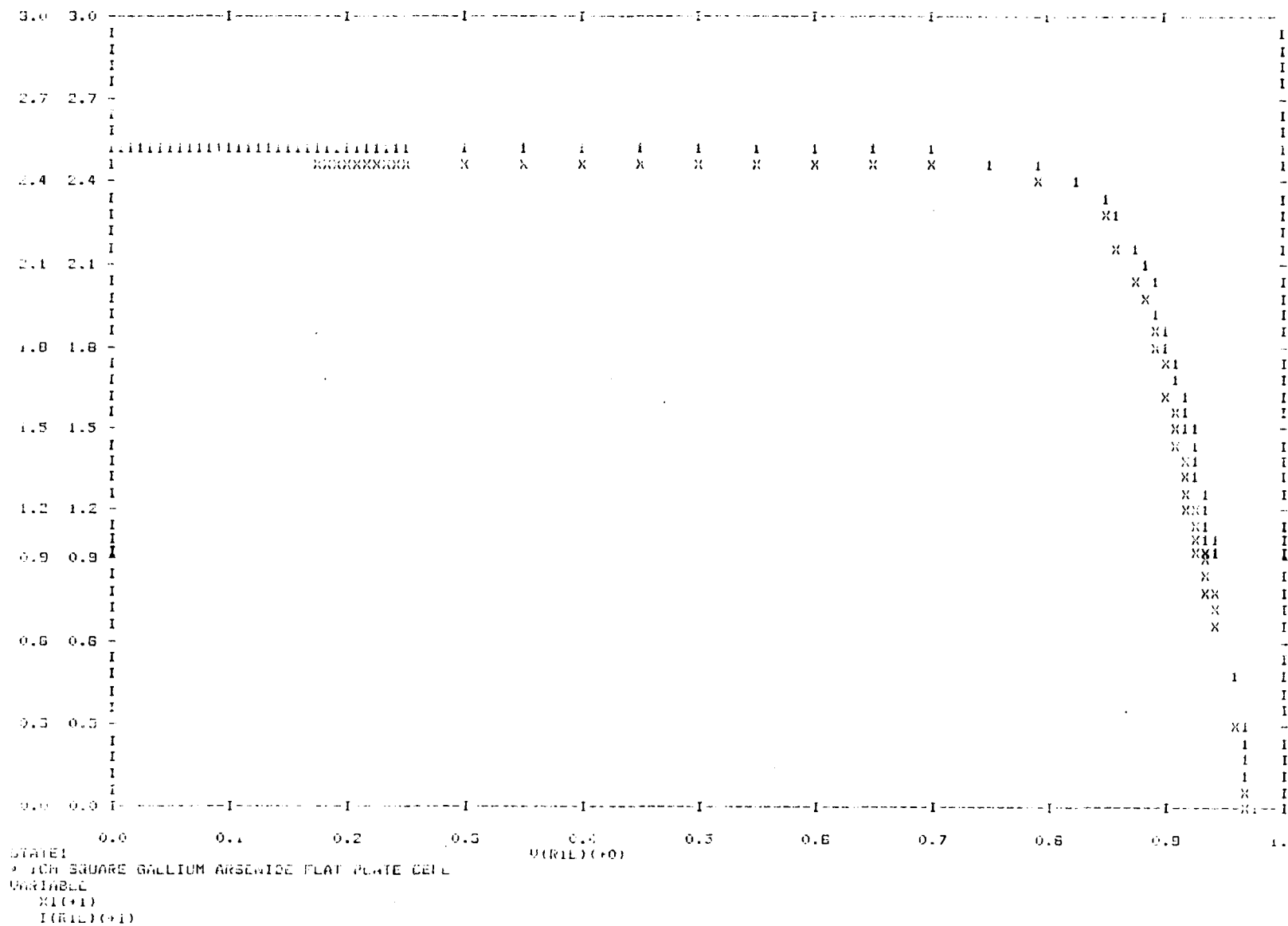
TERMINAL VOLTAGE	CURRENT	
	EXPERIMENTAL	CALCULATED

.8330E+00	.2400E+02	.2398E+02
.8800E+00	.2000E+02	.2120E+02
.9000E+00	.1720E+02	.1868E+02
.9700E+00	0.	.6482E+00

1

LIBRARY VALUES AFTER COMPLETION OF DATA REDUCTION

TYPE	PREFIX	MODEL	
GAS01	PV	11	PHOTOVOLTAIC CELL
G	1.000000-001		
IS	1.967180+007		(5.33+008)
M	1.209428+000		(4.75-001)
VZ	1.100000+000		
N	5.000000-001		
C	1.500000+006		
W	2.000000-005		
A	1.500000+001		
VB	-3.500000+001		
B	1.000000+000		
RS	1.538445-003		(1.67-003)
IP	2.500000+001		
KSC	4.500000+003		
T	5.000000+004		
CS	0.000000+000		
CST	0.000000+000		
CT	0.000000+000		
CTT	0.000000+000		
P	2.480512+000		(9.75-001)
SR	1.000000+000		
TR	2.980000+002		
ETA	1.000000+000		
GK	1.160000+004		
ALPHA	1.757900+004		(6.99+003)



GaAs FLAT PLATE CELL DATA REDUCTION I-V PLOT

GaAs CONCENTRATOR CELL DATA REDUCTION INPUT LISTING

```

1  * GALLIUM ARSENIDE CONCENTRATOR CELL DATA REDUCTION
2  LIBRARY
3      PV GAD01 --
4          E .1
5          IP 17.52
6          TEMP 373
7          ISC 5750
8          DVDT -1.014
9          DIDD 5.0
10         DATA 20
11             1.2 8250 .1
12             1.25 8000 1.0
13             1.3 7500 .1
14             1.5 0.0 1.0
15
16         B BPD1 --
17             RB 1E-4
18             IS 8.24E-5
19             TH 20.
20
21     PVAL 1 0 S T P GAD01 0,0,0,0,0,51
22     VIS 5 0 500
23     VIT 7 0 373
24     DISP 0 1 BPD1
25     RIL 1 0 .08
26     X1=TABLE1(V(RIL))
27
28     TABLE1
29         0.0 8750
30         1.0 8700
31         1.2 8250
32         1.25 8000
33         1.3 7500
34         1.5 0.0
35
36     STATE1
37         RIL 1E-6 1E-5 (8) 1E-4 (20) 2E-4 (8) 1E-3 1E-2 1E-1 1 10
38         PRINT V(RIL) I(RIL) X1 P(RIL) N(1)
39         PLOT X1 I(RIL) VS V(RIL)
40
41     END

```


GaAs CONCENTRATOR CELL CURRENT
COMPARISON AND PARAMETER LISTING

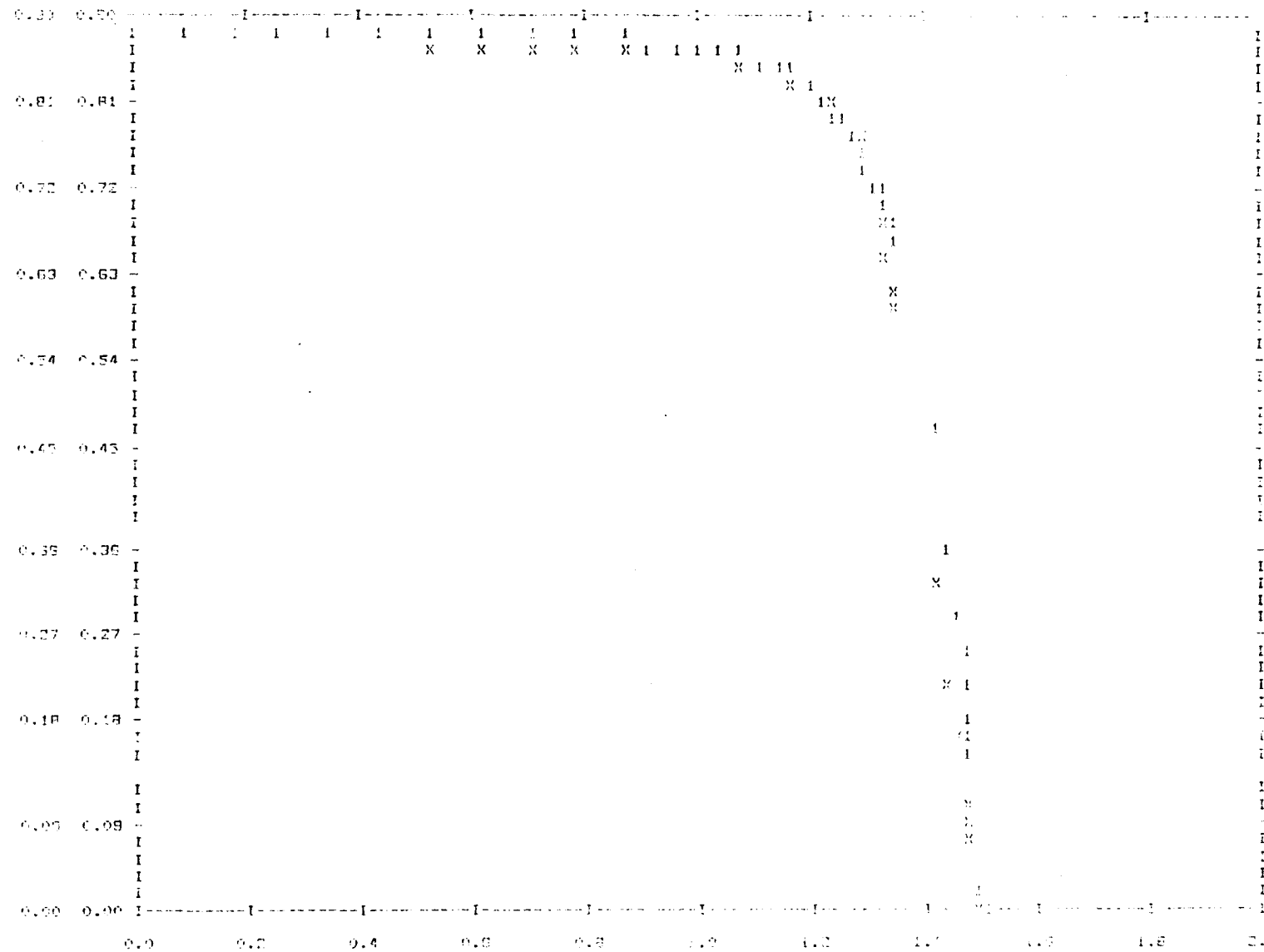
DATA REDUCTION TYPE DC FOR GAC01

TERMINAL VOLTAGE	CURRENT	
	EXPERIMENTAL	CALCULATED

.1200E+01	.8250E+04	.8252E+04
.1230E+01	.8000E+04	.7935E+04
.1300E+01	.7600E+04	.7424E+04
.1500E+01	0.	.2454E+02

LIBRARY VALUES AFTER COMPLETION OF DATA REDUCTION

TYPE	PREFIX	MODEL	
GAC01	PV	11	PHOTOVOLTAIC CELL
G	1.000000-001		
IS	1.126176+023		(5.68+024)
M	3.190282+000		(2.46+000)
VZ	1.100000+000		
N	5.000000-001		
C	1.500000+005		
W	2.000000-005		
A	1.500000+001		
VB	-3.500000+001		
B	1.000000+000		
RS	1.000000-006		(2.37-005)
IP	1.752000+001		
KSC	4.500000+003		
T	5.000000+004		
CS	0.000000+000		
CST	0.000000+000		
CT	0.000000+000		
CYT	0.000000+000		
P	9.403556-001		(7.25-001)
SR	1.000000+000		
TR	2.980000+002		
ETA	1.000000+000		
QK	1.160000+004		
ALPHA	2.394434+004		(1.83+004)



STATISTICAL
 1 GALLIUM ARSENIDE CONCENTRATOR CELL DATA REDUCTION
 VARIABLES
 N = 100
 1. 0.000000

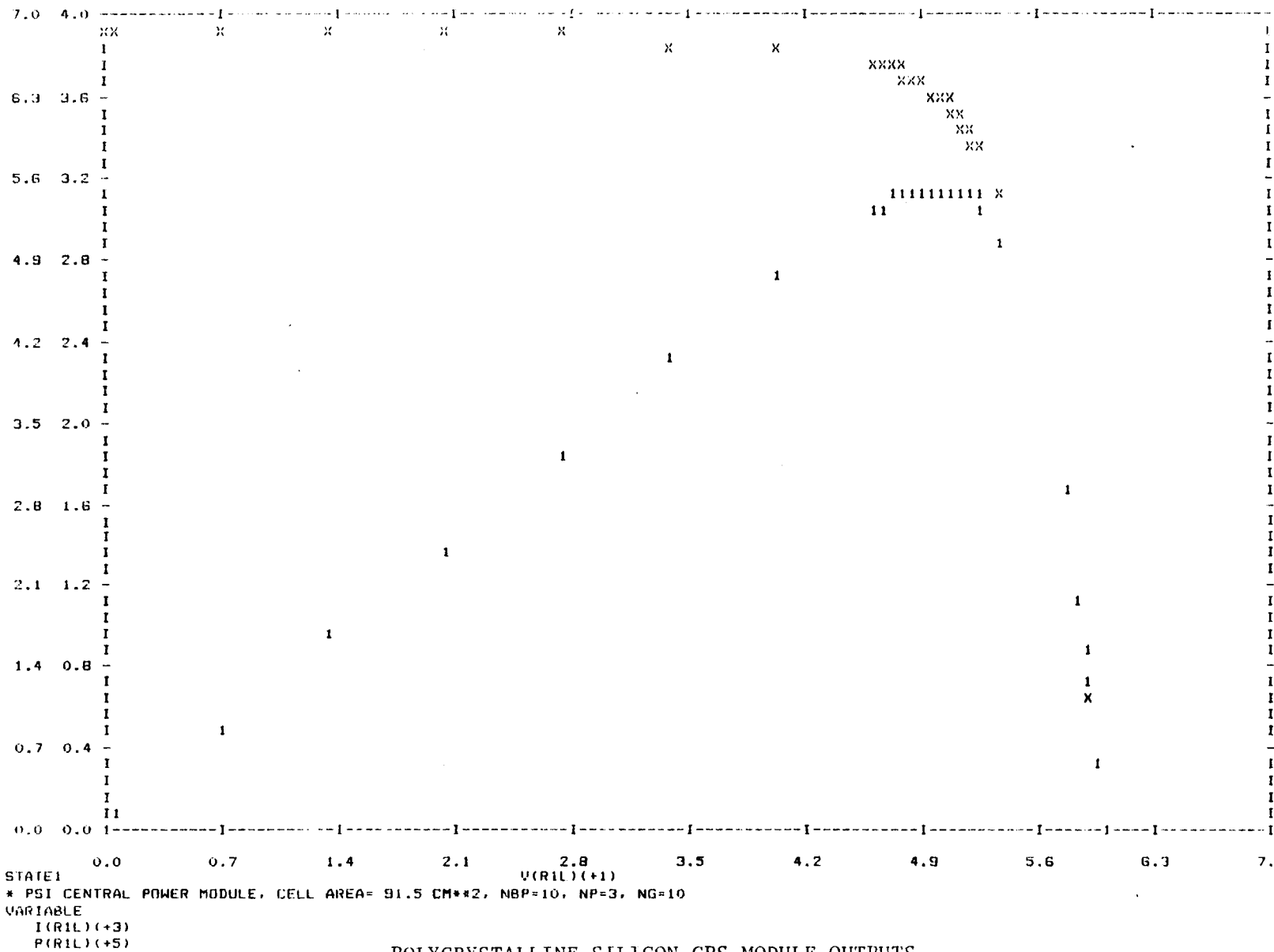
GaAs CONCENTRATOR CELL DATA REDUCTION I-V PLOT

POLYCRYSTALLINE SILICON CPS MODULE COMPUTER MODEL

```

1  * PSI CENTRAL POWER MODULE, CELL AREA= 91.5 CM**2, NBP=10, NP=3, NG=10
2  LIBRARY
3      PU PSI01 11
4          M 1.271214
5          P 2.359849
6          ALPHA 1.05484E4
7          CT .00061
8          G 91.5
9          IP 2.29E3
10         IS 8.01E4
11         RS 4.39E-6
12     D BPD1 1
13         RE 1E-4
14         IS 8.24E-6
15         TH 20.
16     DEFINE MODULE POS NEG 0
17         PVA1 POS 1 S T P1 PSI01 0.0,0.0,0.0,S10P3
18         PVA2 1 2 S T P2 PSI01 0.0,0.0,0.0,S10P3
19         PVA3 2 3 S T P3 PSI01 0.0,0.0,0.0,S10P3
20         PVA4 3 4 S T P4 PSI01 0.0,0.0,0.0,S10P3
21         PVA5 4 5 S T P5 PSI01 0.0,0.0,0.0,S10P3
22         PVA6 5 6 S T P6 PSI01 0.0,0.0,0.0,S10P3
23         PVA7 6 7 S T P7 PSI01 0.0,0.0,0.0,S10P3
24         PVA8 7 8 S T P8 PSI01 0.0,0.0,0.0,S10P3
25         PVA9 8 9 S T P9 PSI01 0.0,0.0,0.0,S10P3
26         PVA10 9 NEG S T P10 PSI01 0.0,0.0,0.0,S10P3
27         D1BP 1 POS 2PD1
28         D2BP 2 1 BPD1
29         D3BP 3 2 BPD1
30         D4BP 4 3 BPD1
31         D5BP 5 4 BPD1
32         D6BP 6 5 BPD1
33         D7BP 7 6 BPD1
34         D8BP 8 7 BPD1
35         D9BP 9 8 BPD1
36         D10BP NEG 9 BPD1
37         V1S S 0 1.0
38         V1T T 0 298
39     MODULE1 1 0 0
40     R1L 1 0 .08
41     STATE1
42         R1L 1E-6 1E-5 1E-4 1E-3$
42     (6) 7E-3 (20) 9E-3 1E-2$
42     (4) 5E-2 1E-1 1 10 100
43     PRINT V(R1L) I(R1L) P(R1L)$
43     V(MODULE1,PVA1) V(MODULE1,PVA2) V(MODULE1,PVA3) V(MODULE1,PVA4)
44     PLOT I(R1L) P(R1L) VS V(R1L)
45     END

```



AMORPHOUS SILICON RESIDENTIAL MODULE COMPUTER MODEL

```

1  * A-SI MODULE, A=23.1CM**2, NBP=7, NF=10, NG=2
2  LIBRARY
3      PV ASI01 11
4          M 3.331877
5          P 9.003934E-1
6          ALPHA 4.364357E3
7          CT .00061
8          G 11.8
9          IP 370
10         IS 118.0
11         RS 2.16E-6
12     D BPD1 1
13         RS 1E-4
14         IS 8.24E-3
15         TH 20.
16 DEFINE MODULE POS NEG 0
17     PVA1 POS 1 S T P1 ASI01 0,0,0,0,0,57P10
18     PVA2 1 NEG S T P2 ASI01 0,0,0,0,0,57P10
19     D1BP 1 POS BPD1
20     D2BP NEG 1 BPD1
21     V1S S 0 1.0
22     V1T T 0 298
23 MODULE1 1 0 0
24 R1L 1 0 .08
25 STATE1
26     R1L 1E-6 1E-5 1E-4 1E-3 (4) 3E-3 (10) 4E-3 (6) 1E-2 (3)*
26     .1 1 10 100
27     PRINT V(R1L) I(R1L) P(R1L) V(MODULE1.PVA1) V(MODULE1.PVA2)
28     PLOT I(R1L) P(R1L) VS V(R1L)
29 END

```

```

...STATE1
* H-BD1 MODULE, A=23.1CM*2, B=7, W=10, M=2
...MODULE
  I(R,1)(-5)
  F(R,2)(+4)

```

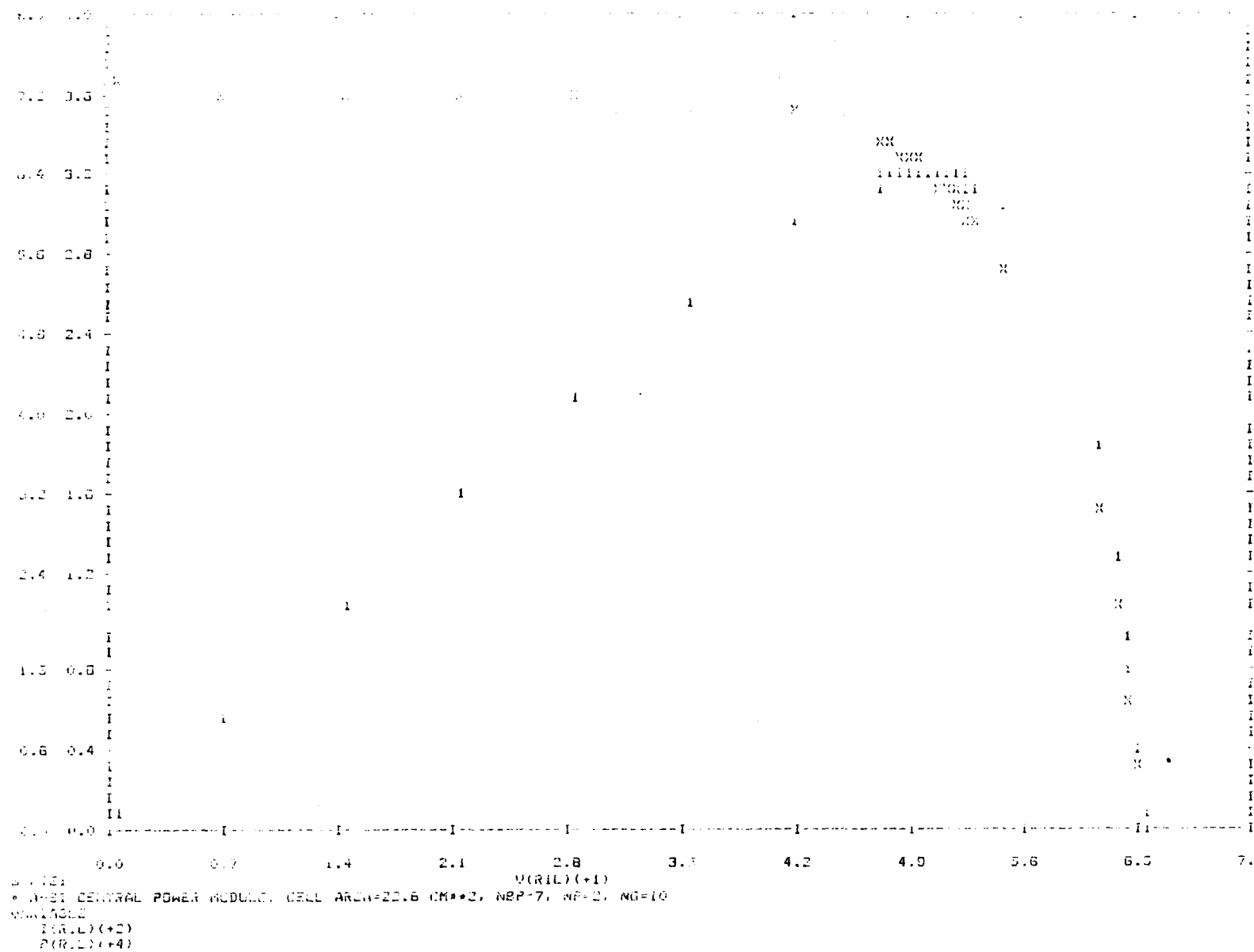
AMORPHOUS SILICON RESIDENTIAL MODULE OUTPUTS

AMORPHOUS SILICON CPS MODULE COMPUTER MODEL

```

1  * A-SI CENTRAL POWER MODULE, CELL AREA=22.8 CM**2, NBP=7, NP=2, NG=10
2  LIBRARY
3      PV ASI01 11
4          M 3.331877
5          P 5.003934E-1
6          ALPHA 4.334337E3
7          CT .0008.
8          G 11.0
9          IP 363
10         IS 118
11         RS 2.19E-6
12     D BPD1 1
13         RS 1E-4
14         IS 8.24E-6
15         TH 20.
16  DEFINE MODULE POS NEG 0
17      PVA1 POS 1 S T P1 ASI01 0.0,0.0,0.0,57F2
18      PVA2 1 2 S T P2 ASI01 0.0,0.0,0.0,57F2
19      PVA3 2 3 S T P3 ASI01 0.0,0.0,0.0,57F2
20      PVA4 3 4 S T P4 ASI01 0.0,0.0,0.0,57F2
21      PVA5 4 5 S T P5 ASI01 0.0,0.0,0.0,57F2
22      PVA6 5 6 S T P6 ASI01 0.0,0.0,0.0,57F2
23      PVA7 6 7 S T P7 ASI01 0.0,0.0,0.0,57F2
24      PVA8 7 8 S T P8 ASI01 0.0,0.0,0.0,57F2
25      PVA9 8 9 S T P9 ASI01 0.0,0.0,0.0,57F2
26      PVA10 9 NEG 5 T P.0 ASI01 0.0,0.0,0.0,57F2
27      D1BP 1 POS BPD1
28      D2BP 2 1 BPD1
29      D3BP 3 2 BPD1
30      D4BP 4 3 BPD1
31      D5BP 5 4 BPD1
32      D6BP 6 5 BPD1
33      D7BP 7 6 BPD1
34      D8BP 8 7 BPD1
35      D9BP 9 8 BPD1
36      D10BP NEG 5 BPD1
37      VIS S 0 1.0
38      VIT T 0 296
39  MODULE1 1 0 0
40  RIL 1 0 .08
41  STATE1
42      RIL 1E-6 1E-5 1E-4 1E-3*
42  1E-2 (5) 7E-2 (20) 5E-2 1E-1 (4) 5E-1 1 10 100
43  PRINT V(RIL) I(RIL) P(RIL) V(MODULE1.PVA1) V(MODULE1.PVA2)
44  PLOT I(RIL) P(RIL) VS V(RIL)
45  END

```



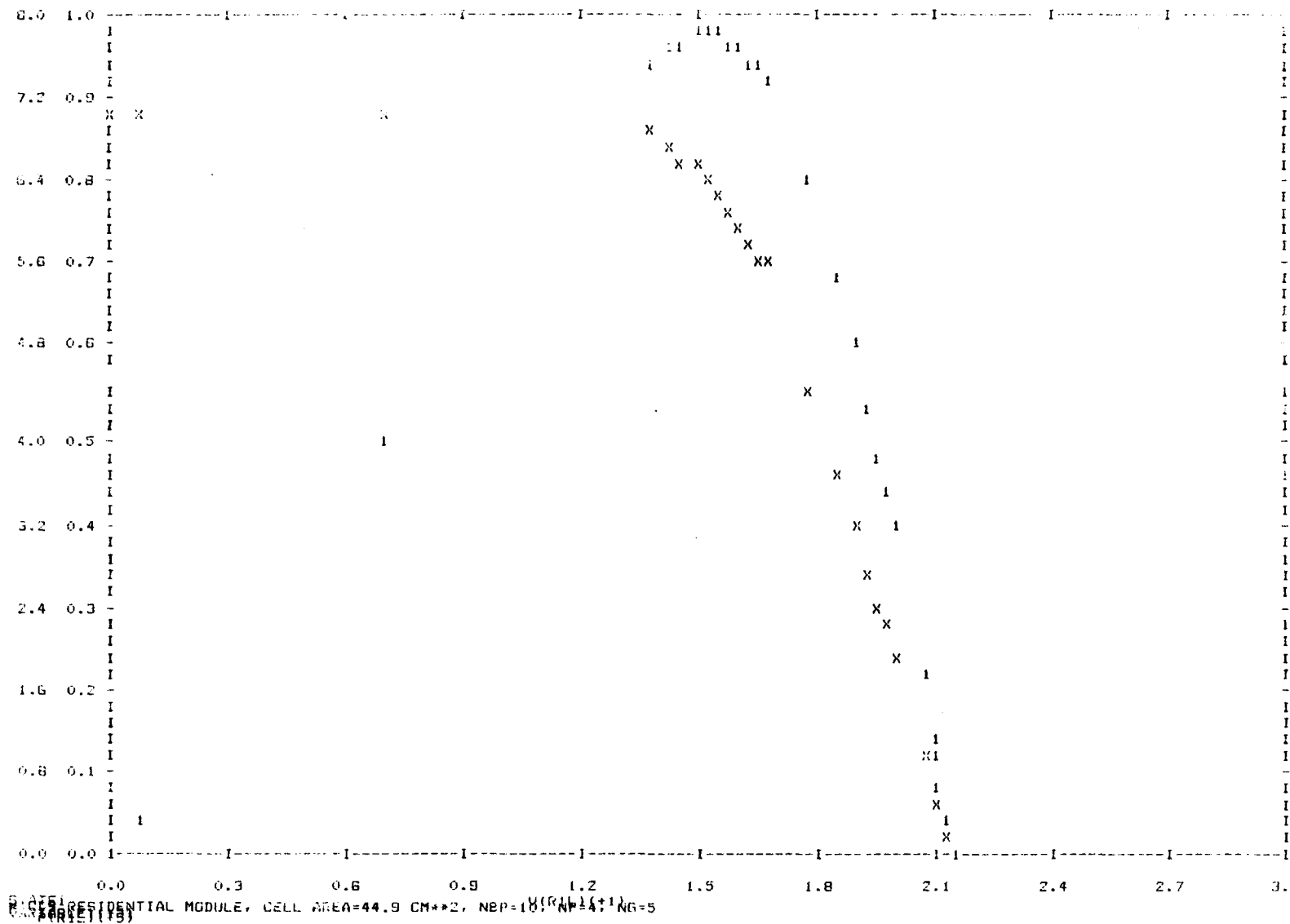
CdS/CuInSe₂ RESIDENTIAL MODULE COMPUTER MODEL

```

1  * CDS RESIDENTIAL MODULE, CELL AREA=44.9 CM**2, NSP=10, NP=4, NG=5
2  LIBRARY
3      PV CDS01 11
4          M .7581508
5          P 3.7585
6          ALPHA 1.418452E4
7          CT .00061
8          G 44.9
9          IP 1.77E3
10         IS 3.65E5
11         RS 4.58E-5

12         D BPD1 1
13             RB 1E-4
14             IS 8.24E-6
15             TH 20.
16     DEFINE MODULE POS NEG 0
17         PVA1 POS 1 S T P1 CDS01 0,0,0,0,0,S10P4
18         PVA2 1 2 S T P2 CDS01 0,0,0,0,0,S10P4
19         PVA3 2 3 S T P3 CDS01 0,0,0,0,0,S10P4
20         PVA4 3 4 S T P4 CDS01 0,0,0,0,0,S10P4
21         PVA5 4 NEG S T P5 CDS01 0,0,0,0,0,S10P4
22         D1BP 1 POS BPD1
23         D2BP 2 1 BPD1
24         D3BP 3 2 BPD1
25         D4BP 4 3 BPD1
26         D5BP NEG 4 BPD1
27         VIS S 0 1.0
28         VIT T 0 298
29     MODULE1 1 0 0
30     R1L 1 0 .08
31     STATE1
32         R1L 1E-6 1E-5 1E-4 1E-3$
32         ZE-3 (10) 3E-3 (7) 1E-2$
32         (4) 5E-2 1E-1 1 10 100
33         PRINT V(R1L) I(R1L) P(R1L)$
33         V(MODULE1.PVA1) V(MODULE1.PVA2) V(MODULE1.PVA4) V(MODULE1.PVA5)
34         PLOT I(R1L) P(R1L) VS V(R1L)
35     END

```

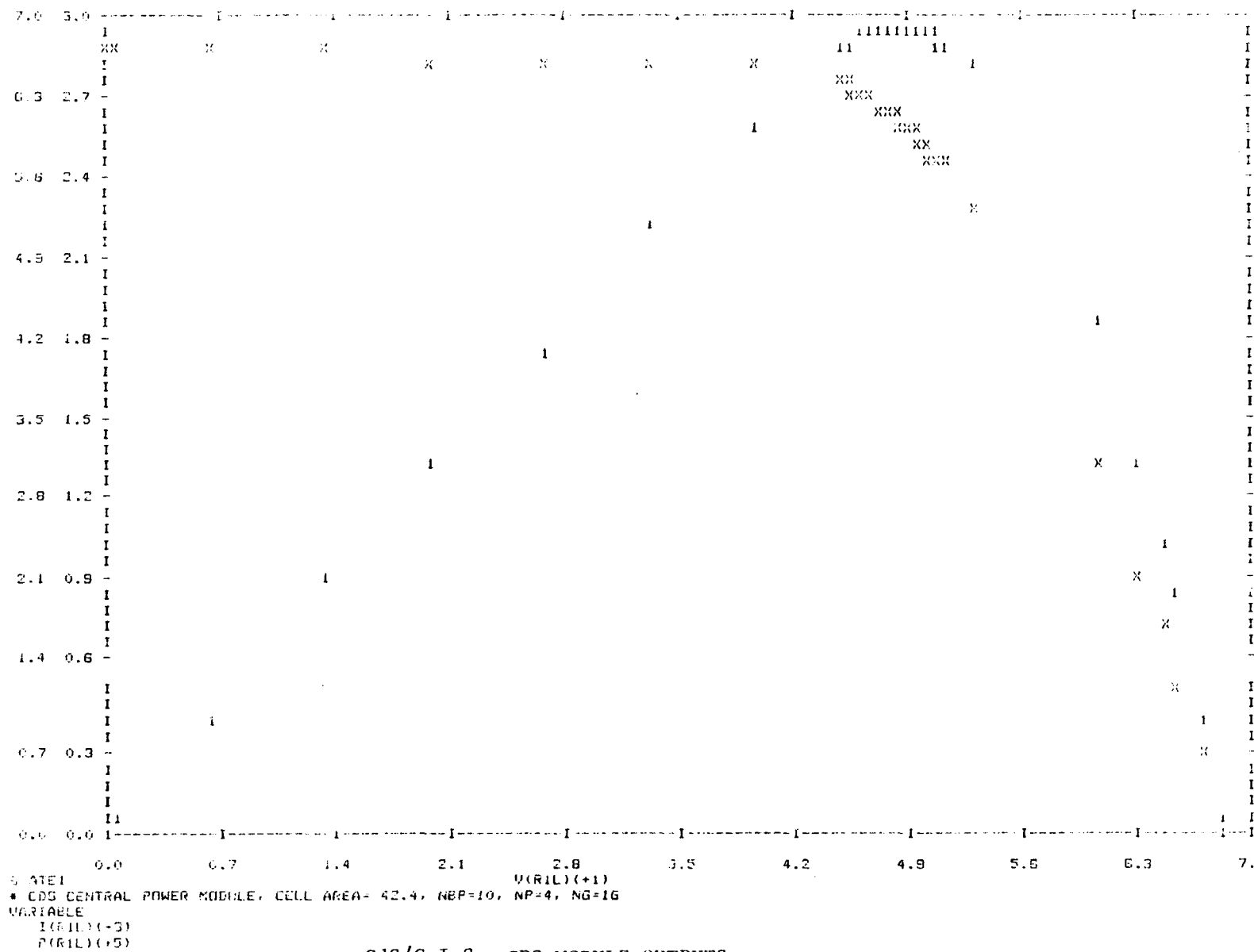


CdS/CuInSe₂ CPS MODULE COMPUTER MODEL

```

1  * CDS CENTRAL POWER MODULE, CELL AREA= 42.4, NBP=10, NP=4, NG=16
2  LIBRARY
3      PU CDS01 11
4          M .7981908
5          ALPHA555419492E4
6          CT .00061
7          G 42.4
8          IP 1.67E3
9          IS 3.44E5
10         RS 4.85E-5
11
12     D BPD1 1
13         RB 1E-4
14         IS 8.24E-6
15         TH 20.
16
17 DEFINE MODULE POS NEG 0
18     PVA1 POS 1 S T P1 CDS01 0.0,0.0,0.0,S10P4
19     PVA2 1 2 S T P2 CDS01 0.0,0.0,0.0,S10P4
20     PVA3 2 3 S T P3 CDS01 0.0,0.0,0.0,S10P4
21     PVA4 3 4 S T P4 CDS01 0.0,0.0,0.0,S10P4
22     PVA5 4 5 S T P5 CDS01 0.0,0.0,0.0,S10P4
23     PVA6 5 6 S T P6 CDS01 0.0,0.0,0.0,S10P4
24     PVA7 6 7 S T P7 CDS01 0.0,0.0,0.0,S10P4
25     PVA8 7 8 S T P8 CDS01 0.0,0.0,0.0,S10P4
26     PVA9 8 9 S T P9 CDS01 0.0,0.0,0.0,S10P4
27     PVA10 9 10 S T P10 CDS01 0.0,0.0,0.0,S10P4
28     PVA11 10 11 S T P11 CDS01 0.0,0.0,0.0,S10P4
29     PVA12 11 12 S T P12 CDS01 0.0,0.0,0.0,S10P4
30     PVA13 12 13 S T P13 CDS01 0.0,0.0,0.0,S10P4
31     PVA14 13 14 S T P14 CDS01 0.0,0.0,0.0,S10P4
32     PVA15 14 15 S T P15 CDS01 0.0,0.0,0.0,S10P4
33     PVA16 15 NEG S T P16 CDS01 0.0,0.0,0.0,S10P4
34     D1BP 1 POS BPD1
35     D2BP 2 1 BPD1
36     D3BP 3 2 BPD1
37     D4BP 4 3 BPD1
38     D5BP 5 4 BPD1
39     D6BP 6 5 BPD1
40     D7BP 7 6 BPD1
41     D8BP 8 7 BPD1
42     D9BP 9 8 BPD1
43     D10BP 10 9 BPD1
44     D11BP 11 10 BPD1
45
46     D12BP 12 11 BPD1
47     D13BP 13 12 BPD1
48     D14BP 14 13 BPD1
49     D15BP 15 14 BPD1
50     D16BP NEG 15 BPD1
51
52     VIS S 0 1.0
53     VIT T 0 298
54
55 MODULE1 1 0 0
56 R1L 1 0 .08
57 STATE1
58     R1L 1E-6 1E-5 1E-4 1E-3*
59     (6) 7E-3 (20) 9E-3 1E-2*
60     (4) 5E-2 1E-1 1 10 100
61     PRINT V(R1L) I(R1L) P(R1L)*
62     V(MODULE1.PVA1) V(MODULE1.PVA4) V(MODULE1.PVA12) V(MODULE1.PVA16)
63     PLOT I(R1L) P(R1L) VS V(R1L)
64
65 END

```

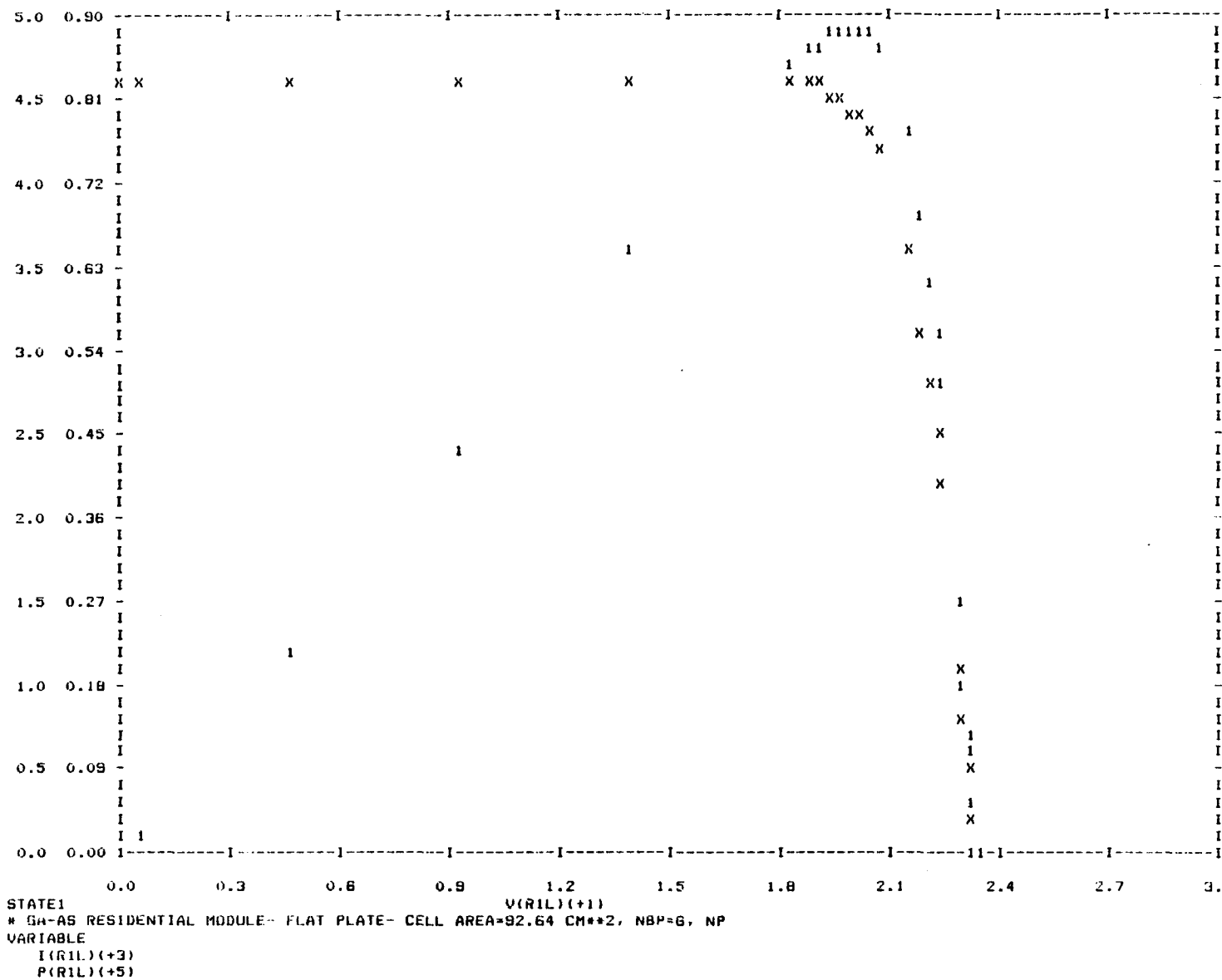


GaAs FLAT PLATE RESIDENTIAL MODULE COMPUTER MODEL

```

1  * GA-AS RESIDENTIAL MODULE- FLAT PLATE- CELL AREA=92.64 CM**2, NBP=6, NP
2  LIBRARY
3      PV GAS01 11
4          M 1.209428
5          P 2.480512
6          ALPHA 1.7579E4
7          CT .00061
8          G 9.264
9          IP 2.316E3
10         IS 1.822E9
11         RS 1.661E-5
12     D BPD1 1
13         RB 1E-4
14         IS 8.24E-6
15         TH 20.
16     DEFINE MODULE POS NEG 0
17         PVA1 POS 1 S T P1 GAS01 0,0,0,0,0,P2SG
18         PVA2 1 2 S T P2 GAS01 0,0,0,0,0,P2SG
19         PVA3 2 3 S T P3 GAS01 0,0,0,0,0,P2SG
20         PVA4 3 NEG S T P4 GAS01 0,0,0,0,0,P2SG
21         D1BP 1 POS BPD1
22         D2BP 2 1 BPD1
23         D3BP 3 2 BPD1
24         D4BP NEG 3 BPD1
25         V1S S 0 1.0
26         V1T T 0 298
27     MODULE1 1 0 0
28     R1L 1 0 .08
29     STATE1
30         R1L 1E-6 1E-5 1E-4 1E-3$
30         (3) 4E-3 (10) 5E-3 (5) 1E-2$
30         (4) 5E-2 1E-1 1 10 100
31         PRINT V(R1L) I(R1L) P(R1L)$
31     V(MODULE1.PVA1) V(MODULE1.PVA2) V(MODULE1.PVA3) V(MODULE1.PVA4)
32     PLOT I(R1L) P(R1L) VS V(R1L)
33     END

```



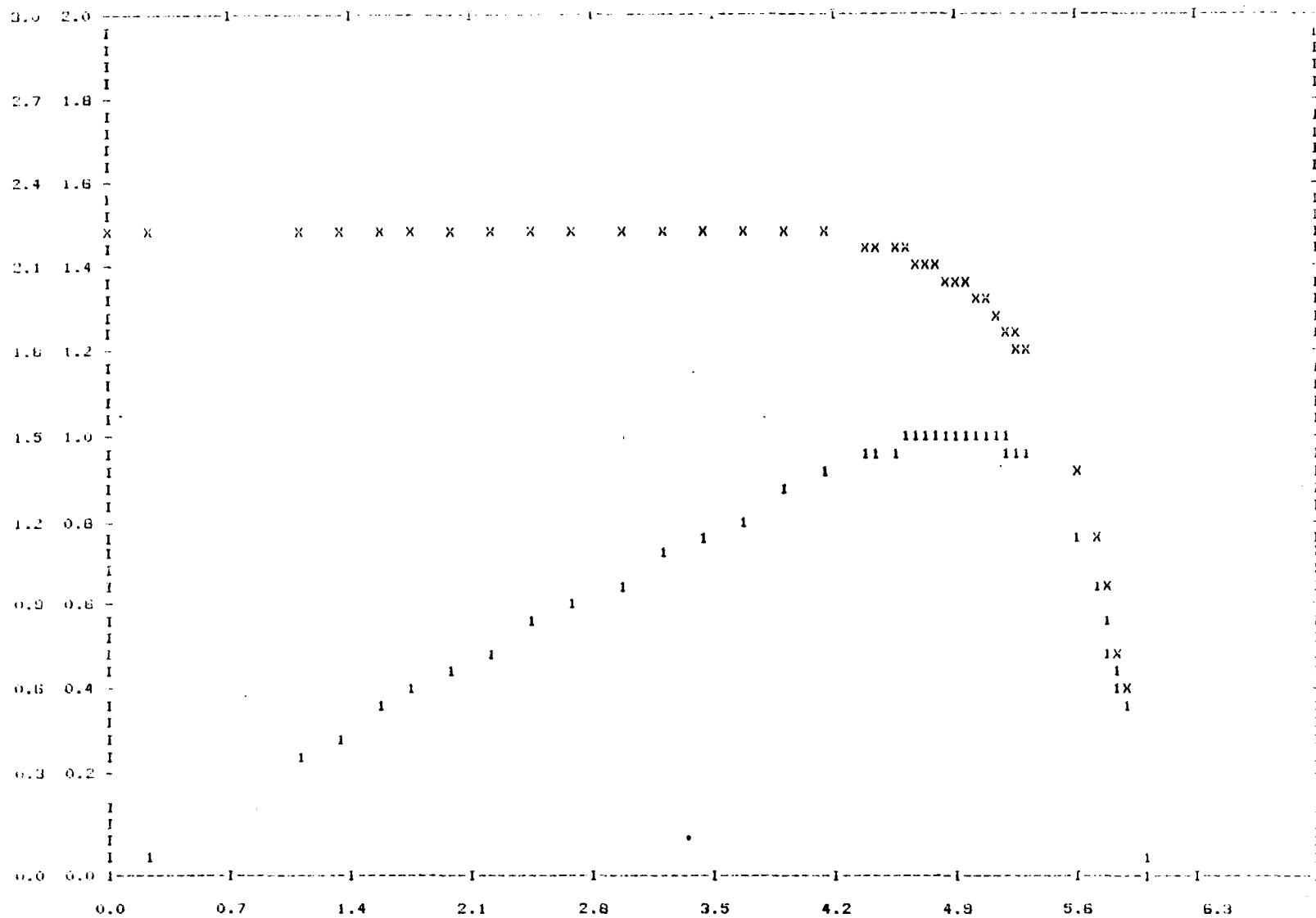
CaAs CONCENTRATOR CPS MODULE COMPUTER MODEL

```

1      * GA-AS CONCENTRATOR CENTRAL POWER MODULE
2      LIBRARY
3          PV GAC01 11
4              M 3.190282
5              P .9403556
6              ALPHA 2.394434E4
7              CT .00061
8              TR 373
9              G .127
10             IS 1.427E23
11             IP 22.20
12             RS 7.893E-7
13         D BPD1 1
14             RB 1E-4
15             IS 8.24E-6
16             TH 20.
17         PVA1 A 1 S T P1 GAC01 0,0,0,0,0,S4P2
18         PVA2 1 2 S T P2 GAC01 0,0,0,0,0,S4P2
19         PVA3 2 3 S T P3 GAC01 0,0,0,0,0,S4P2
20         PVA4 3 4 S T P4 GAC01 0,0,0,0,0,S4P2
21         PVA5 4 5 S T P5 GAC01 0,0,0,0,0,S4P2
22         PVA6 5 6 S T P6 GAC01 0,0,0,0,0,S4P2
23         PVA7 6 7 S T P7 GAC01 0,0,0,0,0,S4P2
24         PVA8 7 8 S T P8 GAC01 0,0,0,0,0,S4P2
25         PVA9 8 9 S T P9 GAC01 0,0,0,0,0,S4P2
26         PVA10 9 8 S T P10 GAC01 0,0,0,0,0,S4P2
27         D1BP 1 A BPD1
28         D2BP 2 1 BPD1
29         D3BP 3 2 BPD1
30         D4BP 4 3 BPD1
31         D5BP 5 4 BPD1
32         D6BP 6 5 BPD1
33         D7BP 7 6 BPD1
34         D8BP 8 7 BPD1
35         D9BP 9 8 BPD1
36         D10BP 9 9 BPD1
37         V1S S 0 500.0
38         V1T T 0 373.0
39         R1L A B .08

40     STATE1
41         R1L 1E-6 1E-5 1E-4 5E-4 (5) 1E-3$
41         (S) 2E-3 (20) 3E-3 (7) 1E-2 1E-1 1 10 100
42         PRINT V(R1L) I(R1L) P(R1L) V(PVA1) V(PVA4) V(PVA8) V(PVA10)
43         PLOT I(R1L) P(R1L) VS V(R1L)
44     END

```



7.

STAFF1

* GA-AS CONCENTRATOR CENTRAL POWER MODULE

VARIABLE

I(R1L)(+4)

P(R1L)(+6)

GaAs CONCENTRATOR CPS MODULE OUTPUTS

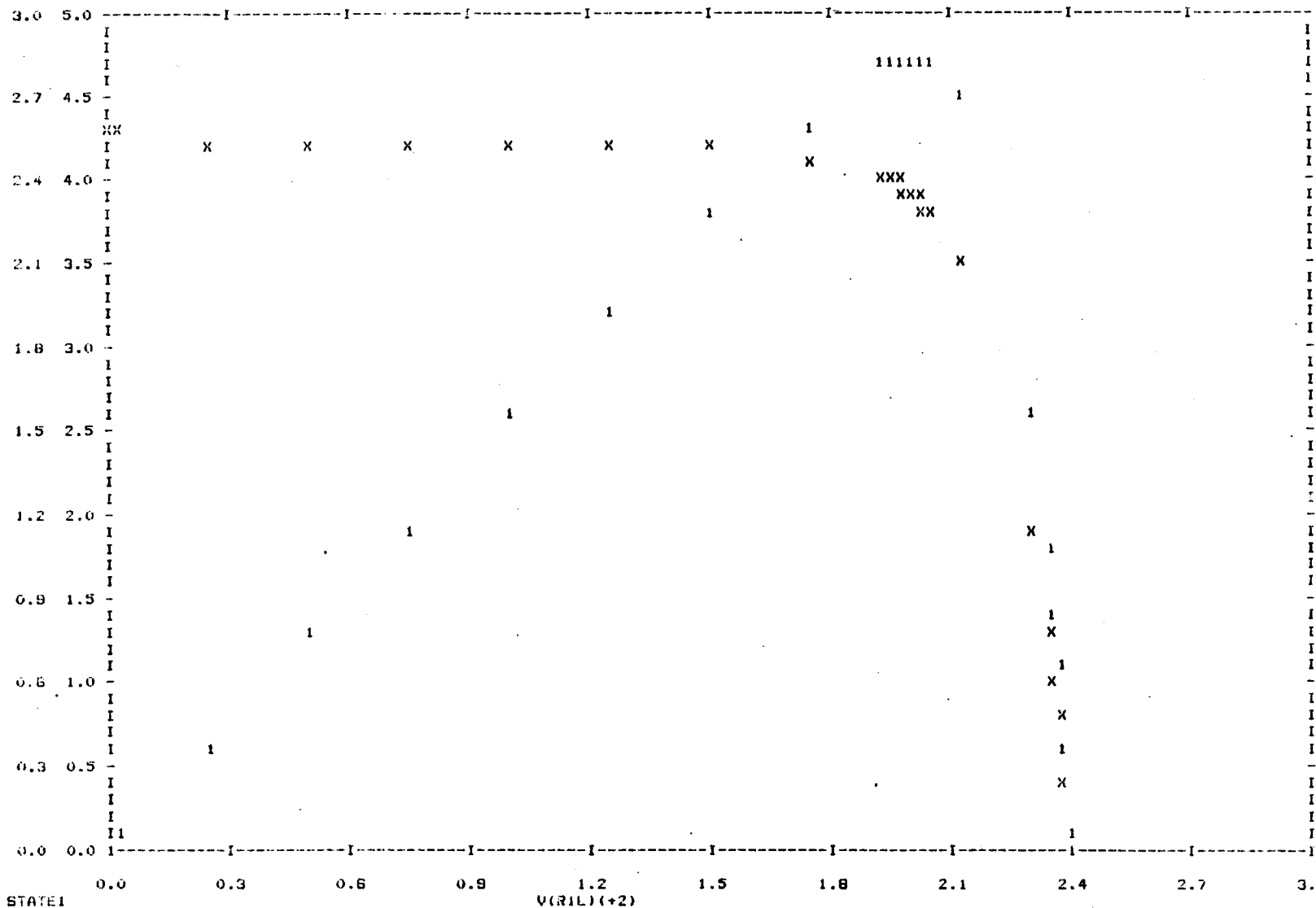
POLYCRYSTALLINE SILICON RESIDENTIAL ARRAY COMPUTER MODEL

```

1      * PSI RESIDENTIAL ARRAY
2      LIBRARY
3          PV PSI01 11
4              M 1.271214
5              P 2.359949
6              ALPHA 1.05484E4
7              CT .00061
8              G 85.1
9              IP 2.13E3
10             IS 7.45E4
11             RS 4.72E-6
12             D BPD1 1
13                 RB 1E-4
14                 IS 8.24E-6
15                 TH 20.
16     DEFINE MODULE POS NEG 0
17         PVA1 POS 1 S T P1 PSI01 0,0,0,0,0,S10P4
18         PVA2 1 2 S T P2 PSI01 0,0,0,0,0,S10P4
19         PVA3 2 3 S T P3 PSI01 0,0,0,0,0,S10P4
20         PVA4 3 NEG S T P4 PSI01 0,0,0,0,0,S10P4
21         D1BP 1 POS BPD1
22         D2BP 2 1 BPD1
23         D3BP 3 2 BPD1
24         D4BP NEG 3 BPD1
25         V1S S 0 1.0
26         V1T T 0 298
27     DEFINE SUBARRAY A B 0
28         MODULE1 A 1 0
29         MODULE2 1 2 0
30         MODULE3 2 3 0
31         MODULE4 3 4 0
32         MODULE5 4 5 0
33         MODULE6 5 6 0
34         MODULE7 6 7 0
35         MODULE8 7 8 0
36         MODULE9 8 9 0
37         MODULE10 9 8 0
38     SUBARRAY1 1 0 0
39     SUBARRAY2 1 0 0
40     SUBARRAY3 1 0 0
41     R1L 1 0 .08
42     STATE1
43         R1L 1E-6 1E-5 1E-4 1E-3$
43     (7) 8E-3 (20) 9E-3 1E-2$
43     (4) 5E-2 1E-1 1 10 100 .
44         PRINT V(R1L) I(R1L) P(R1L)
45         PLOT I(R1L) P(R1L) VS V(R1L)
46     END

```

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STATE1
 * PSI RESIDENTIAL ARRAY
 VARIABLE
 I(RIL)(+4)
 P(RIL)(+6)

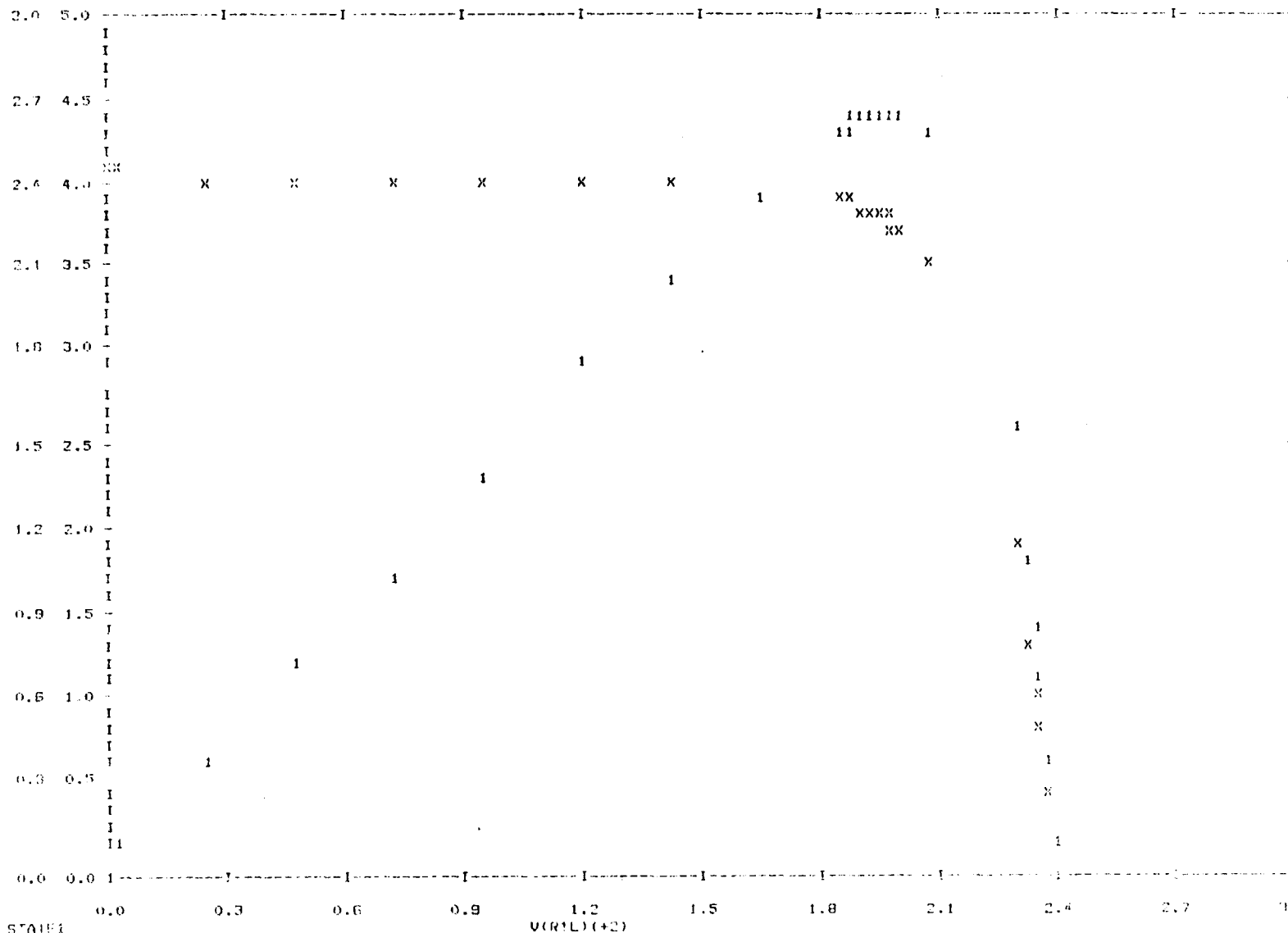
POLYCRYSTALLINE SILICON RESIDENTIAL ARRAY OUTPUT

POLYCRYSTALLINE SILICON RESIDENTIAL ARRAY COMPUTER MODEL
WITH PHOTOCURRENT DISTRIBUTION OF $\pm 10\%$

```

1      * PSI RESIDENTIAL ARRAY
2      LIBRARY
3          PU PSI01 11
4              M 1.271214
5              P 2.359949
6              ALPHA 1.05484E4
7              CT .00061
8              G 85.1
9              IP 2.13E3
10             IS 7.45E4
11             RS 4.72E-6
12         D BPD1 1
13             RB 1E-4
14             IS 8.24E-6
15             TH 20.
16     DEFINE MODULE POS NEG 0
17         PVA1 POS 1 S T P1 PSI01 0,0,0,0,1,S10P4
18         PVA2 1 2 S T P2 PSI01 0,0,0,0,1,S10P4
19         PVA3 2 3 S T P3 PSI01 0,0,0,0,1,S10P4
20         PVA4 3 NEG S T P4 PSI01 0,0,0,0,1,S10P4
21         D1BP 1 POS BPD1
22         D2BP 2 1 BPD1
23         D3BP 3 2 BPD1
24         D4BP NEG 3 BPD1
25         VIS S 0 1.0
26         VIT T 0 298
27     DEFINE SUBARRAY A 2 0
28         MODULE1 A 1 0
29         MODULE2 1 2 0
30         MODULE3 2 3 0
31         MODULE4 3 4 0
32         MODULE5 4 5 0
33         MODULE6 5 6 0
34         MODULE7 6 7 0
35         MODULE8 7 8 0
36         MODULE9 8 9 0
37         MODULE10 9 9 0
38     AGGREGATION1
39         IP GAUGE 1.817E3
40     SUBARRAY1 1 0 0
41     SUBARRAY2 1 0 0
42     SUBARRAY3 1 0 0
43     R1L 1 0 .08
44     STATE1
45         R1L 1E-6 1E-5 1E-4 1E-3$
46     (7) SE-3 (20) SE-3 1E-2$
47     (4) SE-2 1E-1 1 10 100
48     PRINT V(R1L) I(R1L) P(R1L)
49     PLOT I(R1L) P(R1L) VS V(R1L)
50     END

```



STAIR1
 * PSI RESIDENTIAL ARRAY
 VARIABLE
 I(R1L)(+4)
 P(R1L)(+6)

POLYCRYSTALLINE SILICON RESIDENTIAL ARRAY OUTPUT
 RESULTING FROM $\pm 10\%$ I_p DISTRIBUTION

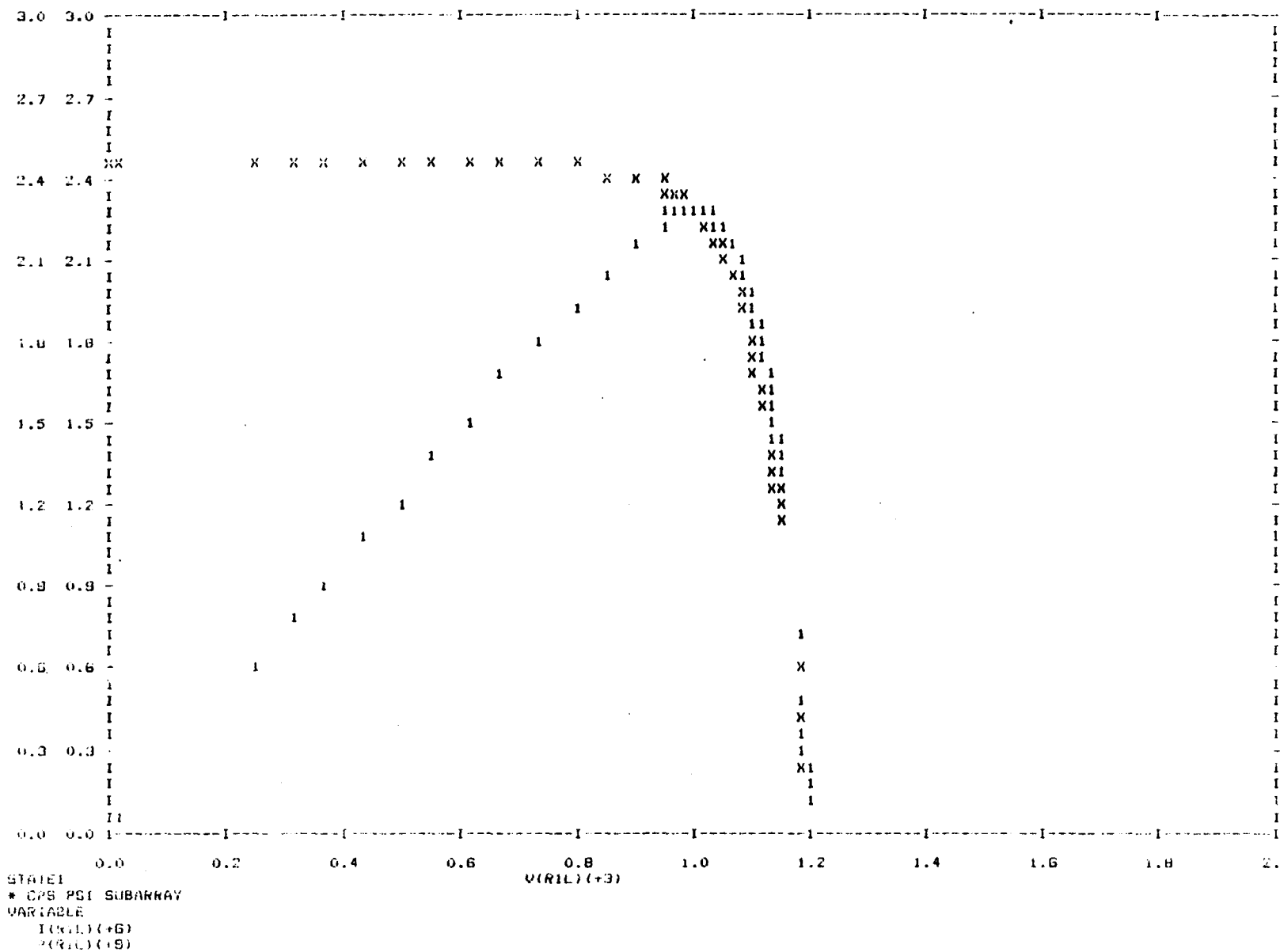
POLYCRYSTALLINE SILICONE RESIDENTIAL ARRAY OUTPUT
RESULTING FROM + 50% I_p DISTRIBUTION

POLYCRYSTALLINE SILICON CPS 2MW SUBARRAY COMPUTER MODEL

```

1      * CPS PSI SUBARRAY
2      LIBRARY
3      PU PSI01 11
4          M 1.271214
5          P 2.355548
6          ALPHA 1.05484E4
7          CT .00061
8          G 91.5
9          IP 2.29E3
10         IS 8.01E4
11         RS 4.35E-6
12     D BPD1 1
13         RB 1E-4
14         IS 8.24E-5
15         TH 20.
16
17     DEFINE MODULE POS NEG 0
18     PVA1 POS 1 S T P1 PSI01 0.0,0.0,0.0,S10P3
19     PVA2 1 2 S T P2 PSI01 0.0,0.0,0.0,S10P3
20     PVA3 2 3 S T P3 PSI01 0.0,0.0,0.0,S10P3
21     PVA4 3 4 S T P4 PSI01 0.0,0.0,0.0,S10P3
22     PVA5 4 5 S T P5 PSI01 0.0,0.0,0.0,S10P3
23     PVA6 5 6 S T P6 PSI01 0.0,0.0,0.0,S10P3
24     PVA7 6 7 S T P7 PSI01 0.0,0.0,0.0,S10P3
25     PVA8 7 8 S T P8 PSI01 0.0,0.0,0.0,S10P3
26     PVA9 8 9 S T P9 PSI01 0.0,0.0,0.0,S10P3
27     PVA10 9 NEG S T P10 PSI01 0.0,0.0,0.0,S10P3
28     D1BP 1 POS BPD1
29     D2BP 2 1 BPD1
30     D3BP 3 2 BPD1
31     D4BP 4 3 BPD1
32     D5BP 5 4 BPD1
33     D6BP 6 5 BPD1
34     D7BP 7 6 BPD1
35     D8BP 8 7 BPD1
36     D9BP 9 8 BPD1
37     D10BP NEG 9 BPD1
38     V1S S 0 1.0
39     V1T T 0 298
40     DEFINE SUB A B 0
41     MODULE1 A 1 0
42     MODULE2 1 2 0
43     MODULE3 2 3 0
44     MODULE4 3 4 0
45     MODULE5 4 5 0
46     MODULE6 5 6 0
47     MODULE7 6 7 0
48     MODULE8 7 8 0
49     MODULE9 8 9 0
50     MODULE10 9 10 0
51     MODULE11 10 11 0
52     MODULE12 11 12 0
53     MODULE13 12 13 0
54     MODULE14 13 14 0
55     MODULE15 14 15 0
56     MODULE16 15 16 0
57     MODULE17 16 17 0
58     MODULE18 17 18 0
59     MODULE19 18 19 0
60     MODULE20 19 20 0
61     SUB1 (362) 1 0 0
62     R1L 1 0 .08
63     STATE1
64     R1L 1E-5 1E-5 1E-4 (12) 4E-4 (20) 5E-4
65     (20) 1E-3 (9) 1E-2 1E-1 1 10 100
66     PRINT V(R1L) I(R1L) P(R1L)

```

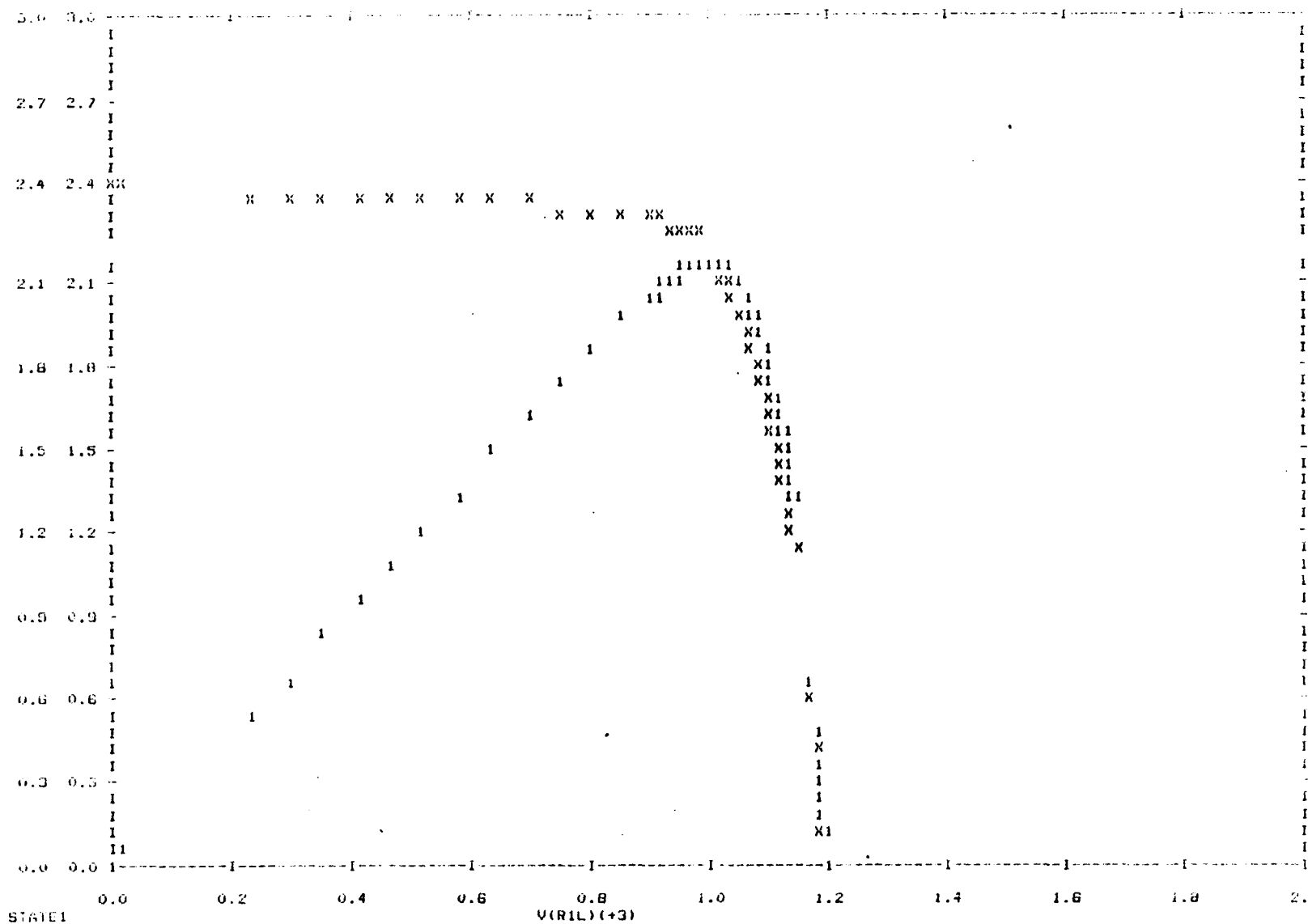


POLYCRYSTALLINE SILICON CPS 2MW SUBARRAY COMPUTER MODEL WITH
PHOTOCURRENT DISTRIBUTION OF $\pm 10\%$

```

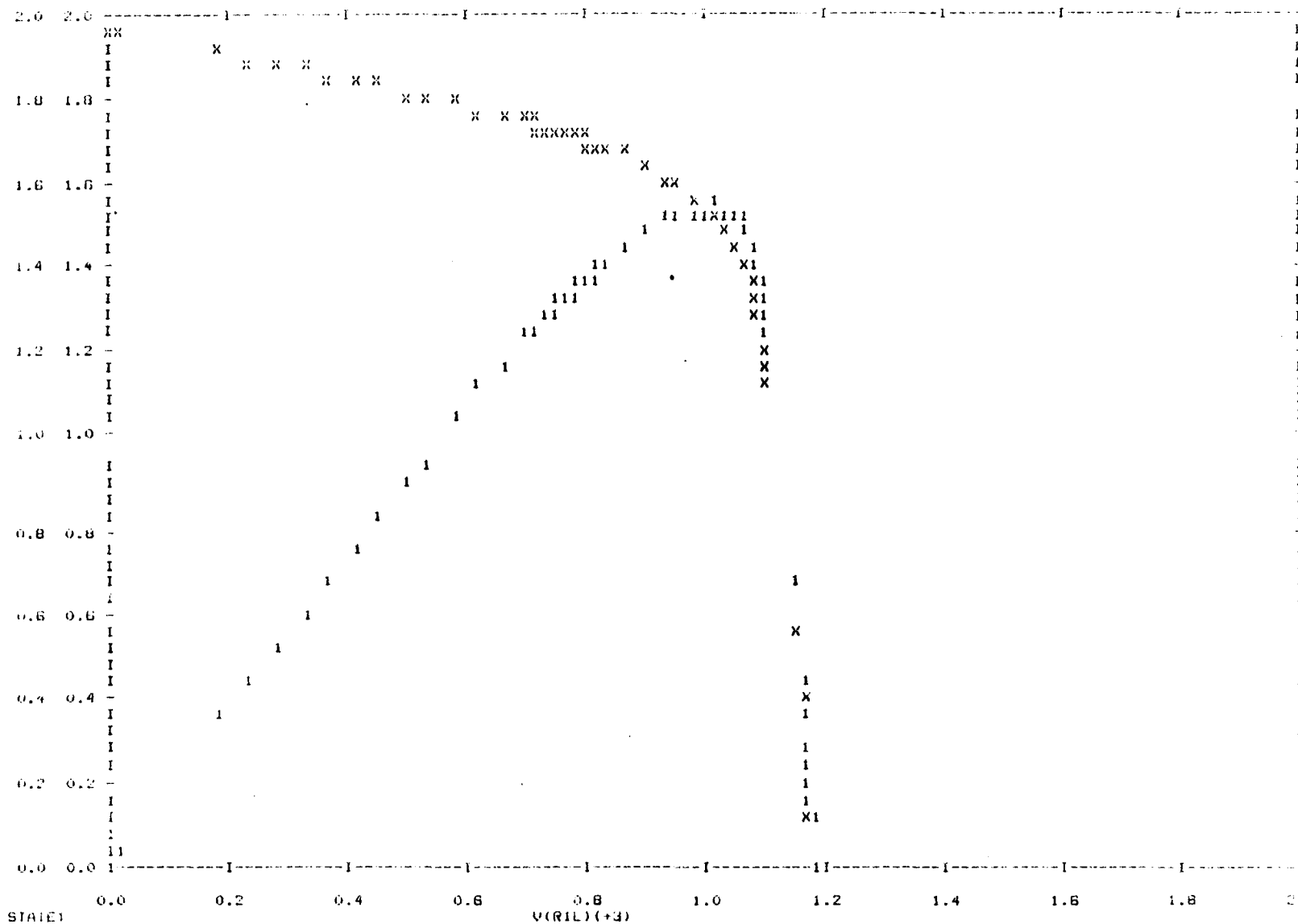
1      * CPS PSI SUBARRAY
2      LIBRARY
3      PJ PSI01 11
4          W 1.271214
5          P 2.359949
6          ALPHA 1.054645
7          CT 1.00061
8          G 91.5
9          IP 2.29E3
10         IS 8.01E4
11         RS 4.39E-6
12     D BPD1 1
13         RB 1E-4
14         IS 8.24E-6
15         TH 20.
16     DEFINE MODULE POS NEG 0
17     PVA1 POS 1 S T P1 PSI01 0.0.0.0.1,S10P3
18     PVA2 1 2 S T P2 PSI01 0.0.0.0.1,S10P3
19     PVA3 2 3 S T P3 PSI01 0.0.0.0.1,S10P3
20     PVA4 3 4 S T P4 PSI01 0.0.0.0.1,S10P3
21     PVA5 4 5 S T P5 PSI01 0.0.0.0.1,S10P3
22     PVA6 5 6 S T P6 PSI01 0.0.0.0.1,S10P3
23     PVA7 6 7 S T P7 PSI01 0.0.0.0.1,S10P3
24     PVA8 7 8 S T P8 PSI01 0.0.0.0.1,S10P3
25     PVA9 8 9 S T P9 PSI01 0.0.0.0.1,S10P3
26     PVA10 9 NEG S T P10 PSI01 0.0.0.0.1,S10P3
27     D18P 1 POS BPD1
28     D28P 2 1 BPD1
29     D38P 3 2 BPD1
30     D48P 4 3 BPD1
31     D58P 5 4 BPD1
32     D68P 6 5 BPD1
33     D78P 7 6 BPD1
34     D88P 8 7 BPD1
35     D98P 9 8 BPD1
36     D108P NEG 9 BPD1
37     VIS 3 0 1.0
38     VIT 0 288
39     DEFINE SUB A B 0
40     MODULE1 A 1 0
41     MODULE2 1 2 0
42     MODULE3 2 3 0
43     MODULE4 3 4 0
44     MODULE5 4 5 0
45     MODULE6 5 6 0
46     MODULE7 6 7 0
47     MODULE8 7 8 0
48     MODULE9 8 9 0
49     MODULE10 9 10 0
50     MODULE11 10 11 0
51     MODULE12 11 12 0
52     MODULE13 12 13 0
53     MODULE14 13 14 0
54     MODULE15 14 15 0
55     MODULE16 15 16 0
56     MODULE17 16 17 0
57     MODULE18 17 18 0
58     MODULE19 18 19 0
59     MODULE20 19 20 0
60     AGGREGATION1
61     IP GAUSS 2.06E3
62     SUB1 (362) 1 0 0
63     R1L 1 0 .08
64     STATE1
65     R1L 1E-6 1E-5 1E-4 (12) 4E-4 (20) 5E-4$
66     (20) 1E-3 (9) 1E-2 1E-1 1 10 100
67     PRINT U(R1L) I(R1L) P(R1L)
68     PLOT I(R1L) P(R1L) VS U(R1L)
69     END

```

STATE1
* CPS PSI SUBARRAY
VARIABLE
I(R1L)(+6)
P(R1L)(+9)

POLYCRYSTALLINE SILICON CPS 2 MW SUBARRAY OUTPUT RESULTING
FORM $\pm$ 10% 1p DISTRIBUTION



STATE1
 * CPS PSI SUBARRAY
 VARIABLE
 V(RIL)(+6)
 V(RIL)(+2)

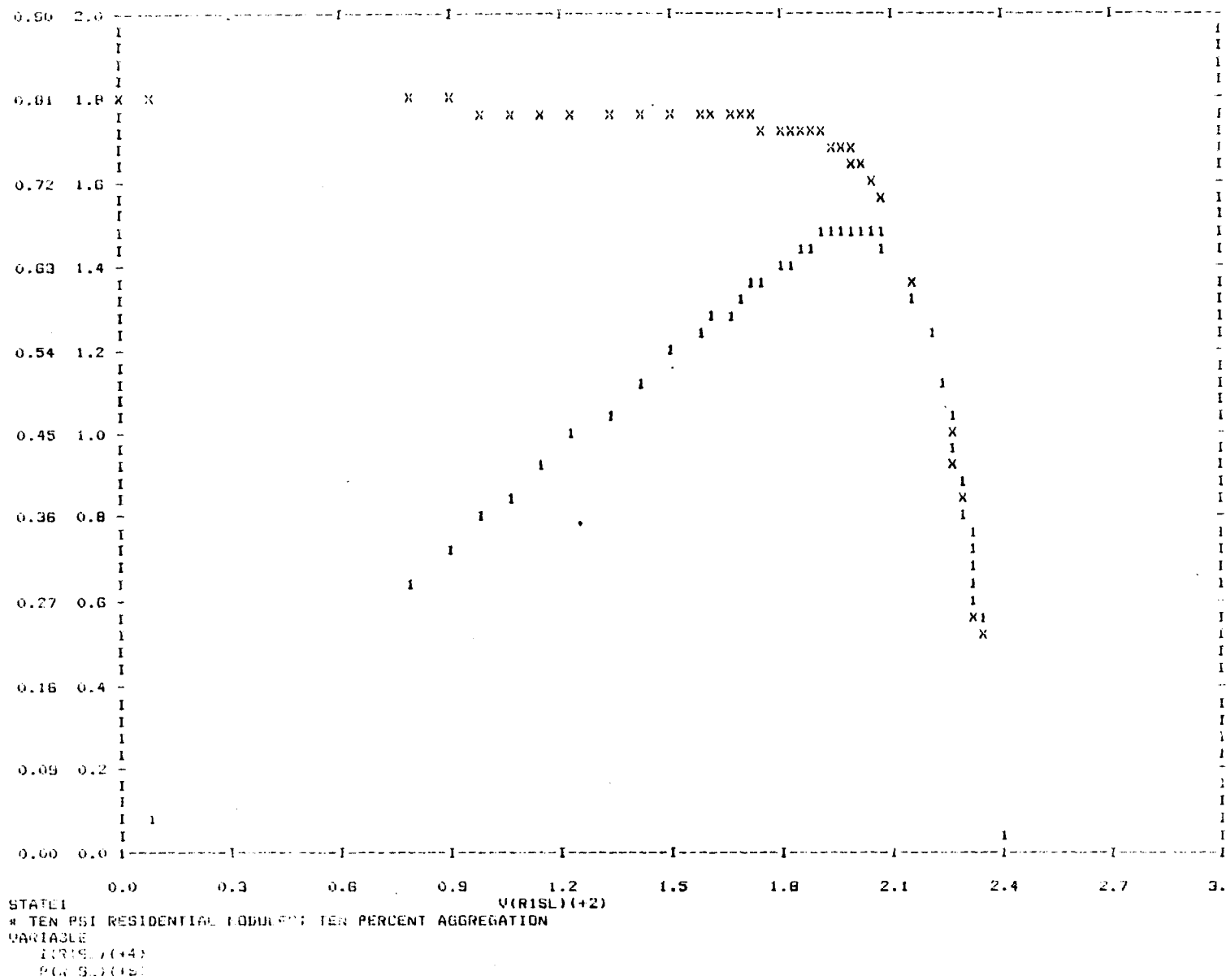
POLYCRYSTALLINE SILICON CPS 2 MW SUBARRAY OUTPUT RESULTING
 FROM $\pm 50\%$ I_p DISTRIBUTION

POLYCRYSTALLINE SILICON RESIDENTIAL SERIES STRING LISTING FOR
+ 10% DISTRIBUTION ASSESSMENT

```

1      * TEN PSI RESIDENTIAL MODULES; TEN PERCENT AGGREGATION
2      LIBRARY
3          PV PSI01 11
4              M 1.271214
5              P 2.359949
6              ALPHA 1.05484E4
7              CT .00061
8              G 85.1
9              IP 2.13E3
10             IS 7.45E4
11             RS 4.72E-6
12             D BPD1 1
13                 RB 1E-4
14                 IS 8.24E-6
15                 TH 20.
16     AGGREGATION1
17         IP GAUSS 1.917E3
18     DEFINE MODULE POS NEG 0
19         PVA1 POS 1 S T P1 PSI01 0,0,0,0,1,S10P4
20         PVA2 1 2 S T P2 PSI01 0,0,0,0,1,S10P4
21         PVA3 2 3 S T P3 PSI01 0,0,0,0,1,S10P4
22         PVA4 3 NEG S T P4 PSI01 0,0,0,0,1,S10P4
23         D1BP 1 POS BPD1
24         D2BP 2 1 BPD1
25         D3BP 3 2 BPD1
26         D4BP NEG 3 BPD1
27         VIS S 0 1.0
28         VIT T 0 298
29     MODULE1 A 1 0
30     MODULE2 1 2 0
31     MODULE3 2 3 0
32     MODULE4 3 4 0
33     MODULE5 4 5 0
34     MODULE6 5 6 0
35     MODULE7 6 7 0
36     MODULE8 7 8 0
37     MODULE9 8 9 0
38     MODULE10 9 8 0
39     R1L A 1 P1
40     R2L 1 2 P1
41     R3L 2 3 P1
42     R4L 3 4 P1
43     R5L 4 5 P1
44     R6L 5 6 P1
45     R7L 6 7 P1
46     R8L 7 8 P1
47     R9L 8 9 P1
48     R10L 9 8 P1
49     R1SL A B .08
50     P1 100
51     STATE1
52         R1SL 1E-6 1E-5 1E-4 1E-3%
52     1E-2 (9) 2E-2 (20) 3E-2 (14) 1E-1 1 10 100
53     PRINT V(R1SL) I(R1SL) P(R1SL)
54     PLOT I(R1SL) P(R1SL) VS V(R1SL)
55     STATE2
56         P1 1E-6
57         PRINT I(R1L) I(R2L) I(R3L) I(R4L) I(R5L)
58         PRINT I(R6L) I(R7L) I(R8L) I(R9L) I(R10L)
59     END

```



POLYCRYSTALLINE SILICON RESIDENTIAL SERIES STRING OUTPUT
FOR + 10% DISTRIBUTION ASSESSMENT

LISTING OF SHORT CIRCUIT CURRENTS OF 10 MODULES FOR $\pm 10\%$
DISTRIBUTION ASSESSMENT

1NET-2

* TEN PSI RESIDENTIAL MODULES; TEN PERCENT AGGREGATION

STATE2

1 TIME
2 I(R1L)
3 I(R2L)
4 I(R3L)
5 I(R4L)
6 I(R5L)

	1	2	3	4	5	6
0	0.00000+00	8.16986+03	8.14803+03	8.09034+03	8.11287+03	8.16133+03

0
1NET-2

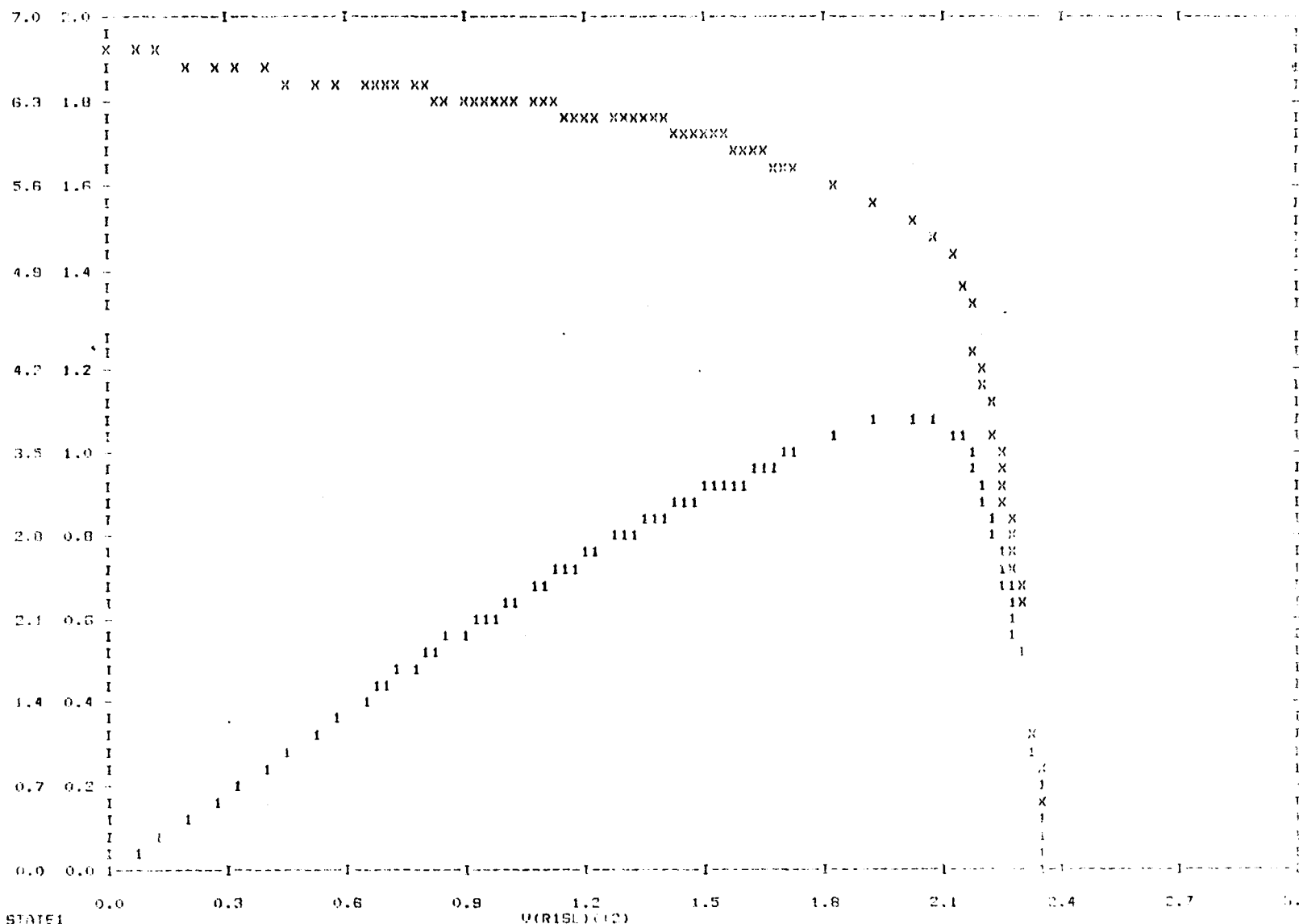
* TEN PSI RESIDENTIAL MODULES; TEN PERCENT AGGREGATION

STATE2

1 TIME
2 I(R6L)
3 I(R7L)
4 I(R8L)
5 I(R9L)
6 I(R10L)

	1	2	3	4	5	6
0	0.00000+00	8.11292+03	8.12279+03	8.14480+03	8.11097+03	8.07897+03

0



STATE1

* TEN PSI MODULES; FIFTY PERCENT AGGREGATION

VARIABLE

I(RISL) (°)

P(RISL) (°)

POLYCRYSTALLINE SILICON RESIDENTIAL SERIES STRING OUTPUT
FOR + 50% DISTRIBUTION ASSESSMENT

OUTPUT LISTING OF SHORT CIRCUIT CURRENTS OF 10 MODULES FOR
± 50% DISTRIBUTION ASSESSMENT

1NET-2

* TEN PSI MODULES; FIFTY PERCENT AGGREGATION

STATE2

1 TIME
 2 I(R1L)
 3 I(R2L)
 4 I(R3L)
 5 I(R4L)
 6 I(R5L)

	1	2	3	4	5	6
0	0.00000+00	7.00258+03	6.81951+03	6.56542+03	6.64696+03	6.84258+03

0

1NET-2

* TEN PSI MODULES; FIFTY PERCENT AGGREGATION

STATE2

1 TIME
 2 I(R6L)
 3 I(R7L)
 4 I(R8L)
 5 I(R9L)
 6 I(R10L)

	1	2	3	4	5	6
0	0.00000+00	6.73636+03	6.76356+03	6.94388+03	6.54788+03	6.42214+03

0

293/294



APPENDIX B

MODULE OPTIMIZATION METHODOLOGY FOR
ADVANCED PV CELLS AND DEVICES



APPENDIX B

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SECTION 1.0 EXECUTIVE SUMMARY

1.1 METHODOLOGY OBJECTIVES

The Module Optimization Methodology has been developed to assist designers and analysts of modules using advanced photovoltaic (PV) cells in obtaining optimum module designs and in evaluating the performance and cost of alternate module designs. The methodology is generic in nature and applicable to most advanced PV cell and device configurations. It provides a basis for designing modules and for performing comparative and trade-off studies for performance and cost.

The methodology can be used as a design or analysis tool for a given technology process to determine:

- Cell arrangement and electrical interconnections within a module
- Module or cell size to obtain maximum packing density
- Conductor cross-sectional area requirements within the module
- Effects of varying cell parameters or module design constraints (electrical or physical)
- Temperature of cell or any other material in the module lamination stack-up for center or edge cells
- Adequacy of structural design for uniform loads, twisting loads and hail impact
- Effects of lamination design variations on thermal or structural characteristics
- Effective cost of the module in dollars per peak watt for a specific process
- Effects of module manufacturing process variations on module cost.

The methodology has been developed for manual use and has also been implemented into a computer code on the SERI CDC 7600 computer. This document presents the basis for the methodology, explanations of the equations used, flowcharts of the methodology algorithms with explanations for their step-by-step use, and examples of the manual and computerized use of the algorithms. In addition to this executive summary, this report is divided into five sections corresponding to the four major methodologies: electrical, thermal, structural, and economic; and to the computerized algorithm user's instructions. The conductor requirements methodology is incorporated into the electrical section. The examples contained in each section of the manual use of the algorithm have been run using the computerized version to verify the operation of the code. These results are contained in section 6.3. Test cases have been run to exercise all elements of the code. These cases are contained in section 6.4. A glossary of terms has been included at the end of each section to assist the user in understanding the individual algorithms.

1.2 OVERVIEW OF METHODOLOGY

The Module Optimization Methodology incorporates four disciplines: electrical, thermal, structural, and economic. An overview of the methodology with interactions between disciplines is included in figure 1-1. The methodologies assume that the user possesses a predefined cell technology such that the cell production process and cell characteristics (electrical, thermal, and structural) are known. Thus, for example, material resistivities, tensile strengths, and thermal conductivities are known, as are the cell metallization grid pattern and substrate characteristics. The methodology does not optimize cell processes such as cell thickness, doping, grid pattern, or deposition rate except as may be implied from the module performance or cost results. The methodology does optimize cell dimensions and module material dimensions and thicknesses, such as glass thickness or conductor width.

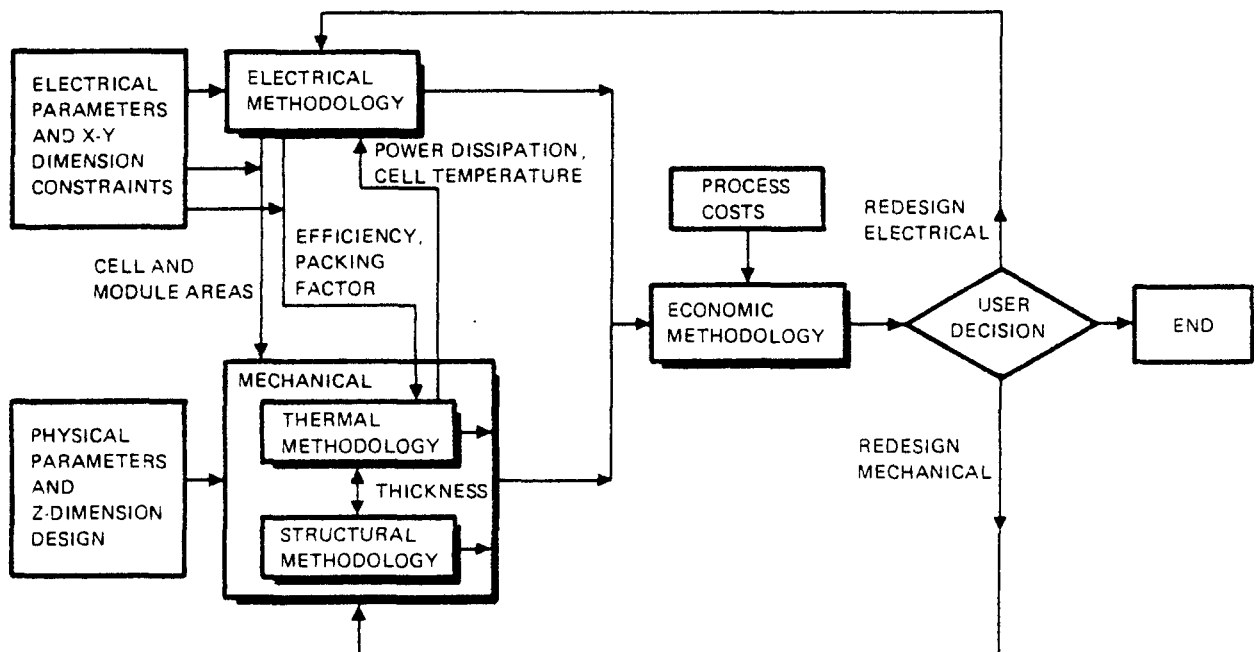


Figure 1-1. Overview of Module Optimization Methodology

The electrical and mechanical methodologies are essentially independent and produce designs in orthogonal directions. That is, the electrical methodology determines the cell dimensions, arrangement of cells and the interconnections in the x-y plane within the module. The mechanical methodologies determine module z-dimension (or lamination stack-up) design and material thicknesses. The exception is the electrical conductor thickness, which is determined by the electrical methodology, but it must conform in the end to thermal and structural constraints.

The electrical methodology uses cell electrical parameters and module x-y dimensional constraints. It may use cell temperature and power dissipation from the thermal methodology or it may postulate a typical cell temperature and calculate power dissipation from typical parameters. The mechanical methodologies use physical characteristics from a postulated z-dimension (or lamination stack-up) design to analyze the thermal or structural

characteristics and adjust the design if needed. The z-dimension lamination stack may be designed by the user or may be partially specified by the cell process - for example, deposition on a glass superstrate. The only x-y constraints required are cell and module areas, packing factor and cell efficiency, which may be obtained from the electrical methodology or may be postulated constraints independent of the electrical design. For example, the module dimensions and cell efficiency may be fixed constraints while a typical packing factor may be assumed. The thermal and structural methodologies are both concerned with material thicknesses and therefore design changes required by one methodology may impact the other's analysis.

The economic methodology is dependent upon the module design obtained from the other methodologies in that material sizes, thicknesses, and quantities will effect the module cost. The economic methodology also incorporates cell and module process costs such as labor, equipment, and facilities.

The electrical methodology is basically formulated as a design tool but may also be used to analyze existing designs and perform tradeoffs on design parameters and constraints. The other methodologies are basically analysis tools in that they start with a potential design. The design, however, may be revised, based on the results of these analyses. The decision, whether or not to revise the module design (either the x-y plane or lamination design) and what to change, is made by the user, based on module performance and costs with an understanding of the production processes involved and use of the module methodologies.

1.3 ELECTRICAL METHODOLOGY OVERVIEW

The electrical methodology was developed to assist the module designer or analyst in determining the optimum physical layout and electrical connection of cells within a module for a given cell technology and application.

The primary objective of the methodology is to produce a module with a specific voltage at peak power, V_{MPM} and reverse bias protection using bypass diodes. Other design objectives such as desired module dimensions or cell area are considered secondary.

The electrical methodology is fully described in section 2.0. The equations used in the methodology are summarized in section 2.1.3. The algorithms are described in detail in section 2.2 through the use of flow charts. An example of the manual use of the algorithm to design a residential polycrystalline module is presented in section 2.3. Section 2.0 concludes with a glossary of terms.

An overview of the electrical methodology algorithm and key features are shown in figure 1-2. The design starts with the cell J-V curve (current density versus voltage). Although efficiency may vary with cell area, the J-V curve is obtained from characteristics at the approximate or maximum cell area anticipated. The parameters thus obtained from this standardized curve can be easily scaled once the final cell area is determined.

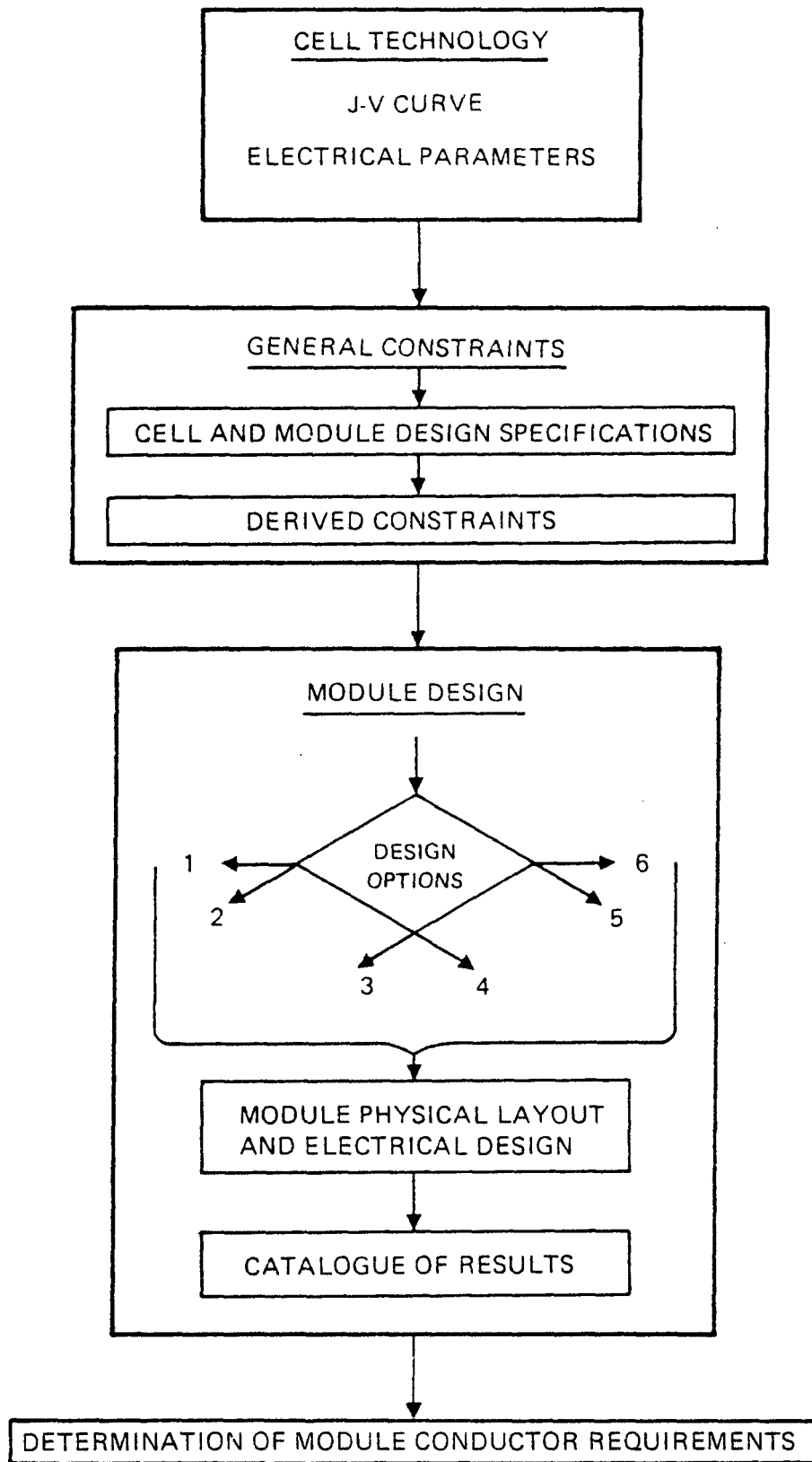


Figure 1-2. Overview of Electrical Methodology

The methodology proceeds, as shown in figure 1-2 under general constraints with the user providing additional cell specifications such as maximum allowable cell temperature and cell reverse breakdown voltage, and module design specifications such as peak power voltage and maximum open circuit voltage for use as design constraints. Module design constraints are also specified and used with cell specifications to derive additional module constraints which will be used in one of six design options to determine the actual cell interconnects and layout.

In the module design section the design options are specified in terms of cell and module dimensional constraints. The options are numbered, as in table 1-1, in order of decreasing packing fraction which would normally be obtained from each option. Thus, in most cases, designing a module with maximum cell area and maximum module dimension constraints will produce a design with higher packing fraction than specifying fixed cell dimensions and maximum module dimensions. Although additional constraint combinations could be postulated, they would tend to produce low packing fractions, or would be contradictory or contain too many variables.

TABLE 1-1. MODULE DESIGN OPTIONS

In Order of Decreasing Packing Fraction, Given:

- 1) Maximum Cell Area and Maximum Module Dimensions
- 2) Number and Dimensions of Cells
- 3) Fixed Cell and Maximum Module Dimensions
- 4) Maximum Cell Width and Area and Fixed Module Dimensions
- 5) Maximum Cell Area and Fixed Module Dimensions
- 6) Maximum Cell Dimensions and Fixed Module Dimensions

Although the various module design option algorithms perform different calculations, they all result in a module design in which the physical layout of the cells in the module, the actual cell and module dimensions, the series and parallel interconnections, and the module conductor requirements are specified. The bypass group design (N_{bp}) and number of bypass groups in series

(N_G) may also be modified in the process. The results of the design process, including all physical and electrical characteristics, are listed at the end of the design process.

1.4 THERMAL METHODOLOGY OVERVIEW

The thermal optimization methodology describes the method for calculating the temperature distribution through the module laminates for flat plate and concentrator geometries. The thermal methodology is described in detail in section 3.0. The algorithms are described in detail through the use of flowcharts in section 3.5. An example of the manual use of the algorithm to calculate the conductances and temperatures in a flat plate PV module is contained in section 3.7. Section 3.0 concludes with a glossary of terms used in the thermal algorithm.

The primary purpose of this algorithm is to determine the PV cell operating temperatures under user defined conditions. Module performance is then calculated based on this cell temperature which is input into the electrical algorithm. In addition, the danger of chemical degradation can be determined from the encapsulant temperature, and thermal stresses can be determined from the temperature distribution through the module.

A one-dimensional steady state situation is assumed and a thermal/electrical circuit analogy is used to calculate the temperature distribution. The typical thermal cell is shown in figure 1-3 where the temperature is calculated at nodes 1 through 5 for a cell in the center of the module, and at all 6 nodes for a cell located at the edge of a module.

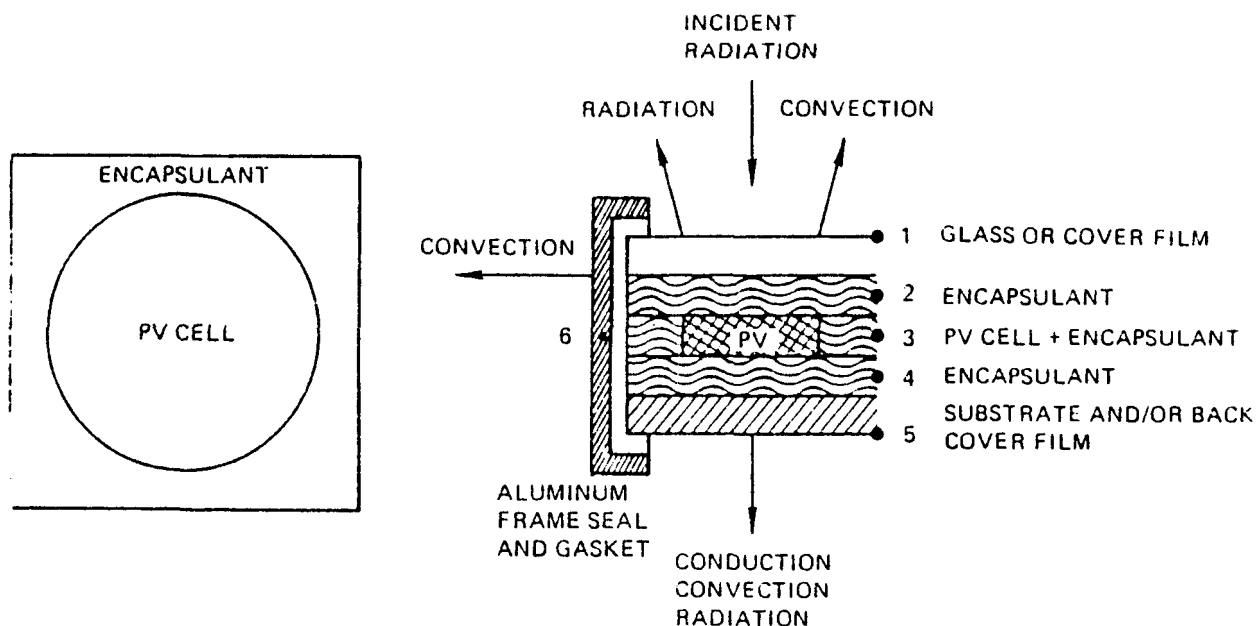
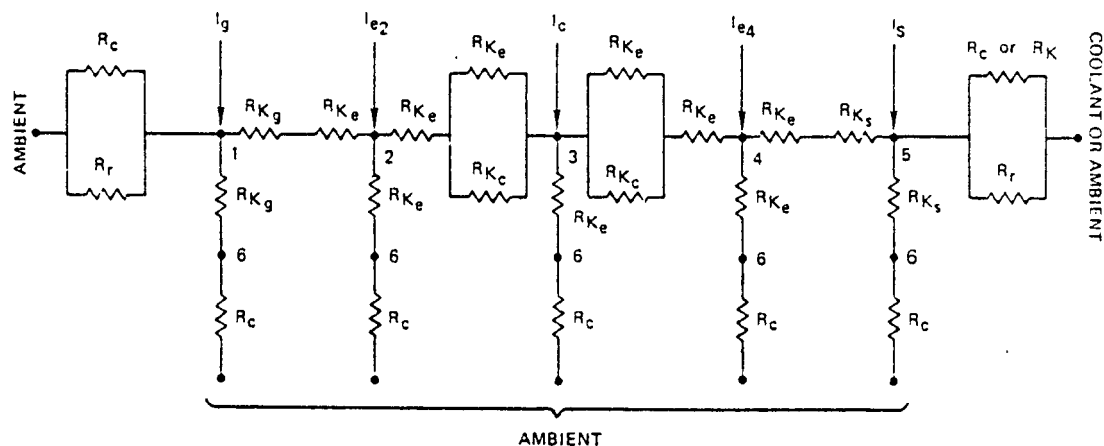


Figure 1-3. Typical Thermal Cell

The PV cell may be defined by the user as square, rectangular or circular, but the thermal cell must be square or rectangular. As shown in figure 1-3 the thermal cell may consist of a cover film, top encapsulant, PV cell, bottom encapsulant or adhesive, and substrate. The frame consists of a seal, gasket, and metal frame. The user may select any of these materials to form a module.

The thermal circuit is shown in figure 1-4. Here, the thermal resistances are denoted by R where the subscripts define the type of resistance as follows: K-conduction, c-convection, r-radiation. The energy input due to insolation absorbed at each module is analogous to current, and the temperatures at each node are analogous to voltage. In this analysis the ambient and coolant temperatures are assumed known as is the insolation incident on the module.

Various geometries may be selected by the designer, including flat plate and concentrating geometries. For a flat plate geometry, the user may assume a fully insulated (adiabatic) back to simulate a module mounted directly to the roof, or a cooled back. The cooled back option may be either air cooled (with or without fins) or forced liquid cooled. The concentrating geometries consist of point focus and linear Fresnel systems passively or actively cooled, or an actively cooled parabolic trough system.



INCIDENT INSOLATION ON THE FOLLOWING LAYERS:

I_g : GLASS
 I_{e2} : TOP LAYER OF ENCAPSULANT
 I_c : PV CELL
 I_{e4} : BOTTOM LAYER OF ENCAPSULANT
 I_s : SUBSTRATE

THERMAL RESISTANCES:

R_c : CONVECTIVE
 R_r : RADIATIVE
 R_K : CONDUCTIVE TROUGH
 R_{Kg} : GLASS
 R_{Ke} : ENCAPSULANT
 R_{Kc} : PV CELL
 R_{Ks} : SUBSTRATE

Figure 1-4. Thermal Circuit

1.5 STRUCTURAL METHODOLOGY OVERVIEW

The purpose of the structural methodology is to analytically predict the survivability of the module under extreme environmental conditions. The effect of external loads is determined which includes uniform loads, twisting loads due to installation and handling misalignment, and hail impact loading. The structural analysis methodology is discussed fully in section 4.0. An example of the manual use of the algorithm is shown in section 4.3.3. The flowcharted algorithm is contained in section 4.7. Section 4.0 concludes with a glossary of terms.

An analysis of the total uniform load on a flat plate module would consist of the module deadweight, snow load, earthquake loads, and time varying wind loads (cyclic pressure loading). The JPL Block V standards indicate that a flat plate module must be able to withstand a mechanical cycling load of ± 50 pounds per square foot for 10,000 cycles as indicated in figure 1-5. This loading is intended to simulate a cyclic wind load. Thus, the structural analysis of a flat plate module is based only on deadweight loading due to the weight of the module and the JPL Block V wind loading requirements. Earthquake and snow loads are site dependent and are not considered here.

- CASES: 1) SIMPLY SUPPORTED PLATES ON ALL EDGES
2) STRUCTURE TYPES: a) GLASS SUPERSTRATE
b) METAL SUBSTRATE

GUIDELINES: MECHANICAL CYCLIC LOADING — JPL SECTION V:
 ± 50 psf UNIFORM LOAD FOR 10,000 CYCLES

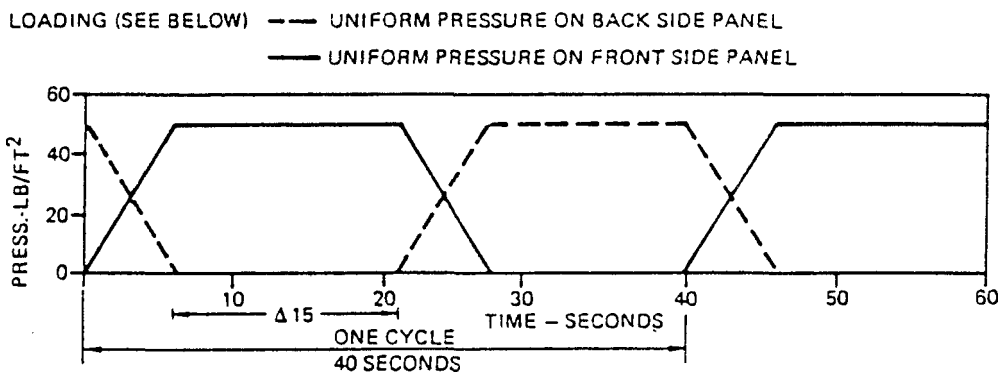


Figure 1-5. Block V Load Standards

The flat plate analysis assume simply supported plates. Analysis of receiver sections for concentrating collectors assumes the sections can be approximated by supported beams which produces a conservative estimate of the stresses in the receiver section due to bending movements and shear. It will be assumed that the receiver section will see only the static load due to the weight of the receiver and cooling fluid.

The methodology performs a simplified structural analysis of a module where the main load bearing members are assumed to bear all of the pressure loads. Thus, for a superstrate design all the pressure load is borne by the glass, and for a substrate design all the pressure load is assumed to be borne by the metal or wood product substrate.

1.6 ECONOMIC METHODOLOGY

The economic methodology incorporated into the module optimization methodology is based upon Improved Price Estimation Guidelines (IPEG) developed by the Jet Propulsion Laboratory (JPL)^[1]. The electrical, structural, and thermal algorithms produce an optimized module with respect to electrical and mechanical configurations. The economics algorithm permits a cost trade-off analysis between alternative configurations for a specific process. The user must input projected cost elements for each process in a manufacturing sequence. Standardized typical item costs are published in the SAMICS Cost Account Catalog (JPL Document 5101-154, April 1980).

The IPEG is a standardized methodology for estimating manufacturing costs. Manufacturing is viewed as a sequence of identifiable production processes. Individual cost elements for each manufacturing process are burdened to incorporate overhead costs. The total process cost is inflated to adjust for subsequent process yield efficiencies. All output costs are expressed in \$/Wp to permit intertechnology and intratechnology comparison. Section 5.2 explains the costing methodology in detail. Section 5.3 develops an FOB cost/Wp for a specific technology as an example of the costing algorithm.

The module optimization costing algorithm projects PV module cost as an estimated \$/M². An adjustment is made to compensate for the effective PV surface of a module. The total cost of the module is multiplied by the inverse of cell packing density. Multiplying the adjusted cost by the inverse of the product of AMI insolation and cell efficiency converts the module cost to \$/Wp.

1.7 PHOTOVOLTAIC MODULE OPTIMIZATION CODE

The algorithms and analysis methodologies contained in this report have been incorporated into a computer program called Photovoltaic Module Optimization Code (PVMOC). The PVMOC program greatly enhances the speed at which individual analysis may be performed. The PVMOC program is operational on the SERI CDC-720 computer in either the batch or interactive operating systems. Complete instructions for using the PVMOC program are contained in section 6.0 including examples and test cases.

The PVMOC program can perform any of the types of analysis described in this report: electrical (including conductor requirements), thermal, structural, and economic. While each analysis may be run independently of other analysis types, data may be generated by one analysis and used in another. For example, a cell temperature computed by thermal analysis may be used in the electrical analysis input.

The computerized PV module optimization scheme is performed by two programs: the input processor (PVINP) and the computational code (PVMOC). The input processor is an interactive data entry aid to constructing an input file for the computational code. Upon execution, PVINP prompts the user as to what type of analysis to run, then asks for appropriate data. The responses to these questions are written to an input file that is structured to be read directly by the PVMOC computational code. The PVMOC code then performs analyses based on the user's responses to the input processor. Analysis output may be displayed on a CRT or sent to a local line printer.

SECTION 2.0 ELECTRICAL METHODOLOGY

2.1 OVERVIEW

2.1.1 Purpose and Principles of Development

The electrical methodology was developed to assist the module designer or analyst in determining the optimum physical layout and electrical connection of cells within a module for a given cell technology and application (residential, central power, etc.).

For all cases, the cell technology is represented by a J-V curve (current density versus voltage) or the key electrical parameters, V_{OCC} , J_{SCC} , V_{MPC} and J_{MPC} (open circuit cell voltage, short circuit current density and voltage and current density at the maximum power point, respectively). The cell production process has been previously defined and the cell characteristics such as material resistivities and thicknesses, metallization grid patterns, and breakdown voltage do not vary. The cell characteristics which are determined in the module design are the cell dimensions. It is assumed that the manufacturer is capable of producing optimum metallization grid patterns on the cell for any cell dimensions that might be obtained. Cell efficiency is held constant during the calculations. If the cell dimensions obtained are smaller than expected, permitting a higher efficiency, the user may repeat the methodology with an updated efficiency.

The primary objective of the methodology is to produce a module with specific peak power voltage, V_{MPM} , and reverse bias protection of cells using bypass diodes. Other design objectives such as desired module dimensions or cell area are considered secondary. The flow charted algorithms and computer code are designed to satisfy this objective. The algorithm can be easily altered, however, to satisfy other objectives when using the methodology in hand analysis.

The methodology and the code are segmented so that the procedures can be easily understood and followed. The experienced user will be able to use individual segments of the methodology and code to study particular design features and make tradeoffs.

2.1.2 Overview of Methodology

An overview of the methodology algorithm and key features are presented in this section. The equations used in the methodology are summarized in section 2.1.3. The algorithms are described in detail in section 2.2 through the use of flow charts. A module design example is detailed in section 2.3. Section 2.4 contains a glossary of terminology for the electrical methodology.

As indicated in figure 2-1, the design starts with the cell J-V curve. Although efficiency may vary with cell area, the J-V curve is obtained from characteristics at the approximate or maximum cell area anticipated. The

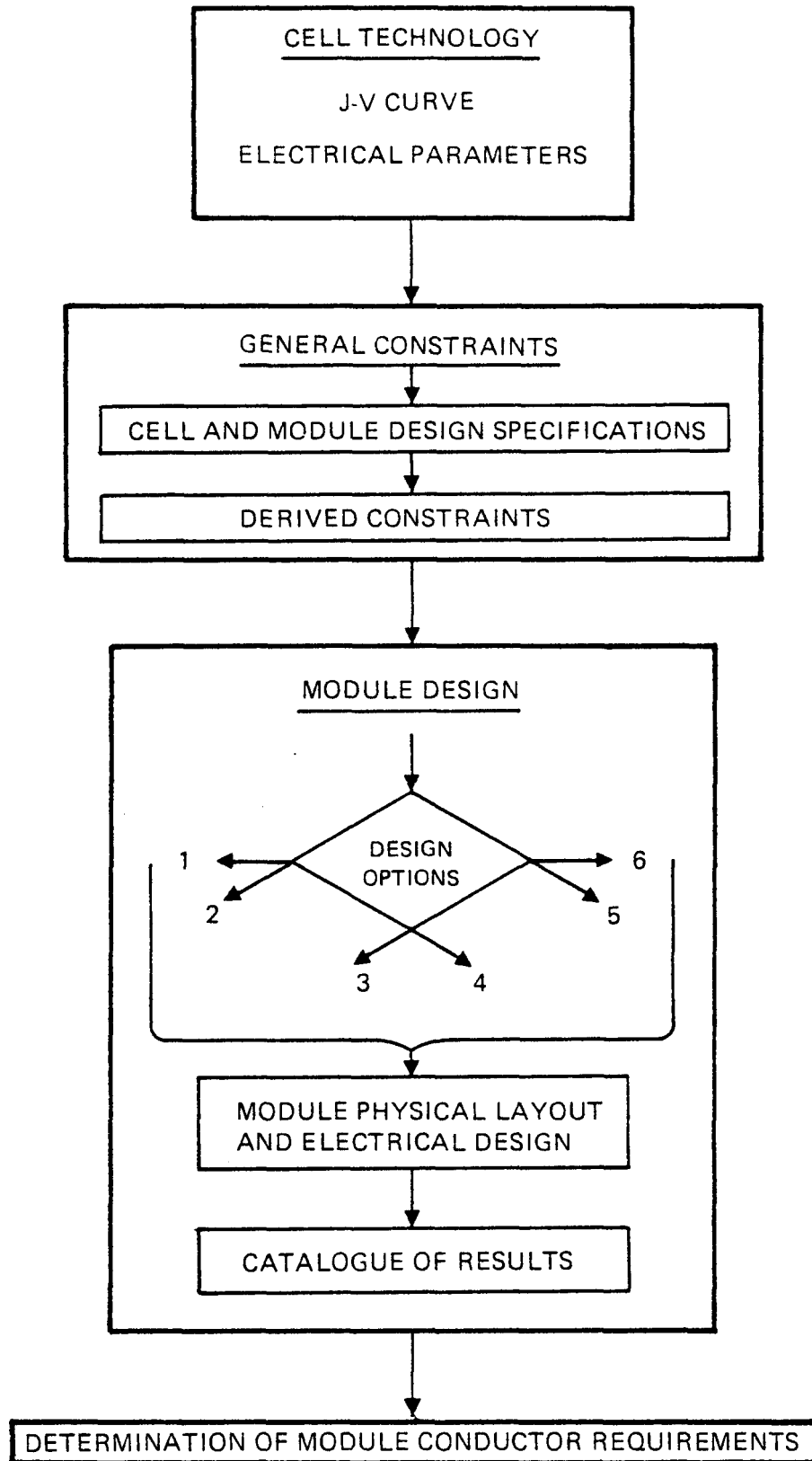


Figure 2-1. Overview of Electrical Methodology

parameters thus obtained from this standardized curve can be easily scaled once the final cell area is determined.

The methodology proceeds, as shown in the second box, with the user providing cell specifications such as maximum allowable cell temperature and cell reverse breakdown voltage, and module design specifications such as peak power voltage and maximum open circuit voltage for use as design constraints. Additional constraints are then derived based on these initial constraints. The constraints and specifications used in this general constraint segment are listed in table 2-1.

The user specifies a series of acceptable module maximum power voltages (V_{MPM} 's). The methodology attempts to design a module to the maximum voltage specified (V_{MPMAX}) but will use a lower voltage if a design can not be obtained at the highest voltage. The module design must not exceed the maximum allowable open circuit voltage (V_{OCMAX}) for a particular application at the lowest expected cell temperature (T_L). Spacings from end cells to edges of the module (Δ_{SE} 's) and between cells (Δ_S 's) in both the series and parallel directions are specified by the user. These are usually determined from manufacturing and assembly tolerances and from frame overlapping, conductor widths, etc.

In order to determine the maximum number of cells allowable in a bypass group (N_{BPMAX}) for reverse bias protection, the user may input maximum allowable cell temperature in reverse bias (T_{CMAX}) or maximum reverse voltage allowable (V_{RMAX}) or V_{RMAX} may be calculated from T_{CMAX} and various cell parameters. The maximum number of bypass groups in series (N_{GMAX}) and the maximum number of cells in series in the module (N_{BGMAX}), which is $N_{BPMAX} \times N_{GMAX}$, are determined from V_{MPMAX} and V_{OCMAX} .

The minimum number of parallel segments required for redundancy (N_{MMIN}) addresses the case of individual cell shadowing or broken interconnects. If N_{MMIN} or more cells or bypass groups are paralleled in the module, the bypass group will not become reverse biased under these conditions but will continue to produce power, albeit at a reduced level.

Following the determination of all general constraints the methodology permits the user to design the module through any one of six options. The design options are specified in terms of cell and module dimensional constraints. The options are numbered, as in table 2-2, in order of decreasing packing fraction which would normally be obtained from each option. Thus, in most cases, designing a module with maximum cell area and maximum module dimension constraints will produce a design with higher packing fraction than specifying fixed cell dimensions and maximum module dimensions. Although additional constraint combinations could be postulated, they would tend to produce low packing fractions, or would be contradictory or contain too many variables.

Design option number 4 is a special case which considers a cell technology that is resistance limited. In this situation, one of the current carriers in the cell has a sufficiently high resistivity to produce significant power losses if the length in the direction of current is not constrained. This is characteristic of many integrated technologies and technologies in which metallization grids cannot be used. Design option 4 is described in section 2.2.4.

TABLE 2-1. GENERAL DESIGN CONSTRAINTS

Constraint and Symbol	Type*
Acceptable Module Peak Power Voltages ($V_{MPM}'s$)	S
Maximum Module Open Circuit Voltage (V_{OCMAX})	S
Lowest Cell Temperature Expected in Application (T_L)	S
Cell-to-Edge and Cell-to-Cell Spacings (Δ_{SE} and Δ_S)	S
Maximum Reverse Cell Voltage Allowable (V_{RMAX})	S/D
Maximum Cell Temperature in Reverse Bias (T_{CMAX})	S
Maximum Number of Cells in Bypass Group (N_{BPMAX})	D
Maximum Number of Bypass Groups in Series (N_{GMAX})	D
Maximum Number of Cells in Series in Module (N_{BGMAX})	D
Minimum Number of Parallel Segments Required for Redundancy (N_{MMIN})	D

*S = Value Specified

D = Value Derived

TABLE 2-2. MODULE DESIGN OPTIONS

In Order of Decreasing Packing Fraction, Given:

- 1) Maximum Cell Area and Maximum Module Dimensions
- 2) Number and Dimensions of Cells
- 3) Fixed Cell and Maximum Module Dimensions
- 4) Maximum Cell Width and Area and Fixed Module Dimensions
- 5) Maximum Cell Area and Fixed Module Dimensions
- 6) Maximum Cell Dimensions and Fixed Module Dimensions

Although the various module design option algorithms perform different calculations, they all result in a module design in which the physical layout of the cells in the module, the actual cell and module dimensions, the series and parallel interconnections, and the module conductor requirements are specified. The bypass group design (N_{BP}) and number of bypass groups in series (N_G) may also be modified in the process. The results of the design process, including all physical and electrical characteristics, are listed at the end of the design process.

Following completion of the Design Options calculations, the methodology proceeds to the Module Conductor Requirements routine to determine the conductor runs in the module.

2.1.3 Summary of Equations

In this section, the equations used in the electrical methodology are described. First, the required cell and conductor parameters are defined and the sources for obtaining them are given. Then, the equations for the general constraints are described in section 2.1.3.2 and those for the design options in section 2.1.3.3. The equations used to calculate the final cell and module electrical parameters are presented in section 2.1.3.4.

2.1.3.1 Cell and Conductor Parameters Required

The cell parameters required to be input by the user are listed in table 2-3 along with the sources for obtaining them. The J-V parameters can be input directly or the program can determine them from a set of J-V point pairs input by the user. FF_C is the cell fill factor. The temperature coefficient for open-circuit voltage ($\Delta V/\Delta T$) is used with V_{OCMAX} to determine the maximum number of cells in series from cell voltage at low temperature. It can be obtained from a voltage versus temperature curve or from J-V curves at two temperatures.

The next set of parameters are used in the determination of the maximum number of cells in a bypass group (N_{BPMAX}). They relate to cell stresses under reverse bias conditions. V_B is the lowest anticipated breakdown voltage. It can be obtained from I-V curves taken to reverse breakdown. The coefficients of temperature variation with insolation ($\Delta T/\Delta S$) and electrical power dissipation ($\Delta T/\Delta P$) can be input by the user from typical module data or can be determined in the thermal methodology.

N_{ACI} is the number of redundant interconnects on the cell. These often run across the whole cell. Breakage of a single interconnect will not produce an open circuit in a series string. The methodology uses this characteristic, for technologies in which it is applicable, to determine the minimum number of parallel segments needed for redundancy (N_{MMIN}) to prevent reverse bias of the bypass group.

For the resistance limited option, the sheet resistivity (R) of the limiting carrier and the fractional power loss allowable (P_{FL}) are needed. They can be obtained from the manufacturer. $P_{FL} = 0.05$ may typically be used. The resistivity (ρ) of the current carriers used for interconnections in the module and the fractional power loss (P_F) allowable in these conductors are needed to calculate width and thickness requirements. The resistivity can be obtained from handbooks and P_F is typically 0.01.

TABLE 2-3. REQUIRED CELL AND CONDUCTOR PARAMETERS

- J_{SCC} , V_{OCC} , J_{MPC} , V_{MPC} , FF_C
 - FROM J-V CURVE AT STANDARD INSOLATION AND SINGLE TEMPERATURE
- $\Delta V / \Delta T$ (OPEN CIRCUIT VOLTAGE TEMPERATURE COEFFICIENT)
 - FROM V-T CURVE
 - FROM J-V CURVES AT 2 TEMPERATURES
- REVERSE BIAS STRESS PARAMETERS
 - V_B (BREAKDOWN VOLTAGE)
 - FROM REVERSE I-V CURVE
 - $\Delta T / \Delta S$ (TEMPERATURE COEFFICIENT FOR INSOLATION POWER) AND
 - $\Delta T / \Delta P$ (TEMPERATURE COEFFICIENT FOR POWER DISSIPATION)
 - FROM THERMAL ANALYSIS OF LAMINATIONS
 - FROM TYPICAL MODULE DATA
- N_{ACI} (NUMBER OF ACROSS-THE-CELL OR REDUNDANT INTERCONNECTS)
 - IF APPLICABLE TO THE CELL TECHNOLOGY
- RESISTANCE LIMITED TECHNOLOGIES
 - $R_{\square}$ (SHEET RESISTIVITY OF LIMITING CURRENT CARRIER IN CELL)
 - P_{FL} (FRACTIONAL POWER LOSS ALLOWABLE IN CURRENT CARRIER)
 - FROM MANUFACTURER
- MODULE CONDUCTOR REQUIREMENTS
 - ρ (RESISTIVITY OF CURRENT CARRIERS IN MODULE) ($\rho = 1.7 \times 10^{-6} \Omega \cdot \text{cm}$ FOR Cu)
 - P_F (FRACTIONAL POWER LOSS ALLOWABLE IN MODULE CONDUCTORS)
 - FROM HANDBOOK OR MANUFACTURER

2.1.3.2 Equations for General Constraints

The basic algorithm for determining the maximum number of cells in a bypass group ($N_{BP\text{MAX}}$) is outlined in figure 2-2. The user specifies V_B . He may also specify the maximum allowable voltage from cell temperature constraints ($V_{RT\text{MAX}}$) or he may elect to calculate $V_{RT\text{MAX}}$ from typical temperature coefficients ($\Delta T/\Delta S$ and $\Delta T/\Delta P$) or from the thermal methodology. The equations in the thermal methodology are discussed in that section. The equation used to calculate $V_{RT\text{MAX}}$ from typical temperature coefficients are [1,2]:

$$P_D = \frac{(\Delta T/\Delta S) I_S A_{C\text{MAX}} - (T_{C\text{MAX}} - T_A)}{(\Delta T/\Delta P)} \quad (2-1)$$

$$V_{RT\text{MAX}} = \frac{P_D}{J_{MPC} A_{C\text{MAX}}} \quad (2-2)$$

where:

P_D = power dissipated in reverse bias
 I_S = standard insolation on cell
 $A_{C\text{MAX}}$ = maximum cell area input for this calculation
 $T_{C\text{MAX}}$ = maximum allowable cell temperature in reverse bias
 T_A = ambient temperature and
other parameters as previously defined.

Equation 2-1 is a heat transfer equation in which power input to a thermal cell produces a temperature rise. Equation 2-2 relates the electrical power dissipation, P_D , to the current and reverse voltage in the cell. J_{MPC} and I_S are used as worst case values since the actual current and insolation in a shadowed cell will be lower.

The lowest of the two voltages ($V_{RT\text{MAX}}$ and V_B) is chosen as the maximum allowable reverse voltage ($V_{R\text{MAX}}$). The equation for $N_{BP\text{MAX}}$ is derived from the equation for a bypass loop with one shadowed cell [3]:

$$(N_{BP} - 1) V_{OCC} = -V_R - V_{FD}$$

where:

V_R = reverse voltage on cell (negative)

V_{FD} = forward voltage of bypass diode

Solving for N_{BP} and substituting $V_{R\text{MAX}}$ in place of V_R ,

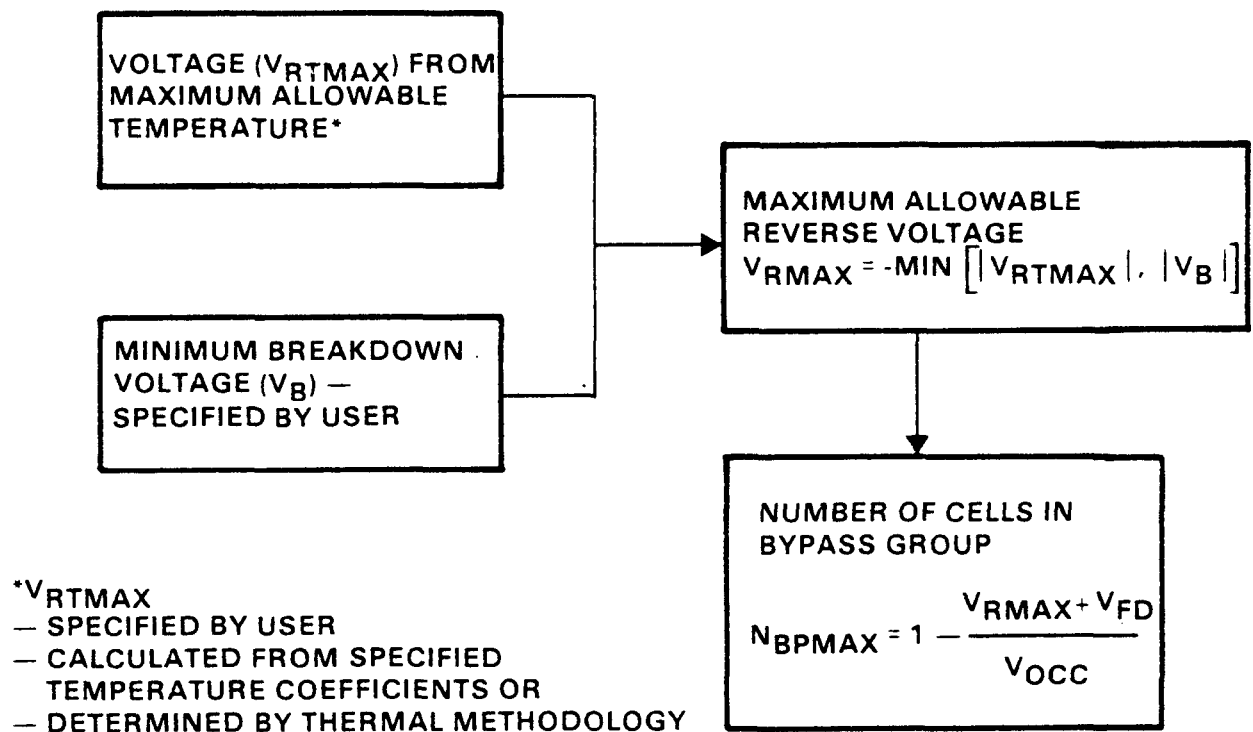


Figure 2-2. Determination of Maximum Number of Cells in Series in a Bypass Group

$$N_{BPMAX} = 1 - \frac{V_{RMAX} + V_{FD}}{V_{OCC}} \quad (2-3)$$

The equations used for the parallel redundancy constraint (N_{MMIN}) are derived from the situation illustrated in figure 2-3. N_M parallel strings are producing a current

$$J = N_M J_{MPC} \quad (2-4)$$

If one of the cells is shadowed or an interconnect is broken, the current capability is reduced. If the parallel group is in series with other identical groups, the tendency will be for this group to try to increase the current from each of the remaining $N_M - 1$ strings. If the $N_M - 1$ strings cannot produce a current equal to the original $N_M J_{MPC}$ before they reach short circuit, they will become reverse biased and not produce any power. To prevent this condition, the equation below must be satisfied.

$$(N_M - 1) J_{SCC} \geq N_M J_{MPC} \quad (2-5)$$

Solving for N_M , we obtain

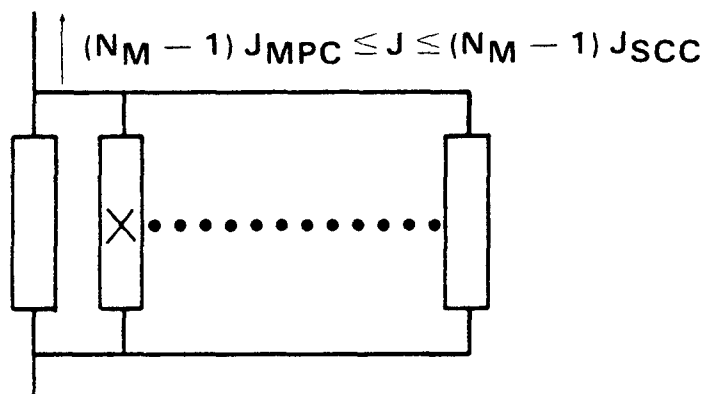
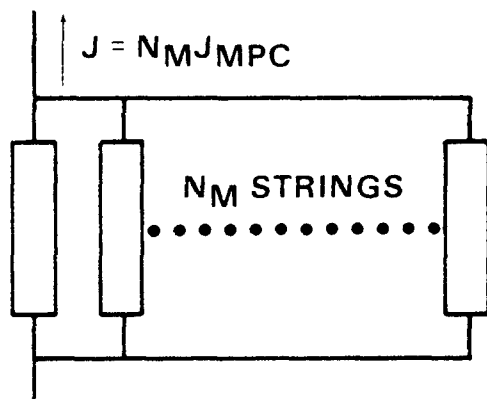
$$N_{MMIN} = \frac{J_{SCC}}{J_{SCC} - J_{MPC}} \quad (2-6)$$

If the PV cells have across-the-cell busbars and redundant interconnects, the parallel redundancy criterion may be redefined as follows. If a single interconnect is broken or a cell is cracked as described in [4], a cell having redundant interconnects will still be able to collect current. The N_{ACI} interconnects effectively divide the cell into $2 N_{ACI}$ sections. Assuming the busbars across the cell are not broken if a cell cracks, it can be seen that the worst condition would be a cell cracking on the outside of the busbars, as shown in figure 2-4, so that a whole section is lost. The cell will still be capable of producing $(2 N_{ACI} - 1) I_{SCC}$ where I_{SCC} is the short circuit current from one section of the cell. Thus, the parallel redundancy criterion can be written for N_M cells or strings as

$$(2 N_{ACI} N_M - 1) I_{SCC} \geq 2 N_M N_{ACI} I_{MPC} \quad (2-7)$$

Since

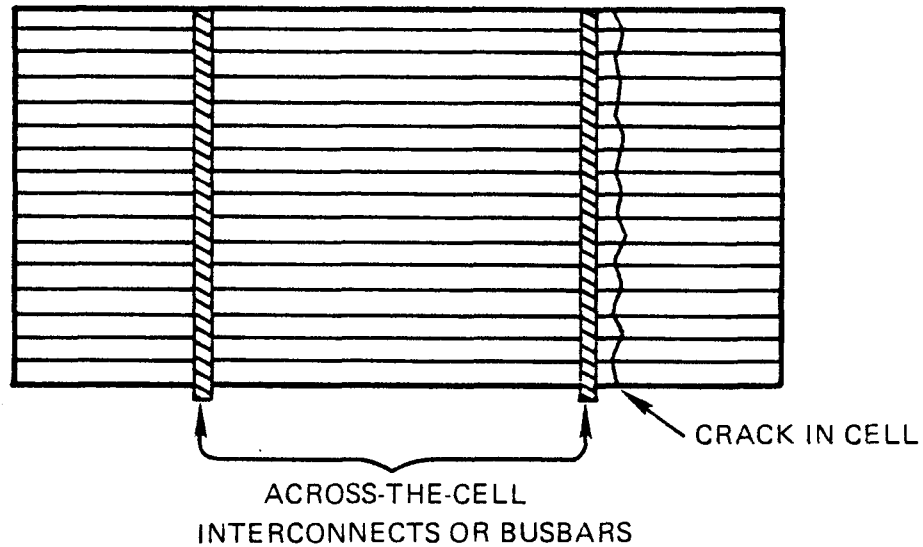
$$\frac{I_{MPC}}{I_{SCC}} = \frac{J_{MPC}}{J_{SCC}} ; \quad (2-8)$$



$$(N_M - 1) J_{SCC} \geq N_M J_{MPC}$$

$$N_{M\text{MIN}} = \frac{J_{SCC}}{J_{SCC} - J_{MPC}}$$

Figure 2-3. Parallel Redundancy Design



N_{ACI} = NUMBER OF ACROSS-CELL INTERCONNECTS

$2N_{ACI}$ = NUMBER OF EQUAL SIZE SECTIONS PRODUCED BY N_{ACI} BUSBARS

$2N_{ACI}-1$ = NUMBER OF SECTIONS FROM WHICH CURRENT CAN BE
COLLECTED WITH WORST CASE CRACK.

Figure 2-4. Cell with Across-Cell Interconnects Illustrating
Worst Case Crack

therefore,

$$N_{MMIN} = \frac{J_{SCC}}{2 N_{ACI} (J_{SCC} - J_{MPC})} \quad (2-9)$$

The equation for the constraint on the maximum number of cells allowable in series in the module (N_{BGMAX}) is obtained from the maximum voltage constraints specified.

$$N_{BGMAX} = \text{MIN} \left[\frac{V_{MPMAX}}{V_{MPC}}, \frac{V_{OCMAX}}{V_{OCC}(T_L)} \right] \quad (2-10)$$

where:

- N_{BGMAX} = maximum allowable number of cells in series in module = $N_{BP}N_G$
- N_{BP} = number of cells in bypass group
- N_G = number of bypass groups in series
- V_{MPMAX} = maximum desirable module voltage at maximum power point
- V_{OCMAX} = maximum allowable module open circuit voltage
- V_{MPC} = cell voltage at maximum power point
- $V_{OCC}(T_L)$ = cell open circuit voltage at the lowest anticipated cell temperature (T_L)
 $= V_{OCC}(T_C) + (\Delta V/\Delta T) (T_L - T_C)$
- T_C = cell temperature at which J-V curve was taken

The maximum desirable module voltage at peak power is divided by the cell peak power voltage and the maximum allowable voltage produced by the module (which will be open circuit voltage at low temperature) is divided by the cell open circuit voltage at the lowest temperature (T_L) anticipated in module applications. The lower of the two values is chosen and truncated to the next lower integer.

The nomenclature, N_{BG} , is obtained from the combination of N_{BP} and N_G since the total number of cells in series (N_{BG}) can be divided into the number of cells in series in a bypass group (N_{BP}) times the number of bypass groups in series in the module (N_G). Thus, the bypass group design proceeds from the same relationship.

$$N_{BP}N_G = \frac{V_{MPM}}{V_{MPC}} \quad (2-11)$$

In the computer program, a matrix of combinations which satisfy the constraints on N_{BPMAX} and N_{BGMAX} is generated and the most desirable combination is selected as the starting values for the module design. The other combinations are

available if a design cannot be obtained with the initial N_{BP} and N_G values. The detailed methodology is described in section 2.2.1.

2.1.3.3 Equations Used in Design Options

The basic electrical constraints and options are determined in the General Constraints methodology. In the design options, the electrical constraints are used in combination with the cell and module dimension constraints to obtain a regular series-parallel design and physical layout. Thus, the dimensional equations shown below are used in various forms to calculate and iterate on cell lengths, numbers of cells and module lengths. The analogous equations for series and parallel directions are:

$$L_{MS} = N_S L_{CS} + 2 \Delta_{SES} + (N_S - 1) \Delta_{SS} \quad (2-12)$$

where:

L_{MS} = module length in series direction
 N_S = number of cells in series direction
 L_{CS} = cell length in series direction
 Δ_{SES} = edge spacing in series direction
 Δ_{SS} = cell-to-cell spacing in series direction

and

$$L_{MP} = N_P L_{CP} + 2 \Delta_{SEP} + (N_P - 1) \Delta_{SP} \quad (2-13)$$

where the symbol definitions are analogous to the series case.

For circular cells, the methodology assumes that cell rows are staggered as shown in figure 2-5. The dimensional equations for this situation are

$$L_{MS} = (N_S - 1/2) b + D + 2 \Delta_{SES} \quad (2-14)$$

$$L_{MP} = (N_P - 1) \cdot a + D + 2 \Delta_{SEP} \quad (2-15)$$

where $b = D + \Delta_{SS}$

$$a = \frac{(D + \Delta_{SP})^2 - (D + \Delta_{SS})^2}{2(D + \Delta_{SP} + D + \Delta_{SS})}$$

$$D = L_{CS} = L_{CP} \quad (2-16)$$

The series direction of the cell is usually known for rectangular cells and is not critical for calculations for square or circular cells. The series dimension in the module is defined as the initial direction of the series

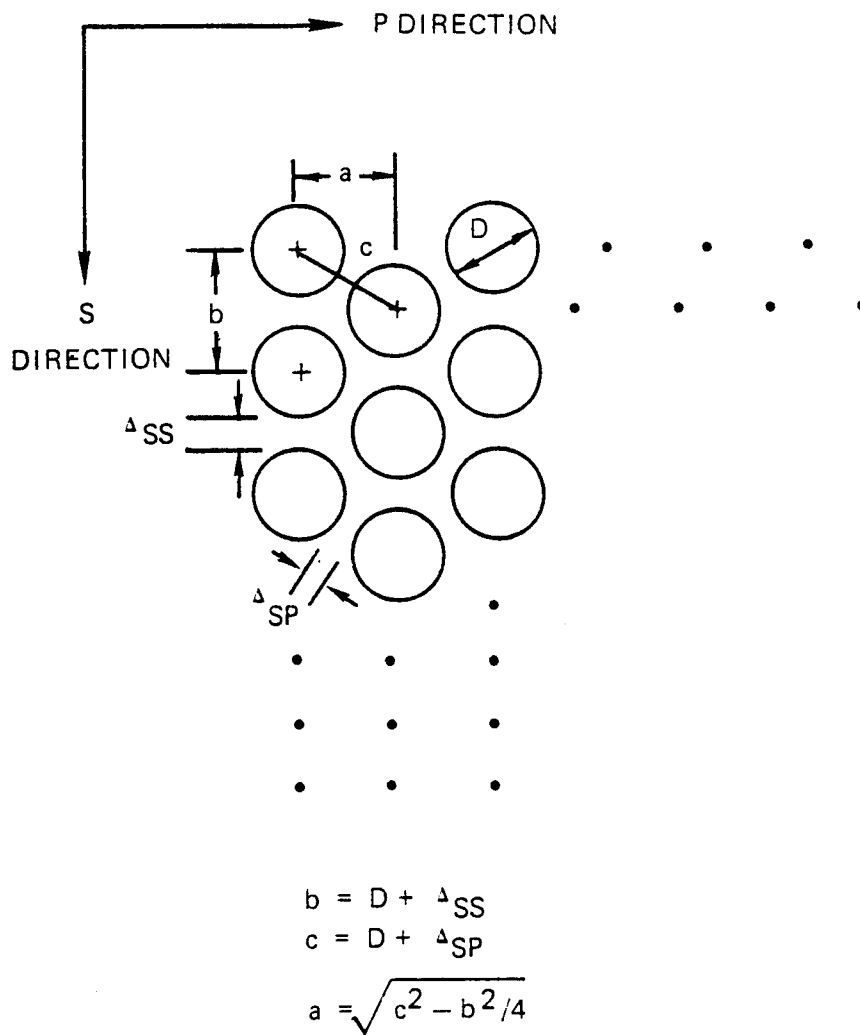


Figure 2-5. Basic Arrangement of Circular Cells in Module

connection of cells in a bypass group. The value of N_S will not always be equal to N_{BG} . N_S refers to the number of cells physically arranged in the series direction while N_{BG} is the number of cells connected in series to obtain the desired voltage. If the bypass group must be cut in half and turned back in the opposite direction in the case of long cells, $N_S = N_{BP}/2$ as shown in figure 2-6a. Then, N_M , defined as the number of bypass groups in the parallel direction, will be one half of N_P which is the number of cells physically arranged in the parallel direction, i.e., $N_M = N_P/2$.

If all N_G bypass groups cannot fit in the series direction, as in many cases with higher module voltages, the N_{BG} series cells can be turned back in the opposite direction one or more times as illustrated in figure 2-6b. In this case, $N_M = N_P/J$ and $N_{BG} = J N_S$ where J is the number of sections in the snake.

In cases of low module voltage, N_{BG} may be less than N_S . Therefore, bypass groups may be connected in parallel in the series direction as illustrated in figure 2-6c. In such cases, N_R is the number of bypass groups in a parallel connection block which are arranged in the series direction or $N_R = N_S/N_G$ and $N_M = N_P N_R$.

For design options 1, 4 and 5 in which the maximum cell area (A_{CMAX}) is specified, the optimum cell lengths in series and parallel are obtained from the equations

$$L_{CSOPT} = \sqrt{A_{CMAX} \left(\frac{\Delta_{SS}}{\Delta_{SP}} \right)} \quad (2-17)$$

$$L_{CPOPT} = \sqrt{A_{CMAX} \left(\frac{\Delta_{SP}}{\Delta_{SS}} \right)} \quad (2-18)$$

If $\Delta_{SS} = \Delta_{SP}$, a square cell is obtained. These equations maximize the packing factor for a given module size and given spacings. They were derived by using equations (2-12) and (2-13) in conjunction with the equation for the module packing factor

$$PF = \frac{N_S L_{CS} N_P L_{CP}}{L_{MS} L_{MP}} \quad (2-19)$$

The packing factor can thus be specified as

$$PF = \left(\frac{L_{MS}^{-2\Delta_{SES} + \Delta_{SS}}}{L_{MS}} \right) \left(\frac{L_{MP}^{-2\Delta_{SEP} + \Delta_{SP}}}{L_{MP}} \right) \left(\frac{L_{CS}}{L_{CS} + \Delta_{SS}} \right) \left(\frac{L_{CP}}{L_{CP} + \Delta_{SP}} \right) \quad (2-20)$$

Since the first two parentheses are constant and using

$$A_C = L_{CS} L_{CP} \quad (2-21)$$

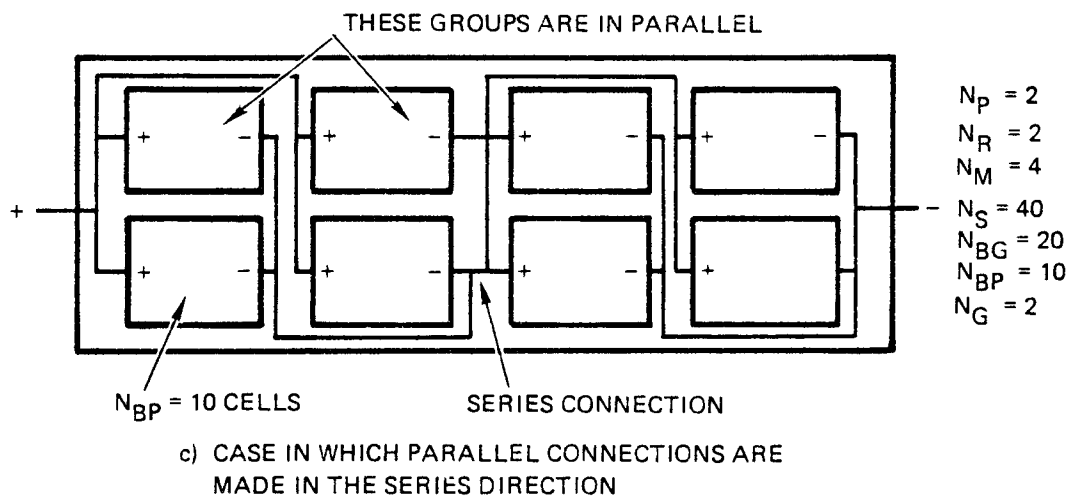
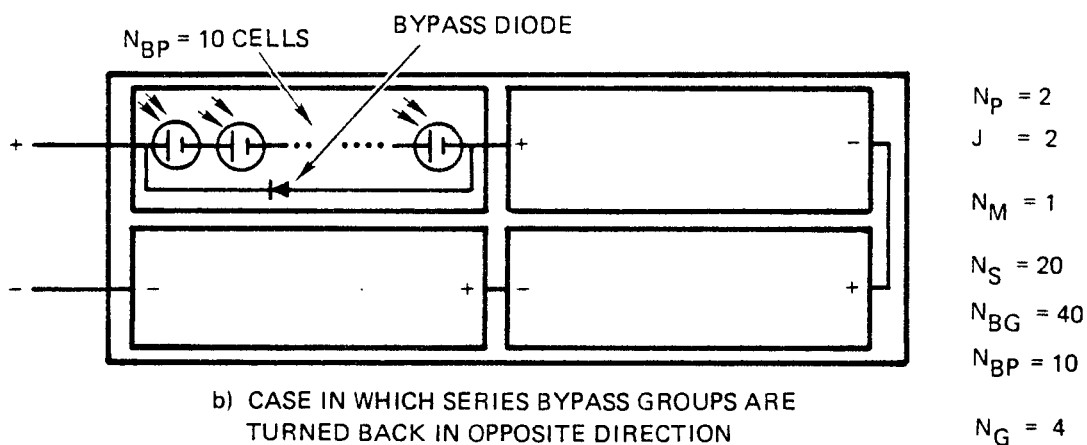
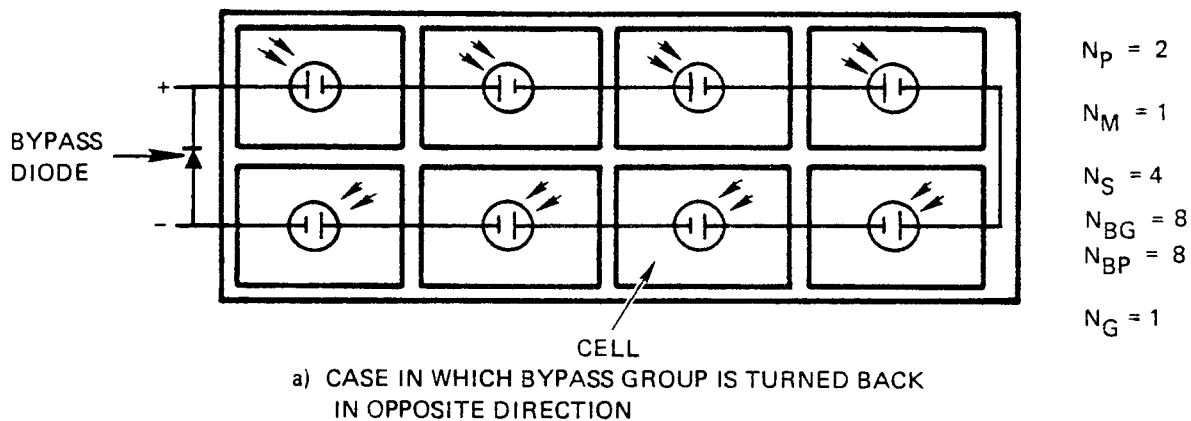


Figure 2-6. Examples in Which Either $N_M \neq N_P$ or $N_{BG} \neq N_S$

we obtain

$$PF = K \left(\frac{L_{CS}}{L_{CS} + \Delta_{SS}} \right) \left(\frac{A_C}{A_C + \Delta_P L_{CS}} \right) \quad (2-22)$$

in which A_C is a constant. Differentiating with respect to L_{CS} and setting the result equal to zero, we obtain the condition for the maximum packing factor

$$L_{CS} = \sqrt{A_C \left(\frac{\Delta_{SS}}{\Delta_{SP}} \right)} \quad (2-23)$$

This is the same as (2-17). Using equations (2-23) and (2-21), we obtain the equation as (2-18).

If the cells are circular, the length and width are the same and equal to the diameter. In this case, the equations reduce to

$$D = L_{CS} = L_{CP} = \sqrt{\frac{4 A_{C\text{MAX}}}{\pi}} \quad (2-24)$$

For the resistance limited case (design option 4), the maximum cell length in the series direction is constrained by the power loss due to the resistance of one of the current carriers in the cell. An equation obtained from reference [5] is used to determine this length constraint called W_{MAX} . It specifies the resistance power loss as a fraction (f) of the cell peak power as illustrated in figure 2-7. It can be derived as follows:

$$\begin{aligned} f P_C &= \frac{\rho}{TL_{CP}} \int_0^{L_{CS}} (JL_{CP}x)^2 dx \\ &= \frac{\rho}{3TL_{CP}} (JL_{CP})^2 L_{CS}^3 \end{aligned} \quad (2-25)$$

since

$$I = JL_{CP} L_{CS}, \quad (2-26)$$

$$f P_C = \frac{\rho}{3TL_{CP}} (I^2 L_{CS}) \quad (2-27)$$

We can apply this to our unit area cell, by returning to current density and noting that

$$P_C = FF_C I_{SCC} V_{OCC} = L_{CS} L_{CP} FF_C J_{SCC} V_{OCC} \quad (2-28)$$

where FF_C = cell fill factor.

Thus,

$$f L_{CS} L_{CP} FF_C J_{SCC} V_{OCC} = \left(\frac{\rho}{3TL_{CP}} \right) L_{CS}^2 L_{CP}^2 J_{SCC}^2 L_{CS} \quad (2-29)$$

We use W_{MAX} for the maximum series length, L_{CS} , to be consistent with [5] and obtain

$$W_{MAX} = \left(\frac{3f V_{OCC} FF_C}{R J_{SCC}} \right)^{1/2} \quad (2-30)$$

where R = sheet resistivity = ρ/T . In the flowcharted algorithms, P_{FL} is used in place of the symbol, f .

2.1.3.4 Equations Used in Module Conductor Requirements Routine

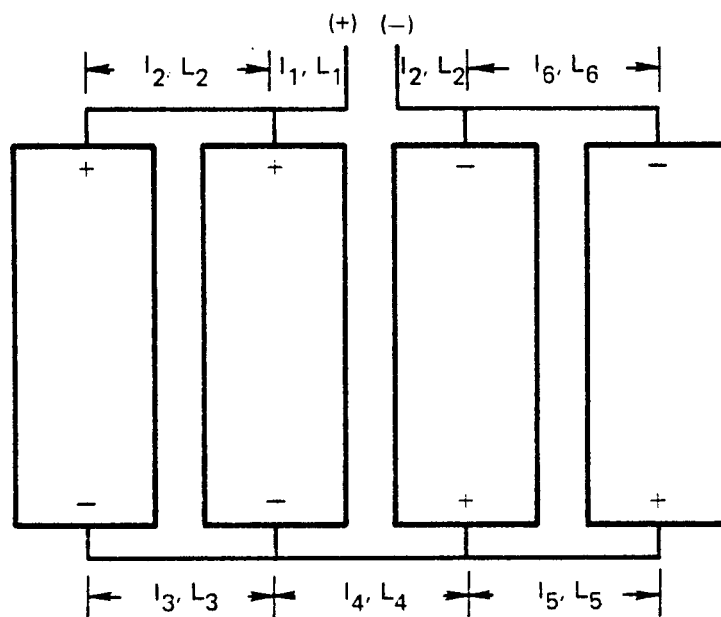
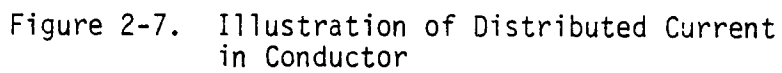
Following module design, the module metallization or interconnect conductor requirements are determined. The equations limit the power loss in the module due to conductor resistance. If the current in a conductor is constant, the equation used is

$$f P_M = \frac{\rho}{T_M W_M} \sum_{i=1}^N I_i^2 L_i \quad (2-31)$$

where the losses are added from all N conductor segments (example in figure 2-7a) which differ only in current or length, not in metal thickness, T_M , or width, W_M . The equation can be solved for T_M , W_M or $A = T_M W_M$ as the user chooses.

If the current is increasing in a distributed manner along the conductor length, analogous to the condition in figure 2-7, an equation similar to (2-27) is used

$$f P_M = \frac{\rho}{3T_M W_M} \sum_{i=1}^N I_i^2 L_i \quad (2-32)$$



$$\sum_{i=1}^7 l_i^2 L_i = l_1^2 L_1 + l_2^2 L_2 + l_3^2 L_3 + l_4^2 L_4 + l_5^2 L_5 + l_6^2 L_6 + l_7^2 L_7$$

WHERE $I_1 = I_4 = I_7 = 2 I_2 = 2 I_3 = 2 I_5 = 2 I_6$ AND

$$L_2 = L_3 = L_4 = L_5 = L_6 = 2L_1 = 2L_7$$

Figure 2-7a. Example of Conductor Runs in Module

This can again be solved for T_M , W_M or $A = T_M W_M$ as desired. In the flowcharted algorithms, P_F is used in place of the symbol, f .

2.1.3.5 Equations for Catalogue of Electrical Parameters

Following module design, the user will calculate and catalogue the cell and module physical and electrical characteristics. The equations listed in table 2-4 are used to obtain the final cell characteristics. The area dependent characteristics are simply multiplied by the final cell area. The equations used to obtain the module electrical characteristics are listed in table 2-5. The module voltages are obtained by multiplying the cell voltages by the number of cells connected in series $N_{BP}N_G$. The module currents are obtained by multiplying the cell currents by the number of cells connected in parallel, N_M . The module fill factor, FF_M , is analogous to the cell fill factor and is simply the module peak power divided by the module open circuit voltage and short circuit current. The packing factor is obtained by comparing the active cell area in the module (total number of cells, $N_G N_p$, times cell area, A_C) with the module area, A_M . The module efficiency can be obtained from the cell efficiency by multiplying by the packing factor of the module.

TABLE 2-4. CELL ELECTRICAL CHARACTERISTICS

$$\begin{aligned} V_{OCC}, V_{MPC}, FF_C, \eta_C & - \text{UNCHANGED} \\ A_C &= L_{CS} L_{CP} \\ I_{SCC} &= A_C J_{SCC} \\ I_{MPC} &= A_C J_{MPC} \\ P_C &= I_{MPC} V_{MPC} \end{aligned}$$

TABLE 2-5. MODULE ELECTRICAL CHARACTERISTICS

$$\begin{aligned} V_{OCM} &= N_{BP}N_G V_{OCC} \\ V_{MPM} &= N_{BP}N_G V_{MPC} \\ I_{SCM} &= N_M I_{SCC} \\ I_{MPM} &= N_M I_{MPC} \\ P_M &= I_{MPM} V_{MPM} \\ FF_M &= P_M / I_{SCM} V_{OCM} \\ PF &= N_G N_p A_C / A_M \\ \eta_M &= PF \eta_C \end{aligned}$$

2.2 USE OF ELECTRICAL METHODOLOGY ALGORITHMS

The flow charted algorithms presented and described in this section are suitable for use with paper and pencil and a hand calculator. The flowcharts differ somewhat from those used for the computer code although the logic of the algorithms is the same. For example, choosing the largest value from a set can be done in one step by the human mind, but requires a comparison routine for determination by computer. The algorithms will produce an optimum design based on the principle constraints for most cases. At times, however, a better design may be obtained by the creative user by revising some of the parameters or constraints input or by revising the logic of the algorithms to match different design principles. For example, the logic is based on obtaining the optimum packing factor at the maximum acceptable module voltage. Other voltages will be used only if a design cannot be obtained at this voltage. The user may instead choose to fix the number of cells in a bypass group and let the module voltage be any multiple of the bypass group voltage by altering these algorithms in the methodology.

Clearly, all possible design constraint options could not be addressed or the methodology would become unwieldy and incomprehensible. However, the experienced user can easily adapt the methodology to different or unusual circumstances. As a corollary to this statement, it becomes obvious that the methodology cannot handle all possible design conditions within the allowable options; for example, if the user specifies a fixed number of cells in Design Option 2 which is not divisible by any available N_{BP} value. But this is a situation in which the problem should have been more carefully formulated and different user-defined constraints imposed. Even in this case, the methodology will provide valuable insight to the user and guide him to a more reasonable problem formulation.

Overview flowcharts are provided for major sections of the methodology. In addition, each major section is divided into subroutines and these are flow-charted in detail. Where subroutines are complicated, both overview and detailed flowcharts are provided. A list of all flowcharts is contained for reference in table 2-6.

2.2.1 Main Routine and General Constraints

An overview of the main program which includes determination of general constraints is presented in figure 2-8. The user may specify cell electric parameters or input J-V curve point pairs and determine the parameters from these. The user is then led through the determination of derived constraints obtained from cell and module specifications and constraints. First, the allowable module peak power voltages, $V_{MPM}^{(M)}$, is specified. The number of cells, N_{BG} , required in series to obtain these voltages are calculated. Next, the maximum number of cells permitted in series in a bypass group, N_{BPMAX} , is determined from either the reverse breakdown voltage, V_B , or from the reverse voltage, V_{RTMAX} , at which maximum cell temperature, T_{CMAX} , is achieved. Both of these conditions are examined and the most restrictive (smallest N_{BPMAX}) is used.

TABLE 2-6. CATALOGUE OF ELECTRICAL ALGORITHM FLOWCHARTS

Type of Flowchart	Description	Figure Number
Overview	Electrical Methodology	2-1
Overview	Main Routine and General Constraints	2-8
Detailed	Unit Cell Characteristics	2-9
Detailed	Catalogue of V_{MPM} , N_{BG} Combinations and Determination of V_{MPMAX}	2-10
Detailed	Determination of N_{BPMAX}	2-11
Detailed	Determination of N_{MMIN}	2-12
Detailed	Determination of N_{BGMAX} and Catalogue of Acceptable N_{BP} , N_G Combinations	2-13
Detailed	Choosing N_{BP} , N_{GMAX} for All Design Options	2-14
Overview	Design Options 1 and 3	2-15
Detailed	Entry and Calculation of Cell Size and Initial Numbers of Cells	2-16
Detailed	Selection of Acceptable N_S , N_{BP} Combination	2-17
Overview	Snaking N_{BG} or Paralleling in Series Direction and/or Altering N_S and N_p	2-18
Detailed	Snaking N_{BG} or Paralleling in Series Direction and/or Altering N_S and N_p	2-19
Overview	Completing Design for $K = N_{GMAX}$ and N_{S2} Condition	2-20
Detailed	Completing Design for $K = N_{GMAX}$ and N_{S2} Condition	2-21
Detailed	N_{MMIN} Check and Completion of Design Options 1 and 3	2-22
Overview	Design Option 2	2-23
Detailed	Determination of Various Acceptable Cell Arrangements	2-24

TABLE 2-6. CATALOGUE OF ELECTRICAL ALGORITHM FLOWCHARTS (CONCLUDED)

Type of Flowchart	Description	Figure Number
Overview	Design Option 4	2-25
Detailed	Determination of Cell Size Constraints	2-27
Detailed	Determination of N_R and L_{CS} and L_{CSMIN} Check	2-28
Detailed	Iterating N_G When Solution Can Not Be Obtained with Allowable N_{BP} Values	2-29
Detailed	Parallel Parameters and Completion of Design Option 4	2-30
Overview	Design Options 5 and 6	2-31
Detailed	Entry and Calculation of Initial Numbers of Cells and Cell Size	2-32
Detailed	Selection of Acceptable N_S , N_{BP} Combination	2-33
Overview	Snaking N_{BG} or Paralleling in Series Direction and/or Altering N_S and N_p	2-34
Detailed	Snaking N_{BG} or Paralleling in Series Direction and/or Altering N_S and N_p	2-35
Overview	Completing Design for $K = N_{GMAX}$ and N_{S2} Condition	2-36
Detailed	Completing Design for $K = N_{GMAX}$ and N_{S2} Condition	2-37
Detailed	N_{MMIN} Check and Completion of Design Options 5 and 6	2-38
Overview	Module Conductor Requirements Routine	2-39
Detailed	Module Conductor Requirements	2-40

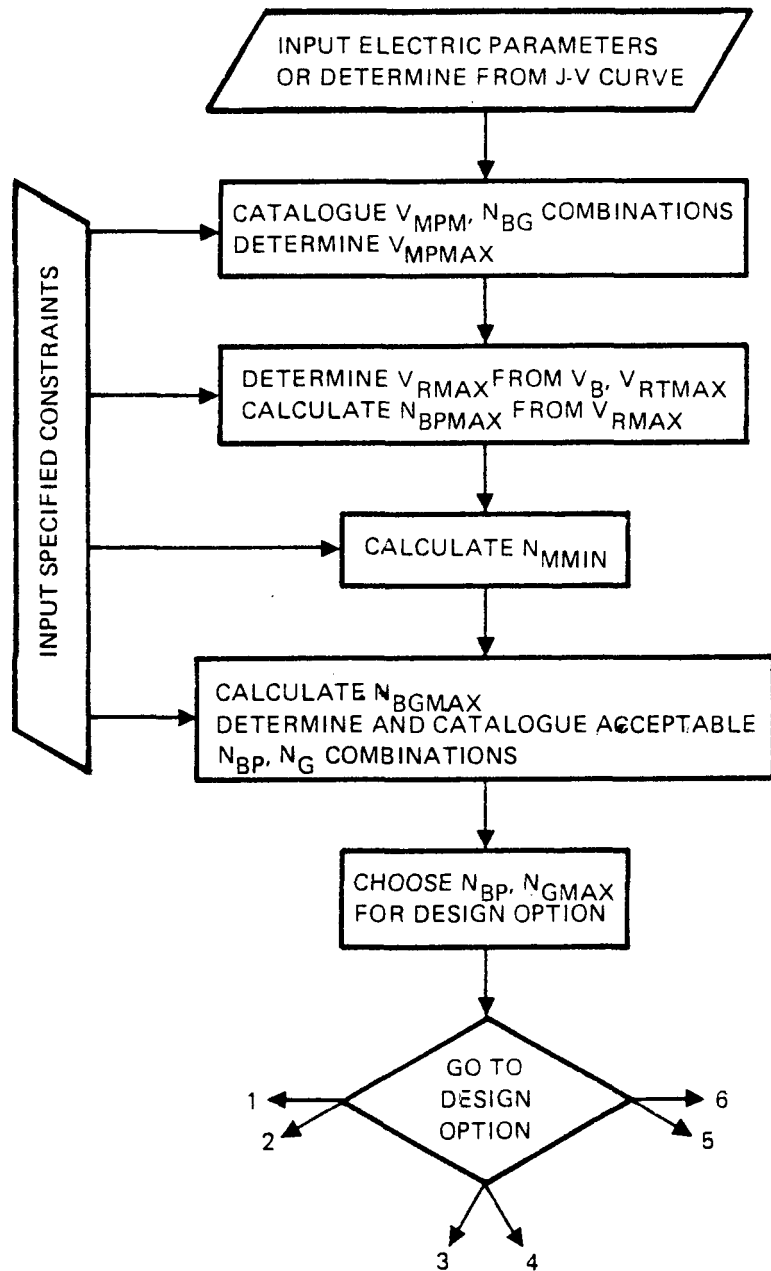


Figure 2-8. Overview Flowchart for Main Routine and General Constraints

The methodology, then, calculates the maximum number of cells or series strings connected in parallel, N_{MIN} , which are needed to ensure parallel redundancy; i.e., the bypass group will produce power with single-cell shadowing or failure, which are considered practical and not overly restrictive. The maximum number of cells allowable in series, N_{BGMAX} , is next determined based on maximum allowable module voltages, V_{MPMAX} and V_{OCMAX} , and the allowable N_{BP} and N_G (number of bypass groups in series) combinations are calculated and catalogued. Finally, the methodology chooses one N_{BP} , N_G combination (largest N_{BP} and highest V_{MPM}) for use in the module design to be completed in one of the six design options.

As shown in the first detailed flowchart in figure 2-9, the user may either input the required cell parameters (option A) or input J-V curve points (option B). In option B, the user inputs the insolation on the cells, S_C , and then operates on the curve points. He selects the point at which $J = 0$ as the open circuit point and the corresponding voltage is the open circuit voltage, V_{OC} . The user, likewise, selects the point at which $V = 0$ as the short-circuit point and the corresponding current density is the short-circuit current density, J_{SC} . For all points, the user calculates the power, $P(N)$, and compares each of them to find the largest value which is the cell peak power, P_C . The voltage and current density at this point are the peak voltage, V_{MPC} , and peak current density, J_{MPC} , respectively. The user then calculates the fill factor, FF_C , and the cell efficiency, η_C .

The method of stepping through a "DO Loop" and performing one calculation and one comparison at a time may seem overly formalized and unnecessary. It was presented in this manner because the notation is understood by most, it provides a method of progressing logically and cataloguing results, and it lends itself well to computer programming.

In the next section, figure 2-10, the user inputs the number, M , of allowable module peak power voltages, V_{MPM} , calculates the number of cells required in series, N_{BG} , for each, and catalogues the values with the indices 1 through M . V_{MPMAX} is catalogued for later use as the largest V_{MPM} input. The values of N_{BG} are either rounded to the nearest integer for $V_{MPM}(M) < V_{MPMAX}$ or truncated to the next lower integer for V_{MPMAX} .

For the determination of N_{BPMAX} (figure 2-11), the user has three options. He may input a value for V_{RTMAX} which was previously determined or estimated; he may use the thermal methodology to calculate V_{RTMAX} from an analysis of the module laminations; or he may calculate V_{RTMAX} based on expected temperature coefficients for insolation ($\Delta T/\Delta S$) and power dissipation ($\Delta T/\Delta P$). Typical values for 4-inch diameter cells are shown. The values should be scaled by area for other size cells. $\Delta T/\Delta S$ is estimated from a typical temperature rise with insolation for flat plate modules of about 25-30°C. $\Delta T/\Delta P$ is usually slightly less due to the spacing between cells and can be estimated by multiplying $\Delta T/\Delta S$ by the packing factor, PF .

The value of reverse voltage, V_{RMAX} , used in the calculation of N_{BPMAX} is the smaller of the thermal based voltage, V_{RTMAX} , and the specified reverse breakdown voltage, V_B . V_{RMAX} is always a negative value. In the N_{BPMAX} equation, V_{FD} is the forward voltage drop of the bypass diode, typically 0.7V. Non-integer values of N_{BPMAX} should be truncated to the next lower integer.

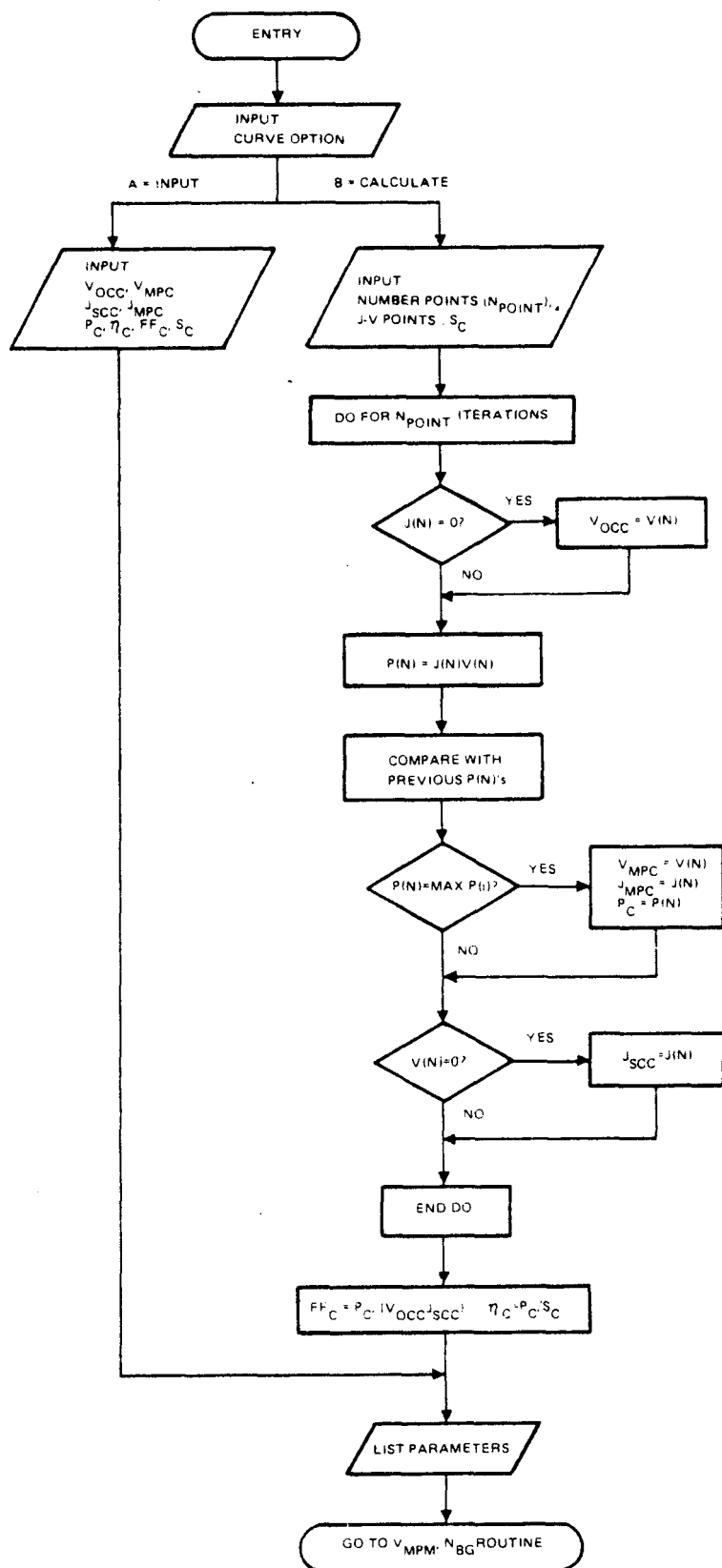


Figure 2-9. Flowchart for Unit Area Cell Characteristics

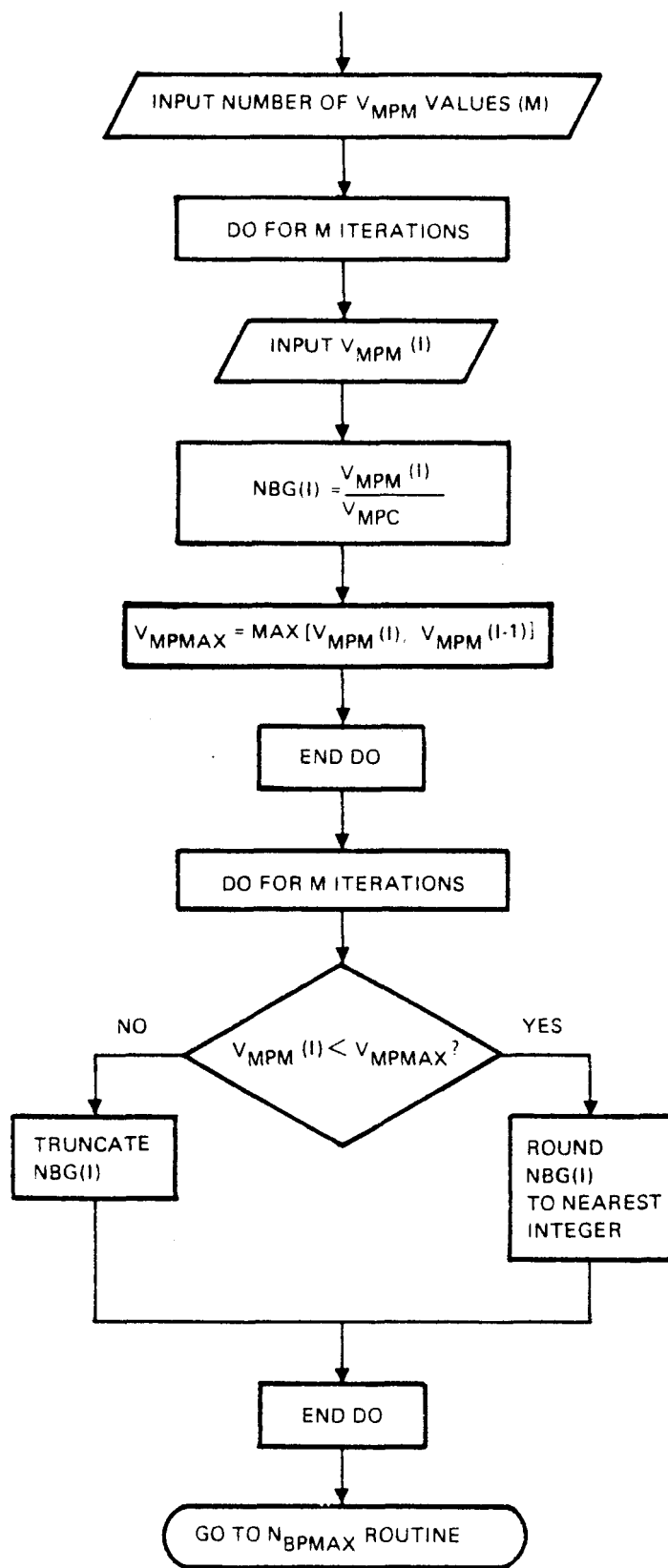


Figure 2-10. Flowchart for Catalogue of V_{MPM} , N_{BG} Value and Determine V_{MPAX}

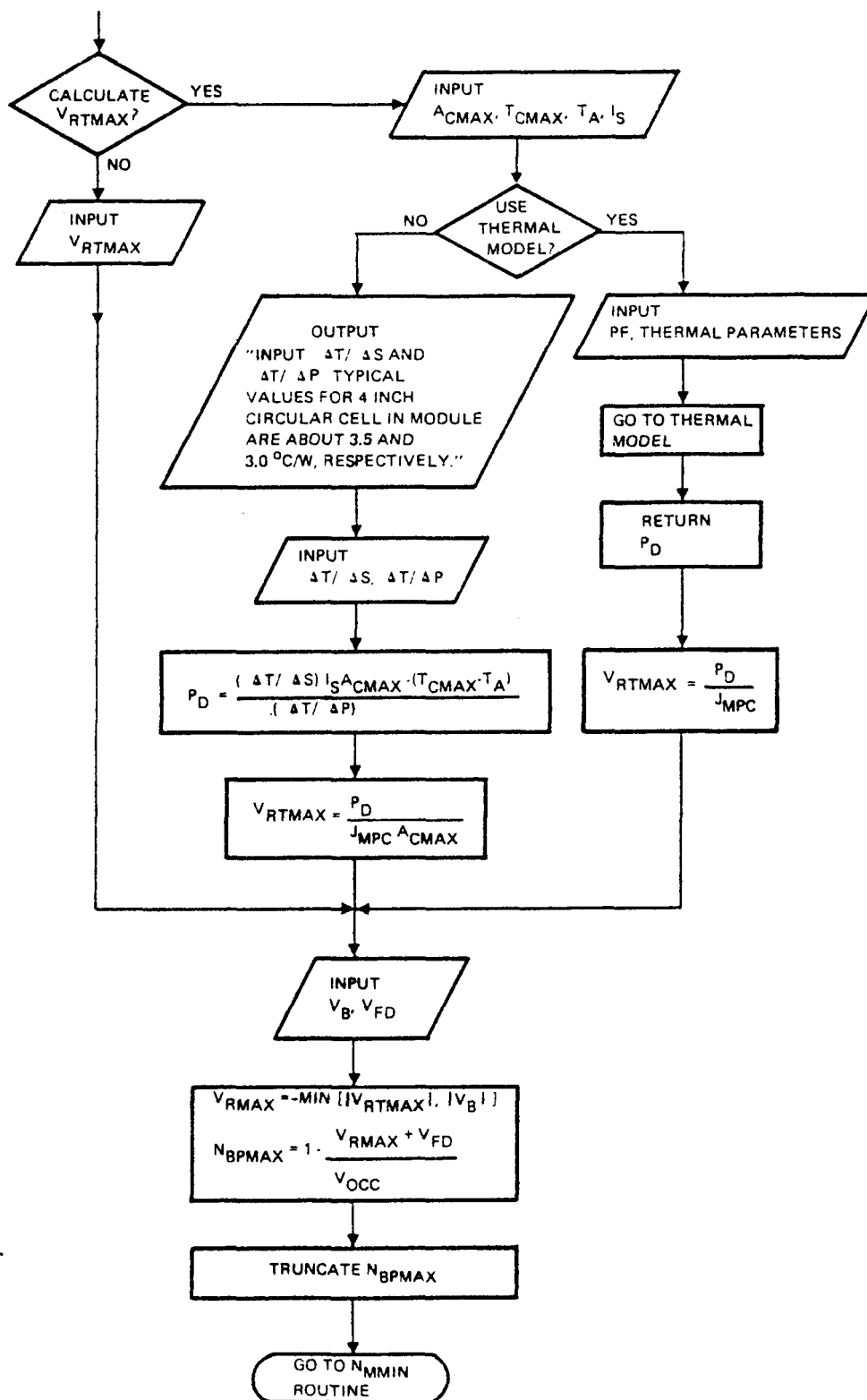


Figure 2-11. Flowchart for Determination of N_{BPMAX}

The flowchart in figure 2-12 is used to determine the parallel redundancy guideline. If the cell contains redundant, across-the-cell interconnects, the equation on the left is used to calculate the minimum number of cells or strings required to be connected in parallel, N_{MMIN} . If the cell has one or no across-the-cell interconnects, the equation on the right is used which produces a larger requirement for the same short-circuit to peak-power current ratio. If the resultant value is not an integer, it is increased to the next higher integer.

The parallel redundancy specification is a soft constraint, i.e., it is not used by the methodology in any design decisions but is provided to the user as a guideline. Not all designs obtained from the methodology will satisfy this constraint. The user may choose to alter the design obtained or reformulate the problem to satisfy this constraint if he wishes. It was felt that attempting to force the methodology to satisfy this constraint would reduce the probability of successfully obtaining a design or would make the algorithms overly complex.

The flowchart in figure 2-13 is used to limit the maximum allowable number of cells in series in the module, N_{BGMAX} . The algorithm chooses the lower value from the two calculations - one from specification of the maximum voltage allowable from safety or reliability considerations, the other from the maximum desirable peak power voltage. Since the highest voltage is obtained at open circuit and at low temperature, V_{OCMAX} is used and applied at the lowest expected cell temperature, T_L , typically -20°C . V_{OCC} is the cell voltage at the nominal temperature obtained from the J-V curve which must be adjusted for low temperature by the voltage coefficient with temperature ($\Delta V/\Delta T$). Frequently, the maximum desirable voltage, V_{MPMAX} , cannot be obtained because the V_{OCMAX} constraint produces a lower N_{BG} . Noninteger values of N_{BGMAX} are truncated.

The methodology then determines and catalogues the acceptable N_{BP} , N_G combinations subject to the constraints:

$$(1) \quad N_{BPMIN} \leq N_{BP} \leq N_{BPMAX} \quad (2-33)$$

$$(2) \quad N_{BP}N_G = N_{BG} \leq N_{BGMAX} \quad (2-34)$$

$$(3) \quad N_{BP} = \text{Integer} \quad (2-35)$$

First, N_{BPMIN} is specified as half N_{BPMAX} . Allowing the bypass group size to be smaller than this could result in using more than twice the diodes necessary for protection, thus, significantly increasing the cost. Of course, the user of the manual calculation methodology can easily alter this constraint value.

Next, the methodology operates upon each of the M values of N_{BG} obtained in figure 2-10. Each $N_{BG}(N)$ value is compared with N_{BGMAX} . If $N_{BG}(N)$ does not satisfy equation 2-34, it is dropped and the methodology proceeds to the next $N_{BG}(N)$. If, on the other hand, $N_{BG}(N) \leq N_{BGMAX}$, it is divided by integer values of N_G from 1 up to $N_{BG}(N)$ to obtain a series of $N_{BP}(N, N_G)$ values. Since N_{BG} is the number of cells connected in series to obtain a particular voltage, dividing it by progressively more bypass groups (N_G) will produce progressively smaller bypass group series (N_{BP}) with the smallest being a

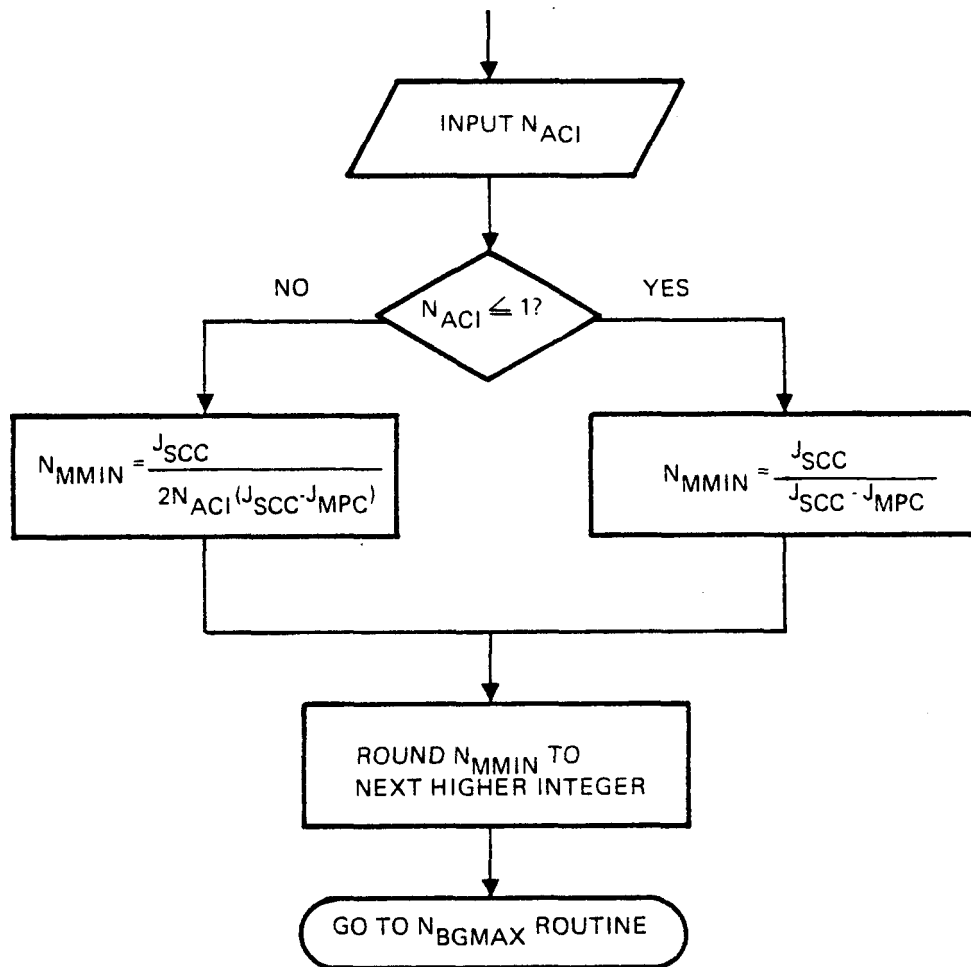


Figure 2-12. Flowchart for Determination of N_{MMIN}

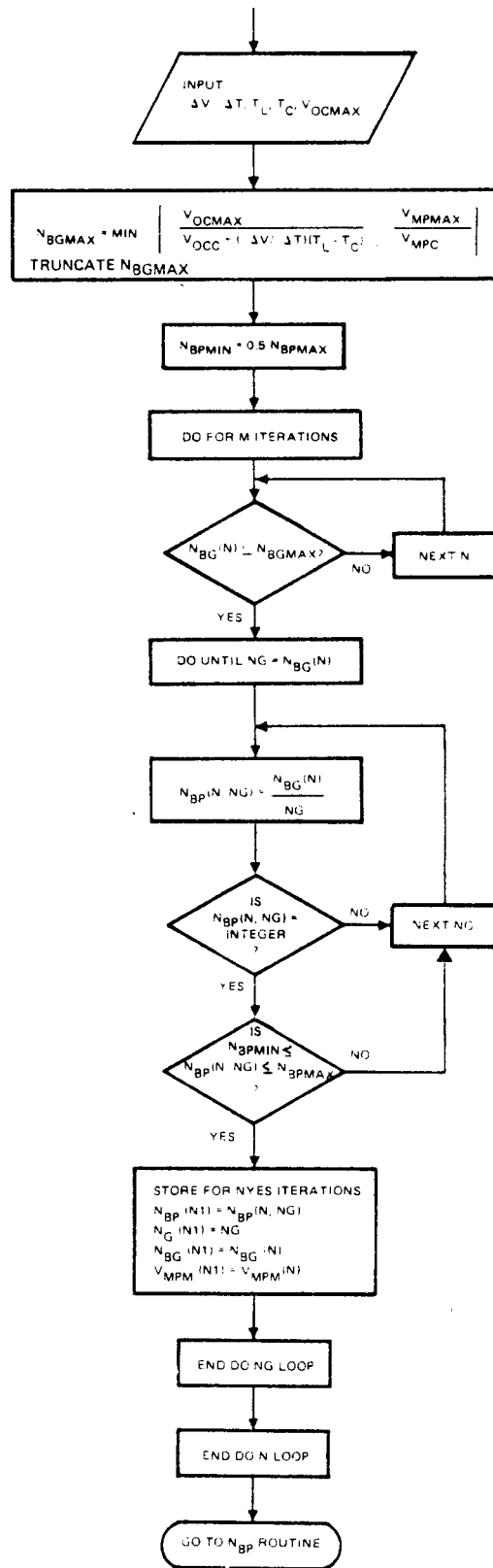


Figure 2-13. Flowchart for Determination of N_{BGMAX} and Catalogue of Acceptable N_{BG} , N_G Combinations

single cell. All N_{BP} values obtained which are both integers and fall between N_{BPMIN} and N_{BPMAX} are catalogued serially with the N_I index along with their associated N_G , N_{BG} and V_{MPM} values. The number of acceptable combinations (yes answers) is stored as the $NYES$ parameter.

Table 2-7 illustrates a typical matrix of N_{BP} , N_G combinations. In constructing the matrix, it was assumed that $V_{MPC} = 0.5V$, $N_{BGMAX} = 35$ (based on the low temperature constraint), $N_{BPMAX} = 8$ and the V_{MPM} values previously input in figure 2-10 were 5V, 10V and 20V. Using the calculational flow chart as illustrated in figure 2-10 yields $N_{BG}(N)$ values of 10, 20 and 40, respectively. For $V_{MPM}(1) = 5V$, $N_{BG} = 10$ and, therefore, the $N_{BP}(1, N_G)$ values range from 10 at $N_G=1$ to 1 at $N_G=10$. $N_{BP}(1, 1) = 10$ is not acceptable because it is greater than $N_{BPMAX} = 8$. $N_{BP}(1, 2) = 5$ is acceptable (yes answer) and is assigned to the first N_I index. Thus, $N_{BP}(1) = 5$. Its associated variables are also stored as $N_G(1) = 2$, $N_{BG}(1) = 10$, $V_{MPM}(1) = 5$.

The N_{BP} values for $N_G = 3, 4$ and 6 through 9 are not acceptable because they are not integers. $N_{BP}(1, 5) = 2$ and $N_{BP}(1, 10) = 1$ are also not acceptable because they are both less than $N_{BPMIN} = 4$.

For the second V_{MPM} value (10V), $N_{BG}(2) = 20$ and N_G is stepped from 1 to 20. There are two acceptable N_{BP} values - $N_{BP}(2, 4) = 5$ and $N_{BP}(2, 5) = 4$. These are assigned the N_I indices, 2 and 3, respectively, with their associated N_G , N_{BG} and V_{MPM} values.

The $N_{BG} = 40$ value, for the third V_{MPM} (20V), is not acceptable since it is greater than $N_{BGMAX} = 35$. Therefore, it is dropped and thus no N_{BP} values calculated for this level. The total number of acceptable N_{BP} results in $NYES = 3$.

The final flowchart (figure 2-14) in the main routine compares the N_I acceptable N_{BP} , N_G combinations and chooses the one which contains the largest N_{BP} in the highest V_{MPM} group. In the example in table 2-7, the methodology would choose the $N_I = 2$ values so that $N_{BP} = N_{BP}(2) = 5$, $N_{GMAX} = N_G(2) = 4$. These values will be used as the starting points for the design options. Since other acceptable combinations may be requested if the starting values are not compatible with the dimensional constraints, they should be catalogued and kept for ready reference.

It can be seen that the experienced user will be capable of exercising other options in this selection process. If he chooses to maximize the number of cells in a bypass group, he can alter his algorithm to choose the largest N_{BP} in the matrix regardless of the V_{MPM} value, or he can accept rounded-off non-integer N_{BP} such as $N_{BP}(2, 3) = 6.67$ rounded to 7 from $N = 2$ and $N_G = 3$. He would then obtain $V_{MPM} = 10.5V$ instead of 10.0V and N_{BG} would change to 21. Thus, for the experienced user, the methodology provides a starting point for more creative designing.

2.2.2 Design Options 1 and 3

Design options 1 and 3 (overview flowchart in figure 2-15) differ only in input constraints and initial cell length calculations. In design option 1,

TABLE 2-7. TYPICAL N_{BP} , N_G MATRIX

N	$V_{MPM}(N)$	$N_{BG}(N)^*$	N_G	$N_{BP}(N, N_G)^*$	ACCEPTABLE	N1
1	5V	10	1	$10 > N_{BPMAX} = 8$	No	-
			2	5	Yes	1
			3-4	Not Integers	No	-
			5	$2 < N_{BPMIN} = 4$	No	-
			6-9	Not Integers	No	-
			10	$1 < N_{BPMIN}$	No	-
2	10V	20	1	$20 > N_{BPMAX}$	No	-
			2	$10 > N_{BPMAX}$	No	-
			3	Not Integer	No	-
			4	5	Yes	2
			5	4	Yes	3
			6-9	Not Integers	No	-
			10	$2 < N_{BPMIN}$	No	-
			11-19	Not Integers	No	-
3	20V	$40 > N_{BGMAX} = 35$	20	$1 < N_{BPMIN}$	No	-
			-	-	No	-

*Assumptions: $N_{BGMAX} = 35$, $N_{BPMAX} = 8$, $V_{MPC} = 0.5V$

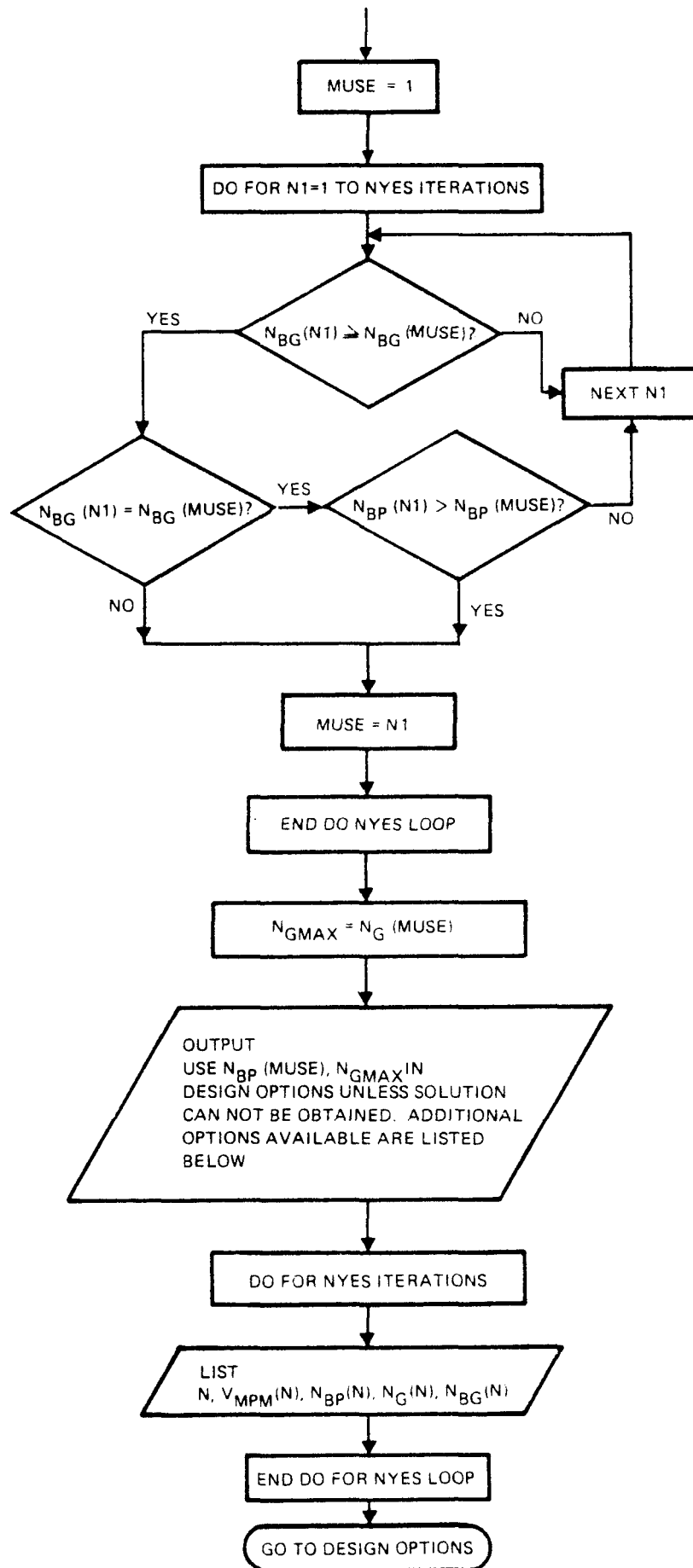


Figure 2-14. Flowchart for Choosing N_{BP} , N_{GMAX} for All Design Options

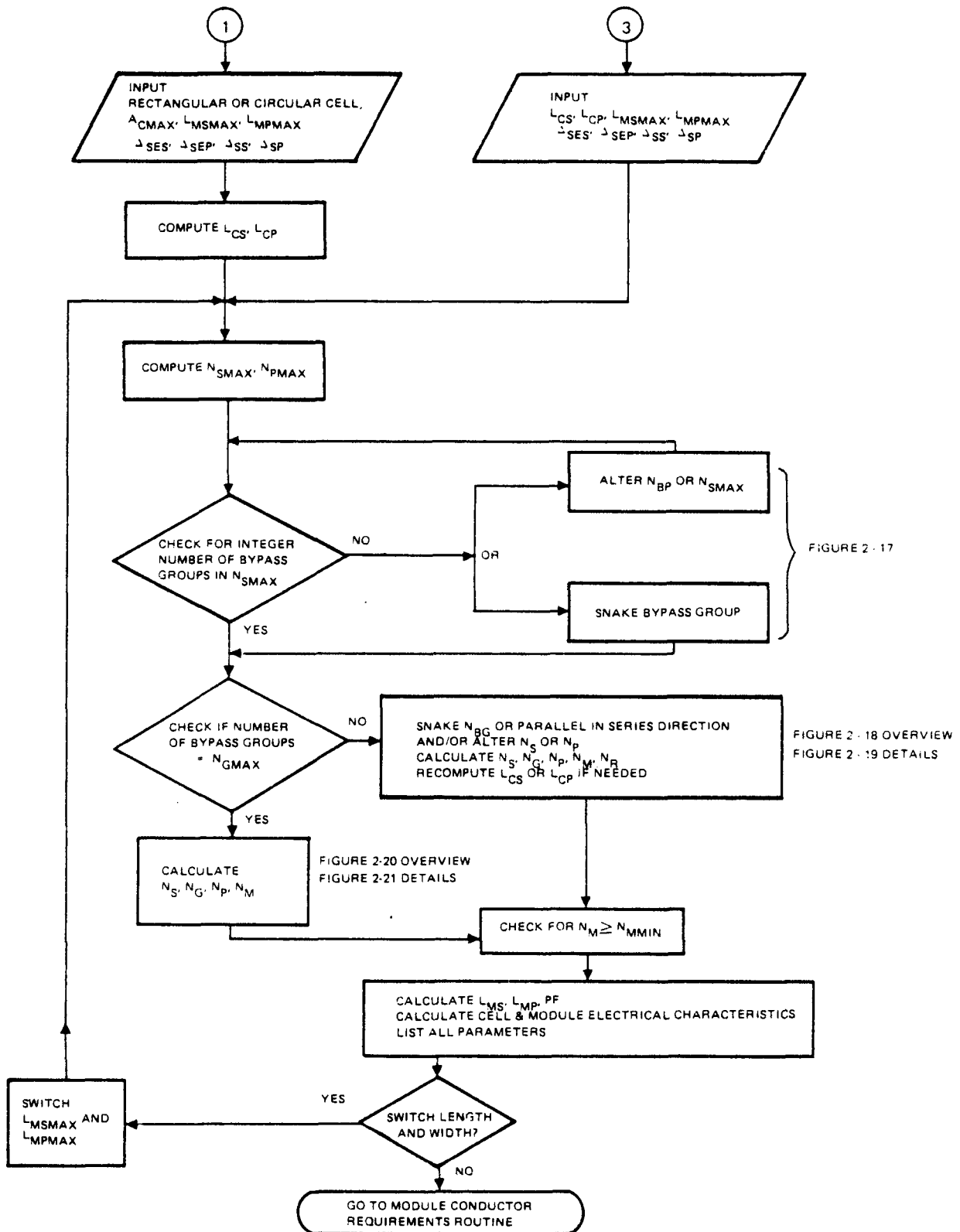


Figure 2-15. Overview Flowchart for Design Options 1 and 3

the maximum cell area is specified and the dimensions of the cell in the series and parallel directions are calculated. In design option 3, the series and parallel cell lengths are input by the user. The methodology attempts to preserve these cell dimensions in the design by reducing the number of cells and the module lengths when needed. As a last resort, the cell lengths may be reduced to prevent exceeding the maximum module lengths when no other method of obtaining a solution is possible. These situations will be described in subsequent detailed flowcharts.

Following determination of cell lengths, the maximum numbers of cells which can fit in each direction, N_{SMAX} and N_{PMAX} , are determined. In the first decision block, N_{SMAX} is checked for divisibility by N_{BP} . If an integral number of bypass groups cannot fit in the series length, either N_{BP} or N_{SMAX} may be altered or the bypass group may be snaked back on itself depending on availability of other N_{BP} options and size of the cells relative to the module. These options will be described in a subsequent flowchart.

The next decision block checks for compatibility of K , the number of bypass groups which fit in the series direction, with N_{GMAX} derived in the main program. If these integers are not equal, the series string may be snaked or bypass groups may be paralleled in the series direction and/or N_S and N_P may be changed depending on relative values of K , N_{GMAX} , N_S , and N_P . If N_S or N_P is increased, the corresponding cell length must be reduced.

Next, the parallel redundancy check is made by comparing N_M , the number of cells or strings connected in parallel, with N_{MIN} , derived in the main program. Then, the final module lengths are calculated from N_S , N_P , L_{CS} , L_{CP} , and the appropriate spacings. The packing factor is calculated as are the final cell and module electrical parameters.

The final decision block recommends switching series and parallel directions in the module to obtain an alternate design. If the user wishes to do this, he returns to the point of calculation of maximum numbers of cells, N_{SMAX} , and N_{PMAX} . When the user is satisfied with the designs, he may proceed to the Module Conductor Requirements routine, which allows him to estimate conductor runs required in the module.

The first detailed flowchart (figure 2-16) diagrams the entry into design options 1 and 3 and the initial calculations through N_{SMAX} and N_{PMAX} . The user inputs either cell maximum area (option 1) or cell dimensions (option 3). He also inputs maximum module dimensions and the spacings from cell to edge in each direction (Δ_{SES} and Δ_{SEP}) and cell-to-cell spacings in each direction (Δ_{SS} and Δ_{SP}).

Design option 1 permits module design with either rectangular or circular cells. For circular cells, the series and parallel lengths are identical and equal to the cell diameter. Calculations in the subsequent flowcharts use L_{CS} and L_{CP} , but it should be understood that these must be kept identical for circular cells. If one must be changed, the other is identically changed.

Different equations are also used for circular versus rectangular cells for calculating N_{SMAX} and N_{PMAX} from cell lengths and maximum module lengths.

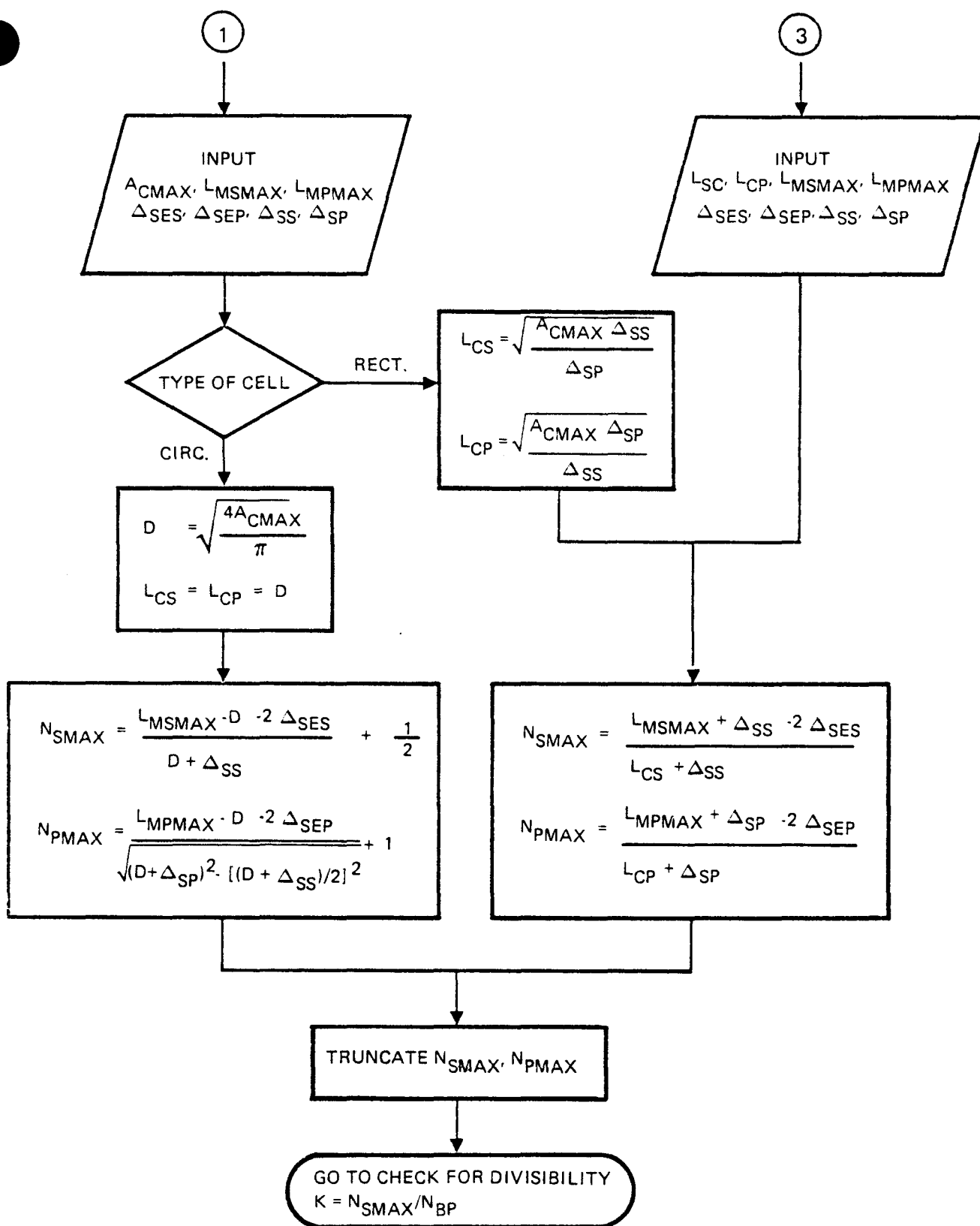


Figure 2-16. Detailed Flowchart for Entry Into Design Options 1 and 3 and Calculation of Cell Size and Initial Numbers of Cells

These equations were derived in section 2.1.3.3. Noninteger values of $N_{S_{MAX}}$ and $N_{p_{MAX}}$ are truncated to the next lower integer. Thus, the cell lengths remain the same but the module lengths (L_{MS} and L_{MP}) will be slightly less than the maximum used ($L_{MS_{MAX}}$ and $L_{MP_{MAX}}$).

The methodology proceeds by checking for the divisibility of $N_{S_{MAX}}$ by N_{BP} (figure 2-17). In other words, "Will an integral number of bypass groups fit within the module series length as represented by $N_{S_{MAX}}$ (the total number of cells which fit in the series length)?" If the answer is "yes"; i.e., $K = \text{integer}$, the user proceeds to the next flowchart. If the answer is "no", N_{BP} or $N_{S_{MAX}}$ must be altered or the bypass group must be snaked.

For K not an integer, the algorithm first searches the matrix of acceptable N_{BP} , N_G combinations to find the next lower N_{BP} which, with its N_G , will produce the same voltage, V_{MPM} . If another combination is found, $N_{G_{MAX}}$ is set equal to the new N_G and a new K is obtained. If this K is an integer, the user exits the flowchart. If K is not an integer, the N_{BP} , N_G matrix is searched for another combination.

Any time another N_{BP} , N_G combination is not available at the original V_{MPM} , the algorithm searches the N_{BP} , N_G matrix for the largest N_{BP} at the next lower V_{MPM} . If found, $N_{G_{MAX}}$ is again set to the new N_G ; K is again obtained and tested as an integer.

If no other N_{BP} , N_G combinations can be found, or if all acceptable N_{BP} values fail to test for divisibility into $N_{S_{MAX}}$, the size of the original N_{BP} is compared with $N_{S_{MAX}}$. If N_{BP} is less than $N_{S_{MAX}}$, so that more than one bypass group can fit in the module series direction, $N_{S_{MAX}}$ is reduced until it can be divided evenly by N_{BP} . In other words, $K = \text{an integer}$. The user then exits the flowchart. Note that since $N_{S_{MAX}}$ is reduced, the module series dimension will also be reduced. If the user wishes to preserve the module size, he should use design option 5 or 6 instead of 1 or 3.

If N_{BP} is larger than $N_{S_{MAX}}$, the algorithm will attempt to snake the bypass group; i.e., one bypass group will be arranged in two rows. If N_{BP} is an odd number, it is reduced to the next lower even number. $N_{G_{MAX}}$ is revised and a new K is obtained. If $K = 1$, the user exits the flowchart. If K is not equal to one, the size of K is assessed. For $K < 0.5$, N_{BP} is reduced by two, $N_{G_{MAX}}$ and K are recalculated and the size of K is again assessed. This procedure will keep N_{BP} an even number while reducing it to no more than twice $N_{S_{MAX}}$.

If K is equal to or greater than 0.5, a new variable N_{S_2} is obtained, equal to twice $N_{S_{MAX}}$, the rest of the algorithm will make $N_{S_2} = N_{BP}$ by reducing N_{S_2} in steps of two until $K = N_{S_2}/N_{BP} = 1$. In a subsequent flowchart, the fact that N_{S_2} was obtained will signal the algorithm that the bypass group was snaked so that this may be considered in determining the design for the parallel direction.

Table 2-8 illustrates a typical example in which K is not an integer so that the algorithms in the figure 2-17 flowchart must be used. In this example, the bypass group is eventually snaked.

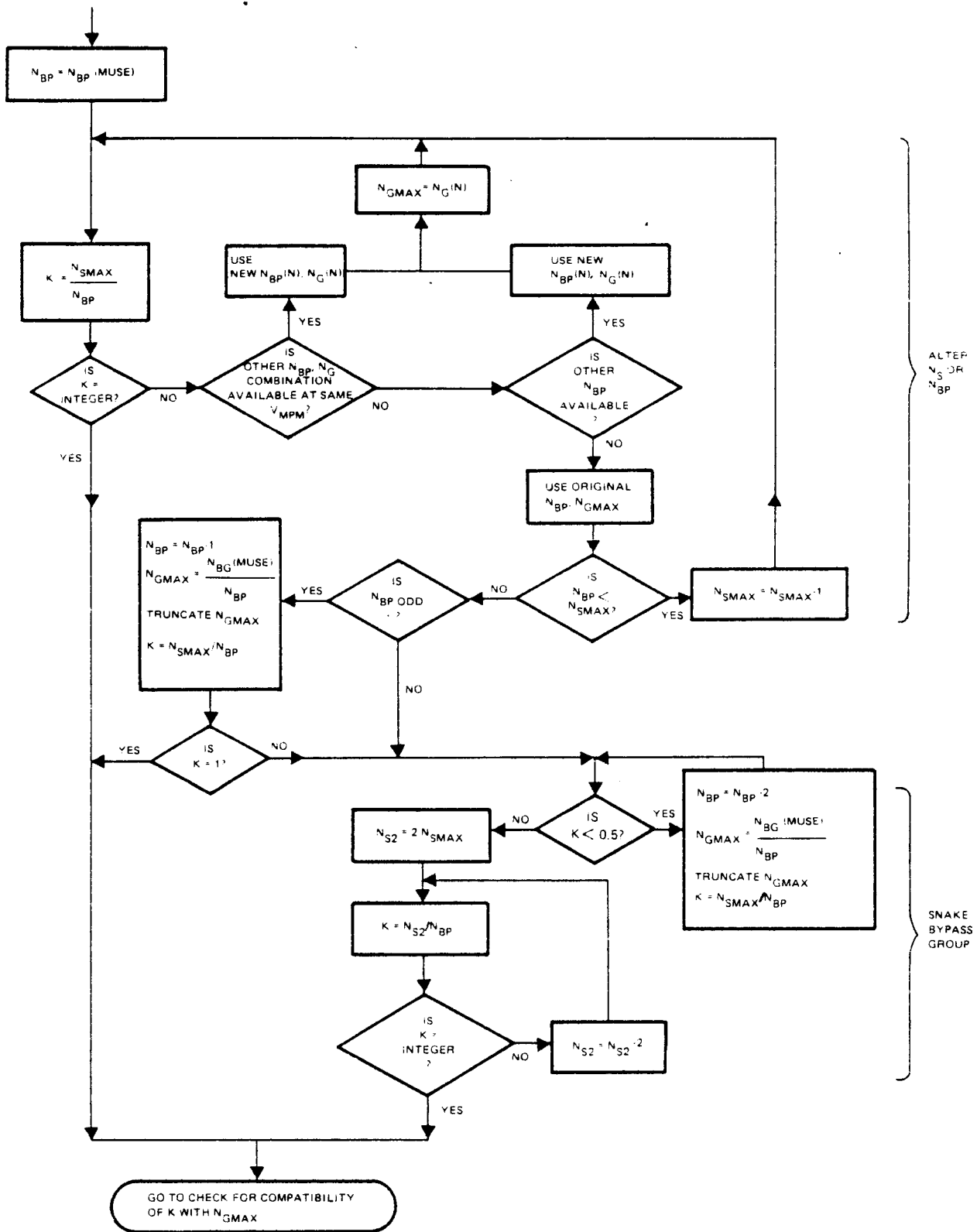


Figure 2-17. Flowchart for Selection of Acceptable N_S and N_{BP} Combination for Design Options 1 and 2

TABLE 2-8. TYPICAL EXAMPLE FOR K NOT AN INTEGER

Assume: $N_{BP} = N_{BP}(1) = 12$, $NG_{MAX} = NG(1) = 2$, $N_{BG}(1) = 24$

$N_{BP}(2) = 12$, $NG(2) = 1$, $N_{BG}(2) = 12$, $N_{S_{MAX}} = 5$

Enter Check for Divisibility of $N_{S_{MAX}}$ by N_{BP}

+ Calculation	-	$K = N_{S_{MAX}}/N_{BP}$
* Results	-	$K = 5/12$
+ Decision	-	Is K Integer? = NO
+ Decision	-	Other N_{BP} , NG Available at Same V_{MPM} ? = NO
+ Decision	-	Other N_{BP} , NG Available? = YES
+ Calculation	-	$N_{BP} = N_{BP}(2)$, $NG_{MAX} = NG(2)$
* Results	-	$N_{BP} = 12$, $NG_{MAX} = 1$
+ Calculation	-	$K = N_{S_{MAX}}/N_{BP}$
* Results	-	$K = 5/12$
+ Decision	-	Is K Integer? = NO
+ Decision	-	Other N_{BP} , NG Available at Same V_{MPM} ? = NO
+ Decision	-	Other N_{BP} , NG Available? = NO
+ Calculation	-	Set N_{BP} , NG_{MAX} to Original Values
* Results	-	$N_{BP} = 12$, $NG_{MAX} = 2$
+ Decision	-	Is $N_{BP} < N_{S_{MAX}}$? = NO
+ Decision	-	Is N_{BP} Odd? = NO
+ Decision	-	Is $K < 0.5$? = YES
+ Calculation	-	$N_{BP} = N_{BP}-2$; $NG_{MAX} = \text{Truncate } [N_{BG}(\text{MUSE})/N_{BP}]$; $K = N_{S_{MAX}}/N_{BP}$ (Increasing K to 0.5)
* Results	-	$N_{BP} = 10$, $NG_{MAX} = 2$, $K = 0.5$
+ Decision	-	Is $K < 0.5$? = NO
+ Calculation	-	$N_{S2} = 2 N_{S_{MAX}}$; $K = N_{S2}/N_{BP}$ (Snaking Bypass Group)
* Results	-	$N_{S2} = 10$, $K = 1$
+ Decision	-	Is K Integer? = YES

Go to Check for Compatibility of K with NG_{MAX}

This formalized procedure works well for the computer application. The user who applies the algorithm by hand, however, should not feel obliged to follow the algorithm exactly if he can find a more creative solution. For example, if the ratio K is $7/8$, the algorithm would lead him to first obtain $N_{S2} = 14$; then, reduce N_{S2} in steps of two until $N_{S2} = 8$. The user may prefer, instead, to reduce N_{BP} to 7 so that $N_{BP} = N_{SMAX}$ ($K = 1$). In this case, N_{BP} need not be snaked but will fit in N_{SMAX} and no reduction in module length will result.

Both an overview flowchart (figure 2-18) and a more detailed flowchart (figure 2-19) are provided for the next section of the methodology to assist the user in understanding both the concepts and the mechanics of the algorithms.

In the first block, K is compared with N_{GMAX} . Previously, the number of cells in a bypass group (N_{BP}) was compared to the number of cells in the series direction (N_{SMAX}). The integer, K , was obtained which represents the number of bypass groups which can fit in the series direction. Now this number, K , is compared with N_{GMAX} , the maximum number of bypass groups needed in series to produce V_{MPM} . In other words, the number of cells needed in series (N_{BG}) to produce V_{MPM} is compared with the number of cells needed in the series direction (N_{SMAX}). If K is greater than N_{GMAX} , the user takes the right branch and divides K by N_{GMAX} . If the value is less than two, N_{SMAX} will be reduced until $K = N_{GMAX}$ and the user will go to the flowchart for $K = N_{GMAX}$. If K/N_{GMAX} is greater than two, the result, called N_R , will be reduced to an integer. N_R represents the number of series strings (N_{BG}) producing V_{MPM} which can fit in the series direction. These will be connected in parallel. Thus, $N_R > 1$ represents paralleling in the series direction. The parallel interconnections may be made at the cell level, at the bypass group level, or at the whole series string level, but the total number of cells arranged in the series direction (N_S) is N_R times the number of cells in the series string (N_{BG}). Thus, the current from the cells in the series direction is N_R times the single cell current. The user then goes to the N_{MMIN} test flowchart.

Going back to the first block in figure 2-18, if K is less than or equal to N_{GMAX} , the lower branch is taken. If N_{S2} was previously obtained or if $K = N_{GMAX}$, the user goes to the flowchart containing the $K = N_{GMAX}$ and the N_{S2} routines. Otherwise, the user continues downwards. In this part, $K < N_{GMAX}$ so that all the cells needed in series cannot fit in the series direction. Therefore, the algorithm will attempt to snake the series strings so that integral numbers of bypass groups will be turned back in the opposite direction as often as needed.

First, the number of cells which will fit in the parallel direction, N_{PMAX} , is checked. If $N_{PMAX} = 1$, no snaking will be done. Instead, all N_{BG} cells will be put in the series direction and the series length of each cell (L_{CS}) will be reduced to prevent exceeding the maximum module length L_{MSMAX} . The user then goes to the N_{MMIN} test routine.

If N_{PMAX} is not equal to one, the number of snake sections (J) will be determined. If J is not an integer (if the N_{BG} cells cannot be divided integrally into N_{SMAX} groups), N_{SMAX} is reduced in steps of N_{BP} to obtain an integral J . Then, the algorithm checks if N_{PMAX} is divisible by J . If the result (N_M) is

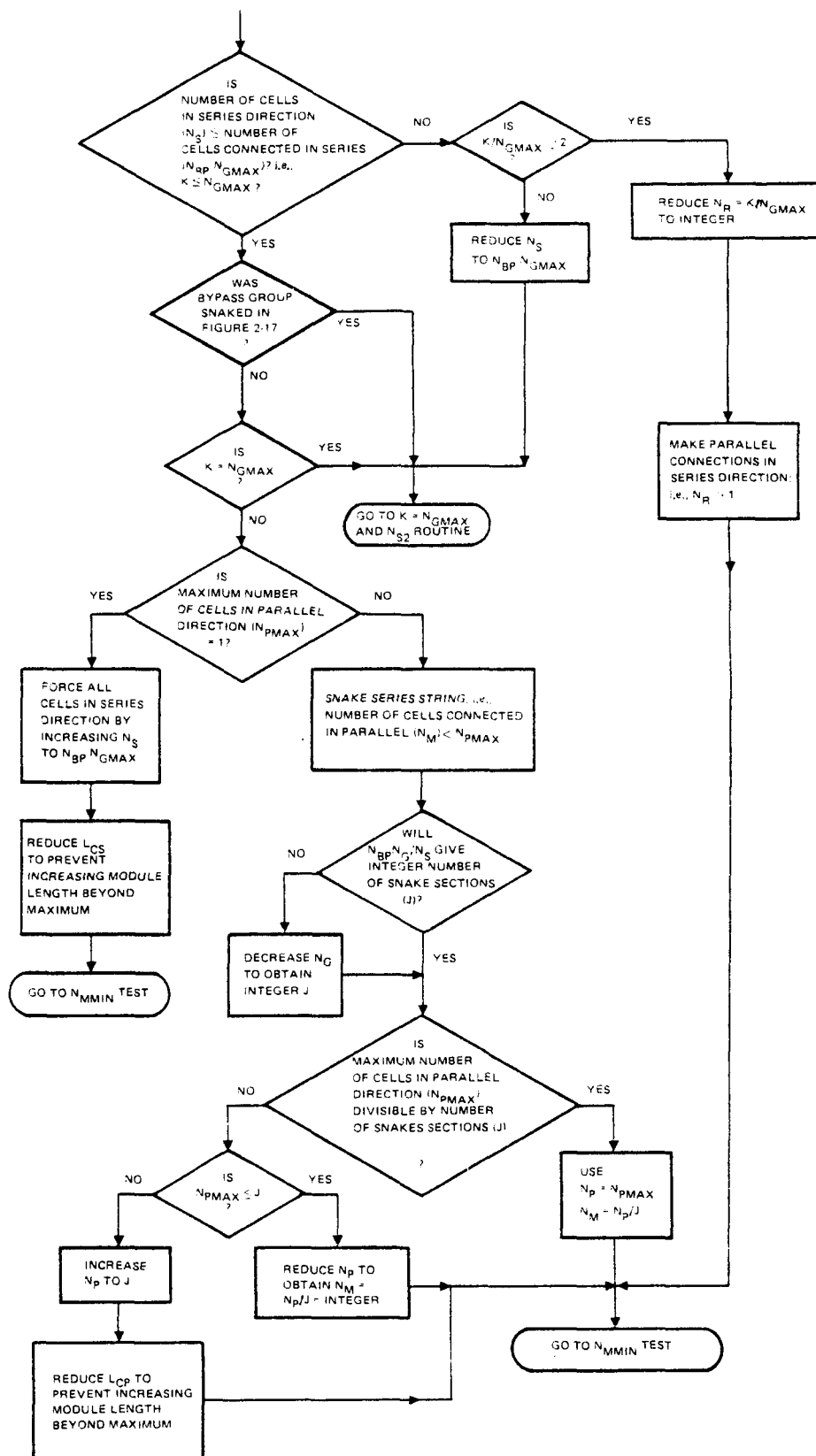


Figure 2-18. Overview Flowchart for Snaking N_{BG} or Paralleling in Series Direction and/or Altering N_S and N_P for Design Options 1 and 3

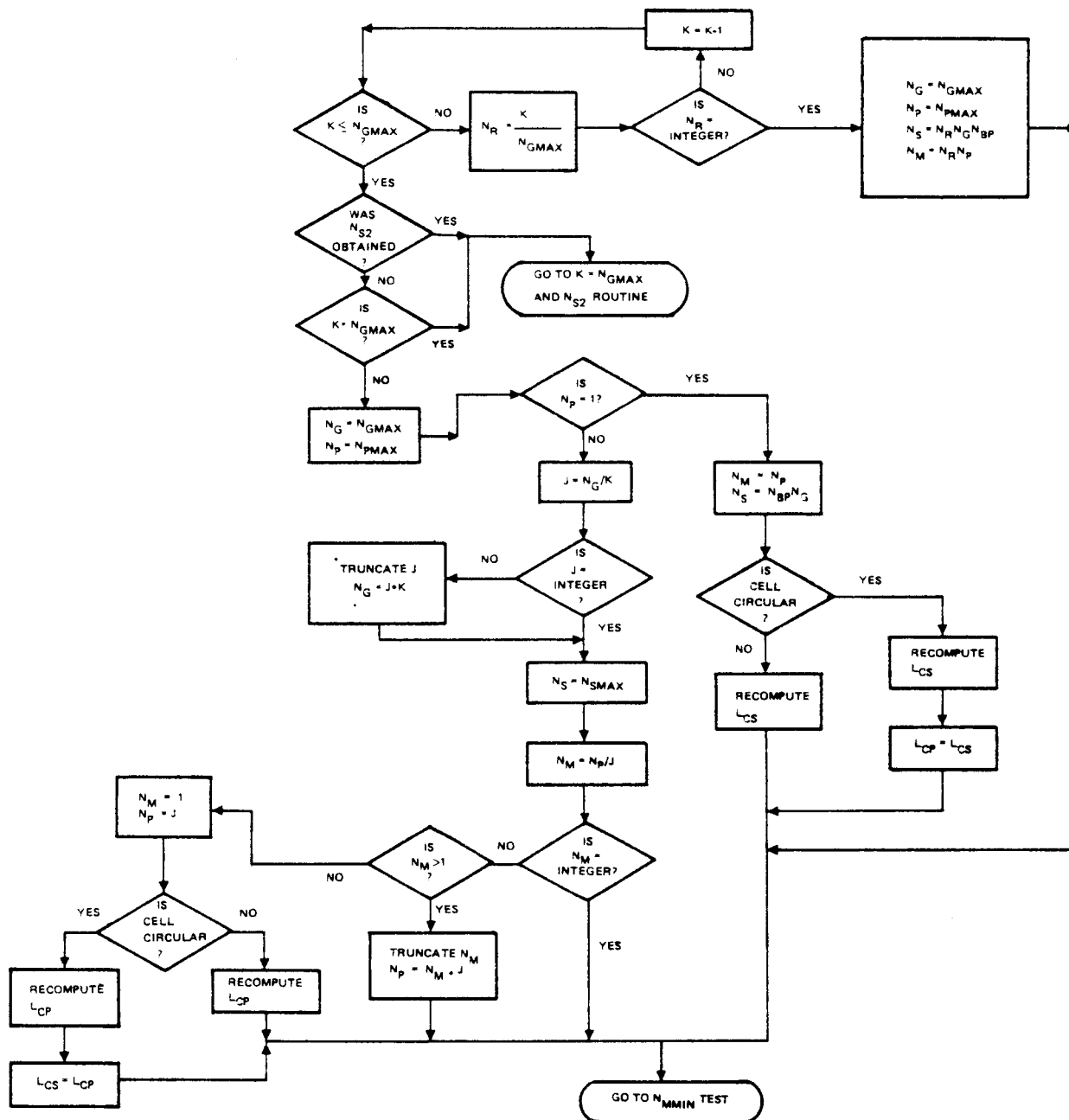


Figure 2-19. Detailed Flowchart for Snaking N_{BG} or Paralleling in Series Direction and/or Altering N_S and N_P for Design Options 1 and 3

an integer, each series string will have J snake sections and the number of strings connected in parallel (N_M) will be N_{PMAX}/J . The user then goes to the N_{MMIN} test routine.

If N_M is not an integer and the number of cells which fit in the parallel direction (N_{PMAX}) is greater than the number of snake sections (J) needed, N_p is reduced to make N_M an integer and the module parallel length is thus reduced. If N_{PMAX} is less than J , N_p is increased to J so that $N_M = 1$ and the cell parallel length must be reduced to prevent exceeding the maximum module length, L_{MPMAX} . Following each of these sections, the user goes to the N_{MMIN} test routine.

The detailed flowchart in figure 2-19 provides the mechanics for implementing the algorithm concepts discussed in figure 2-18. For $K > N_{GMAX}$, the condition for N_R less than two is handled by the test for integer N_R . If $N_R < 2$, reducing K in steps of one will eventually produce $K = N_{GMAX}$; whereas, if $N_R > 2$, reducing K in steps will produce an integer N_R with $K > N_{GMAX}$.

In the portions of the algorithm where L_{CS} or L_{CP} must be reduced, the detailed algorithm checks for circular or rectangular cells. Different equations are used for each. The cell length equations for both circular and rectangular cells are provided in table 2-9. The equations were obtained by solving equations 2-12, 2-13, 2-14 and 2-15 for L_{CS} or L_{CP} , as appropriate. The equation for L_{CP} for circular cells results from the binomial solution of equation 2-15 for L_{CP} . (Note: a , b , c are not the same as A , B , C .) If the cells are circular, the series and parallel lengths must be made equal. Therefore, preventing one module length from exceeding its maximum (either series or parallel) with circular cells results in reducing the other module length below its maximum.

Examples of the use of the concepts from figures 2-18 and 2-19 are contained in tables 2-10 and 2-11. The condition in which $K > N_{GMAX}$ requiring paralleling in the series direction is demonstrated in table 2-10. Table 2-11 contains the opposite conditions in which $K < N_{GMAX}$ requiring snaking of the series string.

Both an overview flowchart describing the algorithm concepts (figure 2-20), and a more detailed flowchart describing the algorithm mechanics (figure 2-21) are provided for the next portion of the methodology. These flowcharts consider either the case in which $K = N_{GMAX}$ or the case in which N_{S2} was obtained via figure 2-17. For $K = N_{GMAX}$, the left branch is followed. This is the simplest case possible. No snaking or paralleling in the series direction is required. Therefore, $N_S = N_{SMAX}$, $N_{BG} = N_S$, $N_p = N_{PMAX}$ and $N_M = N_p$. The user then goes to the N_{MMIN} test routine.

If N_{S2} was previously obtained, the algorithm in figure 2-20 and 2-21 attempts to continue snaking the series string by half bypass groups so that the number of snake sections (J) in the series string is twice the number of bypass groups (N_G). If N_{PMAX} is greater than J , the algorithm attempts to place additional series strings in parallel ($N_M > 1$).

Stepping through the algorithm for snaking the bypass group, first N_S is set to one half N_{S2} and N_M is obtained by dividing N_{PMAX} by $2N_G$. If N_M is an

TABLE 2-9. EQUATIONS FOR RECOMPUTING L_{CS} AND L_{CP}
IN FIGURES 2-19 AND 2-20 FOR DESIGN
OPTIONS 1 AND 3

For Rectangular Cells

$$L_{CS} = \frac{L_{MSMAX} - 2\Delta_{SES} - (N_S - 1) \Delta_{SS}}{N_S} \quad \text{from Eq. 2-12}$$

$$L_{CP} = \frac{L_{MPMAX} - 2\Delta_{SEP} - (N_P - 1) \Delta_{SP}}{N_P} \quad \text{from Eq. 2-13}$$

For Circular Cells

$$L_{CS} = \frac{L_{MSMAX} - 2\Delta_{SES} - (N_S - 1/2) \Delta_{SS}}{(N_S + 1/2)} \quad \text{from Eq. 2-14}$$

$$\text{or } L_{CP} = \frac{-B - \sqrt{B^2 - 4AC}}{2A} \quad \text{from Eq. 2-15}$$

where

$$A = 1 - 3 (N_P - 1)^2 / 4$$

$$B = -2 (L_{MSMAX} - 2\Delta_{SEP}) + [(N_P - 1)^2 (\Delta_{SS} - 2\Delta_{SP})]$$

$$C = (L_{MP} - 2\Delta_{SEP})^2 - [(N_P - 1)^2 (\Delta_{SP}^2 - \Delta_{SS}^2 / 4)]$$

TABLE 2-10. TYPICAL EXAMPLE FOR $K > N_{GMAX}$

Assume: $N_{BP} = 10$, $N_{GMAX} = 4$, $N_{BG} = 40$, $N_{SMAX} = 90$,

$$K = N_{SMAX}/N_{BP} = 9, N_{PMAX} = 2$$

Enter Check for Compatibility of K with N_{GMAX}

+ Decision	-	Is $K \leq N_{GMAX}$? = NO
+ Calculation	-	$N_R = K/N_{GMAX}$ (Paralleling in Series Direction)
* Results	-	$N_R = 2.25$
+ Decision	-	Is N_R Integer? = NO
+ Calculation	-	$K = K-1$
* Results	-	$K = 8$
+ Decision	-	Is $K \leq N_{GMAX}$? = NO
+ Calculation	-	$N_R = K/N_{GMAX}$
* Results	-	$N_R = 2.0$
+ Decision	-	Is N_R Integer? = YES
+ Calculation	-	$N_G = N_{GMAX}$; $N_P = N_{PMAX}$; $N_S = N_R N_G N_{BP}$; $N_M = N_R N_P$
* Results	-	$N_G = 4$; $N_P = 2$; $N_S = 80$; $N_M = 4$

Go to N_{MMIN} Test

TABLE 2-11. TYPICAL EXAMPLE FOR $K < N_{GMAX}$

Assume: $N_{BP} = 10$, $N_{GMAX} = 7$, $N_{BG} = 70$, $N_{S2} = 0$, $N_{SMAX} = 20$,

$N_{PMAX} = 6$, $K = N_{SMAX}/N_{BP} = 2$

Enter Check for Compatibility of K with N_{GMAX}

+ Decision	-	Is $K \leq N_{GMAX}$? = YES
+ Decision	-	Was N_{S2} obtained? = NO
+ Decision	-	Is $K = N_{GMAX}$? = NO
+ Calculation	-	$N_G = N_{GMAX}$; $N_p = N_{PMAX}$
* Results	-	$N_G = 7$, $N_p = 6$
+ Decision	-	Is $N_p = 1$? = NO
+ Calculation	-	$J = N_G/K$ (Snaking Series String)
* Results	-	$J = 3.5$
+ Decision	-	Is J Integer? = NO
+ Calculation	-	Truncate J; $N_G = J * K$
* Results	-	$J = 3$; $N_G = 6$
+ Calculation	-	$N_S = N_{SMAX}$; $N_M = N_p/J$
* Results	-	$N_S = 20$, $N_M = 2$
+ Decision	-	Is N_M Integer? = YES

Go to N_{MIN} Test

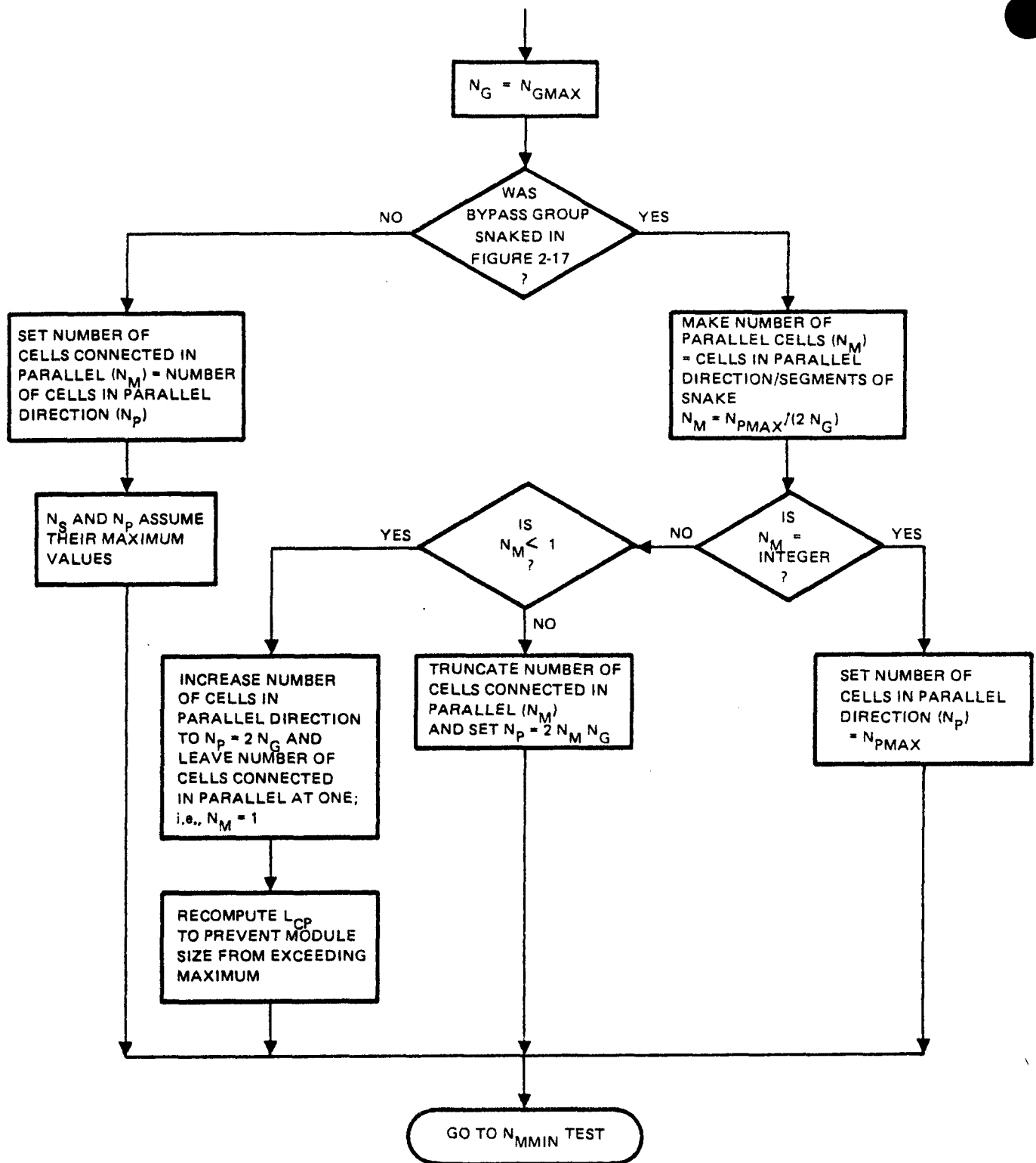


Figure 2-20. Overview Flowchart for Completing Design for $K = N_{GMAX}$ for Design Options 1 and 3

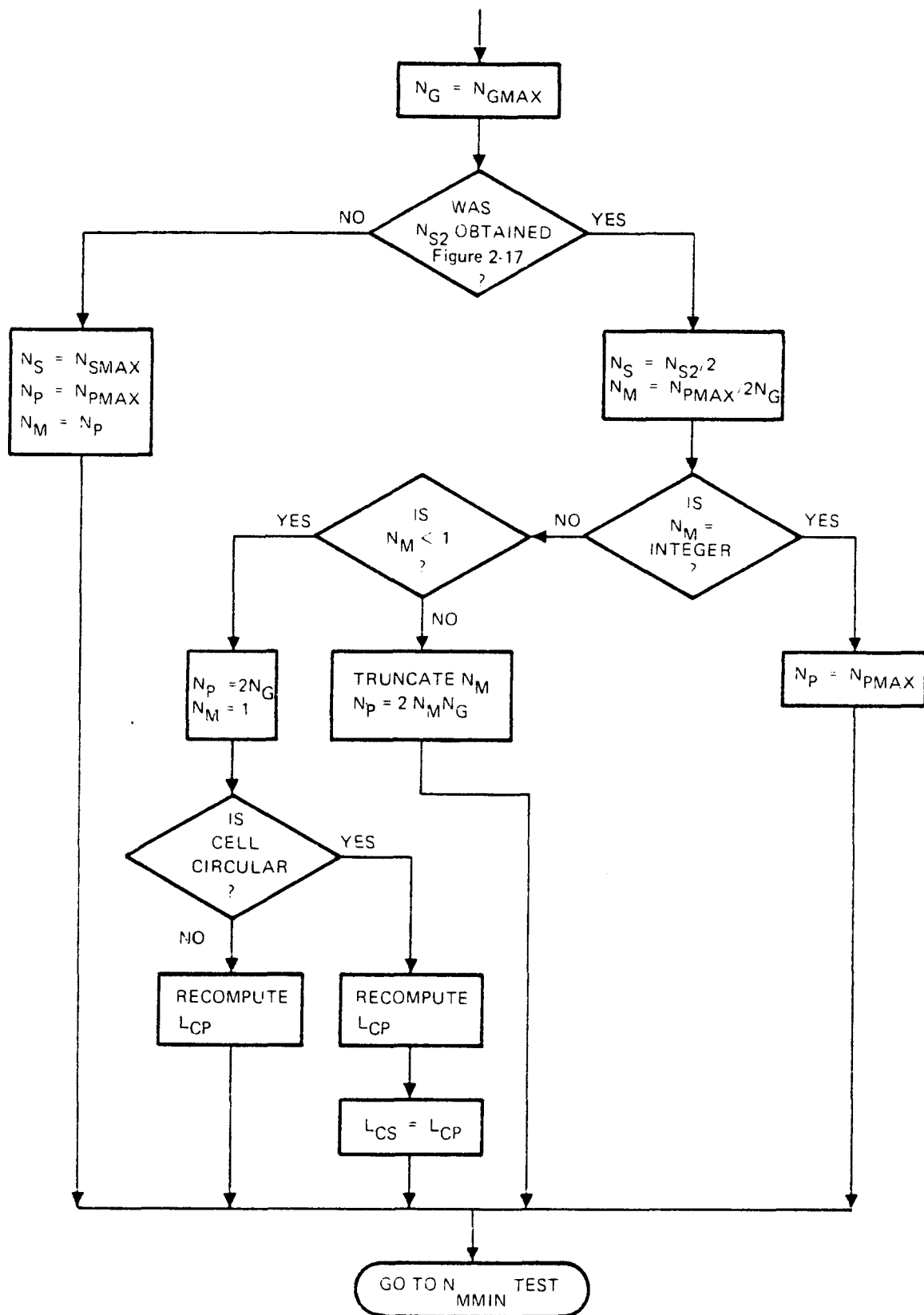


Figure 2-21. Detailed Flowchart for Completing Design for $K = N_{GMAX}$ for Design Options 1 and 3

integer, the design is simple with $N_p = N_{pMAX}$ and N_M as given. The user then goes to the N_{MMIN} test routine.

If N_M is not an integer but is greater than one, N_M is truncated and N_p is set to N_M times $2N_G$. Since N_p is less than N_{pMAX} , the module parallel length is thus reduced. If N_M is less than one, N_p is increased to $2N_G$. Thus, $N_M = 1$ and N_p is greater than N_{pMAX} . Therefore, the cell parallel length (L_{cp}) must be reduced to prevent exceeding the maximum module length (L_{MPMAX}). As before, different equations are used for circular versus rectangular cells given in table 2-9. If the cell is circular, L_{cs} must also be reduced to equal L_{cp} . Following each of these sections, the user then goes to the N_{MMIN} test routine.

An example illustrating the algorithm method for the condition in which N_{S2} was obtained is contained in table 2-12. Notice that, since $N_G = 2$, there are 4 sections in each series snake. Since $N_p = 8$, there are two snakes or series strings in parallel ($N_M = 2$).

The module design is now complete. The flowchart shown in figure 2-22 tests for parallel redundancy and calculates the final cell and module characteristics. If the value of N_M from figure 2-19 or 2-21 is greater than or equal to N_{MIN} , calculated from figure 2-12, the parallel redundancy criteria is satisfied. If it is not, the algorithm proceeds regardless, but the user may, if he chooses, reformulate the problem by designing for a lower voltage (V_{MPM}) which would take him back to figure 2-14 to select a different N_{BP} , N_G combination or by increasing the number of cell interconnects (N_{ACT}) which would take him back to figure 2-12 or by decreasing the cell dimensions or increasing the module dimensions which would take him back to figure 2-16. Other possibilities might also be available, such as using design option 2.

The user next calculates the actual module dimensions (L_{MS} and L_{MP}) based on cell lengths (L_{cs} and L_{cp}), numbers of cells in each direction (N_S and N_p), and the edge and internal spacings in each direction (Δ 's). Different equations are used for rectangular and circular cells. (Remember that circular cell rows overlap.) Next the packing factor is calculated. Then, the cell and module electrical characteristics are calculated using the equations in tables 2-4 and 2-5.

If the module maximum dimensions (L_{MSMAX} and L_{MPMAX}) input in figure 2-16 were not equal (square module), the user may wish to switch these dimensions and go back to figure 2-16 to obtain another design for the module. The entry point for the design procedure for the second option is shown in figure 2-15 where N_{SMAX} and N_{pMAX} are calculated. When the user is finished with Design Options 1 or 3, he may choose to go to the Module Conductor Requirements routine to calculate the required width and thickness of conductor runs for series and parallel connections within the module.

2.2.3 Design Option 2

Design Option 2 (overview flowchart in figure 2-23) is used when the user knows the module voltage and current and therefore, he also knows the total

TABLE 2-12. TYPICAL EXAMPLE FOR CONDITION OF N_{S2} OBTAINED

Assume: $N_{BP} = 10$, $N_{GMAX} = 2$, $N_{S2} = 10$, $N_{SMAX} = 5$, $N_{PMAX} = 9$

Enter Completing Design for $K = N_{GMAX}$ or N_{S2} Condition

+Calculation	-	$N_G = N_{GMAX}$
* Results	-	$N_G = 2$
+ Decision	-	Was N_{S2} Obtained? = YES
+ Calculation	-	$N_S = N_{S2}/2$; $N_M = N_{PMAX}/(2N_G)$
* Results	-	$N_S = 5$, $N_M = 2.25$
+ Decision	-	Is N_M Integer? = NO
+ Decision	-	Is $N_M < 1$? = NO
+ Calculation	-	Truncate N_M ; $N_P = 2 N_M N_G$
* Results	-	$N_M = 2$, $N_P = 8$

Go to N_{MMIN} Test

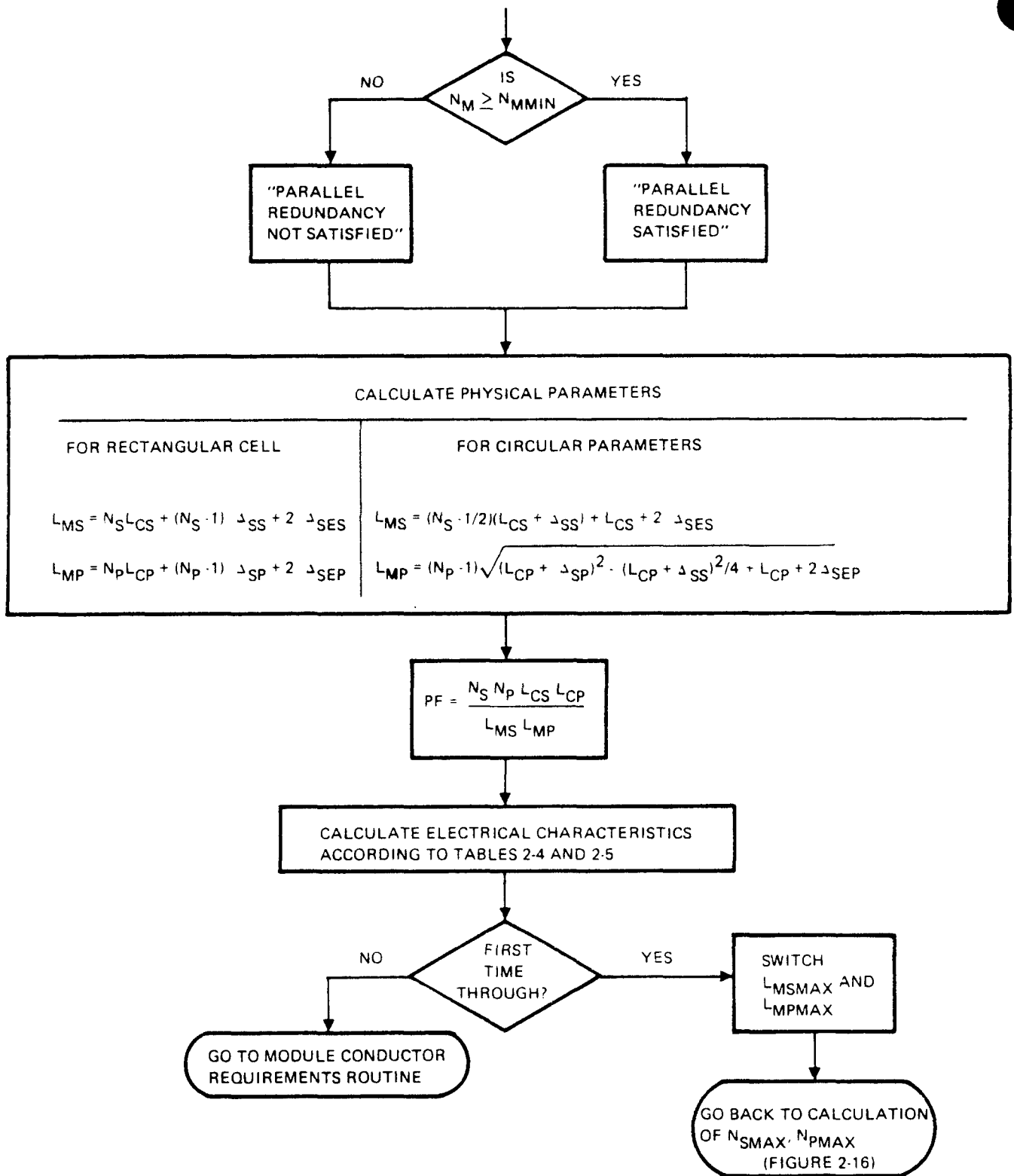


Figure 2-22. Flowchart for N_{MMIN} Check and Completion of Module Design for Design Options 1 and 3

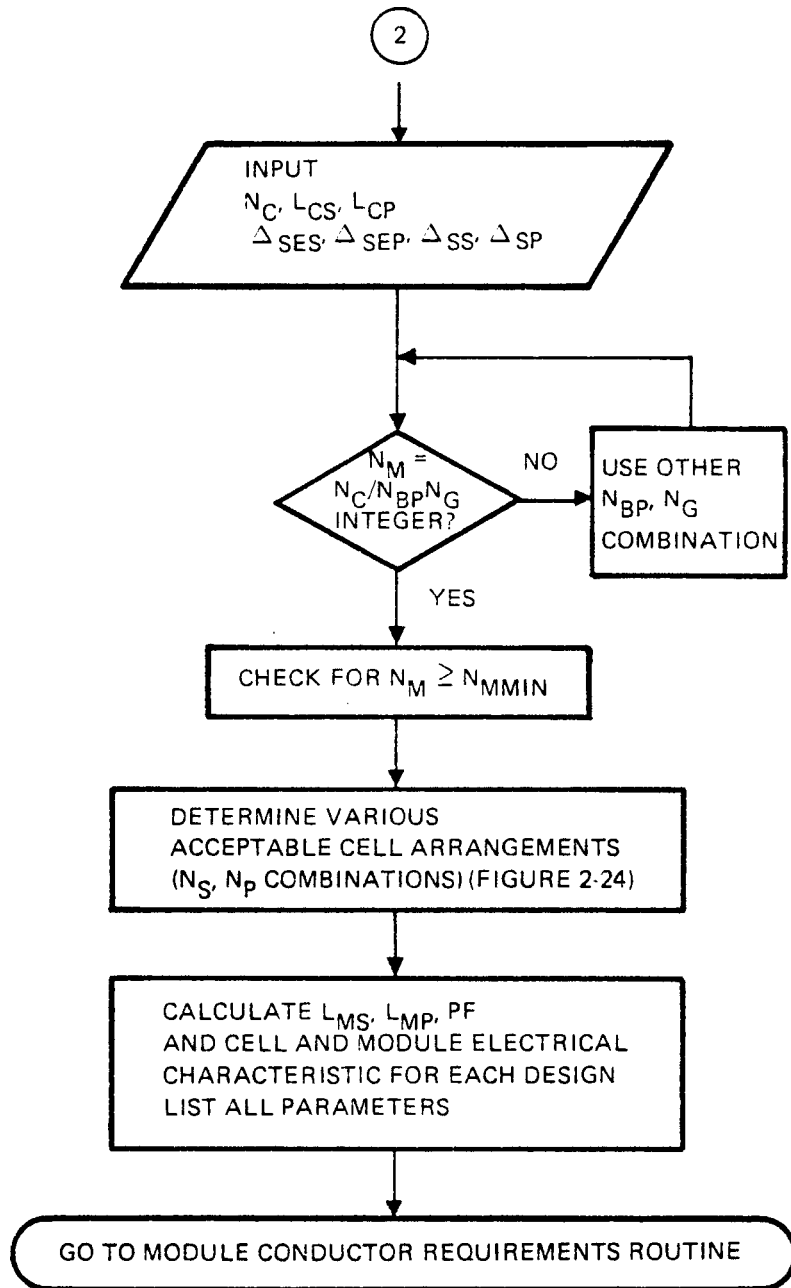


Figure 2-23. Overview Flowchart for Design Option 2

number of cells (N_C) in the module and the cell dimensions. He has already obtained N_{BP} and N_G from the main program; therefore, the number of cells in parallel (N_M) is obtained from $N_C/(N_{BP}N_G)$. His main objective is to determine module length and width options so that he can obtain the most desirable module aspect ratio and the lowest conductor requirements.

If the user is not satisfied with the N_{BP} , N_{GMAX} combination obtained in the main program, he may use another combination. N_C should be chosen to be divisible by the product of the N_{BP} and N_{GMAX} he has chosen. Assuming N_M is an integer, the user next checks for parallel redundancy. He may then go on or reformulate his inputs if $N_M < N_{MIN}$.

Following the parallel redundancy check, the user determines various acceptable cell arrangements by trying various multiples of N_{BP} for the N_S value. The procedure is described in the next flowchart (figure 2-24). If $N_G > 1$, the algorithm attempts to snake the series string. The user steps J , the number of sections of the snake, from two to N_G . N_S is then the number of cells in the series string divided by J . If N_S is an integer, N_p is determined by dividing N_C by N_S . This will also be an integer. N_S and N_p are catalogued and the user steps to the next J and repeats the N_S calculation.

If N_S is not an integer, no values are stored. Instead, the user immediately steps to the next J , and repeats the N_S calculation. Following the $N = N_G$ calculations, the user goes to the left branch to try paralleling in the series direction.

The user steps N_R , the number of parallel segments in the series direction, from one to $N_C/N_{BP}N_G$. At this point, all N_C cells will be arranged in the series direction so that the module is only one cell wide. For each N_R , N_S is determined as the series string times N_R . N_p is the total number of cells divided by N_S . If N_p is an integer, the N_S and N_p values are catalogued and the next N_R is used. If N_p is not an integer, the values are not stored but N_R is stepped to the next value.

After all options are catalogued, the user returns to the flowchart in figure 2-23. From the N_S and N_p values catalogued, the user calculates the module series and parallel lengths and packing factor from equations shown in figure 2-22 for rectangular or circular cells. The cell and module electrical characteristics are determined from the equations in tables 2-4 and 2-5. Since L_{CS} , L_{CP} , N_C and N_M are the same for all options, the electrical characteristics will not vary and need only be calculated once. But the module lengths will be different for each optional design and the packing factor will vary if the series and parallel spacings are not equal; i.e., Δ_{SES} not = Δ_{SEP} or Δ_{SS} not = Δ_{SP} .

Following completion of the calculations and cataloguing of the results, the user may go to the Module Conductor Requirements routine to determine the width and thickness of the conductor runs required for any or all design options. An example of the use of Design Option 2 is included in table 2-13. The table follows the algorithm through specification of the design options but does not calculate the physical characteristics, L_{MS} , L_{MP} and PF, for the designs as these are simple and straightforward.

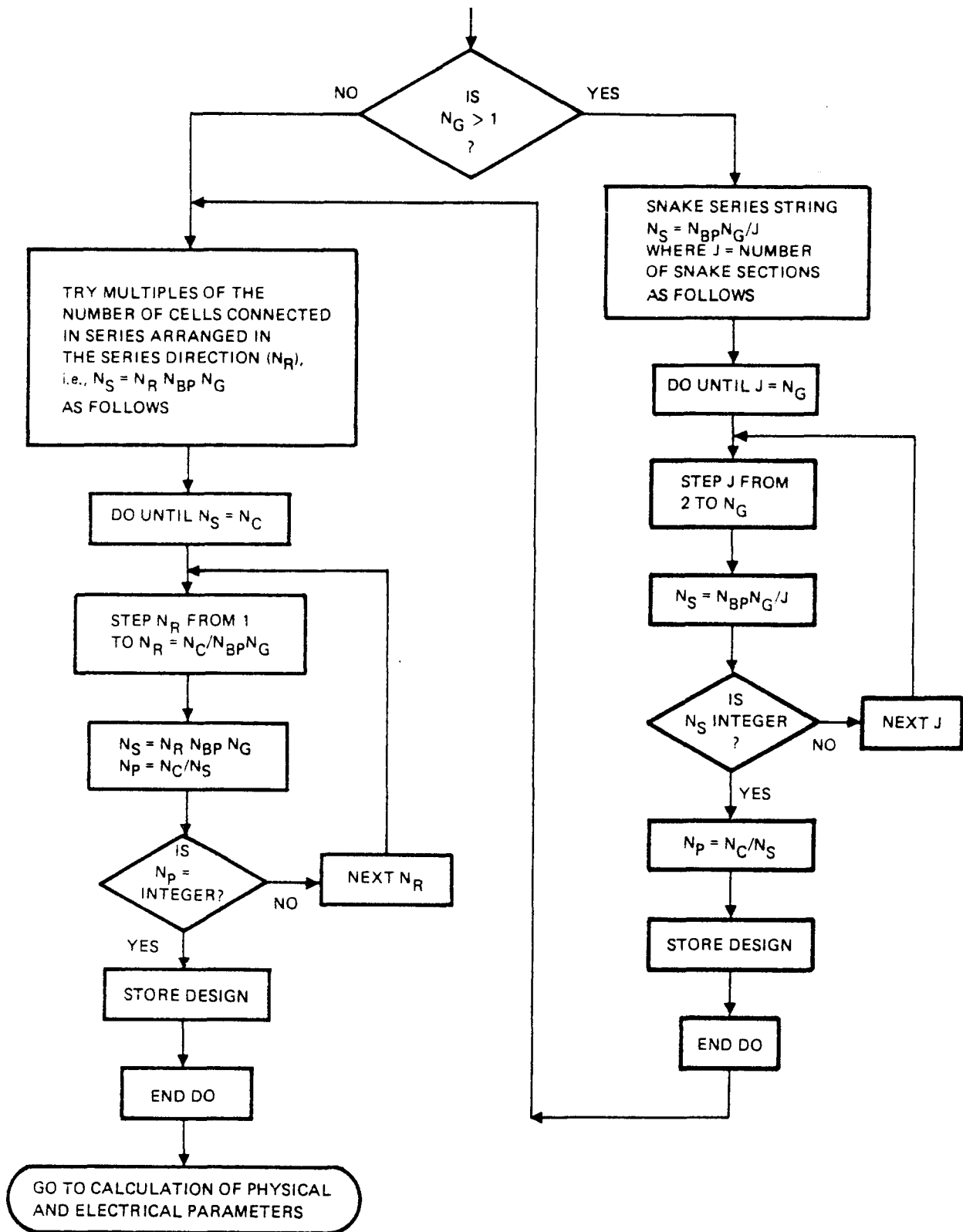


Figure 2-24. Detailed Flowchart for Determination of Various Acceptable Cell Arrangements for Design Option 2

TABLE 2-13. TYPICAL EXAMPLE FOR DESIGN OPTION 2

Assume: $N_{BP} = 6$, $N_{GMAX} = 2$, $N_{BGMAX} = 12$, $N_{MMIN} = 2$

Enter Design Option 2

• Input - $N_C = 24$, $L_{CS} = 5\text{cm}$, $L_{CP} = 10\text{cm}$
 $\Delta_{SES} = \Delta_{SEP} = 1.0\text{cm}$, $\Delta_{SS} = \Delta_{SP} = 0.2\text{cm}$

+ Calculate - $N_G = N_{GMAX}$; $N_M = N_C/N_{BP}N_G$

* Results - $N_G = 2$, $N_M = 2.0$

+ Decision - Is N_M Integer? = Yes

+ Decision - Is $N_M \geq N_{MMIN}$? = Yes

* Results - Parallel Redundancy Satisfied

+ Decision - Is $N_G > 1$? = Yes

+ Calculation - $N_S = N_{BP}N_G/J$ where $J = 2$; $N_p = N_C/N_S$ (Snaking Series String)

* Results - $N_S = 6$, $N_p = 4$ (Store as Design 1)

+ Calculation - Try Multiples of N_R ($N_R > 1$ means Paralleling in Series Direction)

+ Calculation - Determine N_R steps; $N_{RMAX} = N_C/N_{BP}N_G$

* Results - $1 \leq N_R \leq 2$ (Integer Values)

+ Calculation - $N_S = N_R N_{BP} N_G$ for $N_R = 1$; $N_p = N_C/N_S$

* Results - $N_R = 1$, $N_S = 12$, $N_p = 2$

+ Decision - Is N_p Integer? = Yes

* Results - Store Values as Design 2

+ Decision - Is $N_R = N_{RMAX}$? = No

+ Calculation - $N_R = N_R + 1$; $N_S = N_R N_{BP} N_G$; $N_p = N_C/N_S$

* Results - $N_R = 2$, $N_S = 24$, $N_p = 1$

+ Decision - Is N_p Integer? = Yes

* Results - Store Values as Design 3

+ Decision - Is $N_R = N_{RMAX}$? = Yes

Go To Calculations of L_{MS} , L_{MP} , PF and Electrical Parameters
 For All Three Designs

2.2.4 Design Option 4

Design Option 4 (overview flowchart in figure 2-25) was provided to design modules with resistance-limited cells; i.e., power losses in the cells due to

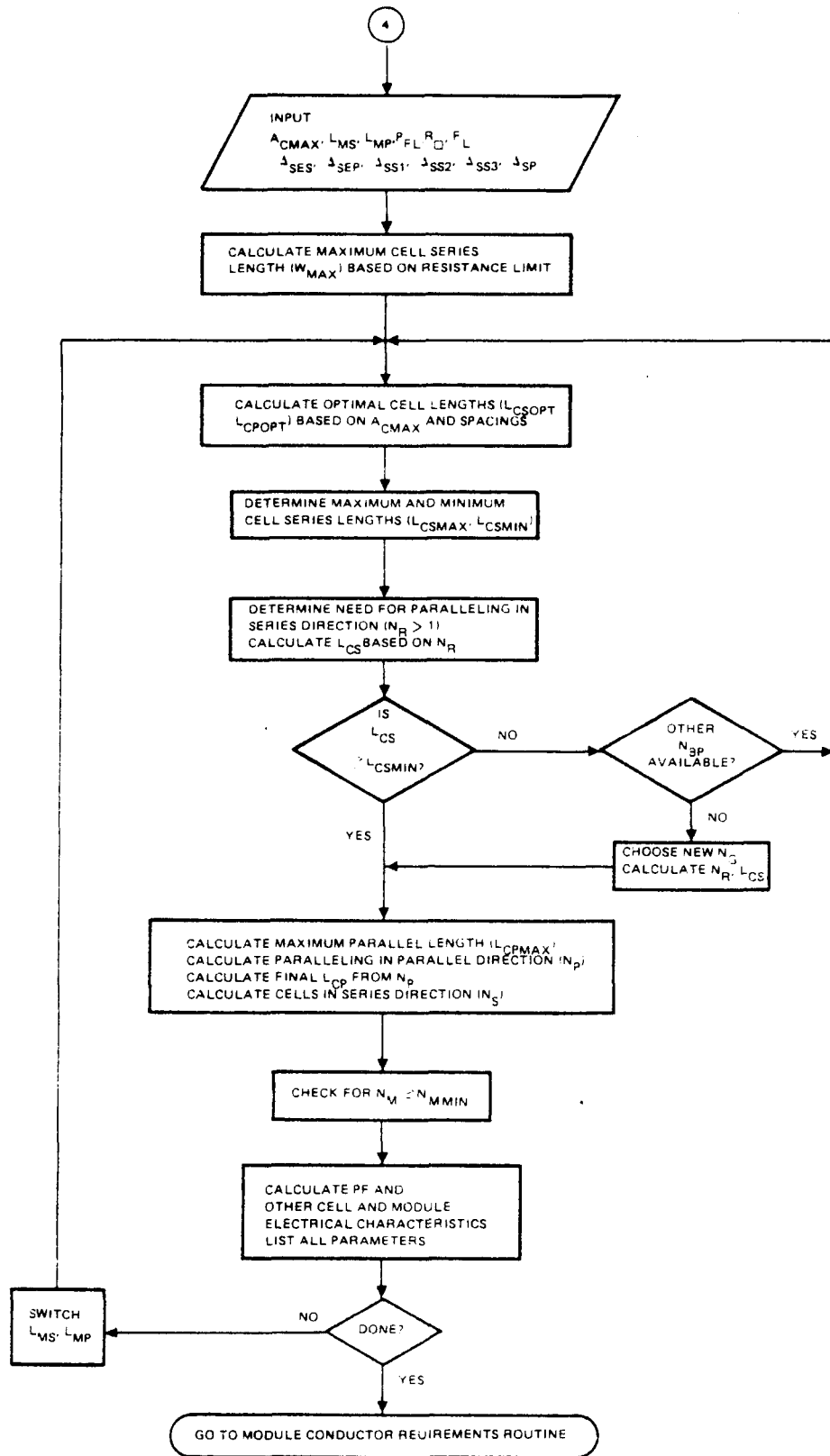


Figure 2-25. Overview Flowchart for Design Option 4

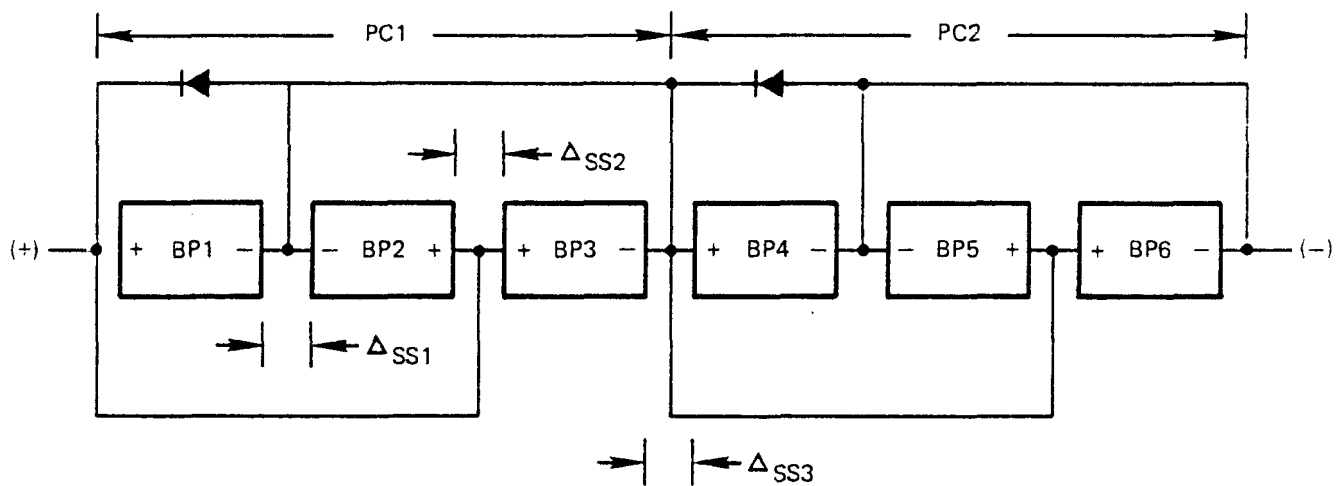
high resistivity current carriers force the user to limit one dimension in addition to the cell area. This condition often occurs in integrated cell technologies and it is specifically for this type of technology that Design Option 4 was created. To accommodate series-limited, non-integrated technologies, these algorithms can be altered by the user or the user can alter Design Options 1 or 5 to restrict the cell series length in addition to the cell area.

The user inputs maximum cell area and fixed module dimensions because it is assumed that module dimensions are constrained by the capabilities of the deposition process and the cell efficiency can not be maintained beyond a given area. The user also inputs the fractional power loss allowable for the cell (P_{FL}) and the sheet resistivity ($R_{\square}$) for the current-limiting conductor. From these, the maximum cell dimension in the series direction (cell width, W_{MAX}) will be calculated. The input F_L is the fractional lower limit on the series length specified by the user based on his experience with the cell technology and the desirable cell dimensions.

In addition to edge spacing in the series and parallel direction and interior parallel direction spacing, the user also inputs three interior series direction spacings (Δ_{SS1} , Δ_{SS2} and Δ_{SS3}), defined in figure 2-26. It is assumed that the integration results in overlapped series connections so that there is negligible spacing between series connected cells in a bypass group. However, in making series or parallel connections of bypass groups in the series direction, spacing is needed for metallization runs and for electrical stand-off. Accordingly, Δ_{SS1} is provided to represent the spacing required between negative ends of adjacent bypass groups which are connected to each other in parallel; Δ_{SS2} represents the corresponding spacing between position ends of adjacent bypass groups connected to each other in parallel; and Δ_{SS3} represents the spacing between the negative end of one bypass group and the positive end of the next when they are connected to each other in series. These definitions were made because the spacings required are the smallest for these combinations and, therefore, the packing factor will be the highest. It can be concluded from this, that when both series and parallel connections are required in the series direction, paralleling should be done first with adjacent bypass groups flip-flopped so that positive ends of one are adjacent to positive ends of the next and negative ends are also adjacent to negative ends. This eliminates the stand-off requirement since adjacent ends are at the same potential. In addition, an odd number of groups should be paralleled so that positive and negative ends will occur at the ends of the parallel segments, permitting direct series connections with no need for stand-off.

After all inputs are made, the maximum series length (W_{MAX}) is determined. Then, the optimum series and parallel lengths (L_{CSOPT} and L_{CPOPT}) are determined based on equations 2-17 and 2-18 modified for the integrated technology conditions in which $N_{BP} L_{CS}$ is substituted in place of L_{CS} in equation 2-20 because there is no spacing between series cells in a bypass group. In addition, Δ_{SS} is replaced by the average series spacing, $(\Delta_{SS1} + \Delta_{SS2})/2$. The maximum series length (L_{CSMAX}) is determined by comparing W_{MAX} with L_{CSOPT} and the minimum series length (L_{CSMIN}) is F_L times L_{CSMAX} .

The need for paralleling in the series direction is then determined from L_{CSMAX} and the actual series length (L_{CS}) is calculated from N_R , the number of



EACH BP = N_{BP} CELLS IN SERIES WITH NEGLIGIBLE SPACING

$BP1 || BP2 || BP3 = PC1$

$BP4 || BP5 || BP6 = PC2$

PC1 IS IN SERIES WITH PC2

$\therefore N_G = 2, N_R = 3$

Figure 2-26. Illustration of Integrated Technology with Paralleling in Series Direction

parallel groups in the series direction. If L_{CS} is no less than L_{CSMIN} , the user continues on to the calculation of the maximum parallel length (L_{CPMAX}). If L_{CS} is less than L_{CSMIN} , however, another value of N_{BP} must be chosen and the loop must be repeated starting with calculation of L_{CSOPT} until $L_{CS} \geq L_{CSMIN}$. If no other N_{BP} are available or if all are exhausted to no avail, a new N_G is chosen by iterating on N_G and calculating N_R and L_{CS} until $L_{CS} \geq L_{CSMIN}$.

Following determination of a satisfactory L_{CS} , the user calculates L_{CPMAX} and then N_p based on L_{CPMAX} . Finally, the actual parallel length (L_{CP}) is determined from N_p . N_S and N_M are then specified and the N_{MMIN} test is performed. The rest of the calculations and switching of module dimensions is analogous to design options 1 and 3.

As shown in the first detailed flowchart (figure 2-27), W_{MAX} is the first calculation made following input of the parameters previously discussed. The derivation of this equation (2-30) was shown in section 2.1.3.3. The user then determines L_{CSOPT} and L_{CPOPT} . Equations 2-17 and 2-18 have been modified for this by incorporating the additional spacings, Δ_{SS1} and Δ_{SS2} , in place of Δ_{SS} and by adding N_{BP} since there is effectively no spacing between cells in the integrated series connections within a bypass group.

L_{CSMAX} is set equal to the smaller of L_{CSOPT} or W_{MAX} . L_{CSMIN} is then F_L times L_{CSMAX} . The user then goes on to the next flowchart to determine the required N_R .

In the flowchart in figure 2-28, N_G is first set equal to N_{GMAX} to make the N_R equation easier to write. N_R is then determined based on L_{CSMAX} and the N_{BP} , N_G combination specified from the main routine. The equation for N_R was obtained by modifying equation 2-12 (module series length) for the integrated series connection technology using the conventions shown in figure 2-26. The resulting equation for L_{MS} is

$$L_{MS} = N_R N_G N_{BP} L_{CS} + N_G (N_R - 1) (\Delta_{SS1} + \Delta_{SS2}) / 2 + (N_G - 1) \Delta_{SS3} + 2 \Delta_{SES} \quad (2-33)$$

This equation was then solved for N_R . If N_R is an odd integer, L_{CSMAX} becomes L_{CS} and the user goes on to the L_{CPMAX} routine. Otherwise, N_R is increased to the next higher odd integer and L_{CS} is determined based on this N_R by replacing L_{CSMAX} with L_{CS} in the N_R equation above and solving for L_{CS} . This L_{CS} will be smaller than L_{CSMAX} .

Next, L_{CS} is compared with L_{CSMIN} . If L_{CS} is no less than L_{CSMIN} , the user goes on to the L_{CPMAX} routine. If L_{CS} is less than L_{CSMIN} , the user chooses another N_{BP} , N_G combination from the set obtained in the main routine and repeats the calculation of L_{CSOPT} in figure 2-27. The user continues through the loop until the L_{CSMIN} check is again made. If no other N_{BP} , N_G combinations are available or if all have been exhausted with all L_{CS} value less than L_{CSMIN} , the user goes to the N_G Iteration routine in the next flowchart.

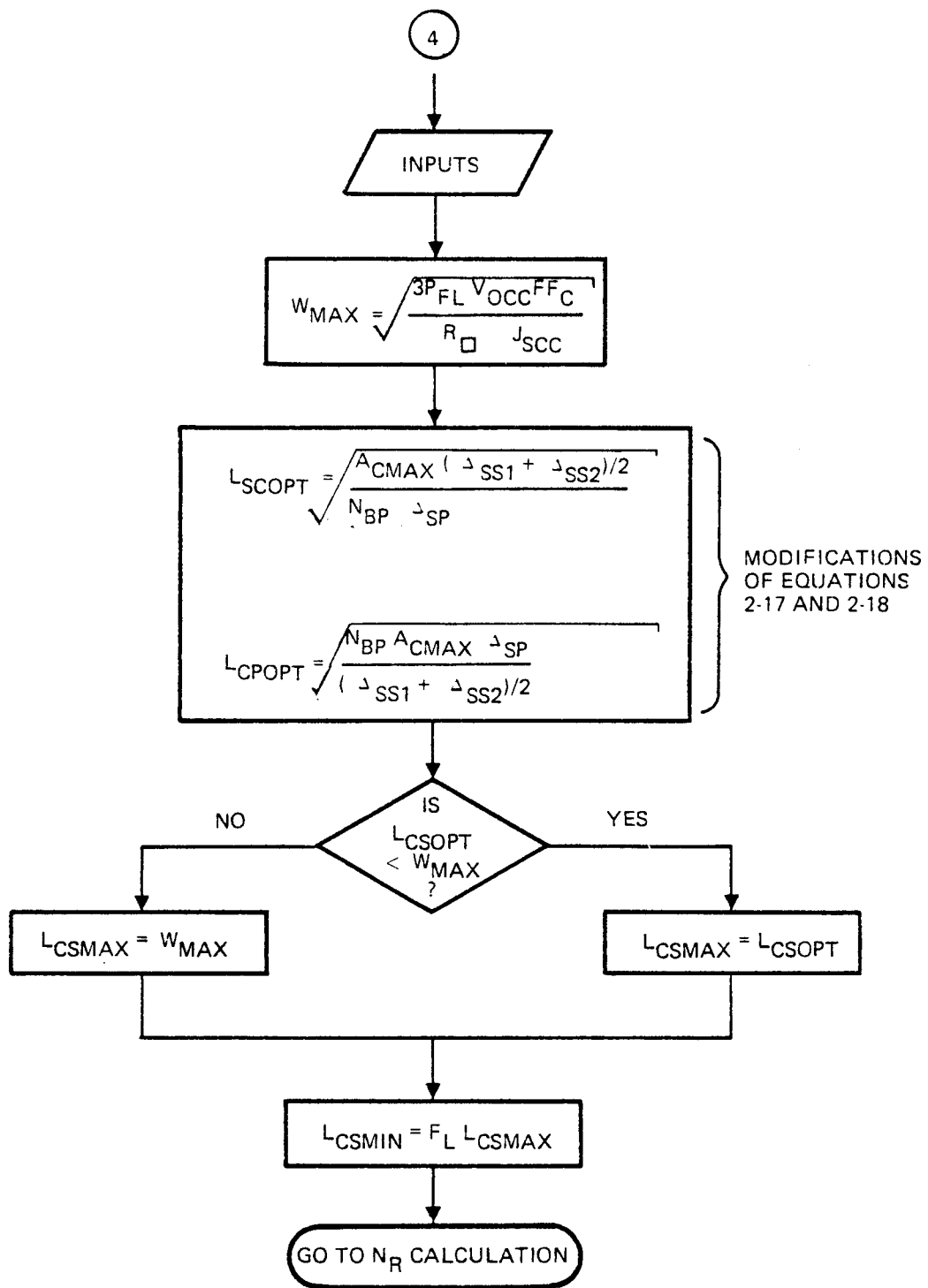


Figure 2-27. Flowchart for Determination of Cell Size Constraints for Design Option 4

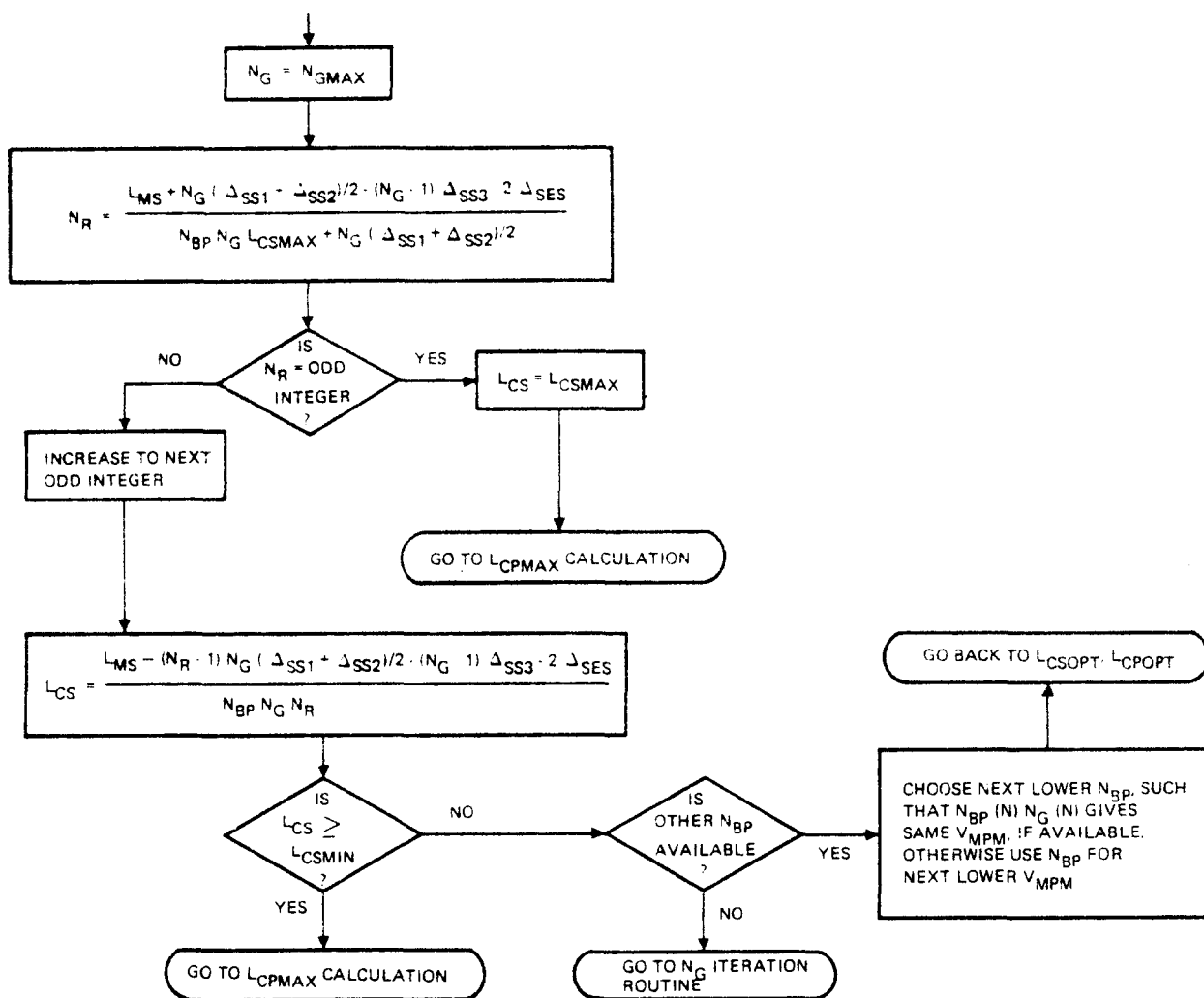


Figure 2-28. Flowchart for Determination of N_R and L_{CS} and L_{CSMIN}
Check for Design Option 4

The N_G Iteration routine in figure 2-29 attempts to find a combination of N_{bp} , N_G , and N_R which will produce a series cell length (L_{CS}) no smaller than L_{CSMIN} . This is accomplished by stepping N_G from 1 to N_{GMAX} using the original N_{bp} and calculating N_R and L_{CS} for each N_G . The largest value of L_{CS} is chosen from the N_{GMAX} possibilities and compared with L_{CSMIN} . If the L_{CSMIN} condition is satisfied, the user goes on to the L_{CPMAX} routine. If not satisfied, the user must reevaluate the problem. The value of F_L can be reduced or some other constraint may be changed.

Following a successful determination of L_{CS} , the user calculates L_{CPMAX} from the first block in figure 2-30 attempting to fully utilize the maximum cell area. The number of cells in the parallel direction (N_p) is then determined as shown from L_{CPMAX} . If N_p is not an integer, it is increased to the next higher integer. The final value of L_{cp} is then calculated based on integer N_p .

To obtain all parameters needed for completing the design, N_S and N_M are calculated as shown. Next, the N_{MMIN} check is made and the packing factor and electrical characteristics are calculated from tables 2-4 and 2-5. The module physical characteristics need not be determined since they were fixed in the input constraints. If the user wishes, he may switch L_{MS} and L_{MP} and return to figure 2-28 to obtain an alternate design. The user starts with $N_G = N_{GMAX}$ at the top of the flowchart. The calculations on the previous flowchart (figure 2-27) need not be repeated since they are independent of module dimensions. After the user is satisfied with the module designs obtained, he may go on to the Module Conductor Requirements routine.

Table 2-14 contains a typical example of the use of design option 4 for a case in which N_G iteration is not required. Table 2-15 contains an example of the use of the N_G iteration routine.

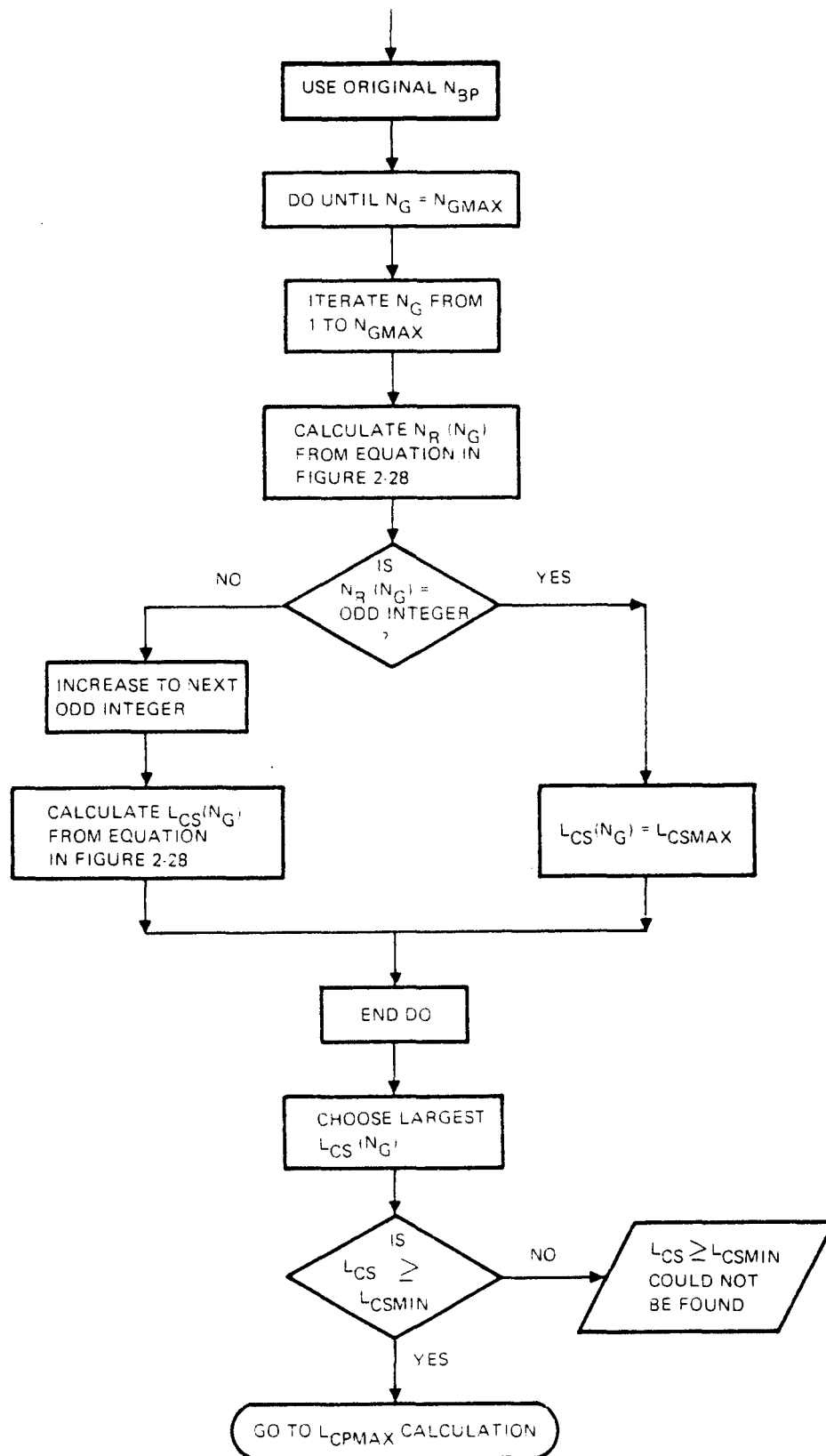


Figure 2-29. Flowchart for Iterating N_G When Solution Cannot Be Obtained with Allowable N_{BP} Values for Design Option 4

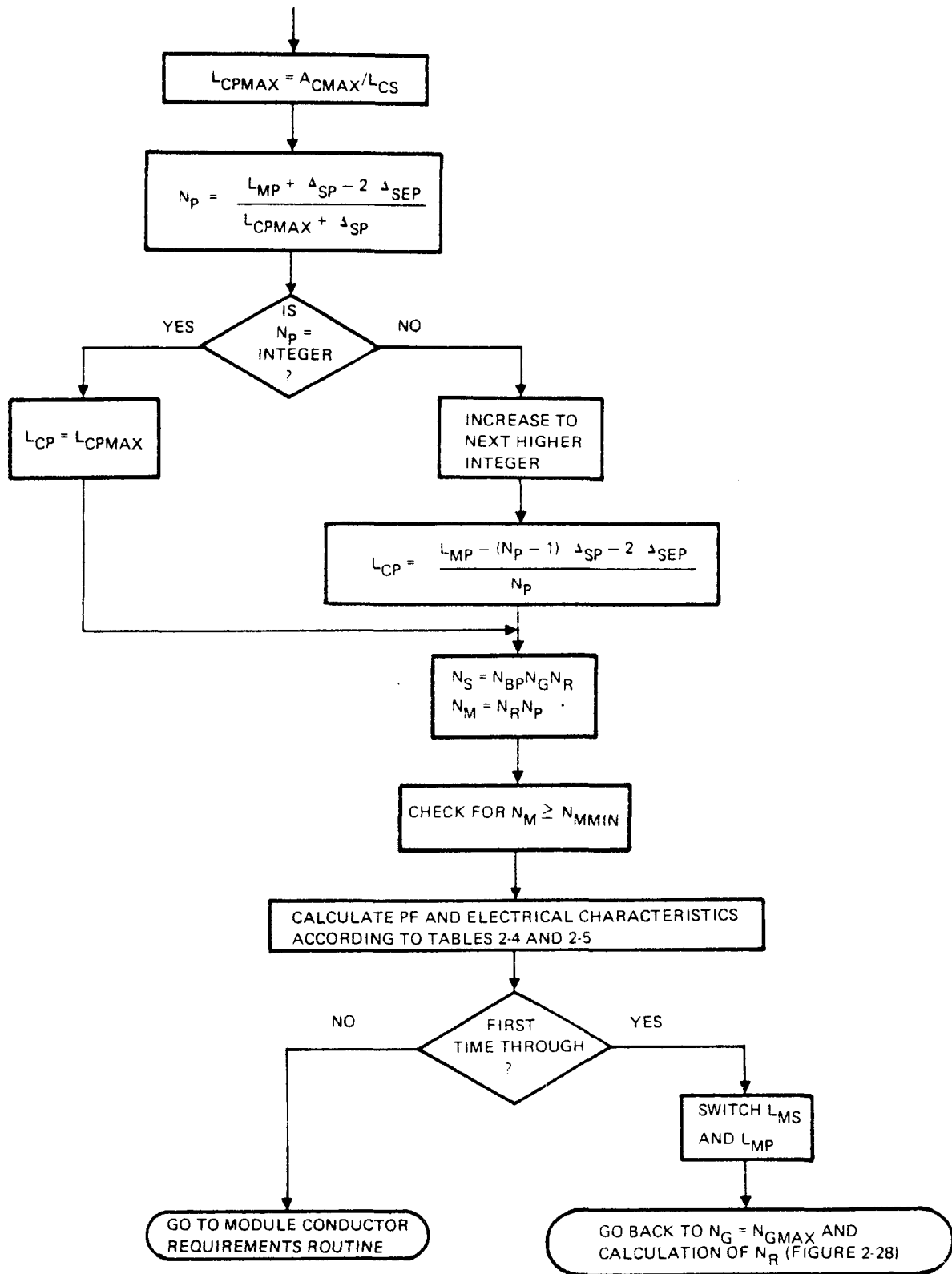


Figure 2-30. Flowchart for Parallel Parameters and Completion of Design Option 4

TABLE 2-14. TYPICAL EXAMPLE FOR DESIGN OPTION 4

Assume: $N_{BP} = 7$, $N_{GMAX} = 2$, $N_{MMIN} = 7$

$V_{OCC} = 0.91V$, $J_{SCC} = 16 \text{ mA/cm}^2$, $FF_C = 0.687$

Enter Design Option 4

. Input - $A_{CMAX} = 25.0 \text{ cm}^2$,
 $L_{MS} = 29.85 \text{ cm (11.75 in)}$, $L_{MP} = 120.65 \text{ cm (47.5 in)}$
 $P_{FL} = 0.05$, $R_{\square} = 1.0\Omega / \text{SQ}$, $F_L = 0.5$
 $\Delta_{SES} = \Delta_{SEP} = 0.953 \text{ cm (3/8 in)}$, $\Delta_{SS1} = 0.318 \text{ cm (1/8 in)}$,
 $\Delta_{SS2} = 0.635 \text{ cm (1/4 in)}$, $\Delta_{SS3} = 0.476 \text{ cm (3/16 in)}$
 $\Delta_{SP} = 0.079 \text{ cm (1/32 in)}$

+ Calculation - $W_{MAX} = \sqrt{\frac{3 P_{FL} V_{OCC} FF_C}{R_{\square} J_{SCC}}}$

$$L_{CSOPT} = \sqrt{\frac{A_{CMAX} (\Delta_{SS1} + \Delta_{SS2})/2}{N_{BP} \Delta_{SP}}}$$

$$L_{CPOPT} = \sqrt{\frac{N_{BP} A_{CMAX} \Delta_{SP}}{(\Delta_{SS1} + \Delta_{SS2})/2}}$$

* Results - $W_{MAX} = 2.421 \text{ cm}$, $L_{CSOPT} = 4.64 \text{ cm}$, $L_{CPOPT} = 5.39 \text{ cm}$

+ Decision - Is $L_{CSOPT} < W_{MAX}$? = NO .

+ Calculation - $L_{CSMAX} = W_{MAX}$; $L_{CSMIN} = F_L L_{CSMAX}$

* Results - $L_{CSMAX} = 2.421 \text{ cm}$; $L_{CSMIN} = 1.211 \text{ cm}$

Go to N_R Calculation

TABLE 2-14. TYPICAL EXAMPLE FOR DESIGN OPTION 4 (Concluded)

Enter N_R Calculation

+ Calculation - $N_G = N_{GMAX}$;

$$N_R = \frac{L_{MS} + N_G (\Delta_{SS1} + \Delta_{SS2})/2 - (N_G - 1)\Delta_{SS3} - 2\Delta_{SES}}{N_{BP} N_G L_{CSMAX} + N_G (\Delta_{SS1} + \Delta_{SS2})/2}$$

* Results - $N_G = 2, N_R = 0.82$

+ Decision - Is N_R Odd Integer? = No

+ Calculation - Increase N_R to Odd Integer;

$$L_{CS} = \frac{L_{MS} - (N_R - 1)N_G (\Delta_{SS1} + \Delta_{SS2})/2 - (N_G - 1)\Delta_{SS3} - 2\Delta_{SES}}{N_{BP} N_G N_R}$$

* Results - $N_R = 1, L_{CS} = 1.962 \text{ cm}$

+ Decision - Is $L_{CS} \geq L_{CSMIN}$? = Yes

Enter Parallel Parameters and Completion of Design

+ Calculation - $L_{CPMAX} = A_{CMAX}/L_{CS}$;

$$N_P = \frac{L_{MP} + \Delta_{SP} - 2\Delta_{SEP}}{L_{CPMAX} + \Delta_{SP}}$$

* Results - $L_{CPMAX} = 12.742 \text{ cm}, N_P = 9.3$

+ Decision - Is N_P Integer? = No

+ Calculation - Increase N_P to Integer;

$$L_{CP} = \frac{L_{MP} - (N_P - 1)\Delta_{SP} - 2\Delta_{SEP}}{N_P} ;$$

$$N_S = N_{BP} N_G N_R; N_M = N_R N_P$$

* Results - $N_P = 10, L_{CP} = 11.80 \text{ cm}, N_S = 14, N_M = 10$

Go to N_{MIN} Test and Calculation of Electrical Characteristics

TABLE 2-15. TYPICAL EXAMPLE FOR N_G ITERATION

Assume: $N_{BP} = 5$, $N_{GMAX} = 3$, $\Delta_{SS3} = 0.60$ cm

Other parameters as in Table 2-14

Enter N_G Iteration Routine

+ Calculation - Step N_G from 1 to N_{GMAX}

$$N_R(N_G) = \frac{L_{MS} + N_G(\Delta_{SS1} + \Delta_{SS2})/2 - (N_G - 1)\Delta_{SS3} - 2\Delta_{SES}}{N_{BP} N_G L_{CSMAX} + N_G(\Delta_{SS1} + \Delta_{SS2})/2}$$

* Results - $N_G = 1$, $N_R(1) = 2.26$

+ Decision - Is N_R Odd Integer? = No

+ Calculation - Increase N_R to Odd Integer;

$$L_{CS}(N_G) = \frac{L_{MS} - (N_R - 1)N_G(\Delta_{SS1} + \Delta_{SS2})/2 - (N_G - 1)\Delta_{SS3} - 2\Delta_{SES}}{N_{BP} N_G N_R}$$

* Results - $N_R(1) = 3$, $L_{CS}(1) = 1.799$ cm

+ Decision - Is $N_G = N_{GMAX}$? = No

+ Calculation - $N_G = N_G + 1$; Calculate $N_R(N_G + 1)$

* Results - $N_G = 2$, $N_R(2) = 1.13$

+ Decision - Is N_R Odd Integer? = No

+ Calculation - Increase N_R to Odd Integer; Calculate $L_{CS}(2)$

* Results - $N_R(2) = 3$, $L_{CS}(2) = 0.900$ cm

+ Decision - Is $N_G = N_{GMAX}$? = No

+ Calculation - $N_G = N_G + 1$; Calculate $N_R(N_G + 1)$

* Results - $N_G = 3$, $N_R(3) = 0.75$

+ Decision - Is N_R Odd Integer? = No

+ Calculation - Increase N_R to Odd Integer, Calculate $L_{CS}(3)$

TABLE 2-15. TYPICAL EXAMPLE FOR N_G ITERATION (Concluded)

* Results - $N_R(3) = 1, L_{CS}(3) = 1.783 \text{ cm}$

+ Decision - Is $N_G = N_{GMAX}$? = Yes

+ Calculation - $L_{CS} = \text{MAX} [L_{CS}(N_G)]$

* Results - $L_{CS} = L_{CS}(1) = 1.799 \text{ cm}$

+ Decision - Is $L_{CS} \geq L_{CSMIN}$? = Yes

Go to L_{CPMAX} Calculation

2.2.5 Design Options 5 and 6

Design options 5 and 6 (overview flowchart in figure 2-31) are provided to design modules with fixed module dimensions in a manner analogous to design options 1 and 3 in which the module dimensions could vary. The user inputs either maximum cell area (option 5) or maximum cell dimensions (option 6), fixed module dimensions, and series and parallel direction spacings. If option 5 is used, the maximum cell dimensions are calculated from equations 2-17 and 2-18. Next, N_S and N_P are determined from LCS_{MAX} and LCP_{MAX} , respectively, and the L_{CS} and L_{CP} required to fit N_S and N_P cells, respectively, in the module dimensions are calculated.

In methods that are analogous to those in design options 1 and 3, N_S is divided by N_{BP} and the bypass group is snaked or changed if needed; then the compatibility of K with NG_{MAX} is checked and snaking or paralleling in the series direction is accomplished if needed. L_{CS} and L_{CP} are also recalculated if needed. After the parallel redundancy check, the packing factor and electrical characteristics are calculated. The physical dimensions need not be calculated since the module dimensions are fixed. Then, the module dimensions may be switched to obtain an alternate design and the user may go to the Module Conductor Requirements routine when satisfied with the design.

The flowchart for entry into design options 5 and 6 is shown in figure 2-32. The procedure is straightforward through the calculation of N_S and N_P . If N_S is an integer, L_{CS} is set to LCS_{MAX} . If N_S is not an integer, N_S is increased to the next higher integer and L_{CS} is calculated from the integer N_S . L_{CS} will be less than LCS_{MAX} . The same procedure is followed for N_P and L_{CP} . The user then goes to the next flowchart.

In the flowchart in figure 2-33, the number of bypass groups (K) which will fit in the series direction is determined. If K is an integer, the user proceeds to the next flowchart. If K is not an integer, alterations must be made to make it an integer. As in design options 1 and 3, the first step is to try other N_{BP} , N_G combinations, first at the same V_{MPM} , and then at other V_{MPM} . If this fails, the relative size of the original N_{BP} with respect to N_S is checked. If N_{BP} is less than N_S , N_{BP} is decreased by one, NG_{MAX} is recalculated and truncated if needed, and K is recalculated. N_S is not changed because this would entail recalculating L_{CS} since L_{MS} must be kept constant. The user may, at his discretion, increase or decrease N_S if he feels this will lead to the best solution. The goal is to make K an integer so that the user can advance to the next flowchart.

If N_{BP} is larger than N_S , the algorithm will check the desirability of snaking the bypass group. If K is greater than 0.5, the bypass group will not be snaked, but instead, N_{BP} will be decreased until it equals N_S , making $K = 1$. If K is less than or equal to 0.5, the bypass group will be snaked. First, the variable N_{S2} is established as 2 times N_S . K is set equal to N_{S2} divided by N_{BP} . If K is an integer, the user proceeds to the next flowchart. If K is not an integer, N_{BP} is decreased until K is an integer. NG_{MAX} is recalculated and truncated whenever N_{BP} is changed. The snaking procedure will always result in $K = 1$.

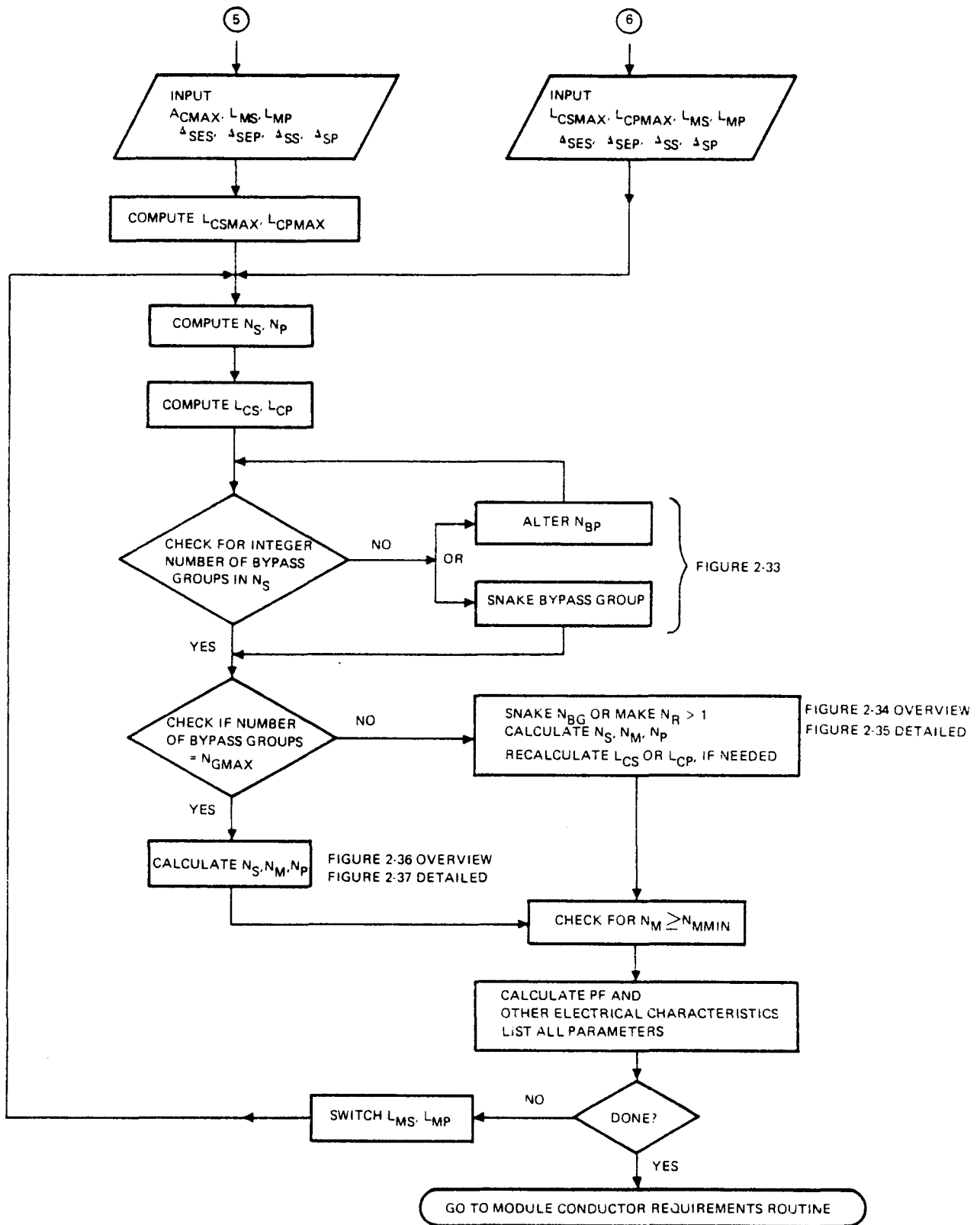


Figure 2-31. Overview Flowchart for Design Options 5 and 6

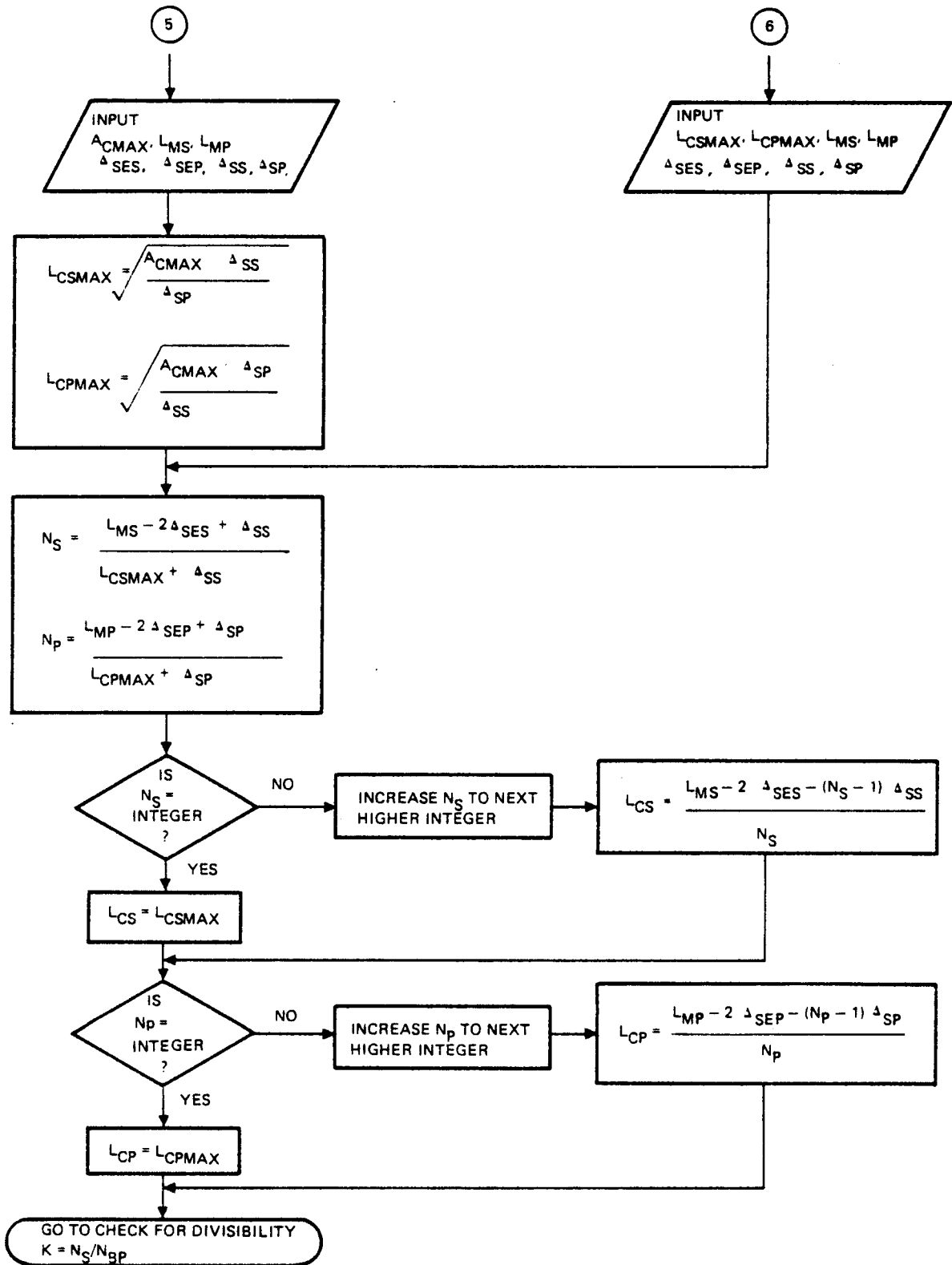


Figure 2-32. Flowchart for Entry into Design Options 5 and 6, and Calculation of Initial Numbers of Cells and Cell Size

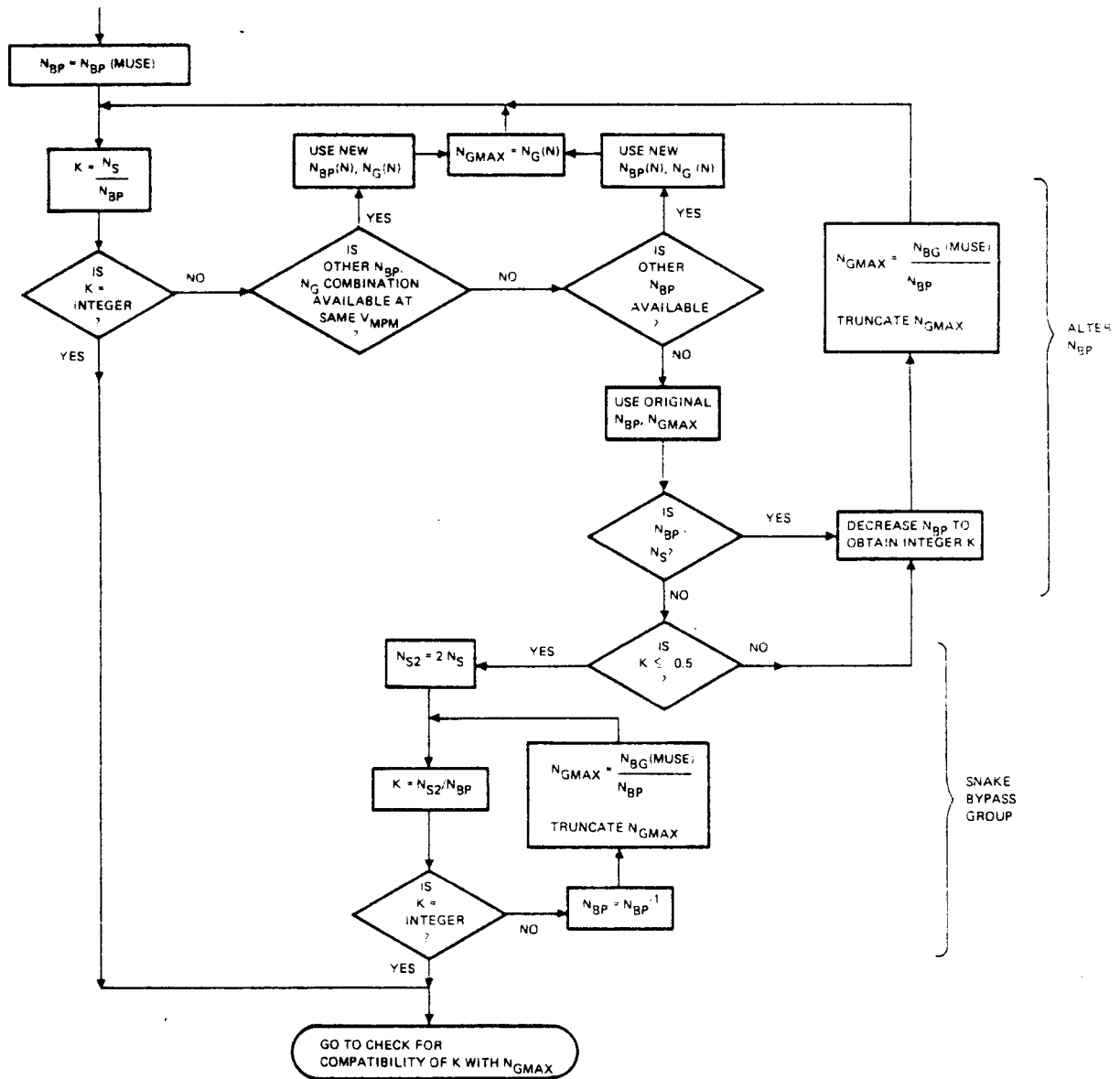


Figure 2-33. Flowchart for Selection of Acceptable N_S and N_{BP} Combination of Design Options 5 and 6

Both an overview flowchart (figure 2-34) and a detailed flowchart (figure 2-35) are provided for the next section of the methodology to assist the user in understanding both the concepts and the mechanics of the algorithms. The algorithms are very similar to those previously described for design options 1 and 3 except that appropriate steps are taken to prevent changing the module dimensions.

First, K is compared with N_{GMAX} . If K is greater than N_{GMAX} , the algorithm will parallel bypass groups in the series direction. N_R is obtained by dividing K by N_{GMAX} . If N_R is not an integer in figure 2-35, it is increased to the next higher integer and N_S is determined from N_R . L_{CS} is recalculated from the equation in figure 2-32 for the new value of N_S in order to keep L_{MS} constant. At this point, both branches of the N_R check converge. N_G is set equal to N_{GMAX} and N_M is determined as N_R times N_p . The user then advances to the parallel redundancy test.

If the K had been less than or equal to N_{GMAX} in the first decision block in figures 2-34 and 2-35, the user would then check if the bypass group had been snaked in figure 2-33; i.e., N_{S2} obtained. If N_{S2} had been obtained, the user proceeds to the N_{S2} routine. Otherwise, the user checks for $K > 0.5 N_{GMAX}$. If this question is true, K is either equal to N_{GMAX} or will be made equal to N_{GMAX} by setting $N_S = N_{BP} N_{GMAX}$. If N_S is changed, L_{CS} is recomputed from the equation in figure 2-32 with the new N_S . The user then proceeds to the $K = N_{GMAX}$ routine.

If K is less than or equal to $0.5 N_{GMAX}$, the algorithm will attempt to snake the series strings as often as needed. Setting $N_G = N_{GMAX}$, the algorithm checks to see if $N_p = 1$. If $N_p = 1$, the whole series string is forced into one row by increasing N_S to equal $N_{BP} N_G$. N_M is set to N_p and L_{CS} is then recalculated from the equation in figure 2-32 with the new N_S .

If $N_p > 1$, the number of snake sections required (J) is determined from N_G/K . If J is not an integer, N_G is reduced to obtain integer J . This is accomplished in figure 2-35 by truncating J and recalculating N_G as K times J . Next, N_M is obtained as N_p/J . If N_M is not an integer, it is increased to the next higher integer and N_p is increased to N_M times J . L_{CP} is recomputed from the equation in figure 2-32 with the new N_p . The user then proceeds to the parallel redundancy test.

The overview flowchart (figure 2-36) and the detailed flowchart (figure 2-37) apply to the cases in which $K = N_{GMAX}$ or the bypass group was snaked (N_{S2} obtained) in figure 2-33. After setting $N_G = N_{GMAX}$, the user branches to either the $K = N_{GMAX}$ routine or the N_{S2} routine. In the $K = N_{GMAX}$ routine, N_M is simply set equal to N_p since the whole series string fits exactly in the module series dimension. The user then goes on to the parallel redundancy test.

In the N_{S2} routine, the algorithm attempts to continue snaking the series string by half bypass groups until all N_G groups are used. Thus, the number of snake sections (J) is twice the number of bypass groups (N_G). First, N_S is set to $N_{S2}/2$ and N_M is specified as N_p divided by J or $2N_G$. If N_M is not an integer, it is increased to the next higher integer and N_p is increased to

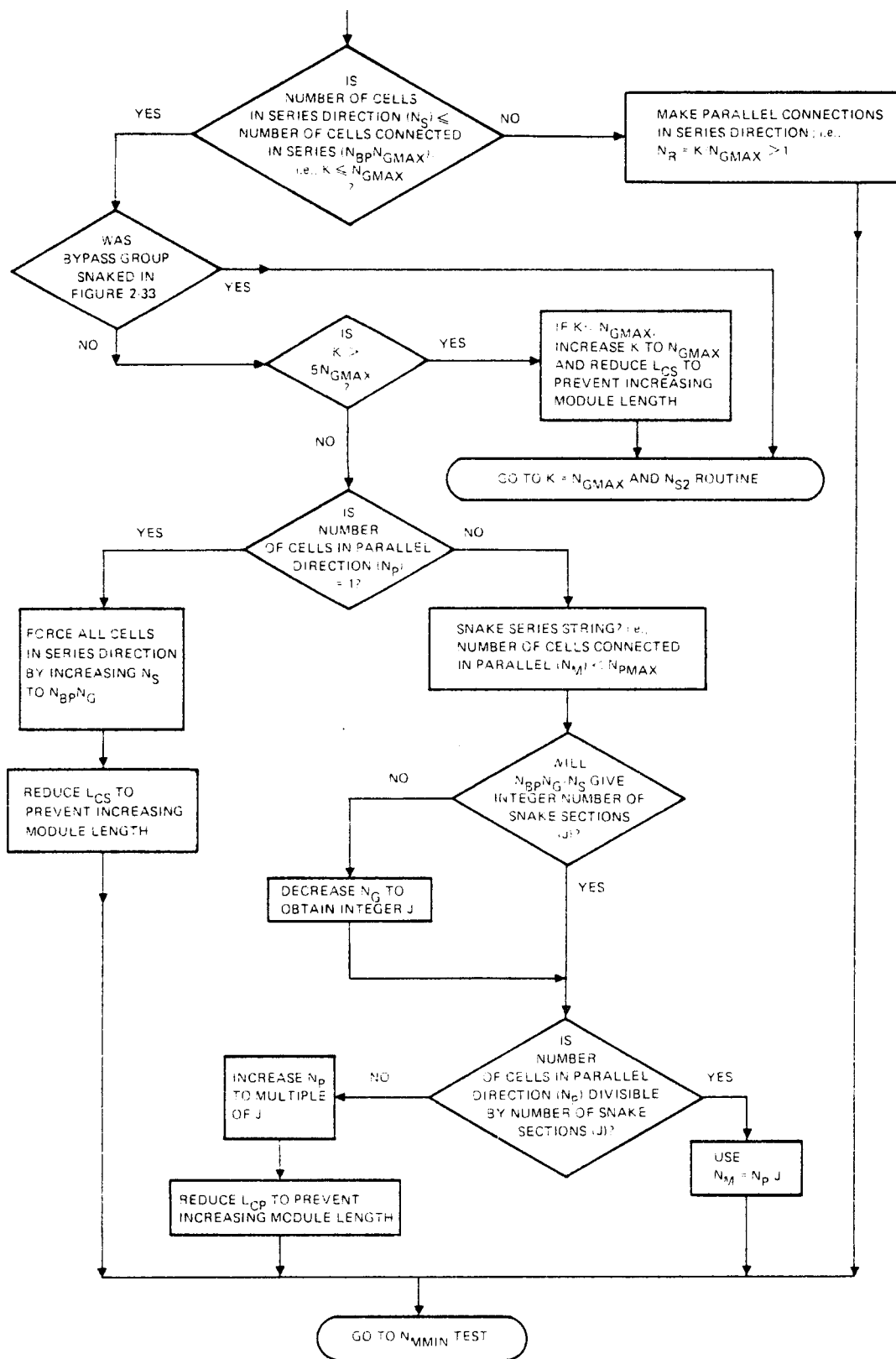
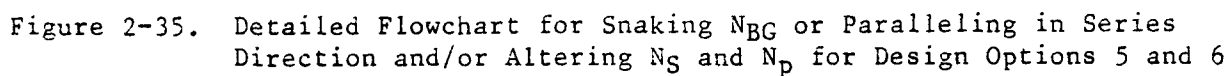


Figure 2-34. Overview Flowchart for Snaking N_B or Paralleling in Series Direction and/or Altering N_S and N_P for Design Options 5 and 6



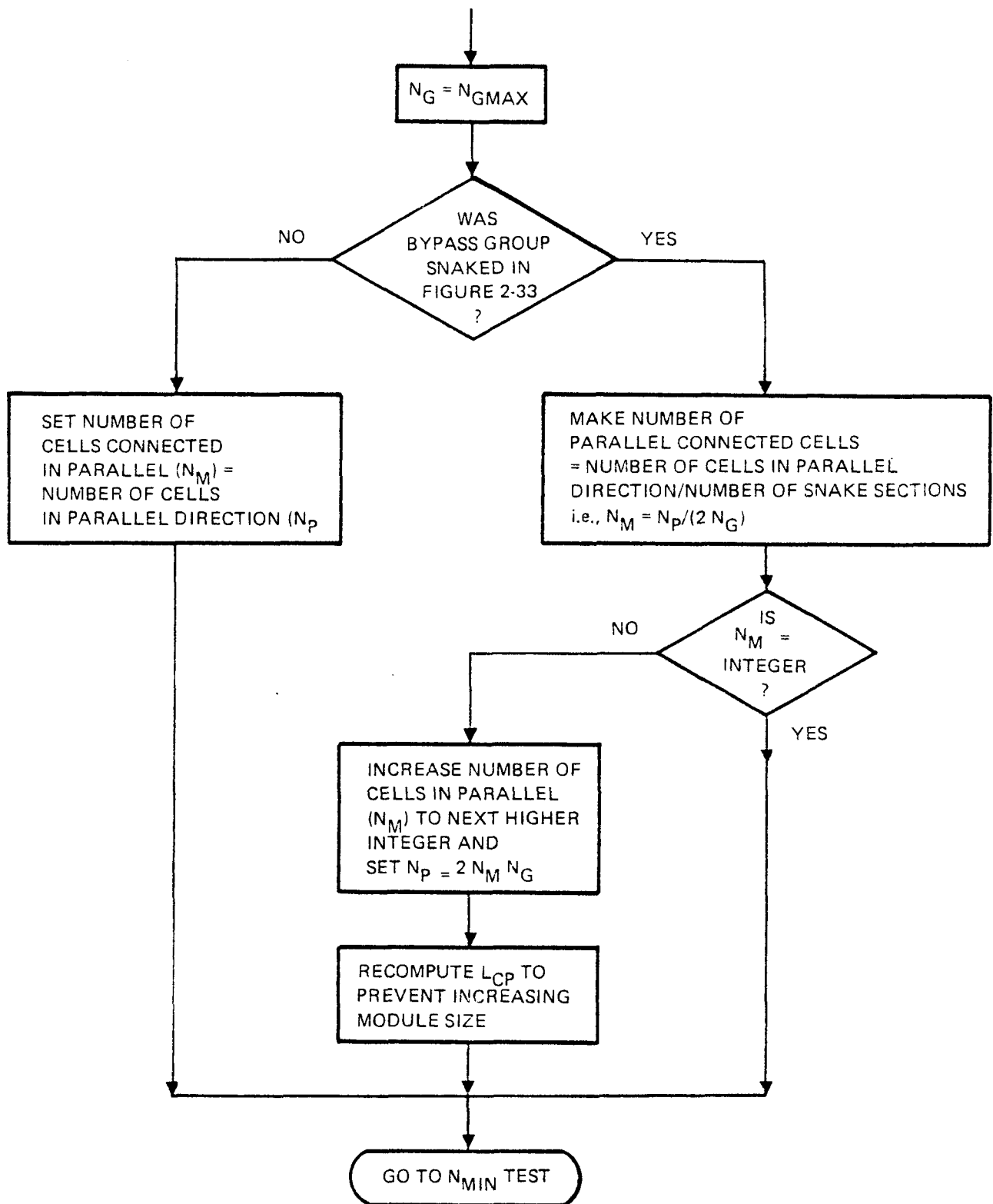


Figure 2-36. Overview Flowchart for Completing Design for $K = N_{GMAX}$ or N_{S2} Condition for Design Options 5 and 6

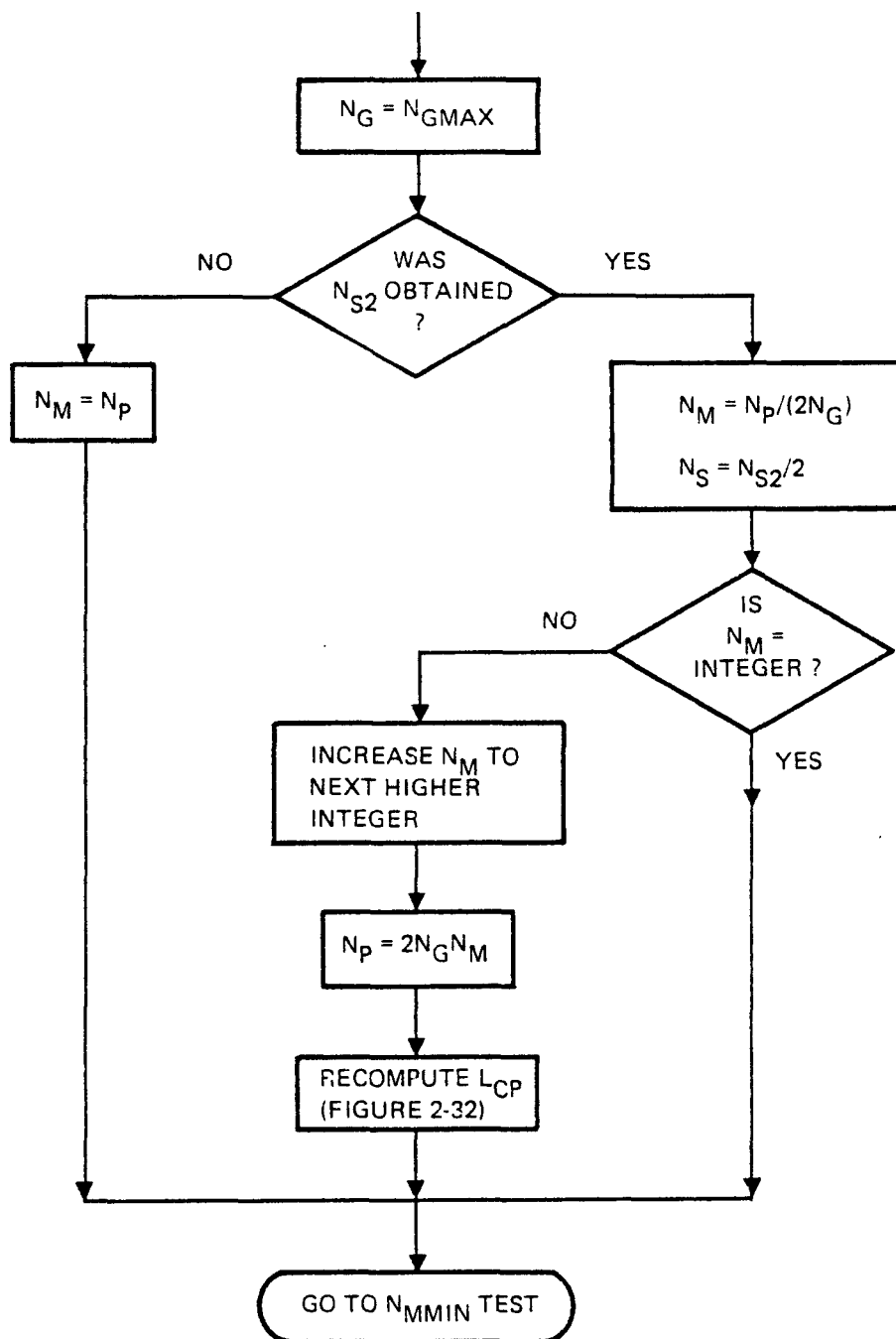


Figure 2-37. Detailed Flowchart for Completing Design for $K = N_{GMAX}$ or N_{S2}
Condition for Design Options 5 and 6

twice N_M times N_G . L_{CP} is then recomputed from the equation in figure 2-32. The user is cautioned that if the original N_M was less than one, the reduction in L_{CP} can be drastic. The user then proceeds to the parallel redundancy test.

The remaining flowchart for design options 5 and 6, shown in figure 2-38, is very similar to that for design options 1 and 3. The user tests for parallel redundancy then calculates the packing factor and the electrical characteristics from the equations in tables 2-4 and 2-5. If he wishes, he may then switch L_{MS} and L_{MP} and return to figure 2-32 to the N_G and N_P calculations to obtain an alternate module design. When finished with design options 5 and 6, the user may go to the Module Conductor Requirements routine.

2.2.6 Module Conductor Requirements Algorithm

The Module Conductor Requirements routine assists the user in determining the positioning of the conductor runs in the module and the width and thickness required for the conductors. An overview flowchart is contained in figure 2-39 and a detailed flowchart in figure 2-40. The user postulates the running of conductors in the module; then, determines the cross-sectional requirements by constraining the power loss in the conductors.

First, the conductor resistivity (ρ), the peak power of the module (P_M), the allowable fractional power loss (P_F), and the number of different conductor segments (N_{SEG}) are entered. The algorithm uses either equation 2-31 or equation 2-32 to calculate the conductor requirements. Here, the symbol, P_F , is used in place of f . The user inputs the length and maximum current of each conductor segment, calculates I^2L for each and sums the results. If the current is constant throughout the length, L , the user branches to the right which follows equation 2-31. If the current increases linearly along the length, L , as illustrated in figure 2-7, the user branches to the left which follows equation 2-32. The only difference is in the factor, 3, seen in equation 2-32.

The mechanics are illustrated in figure 2-40. $P(N) = L(N) I(N)^2$ is not a power, but rather an interim result which has the units of current squared times length (A^2 -cm). For the right branch, P_{SUM} is set to the sum; $P(N)$, previously obtained. For the left distributed branch, $P(N)$ is divided by three to obtain P_{SUM} . The minimum acceptable cross-sectional area for the metal, A_{MIN} , is then calculated.

If the user wishes to specify a maximum allowable conductor width, W_{MAX} , he may calculate the minimum acceptable conductor thickness, T_{MIN} . If he wishes to specify a maximum allowable conductor thickness, T_{MAX} , he may likewise calculate the minimum acceptable conductor width, W_{MIN} .

If he wishes, the user may then try other possible conductor runs or calculate the conductor requirements for alternate module designs. An example of the use of the Module Conductor Requirements routine is included at end of the next section.

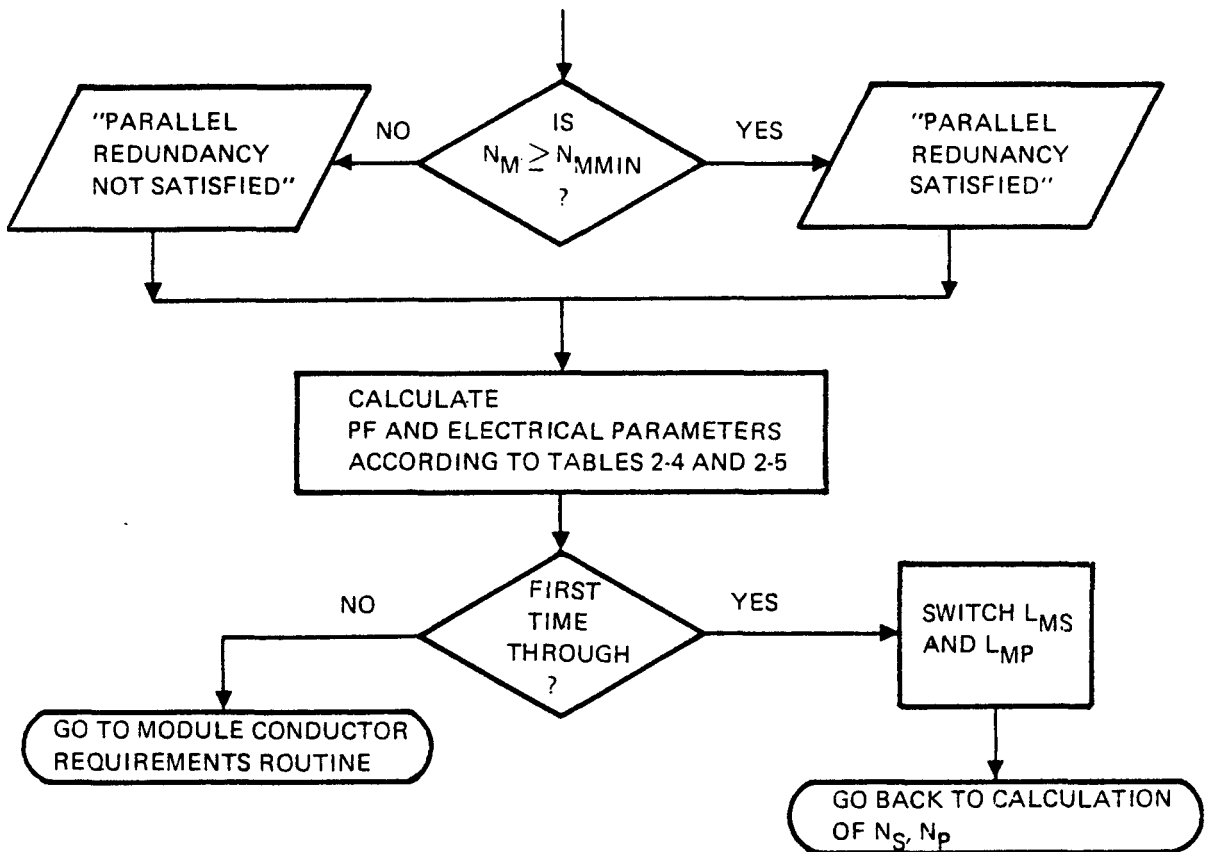


Figure 2-38. Flowchart for N_{MMING} Check and Completion of Design Options 5 and 6

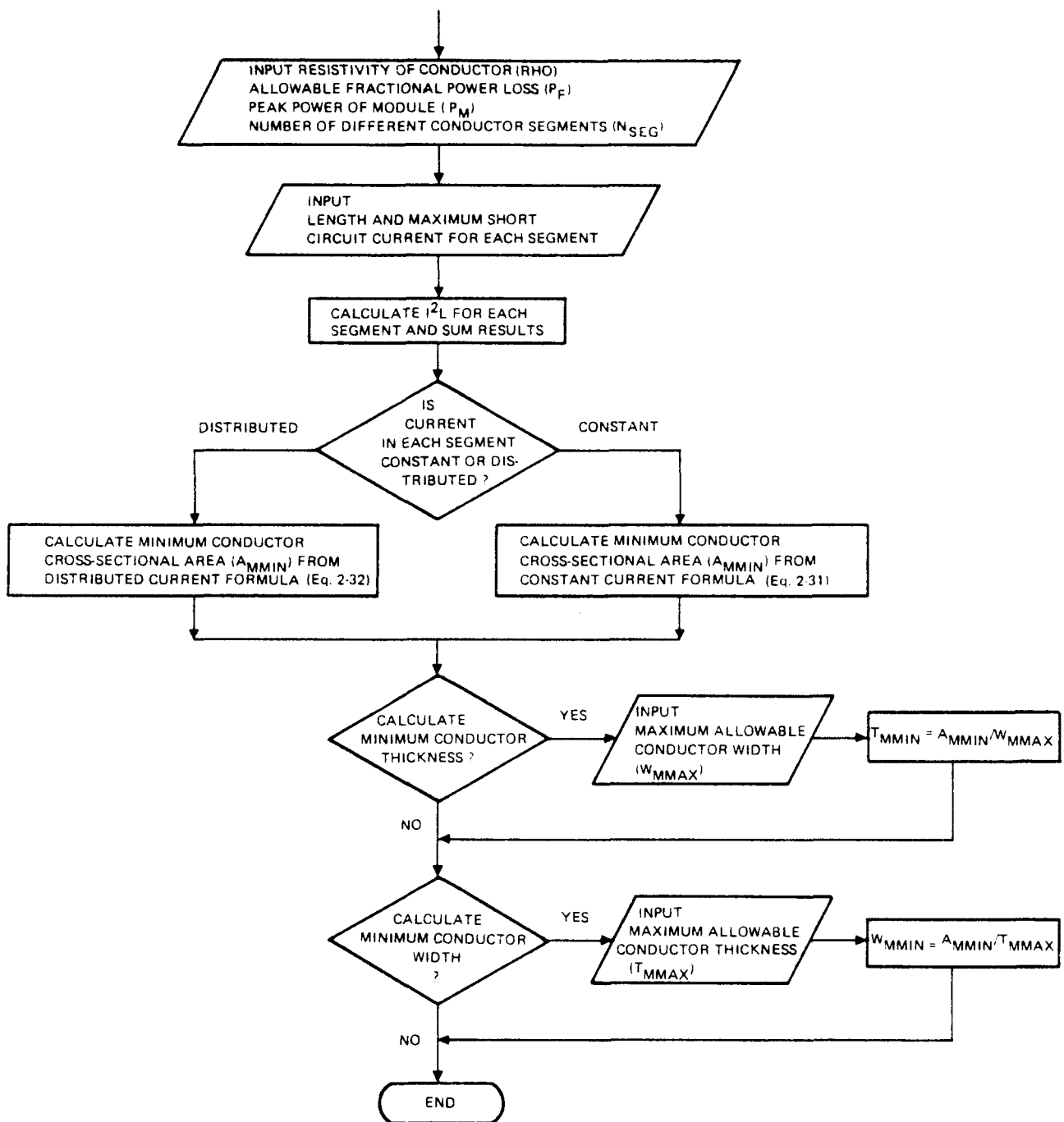


Figure 2-39. Overview Flowchart for Module Conductor Requirements Routine

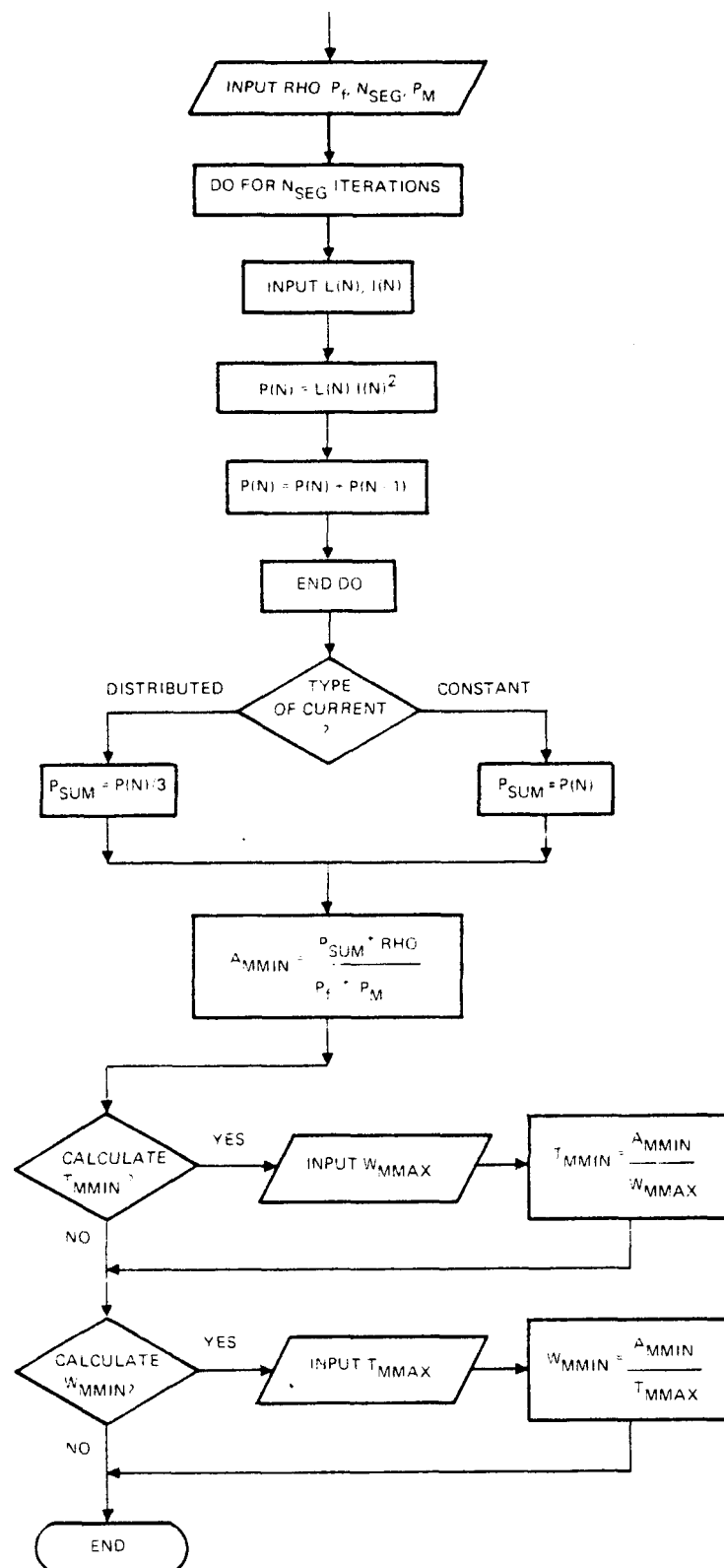


Figure 2-40. Detailed Flowchart for Module Conductor Requirements Routine

2.3 METHODOLOGY EXAMPLE

This example illustrates the use of the electrical methodology in determining the module design for a typical application. The parameters and constraints used in the example are listed in table 2-16. The cell parameters apply to a polycrystalline silicon cell of 11.5-percent efficiency with maximum dimensions of 6.0 cm series length by 16.0 cm parallel length. It has three across-the-cell interconnects. The module is for residential applications with allowable peak power voltages of 5, 10, or 20V and maximum open-circuit voltage of 30V. The module is nominally 4 feet by 4 feet, but the dimensions were set to 47.50 in (120.65 cm) to allow for manufacturing tolerance and roof assembly tolerances. Design option 6 was used which requires maximum cell dimensions and fixed module dimensions.

Tables 2-17 through 2-26 follow the design step-by-step through the appropriate algorithms of the main program and design option 6. Input lines are specified with a bullet at the left margin. Calculations and algorithm decisions are prefaced by a plus sign (+). Results of calculations are prefaced by an asterisk (*).

The design process results in the module described in table 2-27 and diagrammed in figure 2-41. This is a 20V module with 10 cells in a bypass group ($N_{bp} = 10$) and 4 bypass groups in parallel ($N_M = 4$). The 4 bypass groups ($N_G = 4$) connected in series are snaked in two sections ($J = 2$). Parallel redundancy is satisfied since $N_{MIN} = 3$. The module power is 156.8W with a packing factor of 0.935 for a module efficiency of 10.75 percent. The conductor runs shown in figure 2-41 are each 0.51 cm (0.2 in.) wide by 0.0125 cm (0.005 in.) thick. The conductors across the top and bottom of the module were considered in the conductor requirements calculations. The length of each segment is $L_{cp} + \Delta_{sp} = 14.70 \text{ cm} + 0.159 \text{ cm} = 14.859 \text{ cm}$ and the currents in each segment are as shown in figure 2-41. There are two segments with $I(1)$ current and four segments with each of $I(2)$, $I(3)$, and $I(4)$. The horizontal runs through the center of the module and the runs for the bypass diodes were not considered in the conductor requirements calculations since they will not carry current under normal operating conditions and, therefore, do not contribute to the fractional power loss. These conductors, however, should have the same cross-sectional area as all other conductors. The vertical interconnect strips for each cell are also not considered in the calculations since these are part of the cell design and are the same for all module designs.

TABLE 2-16. SPECIFICATION OF PARAMETERS AND CONSTRAINTS
FOR ELECTRICAL METHODOLOGY EXAMPLE

- Initial Cell Parameters (Polycrystalline Silicon)

$$V_{OCC} = 0.6V, V_{MPC} = 0.5V, J_{SCC} = 25\text{mA/cm}^2, J_{MPC} = 23\text{mA/cm}^2$$

$$P_C = 11.5\text{mW/cm}^2, \eta_C = 11.5\%, FF_C = 0.767, T_C = 25^\circ\text{C}$$

$$S_C = 100\text{mW/cm}^2, V_B = -10.0V, \Delta V/\Delta T = -0.0022V/^\circ\text{C}, N_{ACI} = 3$$

- Cell Physical Constraints

$$L_{CSMAX} = 6.0\text{cm}, L_{CPMAX} = 16.0\text{cm} \Rightarrow A_{CMAX} = 96.0\text{cm}^2$$

$$T_{CMAX} = 100^\circ\text{C}$$

- Module Electrical and Thermal Constraints

$$V_{MPM} \text{ Allowable} = 5, 10, 20V$$

$$V_{OCMAX} = 30V \text{ at } T_L = -20^\circ\text{C}$$

$$\Delta T/\Delta S = 3.5^\circ\text{C/W}, \Delta T/\Delta P = 3.0^\circ\text{C/W}$$

- Module Physical Constraints (Design Option 6)

$$L_{MS} = L_{MP} = 120.65\text{cm}$$

$$\Delta_{SES} = \Delta_{SEP} = 0.953\text{cm} (3/8 \text{ in}), \Delta_{SS} = \Delta_{SP} = 0.159\text{cm} (1/16 \text{ in})$$

- Conductor Requirements

$$\rho = 1.7 \times 10^{-6} \Omega\text{-cm}, P_F = 0.01, W_{MMAX} = 0.20\text{in} (0.51\text{cm})$$

TABLE 2-17. EXAMPLE CALCULATION SHEET 1 -
FOLLOWS FIGURES 2-9 AND 2-10

ENTER MAIN PROGRAM

- Input - Option? = A (Input Parameters)
- Input - $V_{OCC} = 0.6V$, $V_{MPC} = 0.5V$, $J_{SCC} = 25mA/cm^2$, $J_{MPC} = 23mA/cm^2$
 $P_C = 11.5mW/cm^2$, $\eta_C = 11.5\%$, $FF_C = 0.767$, $S_C = 100mW/cm^2$

Enter V_{MPM} , N_{BG} Routine

- Input - $M = 3$
 $V_{MPM}(1) = 5V$, $V_{MPM}(2) = 10V$, $V_{MPM}(3) = 20V$
- + Calculate - $N_{BG}(M) = V_{MPM}(M)/V_{MPC}$
- * Results - $V_{MPM}(1) = 5V$, $V_{MPM}(2) = 10V$, $V_{MPM}(3) = 20V$
 $N_{BG}(1) = 10 \text{ cells}$, $N_{BG}(2) = 20$, $N_{BG}(3) = 40$
 $V_{MPMAX} = 20V$

Go To N_{BPMAX} Routine

TABLE 2-18. EXAMPLE CALCULATION SHEET 2

- FOLLOWS FIGURE 2-11

Enter N_{BP}MAX Routine

- . Input - Calculate V_{RTMAX}? = YES

- . Input - A_CMAX = 96.0 cm², T_CMAX = 100°C
 T_A = 20°C, I_S = 100 mW/cm²

- . Input - Use Thermal Model? = NO

- . Input - ΔT/ΔS = 3.5°C/W, ΔT/ΔP = 3.0°C/W

- + Calculate -
$$P_D = \frac{(\Delta T/\Delta S) I_S A_{C\text{MAX}} - (T_{C\text{MAX}} - T_A)}{(\Delta T/\Delta P)}$$

$$V_{RT\text{MAX}} = P_D / (J_{MPC} A_{C\text{MAX}})$$

- * Results - P_D = -15.47 W, V_{RTMAX} = -7.0V

- . Input - V_B = -10.0V, V_{FD} = 0.7V

- + Calculate -
$$V_{R\text{MAX}} = - \text{MIN} \left[|V_{RT\text{MAX}}|, |V_B| \right] ; N_{BP\text{MAX}} = 1 - \frac{V_{R\text{MAX}} + V_{FD}}{V_{OCC}}$$

- * Results - V_RMAX = -7.0V, N_{BP}MAX = 11.5 = 11 (Truncated)

Go to N_{MP}MIN Routine

TABLE 2-19. EXAMPLE CALCULATION SHEET 3
- FOLLOWS FIGURE 2-12

Enter N_{MMIN} Routine

. Input - N_{ACI} = 3

+ Calculate -
$$N_{MMIN} = \frac{J_{SCC}}{2N_{ACI} (J_{SCC} - J_{MPC})}$$

* Results - N_{MMIN} = 2.1 Round Up

N_{MMIN} = 3 Cells in Parallel

Go to N_{BGMAX} Routine

TABLE 2-20. EXAMPLE CALCULATION SHEET 4
- FOLLOWS FIGURE 2-13

Enter N_{BGMAX} Routine

. Input - $\Delta V/\Delta T = -0.0022 \text{ V}/^{\circ}\text{C}$, $T_L = -20^{\circ}\text{C}$

$T_C = 25^{\circ}\text{C}$, $V_{OCMAX} = 30\text{V}$

+ Calculate - $N_{BGMAX} = \text{MIN} \left[\frac{V_{OCMAX}}{V_{OCC} + (\Delta V/\Delta T)(T_L - T_C)}, \frac{V_{MPMAX}}{V_{MPC}} \right]$

* Results - $N_{BGMAX} = \text{MIN} [42.9, 40] = 40$

Go to Catalogue of Acceptable N_{BP}, N_G Combinations

TABLE 2-21. EXAMPLE CALCULATION SHEET 5 -
FOLLOWS FIGURE 2-13

Enter Catalogue of Acceptable N_{BP} , N_G Combination

+ Calculate - $N_{BPMIN} = 0.5 N_{BPMAX}$; N_{BP} , N_G Options ($N_{BP}(N, N_G) = N_{BG}(N)/N_G$)

* Results - $N_{BPMIN} = 5.5$

* Results	- N	$V_{MPM}(N)$	$N_{BG}(N)$	N_G	$N_{BP}(N, N_G)$	Acceptable?	N1
	1	5V	10	1	10	YES	1
				2	$5 < N_{BPMIN}$	NO	-
				3,4	Not Integers	NO	-
				5	$2 < N_{BPMIN}$	NO	-
				6-9	Not Integers	NO	-
				10	$1 < N_{BPMIN}$	NO	-
	2	10V	20	1	$20 < N_{BPMAX}$	NO	-
				2	10	YES	2
				3	Not Integer	NO	-
				4	$5 < N_{BPMIN}$	NO	-
				5	$4 < N_{BPMIN}$	NO	-
				6-9	Not Integers	NO	-
				10	$2 < N_{BPMIN}$	NO	-
				11-19	Not Integers	NO	-
				20	$1 < N_{BPMIN}$	NO	-
	3	20V	40	1	$40 > N_{BPMAX}$	NO	-
				2	$20 > N_{BPMAX}$	NO	-
				3	Not Integer	NO	-
				4	10	YES	3
				5	8	YES	4
				6,7	Not Integers	NO	-
				8	$5 < N_{BPMIN}$	NO	-
				9	Not Integer	NO	-
				10	$4 < N_{BPMIN}$	NO	-
				11-19	Not Integers	NO	-
				20	$2 < N_{BPMIN}$	NO	-
				21-39	Not Integers	NO	-
				40	$1 < N_{BPMIN}$	NO	-

Go To N_{BP} Routine

TABLE 2-22. EXAMPLE CALCULATION SHEET 6 -
FOLLOWS FIGURE 2-14

Enter N_{BP} Routine

+ Calculate - Largest N_{BP} for Largest V_{MPM} Acceptable

$$N_{BP} = N_{BP}(MUSE); N_{GMAX} = N_G(MUSE)$$

* Results - MUSE = 3

$$N_{BP} = 10$$

$$N_{GMAX} = 4$$

Go To Design Options

TABLE 2-23. Example Calculation Sheet 7
- Follows Figure 2-32

Enter Design Option 6

. Input - $L_{CSMAX} = 6.0 \text{ cm}$, $L_{CPMAX} = 16.0 \text{ cm}$

$L_{MS} = 120.65 \text{ cm}$, $L_{MP} = 120.65 \text{ cm}$

$\Delta_{SES} = \Delta_{SEP} = 0.953 \text{ cm}$, $\Delta_{SS} = \Delta_{SP} = 0.159 \text{ cm}$

+ Calculate - $N_S = \frac{L_{MS} - 2\Delta_{SES} + \Delta_{SS}}{L_{CSMAX} + \Delta_{SS}}$, $N_P = \frac{L_{MP} - 2\Delta_{SEP} + \Delta_{SP}}{L_{CPMAX} + \Delta_{SP}}$

* Results - $N_S = 19.3 \text{ Round Up}$, $N_P = 7.4 \text{ Round Up}$

$N_S = 20 \text{ Cells in Series Direction}$

$N_P = 8 \text{ Cells in Parallel Direction}$

+ Calculate - $L_{CS} = \frac{L_{MS} - 2\Delta_{SES} - (N_S - 1)\Delta_{SS}}{N_S}$, $L_{CP} = \frac{L_{MP} - 2\Delta_{SEP} - (N_P - 1)\Delta_{SP}}{N_P}$

* Results - $L_{CS} = 5.79 \text{ cm}$, $L_{CP} = 14.70 \text{ cm}$

Go to Check for Divisibility ($K = N_S/N_{BP}$)

TABLE 2-24. EXAMPLE CALCULATION SHEET 8 -
FOLLOWS FIGURES 2-33 AND 2-34

Enter Check for Divisibility of N_S by N_{BP}

- + Calculate - $K = N_S / N_{BP}$
- * Results - $K = 2.0$
- + Decision - Is K Integer? = Yes

Enter Check for Compatibility of K with N_{GMAX}

- + Decision - Is $K \leq N_{GMAX}$? = Yes
- + Decision - Was N_{S2} Obtained? = No
- + Decision - Is $N_{GMAX}/2 < K \leq N_{GMAX}$? = No
- + Calculate - $N_G = N_{GMAX}$
- * Results - $N_G = 4$
- + Decision - Is $N_P = 1$? = No
- + Calculate - $J = N_G / K$
- * Results - $J = 2.0$
- + Decision - Is J Integer? = Yes
- + Calculate - $N_M = N_P / J$
- * Results - $N_M = 4.0$
- + Decision - Is N_M Integer? = Yes

Go To N_{MMIN} Test

TABLE 2-25. EXAMPLE CALCULATION SHEET 9 -
FOLLOWS FIGURE 2-38

Enter N_{MMIN} Test

- + Decision - Is $N_M \geq N_{MMIN}$? = Yes
- * Results - "Parallel Redundancy Satisfied"
- + Calculate - Cell and Module Electrical Parameters and Packing Factor
- * Results - Cell
 $\frac{A_C}{A_C} = 85.1 \text{ cm}^2, I_{SCC} = 2.13A$
 $I_{MPC} = 1.96A, P_C = 0.98W$
Module
 $V_{OCM} = 24.0V, V_{MPM} = 20.0V$
 $I_{SCM} = 8.52, I_{MPM} = 7.84A$
 $P_M = 156.8W, FF_M = 0.767$
 $PF = 0.935, \eta_M = 10.75\%$
- + Decision - First Time Through? -Yes but $L_{MS} = L_{MP}$; therefore,
 results will not change

Go To Module Conductor Requirements Routine

TABLE 2-26. EXAMPLE CALCULATION SHEET 10 -
FOLLOWS FIGURES 2-39 AND 2-40

Enter Module Conductor Requirements Routine

• Input - $\text{RHO} = 1.7 \times 10^{-6} \Omega\text{-cm}$, $P_f = 0.01$
 $N_{\text{SEG}} = 4$, $P_M = 156.8\text{W}$

• Input - $L(1) = 29.7\text{cm}$, $L(2) = 59.4\text{cm}$, $L(3) = 59.4\text{cm}$, $L(4) = 59.4\text{cm}$
 $I(1) = 8.5\text{A}$, $I(2) = 6.375\text{A}$, $I(3) = 4.25\text{A}$, $I(4) = 2.125\text{A}$

+ Calculate - $P(N) = \sum_{i=1}^4 L(i) I(i)^2$

* Results - $P(N) = 5881\text{cm-A}^2$

+ Decision - Type of Current? = Constant

+ Calculate - $P_{\text{SUM}} = P(N)$

* Results - $P_{\text{SUM}} = 5881\text{cm-A}^2$

+ Calculate - $A_{\text{MMIN}} = P_{\text{SUM}} \text{RHO} / (P_f P_M)$

* Results - $A_{\text{MMIN}} = 6.38 \times 10^{-3} \text{cm}^2$

+ Decision - Calculate T_{MMIN} ? = Yes

• Input - $W_{\text{MMAX}} = 0.51\text{cm}$

+ Calculate - $T_{\text{MMIN}} = A_{\text{MMIN}} / W_{\text{MMAX}}$

* Results - $T_{\text{MMIN}} = 0.0125\text{cm}(0.005 \text{ in})$

+ Decision - Calculate W_{MMIN} ? = No

End

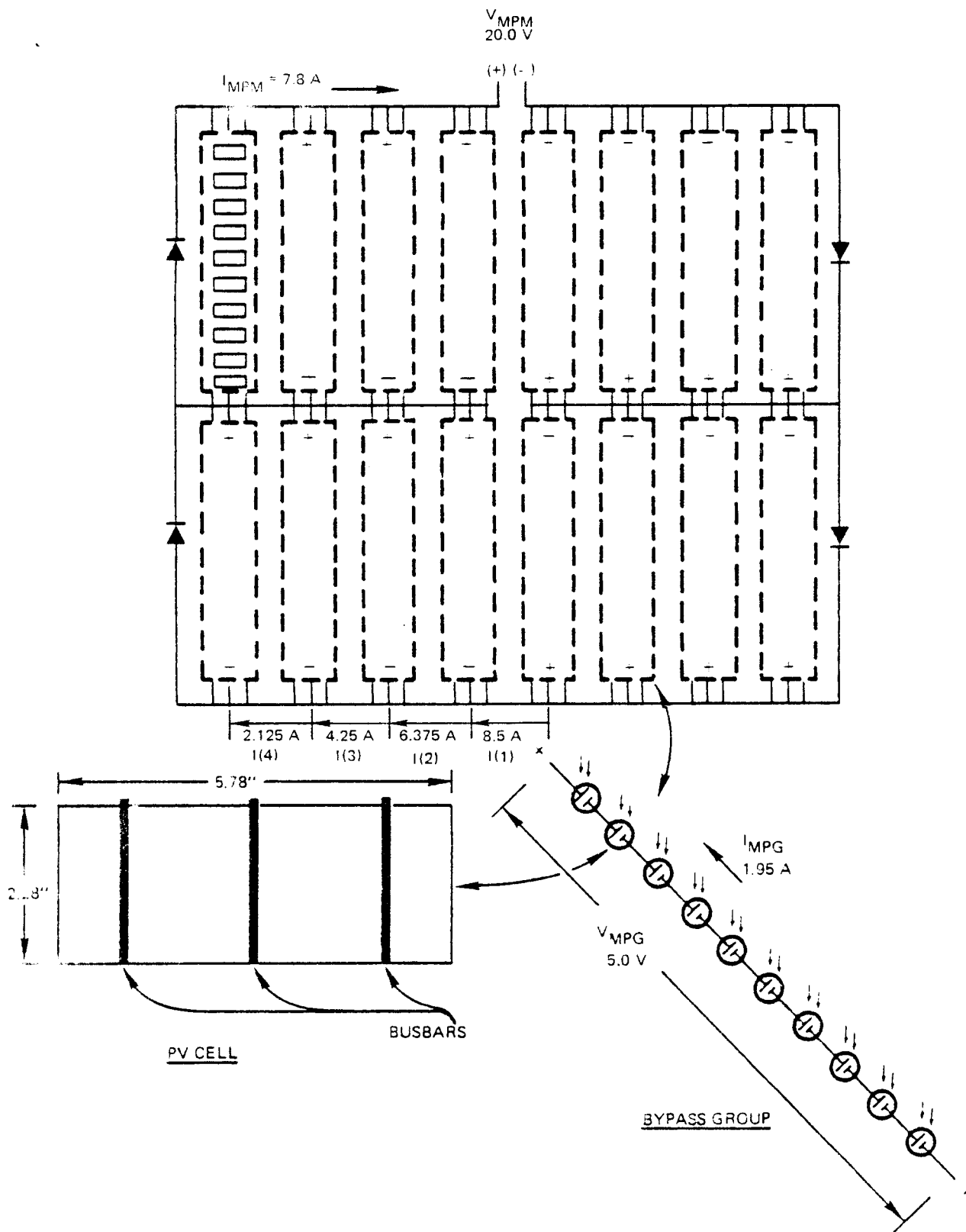


Figure 2-41. Polycrystalline Silicon Residential Module Example Layout

TABLE 2-27. FINAL DESIGN CHARACTERISTICS FOR ELECTRICAL EXAMPLE

- Polycrystalline Silicon Residential Module

- Cell Dimensions

$$L_{CS} = 5.79\text{cm} \times L_{CP} = 14.70\text{cm}; = A_C = 85.1\text{cm}^2$$

$$2.28 \text{ in } \times \quad \quad 5.79 \text{ in}; \quad \quad 13.2 \text{ in}^2$$

$$N_{ACI} = 3 \text{ Busbars}$$

- Module Physical Characteristics

$$N_S = 20, N_P = 8$$

$$L_{MS} = L_{MP} = 120.65\text{cm} (47.50 \text{ in})$$

$$PF = 0.935$$

- Module Electrical Characteristics

$$N_{BP} = 10, N_G = 4, N_{BG} = 40, N_M = 4$$

$$V_{OCM} = 24.0\text{V}, V_{MPM} = 20.0\text{V}$$

$$I_{SCM} = 8.52\text{A}, I_{MPM} = 7.84\text{A}$$

$$P_M = 156.8\text{W}, FF_M = 0.767, \eta_M = 10.75\%$$

$$\text{Conductor - Thickness} = 0.0125 \text{ cm, Width} = 0.51 \text{ cm}$$

2.4 ELECTRICAL GLOSSARY

<u>SYMBOLS</u>	<u>WHERE USED</u>	<u>DEFINITION</u>
A,B,C	DO 1,2,3	Coefficients of quadratic equation for L_{CP} for circular cells (table 2-9)
A_C	DO 1,2,3,4,5,6	Area of cell
A_{CMAX}	GC, DO 1,4,5	Maximum Cell Area
A_{MMIN}	CR	Minimum acceptable metal or conductor cross-sectional area (figures 2-39 and 2-40)

CT = Cell Technology

GC = General Constraints

DO = Design Option

CR = Module Conductor Requirements

<u>SYMBOLS</u>	<u>WHERE USED</u>	<u>DEFINITION</u>
a	DO 1,2,3	Distance between centers of adjacent circular cells in parallel direction (figure 2-5)
b	DO 1,2,3	Distances between centers of adjacent circular cells in series direction (figure 2-5)
c	DO 1,2,3	Distance between centers of adjacent circular cells in diagonal direction (figure 2-5)
D	DO 1,2,3	Diameter of circular cell (figure 2-5)
FF _C , FF _M	CT, DO 1,2,3,4,5,6	Fill factors of cell and module, respectively
F _L	DO 4	Fractional lower limit on cell series length
I _{MPC} , I _{MPM}	DO 1,2,3,4,5,6	Current at maximum power for cell and module, respectively (tables 2-4 and 2-5)
I _{SCC} , I _{SCM}	DO 1,2,3,4,5,6	Short circuit current of cell and module, respectively (tables 2-4 and 2-5)
I _S	GC	Standard insolation on cell for power dissipation calculation (equation 2-1)
I(N)	CR	Maximum current in one of the module conductor segments (figure 2-40)
J	DO 1,2,3,5,6	Number of sections of series snake (figure 2-6b)

CT = Cell Technology

GC = General Constraints

DO = Design Option

CR = Conductor Requirements

<u>SYMBOLS</u>	<u>WHERE USED</u>	<u>DEFINITION</u>
J _{MPC}	CT,GC,DO 1,2,3,4,5,6	Current density at maximum power of cell
J _{SCC}	CT,GC,DO 1,2,3,4,5,6	Short circuit current density of cell
K	DO 1,3,5,6	Number of bypass groups which can fit in module series length ($K = N_S/N_{BP}$)
L _{CP}	DO 1,2,3,4,5,6	Length of cell in parallel direction
L _{CPMAX}	DO 4,5,6	Maximum allowable cell length in parallel direction
L _{CS}	DO 1,2,3,4,5,6	Length of cell in series direction
L _{CSMAX}	DO 4,5,6	Maximum allowable cell length in series direction
L _{CSMIN}	DO4	Minimum acceptable cell length in series direction
L _{CSOPT} ,L _{CPOPT}	DO4	Optimal cell length in series and parallel directions, respectively (Equations 2-17 and 2-18)
L _{MP}	DO 1,2,3,4,5,6	Length of module in parallel direction
L _{MPMAX}	DO 1,3	Maximum allowable module length in parallel direction
L _{MS}	DO 1,2,3,4,5,6	Length of module in series direction
L _{MSMAX}	DO 1,3	Maximum allowable module length in series direction
L(N)	CR	Length of one of the module conductor segments (figure 2-40)
M	GC	Number of allowable module voltages (figure 2-10)

<u>SYMBOLS</u>	<u>WHERE USED</u>	<u>DEFINITION</u>
MUSE	GC	Index of the N_{bp} value to be used (figure 2-14)
N_{ACI}	GC	Number of across-the-cell or redundant interconnects (figures 2-4 and 2-12)
N_{BG}	GC, DO 1,3,5,6	Number of series connected cells required to obtain allowable module voltage
N_{BGMAX}	GC	Maximum number of series connected cells allowable based on maximum module voltage (Equation 2-10 and figure 2-13)
N_{BP}	GC, DO 1,2,3,4,5,6	Number of series-connected cells in bypass group, i.e., shunted by bypass diode
N_{BPMAX}	GC	Maximum number of series-connected cells allowable in a bypass group (figures 2-2 and 2-11)
N_C	DO 2	Total number of cells in module (figure 2-23)
N_G	GC, DO 1,2,3,4,5,6	Number of bypass groups connected in series in module
N_{GMAX}	GC, DO 1,2,3,4,5,6	Maximum number of series-connected bypass groups allowable based on maximum allowable module voltage
N_M	DO 1,2,3,4,5,6	Number of cells or strings connected in parallel in module
N_{MMIN}	GC, DO 1,2,3,4,5,6	Minimum number of cells or strings needed in parallel to ensure redundancy (figures 2-3 and 2-4)
N_p	DO 1,2,3,4,5,6	Number of cells arranged in the parallel direction in the module

<u>SYMBOLS</u>	<u>WHERE USED</u>	<u>DEFINITION</u>
N _{PMAX}	DO 1,3	Maximum number of cells which will fit in the parallel direction in the module
N _{POINT}	CT	Number of point pairs input from cell J-V curve
N _R	DO 1,2,3,4,5,6	Number of series strings connected in parallel in series direction (figure 2-6c)
N _S	DO 1,2,3,4,5,6	Number of cells arranged in the series direction in the module
N _{SMAX}	DO 1,3	Maximum number of cells which will fit in the module in the series direction
N _{SEG}	CR	Number of conductor segments in the module for which I(N) and L(N) are input (figure 2-40)
N _{S2}	DO 1,3,5,6	Twice the number of cells in the series direction; used for snaking the bypass group
N _{YES}	GC	Number of acceptable N _{BP} , N _G combinations available
P _C , P _M	CT, DO 1,2,3,4,5,6	Maximum power of cell and module, respectively
P _D	GC	Power dissipation in cell during reverse bias due to shadowing (equation 2-1 and figure 2-11)
P _F	DO 1,2,3,4,5,6	Module packing factor (table 2-5)
P _F	CR	Fractional power loss allowable in module due to resistance of conductor runs (figure 2-40)

<u>SYMBOLS</u>	<u>WHERE USED</u>	<u>DEFINITION</u>
P_{FL}	DO 4	Fractional power loss allowable in cell due to resistance of limiting current carrier (equation 2-30 and Figure 2-27)
P_{SUM}	CR	$P(N)$ for constant current or $P(N)/3$ for distributed current (figure 2-40)
$P(N)$	CR	Sum of all $I(N)^2 L(N)$ (figure 2-40)
R	DO 4	Sheet resistivity of limiting current carrier (equation 2-30 and figure 2-27)
RHO	CR	Resistivity of module conductors
S_C	CT	Standard insolation for cell J-V curve (figure 2-9)
T_A	GC	Ambient temperature for calculation of P_D (equation 2-1 and figure 2-11)
T_C	GC	Cell temperature at which J-V curve was measured for N_{BGMAX} calculation (equation 2-10 and figure 2-13)
T_{CMAX}	GC	Maximum allowable cell temperature in reverse bias P_D calculation (equation 2-1 and figure 2-11)
T_L	GC	Lowest anticipated cell temperature for N_{BGMAX} calculation (equation 2-10 and figure 2-13)
T_{MMAX}	CR	Maximum allowable thickness of metal for conductor runs in module (figure 2-40)
T_{MMIN}	CR	Minimum acceptable thickness of metal for conductors runs in module (figure 2-40)

<u>SYMBOLS</u>	<u>WHERE USED</u>	<u>DEFINITION</u>
V_B	GC	Reverse breakdown voltage of cell (figures 2-2 and 2-11)
V_{FD}	GC	Forward voltage of bypass diode (figures 2-2 and 2-11)
V_{MPC}, V_{MPM}	CT, GC, DO 1,2,3,4,5,6	Voltage at maximum power for cell and module, respectively
$V_{MPM}(N)$	GC	One of the allowable module voltages (figure 2-10)
V_{MPMAX}	GC	Maximum of the allowable module voltages (figure 2-10)
V_{OCC}, V_{OCM}	CT, GC, DO 1,2,3,4,5,6	Open circuit voltage of cell and module, respectively
V_{OCMAX}	GC	Maximum allowable module open circuit voltage for N_{BCMAX} calculation (equation 2-10 and figure 2-13)
V_{RMAX}	GC	Maximum acceptable cell reverse voltage (figures 2-2 and 2-11)
V_{RTMAX}	GC	Maximum allowable reverse voltage based on T_{CMAX} (equation 2-2 and figures 2-2 and 2-11)
W_{MAX}	DO 4	Maximum acceptable cell length (or width) in series direction due to limiting current carrier (equation 2-30 and figure 2-27)
W_{MMAX}	CR	Maximum allowable width of metal for conductor runs in module (figure 2-40)
W_{MMIN}	CR	Minimum acceptable width of metal for conductor runs in module (figure 2-40)

<u>SYMBOLS</u>	<u>WHERE USED</u>	<u>DEFINITION</u>
$\Delta SES, \Delta SEP$	DO 1,2,3,4,5,6	Edge spacing (distance from cell to edge of module) in series and parallel directions, respectively
ΔSP	DO 1,2,3,4,5,6	Interior spacing (distance between cells) in parallel direction for rectangular cells or in diagonal direction for circular cells (figure 2-5)
ΔSS	DO 1,2,3,5,6	Interior spacing (distance between cells) in series direction
$\Delta SS1$	DO 4	Spacing between negative ends of adjacent bypass groups which are connected to each other in parallel (figure 2-26)
$\Delta SS2$	DO 4	Spacing between positive ends of adjacent bypass groups which are connected to each other in parallel (figure 2-26)
$\Delta SS3$	DO 4	Spacing between the negative end of one bypass group and the positive end of the next when they are connected to each other in series (figure 2-26)
$\Delta T / \Delta P$	GC	Coefficient for temperature increase in cell due to reverse bias power dissipation (equation 2-1 and figure 2-11)
$\Delta T / \Delta S$	GC	Coefficient for voltage increase in cell due to insolation power (equation 2-1 and figure 2-11)
$\Delta V / \Delta T$	GC	Coefficient for voltage variation with temperature for N_{BGMAX} calculation (equation 2-10 and figure 2-13)
η_c, η_m	CT, DOs 1,2,3,4,5,6	Efficiency of cell and module, respectively

2.5 REFERENCES FOR ELECTRICAL METHODOLOGY

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SECTION 3.0 THERMAL ANALYSIS

3.1 INTRODUCTION

This section of the PV Module Optimization Methodology describes the method for calculating the temperature distribution through the module laminates. The methodology will be presented for flat plate and concentrating geometries, and relations will be presented for calculating the required heat transfer coefficients.

The primary purpose of this analysis is to determine the PV cell operating temperature under user-defined conditions. Electrical design will be performed based on the nominal temperature at which the cell characteristics were determined. Subsequently, module performance can be determined at the normal operating cell temperature calculated in this section. In addition, danger of chemical degradation can be determined from the encapsulant temperature, and thermal stresses can be determined from the temperature distribution through the module.

A one-dimensional, steady-state situation is assumed and a thermal/electrical circuit analogy is used to calculate the temperature distribution. A typical thermal cell is shown in figure 3-1 where the temperature is calculated at nodes 1 through 5 for a cell in the center of the module, and at all six nodes for a cell located at the edge of a module. A center cell would have the highest temperature since lateral heat flow would be negligible. A side cell would have the minimum temperature since the cell loses heat not only through the top and bottom faces but also to the side frame.

The PV cell may be defined by the user as square, rectangular or circular, but the thermal cell must be square or rectangular to simplify calculation. The thermal cell dimensions may be defined by the user, or the user may define a packing factor and calculate the area of the thermal cell from equation 3-114. The dimensions of the thermal cell are normally based on the dimensions of the PV cell plus one-half the spacings between cells. As shown in figure 3-1 the thermal cell may consist of a cover film, top encapsulant, PV cell, bottom encapsulant or adhesive, and substrate. The substrate may also consist of several laminated materials; however, the substrate temperature is assumed uniform at the temperature of node 5. The frame consists of a seal, gasket, and metal frame. The user may select any of these materials to form a module. For example, a module using single crystal silicon cells may use all the materials mentioned; however, a thin film technology, such as amorphous silicon, may consist of only a glass cover, an absorbing PV cell with effectively zero thickness, and a substrate.

The thermal circuit is shown in figure 3-2. Here, the thermal resistances are denoted by R where the subscripts define the type of resistance as follows: K-conduction, c-convection, r-radiation. The energy input due to insolation absorbed at each module is analogous to current, and the temperatures at each node are analogous to voltage. In this analysis the ambient and coolant temperatures are assumed known as is the insolation incident on the module.

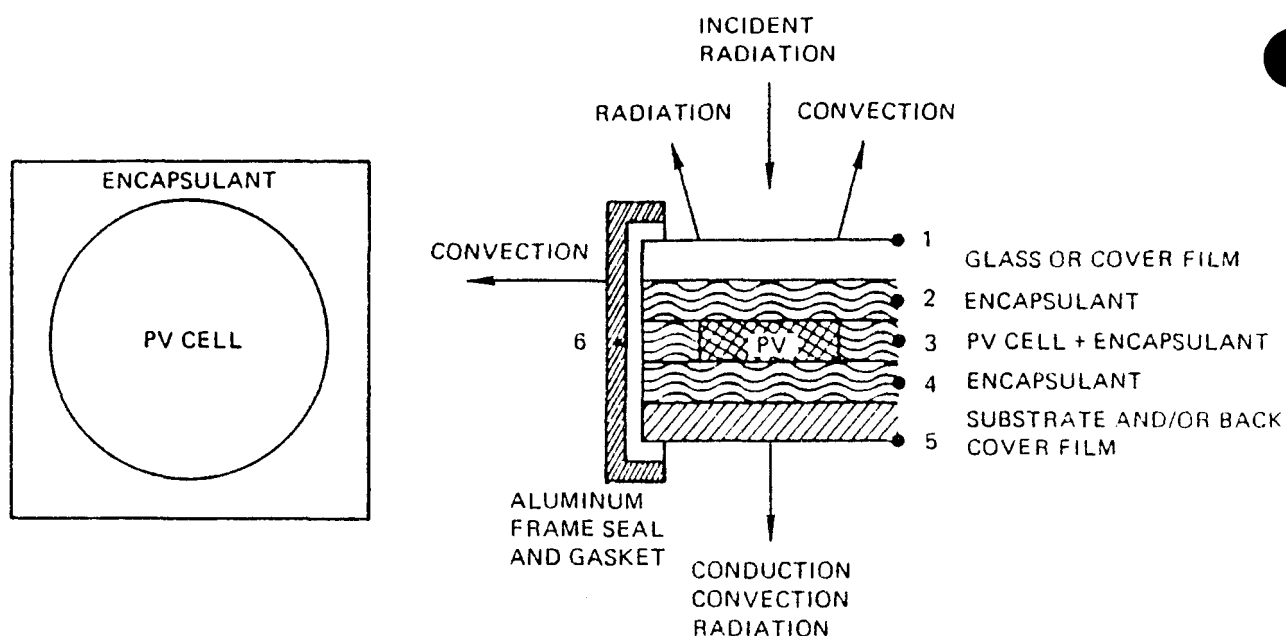


Figure 3-1. Typical Thermal Cell

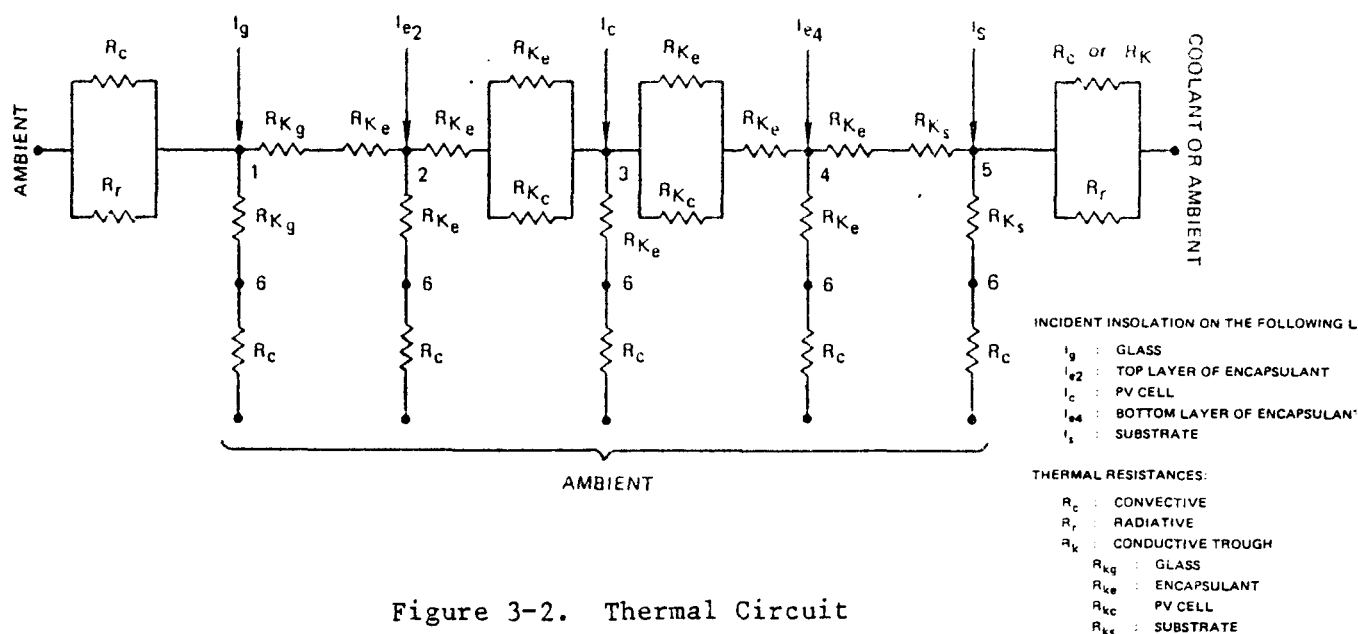


Figure 3-2. Thermal Circuit

Various geometries may be selected by the designer. These included flat plate and concentrating geometries. For a flat plate geometry, the user may assume a fully insulated (adiabatic) back to simulate a module mounted directly to the roof, or a cooled back. The cooled back option may be either air cooled (with or without fins) or forced liquid cooled. The concentrating geometries consist of point focus and liner Fresnel systems passively or actively cooled, or an actively cooled parabolic trough system.

In the following sections the energy balance equations and the thermal conductances will be derived for each of the geometry options. The methodology

will then be described for calculating the temperature distribution. The required input format for the computer program will be defined in the users handbook.

3.2 ENERGY BALANCE EQUATIONS

The energy balance equations consist of equating energy input at each node, to thermal energy transferred from each node. The only differences will be in the user defined materials and the number of nodes to be used.

3.2.1 Energy Input

The energy input to the thermal cell is due to solar insolation and power dissipation if the cell is in reverse bias. For the flat plate systems the insolation consists of direct normal, diffuse and reflected insolation. For concentrating collectors this energy is due only to direct normal insolation. Since solar energy input is a function of many variables such as elevation angle, azimuth angle, latitude, type of ground cover, etc., it will be up to the user to define the insolation on a flat plate collector or on the aperture of a concentrating collector. Then, the insolation incident on the top surface of the thermal cell is

$$I = I_o \eta_o \frac{A_a}{A_m} \quad (3-1)$$

where

I_o = insolation incident on the lens or trough aperture

η_o = optical efficiency

A_a = aperture area

A_m = area of the module PV cells

$\frac{A_a}{A_m}$ = concentration ratio

The energy absorbed at each node is given by

$$I_1 = I A_T \alpha_1 \quad (3-2)$$

$$I_2 = I A_T T_1 \alpha_2 \quad (3-3)$$

$$I_3 = I A_c T_1 T_2 (\alpha_c - \eta_c) + I (A_T - A_c) T_1 T_2 \alpha_3 + P_D A_C \quad (3-4)$$

$$I_4 = I \left[(A_T - A_c) T_3 + A_c T_c \right] T_1 T_2 \alpha_4 \quad (3-5)$$

$$I_5 = I \left[(A_T - A_c) T_3 + A_c T_c \right] T_1 T_2 T_4 \alpha_5 \quad (3-6)$$

$$I_6 = 0 \quad (3-7)$$

where

A_T = area of the thermal cell

A_c = area of the PV cell

α_1, T_1 = absorptivity and transmissivity of the cover

α_2, T_2 = absorptivity and transmissivity of layer 2

α_3, T_3 = absorptivity and transmissivity of pottant between PV cells

α_c, T_c = absorptivity and transmissivity of PV cells

α_4, T_4 = absorptivity and transmissivity of layer 4

α_5, T_5 = absorptivity and transmissivity of surface of substrate

η_c = efficiency of PV cell at an assumed cell temperature

P_D = power dissipation due to reverse bias (if $|P_D| > 0$, $\eta_c = 0$)

This formulation neglects radiation reflected from the front and rear surfaces of the PV cell and subsequently absorbed. Thus, any reflected radiation is assumed to be lost.

3.2.2 Energy Balances

The energy balance equations use conservation of energy where the energy into each node must equal the energy leaving that node. These relations can be written as follows:

$$U_{1a}(T_1 - T_a) + q_{1-sky} + U_{12}(T_1 - T_2) + U_{16}(T_1 - T_6) = I_1/A_T$$

$$U_{23}(T_2 - T_3) + U_{21}(T_2 - T_1) + U_{26}(T_2 - T_6) = I_2/A_T$$

$$U_{34}(T_3 - T_4) + U_{32}(T_3 - T_2) + U_{36}(T_3 - T_6) = I_3/A_T$$

$$U_{45}(T_4 - T_5) + U_{43}(T_4 - T_3) + U_{46}(T_4 - T_6) = I_4/A_T$$

$$U_{54}(T_5 - T_4) + U_{56}(T_5 - T_6) + U_{5c}(T_5 - T_c) + U_{5a}(T_5 - T_a) = I_5/A_T$$

$$U_{61}(T_6 - T_1) + U_{62}(T_6 - T_2) + U_{63}(T_6 - T_3) + U_{64}(T_6 - T_4) + U_{65}(T_6 - T_5) \\ + U_{6a}(T_6 - T_a) = 0$$

where

U_{ij} = thermal conductance between nodes i and j based on the area of the thermal cell

U_{ia} = thermal conductance from node i to the ambient

U_{ic} = thermal conductance from node i to the coolant

T_c = average coolant temperature

T_a = ambient temperature

$q_{1\text{-sky}}$ = radiant heat transfer from node 1 (top surface of a flat plate) to the sky

These equations can be written as six simultaneous equations with six unknown temperatures:

$$(U_{1a} + U_{12} + U_{16})T_1 + q_{1\text{-sky}} - U_{12}T_2 - U_{16}T_6 = I_1/A_T + U_{1a}T_a \quad (3-8)$$

$$- U_{21}T_1 + (U_{23} + U_{21} + U_{26})T_2 - U_{23}T_3 - U_{26}T_6 = I_2/A_T \quad (3-9)$$

$$- U_{32}T_2 + (U_{34} + U_{32} + U_{36})T_3 - U_{34}T_4 - U_{36}T_6 = I_3/A_T \quad (3-10)$$

$$- U_{43}T_3 + (U_{45} + U_{43} + U_{46})T_4 - U_{45}T_5 - U_{46}T_6 = I_4/A_T \quad (3-11)$$

$$\begin{aligned}
 - U_{54}T_4 + (U_{54} + U_{56} + U_{5a} + U_{5c})T_5 - U_{56}T_6 &= I_5/A_T + U_{5c}T_c \\
 &+ U_{5a}T_a
 \end{aligned}
 \tag{3-12}$$

$$\begin{aligned}
 - U_{65}T_5 + (U_{61} + U_{62} + U_{63} + U_{64} + U_{65} + U_{6a})T_6 - U_{61}T_1 - U_{62}T_2 \\
 - U_{63}T_3 - U_{64}T_4 &= U_{6a}T_a
 \end{aligned}
 \tag{3-13}$$

In these relations the conductances are symmetric; that is

$$U_{ij} = U_{ji}$$

and if a center cell is considered, node 6 is not used since it is an edge node and therefore,

$$U_{i6} = U_{6i} = 0$$

Also, the term q_{l-sky} is a function of the surface temperature T_l .

These equations are generic and will be used to determine the temperature distribution in a module for various geometries and material configurations. In subsequent sections the thermal conductances, U_{ij} , will be derived.

3.3 FLAT PLATE PV MODULE

The flat plate PV module configuration assumes front surface cooling by natural air flow and has three options for cooling the back surface: an insulated (adiabatic) back, an air cooled back (with or without fins), and a forced liquid cooled back. The thermal conductances for these configurations will be identical except for the conductance from node 5 (the back surface). These conductances will be derived in the following sections.

3.3.1 Insulated Back

The energy radiated from the top surface can be calculated from the expression

$$q_{sky} = \left\{ \epsilon_g \sigma T_a^4 (0.39 - 0.0096e) \left[1 - a_3(cc) \right] + 4\epsilon_g \sigma T_a^3 (T_l - T_a) \right\} F_{l-sky} A_T
 \tag{3-14}$$

where

ϵ_g = emmissivity of cover material

e = vapor pressure of atmospheric water vapor in mm Hg

cc = cloud cover in tenths

a_3 = emperical constant given in table 3-1

σ = Stephan-Boltzman constant

T_a = absolute ambient temperature

$F_{1\text{-sky}}$ = view factor from the panel to the sky

T_1 = absolute surface temperature node 1

The saturation vapor pressure of water vapor (P_{ws}) in atmospheres is given by

$$\log_{10}(P_{ws}/218.2) = \frac{-\delta}{T_a} \left[(a + b\delta + c\delta^3)/(1 + d\delta) \right] \quad (3-15)$$

where

$$\delta = 647.27 - T_a$$

$$a = 3.244$$

$$b = 5.868 \times 10^{-3}$$

$$c = 1.170 \times 10^{-8}$$

$$d = 2.188 \times 10^{-3}$$

and T_a is in $^{\circ}\text{Kelvin}$. The vapor pressure of water vapor in mm Hg is then obtained from the expression

$$e = 760.2\phi P_{ws} \quad (3-16)$$

where ϕ is the relative humidity. The view factor is given by

$$F_{1\text{-sky}} = \cos^2 \frac{\beta}{2} \quad (3-17)$$

where β is the tilt angle from the horizontal.

TABLE 3-1. VALUE OF COEFFICIENT a_3 FOR THE SKY FLUX EQUATION (3-14)

LATITUDE	a_3
5	0.50
10	0.52
15	0.55
20	0.59
30	0.63
40	0.68
50	0.72
60	0.76
70	0.80
80	0.84
85	0.86

The convective heat transfer coefficient for heat loss to the ambient consists of forced and free convection components. For outside surfaces exposed to the weather, the maximum of the forced or free convective coefficients is taken [2]. Thus

$$h_c = \text{Max} \left[h_{c \text{ free}}, h_{c \text{ forced}} \right] \quad (3-18)$$

The forced convective coefficient for wind blowing over an inclined plate is essentially independent of angle so that

$$h_{c \text{ forced}} = 0.86 \frac{k_a}{L_e} \text{Re}^{1/2} \text{Pr}^{1/3} \quad (3-19)$$

where for air $\text{Pr} \approx 0.72$, and

$$\text{Re} = \frac{VL_e}{\nu}$$

where

Pr = Prandtl Number

Re = Reynolds Number

V = air speed

$\nu = \mu/\rho$ = kinematic viscosity

k_a = thermal conductivity of air

L_e = an effective length $\equiv \frac{(4)(\text{Plate area})}{\text{Plate Perimeter}}$ (3-20)

The free convective heat transfer coefficient depends on the tilt angle and the surface temperature of the glass covering. In most cases the free convective flow over a PV module will be turbulent. Thus, the turbulent free convective heat transfer coefficient is given by [3]

$$h_{c\text{free}} = 0.14 \frac{k_a}{L} \text{Pr}^{0.084} (\text{Ra}_L \cos \beta)^{1/3}, \quad 0 < \beta < 81^\circ \quad (3-21)$$

$$h_{c\text{free}} = 0.1 \frac{k_a}{L} \text{Pr}^{0.084} (\text{Ra}_L \sin \beta)^{1/3}, \quad 81^\circ < \beta < 170^\circ \quad (3-22)$$

where equation (3-22) is applicable to near vertical panels or to the back side of a free standing panel. In these relations the Rayleigh number is defined as

$$\text{Ra}_L = \frac{g\beta(T_1 - T_a)L^3}{\nu\alpha} \quad (3-23)$$

where

L = length of the module

β = coefficient of expansion for air

$\alpha = k/\rho C_p$ = thermal diffusivity for air

ρ = air density

C_p = specific heat of air

g = gravitational constant

Since the temperature of the top surface is required to calculate the free convection heat transfer coefficient, an iterative process is required to solve the simultaneous equations for the temperature distribution.

The conductance from the surface of the module to ambient is given by

$$U_{1a} = h_c \quad (3-24)$$

The heat transfer from node 2 to 1 involves thermal conduction through half the encapsulant and through the cover material. The thermal resistance of the encapsulant is

$$R_{2k} = \frac{\tau_2}{2k_2} \quad (3-25)$$

and the resistance of the cover is

$$R_{1k} = \frac{\tau_1}{k_1} \quad (3-26)$$

Since these resistances are in series

$$R_{12} = \frac{\tau_2}{2k_2} + \frac{\tau_1}{k_1} = \frac{k_1 \tau_2 + 2k_2 \tau_1}{2k_1 k_2} \quad (3-27)$$

and

$$U_{12} = \frac{1}{R_{12}} = \frac{2k_1 k_2}{k_1 \tau_2 + 2k_2 \tau_1} \quad (3-28)$$

where

k_1 , k_2 are the conductivities of medium 1 and 2

τ_1 , τ_2 are the thicknesses of medium 1 and 2

If an edge cell is being analyzed, the conduction from node 1 to the aluminum frame must be determined. This includes lateral conduction through medium 1 and conduction through the seal, gasket and aluminum frame. The heat transferred from the center of the thermal cell to the surface of the frame is given by

$$q_{16} = U_{16} A_T (T_1 - T_6) = h_{1s} A_1 (T_1 - T_s) = h_{sg} A_1 (T_s - T_g) = h_{g6} A_1 (T_g - T_6) \quad (3-29)$$

and

$$T_1 - T_6 = (T_1 - T_s) + (T_s - T_g) + (T_g - T_6) \quad (3-30)$$

where h_{1s} , h_{sg} and h_{g6} are the conductances from the center of the cell to the seal, from the seal to the gasket and from the gasket to node 6, respectively. The area for heat transfer is

$$A_1 = \tau_1 L_T$$

where

$$L_T = \text{length of the thermal cell}$$

Also,

$$h_{1s} = \frac{k_1}{W}, \quad h_{sg} = \frac{k_s}{\tau_s}, \quad h_{g6} = \frac{k_g}{\tau_g}$$

where

W = distance from the center of the thermal cell to the seal

k_s , τ_s = conductivity and thickness of the seal

k_g , τ_g = conductivity and thickness of the gasket

From equations 3-29 and 3-30

$$T_1 - T_6 = \frac{U_{16} A_T}{h_{1s} A_1} (T_1 - T_6) + \frac{U_{16} A_T}{h_{sg} A_1} (T_1 - T_6) + \frac{U_{16} A_T}{h_{g6} A_1} (T_1 - T_6)$$

or

$$U_{16} A_T \left[\frac{1}{h_{1s} A_1} + \frac{1}{h_{sg} A_1} + \frac{1}{h_{g6} A_1} \right] = 1$$

$$U_{16}A_T = \frac{1}{\frac{W}{k_1 \tau_1 L_T} + \frac{\tau_s}{k_s \tau_1 L_T} + \frac{\tau_g}{k_g \tau_1 L_T}}$$

But

$$A_T = W_T L_T$$

where

W_T = width of the thermal cell. Then

$$U_{16} = \frac{1}{\frac{W_T W}{k_1 \tau_1} + \frac{W_T \tau_s}{k_s \tau_1} + \frac{W_T \tau_g}{k_g \tau_1}}$$

or

$$U_{16} = \frac{\frac{\tau_1}{W_T}}{\frac{W}{k_1} + \frac{\tau_s}{k_s} + \frac{\tau_g}{k_g}} \quad (3-31)$$

where the resistance through the aluminum frame has been neglected.

Heat transfer from node 2 to node 3 involves conduction through one-half of medium 2 and one-half of medium 3, where the heat transfer through medium 3 involves parallel conduction through the encapsulant and cell. However, since the conductivity of PV materials is about 2 orders of magnitude greater than the conductivity of the encapsulant, conduction through the encapsulant will be neglected.

$$q_{23} = U_{23}A_T(T_2 - T_3) = h_{2i}A_T(T_2 - T_i) = h_{i3}A_c(T_i - T_3)$$

$$T_2 - T_3 = (T_2 - T_i) + (T_i - T_3)$$

$$T_2 - T_3 = \frac{U_{23}A_T}{h_{2i}A_T}(T_2 - T_3) + \frac{U_{23}A_T}{h_{i3}A_c}(T_2 - T_3)$$

$$U_{23}A_T = \frac{1}{\frac{1}{h_{2i}A_T} + \frac{1}{h_{i3}A_c}}$$

where

$$h_{2i} = \frac{2k_2}{\tau_2} \text{ and } h_{i3} = \frac{2k_c}{\tau_c}$$

so that

$$U_{23} = \frac{1}{\frac{\tau_2}{2k_2} + \frac{\tau_c A_T}{2k_c A_c}} = \frac{2}{\frac{\tau_2}{k_2} + \frac{\tau_c A_T}{k_c A_c}} \quad (3-32)$$

Heat transfer from node 2 to the frame consists of lateral conduction through medium 2, the seal and the gasket. Then equation 3-33 is obtained similarly to the derivation of equation 3-31.

$$U_{26} = \frac{\frac{\tau_2}{W_T}}{\frac{W}{k_2} + \frac{\tau_s}{k_s} + \frac{\tau_g}{k_g}} \quad (3-33)$$

Heat transfer from node 3 to 4 is similar to that from node 2 to 3.

Thus

$$U_{34} = \frac{2}{\frac{\tau_4}{k_4} + \frac{\tau_c A_T}{k_c A_c}} \quad (3-34)$$

where again the conductivity of the pottant (or encapsulant) is neglected compared to that of the PV material.

Heat transfer from node 3 to the frame consists of lateral conduction through the PV cell, the encapsulant, the seal and the gasket. Using a derivation similar to that used to obtain equation 3-31 one gets

$$U_{36} = \frac{\frac{\tau_3}{W_T}}{\frac{W_c}{k_c} + \frac{(W - W_c)}{k_e} + \frac{\tau_s}{k_s} + \frac{\tau_g}{k_g}} \quad (3-35)$$

where

W_c = width of the PV cell

k_e = conductivity of the encapsulant

Heat transfer from node 4 to node 5 consists of conduction through one-half the thickness of the lower encapsulant (or adhesive), and through the substrate. Thus

$$U_{45} = \frac{1}{\frac{\tau_4}{2k_4} + \frac{\tau_5}{k_5}} \quad (3-36)$$

If the substrate (node 5) consists of several layers (i.e., tedlar, metal, back cover film), then this becomes

$$U_{45} = \frac{1}{\frac{\tau_4}{2k_4} + \sum_{i=1}^N \frac{\tau_i}{k_i}} \quad (3-37)$$

where i refers to the various layers associated with the substrate.

Conductance from node 4 to the frame is given by

$$U_{46} = \frac{\frac{\tau_4}{W_T}}{\frac{W}{k_4} + \frac{\tau_s}{k_s} + \frac{\tau_g}{k_g}} \quad (3-38)$$

Conductance from node 5 to the aluminum frame consists of parallel conduction through the various layers which make up the substrate. Letting the conductivity and the thickness of these layers be denoted by k_i and τ_i , respectively, one obtains

$$U_{56} = \frac{\frac{\tau_5}{W_T}}{\frac{W \tau_5}{\sum_{i=1}^N k_i \tau_i} + \frac{\tau_s}{k_s} + \frac{\tau_g}{k_g}} \quad (3-39)$$

where

$$\tau_5 = \sum_{i=1}^N \tau_i$$

For an insulated back, the transverse heat transfer from node 5 is zero, and since there is no coolant

$$U_{5a} = 0 \quad \text{and} \quad U_{5c} = 0 \quad (3-40)$$

Heat transfer from node six consists primarily of convection to the ambient and the conductance is obtained as follows:

$$q_{6a} = U_{6a} A_T (T_6 - T_a) = h_{c6} A_6 (T_6 - T_a)$$

$$U_{6a} = h_{c6} \frac{A_6}{A_T} = h_{c6} \frac{\tau_6 L_T}{W_T L_T} = h_{c6} \frac{\tau_6}{W_T} \quad (3-41)$$

where τ_6 is the width of the aluminum frame. Convection from a vertical surface may be free or forced convection so that

$$h_{c6} = \text{Max} \left[h_{c6 \text{ free}}, h_{c6 \text{ forced}} \right] \quad (3-42)$$

where

$$h_{c6 \text{ free}} = 0.48 \frac{k_a}{\tau_6} (Gr_{\tau_6})^{1/4} \quad (3-43)$$

for laminar free convection in air⁽⁴⁾,

and

$$Gr_{\tau 6} = \frac{g \beta (T_6 - T_a) \tau_6^3}{\nu^2} \quad (3-44)$$

Assuming turbulent forced convection [2]

$$h_{c6 \text{ forced}} = 0.86 \frac{k_a}{L_s} Re^{1/2} Pr^{1/3} \quad (3-45)$$

where

$$Re = \frac{VL_s}{\nu}$$

$$L_s = \text{effective length of the frame} = \frac{(4) (\text{area})}{\text{perimeter}}$$

The procedure for calculating the temperature distribution throughout the thermal cell is given in section 3.5.

3.3.2 Front and Back Surfaces Air Cooled With an Optional Finned Back

In this option, all the conductances remain the same as in the previous option except $U_{5a} \neq 0$ as indicated in equation 3-40. Heat transfer from the back surface now consists of radiation and convection to the ambient. Assuming the back surface faces very little sky and radiates to the ambient, the radiation heat transfer coefficient is

$$h_{r5} = \epsilon_5 \sigma (T_5^2 + T_a^2) (T_5 + T_a) \quad (3-46)$$

where ϵ_5 is the emissivity of the back surface.

Convection from the substrate to the ambient again consists of forced and/or free convection and is given by

$$h_{c5} = \text{Max} [h_{c5 \text{ free}}, h_{c5 \text{ forced}}] \quad (3-47)$$

where h_{c5free} is given by equation 3-22 and $h_{c5forced}$ is given by equation 3-19. If fins are attached to the back surface, the convection coefficient becomes [5]

$$h_{c5} = \text{Max} \left[h_{c5free}, h_{c5forced} \right] (8.3 - 7.8e^{-0.071r}) \quad (3-48)$$

where

r = ratio of heat exchange area to root area for a finned heat exchanger

Thus, the conductance from the substrate to the ambient is given by

$$U_{5a} = h_{r5} + h_{c5} \quad (3-49)$$

Since there is no coolant other than natural air circulation or wind,

$$U_{5c} = 0 \quad (3-50)$$

3.3.3 Front Surface Air Cooled and Back Surface Liquid Cooled

In this option, heat is removed from the substrate by conduction along the substrate to the coolant tubes and convection to the coolant, or it is radiated and convected from the back surface. The conductance for radiation and convection to the ambient is given by equation 3-49.

The conductance to the cooling fluid is given by

$$U_{5c} = \frac{1}{\frac{1}{h_{5w}} + \frac{1}{h_{wf}\pi DN}} \quad (3-51)$$

where

D = diameter of the cooling tubes

N = number of tubes per unit length

h_{5w} = equivalent conductance through the substrate to the tube wall

h_{wf} = convective heat transfer coefficient for heat transfer from the tube wall to the cooling fluid

For conduction of heat to the cooling tubes[5]

$$h_{5w} = 12N^2 k_5 \tau_5 \quad (3-52)$$

where k_5 is the conductivity of the metal substrate. For convection to the fluid,

$$h_{wf} = 0.023 \frac{k_f}{D} Re^{0.8} Pr^{1/3} \quad (\text{for } Re \geq 10000, \text{ turbulent}) \quad (3-53)$$

where

k_f = conductivity of the fluid

Pr = Prandtl Number of the fluid

$$Pr = \frac{C_p \mu}{k_f}$$

$$Re = \frac{V_f D}{\nu_f}$$

V_f = fluid velocity

ν_f = kinematic viscosity

$$h_{wf} = 4.36 \frac{k_f}{D} \quad (\text{for } Re \leq 2100, \text{ laminar}) \quad (3-54)$$

For Reynolds numbers between 2,100 and 10,000, h_{wf} is found by fitting a quadratic curve between the laminar value at $Re = 2,100$ and the turbulent value at $Re = 10,000$.

The fluid properties are evaluated at the bulk temperature of the fluid which may be taken as the average of the inlet and outlet temperatures. In addition, the fluid temperature, T_c , in equation 3-12 is the bulk temperature

Since the outlet temperature is unknown at this stage, one must assume a temperature for the substrate, T_5 , and calculate T_c using the method below. This T_c is then used in equation 3-12 to calculate the temperature distribution through the thermal cell. If the calculated T_5 equals the assumed substrate temperature, and the calculated T_1 and T_6 equal the assumed values, then the calculation is completed. If not, the new temperatures are used to find the heat transfer coefficients and calculate T_c and the process repeated until agreement is reached.

The average coolant temperature depends on the flow rate and the heat transferred to the coolant. Thus

$$\dot{M}_p C_p N L_f (T_{out} - T_{in}) = U_{5c} A_T (T_5 - T_c)$$

where

L_f = length of the thermal cell transverse to the cooling tubes

$\dot{M}$ = mass flow rate in a single tube

$$T_c = \frac{1}{2} (T_{in} + T_{out})$$

so that

$$T_c = \frac{U_{5c} A_T T_5 + 2 \dot{M}_p C_p N L_f T_{in}}{2 \dot{M}_p C_p N L_f + U_{5c} A_T} \quad (3-55)$$

3.4 CONCENTRATING PV MODULES

Concentrating PV systems include point focus Fresnel and line focus Fresnel lens systems, and linear parabolic troughs. The Fresnel lens systems may be actively or passively cooled, but the parabolic trough receiver is only actively cooled.

The laminated structure of the thermal cell will be similar to that for a flat plate module (figure 3-1); however, for concentrating systems it is assumed for the thermal analysis that there is no encapsulating material surrounding the cells. In addition, the area of the heat sink may be greater than the

area of the cell to dissipate the heat more efficiently. The following analysis also neglects side-losses so that the calculated temperatures will be somewhat conservative.

The energy input to the PV cell is obtained from the following relations

$$I_1 = I \alpha_1 \quad (3-56)$$

$$I_2 = I T_1 \alpha_2 \quad (3-57)$$

$$I_3 = I T_1 T_2 (\alpha_c - \eta_c) + P_D \quad (3-58)$$

$$I_4 = I T_1 T_2 T_c \alpha_4 \quad (3-59)$$

$$I_5 = I T_1 T_2 T_c T_4 \alpha_5 \quad (3-60)$$

where the incident energy I is obtained from equation 3-1. The energy balance equations then become

$$(U_{1a} + U_{12})T_1 - U_{12}T_2 = I_1 + U_{1a}T_a \quad (3-61)$$

$$- U_{21}T_1 + (U_{23} + U_{21})T_2 - U_{23}T_3 = I_2 \quad (3-62)$$

$$- U_{32}T_2 + (U_{34} + U_{32})T_3 - U_{34}T_4 = I_3 \quad (3-63)$$

$$- U_{43}T_3 + (U_{45} + U_{43})T_4 - U_{45}T_5 = I_4 \quad (3-64)$$

$$- U_{54}T_4 + (U_{5a} + U_{54} + U_{5c})T_5 = U_{5a}T_a + U_{5c}T_c + I_5 \quad (3-65)$$

3.4.1 Point Focus Fresnel

The radiative heat transfer coefficient for heat loss from the top cover to the lens is

$$h_{r1} = \epsilon_1 \sigma (T_1^2 + T_a^2) (T_1 + T_a) \quad (3-66)$$

where it is assumed that the lens is at ambient temperature, T_a . The convective heat loss is due only to natural convection between the PV cell and the lens since typically Fresnel lens systems are sealed to prevent environmental degradation. Thus, the convective heat transfer coefficient is [6]

$$h_{cl} = 0.074 \frac{k_a}{L_f} Ra^{0.375} \quad (3-67)$$

where

L_f = distance between the lens and PV cell

$$Ra = \frac{g\beta(T_l - T_a)L_f^3}{\nu\alpha}$$

and

$$U_{la} = h_{cl} + h_{rl} \quad (3-68)$$

The internal conductances due to conduction have been derived in the previous section. These are given by the following equations:

$$U_{12} = \frac{2k_1k_2}{2k_2\tau_1 + \tau_2k_1} \quad (3-69)$$

$$U_{23} = \frac{2k_2k_3}{k_3\tau_2 + k_2\tau_3} \quad (3-70)$$

$$U_{34} = \frac{2k_3k_4}{k_3\tau_4 + k_4\tau_3} \quad (3-71)$$

The conductance from node 4 to node 5 consists of conductance through half the bonding material and the metal substrate. However, the substrate may have a larger area than the PV cell in order to spread and dissipate the heat. Thus,

$$U_{45} = \frac{1}{\frac{t_4}{2k_4} + \frac{t_5 A_c}{k_5 A_s}} \quad (3-72)$$

where A_s is the area of the substrate/heat sink.

For the case of passive cooling, the heat transfer from node 5 to the ambient consists of convection and radiation in parallel. The radiative heat transfer coefficient is given by

$$h_{5r} = \epsilon_5 \sigma (T_5^2 + T_a^2) (T_5 + T_a) \quad (3-73)$$

and the convective coefficient is given by [5]

$$h_{5ca} = (9.7V^{0.76} + 3.1)(8.3 - 7.8e^{-0.071r}) \quad (3-74)$$

where V is the wind velocity in meters per second, and the second term is included if the heat sink is finned. Thus, the conductance from node 5 to the ambient is

$$U_{5a} = (h_{5r} + h_{5ca}) \frac{A_s}{A_c} \quad (3-75)$$

For an actively cooled substrate, where the substrate and cooling tube are insulated, node 5 loses thermal energy to the cooling fluid by convection and to the ambient, through the insulation, by radiation and convection. The conductance through the insulation is given by

$$U_{5a} = \frac{1}{\frac{1}{h_{5k}} + \frac{1}{h_{5r} + h_{5ca}}} \frac{A_i}{A_c} \quad (3-76)$$

where A_i is the external area of the insulation. The heat transfer coefficient for conduction is

$$h_{5k} = \frac{k_i}{t_i} \quad (3-77)$$

for convection

$$h_{5ca} = 9.7V^{0.76} + 3.1 \quad (3-78)$$

and for radiation

$$h_{5r} = \epsilon_i \sigma (T_i^2 + T_a^2)(T_i + T_a) \quad (3-79)$$

where T_i is the surface temperature of the insulation.

For convective cooling by the fluid, the heat transfer coefficient is

$$h_{5c} = 0.023 \frac{k_f}{D} Re^{0.8} Pr^{1/3} \quad (\text{for turbulent flow}) \quad (3-80)$$

or

$$h_{5c} = 4.36 \frac{k_f}{D} \quad (\text{for laminar flow}) \quad (3-81)$$

where D is the hydraulic diameter of the cooling channel

$$D = \frac{(4)(\text{cross sectional area})}{\text{wetted perimeter}}$$

so that

$$U_{5c} = h_{5c} \frac{\pi DL}{A_c} \quad (3-82)$$

The average coolant temperature in equation 3-65 is obtained from

$$T_c = \frac{h_{5c} \pi D L N T_5 + 2 M C_p \dot{T}_{in}}{2 M C_p + h_{5c} \pi D L N} \quad (3-83)$$

where N is the number of cells cooled by the channel and L is the distance between PV cells.

To obtain the temperature distribution, one must assume the surface temperatures (T_1 and T_i) to calculate the heat transfer coefficients h_{r1} , h_{c1} and h_{5r} . Then U_{5a} can be calculated, and T_5 calculated from the relation

$$T_5 = \frac{\frac{h_{5k} A_i}{U_{5a} A_c} T_i - T_a}{\frac{h_{5k} A_i}{U_{5a} A_c} - 1} \quad (3-84)$$

and T_c obtained from equation 3-83. The simultaneous equations are then solved for the temperature distribution and the calculated temperatures compared to the assumed temperatures. If the discrepancy is too large (i.e., larger than 1 degree) the process is repeated using calculated temperatures to obtain new heat transfer coefficients.

3.4.2 Line Focus Fresnel

The line focus Fresnel lens system can be analyzed in the same way as the point focus system. The heat transfer coefficients are identical to those for the point focus system except

$$U_{5c} = h_{5c} \frac{\pi D L}{A_c} \quad (3-85)$$

where in this case L is the length of the module. Also, the coolant temperature is given by

$$T_c = \frac{h_{5c} \pi D L T_5 + 2 \dot{M} C_p T_{in}}{2 \dot{M} C_p + h_{5c} \pi D L} \quad (3-86)$$

3.4.3 Linear Parabolic Trough (LPT)

The analysis of a linear parabolic trough is identical to that of a line focus Fresnel except that the convective heat loss from the surface may be due to free or forced convection. The receiver section is not usually insulated so equation 3-75 is used to calculate the conductance to the ambient where h_{5ca} is obtained from equations 3-90 and 3-91. The convective heat transfer coefficients for a horizontal cylinder in air are, for forced convection [7]

$$h_{cl_{forced}} = C \left(\frac{k_a}{D} \right) Re^n \quad (3-87)$$

where Re is the Reynolds number for air flowing across the cylinder

$$Re = \frac{VD}{\nu} \quad (3-88)$$

and

V = wind velocity

D = hydraulic diameter

ν = kinematic viscosity of air

k_a = thermal conductivity of air

The constants in equation 3-87 depend on the value of the Reynolds number and are given in table 3-2.

TABLE 3-2. CONSTANTS FOR USE WITH EQUATION 3-87

<u>Re</u>	<u>C</u>	<u>n</u>
< 4	0.891	0.33
4 - 40	0.821	0.385
40 - 4,000	0.615	0.466
4000 - 40,000	0.174	0.618
40,000 - 400,000	0.0239	0.805

The free convective heat transfer coefficient for a horizontal cylinder is [4,8]

$$h_{cl\_free} = 0.53 Ra^{1/4} \quad \text{for } 10^3 < Ra < 10^9$$

and (3-89)

$$h_{cl\_free} = 0.1 Ra^{1/3} \quad \text{for } Ra > 10^9$$

where Ra denotes the Rayleigh number defined in equation 3-23 with L replaced by the diameter of the cylinder. Thus, the convective heat transfer coefficient is

$$h_{cl} = \text{Max} \left[h_{cl\_free}, h_{cl\_forced} \right] \quad (3-90)$$

Since LPT systems are not usually finned, the convective heat transfer coefficient from the back of the receiver tube is the same as over the PV cell cover so that

$$h_{5ca} = h_{cl} \quad (3-91)$$

If the LPT receiver is a "V" shaped receiver with two rows of PV cells, the cell area is twice the area of a single PV cell.

3.5 METHODOLOGY FOR TEMPERATURE CALCULATION

The general methodology for calculating the temperature distribution is shown in figures 3-3 through 3-13. This procedure will be described in the following sections.

3.5.1 Inputs

Before calculations can begin, the user must define the cell and module geometry, and provide material properties, environmental conditions, and insolation.

The geometry definition will include the following

- Type of Module
 - Flat Plate
 - Point Focus Fresnel

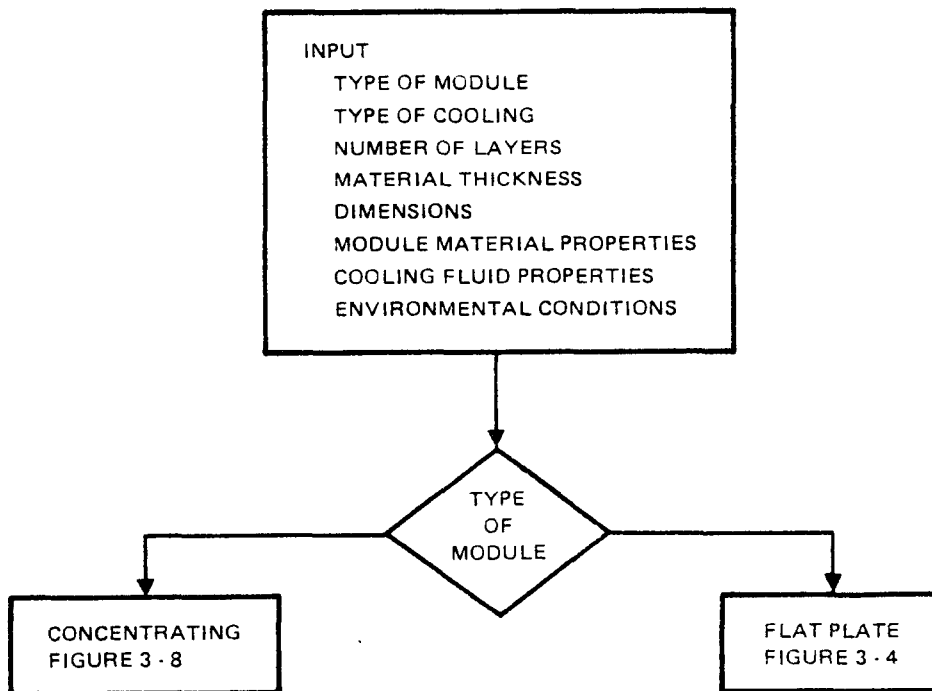


Figure 3-3. Thermal Analysis Top Level Flowchart

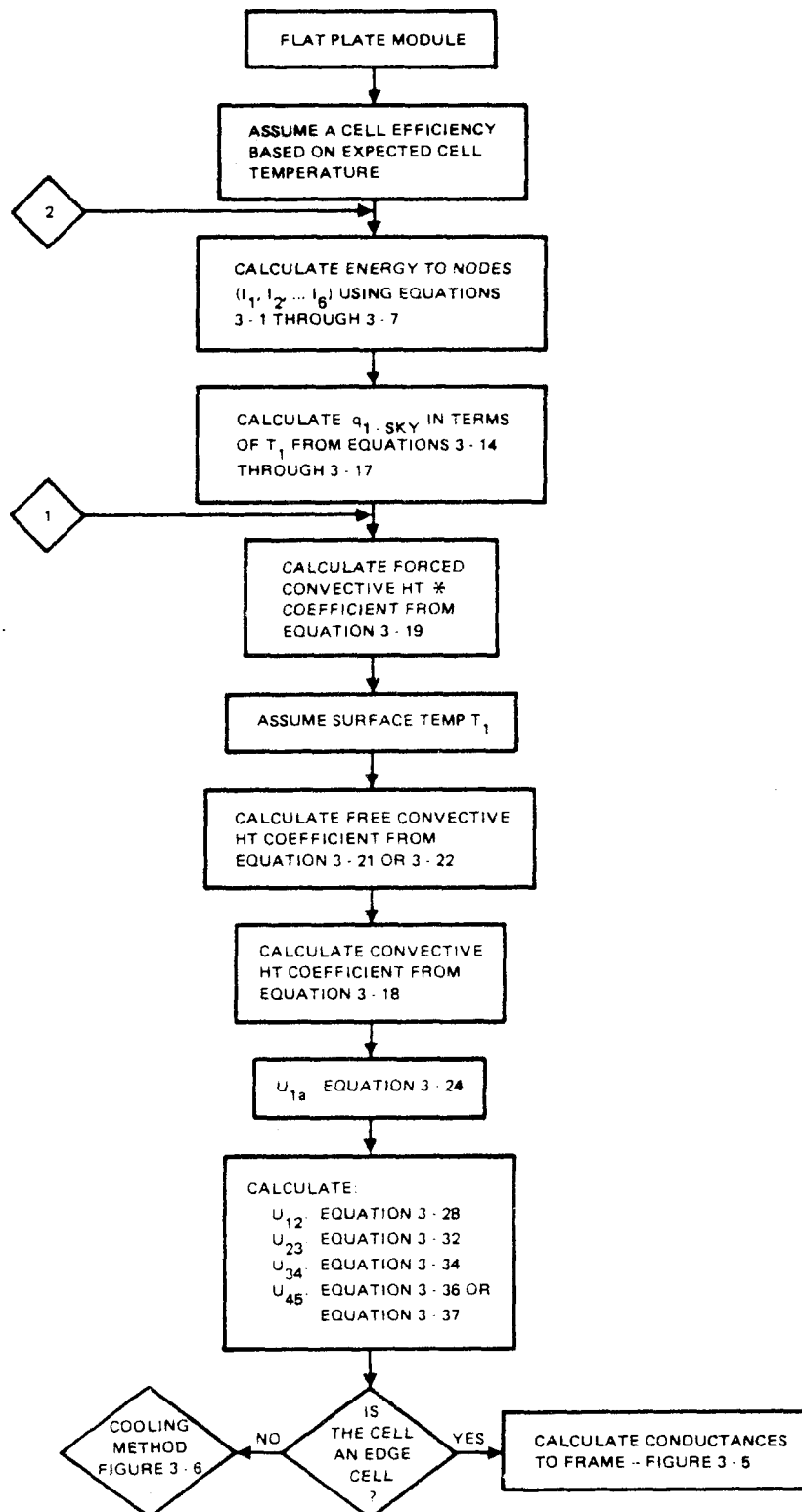


Figure 3-4. Flowchart to Calculate Flat Plate Temperature Distribution
*HT Heat Transfer

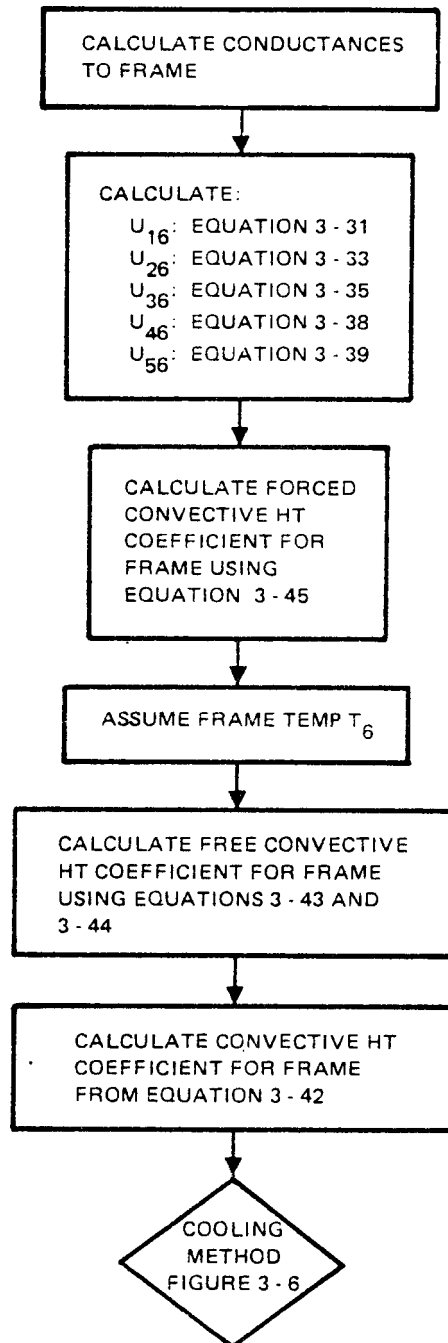


Figure 3-5. Flowchart for Edge Cell Temperature Distribution in Flat Plate Module

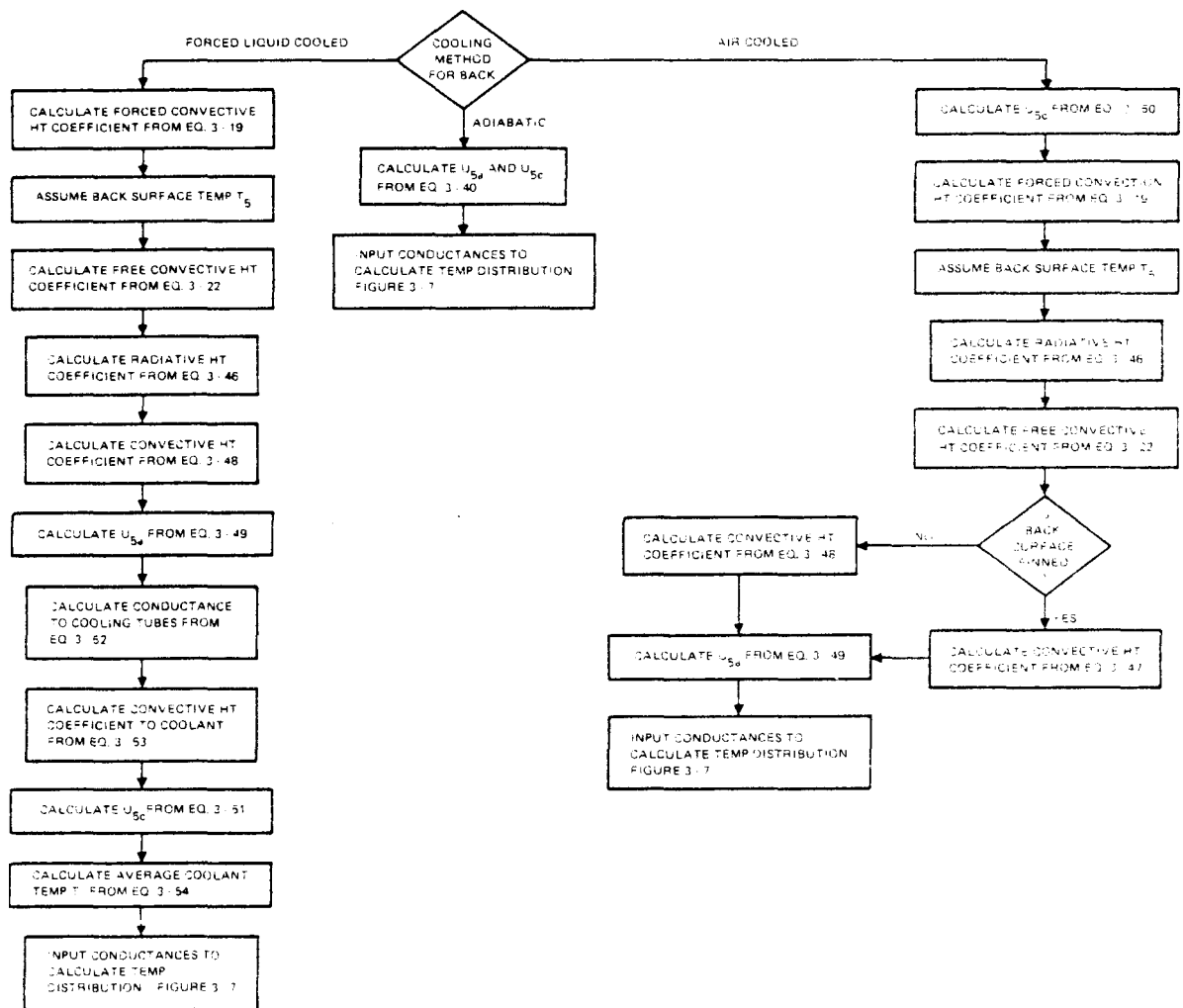


Figure 3-6. Flowchart to Calculate Flat Plate Cooling Conductances

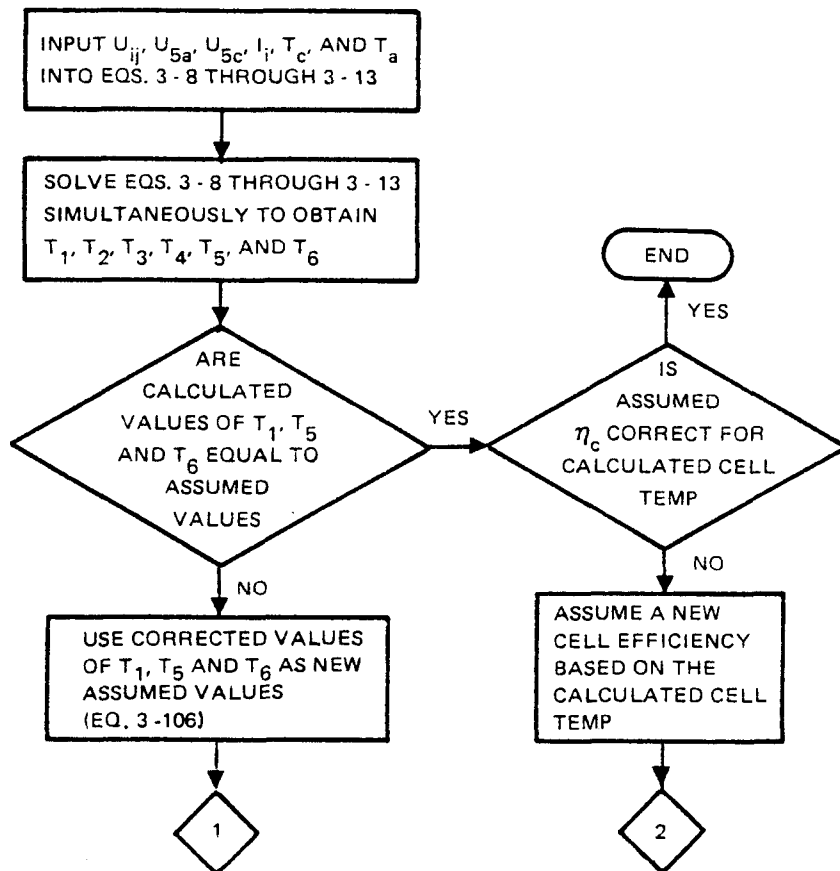
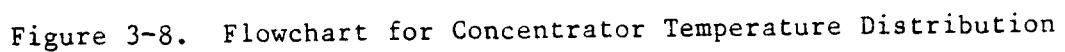


Figure 3-7. Flowchart to Calculate Temperature Distribution in Flat Plate Module



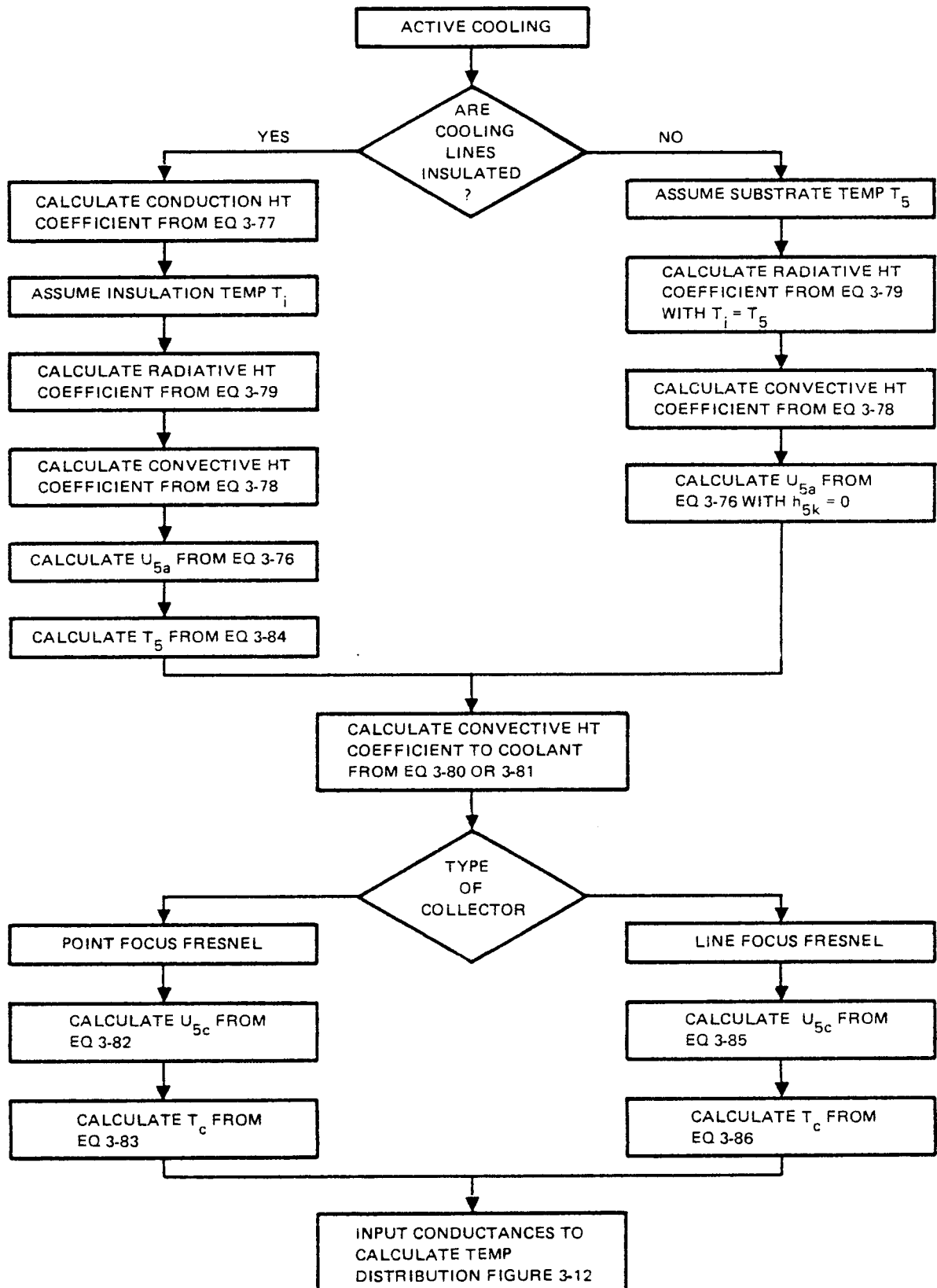


Figure 3-9. Flowchart to Calculate Active Cooling Conductances for Linear and Point Focus Fresnel Systems

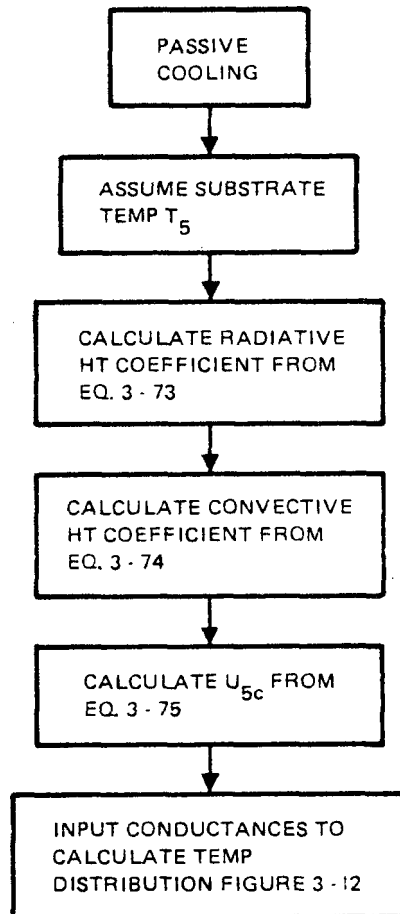


Figure 3-10. Flowchart to Calculate Passive Cooling Conductances for Linear and Point Focus Fresnel Systems

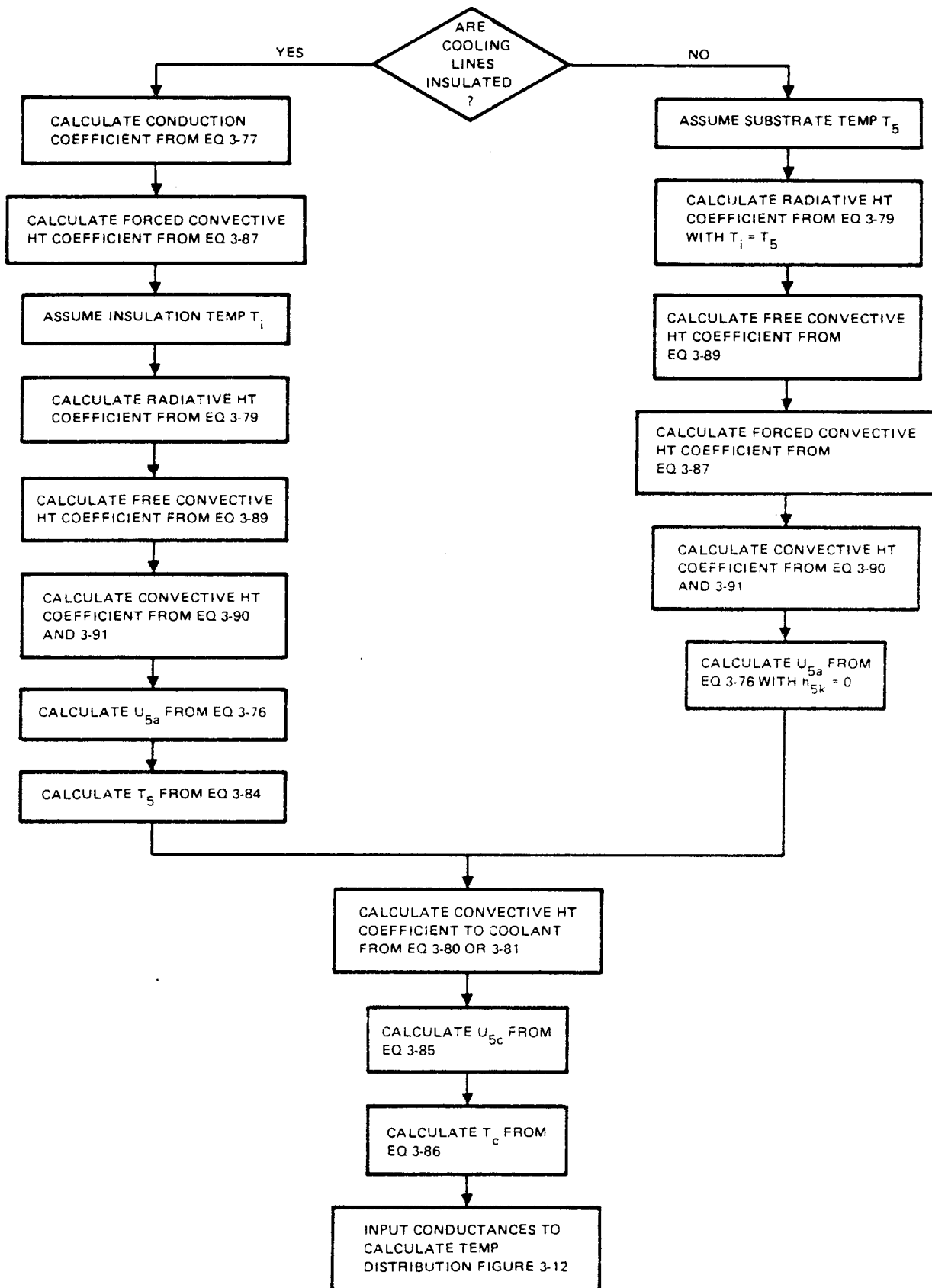


Figure 3-11. Flowchart to Calculate Cooling Conductances for Linear Parabolic Trough Systems

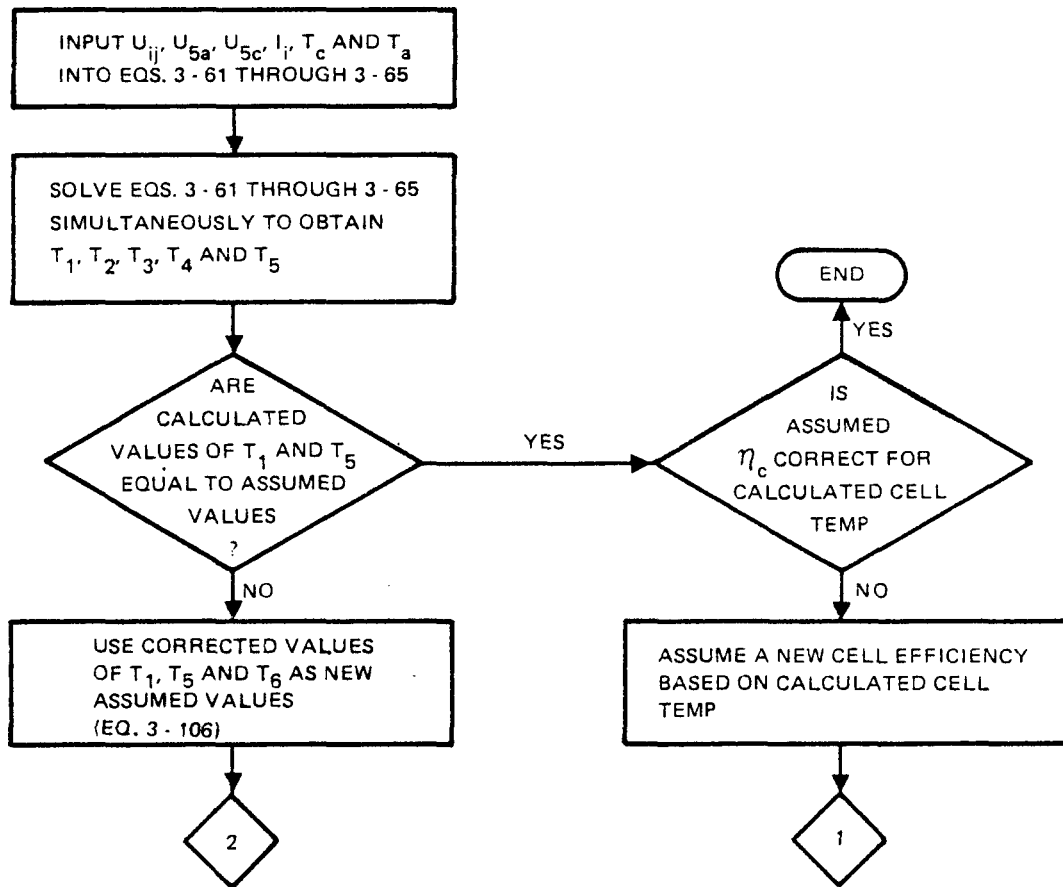


Figure 3-12. Flowchart to Calculate Temperature Distribution

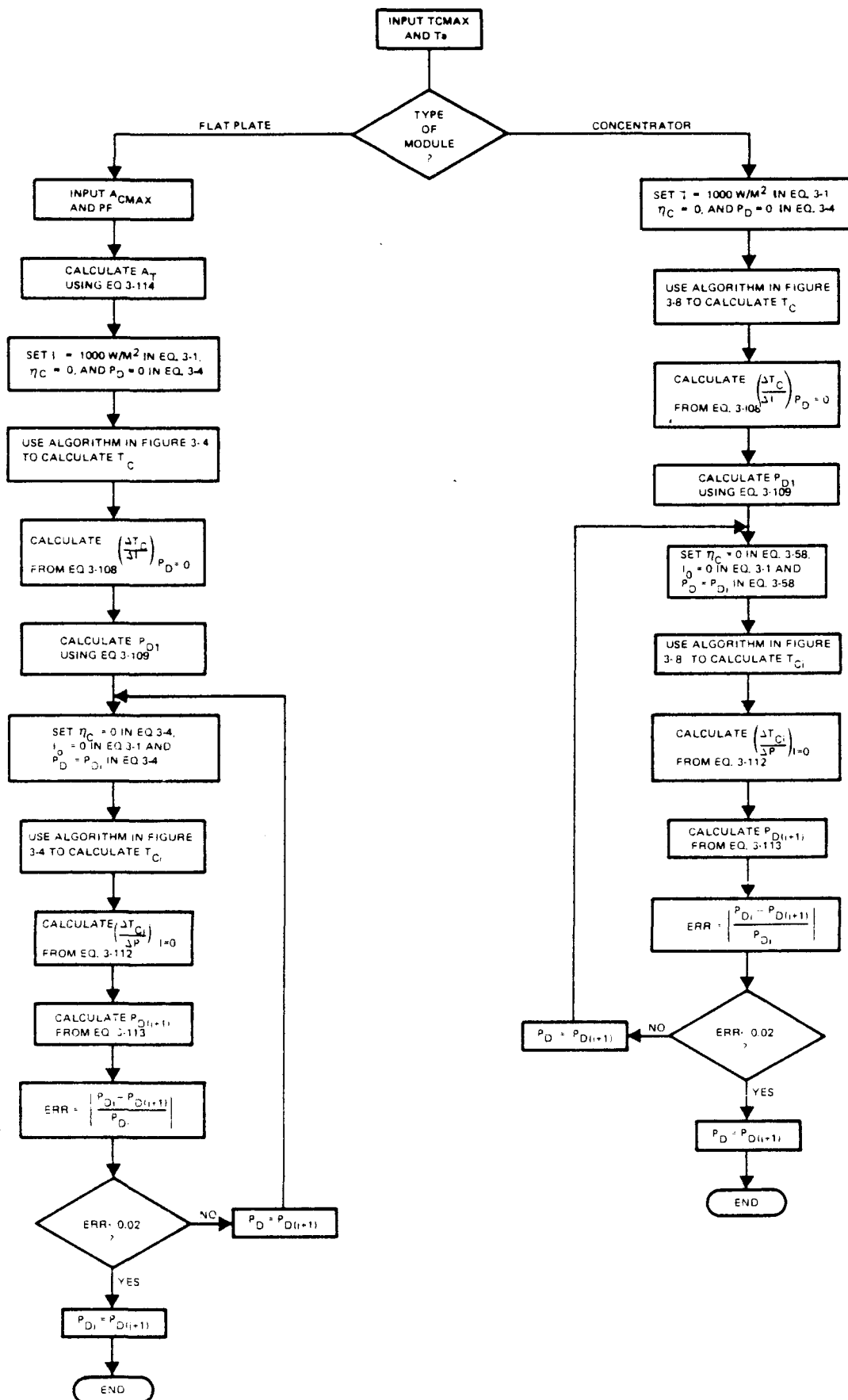


Figure 3-13. Flowchart for Calculation of Maximum Allowable Dissipation in Cell in Reverse Bias

- Line Focus Fresnel
- Linear Parabolic Trough
- Type of Cooling
 - Adiabatic (No Cooling)
 - Passive (With or Without Fins)
 - Active
- Number of Layers
 - Top Cover
 - Top encapsulant
 - PV cell
 - Bottom encapsulant or adhesive
 - Substrate layers in substrate (flat plate only)
- Material Thickness
 - Laminated layers
 - Seal
 - Gasket
 - Substrate layers
- Dimensions
 - Module length and width
 - Thermal cell length and width
 - PV cell length and width
 - Distance between center of thermal cell and edge of module
 - Length and width of frame surface
 - Aperture area
 - Cooling tube diameter
- Number of Cooling Tubes Per Unit Length of Module
- Tilt Angle
- Heat Exchange Area to Root Area for Finned Surfaces

The parameters required for a particular situation will depend on the module being analyzed. For example, if the peak temperature of a cell is required, a center cell should be analyzed so that the distance between the thermal cell and the frame and the characteristics of the frame are not required inputs.

The material properties required include the properties of the laminates, the seal and gasket, and the cooling fluid. Air properties are included in the computer program for a nominal air temperature of 70°F. Other air temperatures will not cause a significant change in the air properties. The following material properties will be required:

- Module Materials
 - Emissivity (top and bottom surface)
 - Transmissivity
 - Absorptivity
 - Conductivity
 - PV cell efficiency
 - Optical efficiency for concentrators

- Cooling Fluid
 - Viscosity
 - Specific heat
 - Prandtl Number
 - Conductivity
- Environmental conditions include:
 - Ambient temperature
 - Relative humidity
 - Wind velocity
 - Insolation incident on the collector aperture
 - Coolant fluid mass flow rate
 - Coolant fluid inlet temperature
 - Power dissipated in cell due to reverse bias
 - Latitude

3.5.2 Energy Input Calculations

With this input data the insolation incident on the collector aperture is obtained from equation 3-1 and the power input to the module is obtained from equation 3-2 through 3-7 for a flat plate collector and equations 3-56 through 3-60 for a concentrator. If there is no power dissipated due to reverse bias then $\eta_c > 0$; however, if $|P_D| > 0$ then $\eta_c = 0$.

The user must identify which node contains the PV cell. With this information these equations can be generalized as follows:

For layers above the PV cell

$$I_i = I A_T \alpha_i \prod_{j=1}^{j=i-1} T_j \quad (3-92)$$

For the layers containing the PV cell

$$I_i = I A_c (\alpha_c - \eta_c) \prod_{j=1}^{j=i-1} T_j + I (A_T - A_c) \alpha_e \prod_{j=1}^{j=i-1} T_j + P_D A_c \quad (3-93)$$

For layers below the PV cell

$$I_i = I \left[(A_T - A_c) + A_c \frac{T_c}{T_e} \right] \alpha_i \prod_{j=1}^{j=i-1} T_j \quad (3-94)$$

where, in the product of transmissivities, the PV cell transmission is not included but T_e is included. For a concentrator they become:

For layers above the PV cell

$$I_i = I \alpha_i \prod_{j=1}^{j=i-1} T_j \quad (3-95)$$

For the PV cell layer

$$I_i = I (\alpha_c - \eta_c) \prod_{j=1}^{j=i-1} T_j + P_D \quad (3-96)$$

For layers below the PV cell

$$I_i = I \alpha_i \prod_{j=1}^{j=i-1} T_j \quad (3-97)$$

where, in the product of transmissivities, the PV cell transmission is included.

In these equations subscript i refers to the i th layer and

T_i = transmissivity of the i th layer

α_i = absorptivity of the i th layer

T_c = transmissivity of the PV cell

α_c = absorptivity of the PV cell

T_e = transmissivity of encapsulant between PV cells in the cell layer

A_T = area of thermal cell

A_c = area of PV cell

P_D = Power dissipated due to reverse bias

To perform these calculations, PV cell efficiency must be assumed based on an expected cell temperature. In subsequent calculations the cell temperature will be determined. The assumed cell efficiency should be compared to the efficiency at the calculated cell temperature. If there is sufficient disagreement the cell efficiency at the calculated temperature is used to determine a new expected cell temperature.

3.5.3 Thermal Conductances

The thermal conductances are calculated based on the area of a thermal cell. If radiation or free convection are important, then the user must assume appropriate surface temperatures to calculate the heat transfer coefficients for surface heat loss.

For a flat plate, radiation from the top surface is to the sky and is given by equation 3-14. In this special case one need not assume a top surface temperature unless free convection dominates over forced convection. The convective heat transfer coefficients are calculated using equations 3-18 and 3-19, 3-21 or 3-22. The heat transfer from the back surface depends on the configuration. If the back surface is insulated it is assumed no heat transfer occurs and $U_{5a} = 0$. For an air cooled surface the convective heat transfer coefficient is given by equation 3-22 or 3-19 and the radiation coefficient is given by equation 3-46; the surface conductance off the back surface is then found from equation 3-49. For a forced liquid cooled back surface the conductance to the air is again obtained from 3-49 and the conductance to the coolant from equation 3-51 and the average coolant temperature from equation 3-55.

Conduction through the layers will depend on the number of layers, their thickness and material properties. These conductances may be generalized as follows:

For the top surface node:

$$U_{1,2} = \frac{2k_1k_2}{k_1\tau_2 + 2k_2\tau_1} \quad (3-98)$$

$$U_{1,6} = \frac{1}{\frac{W_T W}{k_1 \tau_1} + \frac{W_T \tau_s}{k_s \tau_1} + \frac{W_T \tau_g}{k_g \tau_1}} \quad (3-99)$$

For internal nodes where subscript i denotes the i th layer not containing the PV cell and subscript c denotes the PV cell node:

$$U_{i,c} = \frac{2}{\frac{\tau_i}{k_i} + \frac{\tau_c A_T}{k_c A_c}} \quad (3-100)$$

$$U_{c,6} = \frac{\frac{\tau_c}{W_T}}{\frac{W_c}{k_c} + \frac{(W - W_c)}{k_e} + \frac{\tau_s}{k_s} + \frac{\tau_g}{k_g}} \quad (3-101)$$

$$U_{i,i+1} = \frac{2}{\frac{\tau_i}{k_i} + \frac{\tau_{i+1}}{k_{i+1}}} \quad (3-102)$$

$$U_{i,6} = \frac{\frac{\tau_i}{W_T}}{\frac{W}{k_i} + \frac{\tau_s}{k_s} + \frac{\tau_g}{W_g}} \quad (3-103)$$

$$U_{i,5} = \frac{1}{\frac{\tau_i}{2k_i} + \sum_{j=1}^N \frac{\tau_j}{k_j}} \quad (3-104)$$

$$U_{5,6} = \frac{\frac{t_5}{W_T}}{\frac{W t_5}{\sum_{j=1}^N k_j t_j} + \frac{\tau_s}{k_s} + \frac{\tau_g}{k_g}} \quad (3-105)$$

The variables appearing in these equations are defined as follows:

τ_i = thickness of the i th layer

k_i = conductivity of the i th layer

t_c, k_c = thickness and conductivity of the PV cell

t_s, k_s = thickness and conductivity of the frame seal

t_g, k_g = thickness and conductivity of the frame gasket

k_e = conductivity of encapsulant between PV cells in the cell layers

W_T = width of thermal cell

W_c = width of PV cell

W = distance between center of PV cell and frame seal

N = number of layers in the substrate (i.e., tedler steel, tedler substrate)

These conductances, along with the ambient temperature, coolant temperature (if applicable) and input energy are substituted into the equations 3-8 through 3-13. These simultaneous equations are then solved for the temperature distribution.

For point focus Fresnel collectors, the heat transfer off the front face is due to radiation, equation 3-66, and free convection, equation 3-67. Thus, the front face temperature must be assumed to calculate the conductance, equation 3-68. If the back surface is passively cooled, the surface temperature must be assumed to calculate the radiative heat transfer coefficient from equation 3-73. The convective coefficient is obtained from equation 3-74 and the conductance from equation 3-75. For an actively cooled substrate the conductance to the ambient is obtained from equation 3-76 and equations 3-77, 3-78 and 3-79 and conductance to the coolant from equations 3-80 or 3-81 and 3-82. The average coolant temperature is obtained from equation 3-83 and the substrate temperature obtained from equation 3-84 for an assumed temperature of the insulation surface, T_i . The conduction through the layers is easily calculated from equations 3-69 through 3-72.

The analysis of a line focus Fresnel module uses the same relations except for heat transfer to the cooling fluid. In this case the conductance is given by equation 3-85 and average coolant temperature by equation 3-86.

A parabolic trough analysis is identical to that for a Fresnel lens system except for the convective heat transfer coefficient. Thus, the heat transfer coefficient for the front face due to radiation is obtained from equation 3-66, due to forced convection from equation 3-87 and due to free convection from equation 3-89. Equations 3-90 and 3-66 are then used in equation 3-68 to obtain the conductance for the front surface. The rear surface is cooled by

convection to the air and to the cooling fluid. Conductance to the cooling fluid is obtained from equations 3-80 or 3-81 and 3-82. Conductance to the ambient is obtained from equations 3-73, 3-91 and 3-75.

Procedures for calculating the temperature distribution in various types of modulus are contained in the flowcharts in figures 3-5 through 3-12.

When the initial calculation is completed, the calculated temperatures are compared to the assumed temperatures used to determine the heat transfer coefficients. If there is disagreement, new trial temperatures are obtained using equation 3-106

$$T_{\text{TRIAL NEW}} = T_{\text{TRIAL OLD}} + 1/2 \left(T_{\text{CALC}} - T_{\text{TRIAL OLD}} \right) \quad (3-106)$$

3.6 POWER DISSIPATION DUE TO REVERSE BIAS

For a normally operating PV cell, $P_D = 0$ and cell efficiency is positive and a function of temperature. However, if shadowing occurs the cell goes into reverse bias and the magnitude of the power dissipated in the cell becomes greater than zero while the cell efficiency goes to zero. This occurs even if there is only partial shadowing so that the cell temperature is a function of both insolation and power dissipation. This functional relation can be written as

$$\Delta T_c = \left(\frac{\Delta T_c}{\Delta I} \right)_{P_D=0} I + \left(\frac{\Delta T_c}{\Delta P} \right)_{I=0} P_D \quad (3-107)$$

where $\Delta T_c = T_c - T_a$, T_a is the ambient temperature and the differentials are evaluated at zero cell efficiency.

To determine the maximum allowable power dissipation, a worst case situation is assumed where the incident direct normal insolation is taken as 1000 watts/m². The thermal model is then used to calculate the cell temperature under the conditions $I_0 = 1000$ watts/m², $P_D = 0$ and $\eta_c = 0$. Then

$$\left(\frac{\Delta T_c}{\Delta I} \right)_{P_D=0} = \frac{T_c - T_a}{I} \quad (3-108)$$

where I is the insolation calculated from equation 3-1. If the calculated cell temperature, T_c , is greater than T_{CMAX} , a new maximum cell temperature should be assumed or a module redesign accomplished. An initial value of T_c is then obtained from equation 3-109 for a user defined maximum allowable cell temperature, T_{CMAX} .

$$P_{D1} = \frac{T_{CMAX} - T_a - \left(\frac{\Delta T_c}{\Delta I} \right)_{P_D=0} I}{\left(\frac{\Delta T_c}{\Delta I} \right)_{P_D=0}} \quad (3-109)$$

Using this initial value of power dissipation in the thermal model, with $I_o = 0$ and $\eta_c = 0$, a new cell temperature is calculated and the second differential in equation 3-107 is obtained using equation 3-110.

$$\left(\frac{\Delta T_{c1}}{\Delta P} \right)_{I=0} = \frac{T_{c1} - T_a}{P_{D1}} \quad (3-110)$$

A new value for the power dissipation is then obtained in equation 3-111.

$$P_{D2} = \frac{T_{CMAX} - T_a - \left(\frac{\Delta T_c}{\Delta I} \right)_{P_D=0} I}{\left(\frac{\Delta T_{c1}}{\Delta P} \right)_{I=0}} \quad (3-111)$$

This new value of power dissipation is again used in the thermal model to obtain a new cell temperature under the conditions of $I = 0$ and $\eta_c = 0$. The process is repeated using equations 3-112 and 3-113 until $P_{Di} = P_{D(i+1)}$.

$$\left(\frac{\Delta T_{ci}}{\Delta P} \right)_{I=0} = \frac{T_{ci} - T_a}{P_{Di}} \quad (3-112)$$

$$P_{D(i+1)} = \frac{T_{CMAX} - T_a - \left(\frac{\Delta T_c}{\Delta I} \right)_{P_D=0} I}{\left(\frac{\Delta T_{ci}}{\Delta P} \right)_{I=0}} \quad (3-113)$$

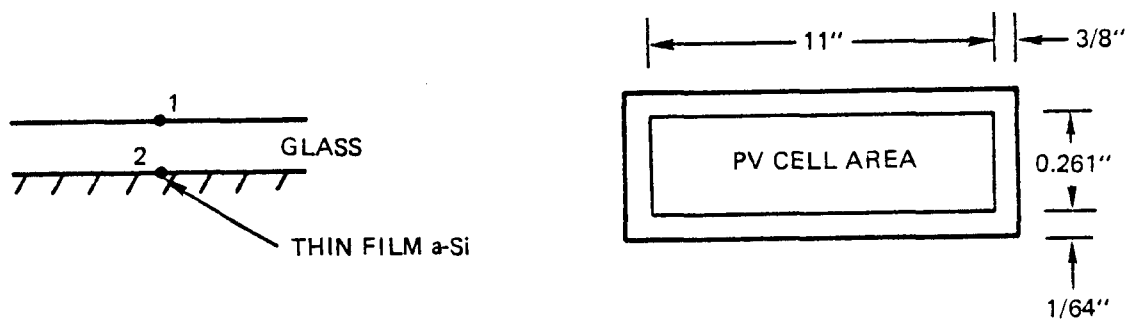
When convergence is obtained, P_{Di} is the maximum allowable power dissipation. This calculation procedure is shown in figure 3-13. When using the thermal

model to obtain the cell temperature, a center cell calculation should be performed to minimize the number of inputs required at the early stages of module optimization. For thermal calculations the power dissipated is taken to be a positive value (that is, a positive energy input to the cell); however, for electrical calculations the power dissipation is usually taken as a negative value. Therefore, when using power dissipation in electrical calculations the sign should be reversed. If a maximum cell area and packing fraction (PF) can be assumed, then the area of the thermal cell (for a flat plate) is obtained from the relation

$$A_T = \frac{A_c}{PF} \quad (3-114)$$

3.7 EXAMPLE

Consider a simple case of a flat plate module 11 3/4 inches wide by 47 1/2 inches long insulated on the back (i.e., mounted directly to a well insulated roof). The module consists of a glass superstrate upon which is layed down a thin film of transparent conducting material (such as indium tin oxide), a thin film of amorphous silicon, metallization, and a thin film of some protective material sprayed over the back of the module. The thermal cell could be as shown in figure 3-14.



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Figure 3-14. Example Thermal Cell

The thin film material deposited on the back of the glass superstrate would not affect the heat transfer characteristics of the glass superstrate above. Therefore, the only material characteristics required are as shown in table 3-3.

TABLE 3-3. REQUIRED INPUT DATA FOR THE EXAMPLE THERMAL ANALYSIS

Glass	$T = 0.8$ $\alpha = 0.065$ $\epsilon = 0.92$	Dimensionless	Geometry	PV cell - 0.261" x 11" Thermal cell - 0.2923" x 11.75" Module - 11.75" x 47.5" Tilt angle - 30°
	$k = 0.45 \text{ BTU/hr. ft. } ^\circ\text{F}$ $\tau = 0.125 \text{ inches}$		Environment	No cloud cover No humidity Air speed - 1m/sec Insolation - 1000 W/m ² Ambient temperature - 70°F
PV Cell	$\alpha_c = 0.98$ $\eta_c = 0.1$ $\alpha_e = 0.15$			

From equations 3-92 and 3-93

$$I_1 = I A_T \alpha_1 = 0.4917 \text{ BTU/hr}$$

$$I_2 = I A_c (\alpha_c - \eta_c) T_1 + I (A_T - A_c) \alpha_e T_1 = 4.603 \text{ BTU/hr}$$

where α_e is the absorptivity of the material applied to the back of the PV cell, and where one W/m² equals 0.317 BTU/hr ft².

Conductances are calculated from the following relations

1. Convection - Equations 3-19, 3-20 and 3-24

$$h_{c_{\text{forced}}} = 0.86 \frac{k_a}{L_e} \text{Re}^{1/2} \text{Pr}^{1/3}$$

$$k_a = 0.015 \text{ BTU/hr ft } ^\circ\text{F}$$

$$\nu_a = 0.17 \times 10^{-3} \text{ ft}^2/\text{sec}$$

$$\text{Pr} = 0.72$$

$$L_e = \frac{(4)(\text{Plate area})}{\text{plate perimeter}} = 1.57 \text{ ft}$$

$$Re = \frac{VL_e}{\nu_a} = 3.04 \times 10^4$$

$$h_{c_{\text{forced}}} = 1.29 \text{ BTU/hr ft}^2 \text{ } ^\circ\text{F}$$

$$U_{1a} = 1.29 \text{ BTU/hr ft}^2 \text{ } ^\circ\text{F}$$

2. Radiation - equation 3-14

$$q_{1\text{-sky}} = \epsilon_1 \sigma T_a^3 (4T_1 - 3.61T_a) F_{1\text{-sky}}$$

$$F_{1\text{-sky}} = \cos^2 \frac{\beta}{2} = 0.933$$

$$q_{1\text{-sky}} = 0.88 T_1 - 419.1$$

3. Conduction - Equation 3-100

$$U_{12} = \frac{k_1}{\tau_1} = 43.2 \text{ BTU/hr ft}^2 \text{ } ^\circ\text{F}$$

where $\tau_c = 0$

These conductances are then used in equations 3-8 and 3-9

$$(U_{1a} + U_{12})T_1 + q_{1\text{-sky}} - U_{12}T_2 = I_1/A_T + U_{1a}T_a$$

$$- U_{12}T_1 + U_{21}T_2 = I_2/A_T$$

Substituting the values of conductances and energy input gives

$$44.5T_1 + 0.88T_1 - 419.1 - 43.2T_2 = 20.62 + (1.29)(530)$$

$$- 43.2T_1 + 43.2T_2 = 193$$

or

$$45.38T_1 - 43.2T_2 = 1117.27$$

$$- 43.2T_1 + 43.2T_2 = 193$$

$$T_1 = 601 \text{ } ^\circ\text{R} = 141 \text{ } ^\circ\text{F}$$

$$T_2 = 605.5 \text{ } ^\circ\text{R} = 145.5 \text{ } ^\circ\text{F}$$

3.8 THERMAL ALGORITHM GLOSSARY

<u>Symbols</u>	<u>Definition</u>
A_a	Aperture area
A_c	Area of a PV Cell
A_m	Area of the module
A_T	Area of the thermal cell
a_3	Coefficient for sky flux equation
α	Thermal diffusivity of air
α_n	Absorptivity of layer (Node) n
β	Tilt angle of array from horizontal
β	Coefficient of thermal expansion for air (Rayleigh Number equation)
cc	Cloud cover (in tenths)
C_p	Specific Heat of Air
D	Cooling tube diameter
e	Vapor pressure of water vapor
g	Emissivity of cover material
F_{l-sky}	View factor from the panel to the sky
g	Gravitational constant
Gr	Grashoff Number
h_c	Convective heat transfer coefficient
I_o	Insolation incident on the lens or trough aperture
k_a	Thermal conductivity of air
K_f	Conductivity of cooling fluid
K_i	Thermal conductivity of layer (Node) i
L_e	Effective Module Length
L_f	Length of thermal cell tranverse to the cooling tubes
L_T	Length of thermal cell

<u>Symbols</u>	<u>Definition</u>
$\dot{M}$	Mass flow rate of coolant in single tube
N	Number of tubes per unit length
η_c	Efficiency of the PV cell at an assumed temperature
η_o	Optical efficiency
P_D	Power dissipation due to reverse bias
Pr	Prandtl Number
P_{ws}	Saturation vapor pressure of water vapor
q_{l-sky}	Radiant heat transfer from top surface to sky
Ra	Rayleigh Number
Re	Reynolds Number
ρ	Air density
σ	Stephan-Boltzman constant
T_a	Ambient air temperature
T_c	Temperature of coolant (coolant calculation)
T_g	Temperature of gasket
T_c	Temperature of cell
T_{cmax}	Maximum allowable cell temperature
T_i	Temperature of material layer (Node) i
T_s	Temperature of seal
τ_i	Thickness of layer (Node) i
T_r	Reference temperature of cell
T_n	Transmissivity of layer (Node) n
U_{ia}	Thermal conductance from node i to ambient
U_{ic}	Thermal conductance from node i to coolant
U_{ij}	Thermal conductance between nodes i and j based on the area of the thermal cell
V	Velocity (Coolant or air)
ν	Kinematic viscosity
W	Distance from center of thermal cell to the seal
W_T	Width of thermal cell

3.9 REFERENCES

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SECTION 4.0 STRUCTURAL ANALYSIS

4.1 INTRODUCTION

The purpose of performing a structural analysis of a PV module is to analytically predict the survivability of the module under extreme environmental conditions. The effect of external loads will be discussed in this section. These loads include uniform loads, twisting loads due to installation and handling misalignment, and hail impact loading.

An analysis of the total uniform load on a flat plate module would consist of the module deadweight, snow load, earthquake loads, and time varying wind loads (cyclic pressure loading). The JPL Block V standards indicate that a flat plate module must be able to withstand a mechanical cycling load of ± 50 pounds per square foot for 10,000 cycles as indicated in figure 4-1. This loading is intended to simulate a cyclic wind load. Thus, the structural analysis of a flat plate module will be based only on deadweight loading due to the weight of the module and the JPL Block V wind loading requirements. Earthquake and snow loads are site dependent and will not be considered here; however, if these loads are to be included in a structural analysis, the guidelines in ANSI A58.1 [1] should be used to determine the appropriate loads for the site being considered.

- CASES:** 1) SIMPLY SUPPORTED PLATES ON ALL EDGES
2) **STRUCTURE TYPES:** a) GLASS SUPERSTRATE
b) METAL SUBSTRATE

GUIDELINES: MECHANICAL CYCLIC LOADING — JPL SECTION V: ± 50 psf UNIFORM LOAD FOR 10,000 CYCLES

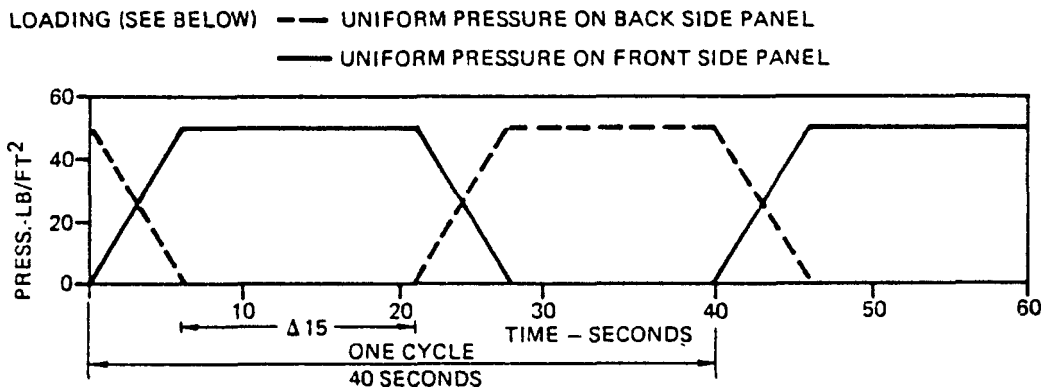


Figure 4-1. JPL Block V Wind Loading Specification

The flat plate analysis will assume simply supported plates. Analysis of receiver sections for concentrating collectors will assume the sections can be approximated by simply supported beams. In actual designs the receiver sections may be clamped at the ends or supported in the middle; however, the assumption of simple supports should give a conservative estimate of the stresses in the receiver section due to bending moments and shear. It will be assumed that the receiver section will see only the static load due to the weight of the receiver and cooling fluid.

A typical module construction might be as shown in figure 4-2. However, for a simplified structural analysis of a module the main load bearing members are assumed to bear all of the pressure loads. Thus, for a superstrate design all the pressure load is born by the glass, and for a substrate design all the pressure load is assumed to be born by the substrate. Other types of modules may be designed such as a laminated module in which part of the load is born by a glass superstrate and part by a substrate; however, the structural analysis of such a module would require a complex computer model, such as the finite element modeling in the NASTRAN computer program, and cannot be handled by the more simplified techniques used for this project.

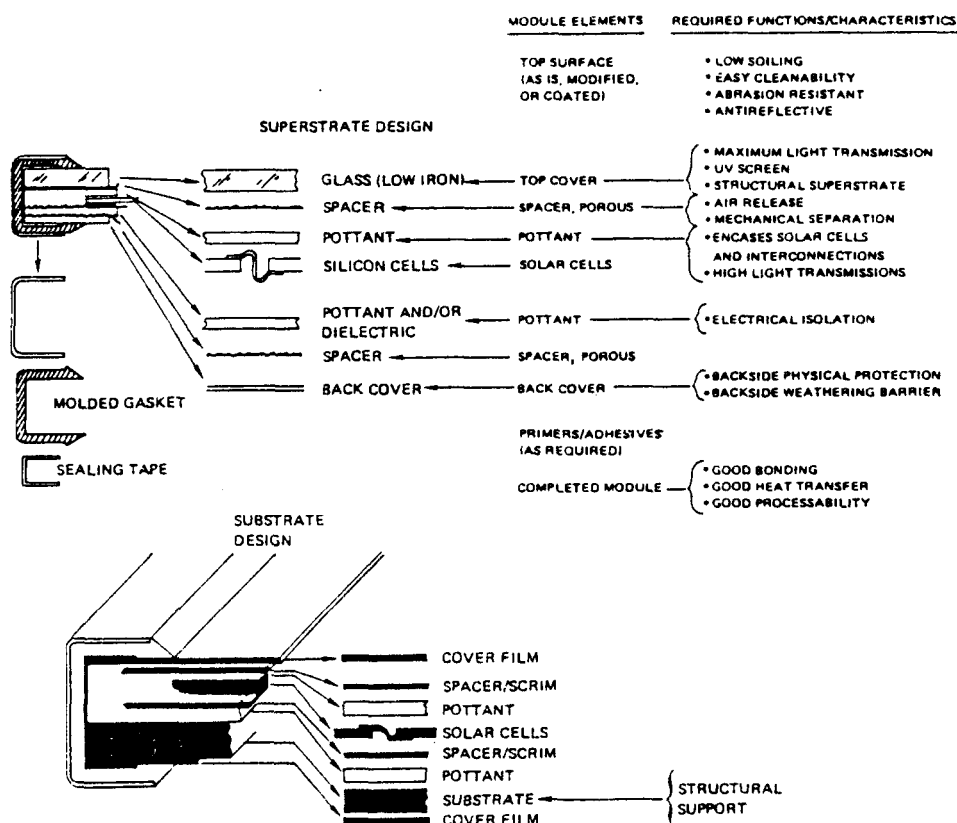


Figure 4-2. Superstrate Design

It is also assumed that the temperature of the load bearing member is uniform and the edges are unconstrained so that no thermal stresses are induced. A more complex analysis would be required to calculate thermal stresses due to localized hot spots produced by shading or a PV cell in reverse bias. Thermal cycling has not been addressed in this analysis.

4.2 FLAT PLATE ANALYSIS - UNIFORM LOADING

Mechanical loading such as wind and snow pressure, acceleration due to earthquakes, and imposed twist due to support settlement or misalignment, will generate stress in the module. As the module deflects under load, the resulting strain in the load bearing layers will transfer through the encapsulant to the solar cells.

In order to determine the sensitivity of solar cell stress to encapsulant modulus of elasticity and thickness, the analysis must account for the strain relief through the thickness of the module provided by the encapsulant layers. The modes of strain relief are transverse shear flexibility and thickness stretch. Classical lamination theory, which is based on simple bending theory, does not account for these modes of strain relief. A finite element analysis using the NASTRAN structural analysis computer program has been performed to determine the stresses transferred to the PV cell under uniform loading. The results of this analysis are reported in reference [2] and summarized here.

In figure 4-3 (from reference [2]) the solar cell stress is plotted as a function of encapsulant thickness and modulus for a 1/8 inch glass superstrate in which the maximum stress was 6000 psi which corresponds to a 50 psf wind load on a 48" x 48" module. The PV cell size was 4" x 4". The encapsulant thickness refers to the thickness between the solar cell and load bearing layer, and the analysis assumed an equal thickness above and below the cell. This analysis shows that for low values of encapsulant modulus, the cell stress decreases as the modulus decreases or as the module thickness increases. The encapsulant provides strain relief through the thickness of the module. For ethylene vinyl acetate (EVA) (E (Young's Modulus) = 1000 PSI), approximately 5 mils are required to maintain cell stress below the assumed 8000 psi allowable stress limit for a solar cell.

Further analysis is required for different configurations and different loading conditions to determine the amount of encapsulant required to decouple the PV cells from the load bearing members for various designs. However, some guidance can be obtained from figure 4-3 in that the designer should use at least 5 mils of encapsulant which has a low modulus of elasticity. Based on the analysis in reference [2] this encapsulant thickness will also prevent thermal stresses from being transferred to the PV cell.

Advanced module designs may use thin film technologies such as amorphous silicon sputtered onto a glass superstrate. In such cases it is the stresses in the superstrate which will cause failure. The thin Si film will not contribute to the strength of the superstrate. In subsequent analysis, it will

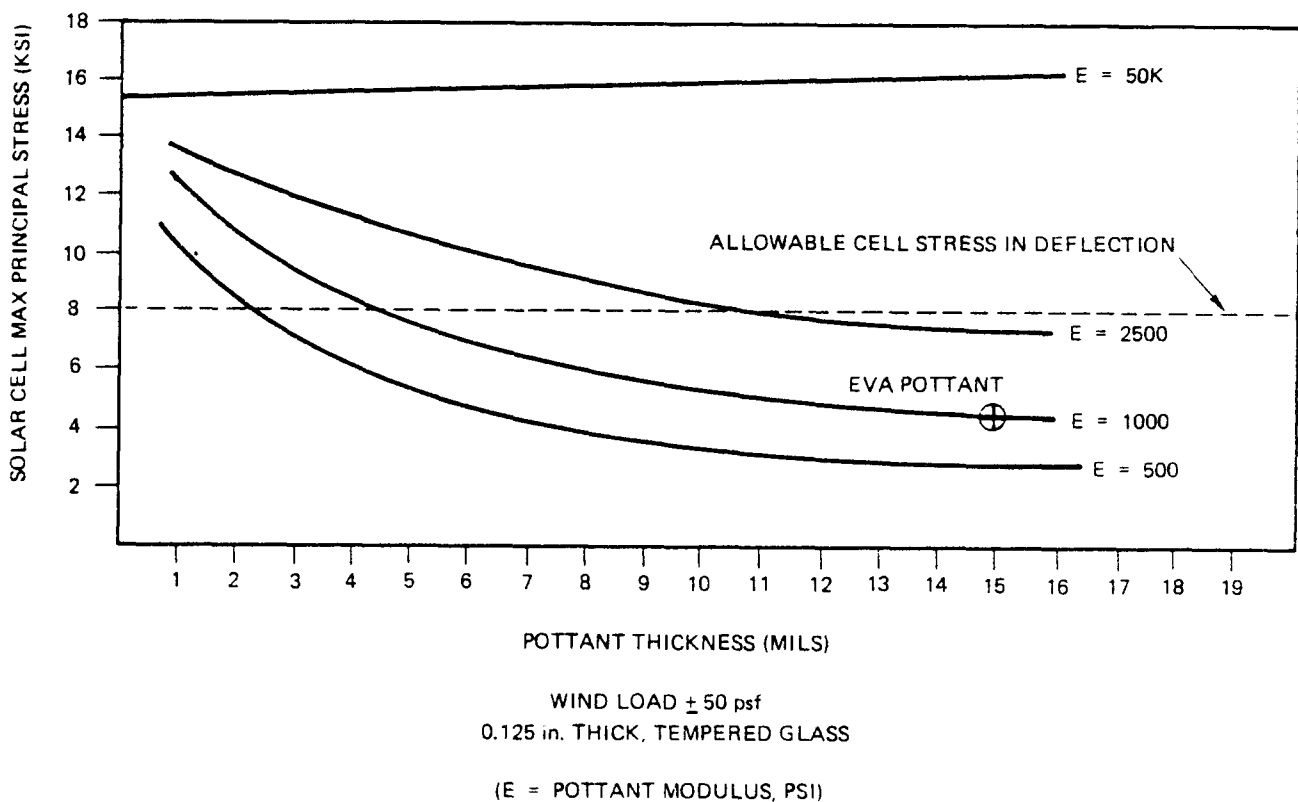


Figure 4-3. Deflection Analysis (Glass Superstrate Design)

be assumed that adequate encapsulation has been provided to decouple the PV cells from the substrate or superstrate. Failure of the substrate plate or superstrate plate implies failure of the module.

To determine whether or not failure will occur under a given load, the analytical prediction of the stress in a plate is compared to an allowable, or breaking, stress. The Jet Propulsion Laboratory has performed extensive analysis using the nonlinear finite element structural analysis program ARGUS to produce design curves for the structural analysis of simply supported rectangular plates [3]. These curves, shown in figures 4-4 through 4-7, provide the center deflection, center stress, and corner stress as a function of a dimensionless parameter describing the load intensity. Results are included for plates having an aspect ratio (length-to-width ratio) of 1, 1.5, 2, 3, and 4.

The dimensionless parameters describing the loading, deflection, and stress are defined as follows:

$$\text{Load intensity factor} = \text{LIF} = \frac{Pb^4}{Dt} \quad (4-1)$$

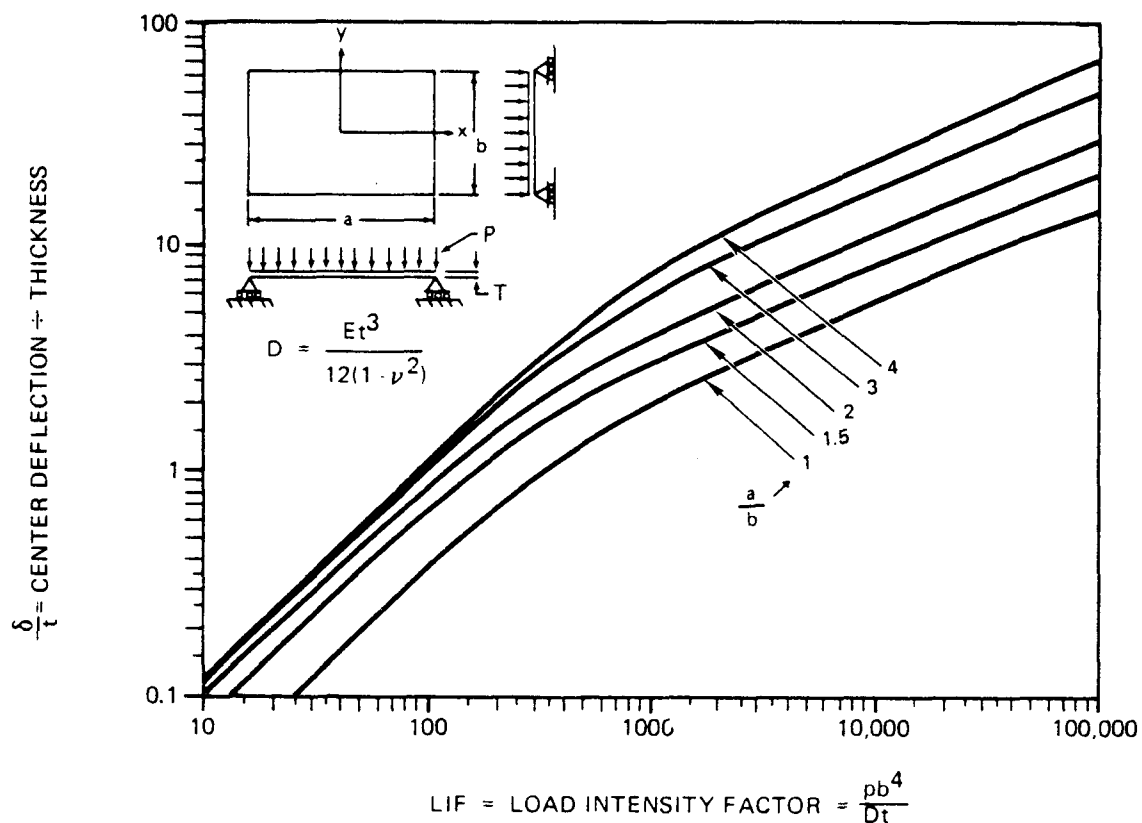


Figure 4-4. Center Deflection--Thickness Versus Load Intensity Factor for Uniformly Loaded, Simply Supported Rectangular Plates

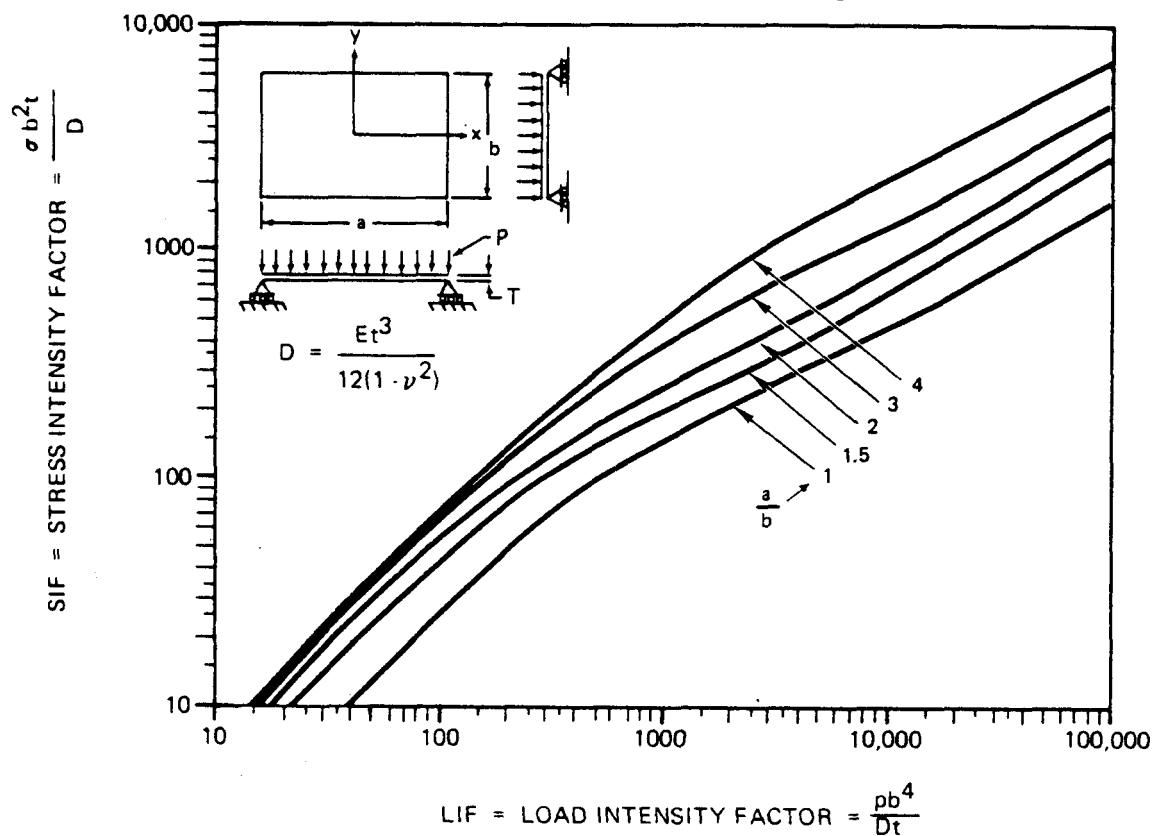


Figure 4-5. Stress Intensity Factor Versus Load Intensity Factor for Maximum Positive Principal Stress at the Bottom Center of the Plate

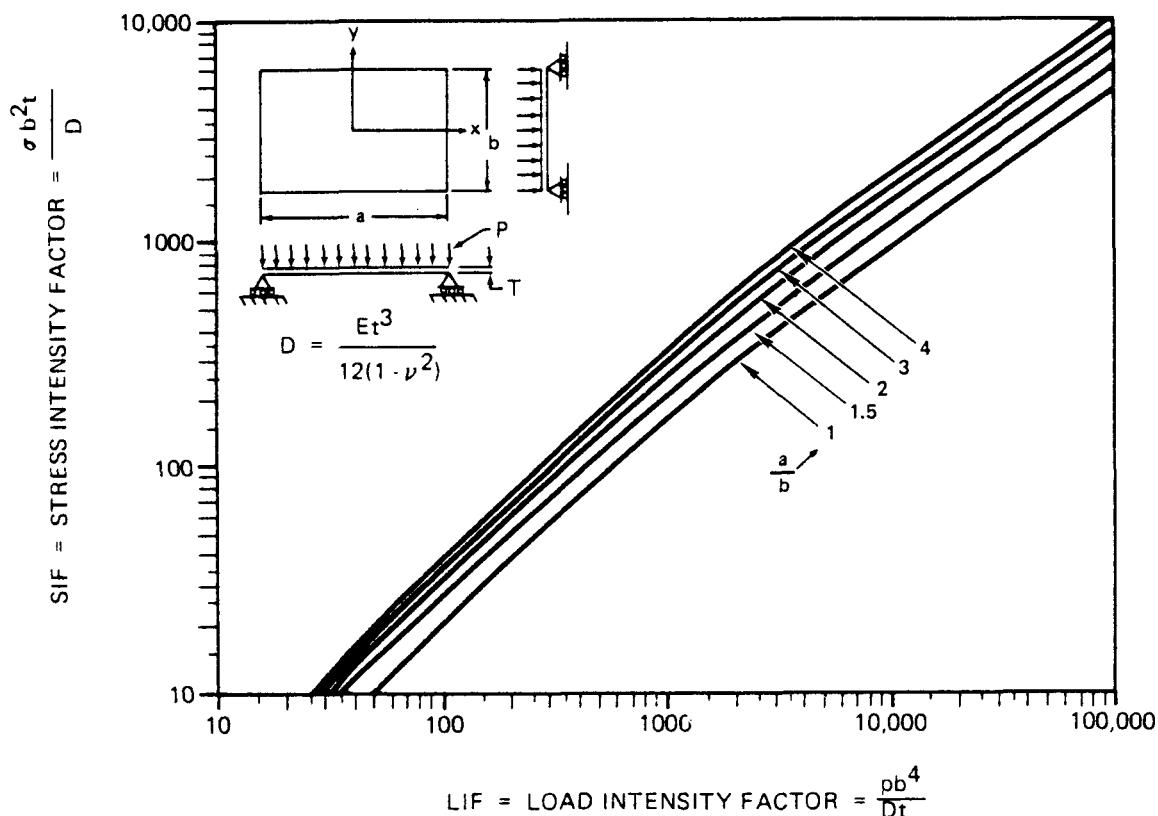


Figure 4-6. Stress Intensity Factor Versus Load Intensity Factor for Maximum Positive Principal Stress at the Top Surface of the Plate in the Proximity of the Corner

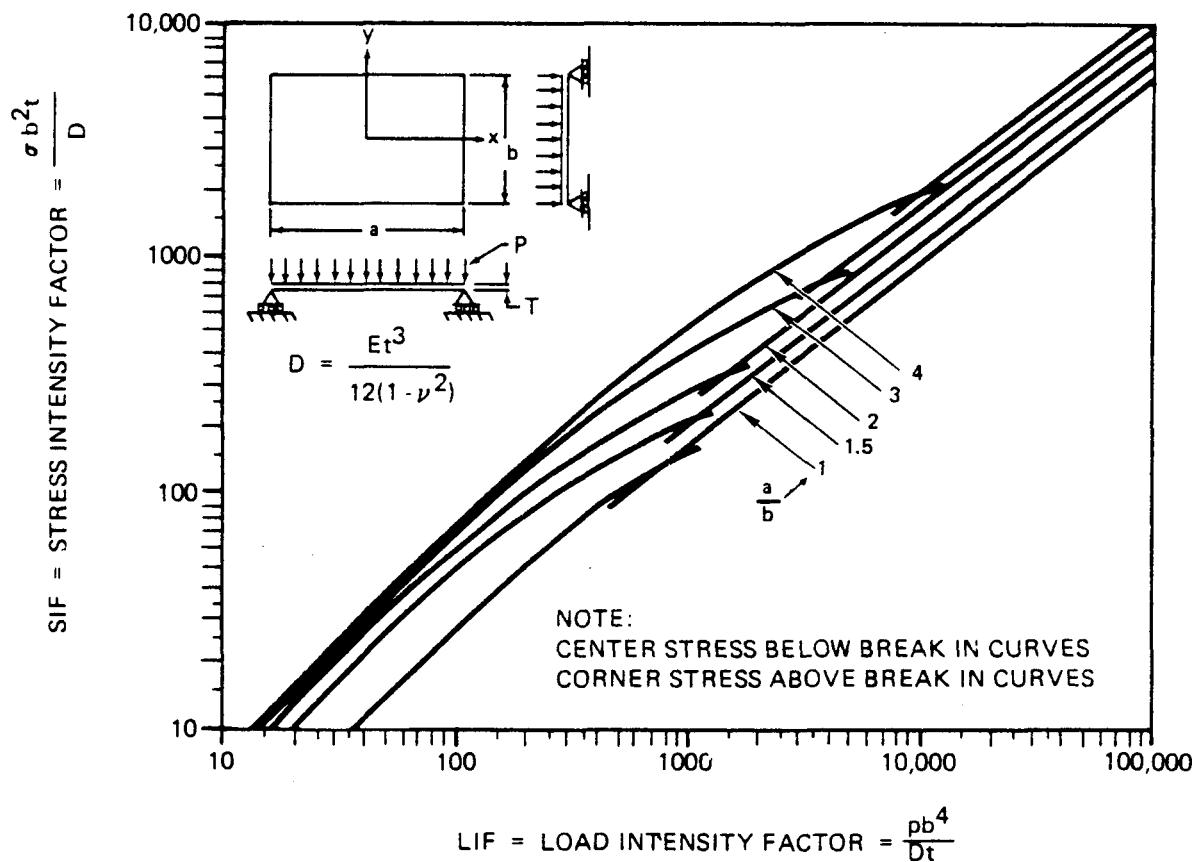


Figure 4-7. SIF Versus LIF Showing Composite Curves of the Larger of the Maximum Positive Principal Stresses on Plate (Center Bottom or Top Surface Near Corner)

where P = load in pounds per square inch

b = width of the plate in inches

t = thickness of the plate in inches

D = flexural rigidity of the plate in inch-pounds

$$D = \frac{E t^3}{12 (1-\nu^2)} \quad (4-2)$$

and E = Young's modulus of elasticity

ν = Poisson's ratio.

$$\text{Stress intensity factor} = \text{SIF} = \frac{\sigma b^2 t}{D}, \quad (4-3)$$

where σ = maximum positive principal stress in the plate in pounds per square inch.

$$\text{Dimensionless center deflection} = \frac{\delta}{t} \quad (4-4)$$

where δ = deflection of the center of the plate.

The load is a combination of deadweight load and wind loading. The deadweight load is obtained from equation 4-5.

$$W = \sum_{i=1}^N t_i \rho_i \quad (4-5)$$

where t_i = thickness of the i th layer

ρ_i = density of the i th layer

Since the module is to be designed for a wind loading of 50 psf, the uniform wind loading is (in psi)

$$P_W = 0.347 \text{ psi} \quad (4-6a)$$

and the deadweight loading for a module tilted at an angle β from the horizontal is

$$P_D = W \cos \beta. \quad (4-6b)$$

It can be seen (figures 4-5 and 4-6), that stress at the center of the plate is higher than at the corners of the plate for low to moderate loading. At higher loads, however, the stress at the corners of the plate is higher. Figure 4-7 is constructed by superimposing figure 4-5 on figure 4-6, but showing only the higher of the center or corner stresses at any given load intensity. Figure 4-7 gives the maximum positive principal stress, σ , versus load intensity factor for aspect ratios of 1, 1.5, 2, 3, and 4. The maximum positive principal stress occurs on the bottom surface of the plate at the center and on the top surface of the plate at the corners. At the center it is predominantly membrane tension stress plus bending stress. At the corners it is largely shear stress.

To obtain the stress in a plate the LIF is calculated using equation 4-1. The SIF is obtained from figure 4-7 and the maximum stress is calculated. This stress is then compared to the allowable stress to be determined as shown in the following section. If the calculated stress is greater than the allowable stress the designer has several options: (1) use a stronger material with a larger modulus or greater allowable stress, (2) increase the thickness of the plate, (3) decrease the size of the module (i.e., decrease the aspect ratio), or (4) add stiffness or beams across the back of the module.

4.3 ALLOWABLE STRESS

The allowable stress for a flat plate module depends on the material of the main load bearing member. In addition, the allowable stress will depend on whether the load is static (the deadweight of the module), or dynamic, such as the wind loading. In the following sections the method for obtaining the allowable stresses for metal and glass plates will be described. There are two allowable stresses to be determined for each material; the allowable stress for static loads and the fatigue limit for cyclic loads.

4.3.1 Metal Substrates

For metal plates subjected to a static deadweight load, the maximum allowable stress is the yield strength of the material. Since there are so many steel and aluminum alloys, the yield strength of the various metals will not be provided here. Rather, the designer is referred to one of the many handbooks available (i.e., reference [4]).

For cyclic loading, as in the JPL Block V standard shown in figure 4-1, the allowable stress depends on the number of loading cycles. As the number of cycles increases the maximum allowable stress decreases as shown in figure 4-8 (from reference [5]). In the case of ferrous metals and alloys, the curve becomes horizontal after the material has been stressed for a certain number of cycles; failure will not occur if the stress is below this value, no matter how many stress cycles are applied. When this is the case, the stress intensity represented by the horizontal line is called the endurance limit. In the case of nonferrous metals and alloys, the line never becomes horizontal so that these metals do not have an endurance limit.

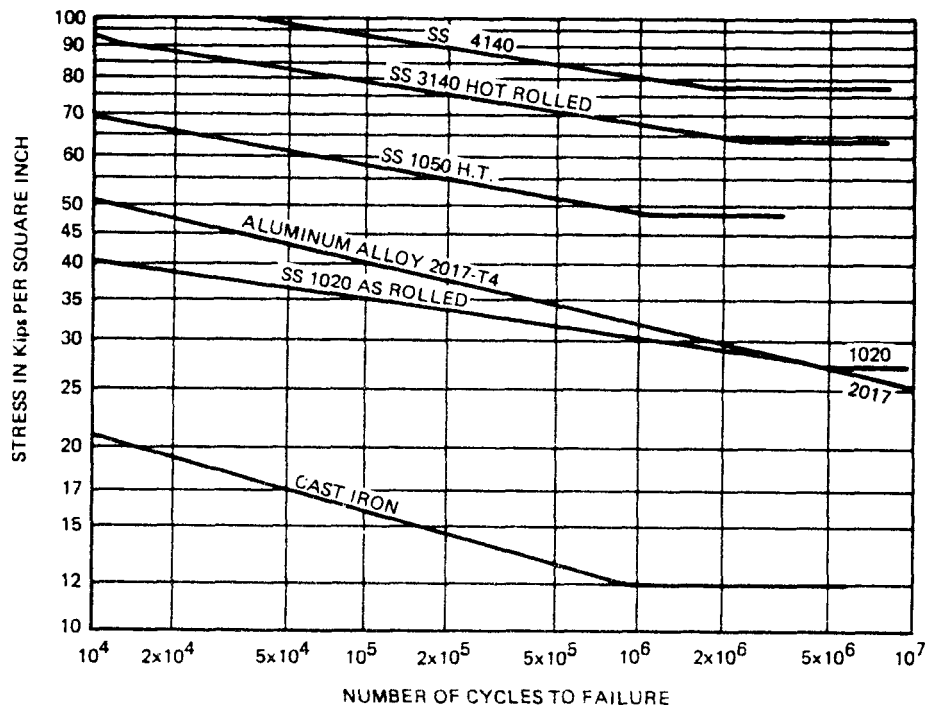


Figure 4-8. Typical Stress-Cycle Curves for Stainless Steels, Cast Iron, and Aluminum (Reference 5)

These stress-cycle curves can be extended to lower cycles using the following procedure. If the allowable stress at M cycles is known, and the allowable stress at N cycles is desired, then one can use the following relation

$$\sigma_{ALL} = \sigma_M \left(\frac{M}{N} \right)^{\alpha} \quad (4-7)$$

where α is an empirically obtained constant defined as

$\alpha = 0.09$ for stainless steel

$= 0.10$ for aluminum

$= 0.116$ for cast iron

and σ_M = known allowable stress for M cycles

σ_{ALL} = desired allowable stress at N cycles

For example, for heat treated 1050 stainless steel, $\sigma_M = 61,000$ psi at 5×10^4 cycles. Using equation 4-7 to find the allowable stress at 10,000 cycles as required by the JPL Block V standards

$$\sigma_{ALL} = (61,000) \left(\frac{5 \times 10^4}{10^4} \right)^{0.09} = 70,000 \text{ psi}$$

If a stress cycle curve is not available for a particular ferrous material, the endurance limit can be obtained from equation 4-8 where the knee is assumed to occur at 10^6 cycles [5]

$$\sigma_M = \text{endurance limit} = 1/2 (\text{ultimate strength}) \quad (4-8)$$

The allowable stress for a lesser number of cycles can then be found from equation 4-7.

4.3.2 Glass Superstrate

The failure characteristics of glass are quite different from those of metals due to the brittle nature of glass. Failure occurs when stress concentrations at the tips of existing flaws, especially surface flaws, are not relieved by plastic yielding of the material. For this reason glass always fails in tension when these flaws grow, under sustained loading, to some critical size. Thus, the surface condition of the glass is the most important single factor influencing the breakage strength of a glass plate.

The allowable stress in a glass plate will be a function of the following factors:

- Area. Large area plates have more and larger surface flaws increasing the probability that a severe flaw will coincide with a region of high tensile stress. This phenomenon leads to a lower breakage stress for larger glass parts.
- Degree of temper. Glass taken through different processes may be inherently stronger or may have had surface flaws and stress concentrations decreased by annealing or tempering.
- Load duration. Glass parts will sustain loads for short periods of time; however, the same loads applied for longer durations will eventually result in failure. The existing flaws in the glass grow under the influence of sustained loads. When these cracks reach some critical size, failure occurs.
- Probability of failure. For a given size glass plate, a given load duration, and degree of temper, glass has a Weibull distribution of failure probability vs. breakage strength [3]. This is due to the probability of a flaw existing in the plate which will grow to a critical size during the period of load application.

The fatigue characteristics exhibited by glass under static loads are somewhat similar to those of metals under conditions of cyclic loading. In both cases, delayed failure results from the slow progress of flaws. There is little difference in the stress-time curves of glass under static loading and cyclic loading with complete stress reversal if the maximum stress and time duration are the same. This is indicated in figure 4-9 (reference [6]).

Thus, the cyclic wind loading specifications indicated in figure 4-1 can be assumed to be a static load of 50 psf. The time duration of this load is

determined by the number of cycles (10,000) and the time duration of each cycle (40 seconds). Thus, an equivalent static load would be 50 psf for 4.6 days.

To obtain the allowable stress in glass, the designer must specify an acceptable failure rate. This should be based on economic considerations; that is, the failure rate which produces the minimum life-cycle cost for a given application should be used. From figure 4-10 the breakage strength for the specified glass type is obtained for a 1-square meter sample subjected to a load of 1-minute total duration corresponding to the chosen failure rate. This breakage stress is denoted by σ_{11} .

The fraction of σ_{11} for a plate area other than 1-square meter is then obtained from figure 4-11 or equation 4-9.

$$f_A = \left(\frac{1}{A} \right)^{1/6} \quad (4-9)$$

where A = plate area in square meters.

Next, the designer must determine the total duration of the loading conditions of wind and deadweight. As indicated previously, the JPL Block V standards indicate a design wind load duration of 4.6 days. For a typical design life the deadweight loading will be 20 years. Using figure 4-12 and these load durations, the fraction of σ_{11} for total load durations other than 1-minute are obtained for the type of glass being considered and for each load.

The breaking stress, or allowable stress, is then obtained from equation 4-10

$$\sigma_B = \sigma_{11} f_A f_T \quad (4-10a)$$

Thus, the breaking stress for the wind load is

$$\sigma_{BW} = \sigma_{11} f_A f_{T_W} \quad (4-10b)$$

and for the deadweight load

$$\sigma_{BD} = \sigma_{11} f_A f_{T_D} \quad (4-10c)$$

These allowable stresses are then compared to the actual stresses obtained in section 3-2. The glass thickness is considered adequate if the following combined loading criteria are satisfied:

$$\frac{\sigma_D}{\sigma_{BD}} < 1 \quad (4-11)$$

$$\frac{\sigma_D + \sigma_W}{\sigma_{BW}} < 1$$

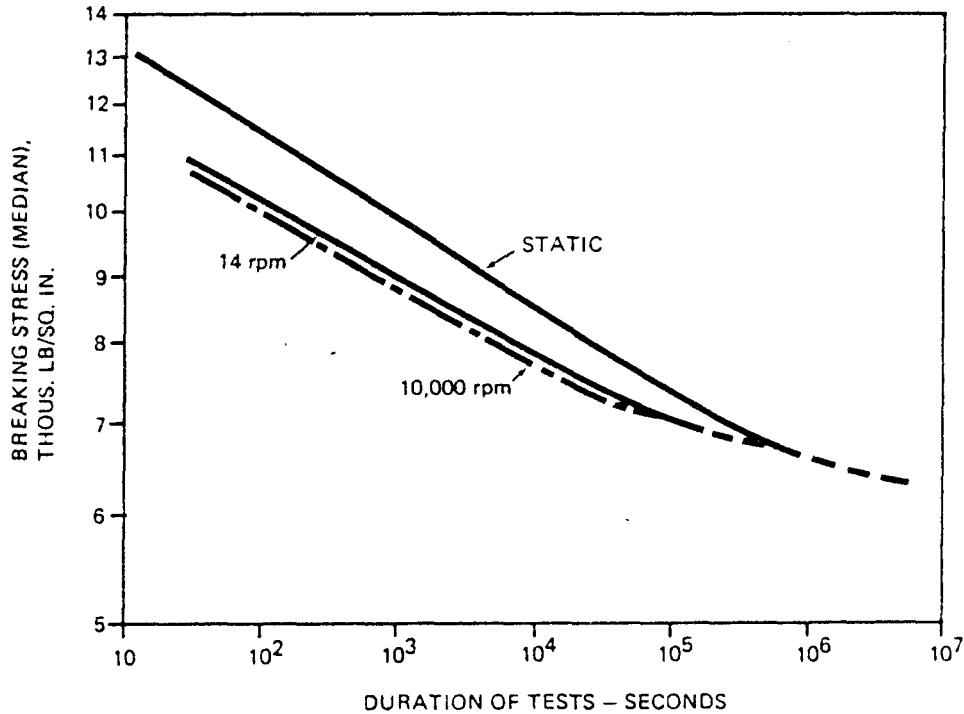


Figure 4-9. Comparison of Static and Dynamic Fatigue Tests in Bending on Annealed Glass Rods, $\frac{1}{4}$ -Inch Diameter (Reference 6)

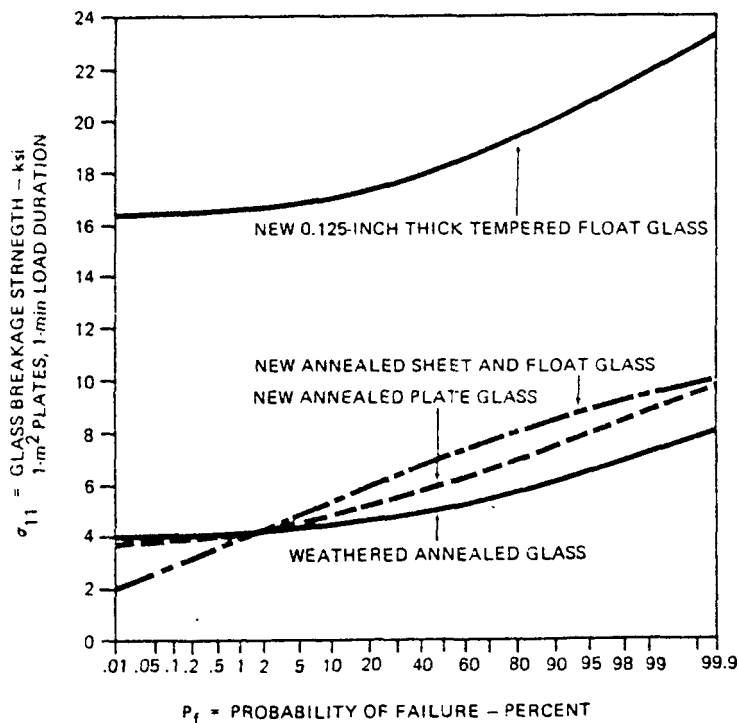


Figure 4-10. Recommended Design Values for Breakage Strength Versus Probability of Failure for $1m^2$, Simply Supported Glass Plates Subjected to a Uniform Normal Pressure Load of 1-Minute Duration [3]

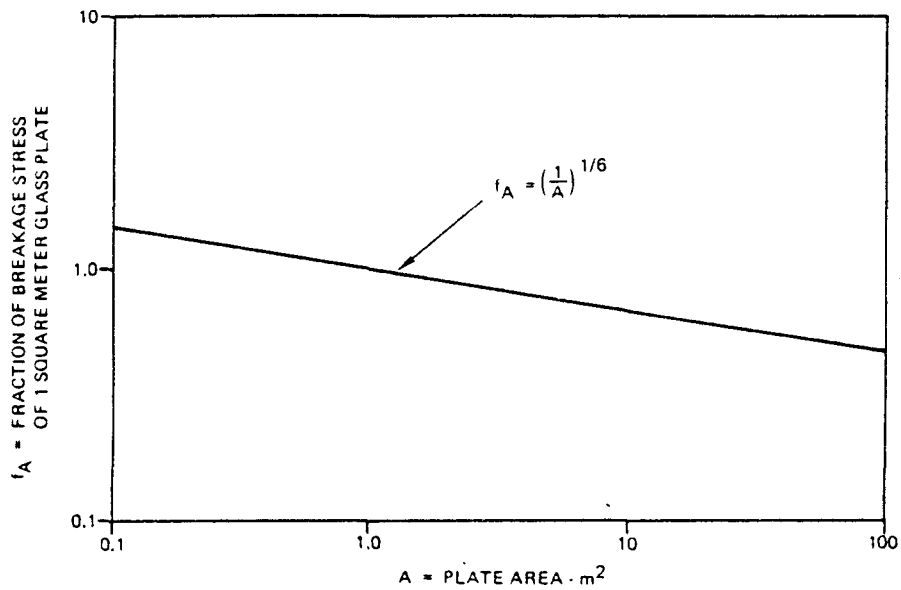


Figure 4-11. Fraction of Breakage Strength of 1-Square-Meter Glass Plates Versus Plate Area [3]

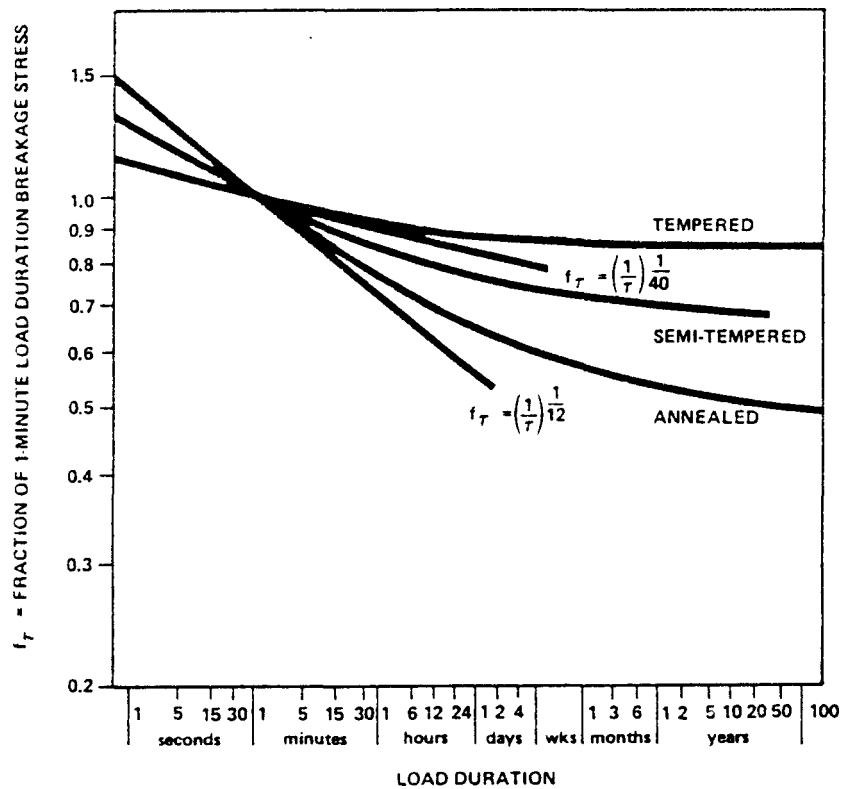


Figure 4-12. Fraction of 1-Minute Load Duration Glass Breakage Stress Versus Load Duration [3]

where σ_D = stress in the plate due to the deadweight load alone.
 σ_W = stress in the plate due to the wind load of 0.347 psi.

4.3.3 Example

As an example of an application of the analysis presented in the previous sections, consider a glass superstrate design using a 4 ft x 4 ft panel of 1/8 inch tempered glass. The glass has the following properties:

Young's Modulus of Elasticity: $E = 10 \times 10^6$ psi

Poisson's ratio: $\nu = 0.22$

Density: $\rho = 0.1 \text{ lb/in}^3$

Neglecting the weight of encapsulant and metal foil substrate, and assuming a tilt angle of 35° , the deadweight load is obtained from equations 4-5 and 4-6b:

$$P_D = (0.125 \text{ inches})(0.1 \text{ lb/in}^3) \cos 35^\circ$$

$$P_D = 0.01 \text{ lb/in}^2$$

The wind loading is obtained from equation 4-6a as

$$P_W = 0.347 \text{ psi}$$

From equation 4-2, the flexural rigidity is

$$D = \frac{(10 \times 10^6)(0.125)^3}{12(1 - 0.22^2)} = 1.71 \times 10^3$$

From equation 4-1 the load intensity factor for deadweight loading is

$$LIF_D = \frac{(0.01)(48)^4}{(1.71 \times 10^3)(0.125)} = 248 \text{ psi}$$

and for wind loading

$$LIF_W = \frac{(0.347)(48)^4}{(1.71 \times 10^3)(0.125)} = 8.62 \times 10^3$$

The stress intensity factor for each load is found from figure 4-7 for $a/b = 1$ as:

$$SIF_D = 60$$

$$SIF_W = 800$$

The stress in the panel for each load can be obtained from equation 4-3:

$$\sigma_D = \frac{(60)(1.71 \times 10^3)}{(48)^2(0.125)} = 356 \text{ psi}$$

$$\sigma_W = \frac{(800)(1.71 \times 10^3)}{(48)^2(0.125)} = 4750 \text{ psi}$$

From figure 4-7, the maximum deadweight stress occurs at the center of the plate and the maximum stress due to wind loading occurs near the corner. The total deflection can be found from figure 4-4 for a combined LIF of 8870 as

$$\delta/t = 5$$

so that $\delta = (0.125)(5) = 0.625$ inches.

Assuming an economic failure rate of 2 percent, then for $P_f = 0.02$ the breaking stress for a 1 m^2 plate with a 1-minute load duration is found from figure 4-10 for tempered float glass as

$$\sigma_{11} = 16,400 \text{ psi}$$

The area and load duration correction factors are found from equation 4-9 and figure 4-12, respectively, as

$$f_A = 0.936 \quad \text{for} \quad A = 1.49 \text{ m}^2$$

$$f_\tau = 0.87 \quad \text{for} \quad \tau = 4.6 \text{ days}$$

$$f_\tau = 0.85 \quad \text{for} \quad \tau = 20 \text{ years}$$

Thus, the breaking stress for the wind load is, from equation 4-10b

$$\sigma_{BW} = (16,400)(0.936)(0.87) = 13355 \text{ psi}$$

and the breaking stress for the deadweight load is

$$\sigma_{BD} = (16,400)(0.936)(0.85) = 13048 \text{ psi}$$

Comparing these allowable stresses to the actual stresses in the plate, as indicated in equations 4-11:

$$\frac{\sigma_D}{\sigma_{BD}} = \frac{356}{13048} = 0.03 < 1$$

$$\frac{\sigma_D + \sigma_W}{\sigma_{BW}} = \frac{356 + 4750}{13355} = 0.4 < 1$$

Therefore, the glass thickness is adequate and the plate would withstand the deadweight and wind loading.

4.4 CONCENTRATOR RECEIVER TUBE ANALYSIS

A linear receiver section for either linear concentrating or point focus collectors may be approximated by a simply supported beam. The load on the beam is uniform and due simply to the weight of the beam. Simple beam theory can be used to obtain the bending moments, shear forces, and deflection of a simply supported beam with a uniform load as shown in figure 4-13 (from reference [7]).

Typical cross-sections for actively and passively cooled receiver sections are shown in figure 4-14. The loading on a linear receiver section is due to the weight of the material and the weight of cooling fluid when applicable and is given by equation 4-12

$$w = A_m P_m + A_c P_c + A_f P_f \quad (4-12)$$

where A_m = area of the metal heat sink
 A_c = area of the PV cell assembly
 A_f = area of the cooling channel
 P_m = density of the metal
 P_c = density of the PV cell assembly
 P_f = density of the fluid.

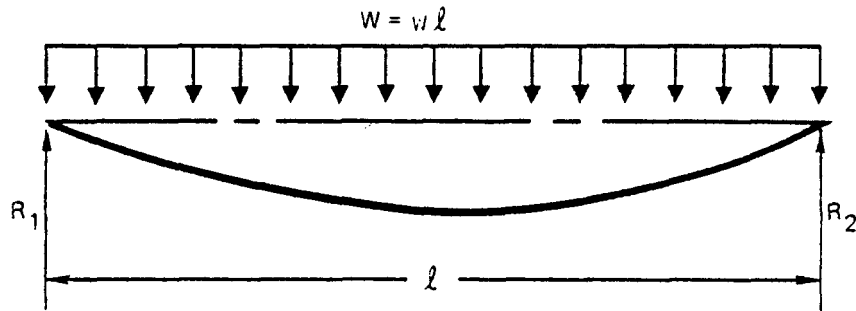


Figure 4-13. Forces, Moments and Deflection for a Beam Under Uniform Loading with Simple End Supports

Uniform load: w lbs/ft

Reaction forces: $R_1 = R_2 = \frac{1}{2} W$

Shear forces: $V = \frac{1}{2} W \left(1 - \frac{2x}{l} \right)$

Bending moments: $M = \frac{1}{2} W \left(x - \frac{x^2}{l} \right)$

$$M_{\max} = \frac{1}{8} W l \text{ at } x = \frac{1}{2} l$$

Deflection: $y = \frac{1}{24} \frac{W x}{E I l} \left(l^3 - 2 l x^2 + x^3 \right)$

$$y_{\max} = - \frac{5}{384} \frac{W l^3}{E I} \text{ at } x = \frac{1}{2} l$$

where I is the moment of inertia of the cross-section.

For the sections shown in figure 4-14, the areas are:

1. Passively cooled finned heat sink

$$\begin{aligned} A_m &= W t_m + N W_f h \\ N &= \text{number of fins} \\ A_c &= W_g t_g \end{aligned}$$

2. Actively cooled heat sink

$$\begin{aligned} A_m &= (W_o - W_i) (h_o - h_i) \\ A_c &= W_g t_g \\ A_f &= W_i h_i \end{aligned}$$

3. Actively cooled LPT receiver

$$A_m = \frac{1}{2}(b_o h_o - b_i h_i)$$

$$A_c = W_g t_g$$

$$W_g \approx \frac{b_o}{2 \sin \theta}$$

$$\theta = \arctan \frac{b_o}{2h_o}$$

$$A_f = \frac{1}{2} b_i h_i$$

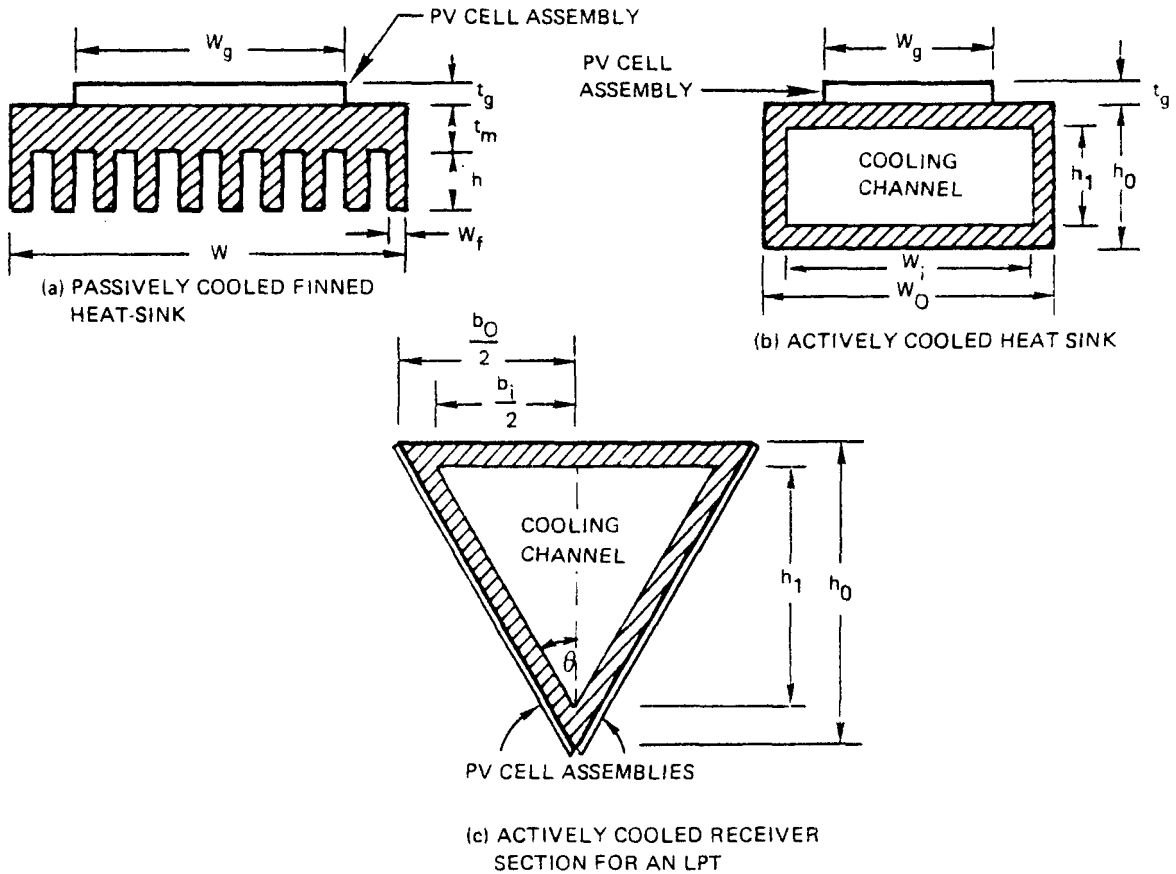


Figure 4-14. Typical Concentrating Receiver Cross-Sections

To determine the stresses in the PV cell and metal layers, beam theory gives the following relations:

$$\sigma = \frac{MC}{I} \quad (4-13)$$

$$T = \frac{VA\bar{y}}{It} \quad (4-14)$$

where:

σ = bending stress in the beam due to the bending moment M at a distance C from the neutral axis

C = distance from the neutral axis

I = moment of inertia of the cross-section

T = shear stress in the beam on a given horizontal section cut through the cross-section

A = partial area of the beam above the cut through the cross-section

$\bar{y}$ = distance between the neutral axis and the centroid of area A

t = thickness of the beam section over which the shear stress is to be found

The bending and shear stresses in beams having cross-sections shown in figure 4-14 will now be derived.

To obtain the stresses in the passively cooled finned receiver section shown in figure 4-14a, one must first find the moment of inertia of the heat sink. This is done as follows:

$$y_s = \frac{A_f y_f + A_b y_b}{A_f + A_b} \quad (4-15)$$

where:

y_s = centroid of the heat sink measured from the bottom

A_t = area of the fins = $w_f h N$

y_t = distance from the bottom to the centroid of the fins
= $h/2$

A_b = area of the base = Wt_m

y_b = $h + t_m/2$

For the fin area,
$$I_f = \frac{W_f N h^3}{12} \quad (4-16)$$

$$A_f d_f^2 = W_f h N \left(y_s - \frac{h}{2} \right)^2 \quad (4-17)$$

where d_f is the distance between the centroid of the heat sink and the centroid of the fins.

For the base area,
$$I_b = \frac{W t_m^3}{12} \quad (4-18)$$

$$A_b d_b^2 = W t_m \left(h + \frac{t_m}{2} - y_s \right)^2 \quad (4-19)$$

where d_b is the distance between the centroid of the heat sink and the centroid of the base area alone. Then, the moment of inertia of the heat sink is

$$I_s = I_f + A_f d_f^2 + I_b + A_b d_b^2 \quad (4-20)$$

$$I_s = \frac{W_f N h^3}{12} + W_f h N \left(y_s - \frac{h}{2} \right)^2 + \frac{W t_m^3}{12} + W t_m \left(h + \frac{t_m}{2} - y_s \right)^2$$

Now, since the beam is a composite consisting of the heat sink and a PV cell assembly, an equivalent beam section must be obtained and a new moment of inertia derived. The equivalent section will be obtained by transforming the width of the PV assembly by the ratio E_c/E_m where E_m is Young's modulus of the metal heat sink and E_c is Young's modulus of the PV cell assembly. If the cell assembly consists of the encapsulated PV cell with a soft cover material, E_c should be 15.5×10^6 psi for the silicon cell. If the PV cell is covered with glass, E_c should be that of glass (10×10^6 psi is an average value) since higher stresses will occur in the outer material.

The equivalent width of the PV cell assembly is

$$W_e = \frac{E_c}{E_m} W_g \quad (4-22)$$

and the centroid (or neutral axis) measured from the bottom is located at

$$y = \frac{A_s y_s + A_e (t_m + h + \frac{t_g}{2})}{A_s + A_e} \quad (4-23)$$

where

$$A_s = A_b + A_f$$

$$A_e = W_e t_g \quad (4-24)$$

The moment of inertia is

$$I = I_s + A_s (y - y_s)^2 + \frac{1}{12} W_e t_g^3 + A_e (t_m + h + \frac{t_g}{2} - y)^2 \quad (4-25)$$

The maximum bending stress in the heat sink is given by equation 4-26, where the stress is in tension.

$$(\sigma_s)_{\max} = \frac{M y}{I} \quad (4-26)$$

The maximum stress in the PV cell assembly is a compressive stress given by 4-27

$$(\sigma_c)_{\max} = \frac{E_c M}{E_m I} (t_m + h + t_g - y) \quad (4-27)$$

where M is the maximum bending moment obtained from figure 4-13. The shear stress at the PV cell/heat sink interface is obtained from equation 4-28.

$$\tau = \frac{V t_g}{I} (t_m + h + t_g/2 - y) \quad (4-28)$$

The tensile stress in the heat sink (σ_s) should be compared to the yield stress of the heat sink material to determine whether failure will occur. Also, the compressive stress in the PV cell assembly (either the PV cell or glass cover) should be compared to the compressive strength of the material, and the shear stress at the interface compared to the bonding strength of the adhesive. If the stresses due to the load are greater than strengths of the material or bond, then failure will occur. If this is the case, a support may be placed in the center of the receiver section and another analysis performed for one-half the original beam length.

Even if failure did not occur, excess deflection may occur thereby preventing full concentration at the center of the receiver tube. If this is to be a consideration in the design, the user must indicate the maximum amount of deflection acceptable and compare that with the deflection due to the load obtained from figure 4-13.

The stresses in the actively cooled system are obtained in essentially the same manner. The centroid, or neutral axis is located at

$$y = \frac{A_s y_s + A_e (t_m + \frac{t_g}{2})}{A_s + A_e} \quad (4-29)$$

where

$$A_s = (W_o - W_i)(h_o - h_i)$$

$$y_s = 1/2 h_o$$

$$A_e = W_e t_g \quad (4-30)$$

$$W_e = \frac{E_c}{E_m} W_g$$

and the moment of Inertia is

$$I = I_s + A_s (y - y_s)^2 + \frac{1}{12} W_e t_g^3 + A_e (h_o + \frac{t_g}{2} - y)^2 \quad (4-31)$$

where

$$I_s = \frac{1}{12} (W_o h_o^3 - W_i h_i^3) \quad (4-31)$$

The maximum bending stresses are

$$(\sigma_s)_{\max} = \frac{My}{I} \quad (4-32)$$

$$(\sigma_c)_{\max} = \frac{E_c M}{E_m I} (t_m + t_g - y) \quad (4-33)$$

and the maximum shear stress in the bond line is given by

$$\tau = \frac{V t_g}{I} (h_o + t_g - y) \quad (4-34)$$

Due to the geometry of the cross-section, the moment of inertia and stresses in the PV assembly of the triangular section are more difficult to calculate. In sections of this type the PV cell is usually covered by glass which, on the average, has a modulus very close to that of aluminum. Therefore, it will be assumed that the section is made of one material and the tensile stresses at the bottom are the same in the glass cover as in the aluminum heat sink. The moment of inertia, bending stresses and shear stress will be derived in the following sections.

The centroid of the total triangular area is located at a distance measured from the bottom (or apex) given by

$$y_o = \frac{2}{3} h_o, \quad (4-35)$$

and the moment of inertia is

$$I_o = \frac{b_o h_o^3}{36} \quad (4-36)$$

The centroid of the hollow triangular area is at the same location with a moment of inertia given by

$$I_i = \frac{b_i h_i^3}{36} \quad (4-37)$$

Thus, the moment of inertia of the hollow triangular beam is

$$I = I_o - I_i \quad (4-38)$$

The maximum compressive stress occurs at the top of the beam in the aluminum and is given by

$$(\sigma_c)_{\max} = \frac{M}{I} \left(\frac{1}{3} h_o \right) \quad (4-39)$$

and the maximum tensile stress occurs at the apex and is given by

$$(\sigma_s)_{\max} = \frac{M}{I} \left(\frac{2}{3} h_o \right) \quad (4-40)$$

Since glass is the weakest member in tension, this stress due to the load should be compared to the allowable stress in glass defined in the previous section. If the allowable stress is less than the stress calculated with equation 4-40, the glass cover will fail.

The maximum shear stresses occur on a plane through the neutral axis. The area above the neutral axis is trapezoidal in shape with the total area given by

$$A_T = \frac{1}{2} b_o h_o - \frac{4}{9} h_o^2 \tan \theta \quad (4-41)$$

and the area of the hollow portion given by

$$A_i = \frac{1}{2} b_i h_i - \frac{4}{9} h_i^2 \tan \theta \quad (4-42)$$

The area of the beam above the neutral axis is then

$$A = A_T - A_i \quad (4-43)$$

The centroid of a trapezoidal area is given in Reference 4. For the total area the centroid is at a distance above the apex given by

$$C_T = \frac{1}{3} \frac{3b_1 + 2b_2}{2b_1 + b_2} \frac{h_o}{3} + \frac{2}{3} h_o \quad (4-44)$$

and the centroid of the hollow area is at a distance above the apex given by

$$C_i = \frac{1}{3} \frac{3b_3 + 2b_4}{2b_3 + b_4} \frac{h_i}{3} + \frac{2}{3} h_o \quad (4-45)$$

where

$$\begin{aligned} b_1 &= \frac{4}{3} h_o \tan \theta \\ b_2 &= b_o - b_1 \\ b_3 &= \frac{4}{3} h_i \tan \theta \\ b_4 &= b_i - b_3 \end{aligned} \quad (4-46)$$

The centroid of the trapezoidal area above the neutral axis is then at a position above the apex given by

$$y = \frac{A_T C_T - A_i C_i}{A_T - A_i} \quad (4-47)$$

and the distance between the neutral axis and the centroid is

$$\bar{y} = y - \frac{2}{3} h_o \quad (4-48)$$

The shear stress at the PV cell assembly/metal interface is then obtained from

$$\tau = \frac{VA}{It} \bar{y} \quad (4-49)$$

where

$$t \approx b_o - b_i \quad (4-50)$$

4.5 TWISTING LOAD

Twisting loads occur when a plate is misaligned during installation. Such loads produce almost pure shear stresses which can be calculated from equation 4-51.

$$T = \frac{\phi \tau G}{a} \quad (4-51)$$

where:

T = shear stress (psi)
 ϕ = angle of twist (radians)
 τ = thickness of the structural member
 a = length of the plate
 G = shear modulus (psi)

$$G = \frac{E}{2(1+\nu)} \quad (4-52)$$

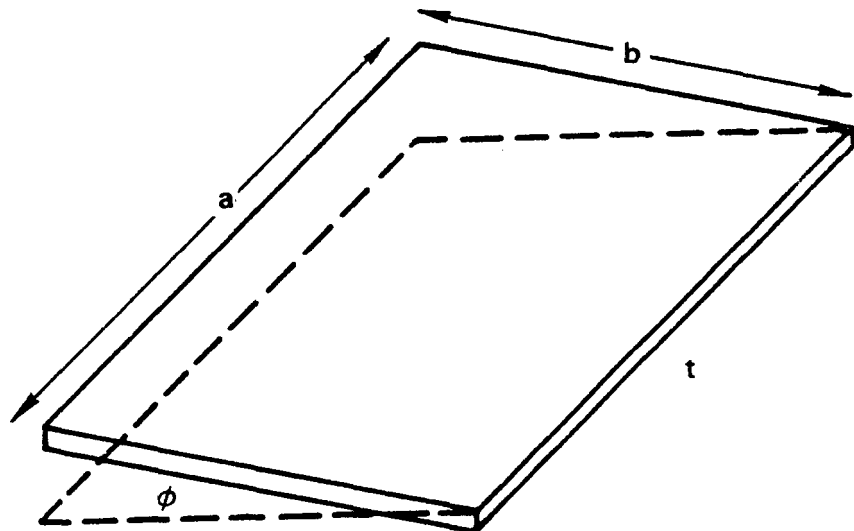
This relation for shear stress is valid for $b/\tau > 6$, where b is the width of the plate (see figure 4-15).

The allowable shear stress is found from equation 4-53.

$$T_{ALL} = \frac{1}{2} \sigma_{ALL} \quad (4-53)$$

where σ_{ALL} is obtained using the procedures of sections 4.3.1 and 4.3.2.

GUIDELINE: JPL SECTION V: 1/2" PER FT. TWIST



1/2" PER FT.

SHEAR STRESS FOR $a/t > 6.00$

$$\tau = \frac{\phi t G}{b}$$

Figure 4-15. Misalignment (Twisting)

In accordance with the JPL section V standards, a flat plate module must withstand a twist of 1/2-inch per foot of module. Using this specification, the angle of twist is 0.0416 radians.

4.6 HAIL IMPACT

The Jet Propulsion Laboratory (JPL) has performed tests on several PV modules. The results of these tests are reported in reference [8] and summarized here. It was found that the top surface material of the module has a dominant influence on its hail impact resistance. In order of increasing impact strength for a given thickness, the top surface materials tested were: clear silicone rubber, annealed glass, tempered glass, and acrylic sheet. These results are summarized in figure 4-16.

TOP SURFACE OF PANEL

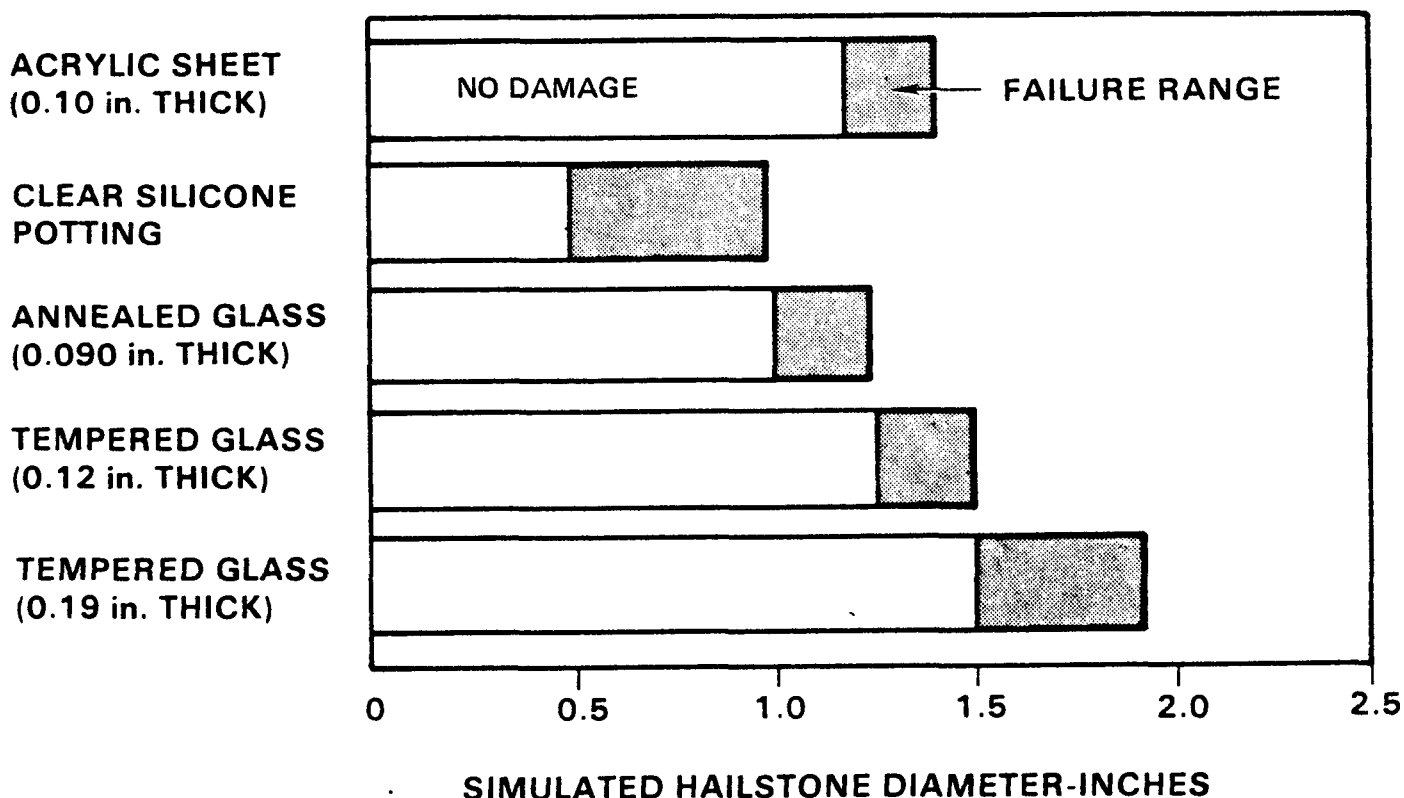


Figure 4-16. Type of Photovoltaic Panel Material Versus Simulated Hailstone Diameter

None of the tested panel designs, which incorporated clear potting silicone material as the outermost layer, was capable of protecting the silicon solar cells from damage due to impacts by simulated hailstones of 1-inch diameter or larger. Further tests of acrylic sheets determined that a 0.188-inch thick

sheet can withstand the impact of a 2-inch diameter hailstone. An evaluation of candidate solar panel top surface material is given in table 4-1.

Preliminary tests indicate that soft mounting has the potential for increasing the impact resistance of solar panels. For example, it was found that panels using rubber grommets resisted impact better than panels without grommets.

Based on the JPL section V standards, a PV module must be designed to withstand the impact of 1-inch diameter hail traveling at terminal velocity. Appropriate materials and thicknesses can be determined by referring to figure 4-16 or table 4-1.

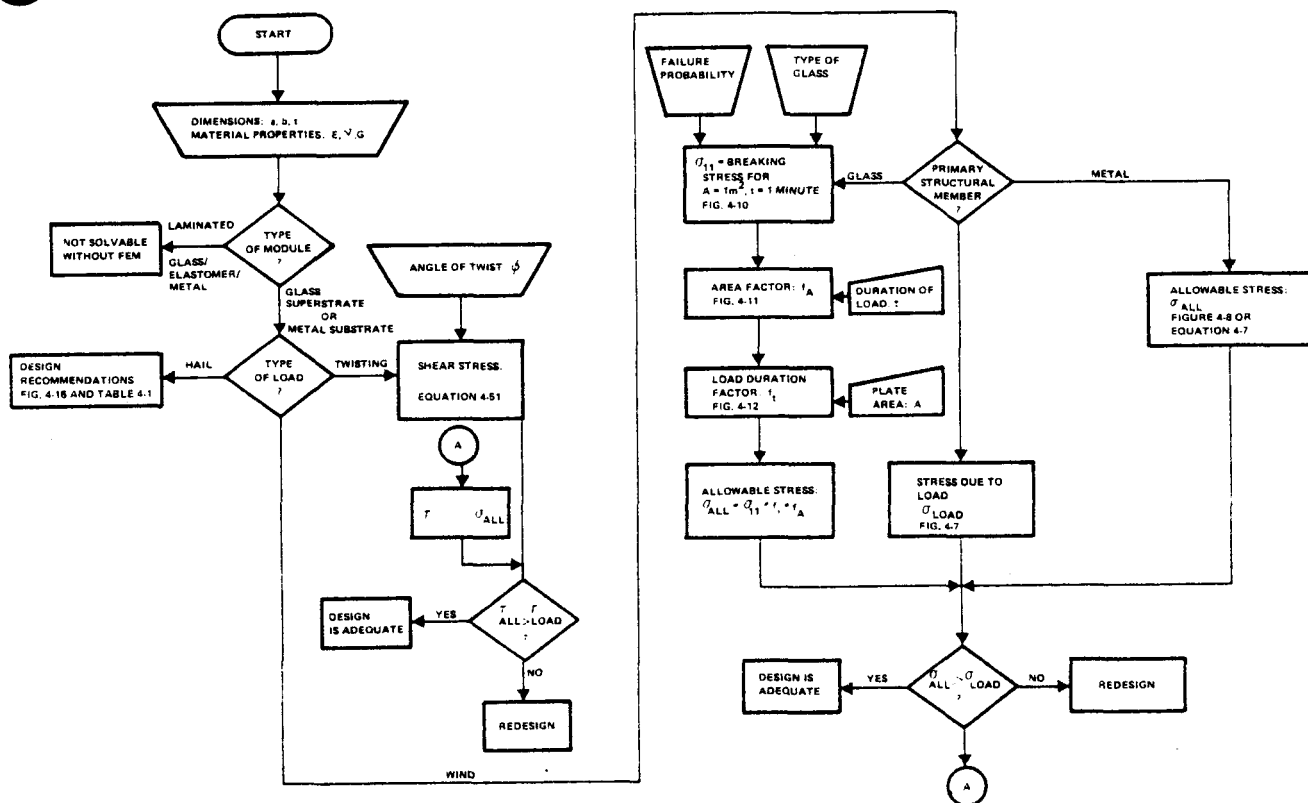
TABLE 4-1. EVALUATION OF CANDIDATE SOLAR PANEL
TOP SURFACE MATERIALS

MATERIAL	THICKNESS, INCHES	IMPACT RESISTANCE INCHES ^a	COST \$/ft ²	TRANSPARENCY	WEATHER RESISTANCE	ABRASION RESISTANCE
ANNEALED GLASS	0.125	1	0.3	EXCELLENT	EXCELLENT	EXCELLENT
TEMPERED GLASS	0.125	1 1/4	1.0	EXCELLENT	EXCELLENT	EXCELLENT
TEMPERED GLASS	0.188	1 1/2	1.5	EXCELLENT	EXCELLENT	EXCELLENT
ACRYLIC	0.100	1 1/4	0.8	EXCELLENT	VERY GOOD	GOOD
ACRYLIC	0.125	1 1/2	0.9	EXCELLENT	VERY GOOD	GOOD
ACRYLIC	0.188	2	1.0	EXCELLENT	VERY GOOD	GOOD

^aWITHSTANDS SIMULATED HAILSTONE OF DIAMETER INDICATED. [8]

4.7 STRUCTURAL ANALYSIS METHODOLOGY

The methodology for determining the structural adequacy of a PV module is shown in figures 4-17 and 4-18. The dimensions and material properties of the load bearing plate or receiver material are inputs to the methodology. Laminated structures with more than one load bearing plate require finite element modeling. Design recommendations pertaining to type and thickness of flat plate cover material, required to survive the impact of 1-inch diameter hail, can be obtained from figure 4-16 and table 4-1.



*FINITE ELEMENT ANALYSIS

Figure 4-17. Structural Design Methodology (Flat Plate)

For uniform loading such as wind or deadweight loads, the allowable stress is obtained for a flat plate and compared to the actual stress in the load bearing plate. The actual load stress is obtained from figure 4-7 for a given load intensity factor (equation 4-1) calculated for a given load defined in equations 4-6a or 4-6b, depending on whether static deadweight or cyclic wind loading is being considered.

For a glass superstrate, the designer defines a failure probability and, for a given temper of glass, σ_{11} is obtained from figure 4-10. For a given plate area, f_A is obtained from figure 4-11 and f_t is obtained from figure 4-12. The load duration is specified in JPL section V as 4.6 days for cyclic wind loading and 20 years for deadweight loads. The allowable stress is obtained from equation 4-10 for wind and deadweight loads and compared to the actual stress as in equation 4-11. If the load stress is less than the allowable stress then the design is adequate.

The allowable stress for a metal substrate is obtained from figure 4-8 or equation 4-7 for cyclic loads. For static loads the allowable stress is the stress in the given material at its yield point. The yield point of the substrate material must be provided by the user.

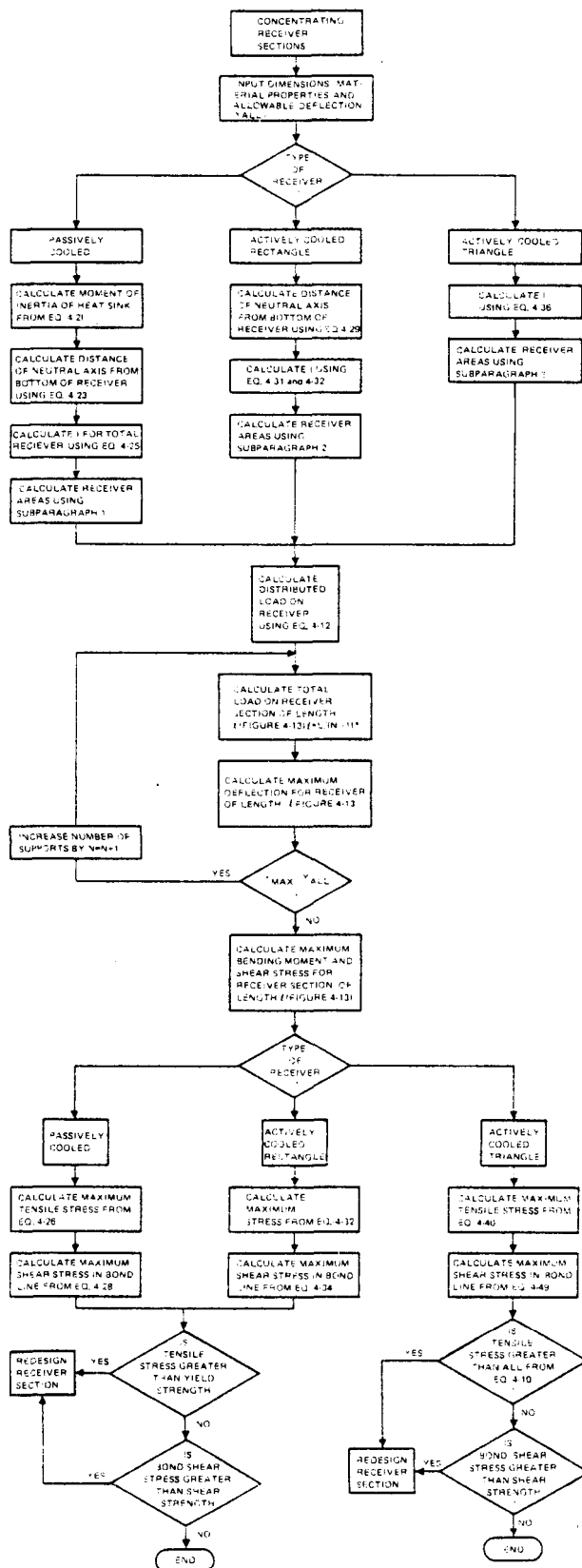
The stress due to twisting is then obtained from equation 4-51 and compared to the allowable shear stress defined in equation 4-50 for glass or metal plates. If the shear stress due to a twisting of 1/2-inch per foot is less than the allowable shear stress the design is adequate.

A flowchart showing the procedure for structural analysis and design of flat plate modules is provided in figure 4-17. Figure 4-18 contains a flowchart for determining stresses in the receiver section of a concentrating collector.

The user must provide the receiver section dimensions, material properties, and allowable deflection. For each type of cross-section the moment of inertia must be determined. The loading is then calculated using equation 4-12. Given the moment of inertia, loading, and length of the receiver section, the maximum deflection is determined using the relations in figure 4-13. This calculated deflection due to the load is then compared to the maximum allowable deflection and, if the calculated deflection is too large, a support, is placed at the center of the receiver. The deflection for one-half the total length of the receiver is then calculated and if it again exceeds the allowable deflection, a third support is added. This process continues until the deflection under load is less than the allowable deflection. The stresses in the receiver section can now be calculated using a length equal to the distance between supports.

The total loading for the section between supports is determined, and the maximum moment and shear stresses determined from the relations in figure 4-13. Using the moments of inertia calculated previously, the maximum tensile stress in the receiver section is calculated. If this occurs in metal, it is compared to the yield strength of the metal. If the maximum tensile stress is greater than the yield strength of the metal the receiver section should be redesigned. If the tensile stress under load occurs in the glass cell covering, it should be compared to the allowable stress in glass obtained from equation 4-10.

The shear stress in the bond between the PV cell and heat sink can also be obtained (see figure 4-18) and compared to the shear strength of the bonding material. If the shear stress is greater than the strength of the bond, delamination may occur, decreasing the thermal conductivity or dielectric strength of the bond line. Thus, the receiver section should be redesigned.



N = NUMBER OF SUPPORTS

Figure 4-18. Structural Methodology for Concentrating Collector Receiver Sections

<u>SYMBOLS</u>	<u>DEFINITION</u>
A	Partial area of beam
A_c	Area of PV cell assembly
A_f	Area of cooling channel
A_i	Area of layer i
A_m	Area of metal heat sink
A_t	Area of fins
a	Length of module plate
b	Width of module plate
β	Module tilt angle from horizontal
C	Distance from neutral axis
D	Flexural rigidity of module plate
δ	Deflection at the center of the module plate
E	Young's modulus of elasticity
E_c	Young's Modulus of the metal heat sink
E_m	Young's Modulus of PV cell assembly
f_A	Fraction of breakage stress of $1m^2$ glass plate
f_T	Fraction of 1-minute load duration breakage stress
G	Shear modulus
h_1	Interior receiver cross sectional height
h_o	Exterior receiver cross sectional height
I	Moment of Inertia
Ksi	Kilo pounds per square inch
LIF	Load Intensity Factor
M	Bending moment

<u>SYMBOLS</u>	<u>DEFINITION</u>
N	Number of pins
P	Load on module for LIF calculation
P_c	Density of PV cell assembly
P_D	Deadweight module load
P_f	Density of fluid
P_f	Probability of failure
ρ_i	Density of ith layer
P_w	Wind module load
ϕ	Angle of twist of module plate
P_i	Density of layer i
SIF	Stress Intensity Factor
σ	Bending stress in beam
σ_{ALL}	Allowable stress on substrate
σ_B	Breakage stress
σ_{BD}	Breakage stress for deadweight load
σ_{BW}	Breakage stress for wind load
σ_D	Maximum stress due to deadweight
σ_m	Endurance limit (1/2 ultimate strength)
σ_w	Maximum stress due to wind load
σ_{ll}	Glass breakage strength
t	Thickness of module plate
t_g	Thickness of PV cell assembly
t_i	Thickness of ith layer
t_m	Thickness of heat sink
V	Sheer force
T	Shear stress in beam

<u>SYMBOLS</u>	<u>DEFINITION</u>
T_{ALL}	Allowable shear stress
ν	Poisson's ratio
W_f	Width of fin
W_g	Width of PV cell assembly
W_i	Interior receiver cross sectional width
y	Centroid of beam
$\bar{y}$	Distance between neutral axis and centroid of area A
y_t	Distance from bottom of centroid to fins

4.9 REFERENCES

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2. A. Garcia, C. P. Minning and E. F. Cuddihy, "An Analytical Approach to Photovoltaic Encapsulation System Design," Fifteenth IEEE Photovoltaic Specialists Conference, pp. 460-465, Orlando, Florida, May 1981.
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4. T. Brumeister, ed. Marks' Standard Handbook for Mechanical Engineers, 8th Edition, McGraw-Hill Book Co., 1978.
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8. D. Moore and A. Wilson, Photovoltaic Solar Panel Resistance to Simulated Hail, Low-Cost Solar Array Project Report #5101-62, Jet Propulsion Laboratory, Pasadena, California, October 15, 1978.



SECTION 5.0 ECONOMICS METHODOLOGY

5.1 INTRODUCTION

The economic methodology incorporated into the module optimization methodology is based upon Improved Price Estimation Guidelines (IPEG) developed by the Jet Propulsion Laboratory (JPL). The electrical, structural, and thermal algorithms produce an optimized module electric and mechanical configuration. The economics algorithm permits a cost trade-off analysis between alternative configurations. The user must input projected cost elements for each process in a manufacturing sequence. Standardized typical item costs are published in the SAMICS Cost Account Catalog (JPL Document 5101-154, April 1980).

Individual cost elements for each manufacturing process are burdened to incorporate overhead costs. The total process cost is inflated to adjust for subsequent process yield efficiencies. All output costs are expressed in \$/Wp to permit intertechnology and intratechnology comparison. Section 5.2 explains the costing methodology in detail. Section 5.3 develops an FOB cost/Wp for a specific technology as an example of the costing algorithm using the Honeywell SOC process.

5.2 METHODOLOGY

The IPEG is a standardized methodology for estimating manufacturing costs. Manufacturing is viewed as a sequence of identifiable production processes. The price of the final product is in essence the sum of the costs generated by each production process. Production costs consist of two elements: direct charge items and indirect charge items. Direct charge items are consumed during production. Operator labor is an example of a direct item. All direct costs are stated as \$/M² to facilitate intermodule comparison. Indirect charge items are not consumed by production but are necessary to support the production process. Operator supervision is an example of an indirect charge item. IPEG allocates a uniform indirect cost to each specified direct cost.

The production process cost equation is:

$$\text{COST} = K_1 * \text{EQPT} + K_2 * \text{SQFT} + K_3 * \text{DLAB} + K_4 * \text{MATS} + K_5 * \text{UTIL}$$

where EQPT = cost of equipment

 SQFT = square footage of floorspace required for equipment and operator

 DLAB = salary of operators without fringes

 MATS = cost of direct materials and supplies

 UTIL = cost of direct utilities

All of these process costs are limited to a specific process. The process costs are calculated in accordance with IPEG-2¹. Let

M = minutes/operating year

D = Process duty cycle

R = Yielded process output rate

S = Output unit size in square meters

then:

$$\text{EQPT cost} = \frac{(\text{Installed cost} - \text{salvage value}) * K_1}{M * D * R * S}$$

$$\text{SQFT cost} = \frac{(\text{Manufacturing floor space}) * K_2}{M * D * R * S}$$

$$\text{DLAB cost} = \frac{\text{Annual salary} * \frac{\text{operator}}{\text{machines run}} * 4.7 \frac{\text{shifts}}{\text{year}} * K_3}{M * D * R * S}$$

$$\text{MATS cost} = \frac{\frac{\text{Item cost}}{\text{unit product}} * K_4}{R * S}$$

$$\text{UTIL cost} = \frac{\frac{\text{Item cost}}{\text{unit product}} * K_5}{R * S}$$

The process coefficients are process independent and are:

K₁ is a function of process equipment life:

<u>Life (Years)</u>	<u>K₁</u>
3	0.83
4	0.65
7	0.57
10	0.52
15	0.48
20	0.46

¹R.W. Aster, "IPEG-2 Improved Price Estimation Guidelines," LSAP Progress Report No. 14, JPL Document 5101-142, Jet Propulsion Laboratory, Pasadena, CA December 1979.

$K_2 = \$109/\text{ft}^2$
 $K_3 = 2.8$
 $K_4 = 1.2$
 $K_5 = 1.2$

The coefficients adjust a direct input cost to reflect the indirect charges encountered in a typical photovoltaic module production facility. These constants are process independent but are based on 1980 dollars. If process specific coefficients are required, a SAMIS run will be required. (JPL 5101-60, Solar Array Manufacturing Industry Simulation Computer Program Users Guide).

Successive process yield factors influence the costs of preceeding processes. The inverse of the product of each successive process yield factor establishes the effective cost of a specific process for a given level of PV production. This relationship for process n can be stated by the equation:

$$\text{Effective Cost } n = \frac{\text{Cost}_n}{Y_{n+1} * \dots * Y_{n+m}}$$

where:

Cost_n = process cost established by IPEG algorithm

Y_n = yield factor for process n

Y_{n+1} = yield factor for process n + 1

Y_{n+m} = yield factor for final manufacturing process

The module optimization costing algorithm projects PV cost as an estimated \$/M². An adjustment is made to compensate for the effective PV surface of a module. The total cost of the module is multiplied by the inverse of cell packing density. Multiplying the adjusted cost by the inverse of the product of AM1 insolation and cell efficiency converts the module cost to \$/Wp.

5.3 ECONOMIC METHODOLOGY APPLICATION

As an example of the Module Optimization economic methodology an FOB cost/Wp was generated for the Honeywell SOC technology.² The Honeywell SOC technology was used as an example because the data contained in [2] represented the most

²Process sequence and cost input data used with permission from S. Schuld, et al, "Low-Cost Manufacturing Potential of Silicon-On-Ceramic Photovoltaic Modules," Honeywell Corporation, Bloomington, MN, April 1981.

complete production cost figures available for the preparation of this report. Data are extracted from [2] for the first process, CARBCOAT. The SAMICS Format A is depicted in figure 5-1. Data entered into the module optimization algorithm is:

Process name: CARBCOAT
 Duty Cycle (A-8): 0.95
 Yielded Output Rate (A-6): 15.52
 Piece Size in m² (A-5): 0.116
 Process yield (A-28): 99.99
 EQPT: 10450
 LIFE: 7
 SQFT: 192
 DLAB: 1598.57
 MATS: 8.907
 UTIL: 0.0066

The cost is calculated according to the following methodology, using cost data and production estimates from [2].

M = 525,600 (minutes per calendar year) Honeywell production estimate
 D = duty cycle (line A-8 of Format A, figure 5-1)
 R = yielded output rate (line A-6, figure 5-1)
 S = unit size in square meters
 F = conversion factor for line A-23, figure 5-1, 1980 dollars per unit quantity
 K = IPEG-2 coefficient
 \$ = burdened cost per square meter

EQPT

$$\$ = (A11 + A14 - A13) * K_1 / (M * D * R * S)$$

where A11 means entry on line A-11, figure 5-1 (1980 dollars assumed), and K₁ depends on equipment life.

SQFT (Type A Manufacturing Space)

$$\$ = (109) * A19 / (M * D * R * S)$$

DLAB

$$\$ = (4.7) * (2.8) * A18 * Q / (M * D * R * S)$$

where Q is annual salary without fringe benefits (1980 dollars), with 4.7 shifts are required for continuous factory operation (Honeywell estimate).

MATS and UTIL

$$\$ = (1.2) * A22 * F / (R * S)$$



SOLAR ARRAY MANUFACTURING INDUSTRY COSTING STANDARDS

Page 1 of 2

FORMAT A — PROCESS DESCRIPTION

SOLAR PROPRIETARY LABORATORY
Copyright © 1975 by Solar Energy Research Institute
1700 East Street, Suite 100, Boulder, CO 80501

A-1 Process (Referent)

CARBCOAT

Note: Names given in brackets () are the names of process attributes requested by the SAMIS computer program.

A 2 [Descriptive Name] of Process	Apply carbon-in-alcohol suspension to one surface of panels		
PART 1 — PRODUCT DESCRIPTION			
A 3 [Product Referent]	COC		
A 4 Descriptive Name [Product Name]	Carbon coated panel		
A 5 Unit Of Measure [Product, Units]	Panels - 0.116 M ²		
PART 2 — PROCESS CHARACTERISTICS			
A 6 [Output Rate] (Not Throughput)	15.52	Units (given on line A 5) Per Operating Minute	
A 7 [In-process Inventory, Time]	0.350	Calendar Minutes (Used only to compute in-process inventory)	
A 8 [Duty Cycle]	0.95	Operating Minutes Per Minute	
A 8a [Number Of Shifts Per Day]	3.0	Shifts	
A 8b [Personnel, Intergration, Override, Switch]	Off	(Off or On)	
PART 3 — EQUIPMENT COST FACTORS (Machine Description)			
A 9 Component [Referent]	CRBCOATER		
A 9a Component [Descriptive Name]			
A 10 Base Year For Equipment Prices [Price, Year]	1980		
A 11 [Purchase Cost Vs. Quantity Bought Table] (Number Of and \$ Per Component)	11,000		
A 12 Anticipated [Useful Life] (Years)	7		
A 13 [Salvage Value] (\$ Per Component)	1,100		
A 14 [Removal And Installation Cost] (\$/Component)	550		

Note: The SAMIS computer program also prompts for the [Payment, Float, Interval], the [Inflation Rate Table], the [Equipment Tax Depreciation Method], and the [Equipment Book Depreciation Method]. In the LSA SAMIS context, use (1) 0, (1975 6 0 +), DOB, and SL. (The asterisk is a signal to the computer, not a reference to a footnote.)

Format A — Process Description (Continued)

Page 2 of 2

A 15 Process Referent (From Front Side Line A 1) CARBCOAT

PART 4 — DIRECT REQUIREMENTS PER MACHINE (Facilities) OR PER MACHINE PER SHIFT (Personnel)				
[Facility, Or, Personnel Requirement]				
A 16 Catalog Number (Expense Item Referent)	A 18 Amount Required Per Machine (Per Shift) (Amount, Per, Machine)	A 19 Units	A 17 Requirement Description or Name	
A2064D	192	Sq. Ft.	Type A manufacturing space	
B3752D	0.125	Person/Shift	Production Machine Operator	
PART 5 — DIRECT REQUIREMENTS PER MACHINE PER MINUTE (SAMIS will ask first for Byproducts)				
[Byproduct] and [Utility, Or, Commodity Requirement]				
A 20 Catalog Number (Expense Item Referent)	A 22 Amount Required Per Machine Per Minute (Amount, Per, Cycle)	A 23 Units	A 21 Requirement Description or Name	
E1352D	0.082	\$/Min.	Carbon in isopropanol suspension	
C1032B	0.0091	Gal./Min.	Alcohol, Isopropyl	
	0.167	KWH/Min.	Electricity	
	1.8	*Sq.M./Min.	Slotted ceramic panels	
PART 6 — INTRA INDUSTRY PRODUCT(S) REQUIRED				
A 24 [Required Product] [Reference]	A 28 [Yield] * (%)	A 26 [Ideal Ratio] ** Of Units Out/Units In	A 27 Units Of A 26***	A 25 Product Name
None	99.99	1/1	Panel/Panel	
PREPARED BY S.B. Schuldt, CTC				
DATE				12/8/80

*100% minus percentage of required product lost in this process.

** Assume 100% yield here

*** Examples: Module/Cell or Cells/Water

Rev. 4/3/81

Figure 5-1. SAMIS Format A [2]

The projected burdened cost for CARBCOAT is \$6.014/m²; the effective cost for CARBCOAT (the consequence of successive process yield factors) is \$7.296/m².

Table 5-1 presents the projected process costs and effective process costs for the Honeywell SOC technology. These costs are selected for sheet concept C and Module Concept III as reported in reference 2. These concepts were selected as an example because they represented the most complete cost data available to demonstrate the methodology. The total cost/m² projected by Module Optimization is \$45.25/m². This cost is obtained by summing the effective costs shown in table 5-1. A cell packing density of 0.9767 and a module efficiency of 10.5 percent yields a projected cost of \$0.441/Wp.

5.4 ECONOMIC GLOSSARY

EQPT - cost of equipment
SQFT - square footage of floorspace required for equipment and operator
DLAB - salary of operators without fringe
MATS - cost of direct materials and supplies
UTIL - cost of direct utilities
M - minutes per operating year
D - process duty cycle
R - yielded process output rate
S - output unit size in M²
K - process coefficient

TABLE 5-1. EXAMPLE OF THE ECONOMIC METHODOLOGY USED TO CALCULATE
HONEYWELL SOC PROCESS COSTS

Process	EQPT	SQFT	DLAB	MATS	UTIL	Total	Process Yield	Cumulative Yield	Effective Cost/M ²
CARBCOAT	0.0066	0.0233	0.0234	5.956	0.0047	6.014	0.9999	.8244	7.2959
SAILCOAT1	2.163	0.195	1.706	0.862	0.240	5.166	0.95	.8678	6.2664
SILTEST	0.0796	0.0853	0.7116	--	0.0024	0.879	1.00	.8678	1.0129
IMPLANT	0.882	0.028	0.870	0.157	0.050	1.93	0.98	.8855	2.2240
ANNEAL	0.542	0.014	0.260	0.067	0.017	0.90	0.995	.8899	1.0164
BACKIMPL	0.685	0.014	0.870	0.173	0.050	1.792	0.995	.8944	2.0137
BACKANNL	0.542	0.014	0.260	0.067	0.017	0.900	0.995	.8989	1.0063
ARCOAT	0.865	0.25	0.483	0.061	0.180	2.14	0.99	.9080	2.3807
MASK	0.0747	0.0932	0.769	0.436	0.014	1.39	0.995	.9125	1.5308
ARETCH	0.0032	0.0133	0.0439	0.0089	--	0.07	0.995	.9171	.0767
PDCAT	0.0497	0.0932	0.769	0.159	--	1.07	0.995	.9217	1.1667
NIPLATE	0.0176	0.0266	0.439	0.0681	0.0058	0.56	0.995	.9263	.6076
SOLCOAT	0.0779	0.160	0.879	0.552	0.0252	1.69	0.995	.9310	1.8245
INSPSORT	0.070	0.019	0.107	--	0.001	0.197	0.95	.98	.2116
INTERCON3	0.369	0.065	0.359	2.843	0.010	3.637	0.99	.9899	3.7112
MODFAB2	0.285	0.191	0.879	10.629	0.007	11.991	0.99	.9999	12.1133
MODTEST	0.018	0.017	0.051	--	0.004	0.090	1.00	.9999	.0900
PACKAGE	0.0054	0.057	0.411	0.228	0.0003	0.702	0.9999	1.0000	.7021



SECTION 6.0
PVMOC: A USER-ORIENTED CODE FOR PHOTOVOLTAIC
MODULE OPTIMIZATION ANALYSIS

6.1 INTRODUCTION

The Module Optimization Methodology, a design and analysis tool for advanced photovoltaic (PV) cells, has been developed into a computer program called PVMOC (PhotoVoltaic Module Optimization Code). This section is a guide to the use of the PVMOC program. It includes a complete description of the code with an executive flowchart and example runs. The examples used in the previous sections to illustrate the manual use of the algorithm have been reproduced in section 6.3 using PVMOC. The test cases which have been used to exercise the code are described in section 6.4

6.1.1 Photovoltaic Module Optimization Code-Overview

The PVMOC program performs the five types of analysis described earlier in this report: electrical, conductor requirements, thermal, structural, and economic. While each analysis may be run independently of other analysis types, data may be generated by one analysis and used in another. For example, a cell temperature computed by thermal analysis may be used in the electrical analysis input.

The computerized PV module optimization scheme is performed by two programs: the input processor (PVINP) and the computational code (PVMOC). The input processor is an interactive data entry aid to constructing an input file for the computational code. Upon execution, PVINP prompts the user as to what type of analysis to run, then asks for appropriate data. For example, if one wishes to run a structural stress analysis on a PV module, questions relating to module size, load, and strength will be asked. The responses to these questions are written on an input file that is structured to be read directly by the PVMOC computational code.

The PVMOC program, greatly enhances the speed at which PV design analyses may be performed. The PVMOC operates on the SERI CDC-720 computers in either Batch or Interactive mode.

6.1.2 Functional Description

The PVMOC program and job controls were designed to be used with as little effort on the user's part as possible. IMPORTANT: The user must be familiar enough with the analysis requirements to be able to enter the correct inputs into the input processor PVINP. Knowledge of NOS (Network Operating System) batch and interactive Job Control (JC) statements is not necessary since examples are included in this manual.

6.1.3 Code Development Philosophy

The PVMOC program and PVINP input pre-processor were designed to be user friendly and simple to use. The PVMOC program was developed with a program design tool called Program Design Language (PDL). PDL requires that the program be outlined in a top-down structured form that is more comprehensive than flowcharts. Each PDL statement is an abbreviated description of a process or set of processes to take place in the program. Usually (as in the case of PVMOC), FORTRAN statements applying to a particular process are inserted directly after the PDL statement that describes the process. Thus, the PDL statements serve as code comments. For example, the input portion of a generic code may be designed as follows using PDL:

```
C*INPUT LENGTH AND WIDTH OF MODULE.  
C*INPUT NUMBER OF LAYERS IN MODULE.  
C*DO FOR EACH LAYER.  
C    *INPUT TEMPERATURE GUESS IN DEGREES FOR EACH LAYER IN MODULE  
C    *CONVERT TEMPERATURE TO DEGREES R.  
C*ENDDO.
```

This portion describes the input of the module length and width, number of layers in the module, and a temperature for each layer. In addition, each temperature is converted to degrees Rankine as it is read. FORTRAN statements are inserted as follows:

```
C*INPUT LENGTH AND WIDTH OF MODULE.  
    READ(4,10) XLEN  
    READ(4,10) WIDTH  
10  FORMAT(F6.2)  
C*INPUT NUMBER OF LAYERS IN MODULE.  
    READ(4,20) NLAYER  
20  FORMAT(I2)  
C*DO FOR EACH LAYER.  
    DO 40 I=1,NLAYER  
C    *INPUT TEMPERATURE GUESS IN DEGREES F FOR EACH LAYER IN MODULE  
    READ(4,30) TEMP(I)  
30  FORMAT(F7.2)  
C    *CONVERT TEMPERATURE TO DEGREES R.  
    TEMP(I) = TEMP(I) + 459.7  
C*ENDDO  
40  CONTINUE
```


The PDL is written and checked line by line by hand for logic errors. Then the FORTRAN is added where specified by the PDL. If the logic in the PDL checks, there should be no logic errors in the FORTRAN. This was the case in PVMOC. No logic errors were found in PVMOC and debugging was restricted to typographical and arithmetic errors.

The PVMOC program is divided into five major subprograms--one for each analysis. Each of these subprograms operates independently of the others, however all subprograms may be run back-to-back at one time in this order: thermal, electrical, structural, economic and conductor requirements. Because array storage requirements are relatively low, arrays are dimensioned within applicable subroutines.

When using the PVMOC program to design or evaluate the design of a PV module, resultant output evaluation is based solely on information entered by the user (user input). Some of the analyses are so sensitive that a small variability in only one parameter could effect a positive or negative evaluation. In other words, a negative evaluation could be remedied by changing one variable a small amount. With each run, however, the PVMOC program reads all variables. This necessitates an input file strategy in the program to eliminate the need for entering all input variables each time PVMOC is run.

Generating an input file by hand is relatively simple if one knows the code inputs and formats. A method has been devised that makes input entry as painless to the user as possible. A separate program called PVINP, the user input pre-processor, queries the user at an interactive terminal work station. The user need not burden himself with formats or the order of data entry. The PVINP program automatically places each value in its proper location on the file with the proper format, then adds a description which explains what the value is.

Example data line in input file generated by PVINP:

160.25 FRAME LENGTH

Should the user enter an incorrect value while running the input processor or wish to change a single value after running PVMOC, it is not necessary to rerun the entire input processor to change the value. The input file called TAPE4 may be loaded into the editor and the incorrect value may be changed. Since descriptions of each value are contained in TAPE4, locating an incorrect value is easy.

6.1.4 SERI Computer System Operation

The PVMOC program is operational on the SERI CDC-720 computer. The program architecture was written to allow operation of the PVMOC program in either batch or interactive time share. Job control statements for both batch and interactive operation are included in section 6.2.

Since the PVMOC program runs in a relatively short time, (less than one CPU second usually) most users will probably want to run it under interactive time share from a remote terminal. With an input file (TAPE4) already created, time share turnaround is usually within five minutes on the CDC-720 with

results being printed at the terminal. Depending on backlog, batch turnaround may be either slower or faster, however PVMOC output is printed at either the central site or a specified RJE site. The PVINP input pre-processor may only be run on remote time share. However, the input file (TAPE4) may be created several ways:

- Run PVINP to create TAPE4 (preferred method).
- Create TAPE4 in XEDIT editor (not recommended).
- Punch cards, then read cards into TAPE4 file (not recommended).

The second and third methods above are not recommended since the user must keep track of variable format and order. The PVINP program handles this automatically.

6.1.5 PVMOC Operational Overview

All input for the PVMOC program is contained in TAPE4, generated automatically by PVINP. The PVMOC job control statements automatically retrieve TAPE4 and cause execution of the PVMOC program. Program output contains the results of the analyses and is written on a file called TAPE6.

The PVMOC program begins execution by entering a driver subroutine. The driver evaluates which analysis (analyses) will be performed based on information on the first line of the input file TAPE4. Then the appropriate subprogram(s) is called. The five main subprograms are named appropriately Elect, Therm, Struct, Econ and Conreq for electrical, thermal, structural, economic and conductor requirement analysis respectively. Each of these analyses is described in more detail in their respective sections in this document.

Analysis results are written on the output file TAPE6 which defaults to the printer in batch mode. For examination in interactive time share mode, TAPE6 may be placed in the XEDIT editor.

6.2. USING THE PVMOC PROGRAM

In this section, complete instructions for running the PVMOC program will be presented. This section is divided into two parts, one for the input pre-processor PVINP, and the other for PVMOC. Pay particular attention to the "conditions and limitations" sections. These will help the user to avoid trying to make PVMOC do things of which it is incapable. As with most computer programs, the best way to learn to use PVMOC is to run it. This section guides the user step by step through the operation of PVINP and PVMOC.

6.2.1 Input Pre-Processor PVINP

As mentioned previously, the PVINP program is a user-interactive program for the generation of the PVMOC input file called TAPE4. The user is queried at the terminal for each parameter and responds by typing in the parameter in the format and units specified. The responses are then written in the correct order and format on the TAPE4 file.

6.2.2 PVINP Use

To obtain the job control (JC) string for operating PVINP, the user must type:*

```
GET,INPJCL/UN=CAT73
```

The INPJCL JC string is as follows:

```
GET,PVINPC/UN=CAT73.
```

```
REWIND,PVINPC.
```

```
PVINPC.
```

To run PVINP, type:

```
CALL,INPJCL
```

The user will then be queried appropriately. Obviously, if only a thermal analysis is to be performed, the user will not be asked questions pertaining to an electrical analysis:

Prompts generated by PVINP include a description of the parameter, the units (i.e., feet, degrees F, etc.), and format (i.e., floating point F8.2, integer I3, etc.).

Upon answering the questions, parameter values are automatically written to TAPE4 with descriptions of the values. To change a single variable or a series of entered values, it is not necessary to (although one could) rerun PVINP. Simply put TAPE4 in the XEDIT editor and change the necessary numbers. For example, to change the value for module width in the second line of the file called TAPE4, insert TAPE4 into the XEDIT editor and perform the following:

```
p19 <----- p19 means print the first 19 lines
10000      THERMAL,ELECTRICAL,STRUCTURAL,COST,METALIZATION
FP        TYPE OF MODULE
SI        PV CELL TYPE
AD        TYPE OF COOLING
0.00      RATIO OF FIN AREA TO BACKING ROOT AREA
2         NUMBER OF NODES (LAYERS)
1         1 ==> GLASS LAYER
0         1 ==> UPPER ENCAPSULANT LAYER
1         1 ==> PV CELL LAYER
0         1 ==> LOWER ENCAPSULANT LAYER
0         1 ==> BACKING LAYER
0         1 ==> FRAME
.125      MATERIAL THICKNESS FOR MATERIAL 1
0.00      MATERIAL THICKNESS FOR MATERIAL 2
0.00      MATERIAL THICKNESS FOR MATERIAL 3
0.00      MATERIAL THICKNESS FOR MATERIAL 4
0.00      MATERIAL THICKNESS FOR MATERIAL 5
0.00      MATERIAL THICKNESS FOR MATERIAL 6
47.500 11.75<----- MODULE LENGTH,WIDTH
?? c/11.75/11.50/----- We want to change
47.500 11.50<----- MODULE LENGTH,WIDTH      this value to 11.50.
?? e,taped4----- Value has
TAPE4 IS A LOCAL FILE      been changed.

READY.
replace,taped4<----- Replace old taped4 file
                        on disk with new taped
                        file.

READY.
```

*It is assumed that the user has logged on successfully.

In any case, XEDIT is handy for checking the TAPE4 file before it is made permanent disk file. The PVMOC JC string expects TAPE4 to be a permanent disk file. To save TAPE4 on disk, type:

SAVE,TAPE4

If TAPE4 already exists, (left over input file from earlier analysis), type:

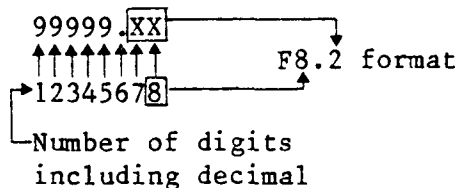
REPLACE,TAPE4

This will overwrite the earlier TAPE4 file with the new one. If one wishes to save the old TAPE4, copy the old TAPE4 to a different file name and save that new file name.

6.2.3 Conditions and Limitations

The only major condition on the PVINP program itself is that data must be entered in the proper format in order to write TAPE4 correctly. Other conditions pertain to the data contents themselves. Certain values in input will not work or may cause erroneous answers in the analysis.

Data must be entered in the format specified in the query. This pertains mostly to integer data contained in an I format. Floating point data may be specified in just about any form, however it must not exceed the bounds of the format. For example, numbers that will never be greater than 99999.99 and should be taken to two places will be specified as follows:



Ideally, the number 132.16 would be entered `132.16` where denotes a space. However, this number may be entered simply 132.16 without the leading spaces since FORTRAN F format uses the decimal as a reference. The F format is used in most numerical entries. A decimal point must be included in all F format data entries, or a series of *'s will be written in the numeric field.

One must be careful when entering integer values. For example, when entering the number "3" into an I3 integer field, the number "3" must be right justified. An I3 field will accept a number up to 999. The number "3" is entered as follows:

`3` where denotes a space.

Entering the following:

3 without leading spaces will be read as 300 on an I3 format! THIS IS ONE OF THE MOST IMPORTANT FACTS TO REMEMBER WHEN RUNNING PVINP.

There are specific conditions on inputs as queried by the input processor:

- For the thermal and structural inputs, the user is given the choice of entering length, temperature data in units of inches, °F or centimeters, °C. However, if data is entered in units of cm, °C; it is converted in the input processor to inches, °F for the input file. Therefore, if you enter a module length of 120.65 cm, do not be surprised to see 47.5 inches in the input file listing.
- Answer questions where the choices are given in parentheses such as (Y or N) or (SI, GA, or CD) only with answers provided. (M for "maybe" will not work where Y or N is expected.)
- Answer percent values in decimal percent unless otherwise specified. For example 92 percent should be entered as .92.
- Make sure temperatures are entered in the proper units.
- On load duration units, S, M, H, D, W, T, Y correspond to Seconds, Minutes, Hours, Days, Weeks, Months, Years respectively. The PVINP processor asks for time durations in above units.

For the example of 20 minutes, answer the first question with "M" and the second question with "20."

- Do not make obvious mistakes such as PV cell dimensions greater than module dimensions.
- Check the file TAPE4 for errors. If the data is not correct, the PVMOC program will either issue error messages, or generate erroneous data in the analysis. Check for "*****" in a numerical data field. This means the number entered is too big or that the decimal point was omitted in an F format number.

6.2.4 Computational Program PVMOC

As mentioned previously, the PVMOC program runs any of five module analyses; electrical, conductor requirements, thermal, structural, and economic. The analyses follow the methodologies described in previous sections as closely as is feasible. Output is written to a file called TAPE6 and may be displayed on the user's terminal in time share mode or is sent to a central site line printer in batch mode.

6.2.5 PVMOC Use

To obtain the time share job control (JC) string for operating PVMOC, the user must type:

```
GET,PVJCL/UN=CAT73
```

The PVJCL time share JC string is as follows:

```
GET,PVMOCC/UN=CAT73.  
GET,TAPE4.  
REWIND,PVMOCC,TAPE4.  
PVMOCC.
```

The PVJCL JC string will operate only if the TAPE4 input file has been stored on permanent disk (see section 2.1.1).

To run PVMOC in time share, type:

```
CALL,PVJCL
```

PVMOC will then automatically be executed and all output will be written on the file called TAPE6. If one wishes a hardcopy of the output, list TAPE6 and use a printer-terminal or a CRT terminal with a screen dump hardcopy device.

When running batch, PVMOC output is always sent to the central site line printer for pickup. To obtain the PVMOC batch JC string, type:

```
GET,PVBAT
```

The PVBAT batch JC string is as follows:

```
Jobname,CM200000.  
ACCOUNT,username,password.  
CHARGE,charge number, project number.  
GET,PVMOCC/UN=CAT73.  
GET,TAPE4.  
REWIND,PVMOCC,TAPE4.  
PVMOCC.
```

Where:

```
Username      = 1-7 character user number  
Password      = 0-7 character password  
Charge Number = 1-10 character charge number  
Project Number = 1-20 character project number
```

To run this JC string (execute PVMOC batch), it is necessary to submit the JC for batch processing. To do this, type:

```
SUBMIT,PVBAT,B
```

Output is diverted to a local batch printer because of submit option "B".

The PVMOC interactive output is written to a file called TAPE6. This file may be listed by typing the following into the terminal:

```
XEDIT,TAPE6    (Place TAPE6 in the editor)
P*             (Print all lines)
```

6.2.6 Options

The following major program options are available in each of the five analyses. Additional subprogram input options have been flow charted in previous sections of this report.

- Electrical. Six design options are available. They are (in order of decreasing packing fraction):

Design Option Number	Description
1.	Maximum cell area and maximum module dimensions
2.	Number and dimensions of cells
3.	Fixed cell and maximum module dimensions
4.	Maximum cell width and area and fixed module dimensions
5.	Maximum cell area and fixed module dimensions
6.	Maximum cell dimensions and fixed module dimensions

A complete description of these design options is included in section 2.0. The design option number is entered into the input processor and the user will automatically be queried for the correct inputs needed for that option.

- Thermal. Options for the thermal model include solutions for flat plate and concentrating collectors, liquid or air cooled, any variety of up to five layers and a frame, insulated or cooled back (with or without fins), and point or line focus Fresnel systems or linear parabolic trough systems.
- Structural. Options for the structural model include solutions for flat plate or concentrating collectors with three basic geometries for concentrating collectors, and actively or passively cooled heat sinks. Also, several types of glass and heat sink materials may be chosen from the PVINP menu.
- Economic. The economic analysis is fairly straightforward. There are really no "options." The economics methodology is performed exactly as outlined in section 5.0.
- Conductor Requirements. Given the materials and electrical properties of a conductor, either minimum conductor width based on maximum thickness or minimum conductor thickness based on maximum width or both may be computed. These options are entirely up to the user.

6.2.7 Conditions and Limitations

Correct data entry ensures that the PVMOC program will function correctly. The analyses performed is only as good as the input data it has to work with. The user, therefore, should be aware of the following conditions:

- In the electrical and structural models, the code will stop when certain conditions are not met. A diagnostic is also written such as

"Module aspect ratio > 4.0"

and the program is halted. (NP is defined in the Glossary at the end of section 2 as the number of cells in a parallel direction in the module. Definitions for variable names are found in each sections respective glossaries.) Input variables must be changed to remedy the problem. Check section 2.0 for a diagnosis of the problem.

- The economic model output is 132 columns wide and wraparound will make it hard to read on an 80 column terminal. The economic model output should be listed on a 132 column terminal or be submitted as a batch job.
- ENTER THE CORRECT DATA! Incorrect data will yield incorrect results or errors.
- The thermal analysis cannot be performed without a PV cell layer. Be sure to specify a PV cell layer in the user input.
- The thermal analysis requires at least two layers in the module. One of the layers must be PV cells.

6.3 PVMOC EXAMPLES

The sample methodology test problems shown in sections 2-5 were run through the PVMOC program which generated the following analysis results. The input file and results of each run is included. Each facet of each run is separated by a page or continued as specified.

6.3.1 Electrical Example

This is the PVMOC run for the electrical example (design option 6) shown in section 2.3.

INPUT FILE

01000

THERMAL, ELECTRICAL, STRUCTURAL, COST, METALIZATION
*****ELECTRICAL ANALYSIS INPUTS*****

```

C          INPUT OR COMPUTE ELECTRICAL PARAMETERS
5          NUMBER OF POINTS ON I VS V CURVE
    0.00    25.00    V( 1) ,J( 1)
    .45     24.10    V( 2) ,J( 2)
    .50     23.00    V( 3) ,J( 3)
    .55     17.30    V( 4) ,J( 4)
    .60      0.00    V( 5) ,J( 5)
100.000
          INSOLATION
4          NUMBER OF OUTPUT VOLTAGES
    5.0      VOLTAGE VMPP( 1)
   10.0      VOLTAGE VMPP( 2)
   15.0      VOLTAGE VMPP( 3)
   20.0      VOLTAGE VMPP( 4)
   25.0      CELL TEMPERATURE
   96.0      MAXIMUM CELL AREA
   20.0      AMBIENT AIR TEMPERATURE
Y          DO YOU WISH TO COMPUTER POWER DISSIPATED?
100.0      MAXIMUM CELL TEMPERATURE
    .0035000    DELTA T/DELTA S
    .0030000    DELTA T/DELTA P
    .7          FORWARD DIODE VOLTAGE
   -0.0022000    PARTIAL OF VOLTAGE WITH RESPECT TO TEMP.
  -20.0      LOWEST ANTICIPATED CELL TEMPERATURE
    3          NUMBER OF INTERCONNECT RIBS ON CELL
   30.0      MAXIMUM OC VOLTAGE AT TL
  -10.0      BREAKDOWN VOLTAGE (< 0.0)
6          DESIGN OPTION NUMBER 1,2,3,4,5, OR 6
    .15875    SPACING BETWEEN CELL IN SERIES DIRECTION
    .15875    SPACING BETWEEN CELLS IN PARALLEL DIRECTION
    .95250    DISTANCE BETWEEN CELL AND FRAME EDGE IN SERIES
    .95250    DISTANCE BETWEEN CELL AND FRAME EDGE IN PARALLEL
    6.00000    MAXIMUM CELL DIMENSION IN SERIES DIRECTION
   16.00000    MAXIMUM CELL DIMENSION IN PARALLEL DIRECTION
  120.65000    LENGTH OF MOD IN SERIES DIRECTION
  120.65000    LENGTH OF MOD IN PARALLEL DIRECTION

```

OUTPUT

*****ELECTRICAL ANALYSIS PRELIMINARY RESULTS*****

OPEN CIRCUIT VOLTAGE .60
 CELL VOLTAGE AT MAX POWER .50
 SHORT CIRCUIT CURRENT 25.00
 CELL CURRENT AT MAX POWER 23.00
 MAXIMUM CELL POWER 11.50
 CELL EFFICIENCY .115
 FFC .767

NGMAX= 4

BYPASS GROUP NBP= 10.

WILL BE USED IN THE DESIGN UNLESS SOLUTION CANNOT BE OBTAINED.

M	VMPM(M)	NBP(M)	NG(M)	NBG(M)
1	5.	10.	1	10.
2	10.	10.	2	20.
3	15.	10.	3	30.
4	15.	6.	5	30.
5	20.	10.	4	40.
6	20.	8.	5	40.

WHERE:

M = MODULE VOLTAGE NUMBER
 VMPM = MAXIMUM POWER VOLTAGE
 NBP = NUMBER OF SERIES CONNECTED CELLS IN BYPASS GROUP
 NG = NUMBER OF BYPASS GROUPS CONNECTED IN SERIES
 NBG = SERIES CONNECTED CELLS TO GET MODULE VOLTAGE

*****ELECTRICAL ANALYSIS RESULTS*****

RESULTS FOR ELECTRICAL DESIGN OPTION 6 ARE AS FOLLOWS:

---MODULE ELECTRICAL PARAMETERS---

MODULE OPEN CIRCUIT VOLTAGE: 24.00
 MODULE VOLTAGE AT MAXIMUM POWER: 20.00
 MODULE SHORT CIRCUIT CURRENT: 8.51 AMPS
 MODULE CURRENT AT MAXIMUM POWER: 7.83 AMPS
 MAXIMUM MODULE POWER: 156.6 WATTS
 MODULE EFFICIENCY: .108X100
 MODULE FILL FACTOR: .7667
 NUMBER CELLS IN SERIES FORMING
 BYPASS GROUP: 10
 NUMBER OF BYPASS GROUPS IN SERIES: 4
 NUMBER OF BYPASS GROUPS IN PARALLEL: 4
 MAXIMUM REVERSE VOLTAGE OF CELL: -7.005
 FORWARD DIODE VOLTAGE: .700
 PARTIAL OF VOLTAGE WITH RESPECT
 TO TEMPERATURE: -.22E-02
 AMBIENT AIR TEMPERATURE IN DEGREES C: 20.0
 TEMPERATURE WHERE MODULE OUTPUT DOES
 NOT EXCEED VOCMAX FOR SAFETY REASONS: -20.0

OUTPUT (Continued)

---MODULE PHYSICAL PARAMETERS---

PACINGS BETWEEN CELLS IN SERIES:	.15875 CM
SPACINGS BETWEEN CELLS IN PARALLEL:	.15875 CM
SPACING BETWEEN CELLS AND EDGE IN SERIES:	.95250 CM
LENGTH OF MODULE IN SERIES DIRECTION:	120.65000 CM
LENGTH OF MODULE IN PARALLEL DIRECTION:	120.65000 CM
LENGTH OF CELL IN SERIES DIRECTION:	5.78644
LENGTH OF CELL IN PARALLEL DIRECTION:	14.70422
NUMBER OF INTERCONNECT ELECTRICAL CELL RIBS	3
NUMBER OF CELLS IN SERIES DIRECTION	20
NUMBER OF CELLS IN PARALLEL DIRECTION	8
CELL PACKING FRACTION:	.935X100

OUTPUT WITH MODULE LENGTH IN SERIES AND PARALLEL DIRECTIONS SWITCHED:

*****ELECTRICAL ANALYSIS RESULTS***** RESULTS FOR ELECTRICAL DESIGN OPTION 6 ARE AS FOLLOWS:

---MODULE ELECTRICAL PARAMETERS---

MODULE OPEN CIRCUIT VOLTAGE:	24.00
MODULE VOLTAGE AT MAXIMUM POWER:	20.00
MODULE SHORT CIRCUIT CURRENT:	8.51 AMPS
MODULE CURRENT AT MAXIMUM POWER:	7.83 AMPS
MAXIMUM MODULE POWER:	156.6 WATTS
MODULE EFFICIENCY:	.108X100
MODULE FILL FACTOR:	.7667
NUMBER CELLS IN SERIES FORMING BYPASS GRP:	10
NUMBER OF BYPASS GROUPS IN SERIES:	4
NUMBER OF BYPASS GROUPS IN PARALLEL:	4
MAXIMUM REVERSE VOLTAGE OF CELL:	-7.005
FORWARD DIODE VOLTAGE:	.700
PARTIAL OF VOLTAGE WITH RESPECT TO TEMPERATURE:	-.22E-02
AMBIENT AIR TEMPERATURE IN DEGREES C:	20.0
TEMPERATURE WHERE MODULE OUTPUT DOES NOT EXCEED VOCMAX FOR SAFETY REASONS:	-20.0

---MODULE PHYSICAL PARAMETERS---

SPACING BETWEEN CELLS IN SERIES:	.15875 CM
SPACINGS BETWEEN CELLS IN PARALLEL:	.15875 CM
SPACING BETWEEN CELLS AND EDGE IN SERIES:	.95250 CM
LENGTH OF MODULE IN SERIES DIRECTION:	120.65000 CM
LENGTH OF MODULE IN PARALLEL DIRECTION:	120.65000 CM
LENGTH OF CELL IN SERIES DIRECTION:	5.78644 CM
LENGTH OF CELL IN PARALLEL DIRECTION:	14.70422 CM
NUMBER OF INTERCONNECT ELECTRICAL CELL RIBS:	3
NUMBER OF CELLS IN SERIES DIRECTION:	20
NUMBER OF CELLS IN PARALLEL DIRECTION:	8
CELL PACKING FRACTION:	.935X100

6.3.2 Conductor Requirements

This example is illustrated at the end of section 2.3. This particular example shows the questions asked by the input processor for the conductor requirements analysis. It also shows that data may be changed in the data file through the editor. The results of the analysis with the new data then follow.

```
ENTER DO YOU WISH TO RUN THERMAL ANALYSIS?           (Y OR N)  A1
? n
ENTER DO YOU WISH TO RUN ELECTRICAL ANALYSIS?        (Y OR N)  A1
? n
ENTER DO YOU WISH TO RUN STRUCTURAL ANALYSIS?        (Y OR N)  A1
? n
ENTER DO YOU WISH TO RUN ECONOMIC ANALYSIS?          (Y OR N)  A1
? n
ENTER DO YOU WISH TO STUDY CONDUCTOR REQUIREMENTS    (Y OR N)  A1
? y
ENTER MODULE CONDUCTOR RESISTIVITY (OHM-CM) F12.9
EXAMPLE: 0.0000017 OHM-CM
? 0.0000017
ENTER ALLOWABLE FRACTIONAL POWER LOSS DUE TO RESISTANCE
OF CONDUCTOR RUNS (FRACTIONAL PERCENT)
F5.3      EXAMPLE: 1% SHOULD BE ENTERED AS 0.01
? 0.01
ENTER MAXIMUM MODULE POWER (WATTS) F8.2
? 156.8
ENTER NUMBER OF CONDUCTOR SEGMENTS IN THE MODULE
(NUMBER)  I2
? 4
YOU HAVE ENTERED A VALUE OF 4 SEGMENTS.
IS THIS VALUE CORRECT (Y OR N)?
? y
ENTER LENGTH OF CONDUCTOR SEGMENT 1 (CM) F8.2
? 29.6
ENTER CURRENT THROUGH CONDUCTOR SEGMENT 1
(AMPS) F8.2
? 8.5
ENTER LENGTH OF CONDUCTOR SEGMENT 2 (CM) F8.2
? 59.2
```

INPUT (Concluded)

ENTER CURRENT THROUGH CONDUCTOR SEGMENT 2
(AMPS) F8.2
? 6.375
ENTER LENGTH OF CONDUCTOR SEGMENT 3 (CM) F8.2
? 59.2
ENTER CURRENT THROUGH CONDUCTOR SEGMENT 3
(AMPS) F8.2
? 4.25
ENTER LENGTH OF CONDUCTOR SEGMENT 4 (CM) F8.2
? 59.2
2.125
ENTER CURRENT THROUGH CONDUCTOR SEGMENT 4
(AMPS) F8.2
? ENTER TYPE OF CURRENT: CONSTANT OR DISTRIBUTED (C OR D)
CONSTANT MEANS CURRENT IS CONSTANT THROUGHOUT
LENGTH OF CONDUCTOR. DISTRIBUTED MEANS CURRENT INCREASES
LINEARLY THROUGH THE LENGTH OF THE CONDUCTOR. A1
? c
ENTER DO YOU WANT TO COMPUTE MINIMUM ALLOWABLE
CONDUCTOR THICKNESS FROM MAXIMUM CONDUCTOR WIDTH (Y OR N)
? y
ENTER MAXIMUM CONDUCTOR WIDTH (CM) F12.9
? 0.51
ENTER DO YOU WANT TO COMPUTE MINIMUM ALLOWABLE
CONDUCTOR WIDTH FROM MAXIMUM CONDUCTOR THICKNESS (Y OR N)
? y
ENTER MAXIMUM CONDUCTOR THICKNESS (CM) F12.9
? 0.0105
READY

INPUT FILE

xedit, tape4

XEDIT 3.1.00

?? p*

00001

THERMAL, ELECTRICAL, STRUCTURAL, COST, METALIZATION

*****CONDUCTOR REQUIREMENTS INPUTS*****

.000001700

CONDUCTOR RESISTIVITY IN OHM-CM

.010

FRACT. POWER LOSS IN CONDUCTOR ALLOWABLE

156.80

MAXIMUM MODULE POWER

4

NUMBER OF CONDUCTOR SEGMENTS

29.60

LENGTH OF CONDUCTOR SEGMENT 1

8.50

CURRENT THROUGH CONDUCTOR SEGMENT 1

59.20

LENGTH OF CONDUCTOR SEGMENT 2

6.38

CURRENT THROUGH CONDUCTOR SEGMENT 2

59.20

LENGTH OF CONDUCTOR SEGMENT 3

4.25

CURRENT THROUGH CONDUCTOR SEGMENT 3

59.20

LENGTH OF CONDUCTOR SEGMENT 4

2.13

CURRENT THROUGH CONDUCTOR SEGMENT 4

C

TYPE OF CURRENT IN CONDUCTOR

Y

COMPUTE MIN THICKNESS

.510000000

MAXIMUM CONDUCTOR WIDTH

Y

COMPUTE MIN WIDTH

.010500000

MAXIMUM CONDUCTOR THICKNESS

END OF FILE

??

replace, tape 4

READY.
call,pvjcl

READY.
xedit,tape6

XEDIT 3.1.00
?? p*

OUTPUT

*****CONDUCTOR REQUIREMENTS RESULTS*****

MINIMUM ACCEPTABLE CROSS SECTIONAL AREA FOR
THE CONDUCTOR IS .006381706SQ-CM
MAXIMUM CONDUCTOR WIDTH IS SPECIFIED AS .510000000CM
MINIMUM ALLOWABLE CONDUCTOR THICKNESS IS .012513148CM
MAXIMUM CONDUCTOR THICKNESS SPECIFIED AS .010500000CM
MINIMUM ALLOWABLE CONDUCTOR WIDTH IS .607781489CM

END OF FILE

?? e

TAPE6 IS A LOCAL FILE

READY.
xedit,tape4

XEDIT 3.1.00
?? 1/0105/
.010500000 MAXIMUM CONDUCTOR THICKNESS
?? c/0105/0200/
.020000000 MAXIMUM CONDUCTOR THICKNESS
?? e
TAPE4 IS A LOCAL FILE

READY.
replace,tape4

READY.
call,pvjcl

READY.
xedit,tape6

XEDIT 3.1.00
?? p*

*****CONDUCTOR REQUIREMENTS RESULTS*****

MINIMUM ACCEPTABLE CROSS SECTIONAL AREA FOR
THE CONDUCTOR IS .006381706SQ-CM
MAXIMUM CONDUCTOR WIDTH SPECIFIED AS .510000000CM
MINIMUM ALLOWABLE CONDUCTOR THICKNESS IS .012513148CM
MAXIMUM CONDUCTOR THICKNESS SPECIFIED AS .020000000CM
MINIMUM ALLOWABLE CONDUCTOR WIDTH IS .319085282CM

6.3.3 Thermal Example

This thermal analysis run is the two layer example shown in section 3.7. The example problem results may vary slightly from the hand calculations due to round off error.

```
10000          THERMAL, ELECTRICAL, STRUCTURAL, COST, METALIZATION
                *****THERMAL ANALYSIS INPUTS*****
FP             TYPE OF MODULE
SI             PV CELL TYPE
AD             TYPE OF COOLING
2             NUMBER OF NODES (LAYERS)
1             1 ==> GLASS LAYER
Ø             1 ==> UPPER ENCAPSULANT LAYER
1             1 ==> PV CELL LAYER
Ø             1 ==> LOWER ENCAPSULANT LAYER
Ø             1 ==> BACKING LAYER
Ø             1 ==> FRAME
.125           MATERIAL THICKNESS FOR COVER GLASS
0.000          MATERIAL THICKNESS FOR PV CELL
47.5000        11.7500  MODULE LENGTH, WIDTH
11.7500        .2923   THERMAL CELL LENGTH, WIDTH (INSOLATION
                    FOR FRESNEL)
11.0000        .2610   PV CELL LENGTH, WIDTH (CIRC=>WIDTH=DIA*Ø.886)
5.8000         DISTANCE BETWEEN CENTER OF TC AND MOD. EDGE
11.0000        .2600   FRAME LENGTH, WIDTH (APERTURE LENGTH, WIDTH)
500.00         AREA OF BACKING ON HEAT SINK
Ø             NUMBER OF COLLING TUBES PER FOOT
0.00           DIAMETER OF COOLING TUBES
30.0           ARRAY TILT ANGLE FROM HORIZONTAL
.920           EMISSIVITY OF TOP SURFACE
0.000          EMISSIVITY OF BOTTOM SURFACE
.95            GLASS OR LENS OPTICAL EFFICIENCY
100.0          INITIAL TEMPERATURE GUESS FOR TOP LAYER
120.0          INITIAL TEMPERATURE GUESS FOR PV CELL
120.0          INITIAL GUESS FOR BACK SURFACE TEMPERATURE
120.0          REFERENCE TABLE OF PV CELL
200.0          MAXIMUM ALLOWABLE CELL TEMPERATURE
.8000          TRANSMISSIVITY OF COVER GLASS
.0650          ABSORBTIVITY OF COVER GLASS
.5             CONDUCTIVITY OF COVER GLASS
.0200          TRANSMISSIVITY OF PV CELL
.9800          ABSORBTIVITY OF PV CELL
1.0            CONDUCTIVITY OF PV CELL
70.0          AMBIENT AIR TEMPERATURE
0.0           RELATIVE AIR HUMIDITY
1.0           WIND SPEED
0.00          CLOUD COVER
60.00         LATITUDE
.8400         PACKING FRACTION
.1000         CELL EFFICIENCY
END OF FILE
?? -
```


*****FLAT PLATE THERMAL ANALYSIS*****

FULL SUN ON MODULE--NORMAL OPERATING CONDITIONS

NODE1 TEMPERATURE IS 139.2 DEGREES F.

NODE3 TEMPERATURE IS 142.5 DEGREES F.

POWER DISSIPATED DUE TO REVERSE BIAS IS 503.43 W/SQ-M

INSOLATION=1000W/SQ-M CELL EFFICIENCY=0

NODE1 TEMPERATURE IS 142.9 DEGREES F.

NODE3 TEMPERATURE IS 149.8 DEGREES F.

PV CELL IS SHADED ==> INSOLATION=0 CELL EFFICIENCY=0

NODE1 TEMPERATURE IS 118.7 DEGREES F.

NODE3 TEMPERATURE IS 120.7 DEGREES F.

POWER DISSIPATED DUE TO REVERSE BIAS IS 551.80 W/SQ-M

6.3.4 Structural Example

This structural example is worked by hand in section 4.3. The example problem results vary slightly from the manual calculations due to the interpolation of curves such as the stress intensity factor. If, for some reason the module fails, a diagnostic message recommends a solution to remedy the failure.

INPUT FILE

```
001000      THERMAL, ELECTRICAL, STRUCTURAL, COST, METALIZATION
          *****STRUCTURAL ANALYSIS INPUTS*****
    48.0  48.0  .125  MODULE LENGTH, WIDTH, THICKNESS
      .125      GLASS THICKNESS
FP      COLLECTOR TYPE CONC OR FLAT PLATE
    35.0      ARRAY TILT ANGLE FROM HORIZONTAL
      10000000.    YOUNG'S MODULUS OF MODULE
      .220      POISSON'S RATIO
    50.0      DESIGN LOAD
    49.9      WIND LOAD
      1.4      DEADWEIGHT LOAD
N      IS STRESS CYCLE CURVE AVAILABLE?
NO     METAL SUBSTRATE MATERIAL
    4      TYPE OF GLASS
    D      WINDLOAD DURATION UNITS S,M,H,D,W,T,Y
    50     LOAD DURATION IN ABOVE UNITS
Y      DEADWEIGHT LOAD DURATION UNITS
    20     DEADWEIGHT LOAD DURATION IN ABOVE UNITS
    .02    PROBABILITY OF FAILURE (<30%)
```

ANALYSIS OUTPUT

*****STRUCTURAL ANALYSIS*****

RESULTS FOR FLAT PLATE COLLECTOR

STRESS FOR DEADWEIGHT LOAD IS .358E+03 PSI
STRESS FOR THE WIND LOAD IS .470E+04 PSI
BREAKING STRESS DUE TO DEADWEIGHT IS .129E+05 PSI
BREAKING STRESS DUE TO WIND LOAD IS .130E+05 PSI
MAXIMUM COMBINED PRINCIPAL STRESS IS .506E+04 PSI
GLASS THICKNESS ADEQUATE ACCORDING TO ANALYSIS.

TWISTING LOAD ANALYSIS

MODULE PASSES TWISTING TEST.

HAIL IMPACT ANALYSIS

GLASS WILL WITHSTAND HAIL IMPACT.

6.3.5 Economic Analysis Example

This example of a single process was taken from the description of the CARBCOAT process described in section 5.3. The total production costs are for one process in an 18 step manufacturing sequence which when totalled equals \$0.44/wp.

INPUT FILE

```
000100      THERMAL, ELECTRICAL, STRUCTURAL, COST METALIZATION
          *****ECONOMIC ANALYSIS INPUTS*****
1          NUMBER OF MANUFACTURING PROCESSES
.105       PV CELL EFFICIENCY
.976       MODULE PACKING FRACTION
CARBCOAT   PROCESS DESCRIPTION
.950       PROCESS DUTY CYCLE
15.52000   YIELDED PROCESS OUTPUT RATE
.11600     OUTPUT UNIT SIZE IN SQ-METERS
.99990     PROCESS YIELD
10450.0000 EQUIPMENT COST DATA COST( 1)
7          EQUIPMENT LIFETIME FOR PROCESS 1
192.0000   PROCESS FLOOR SPACE FOR PROCESS 1
1598.5700  LABOR FOR PROCESS 1
8.9070     MATERIALS AND SUPPLIES FOR PROCESS 1
.0066      UTILITIES COST FR PROCESS 1
```

ANALYSIS OUTPUT

```
*****ECONOMIC ANALYSIS*****
          PROCESS  CUMULT.  EFFECTIVE  CUMULT.
PROCESS  EQPT  SQFT  DLAB  MATS  UTIL  TOTAL  YIELD  YIELD  COST/SQ-M  COST
CARBCOAT .0066 .0233 .0234 5.9369 .0044 .1274 .9999 1.0000   .127     .127
```

TOTAL PRODUCTION COSTS = .06 \$/PW

6.4 EXAMPLE TEST CASES

The following examples were generated both to exercise the PVMOC program, and to illustrate the format of the input files and output listings. In each case, the input file for a particular run preceeds the output listing., For the electrical examples in design options 1-3, 5 and 6, polycrystalline cell data was used. Amorphous silicon cell data was used for design option 4.

ELECTRICAL

Design option 1

INPUT FILE

```
01000      THERMAL, ELECTRICAL, STRUCTURAL, COST, METALIZATION
          *****ELECTRICAL ANALYSIS INPUTS*****
I          INPUT OR COMPUTE ELECTRICAL PARAMETERS
      .970          OPEN CIRCUIT VOLTAGE
      .833          MAXIMUM CELL VOLTAGE
      25.000        SHORT CIRCUIT CURRENT
      24.000        MAXIMUM CELL CURRENT
      20.000        MAXIMUM POWER
      .824          FILL FACTOR OF PV CELLS ON MODULE
      .2000         CELL EFFICIENCY
     100.000        INSOLATION
2          NUMBER OF OUTPUT VOLTAGES
      5.0          VOLTAGE VMPM( 1)
     10.0          VOLTAGE VMPM( 2)
     25.0          CELL TEMPERATURE
    100.00         MAXIMUM CELL TEMPERATURE
     25.0          MAXIMUM CELL AREA
     20.0          AMBIENT AIR TEMPERATURE
N          DO YOU WISH TO COMPUTE POWER DISSIPATED?
     -6.7          MAXIMUM REVERSE CELL VOLTAGE
      .7          FORWARD DIODE VOLTAGE
    -0.0032000     PARTIAL OF VOLTAGE WITH RESPECT TO TEMPERATURE
    -20.00         LOWEST TEMP WHERE MOD. OUTPUT   VOCMAX
      2          NUMBER OF INTERCONNECT RIBS ON CELL
     30.00         MAXIMUM OC VOLTAGE AT TL
    -10.0          BREAKDOWN VOLTAGE (< 0.0)
1          DESIGN OPTION NUMBER 1,2,3,4,5,OR 6
      .20000       SPACING BETWEEN CELL IN SERIES DIRECTION
      .20000       SPACING BETWEEN CELLS IN PARALLEL DIRECTION
     1.00000       DIST BETW. CELL & FRAME EDGE IN SERIES
     1.00000       DIST BETW. CELL & FRAME EDGE IN PARALLEL
    143.40000      LENGTH OF MOD IN SERIES DIRECTION
     10.40000      LENGTH OF MOD IN PARALLEL DIRECTION
```

OUTPUT FILE

*****ELECTRICAL ANALYSIS PRELIMINARY RESULTS*****

OPEN CIRCUIT VOLTAGE .97
 CELL VOLTAGE AT MAX POWER .83
 SHORT CIRCUIT CURRENT 25.00
 CELL CURRENT AT MAX POWER 24.00
 MAXIMUM CELL POWER 20.00
 CELL EFFICIENCY .200
 FFC .824

NGMAX= 2

BYPASS GROUP NBP= 6.

WILL BE USED IN THE DESIGN UNLESS SOLUTION CANNOT BE OBTAINED.

M	VMPM(M)	NBP(M)	NG(M)	NBG(M)
1	5.	6.	1	6.
2	10.	6.	2	12.
3	10.	4.	3	12.

WHERE:

M = MODULE VOLTAGE NUMBER
 VMPM = MAXIMUM POWER VOLTAGE
 NBP = NUMBER OF SERIES CONNECTED CELLS IN BYPASS GRP
 NG = NUMBER OF BYPASS GROUPS CONNECTED IN SERIES
 NBG = SERIES CONNECTED CELLS TO GET MODULE VOLTAGE

*****ELECTRICAL ANALYSIS RESULTS*****

RESULTS FOR ELECTRICAL DESIGN OPTION 1 ARE AS FOLLOWS:

---MODULE ELECTRICAL PARAMETERS---

MODULE OPEN CIRCUIT VOLTAGE:	11.64
MODULE VOLTAGE AT MAXIMUM POWER:	10.00
MODULE SHORT CIRCUIT CURRENT:	.63 AMPS
MODULE CURRENT AT MAXIMUM POWER:	.60 AMPS
MAXIMUM MODULE POWER:	6.0 WATTS
MODULE EFFICIENCY:	.136X100
MODULE FILL FACTOR:	.8244
NUMBER CELLS IN SERIES FORMING BYPASS GROUP	6
NUMBER OF BYPASS GROUPS IN SERIES	2
NUMBER OF BYPASS GROUPS IN PARALLEL	1
MAXIMUM REVERSE VOLTAGE OF CELL:	-6.700
FORWARD DIODE VOLTAGE:	.700
PARTIAL OF VOLTAGE WITH RESP. TO TMPRTRE:	-.32E-02
AMBIENT AIR TEMPERATURE IN DEGREES C:	20.0
TEMPERATURE WHERE MODULE OUTPUT DOES NOT EXCEED VOCMAX FOR SAFETY REASONS:	-20.0

OUTPUT FILE (Continued)

---MODULE PHYSICAL PARAMETERS---

SPACINGS BETWEEN CELLS IN SERIES:	.20000 CM
SPACINGS BETWEEN CELLS IN PARALLEL:	.20000 CM
SPACINGS BETWEEN CELLS AND EDGE IN SERIES:	1.00000 CM
LENGTH OF MODULE IN SERIES DIRECTION:	142.20000 CM
LENGTH OF MODULE IN PARALLEL DIRECTION:	7.00000 CM
LENGTH OF CELL IN SERIES DIRECTION:	5.00000 CM
LENGTH OF CELL IN PARALLEL DIRECTION:	5.00000 CM
NUMBER OF INTERCONNECT ELECT. CELL RIBS	2
NUMBER OF CELLS IN SERIES DIRECTION:	27
NUMBER OF CELLS IN PARALLEL DIRECTION:	1
CELL PACKING FRACTION:	.678X100

Design Option 2 (Note: The input processor questions and answers for this run have been included as an example.)

INPUT PROCESSOR SESSION

THIS IS THE INPUT PRE-PROCESSOR FOR THE PVMOC PROGRAM. IT GENERATES THE INPUT FILE TAPE4 WHICH CONTAINS ALL NEEDED INPUTS FOR RUNNING ANY OR ALL OF THE FOLLOWING ANALYSES: THERMAL, ELECTRICAL, STRUCTURAL, AND ECONOMIC.

IT MAY BE NECESSARY TO CONSULT MATERIALS MANUALS FOR CERTAIN PHYSICAL PROPERTIES OF MODULE MATERIALS. FOR THE USER'S CONVENIENCE, HOWEVER, SOME DEFAULT VALUES ARE GIVEN.

THE USER WILL BE PROMPTED WITH A DESCRIPTION OF WHATEVER IS SUPPOSED TO BE ENTERED, THE UNITS OR OPTIONS, AND THE CORRECT INPUT FORMATS. INTEGERS MUST BE LEFT JUSTIFIED! IF NOT, A 3 COULD BE READ AS 300!

```
ENTER DO YOU WISH TO RUN THERMAL ANALYSIS?          (Y OR N)  A1
? n
ENTER DO YOU WISH TO RUN ELECTRICAL ANALYSIS?        (Y OR N)  A1
? y
ENTER DO YOU WISH TO RUN STRUCTURAL ANALYSIS?        (Y OR N)  A1
? n
ENTER DO YOU WISH TO RUN ECONOMIC ANALYSIS?          (Y OR N)  A1
? n
ENTER DO YOU WISH TO STUDY CONDUCTOR REQUIREMENTS    (Y OR N)  A1
? n
```

*****ELECTRICAL ANALYSIS INPUTS*****

```
ENTER INPUT OR COMPUTE ELECTRICAL PARAMETERS        (I OR C)  A1
? i
ENTER OPEN CIRCUIT VOLTAGE                          (VOLTS)    F8.3
? 0.97
ENTER MAXIMUM CELL VOLTAGE                          (VOLTS)    F8.3
? 0.833
ENTER SHORT CIRCUIT CURRENT DENSITY                 (MA/SQ CM)  F8.3
? 25.0
ENTER CELL CURRENT AT MAXIMUM POWER                 (MA/SQ CM)  F8.3
? 24.0
ENTER MAXIMUM POWER                                 (MW/SQ CM)  F8.3
? 20.0
ENTER FILL FACTOR OF PV CELLS IN MODULE (DECIMAL PERCENT)  F8.3
? 0.824
ENTER CELL EFFICIENCY                               (DECIMAL PERCENT)  F6.4
? 0.2
ENTER INSOLATION                                     (MW/SQ CM)  F8.3
@ ? 100.  100 MW/SQ-CM FOR DEFAULT.
ENTER NUMBER OF OUTPUT VOLTAGES                     (INTEGER)   12
? 2
YOU HAVE 20 OUTPUT VOLTAGES. IS THAT CORRECT?
ANSWER Y OR N.
? n
ENTER NUMBER OF OUTPUT VOLTAGES                     (INTEGER)   12
? 2
```


INPUT (Continued)

YOU HAVE 2 OUTPUT VOLTAGES. IS THAT CORRECT?
ANSWER Y OR N.

? y
ENTER VOLTAGE (1) (VOLTS) NNNN.N F 6.1

?
ENTER VOLTAGE (1) (VOLTS) NNNN.N F 6.1

? 5.
ENTER VOLTAGE (2) (VOLTS) NNNN.N F 6.1

? 10.
ENTER CELL TEMPERATURE (DEGREES C) F6.1

? 25.
ENTER MAXIMUM CELL TEMPERATURE (DEGREES C) F6.1

? 212
ENTER MAXIMUM CELL AREA (SQ-CM) F6.1

? 25.
ENTER AMBIENT AIR TEMPERATURE (DEGREES C) F6.1

? 20.
ENTER DO YOU WISH TO COMPUTE POWER DISSIPATED? (Y OR N) A1

? y
ENTER DELTA T/DELTA S (DEG C/SQCM) F12.7

? -0.0032
ENTER DELTA T/DELTA P (DEG C/MW) F12.7

? 0.
ENTER FORWARD DIODE VOLTAGE (VOLTS) F6.1

? 0.7
ENTER PARTIAL OF VOLTAGE WITH RESPECT TO TEMP. (V/DEG C) F12.7

? -0.0032
ENTER LOWEST TEMP WHERE MOD. OUTPUT < VOCMAX (DEGREES C) F6.1

? -20.
ENTER NUMBER OF INTERCONNECT RIBS ON CELL (INTEGER) I3

? 24
ENTER MAXIMUM OC VOLTAGE AT LOWEST TEMP AT WHICH MODULE OUTPUT
MAXIMUM OPEN CIRCUIT VOLTAGE (VOLTS) F6.1

? 30.
ENTER BREAKDOWN VOLTAGE (0.0 ==> NEGATIVE) (VOLTS) F6.1

? -10.
ENTER DESIGN OPTION NUMBER 1,2,3,4,5,OR 6 (INTEGER) I1

DESIGN OPTIONS AS FOLLOWS:

- 1- MAXIMUM CELL AREA AND MAXIMUM MODULE DIMENSIONS
- 2- NUMBER AND DIMENSION OF CELLS
- 3- FIXED CELL AND MAXIMUM MODULE DIMENSIONS
- 4- MAXIMUM CELL WIDTH AND AREA FIXED MODULE DIMENSIONS
- 5- MAXIMUM CELL AREA AND FIXED MODULE DIMENSIONS
- 6- MAXIMUM CELL DIMENSIONS AND FIXED MODULE DIMENSIONS

? 2
ENTER SPACING BETWEEN CELL IN SERIES DIRECTION (CM) F9.5

? 0.2
ENTER SPACING BETW. CELLS IN PARALLEL DIRECTION(CM) F9.5

? 0.2

INPUT (Continued)

```

ENTER DIST BETW CELL & FRAME EDGE IN SERIES      (CM)   F9.5
? 1.0
ENTER DIST BETW CELL & FRAME EDGE IN PARALLEL    (CM)   F9.5
? 1.0
ENTER NUMBER OF CELLS IN MODULE                    (INTEGER) I3
? 24
ENTER LENGTH OF CELL IN SERIES DIRECTION          (CM)   F9.5
? 5.0
ENTER LENGTH OF CELL IN PARALLEL DIRECTION        (CM)   F9.5
? 10.0
READY.
xedit,tape4
XEDIT 3.1.00
?? p*
```

Design Option 2

INPUT FILE

```

01000      THERMAL, ELECTRICAL, STRUCTURAL, COST METALIZATION
          *****ELECTRICAL ANALYSIS INPUTS*****
I          INPUT OR COMPUTE ELECTRICAL PARAMETERS
          .970      OPEN CIRCUIT VOLTAGE
          .833      MAXIMUM CELL VOLTAGE
          25.000     SHORT CIRCUIT CURRENT
          24.000     MAXIMUM CELL CURRENT
          20.000     MAXIMUM POWER
          .824      FILL FACTOR OF PV CELLS ON MODULE
          .2000     CELL EFFICIENCY
          100.000    INSOLATION
          2          NUMBER OF OUTPUT VOLTAGES
          5.0       VOLTAGE VMPM( 1)
          10.0      VOLTAGE VMPM( 2)
          25.0      CELL TEMPERATURE
          100.0     MAXIMUM CELL TEMPERATURE
          25.0      MAXIMUM CELL AREA
          20.0      AMBIENT AIR TEMPERATURE
N          DO YOU WISH TO COMPUTE POWER DISSIPATED?
          -6.700000  VRTMAX
          .7         FORWARD DIODE VOLTAGE
          -.0032000  PARTIAL OF VOLTAGE WITH RESPECT TO TEMP.
          -20.0      LOWEST TEMP WHERE MOD. OUTPUT < VOCMAX
          2          NUMBER OF INTERCONNECT RIBS ON CELL
          30.0       MAXIMUM OC VOLTAGE AT TL
          -10.0      BREAKDOWN VOLTAGE (< 0.0)
          2          DESIGN OPTION NUMBER 1,2,3,4,5,OR 6
          .20000     SPACING BETWEEN CELL IN SERIES DIRECTION
          .20000     SPACING BETWEEN CELLS IN PARALLEL DIRECTION
          1.00000     DIST BETW CELL & FRAME EDGE IN SERIES
          1.00000     DIST BETW CELL & FRAME EDGE IN PARALLEL
          24         NUMBER OF CELLS
          5.00000     LENGTH OF CELL IN SERIES DIRECTION
          10.00000    LENGTH OF CELL IN PARALLEL DIRECTION
```

Design Option 3

Output Listing

*****ELECTRICAL ANALYSIS PRELIMINARY RESULTS*****

OPEN CIRCUIT VOLTAGE .97
 CELL VOLTAGE AT MAX POWER .83
 SHORT CIRCUIT CURRENT 25.00
 CELL CURRENT AT MAX POWER 24.00
 MAXIMUM CELL POWER 20.00
 CELL EFFICIENCY .200
 FFC .824

NGMAX= 2

BYPASS GROUP NBP= 6.

WILL BE USED IN THE DESIGN UNLESS SOLUTION CANNOT BE OBTAINED.

M	VMPM(M)	NBP(M)	NG(M)	NBG(M)
1	5.	6.	1	6.
2	10.	6.	2	12.
3	10.	4.	3	12.

WHERE:

M = MODULE VOLTAGE NUMBER
 VMPM = MAXIMUM POWER VOLTAGE
 NBP = NUMBER OF SERIES CONNECTED CELLS IN BYPASS GRP
 NG = NUMBER OF BYPASS GROUPS CONNECTED IN SERIES
 NBG = SERIES CONNECTED CELLS TO GET MODULE VOLTAGE

M	XMLSS(M)	XMLPP(M)	PFI(M)	XNM(M)
1	71.4	21.4	.8	1.0
2	143.4	10.4	.8	1.0

WHERE:

M = NUMBER OF SERIES CONNECTED BYPASS GROUPS
 XMLSS= LENGTH OF MODULE IN SERIES DIRECTION FOR M
 XMLPP= LENGTH OF MODULE IN PARALLEL DIRECTION FOR M
 PFI = MODULE PACKING FRACTION FOR M BYPASS GROUPS
 XNM = MINIMUM NUMBER OF CELLS IN PARALLEL TO INSURE REDUNDANCY

INPUT (Continued)

OUTPUT LISTING (Continued)

*****ELECTRICAL ANALYSIS RESULTS*****

RESULTS FOR ELECTRICAL DESIGN OPTION 2 ARE AS FOLLOWS:

---MODULE ELECTRICAL PARAMETERS---

MODULE OPEN CIRCUIT VOLTAGE:	11.64
MODULE VOLTAGE AT MAXIMUM POWER:	10.00
MODULE SHORT CIRCUIT CURRENT:	2.50 AMPS
MODULE CURRENT AT MAXIMUM POWER:	2.40 AMPS
MAXIMUM MODULE POWER:	24.0 WATTS
MODULE EFFICIENCY:	.161X100
MODULE FILL FACTOR:	.8244
NUMBER CELLS IN SERIES FORMING BYPASS GRP:	6
NUMBER OF BYPASS GROUPS IN SERIES:	2
NUMBER OF BYPASS GROUPS IN PARALLEL:	2
MAXIMUM REVERSE VOLTAGE OF CELL:	-6.700
FORWARD DIODE VOLTAGE:	.700
PARTIAL OF VOLTAGE WITH RESP. TO TMPRTURE:	-.32E-02
AMBIENT AIR TEMPERATURE IN DEGREES C:	20.0
TEMPERATURE WHERE MODULE OUTPUT DOES NOT EXCEED VOCMAX FOR SAFETY REASONS:	-20.0

---MODULE PHYSICAL PARAMETERS---

SPACINGS BETWEEN CELLS IN SERIES:	.20000 CM
SPACINGS BETWEEN CELLS AND EDGE IN SERIES:	1.00000 CM
LENGTH OF MODULE IN SERIES DIRECTION:	143.40000 CM
LENGTH OF MODULE IN PARALLEL DIRECTION:	10.40000 CM
LENGTH OF CELL IN SERIES DIRECTION:	5.00000 CM
LENGTH OF CELL IN PARALLEL DIRECTION:	10.00000 CM
NUMBER OF INTERCONNECT ELECT. CELL RIBS	2
NUMBER OF CELLS IN SERIES DIRECTION:	24
NUMBER OF CELLS IN PARALELL DIRECTION:	1
CELL PACKING FRACTION:	.805X100

Design Option 3

```

                                INPUT FILE
0100      THERMAL, ELECTRICAL, STRUCTURAL, COST, METALIZATION
          *****ELECTRICAL ANALYSIS INPUTS*****
I          INPUT OR COMPUTE ELECTRICAL PARAMETERS
          .970      OPEN CIRCUIT VOLTAGE
          .820      MAXIMUM CELL VOLTAGE
          25.000     SHORT CIRCUIT CURRENT
          24.000     MAXIMUM CELL CURRENT
          20.000     MAXIMUM POWER
          .935      FILL FACTOR OF PV CELLS ON MODULE
          .1500     CELL EFFICIENCY
          100.00    INSOLATION
2          NUMBER OF OUTPUT VOLTAGES
          5.0      VOLTAGE VMPM( 1)
          10.0     VOLTAGE VMPM( 2)
          25.0     CELL TEMPERATURE
          100.0    MAXIMUM CELL TEMPERATURE
          25.0     MAXIMUM CELL AREA
          20.0     AMBIENT AIR TEMPERATURE
N          DO YOU WISH TO COMPUTE POWER DISSIPATED?
          -6.7     MAXIMUM REVERSE CELL VOLTAGE
          .7       FORWARD DIODE VOLTAGE
          -.0032000 PARTIAL OF VOLTAGE WITH RESPECT TO TEMP.
          -20.0    LOWEST TEMP WHERE MOD. OUTPUT < VOCMAX
1          NUMBER OF INTERCONNECT RIBS ON CELL
          30.0     MAXIMUM OC VOLTAGE AT TL
          -10.0    BREAKDOWN VOLTAGE (< 0.0)
3          DESIGN OPTION NUMBER 1,2,3,4,5,OR 6
          .20000   SPACING BETWEEN CELL IN SERIES DIRECTION
          .20000   SPACING BETWEEN CELLS IN PARALLEL DIRECTION
          1.00000   DIST BETW CELL & FRAME EDGE IN SERIES
          1.00000   DIST BETW CELL & FRAME EDGE IN PARALLEL
          5.00000   LENGTH OF CELL IN SERIES DIRECTION
          10.00000  LENGTH OF CELL IN PARALLEL DIRECTION
          143.40000 LENGTH OF MOD IN SERIES DIRECTION
          10.40000  LENGTH OF MOD IN PARALLEL DIRECTION

```

Design Option 3

Output Listing

*****ELECTRICAL ANALYSIS PRELIMINARY RESULTS*****

OPEN CIRCUIT VOLTAGE .97
 CELL VOLTAGE AT MAX POWER .82
 SHORT CIRCUIT CURRENT 25.00
 CELL CURRENT AT MAX POWER 24.00
 MAXIMUM CELL POWER 20.00
 CELL EFFICIENCY .150
 FFC .935

NGMAX= 2

BYPASS GROUP NBP= 6.

WILL BE USED IN THE DESIGN UNLESS SOLUTION CANNOT BE OBTAINED.

M	VMPM(M)	NBP(M)	NG(M)	NBG(M)
1	5.	6.	1	6.
2	10.	6.	2	12.
3	10.	4.	3	12.

WHERE:

M = MODULE VOLTAGE POWER
 VMPM = MAXIMUM POWER VOLTAGE
 NBP = NUMBER OF SERIES CONNECTED CELLS IN BYPASS GRP
 NG = NUMBER OF BYPASS GROUPS CONNECTED IN SERIES
 NBG = SERIES CONNECTED CELLS TO GET MODULE VOLTAGE

*****ELECTRICAL ANALYSIS RESULTS*****

RESULTS FOR ELECTRICAL DESIGN OPTION 3 ARE AS FOLLOWS:

---MODULE ELECTRICAL PARAMETERS---

MODULE OPEN CIRCUIT VOLTAGE:	11.64
MODULE VOLTAGE AT MAXIMUM POWER:	9.84
MODULE SHORT CIRCUIT CURRENT:	1.25 AMPS
MODULE CURRENT AT MAXIMUM POWER:	1.20 AMPS
MAXIMUM MODULE POWER:	11.8 WATTS
MODULE EFFICIENCY:	.119X100
MODULE FILL FACTOR:	.8115
NUMBER CELLS IN SERIES FORMING BYPASS GROUP	6
NUMBER OF BYPASS GROUPS IN SERIES:	2
NUMBER OF BYPASS GROUPS IN PARALLEL	1
MAXIMUM REVERSE VOLTAGE OF CELL:	-6.700
FORWARD DIODE VOLTAGE:	.700
PARTIAL OF VOLTAGE WITH RESPECT TO TEMPERATURE	-.32E-02
AMBIENT AIR TEMPERATURE IN DEGREES C:	20.0
TEMPERATURE WHERE MODULE OUTPUT DOES NOT EXCEED VOCMAX FOR SAFETY REASONS:	-20.0

OUTPUT LISTING (Continued)

---MODULE PHYSICAL PARAMETERS---

SPACINGS BETWEEN CELLS IN SERIES:	.20000 CM
SPACINGS BETWEEN CELLS IN PARALLEL:	.20000 CM
SPACING BETWEEN CELLS AND EDGE IN SERIES:	1.00000 CM
LENGTH OF MODULE IN SERIES DIRECTION:	142.20000 CM
LENGTH OF MODULE IN PARALLEL DIRECTION:	12.00000 CM
LENGTH OF CELL IN SERIES DIRECTION:	5.00000 CM
LENGTH OF CELL IN PARALLEL DIRECTION:	10.00000 CM
NUMBER OF INTERCONNECT ELECT. CELL RIBS	1
NUMBER OF CELLS IN SERIES DIRECTION:	27
NUMBER OF CELLS IN PARALLEL DIRECTION:	1
CELL PACKING FRACTION:	.791X100

Design Option 4

INPUT FILE

```

01000      THERMAL, ELECTRICAL, STRUCTURAL, COST METALIZATION
          *****ELECTRICAL ANALYSIS INPUTS*****
I      INPUT OR COMPUTE ELECTRICAL PARAMETERS
      .91      OPEN CIRCUIT VOLTAGE
      .714     MAXIMUM CELL VOLTAGE
      16.0     SHORT CIRCUIT CURRENT
      14.0     MAXIMUM CELL CURRENT
      10.0     MAXIMUM POWER
      .687     FILL FACTOR OF PV CELLS ON MODULE
      .1000    CELL EFFICIENCY
      100.0    INSULATION
2      NUMBER OF OUTPUT VOLTAGES
      5.0      VOLTAGE VMPM( 1)
      10.0     VOLTAGE VMPM( 1)
      25.0     CELL TEMPERATURE
      100.0    MAXIMUM CELL TEMPERATURE
      25.0     MAXIMUM CELL AREA
      20.0     AMBIENT AIR TEMPERATURE
N      DO YOU WISH TO COMPUTE POWER DISSIPATED?
      -6.7     MAXIMUM REVERSE CELL VOLTAGE
      .7       FORWARD DIODE VOLTAGE
      -.0016000 PARTIAL OF VOLTAGE WITH RESPECT TO TEMP.
      -20.0    LOWEST TEMP WHERE MOD. OUTPUT < VOCMAX
1      NUMBER OF INTERCONNECT RIBS ON CELL
      30.0     MAXIMUM OC VOLTAGE AT TL
      -10.0    BREAKDOWN VOLTAGE (< 0.0)
4      DESIGN OPTION NUMBER 1,2,3,4,5,OR 6
      .31800   SPACING BETWEEN CELL IN SERIES DIRECTION
      .07900   SPACING BETWEEN CELLS IN PARALLEL DIRECTION
      .95300   DIST BETW CELL & FRAME EDGE IN SERIES
      .95300   DIST BETW CELL & FRAME EDGE IN PARALLEL
      29.85000 LENGTH OF MOD IN SERIES DIRECTION
      120.65000 LENGTH OF MOD IN PARALLEL DIRECTION
      .31800   SPACING BET 2 NEG ENDS OF 2 BP GRPS SERIES
      .63500   SPCNG BET 2 POS ENDS OF 2 BP GRPS PARALLEL
      .47600   SPCNG BET A NEG AND POS BP GRP IN SERIES
      .50      FRACTIONAL LOWER LIMIT ON XLCS
      .05      FRACTIONAL POWER LOSS
      1.       SHEET RESISTIVITY

```


OUTPUT LISTING

*****ELECTRICAL ANALYSIS PRELIMINARY RESULTS*****

OPEN CIRCUIT VOLTAGE	.91
CELL VOLTAGE AT MAX POWER	.71
SHORT CIRCUIT CURRENT	16.00
CELL CURRENT AT MAX POWER	14.00
MAXIMUM CELL POWER	10.00
CELL EFFICIENCY	.100
FFC	.687

NGMAX= 2

BYPASS GROUP NBP= 7.

WILL BE USED IN THE DESIGN UNLESS SOLUTION CANNOT BE OBTAINED.

M	VMPM(M)	NBP(M)	NG(M)	NBG(M)
1	5.	7.	1	7.
2	10.	7.	2	14.

WHERE:

M = MODULE VOLTAGE NUMBER
 VMPM = MAXIMUM POWER VOLTAGE
 NBP = NUMBER OF SERIES CONNECTED CELLS IN BYPASS GRP
 NG = NUMBER OF BYPASS GROUP CONNECTED IN SERIES
 NBG = SERIES CONNECTED CELLS TO GET MODULE VOLTAGE

*****ELECTRICAL ANALYSIS RESULTS*****

RESULTS FOR ELECTRICAL DESIGN OPTION 4 ARE AS FOLLOWS:

---MODULE ELECTRICAL PARAMETERS---

MODULE OPEN CIRCUIT VOLTAGE:	12.74
MODULE VOLTAGE AT MAXIMUM POWER:	10.00
MODULE SHORT CIRCUIT CURRENT:	3.71 AMPS
MODULE CURRENT AT MAXIMUM POWER:	3.24 AMPS
MAXIMUM MODULE POWER:	32.4 WATTS
MODULE EFFICIENCY:	.090X100
MODULE FILL FACTOR:	.6865
NUMBER OF CELLS IN SERIES FORMING BYPASS GROUP:	7
NUMBER OF BYPASS GROUPS IN SERIES:	2
NUMBER OF BYPASS GROUPS IN PARALLEL:	10
MAXIMUM REVERSE VOLTAGE OF CELL:	-6.700
FORWARD DIODE VOLTAGE:	.700
PARTIAL OF VOLTAGE WITH RESP. TO TMPRTURE:	-.16E-02
AMBIENT AIR TEMPERATURE IN DEGREES C:	20.0
TEMPERATURE WHERE MODULE OUTPUT DOES NOT EXCEED VOCMAX FOR SAFETY REASONS:	-20.0

OUTPUT (Continued)

---MODULE PHYSICAL PARAMETERS---

SPACINGS BETWEEN CELLS IN SERIES:	.31800 CM
SPACINGS BETWEEN CELLS IN PARALLEL:	.07900 CM
SPACING BETWEEN CELLS AND EDGE IN SERIES:	.95300 CM
LENGTH OF MODULE IN SERIES DIRECTION:	29.85000 CM
LENGTH OF MODULE IN PARALLEL DIRECTION:	120.65000 CM
LENGTH OF CELL IN SERIES DIRECTION:	1.96200 CM
LENGTH OF CELL IN PARALLEL DIRECTION:	11.80330 CM
NUMBER OF INTERCONNECT ELECT. CELL RIBS:	1
NUMBER OF CELLS IN SERIES DIRECTION:	14
NUMBER OF CELLS IN PARALLEL DIRECTION:	10
CELL PACKING FRACTION:	.900X100

Design Option 5

```

                                INPUT FILE
01000      THERMAL, ELECTRICAL, STRUCTURAL, COST METALIZATION
                                *****ELECTRICAL ANALYSIS INPUTS*****
C          INPUT OR COMPUTE ELECTRICAL PARAMETERS
5          NUMBER OF POINTS ON I VS V CURVE
    0.00      25.00      V( 1) ,J( 1)
    .45      24.10      V( 2) ,J( 2)
    .50      23.00      V( 3) ,J( 3)
    .55      17.30      V( 4) ,J( 4)
    .60      0.00      V( 5) ,J( 5)
100.000      INSOLATION
4          NUMBER OF OUTPUT VOLTAGES
    5.0      VOLTAGE VMPM( 1)
   10.0      VOLTAGE VMPM( 2)
   15.0      VOLTAGE VMPM( 3)
   20.0      VOLTAGE VMPM( 4)
   25.0      CELL TEMPERATURE
   96.0      MAXIMUM CELL AREA
   20.0      AMBIENT AIR TEMPERATURE
Y          DO YOU WISH TO COMPUTE POWER DISSIPATED?
100.0      MAXIMUM CELL TEMPERATURE
    .0035000      DELTA T/DELTA S
    .0030000      DELTA T/DELTA P
    .7          FORWARD DIODE VOLTAGE
   -0.0022000      PARTIAL OF VOLTAGE WITH RESPECT TO TEMP.
  -20.0      LOWEST ANTICIPATED CELL TEMPERATURE
    3          NUMBER OF INTERCONNECT RIBS ON CELL
   30.0      MAXIMUM OC VOLTAGE AT TL
  -10.0      BREAKDOWN VOLTAGE (< 0.0)
5          DESIGN OPTION NUMBER 1,2,3,4,5,OR 6
    .15785      SPACING BETWEEN CELL IN SERIES DIRECTION
    .15785      SPACING BETWEEN CELLS IN PARALLEL DIRECTION
    .95250      DIST BETW CELL & FRAME EDGE IN SERIES
    .95250      DIST BETW CELL & FRAME EDGE IN PARALLEL
  120.65000      LENGTH OF MOD IN SERIES DIRECTION
  120.65000      LENGTH OF MOD IN PARALLEL DIRECTION

```

OUTPUT LISTING

*****ELECTRICAL ANALYSIS PRELIMINARY RESULTS*****

OPEN CIRCUIT VOLTAGE .60
 CELL VOLTAGE AT MAX POWER .50
 SHORT CIRCUIT CURRENT 24.00
 CELL CURRENT AT MAX POWER 23.00
 MAXIMUM CELL POWER 11.50
 CELL EFFICIENCY .115
 FFC .767

NGMAX= 4

BYPASS GROUP NBP= 10.

WILL BE USED IN THE DESIGN UNLESS SOLUTION CANNOT BE OBTAINED.

M	VMPM(M)	NBP(M)	NG(M)	NBG(M)
1	5.	10.	1	10.
2	10.	10.	2	20.
3	15.	10.	3	30.
4	15.	6.	5	30.
5	20.	10.	4	40.
6	20.	8.	5	40.

WHERE:

M = MODULE VOLTAGE NUMBER
 VMPM = MAXIMUM POWER VOLTAGE
 NBP = NUMBER OF SERIES CONNECTED CELLS IN BYPASS GRP
 NG = NUMBER OF BYPASS GROUPS CONNECTED IN SERIES
 NBG = SERIES CONNECTED CELLS TO GET MODULE VOLTAGE

*****ELECTRICAL ANALYSIS RESULTS*****

RESULTS FOR ELECTRICAL OPTION 5 ARE AS FOLLOWS:

---MODULE ELECTRICAL PARAMETERS---

MODULE OPEN CIRCUIT VOLTAGE: 18.00
 MODULE VOLTAGE AT MAXIMUM POWER: 15.00
 MODULE SHORT CIRCUIT CURRENT: .32 AMPS
 MODULE CURRENT AT MAXIMUM POWER: .30 AMPS
 MAXIMUM MODULE POWER: 4.5 WATTS
 MODULE EFFICIENCY: .038X100
 MODULE FILL FACTOR: .7667
 NUMBER OF CELLS IN SERIES FORMING BYPASS GRP: 6
 NUMBER OF BYPASS GROUPS IN SERIES: 5
 NUMBER OF BYPASS GROUPS IN PARALLEL: 12
 MAXIMUM REVERSE VOLTAGE OF CELL: -7.005
 FORWARD DIODE VOLTAGE: .700
 PARTIAL OF VOLTAGE WITH RESP. TO TMPRTURE: -.22E-02
 AMBIENT AIR TEMPERATURE IN DEGREES C: 20.0
 TEMPERATURE WHERE MODULE DOES NOT
 EXCEED VOCMAX FOR SAFETY REASONS: -20.0

OUTPUT (Continued)

---MODULE PHYSICAL PARAMETERS---

SPACINGS BETWEEN CELLS IN SERIES:	.15785 CM
SPACINGS BETWEEN CELLS IN PARALLEL:	.15785 CM
SPACING BETWEEN CELLS AND EDGE IN SERIES:	.95250 CM
LENGTH OF MODULE IN SERIES DIRECTION:	9.79796 CM
LENGTH OF MODULE IN PARALLEL DIRECTION:	299.00428 CM
LENGTH OF CELL IN SERIES DIRECTION:	.11050 CM
LENGTH OF CELL IN PARALLEL DIRECTION:	9.75072 CM
NUMBER OF INTERCONNECT ELECT. CELL RIBS:	3
NUMBER OF CELLS IN SERIES DIRECTION:	30
NUMBER OF CELLS IN PARALLEL DIRECTION:	30
CELL PACKING FRACTION:	.331X100
END OF FILE	

THERMAL

Three layer flat plate.

INPUT FILE

```

10000      THERMAL, ELECTRICAL, STRUCTURAL, COST, METALIZATION
          *****THERMAL ANALYSIS INPUTS*****
FP          TYPE OF MODULE
SI          PV CELL TYPE
AD          TYPE OF COOLING
3          NUMBER OF NODES (LAYERS)
1          1 ==> GLASS LAYER
0          1 ==> UPPER ENCAPSULANT LAYER
1          1 ==> PV CELL LAYER
0          1 ==> LOWER ENCAPSULANT LAYER
1          1 ==> BACKING LAYER
0          1 ==> FRAME
.125        MATERIAL THICKNESS FOR COVER GLASS
0.000        MATERIAL THICKNESS FOR PV CELL
.083        MATERIAL THICKNESS FOR BACKING MATERIAL
47.5000     11.7500  MODULE LENGTH, WIDTH
11.7500     .2923   THERMAL CELL LENGTH,WIDTH (INSOLATION
                  FOR FRESNEL)
11.0000     .2610   PV CELL LENGTH, WIDTH (CIRC=> WIDTH=DIA*0.0886
5.8000      DISTANCE BETWEEN CENTER OF TC AND MOD. EDGE
11.0000     .2600   FRAME LENGTH, WIDTH (APERTURE LENGTH, WIDTH)
568.00      AREA OF BACKING ON HEAT SINK
0          NUMBER OF COOLING TUBES PER FOOT
0.00        DIAMETER OF COOLING TUBES
30.0        ARRAY TILT ANGLE FROM HORIZONTAL
.920        EMISSIVITY OF TOP SURFACE
.040        EMISSIVITY OF BOTTOM SURFACE
.80         GLASS OR LENS OPTICAL EFFICIENCY
120.0       INITIAL TEMPERATURE GUESS FOR TOP LAYER
120.0       INITIAL TEMPERATURE GUESS FOR PV CELL
120.0       INITIAL GUESS FOR BACK SURFACE TEMP.
135.0       REFERENCE TEMPERATURE OF PV CELL
185.0       MAXIMUM ALLOWABLE CELL TEMPERATURE
.9350       TRANSMISSIVITY OF COVER GLASS
.0650       ABSORBIVITY OF COVER GLASS
.5          CONDUCTIVITY OF COVER GLASS
.0200       TRANSMISSIVITY OF PV CELL
.9800       ABSORBIVITY OF PV CELL
1.0         CONDUCTIVITY OF PV CELL
.0200       TRANSMISSIVITY OF BACKING MATERIAL
.9800       ABSORBIVITY OF BACKING MATERIAL
130.0       CONDUCTIVITY OF BACKING MATERIAL
72.5        AMBIENT AIR TEMPERATURE
10.0        RELATIVE AIR HUMIDITY
1.3         WIND SPEED
0.00        CLOUD COVER
60.0        LATITUDE
.8750       PACKING FRACTION
.1085       CELL EFFICIENCY

```

OUTPUT LISTING

*****FLAT PLATE THERMAL ANALYSIS*****

NODE1 TEMPERATURE IS 144.6 DEGREES F.
NODE3 TEMPERATURE IS 149.1 DEGREES F.
NODE5 TEMPERATURE IS 149.1 DEGREES F.
POWER DISSIPATED DUE TO REVERSE BIAS IS 251.29 W/SQ-M
INSOLATION=1000W/SQ-M CELL EFFICIENCY=0
NODE1 TEMPERATURE IS 149.1 DEGREES F.
NODE3 TEMPERATURE IS 158.1 DEGREES F.
NODE5 TEMPERATURE IS 158.1 DEGREES F.
PV CELL IS SHADED ==> INSOLATION=0 CELL EFFICIENCY=0
NODE1 TEMPERATURE IS 97.4 DEGREES F.
NODE3 TEMPERATURE IS 99.8 DEGREES F.
NODE5 TEMPERATURE IS 99.8 DEGREES F.
POWER DISSIPATED DUE TO REVERSE BIAS IS 381.52 W/SQ-M
END OF FILE
?? _

STRUCTURAL

Concentrating Collector (Sample PVINP run has been included).

PVINP Example

THIS IS THE INPUT PRE-PROCESSOR FOR THE PVMOC PROGRAM. IT GENERATES THE INPUT FILE TAPE4 WHICH CONTAINS ALL NEEDED INPUTS FOR RUNNING ANY OR ALL OF THE FOLLOWING ANALYSES: THERMAL, ELECTRICAL, STRUCTURAL, ECONOMIC, AND CONDUCTOR REQUIREMENTS (METALIZATION).

IT MAY BE NECESSARY TO CONSULT MATERIALS MANUALS FOR CERTAIN PHYSICAL PROPERTIES OF MODULE MATERIALS. FOR THE USER'S CONVENIENCE, HOWEVER, SOME SUGGESTED VALUES ARE GIVEN. THESE VALUES MUST BE ENTERED BY THE USER.

THE USER WILL BE PROMPTED WITH A DESCRIPTION OF WHATEVER IS SUPPOSED TO BE ENTERED, THE UNITS OR OPTIONS, AND THE CORRECT INPUT FORMATS. INTEGERS MUST BE RIGHT JUSTIFIED! IN NOT, A 3 COULD BE READ AS 300!

```
ENTER DO YOU WISH TO RUN THERMAL ANALYSIS?           (Y OR N)  A1
? n
ENTER DO YOU WISH TO RUN ELECTRICAL ANALYSIS?         (Y OR N)  A1
? n
ENTER DO YOU WISH TO RUN STRUCTURAL ANALYSIS?         (Y OR N)  A1
? y
ENTER DO YOU WISH TO RUN ECONOMIC ANALYSIS?           (Y OR N)  A1
? n
ENTER DO YOU WISH TO STUDY CONDUCTOR REQUIREMENTS     (Y OR N)  A1
? n
```

*****STRUCTURAL ANALYSIS INPUTS*****

MATERIALS OR PHYSICAL METALLURGY HANDBOOK MAY BE NEEDED.

```
DO YOU WISH TO ENTER LENGTH & TEMPERATURE IN TERMS
OF          INCHES & DEGREES F          (ENTER 'IF')
OR          CENTIMETERS & DEGREES C     (ENTER 'CC')
A2
? if
ENTER MODULE PLATE LENGTH                     (INCHES)      F5.1
? 120.
ENTER MODULE PLATE WIDTH                     (INCHES)      F5.1
? 2.0
ENTER GLASS THICKNESS                       (INCHES)      F5.3
? 0.125
ENTER BACKING METAL THICKNESS                 (INCHES)      F5.3
IF BACKING METAL DOES NOT EXIST OR BACKING MATERIAL IS
  PLASTIC, ENTER 0.0 FOR THICKNESS.
? 0.83
ENTER COLLECTOR TYPE CONC OR FLAT PLATE       (CO OR FP)    A2
? conc
ENTER ARRAY TILT ANGLE FROM HORIZONTAL        (DEGREES)    F4.1
? 30.
```


INPUT (Continued)

ENTER YOUNGS MODULUS OF MODULE (PLATE) (PSI) F12.0
 ENTER 10000000. FOR ALUMINUM
 30700000. FOR STEEL
 10000000. IF MODULE HAS NO METAL BACKING
 ? 10000000.
 ENTER POISSONS RATIO OF MODULE (DIMENSIONLESS) F4.3
 ENTER 0.333 FOR DEFAULT.
 ? 0.33
 ENTER DESIGN LOAD
 ? 50.

TYPE 1-PCF

```

*****
*****
*****
**  **  **  **  **
**  **  **  **  **
**  **  **  **  **
  
```

TYPE 2-ACH

```

*****
*****
*
*
*
*****
*****
  
```

TYPE 3-ACL

```

*****
*
*
*
*
**
  
```

ENTER BEAM TYPE (PCF,ACH,ACL) (TYPE) I1
 PCF=PASSIVELY COOLED FINNED HEAT SINK=TYPE 1
 ACH=ACTIVELY COOLED HEAT SINK =TYPE 2
 ACL=ACTIVELY COOLED L.P.T. =TYPE 3
 ? 1

INPUT (Continued)

ENTER WIDTH OF PV CELL ASSEMBLY (INCHES) F4.2
 ? 1.8
 ENTER YOUNGS MODULUS OF HEAT SINK MATL (PSI) F12.0
 ? 10000000.
 ENTER IS THERE GLASS COATING ON CELL? (Y OR N) A1
 ? y
 ENTER YIELD STRENGTH OF HEAT SINK MATERIAL (PSI) F12.0
 ? 60000000.
 ENTER COMPRESSIVE STRENGTH OF PV MATERIAL (PSI) F12.0
 ? 45000000.
 ENTER MAXIMUM ALLOWABLE DEFLECTION FROM FOCUS (INCHES) F4.3
 ? 0.75
 ENTER LOAD (UNIFORM=LOAD/ASSY LENGTH) (PSI) F4.1
 FOR EXAMPLE, A TEN FOOT BEAM LOADED WITH 100 POUNDS
 WOULD BE 10 PSF OR 0.8 PSI
 ? 0.65
 ENTER ASSEMBLY (BEAM) LENGTH BETWEEN SUPPORTS (INCHES) F5.1
 ? 120.
 ENTER HEAT SINK MATERIAL YIELD STRESS (PSI) F12.0
 ? 60000000.
 ENTER COMPRESSIVE STRENGTH OF MATERIAL OR BOND (PSI) F12.0
 ? 45000000.
 ENTER INSIDE CHANNEL HEIGHT (INCHES) F6.3
 ? 0.5
 ENTER NUMBER OF FINS (NUMBER) I3
 ? 10
 ENTER FIN LENGTH (INCHES) F4.1
 ? 0.4
 ENTER FIN LENGTH (INCHES) F6.3
 ? 0.04
 ENTER BEAM THICKNESS (INCHES) F6.3
 ? 0.083
 ENTER BEAM WIDTH (INCHES) F6.3
 ? 2.0
 READY.

INPUT FILE

```

10          NUMBER OF FINS
.4          FIN LENGTH
.040       FIN WIDTH
.083       BEAM THICKNESS
2.000     BEAM WIDTH
END OF FILE
?? 1/beam th/
.083       BEAM THICKNESS
?? c/083/208/
.208       BEAM THICKNESS
?? t
?? p*
00100      THERMAL,ELECTRICAL,STRUCTURAL,COST,METALIZATION

          *****STRUCTURAL ANALYSIS INPUTS*****
120.0  2.0  .083      MODULE LENGTH,WIDTH,THICKNESS
.125      GLASS THICKNESS
CO        COLLECTOR TYPE CONC OR FLAT PLATE
30.0      ARRAY TILT ANGLE FROM HORIZONTAL
10000000. YOUNGS MODULUS OF MODULE
.330      POISSONS RATIO
50.0      DESIGN RATIO
1         BEAM TYPE (PCF,ACH,ACL)
1.80      WIDTH OF PV CELL ASSEMBLY
10000000. YOUNGS MODULUS OF HEAT SINK MATL
Y         IS THERE GLASS COATING ON CELL?
60000000. YIELD STRENGTH OF HEAT SINK MATERIAL
45000000. COMPRESSIVE STRENGTH OF PV MATERIAL
.750      MAXIMUM ALLOWABLE DEFLECTION
.7         LOAD (UNIFORM=LOAD/ASSY LENGTH)
120.0     ASSEMBLY LENGTH
60000000. HEAT SINK MATERIAL YIELD STRESS
45000000. COMPRESSIVE STRENGTH OF MATERIAL OR BOND
.500      INSIDE CHANNEL HEIGHT
10        NUMBER OF FINS
.4        FIN LENGTH
.040     FIN WIDTH
.208     BEAM THICKNESS
2.000    BEAM WIDTH
END OF FILE
?? _

```

OUTPUT LISTING

*****STRUCTURAL ANALYSIS*****

RESULTS FOR CONCENTRATING COLLECTOR

STRUCTURAL ANALYSIS COMPLETE.

PASSIVE FINNED HEAT SINK PASSED WITH FOLLOWING CONSTRAINTS:

DISTANCE BETWEEN SUPPORTS:	120.00 INCHES.
TENSILE STRESS IN BEAM:	102.0 PSI.
MAXIMUM ALLOWABLE TENSILE STRESS:	.600E+08 PSI.
ACTUAL BEAM DEFLECTION:	.028 INCHES.

FLAT PLATE STRUCTURAL ANALYSIS

Note that on the next page, by changing the module width from 11.8 inches to 11.9 inches in the input file, the fatal error shown was corrected.

INPUT FILE

00100 THERMAL,ELECTRICAL,STRUCTURAL,COST,METALIZATION

*****STRUCTURAL ANALYSIS INPUTS*****

47.5 11.8 .083 MODULE LENGTH,WIDTH,THICKNESS
.125 GLASS THICKNESS
FP COLLECTOR TYPE CONC OR FLAT PLATE
30.0 ARRAY TILT ANGLE FROM HORIZONTAL
10000000. YOUNGS MODULUS OF MODULE
.330 POISSONS RATIO
50.0 DESIGN LOAD
4.0 WIND LOAD
2.1 DEADWEIGHT LOAD
N IS STRESS CYCLE CURVE AVAILABLE?
AL METAL SUBSTRATE MATERIAL
200000000. METAL ULTIMATE STRENGTH (YIELD STRESS)
4 TYPE OF GLASS
M WINDLOAD DURATION UNITS S,M,D,W,T,Y
5 LOAD DURATION IN ABOVE UNITS
Y DEADWEIGHT LOAD DURATION UNITS
20 DEADWEIGHT LOAD DURATION IN ABOVE UNITS
.15 PROBABILITY OF FAILURE (<30%)
END OF FILE
?? e
TAPE4 IS A LOCAL FILE

READY.

OUTPUT LISTING

*****STRUCTURAL ANALYSIS

RESULTS FOR FLAT PLATE COLLECTOR

***FATAL ERROR *** ASPECT RATIO OF MODULE (4.03) > 4.0

CANNOT INTERPOLATE SIF.

END OF FILE

?? e

TAPE6 IS A LOCAL FILE

READY.

xedit,tape4

XEDIT 3.1.00

?? c/11.8/11.9/

47.5 11.9 .083 MODULE LENGTH,WIDTH,THICKNESS

?? e

TAPE4 IS A LOCAL FILE

READY.

replace,tape4

READY.

call,pvjcl

READY.

xedit,tape6

XEDIT 3.1.00

?? p*

*****STRUCTURAL ANALYSIS*****

RESULTS FOR FLAT PLATE COLLECTOR

MAXIMUM ALLOWABLE STRESS FOR METAL PLATE IS .16E+08 PSI

STRESS FOR DEADWEIGHT LOAD IS .504E+03 PSI

STRESS FOR THE WIND LOAD IS .504E+03 PSI

BREAKING STRESS DUE TO DEADWEIGHT IS .164E+05 PSI

BREAKING STRESS DUE TO WIND LOAD IS .191E+05 PSI

MAXIMUM COMBINED PRINCIPAL STRESS IS .101E+04 PSI

GLASS THICKNESS ADEQUATE ACCORDING TO ANALYSIS

TWISTING LOAD ANALYSIS

MODULE PASSES TWISTING TEST.

HAIL IMPACT ANALYSIS

GLASS WILL WITHSTAND HAIL IMPACT.

END OF FILE

ECONOMIC

Three process analysis. These process costs are strawman values only and do not represent real manufacturing costs.

INPUT FILE

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01000      THERMAL,ELECTRICAL,STRUCTURAL,COST,METALIZATION
          *****ECONOMIC ANALYSIS INPUTS*****
3          NUMBER OF MANUFACTURING PROCESSES
.105      PV CELL EFFICIENCY
.925      MODULE PACKING FRACTION
TESTING   PROCESS DESCRIPTION
.900      PROCESS DUTY CYCLE
60.00000  YIELDED PROCESS OUTPUT RATE
          2.50000  OUTPUT UNIT SIZE IN SQ-METERS
.95000    PROCESS YIELD
          0.0000  EQUIPMENT COST DATA COST( 1)
12        EQUIPMENT LIFETIME FOR PROCESS 1
          1200.0000 PROCESS FLOOR SPACE FOR PROCESS 1
          1500.0000 LABOR FOR PROCESS 1
          130.0000  MATERIALS AND SUPPLIES FOR PROCESS 1
          500.0000  UTILITIES COST FOR PROCESS 1
CONSTRUCT PROCESS DESCRIPTION
.890      PROCESS DUTY CYCLE
15.52000  YIELDED PROCESS OUTPUT RATE
          2.00000  OUTPUT UNIT SIZE IN SQ-METERS
.86000    PROCESS YIELD
1200000.0000 EQUIPMENT COST DATA COST( 2)
6         EQUIPMENT LIFETIME FOR PROCESS 2
          750.0000  PROCESS FLOOR SPACE FOR PROCESS 2
          600.0000  LABOR FOR PROCESS 2
          1200.0000 MATERIALS AND SUPPLIES FOR PROCESS 2
          400.0000  UTILITIES COST FOR PROCESS 2
DESIGN    PROCESS DESCRIPTION
1.000     PROCESS DUTY CYCLE
13.7      YIELDED PROCESS OUTPUT RATE
          2.00000  OUTPUT UNIT SIZE IN SQ-METERS
.99990    PROCESS YIELD
24800.0000 EQUIPMENT COST DATA COST( 3)
00        EQUIPMENT LIFETIME FOR PROCESS 3
          400.0000  PROCESS FLOOR SPACE FOR PROCESS 3
          400.0000  LABOR FOR PROCESS 3
          450.0000  MATERIALS AND SUPPLIES FOR PROCESS 3
          500.0000  UTILITIES COST FOR PROCESS 3
END OF FILE
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OUTPUT LISTING

*****ECONOMIC ANALYSIS*****

PROCESS	EQPT	SQFT	DLAB	MATS	UTIL	TOTAL	PROCESS YIELD	CUMULT. YIELD	EFFECTIVE COST/SQ-M	CUMULT. COST
TESTING	0.0000	.0018	.0003	1.0400	4.0000	5.0421	.9500	.9500	5.307	5.307
CONSTRUCT	.0471	.0056	.0005	46.3918	15.4639	61.9090	.8600	.8170	75.776	81.083
DESIGN	.0014	.0030	.0004	19.7080	21.8978	41.6107	.9999	.8169	50.936	132.020

TOTAL PRODUCTION COST = 1.36 \$/PW