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# AUTOMATED ARRAY ASSEMBLY. PHASE 2

Quarterly Technical Progress Report, April—June 1979

By
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July 1979

Work Performed Under Contract No. NAS-7-100-954881

Texas Instruments, Incorporated
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# SECTION I

# INTRODUCTION

The Automated Array Assembly Task, Phase 2 of the Low Cost Solar Array (LSA) Project is a process development task. This contract provides for the fabrication of modules from large area Tandem Junction Cells (TJC). The key activities in this contract effort are a) Large Area TJC including cell design, process verification and cell fabrication and b) Tandem Junction Module (TJM) including definition of the cell-module interfaces, substrate fabrication, interconnect fabrication and module assembly. The overall goal is to advance solar cell module process technology to meet the 1986 goal of a production capability of 500 megawatts per year at a cost of less than $500 per peak kilowatt. This contract will focus on the Tandem Junction Module process.

During this quarter, effort was focused on design and process verification. The large area TJC design was completed and the design verification was completed. Process variation experiments led to refinements in the baseline TJC process. Formed steel substrates were porcelainized. Cell array assembly techniques using infrared soldering are being checked out. Dummy cell arrays up to 5 cell by 5 cell have been assembled using all backside contacts.

## SECTION II

## TECHNICAL DISCUSSION

Both major task areas are in progress. A brief description of the activities in each area follows.

I. Large Area Tandem Junction Cell

1. Cell Design

The photomasks for the large area TJC were received. The mask registration was checked by printing level 1 and etching an oxide layer (N+ diffusion area) then printing level 2 and etching the remaining oxide layer (P+ contact area). Level 3 (metal contacts) was developed in the photoresist over levels 1 & 2 but not etched. Level 4 (matal pattern) was developed in the photoresist over the etched patterns of levels 1 & 2 but not etched.

Levels 2,3, & 4 overlay with virtually no mismatch (well within the normal tolerance of 0.1 mil). The overlay of level 1 to level 2, however, shows a mismatch across the cell of approximately 0.5 mil ($1.27 \times 10^{-3}$ cm). The minimum N+ to P+ design spacing is 1.0 mil ($2.54 \times 10^{-3}$cm) and this mismatch could lead to yield problems.

The level 1 mask was refabricated eliminating the level 1 to level 2 mismatch. Contact print of level 1 and level 2 now exhibit the correct N+ to P+ spacing of 1.0 mil ($2.54 \times 10^{-3}$cm). This activity is now complete.

2. Process Verification

Two Czochralski (Cz) grown crystals were used to check minority carrier lifetime after a steam oxidation and again after a $POCl_3$ diffusion at 850°C.

Two slices from each crystal were oxidized in steam at 850°C the oxide was stripped and the lifetime was measured using the surface photovoltage (SPV) technique. The slices were then coated on one side with a low temperature plasma deposited silicon oxide and the other side was phosphorous diffused at 850°C for 60 minutes. The oxide was removed and the SPV lifetime measurement was repeated. Two fresh slices from each Cz crystal were coated on one side with plasma deposited silicon oxide and subjected to the same phosphorous diffusion conditions. The oxide was removed and the SPV lifetime measurement was made. The results are tabulated in Table 1.

TABLE I. PROCESS LIFETIME MEASUREMENTS

| Crystal | Lifetime After Steam Oxidation | Lifetime After $POCl_3$ Diffusion (μsec) |
|---|---|---|
| 548 | 6 - 8.5 | 24 - 27 |
| 548 | No Oxidation | 28 |
| 549 | 7.5 - 16 | 33 - 42 |
| 549 | No Oxidation | 45 - 50 |

The data suggests that while a steam oxidation degrades minority carrier lifetime, a subsequent phosphorous diffusion provides a gettering effect that substantially recovers the lifetime. The conclusion from this data is that any process sequence that uses a steam oxidation step must follow the steam oxidation with a phosphorous diffusion step to retain minority carrier lifetime for solar cell operation.

Contact resistivity to a P+ region formed by alloying evaporated Al at 850 C for thirty (30) minutes was rechecked using the concentric ring test pattern described earlier. Contact resistivity between the alloyed region and evaporated Ti-Pd-Ag metallization is in the range of $7 \times 10^{-4}$ $\Omega$-cm$^2$ without sintering. Sintering at 450$^0$C does not improve contact resistivity.

Process variation test runs were completed on three groups. A baseline group ($1 \times 10^{14}$ atom/cm$^2$ B implant, 850$^0$C $POCl_3$ diffusion), lot AAAP-II-107; a reduced implant group ($5 \times 10^{13}$ atom/cm$^2$ B implant, 850$^0$C $POCl_3$ diffusion), lot AAAP-II-108; lot AAAP-II-108; and a high temperature phosphorous diffusion group ($1 \times 10^{14}$ atom/cm$^2$ B implant, 1000$^0$C $POCl_3$ diffusion). Each group contained 100μm and 150μm thick wafers. The 2 X 2 cm cells were attached to gold ribbon tabs and measured at AM1. The results are shown in Table 2.

TABLE 2. PROCESS VARIATION PHOTORESPONSE

| Lot No. | Thickness (μm) | $V_{oc}$ (V) | $J_{sc}$ (mA/cm$^2$) |
|---|---|---|---|
| AAAP-II-107 | 100 | .575 | 26 |
| | 150 | .575 | 27 |
| AAAP-II-108 | 100 | .577 | 31 |
| | 150 | .52 | 10 |
| AAAP-II-109 | 100 | .50 | ~10 |
| | 150 | .50 | ~10 |

The baseline process lot AAAP-II-107 results are typical for this modest lifetime crystal. The equivalent results for both thicknesses are encouraging. The reduced implant process, lot AAAP-II-108, is also encouraging at 100μm thickness. The optimum implant dose has a fairly broad range, $5 \times 10^{12}$ -- $1 \times 10^{14}$ atom/cm$^2$. The high temperature phosphorous diffusion process, lot AAAP-II-109, is not acceptable and apparently the high temperature causes lifetime degradation.

During this quarter it was noticed that $V_{oc}$ values after mounting for test were lower than anticipated, see Table 2. A careful evaluation of the "tail end" mounting process sequence, strip front side process oxide, deposit AR coating, saw, gold tab bond, showed that the gold tab mounting process was causing a degradation in the cell photoresponse. The saw and gold tab bonding process are carried out in a separate facility as a service to this program. Careful checking of recent history showed that a change had been made in the routine gold bonding proceedure several months ago. The bonding pressure had been increased significantly to improve bond strength on ICs. One wafer, containing two 2 X 2 cm cells was carefully monitored through the process to verify that the increased bonding pressure was the culprit. The front oxide strip, AR deposition steps were replaced by a thinning of the front oxide to eliminate the possibility of photoresponse degradation, increased surface recombination, while the front surface was bare. Data on the 150μm thick wafer from lot AAAP-II-116 is shown in Table 3. Prior to gold tab bonding all measurements are made with backside illumination (it is not convenient to make front side illumination measurements on a TJC without bond tabs) under an AM1 source (ELH lamp).

TABLE 3. Photoresponse During Assembly for Test

| Assembly Process Step | Illumination Side | 12 Finger TJC $V_{OC}$ (mV) | 12 Finger TJC $I_{SC}$ (mA) | 16 Finger TJC $V_{OC}$ (mV) | 16 Finger TJC $I_{SC}$ (mA) |
|---|---|---|---|---|---|
| Before Saw | Back | 589 | 94 | 588 | 87 |
| After Saw | Back | 587 | 86 | 585 | 79 |
| After Bond | Back | 576 | 80 | 576 | 74 |
| After Bond | Front | 586 | 130 | 589 | 128 |

The drop in $I_{SC}$ after saw is due to the elimination of lateral collection from areas external to the cell, this is expected. After bond, both $V_{OC}$ and $I_{SC}$ show significant degradation. This degradation is attributed to damage generated in the diffused region under the bond. This effect is of no concern in the proposed module assembly scheme since reflow solder bonding will be used to assembly the modules. Reverse leakage across the collector-base junction at 1 volt did not change during the assembly for test process.

TJC's from lots AAAP-II-113 and -116 were assembled using a low pressure gold tab bonding process. Photoresponse was measured under an AM1 source (ELH lamp) using front illumination. The data on three cells from each lot is shown in Table 4. The increase in $V_{OC}$ and $I_{SC}$ for lot AAAP-II-116 is evident (compare to bottom line of Table 3).

TABLE 4. Photoresponse with Corrected Gold Tab Bond Process

| Lot No. | Al Alloy temp ( C) | $V_{OC}$ (V) | $I_{SC}$ (mA) | $J_{SC}$ (mA/cm$^2$) |
|---|---|---|---|---|
| AAAP-II-113 | 650 | .590 | 136 | 34 |
| AAAP-II-116 | 850 | .599 | 142 | 36 |

Five process variation test lots were completed through backside illumination testing. These process variations and back side photoresponse measurements are summarized in Table 5. Several useful correlations can be made from this and earlier data.

TABLE 5. Process Variation Test Runs

| Lot Number | No. | Crystal Type | Res (Ω-cm) | Thickness (μm) | Back Illumination $V_{OC}$ (v) | Back Illumination $I_{SC}$ (mA) | Process Variation |
|---|---|---|---|---|---|---|---|
| AAAP-II-113 | 452 | 2"Cz | 6 | 100,150 | .588* | 89* | Deep Front N+ |
| AAAP-II-113A | 348 | 3"Fz | 10 | 150 | .573-.579† | 105-120† | Baseline |
| AAAP-II-114 | 348 | 3"Fz | 10 | 150 | .578-.581† | 96-107† | 1000°C Oxidation |
| AAAP-II-115 | 348 | 3"Fz | 10 | 150 | .571-.576† | 104-116† | Silane Oxide |
| AAAP-II-116 | 348 | 3"Fz | 10 | 100,125,150 | .595-.599† | 107-115† | 850°C Al Alloy |

* AM1 Illumination
† W-lamp

Lot AAAP-II-113 - the deep front N+ diffusion, ~0.5 - 0.6μm, does not severely impace current collection during back illumination. This effect was checked using front illumination, see Table 4, confirming the transistor model proposed earlier for the TJC.

Lots AAAP-II-113A, - 114 and -115, variations in the first oxidation process step, have only second order effects on photoresponse. In particular, the 1000°C dry $O_2$ oxidation does not exhibit any marked reduction in lifetime when followed by an 850°C phosphorous diffusion. The low temperature, 450°C, silane deposition does not offer any marked advantage.

Lot AAAP-II-116 - the increase in the Al alloy process step from 650°C to 850°C appears to offer a significant improvement in the baseline process.

The process variation data reported above coupled with earlier reported process variation data gives the outline for an updated baseline process relative to each of the high temperature operations. The optimal conditions for each critical process step are outlined below.

- Back side boron implant dose - $5 \times 10^{13}$ to $1 \times 10^{14}$ atom/cm$^2$ at 35KeV
- First oxidation - 850°C steam oxidation will be retained but the upper temperature limit could be raised if it offered a processing advantage so long as the oxidation is followed by a phosphorous diffusion.
- Phosphorous diffusion - 850°C appears to be near optimum, 950°C causes a marked loss in collection efficiency. The depth of the front N+ diffusion up to ~0.6μm does not appear to have a significant effect. This latter statement is still subject to verification using front illumination.

- Al alloy - An 850°C alloy process step appears to offer significantly better response than a 650°C alloy. This effect is probably due to improved electrical activation of the alloyed Al atoms.

Lots AAAP-II-113A, -114, -115 and -116 were all run using 3" (7.62 cm) wafers. No particular handling or breakage problems have been observed. The 150μm thick wafers are somewhat less fragile than the 100μm thick wafers.

3. Design Verification

Mask overlay registration has been verified and no mechanical or geometry problems remain. Process check out has been completed. Large area cells, 6.2 X 6.2cm, from lot AAAP-II-120 were back side probed after metallization definition. Initial measurements give $I_{SC}$> 0.6A and $V_{OC}$ ~0.55v. Since over 50% of the back is covered by metal, the expected $I_{SC}$ for front illumination is>1A. The design verification is complete.

4. Cell Fabrication

Fabrication of 6.2 X 6.2cm TJCs to populate minimodules has been started. Initial cells are at metal plating.

II. TANDEM JUNCTION MODULES

1. Define Cell - Module

Complete

2. Modify Tooling

Complete

3. Define Heat Treatment

Formed steel substrates were stress relieved at 600 F (316 C). Ten (10) formed substrates at each of two gauges (0.091 cm and 0.076 cm) were heat treated and ten (10) formed substrates from each gauge were not heat treated. After porcelainizing, the substrates were measured for bow. The measurements are given in Table 6. Heat treatment at 600 F has no significant effect on bowing of the formed substrates during the porcelainizing operation. Thickness or gauge of the formed substrate does not appear to be a significant factor.

TABLE 6. Heat Treatment Results

| Substrate Number | Heat Treat | Gauge (cm) | Convex Bow | |
|---|---|---|---|---|
| | | | Avg. (cm) | Range-Min-Max (cm) |
| 1-10 | No | 0.091 | .181 | 0.152-0.889 |
| 11-20 | Yes | 0.091 | .150 | 0.127-1.09 |
| 51-60 | No | 0.076 | .141 | 0.127-0.686 |
| 61-70 | Yes | 0.076 | .163 | 0.064-0.828 |

Post porcelainized heat treatments are being checked on some of the extra samples.

4. Porcelainized Substrate

As reported above, all substrates exhibited some bow. A fixture was built to attempt a straightening operation after porcelainizing. See figures 1 and 2.

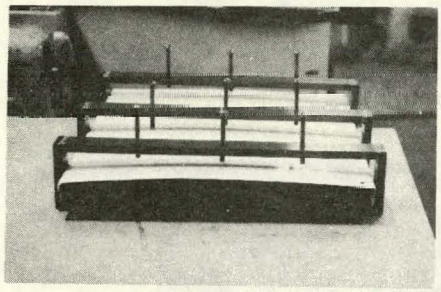

Figure 1

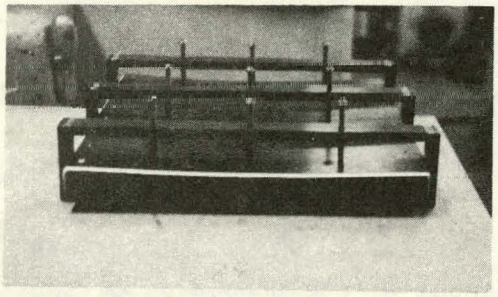

Figure 2

Figure 1 shows the substrate in the fixture before reversing the bow. Figure 2 shows the substrate with the bow reversed prior to heat treating. Preliminary tests indicate that a low temperature-time heat treat reduces the bow.

5. Design and Form Bus Bars

Copper clad Invar bus bar material has been completely processed to the required dimensions for minimodule assembly. The bus bar material will be pre tinned before assembly of the cell matrix.

6. Solder Fixture

A soldering fixture was completed which could accommodate up to a 5 x 6 matrix. It is basically a vacuum chuck on which the cells are positioned. The vacuum chuck is supported by a hot plate which pre-heats the chuck to minimize heat sinking, see Figures 3 and 4.

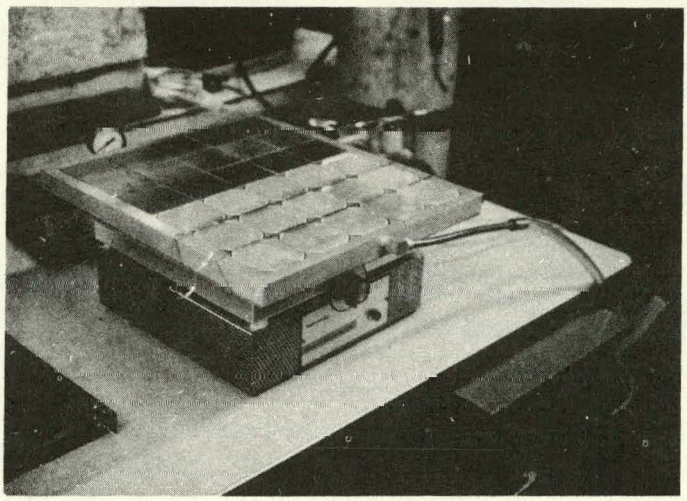

Figure 3. Vacuum Chuck with
3 x 5 Cell Matrix

Figure 4. Vacuum Chuck with
3 x 5 Cell Matrix

7. Assemble Cell Matrix

Infrared soldering was first successfully demonstrated on a one-cell and a two-cell string of dummy cells. The dummy cells contain the correct metallization pattern but are not electrically active.

Using dummy cells a 3 x 5 cell matrix and 5 x 5 cell matrix were assembled to check out the assembly technique. The two parallel-series cell matrices are shown in Figures 5 and 6. The excellent cell nesting efficiency is evident in these figures.

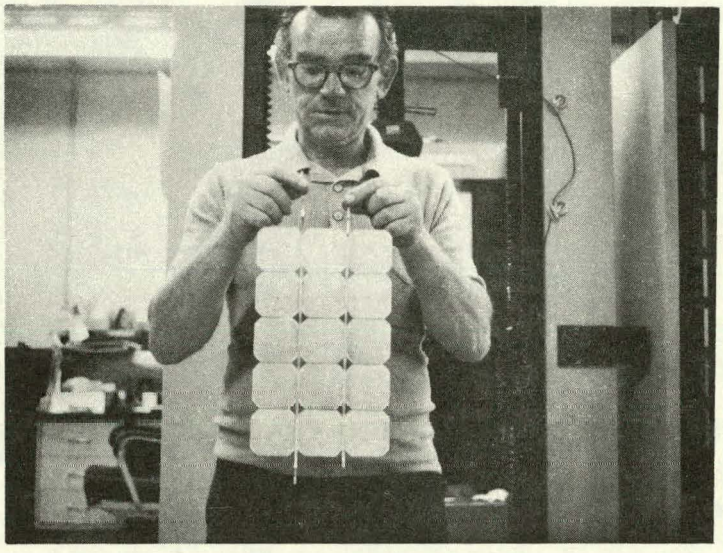

Figure 5. 3 x 5 Cell Matrix

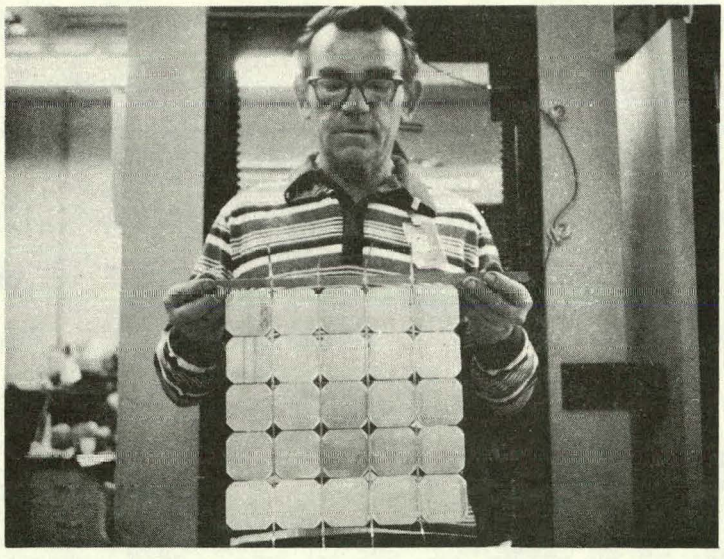

Figure 6. 5 x 5 Cell Matrix

## SECTION III

## CONCLUSIONS AND RECOMMENDATIONS

- Any process sequence that uses a steam oxidation step must follow the steam oxidation with a phosphorous diffusion step to retain minority carrier lifetime for solar cell operation.
- High temperature ($\geq 1000^{0}C$) phosphorous diffusions degrade solar cell performance.
- Thermocompression bonding directly over the N+/P junction must be carefully controlled to avoid photoresponse degradation.

## SECTION IV

## NEW TECHNOLOGY

No areas of new technology were identified this quarter.

# SECTION V

# PROGRAM SUMMARY

Figure 7 shows the current work plan status. All scheduled activities are in process. No problems are apparent at present that will prevent attaining the indicated milestones.

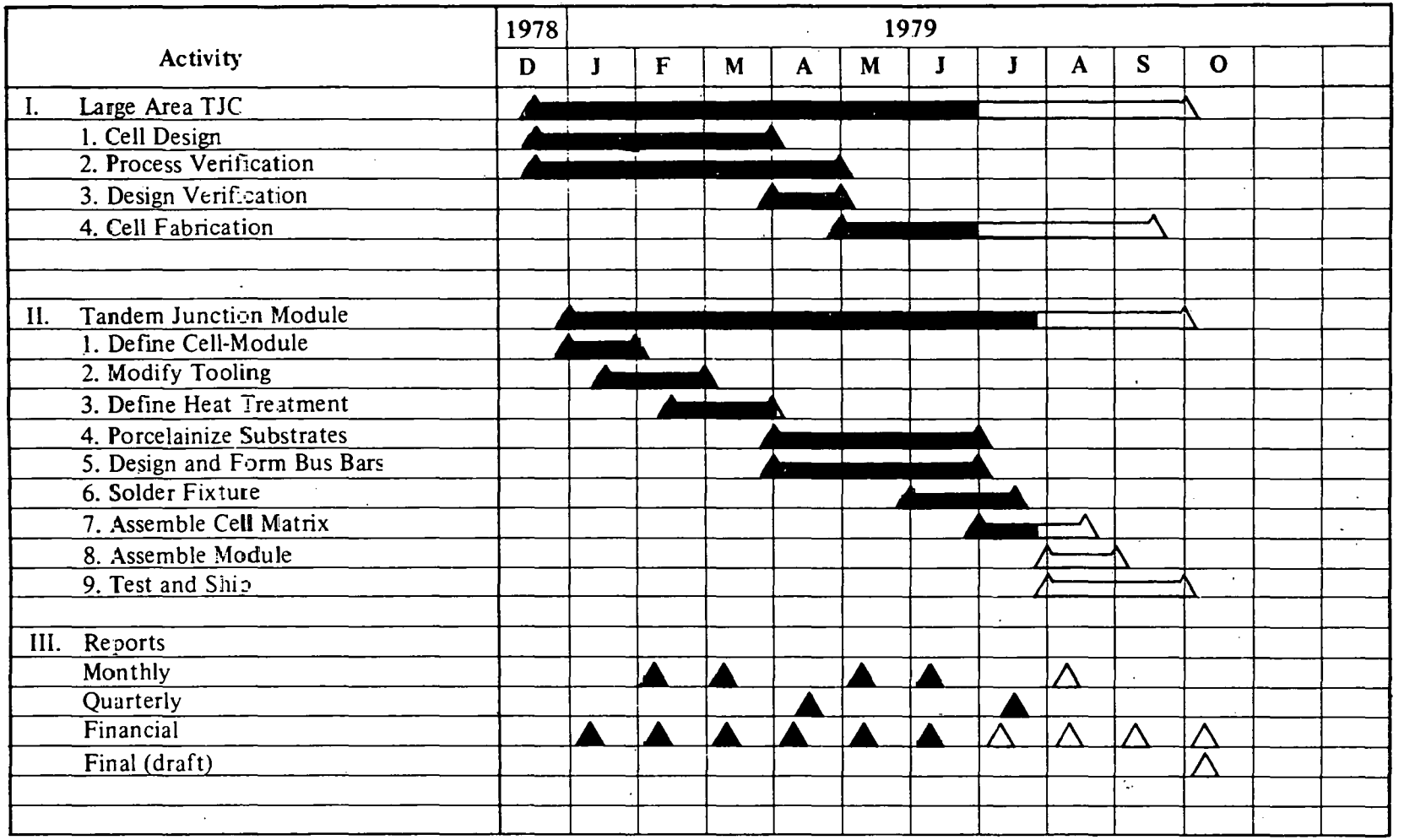


FIGURE 7. WORK PLAN STATUS



*U.S. GOVERNMENT PRINTING OFFICE: 1979-640-258-1505